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# Inkjet patterned anodic aluminum oxide for rear metal contacts of silicon solar cells

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# Abstract

Local rear metal contacting through passivating dielectric layers has the ability to increase silicon solar cell efficiencies to over 20%. To-date most contact schemes have involved the formation of localised aluminium-alloyed regions through patterned  $AlO_x$  or  $SiN_x$  passivating layers. Recently electrochemically-formed anodic aluminium oxide (AAO) layers have been shown to enhance minority carrier lifetimes of phosphorus–diffused p-type CZ wafers when formed over an intervening layer of  $SiO_2$  or  $SiN_x$ , suggesting that these layers may find applications as passivation layers for cells. We report here on the inkjet patterning of AAO layers formed over a thermally-grown thin oxide layer on p-type silicon surfaces. The process, which involves the inkjet printing of 50% (w/w) phosphoric acid, was used to form well-resolved arrays of holes with a diameter as small as 20-40  $\mu$ m in the dielectric stack. Alloying of aluminium, which was evaporated over the patterned dielectric stack, resulted in the formation of localised back surface field (BSF) regions having a thickness up to 8  $\mu$ m. Future work will focus on adapting this process for use in local rear metal contacting of silicon solar cells.

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Keywords: Inkjet patterning; Anodic aluminium oxide; rear contact; local back surface field.

# 1. Introduction

Most reported rear localised aluminium-alloyed metal contacting schemes for silicon solar cells have employed laser ablation [1-4], laser doping [5-8] or the use of etching pastes [9] to pattern a dielectric layer before the aluminium alloying process. However, very few silicon solar cell manufacturing companies have committed to volume production of these localised rear contact cells, thus raising

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questions about the ability to pattern the dielectric layers in a cost-effective way at high throughput. Furthermore the continued reliance on screen printing and its associated issues of wafer bowing and high paste costs limit the adoption of these local contacting methods for use with emerging thin silicon technologies [10].

Electrochemically formed anodic aluminium oxide (AAO) is a potentially low-cost dielectric which may also provide a valuable template for novel light trapping structures for thin silicon cells in the future [11]. The layers have been shown to enhance minority carrier lifetimes of phosphorus–diffused p-type CZ wafers when formed over an intervening layer of  $SiO_2$  or  $SiN_x$  [12, 13]. In this paper, we report on the inkjet patterning of these layers, when formed over a thin  $SiO_2$  layer, to form well-resolved arrays of holes with a diameter as small as 20  $\mu$ m in the dielectric stack. Furthermore, after alloying of evaporated aluminium, it is shown that local BSF regions having a thickness approaching 8 um can be formed through the point contact openings.

## 2. Experimental

The inkjet patterning experiments were performed using: (i) 240  $\mu$ m thick polished 10  $\Omega$  cm p-type Cz silicon wafers; and (ii) 200  $\mu$ m thick alkaline-textured 1-3  $\Omega$  cm p-type Cz silicon wafers. Half of the textured wafers underwent a 7 min saw damage etch in 25% (w/v) NaOH at 80 ± 2 °C to simulate a rearetched surface. A 15 nm thin SiO<sub>2</sub> layer was thermally-grown on both surfaces of all wafers. This layer acted as an effective barrier layer to prevent anodisation of the silicon substrate when the aluminium layer was fully anodised [14]. A 600 nm aluminium layer was then thermally-evaporated on to one side of the wafers, followed by anodisation under 25 V DC bias in the electrolyte containing 0.5 M H<sub>2</sub>SO<sub>4</sub>.

A 50% (w/w) H<sub>3</sub>PO<sub>4</sub> solution was inkjet-printed using a FUJIFILM Dimatix Materials Printer (DMP-2831), which utilized piezoelectric silicon MEMS DMC-11601 ink cartridge with 16 nozzles, with each nozzle having a nominal drop volume of 1 pL. Printing was performed at 5 kHz, and the voltage was varied between 11.2-12.8 V. These settings were selected in order to maintain a drop velocity of 10 m/s using the DMP tool's drop watcher application. A single nozzle was used for each printing process to improve the accuracy of alignment between printed layers. The platen temperature during printing was varied between 30 °C and 60 °C to ascertain the effect of varying substrate temperature on the AAO etching process. However, the heat from the platen affected the cartridge temperature, therefore the cartridge temperature was set at 30 °C to mitigate the temperature variation of the ink during the printing. Following the printing, the wafers remained on the heated platen for varying durations to facilitate the etching process. Wafers were then rinsed in deionized water (~18 M $\Omega$ ·cm) and visually inspected. The etching process was characterised using optical microscopy, atomic force microscopy (AFM) and scanning electron microscopy (SEM). Etched hole arrays were achieved by increasing the drop spacing applied to a pattern of lines. Larger drop spacing enables fast printing speeds over each printed line. In this work, the typical test pattern consisted of a 2 cm  $\times$  2 cm array of points (or holes) with 250  $\mu$ m spacing.

After having established a repeatable process to create point openings in the AAO by inkjet printing, wafers with a planarised surface were prepared and used to investigate the contact formation after aluminium alloying. The wafers were inkjet-patterned using printing conditions found to be optimal in the initial patterning experiments using polished wafers. The platen temperature was set to 60 °C and cartridge temperature to 30 °C. Nozzle voltage and jetting frequency were set to 11.4 V and 5 kHz accordingly. Point openings were formed by printing 8 layers of 50% (w/w)  $H_3PO_4$  with a 1 pL ink

cartridge and etching for 45 min on the platen. After patterning, a capping layer of 2  $\mu$ m aluminium was thermally-evaporated onto the patterned AAO, followed by firing in a Centrotherm belt furnace at 850 °C with 4800 mm/min belt speed. This corresponded to the wafers being exposed to the peak firing temperature for duration of 5 sec. For all wafers, the local back surface field (BSF) regions were exposed by laser cleaving from the front (i.e., non-aluminium) surface and etched for 20 sec in an CH<sub>3</sub>COOH:HNO<sub>3</sub>:HF (6:3:1) solution which etches heavily-doped p+ silicon at a much faster rate than lightly-doped silicon. The wafer cross sections were then imaged by SEM to visualise the formed p+ BSF regions and to estimate their depth and uniformity.

# 3. Inkjet patterning results

#### 3.1. Effect of etchant volume and etching duration

The amount of etchant deposited was directly related to the number of layers printed. To increase the etching duration, after printing the samples were left on the 60°C heated platen for varying periods of time. The etching duration was assumed to start when the first droplets were fired and to end when the samples were removed from the platen. After rinsing, the samples were observed under an optical microscope to measure the hole diameter and assess the depth, or extent, of etching.

Table 1 shows the relationship between the etched hole diameter and the amount of AAO etched for a polished wafer surface. As fewer layers were printed, which corresponded to less etchant being deposited, the extent or depth of etching was reduced as evidenced by AAO remaining visible in the regions where etchant was deposited. Furthermore, as the number of layers decreased, the diameter of the holes was also reduced. This is because of the etchant typically spreads as more layers are applied to the same location. The diameter of the hole openings was also impacted by the drop placement accuracy. Misaligned droplets increased the area exposed to etchant and hence the opening diameter. Such misaligned droplets are clearly evident in the optical images from samples etched for 45 mins in Table 1. Clearly good alignment between printed layers is important for the etching of small clearly defined holes. The drop placement accuracy for the DMP-2831 is specified as  $\pm 25 \ \mu m \ [15]$  which is less than many other available inkjet printing devices.

Increased etching duration resulted in an increased depth of AAO etching for a given number of layers but did not appear to increase the etched hole diameter. Longer etching durations did not appear to increase the etched hole diameter. This would suggest that the spreading of the etchant, which occurred as increased layers were printed, had a more significant effect on the diameter of the etched holes than the time over which etching occurred.

# 3.2. Effect of etching temperature

The temperature of the samples during printing was varied to ascertain the effect of temperature on the etch rate. In initial experiments, samples were heated in a pre-heated oven for 15 min at 160 °C following deposition of etchant, however only partial etching was observed in these experiments. It was concluded that this was due to excessive evaporation of the water in the deposited etchant solution. In subsequent experiments, the effect of temperature was ascertained by varying the printer platen temperature and leaving samples on the platen for different durations as described in Section 2. Three different platen temperatures were tested: 30 °C, 60 °C and 75 °C. Optical images of selected holes from wafers etched at these different temperatures are shown in Table 2.

From Table 2 it is clear that as the platen temperature was increased from 30 °C to 60 °C given the same etching duration and number of printed layers, the etching rate increased significantly and more of

the AAO was etched in the hole regions. The effect of temperature appeared to be more critical than that of etching time and suggests that use of a higher platen temperature can be used to offset the requirement for a longer etching duration. However there is a limit to the extent that the etching process can be accelerated through increased platen temperature. Further increases in temperature above 60 °C appeared not to increase etching rate most likely due to enhanced evaporation of water from the deposited etchant solution. Samples etched at 75 °C exhibited 'rings' of graduated etching with the most-etched regions occurring in the centre. This etching pattern is consistent with water evaporating at the perimeter of the printed droplet and causing the circumference of the etched droplet to decrease as etching proceeds leaving partially etched regions at the perimeter of the area wetted by the deposited drops. The result is conical etch profiles in the AAO layer with a smaller central hole diameter.

Table 1. Effect of etching duration on the depth of etching and etched -hole diameter (d), for different numbers of printed layers of etchant. The platen temperature was set to 60 °C for all experiments. Etched-hole diameters represent the mean of 3 individual measurements.



The appearance of clearly defined rings appearing in the etched opening profile as the etch temperature increased was also noted by Lennon et al., when inkjet patterning  $SiN_x$  layers with a formed hydrofluoric acid solution [16]. In these experiments, the evaporation of the droplet caused a transient flow of the reactants to the perimeter of the wetted area. However, the etched profiles obtained with higher platen

temperatures appear to graduate inwards, with the centre of the etched opening being the most etched, unlike the 'donut shaped' profile observed in Lennon et al.'s experiments, which became more prominent as the temperature increased. Further increases in platen temperature may produce similar 'donut-shaped' structures, however it is possible that the lateral flow of the etchant may be disrupted by the porous structure of the AAO layer. Therefore, rather than a single 'coffee-ring' structure or a donut profile being observed, a series of coffee rings forms as a result of the simultaneous processes of etchant being trapped in the porous layer as water evaporates from the edge inwards, creating a series of 'coffee ring' structures around the etched opening.

Table 2. Effect of platen temperature and the number of printed layers on the etched hole diameter (d) and the depth of etching.

Platen Temperature	8 Layers	6 Layers	4 Layers	2 Layers	1 Layer
<i>T</i> = 30°C <i>t</i> = 60 min	d = 33 μm	$d = 26  \mu \mathrm{m}$	$d = 24  \mu \mathrm{m}$		
$T = 60^{\circ}C$ $t = 60 min$	<i>d</i> = 27 μm	$d = 25  \mu \mathrm{m}$	$d = 24 \ \mu m$	<i>d</i> = 23 μm	$d = 20 \mu\text{m}$
<i>T</i> = 60°C <i>t</i> = 10 min	$\int_{d=30  \mu m}$	$d = 29  \mu \mathrm{m}$	$d = 26 \ \mu \text{m}$	$d = 22 \mu\text{m}$	
<i>T</i> = 75°C <i>t</i> = 10 min		$d = 22 \ \mu m$	$d = 22 \ \mu m$	$d = 20 \mu\text{m}$	$d = 22 \mu\text{m}$

# 3.3. Effect of surface morphology

Different surface morphology (e.g., polished, planar or textured) affected the way holes were etched in AAO layers. Polished surfaces resulted in the smallest etched hole diameters, with diameters of 20-30  $\mu$ m being observed. In comparison, planarised samples required more layers of etchant to etch through the

same thickness of AAO, which increased the diameter of the etched holes. This observation is supported by the trends shown in Table 1 and Table 2. The etching on textured surfaces with random pyramid sizes in the range of  $3-5 \mu m$ , required the largest amount of etchant and longest etching duration.



Fig. 1. Array of holes etched in an AAO layer formed on: (a) a polished wafer by depositing 6 layers of etchant; (b) a planar wafer by depositing 12 layers of etchant; and (c) a textured wafer by depositing 12 layers of etchant. The etchant in all cases was 50% (w/w) H<sub>3</sub>PO<sub>4</sub>, and it was deposited using a 1 pL cartridge of the DMP-2831. (d) shows the local BSF formed by alloying aluminium through the etched openings at 850 °C.

As the roughness of the surface increased, the uneven topography of the pyramids, which created troughs where etchant could pool, most likely disrupted the surface tension of the droplets on the wafer surface and therefore caused more spreading etchant over the surface. Furthermore, etchant spreading reduced the amount of effective etchant per unit area, thus more layers of etchant were required to etch through the same thickness of AAO. However, as a planarised (e.g., rear-etched) surface enables improved surface passivation over an alkaline-textured surface, the etching on planar surface will probably be of most practical concern. The optimal printing parameters required to successfully etch holes in a 600 nm thick AAO layer on different surface types are summarized in Table 3. The minimum printing parameters also demonstrate the possible choice between reducing the number of layers printed, or the etching duration.

Surface Texture	Number of Layers	Etch Time (min)
Polished	4	30
	6	13
Planarised	6	45
	8	30
Textured	12	70
	24	45

Table 3. Optimal printing parameters required to etch holes in a 600 nm AAO layer on different surfaces.

#### 4. Contact formation results

### 4.1. Effect of contact spacing

Holes in a 2D array were etched in 600 nm AAO layers formed on planarised wafer surfaces with spacings of 125  $\mu$ m, 177  $\mu$ m and 250  $\mu$ m. This corresponded to metal-silicon contact fractions of ~ 5%, 2%, and 1%, respectively, assuming a circular metal contact area having a diameter of 30  $\mu$ m. The implied open circuit voltages ( $V_{OC}$ ), estimated by photo-conductance decay before and after the etching process with varied contact spacing, are compared in Fig. 2. All contact spacing variations lay within the margin of measurement error. This indicated that the inkjet patterning process had a negligible effect on the passivation of the wafers.

After metallization firing, the formation of local BSF was visualised by selective etching of the aluminium-doped p+ region. The dimension and uniformity of local BSF regions were measured from the SEM images. Fig. 3 shows the etched hole diameter before and after firing, the contact depth and the thickness of local BSF with different contact spacing. Firing increased the contact diameter over a wide range of contact spacing. Although all the wafers had similar initial diameter of 30  $\mu$ m before firing, the diameter of 125  $\mu$ m spaced contacts experienced significantly more increase than that of 250  $\mu$ m, which was in good agreement with [17]. This widening effect of the contact during firing suggested a link between the aluminium-silicon alloying process and contact widening. It is possible that saturation of aluminium with silicon of silicon on heating due to the increased fluidity of the surrounding molten alloy. This trend was useful for the rear contact design, with the contact widening effect becoming less evident towards 1% optimal metal-silicon contact fraction [18]. On the contrary, the thickness of the local BSF regions increased with increased contact spacing. However the increase in the thickness is largely dominated by the peak firing temperature which is discussed further in Section 4.2.



Fig. 2. The variation of implied Voc before and after etching. The error bars showing the standard deviation of 6 wafers.



Fig. 3. Contact dimension and BSF thickness graphed as a function of contact spacing (all samples were fired at 850 °C in an inline firing furnace where the peak firing temperature was experienced for a time of 5 sec).

### 4.2. Effect of firing temperature

The amount of silicon which forms the local BSF region is dependent largely on the peak firing temperature, with the thickness of the local BSF regions increasing with increased peak firing temperature. At higher peak firing temperatures, the solubility of aluminium in the silicon increases, hence making the concentration of aluminium higher at the initial interface during liquid phase epitaxial growth. Moreover, given an identical cooling rate, a higher peaking firing temperature allows longer time for the sample to cool to the eutectic temperature, thus resulting in more time for epitaxial growth and therefore a thicker local BSF region [17].

From Fig. 4 it is clear that as the temperature increased, so did the depth, width and local BSF thickness of the contact regions. These effects occur markedly at temperatures greater than 700 °C. In contrast, no p+ BSF regions were evident for samples fired at temperatures  $\leq 650$  °C, as the aluminium melt begins at temperatures in excess of 660 °C [19]. This confirms the findings of Urrejola et al that the temperature is a strong driver of the diffusion process which alloys the aluminium and silicon in the firing process [20].

The increase in contact area occurs because of the relation between temperature and the diffusion of aluminium into the silicon and vice versa. At higher peak firing temperatures, the inter-diffusion of silicon and aluminium are both increased [21]. A more rigorous alloying process occurs at the silicon/aluminium interface, therefore forming a large reservoir of molten alloy in the contact area. However during cool down, once the eutectic temperature is reached, a eutectic layer of approximately 12% silicon and aluminium immediately solidifies [19]. Consequently, the size of the eutectic is a reflection of the amount of silicon dissolved into the aluminium and hence a higher temperature results in larger contact widths and depths.



Fig. 4. Contact dimension and BSF thickness graphed as a function of peak firing temperature (all samples were fired in an inline firing furnace where the peak firing temperature was experienced for a time of 5 sec)

#### 5. Conclusions

In this paper, we have described an inkjet printing method for patterning an AAO layer into an array of holes that may be used to facilitate localised rear metal contacts for silicon solar cells. Holes of diameter of ~ 30  $\mu$ m can be etched in 600 nm thick layers of AAO formed on planarised (rear-etched) surfaces of silicon wafers. Even smaller openings having a diameter of ~ 20  $\mu$ m can be etched in AAO layers formed on polished silicon surfaces. Localised metal contact regions were formed by aluminium alloying through the inkjet-patterned holes, resulting in local BSF regions of thickness up to 8  $\mu$ m. Dielectric stacks comprising SiO<sub>2</sub>/AAO have been demonstrated to be thermally stable at 700 °C, therefore making the described patterning method a possible alternative to dielectric stacks comprising SiO<sub>2</sub>/SiNx. The AAO layers can serve to both passivate surfaces and facilitate small-area metal contacting by way of their porosity serving to reduce etchant spreading for chemical patterning processes.

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#### References

1. Engelhart, P., et al., *Laser structuring for back junction silicon solar cells*. Progress in Photovoltaics: Research and Applications, 2007. **15**(3): p. 237-243.

2. Glunz, S.W., et al. New simplified methods for patterning the rear contact of RP-PERC high-efficiency solar cells. in Photovoltaic Specialists Conference, 2000. Conference Record of the Twenty-Eighth IEEE. 2000.

3. Knorz, A., et al., *Selective laser ablation of SiNx layers on textured surfaces for low temperature front side metallizations*. Progress in Photovoltaics: Research and Applications, 2009. **17**(2): p. 127-136.

4. M.C.Morilla, R.R., J.M.Fernandez, Laser Induced Ablation and Doping Processes on High Efficiency Silicon Solar Cells, in 23rd European Photovoltaic Solar Energy Conference and Exhibition2008: Valencia, Spain.

5. Hallam, B., et al., *Record Large-Area p-Type CZ Production Cell Efficiency of 19.3% Based on LDSE Technology*. IEEE J. Photovolt., 2011. **1**(1): p. 43-48.

6. Z. Hameiri, L.M., A. Sproul, and S. R. Wenham, 18.7% efficient laser-doped solar cell on p-type Czochralski silicon. Appl. Phys. Lett., 2010. 97(222111).

7. Kray, D., et al. Laser-doped silicon solar cells by Laser Chemical Processing (LCP) exceeding 20% efficiency. in Photovoltaic Specialists Conference, 2008. PVSC '08. 33rd IEEE. 2008.

8. Wang, Z., et al., Advanced PERC and PERL production cells with 20.3% record efficiency for standard commercial p-type silicon wafers. Progress in Photovoltaics: Research and Applications, 2012. 20(3): p. 260-268.

9. MERCK. Innovative Structuring Concepts for Solar Cell Production. 2012 [cited 2012 September 20]; Available from: http://www.merck-performance-

materials.com/en/solar\_and\_energy/isishape\_topic\_solar\_and\_energy/isishape\_topic\_solar\_and\_energy.html.

10. Allen Barnett, R.H., C. Paola Murcia, Anthony Lochtefeld, Christopher Leitz, Andrew Gerger, Michael Curtin. Independent Approaches to Increase Voltage and Current in Thin Crystalline Silicon Solar Cells. in 26th European Photovoltaic Solar Energy Conference. 2011. Hamburg, Germany.

11. Li, Y., Z. Lu, and A.J. Lennon, Optical modeling of anodic aluminum oxide for light-trapping in silicon solar cells, in Solar 2012 Conference2012: Melbourne, Australia.

12. Lu, P.H., et al., Enhanced passivation for silicon solar cells by anodic aluminium oxide, in 37th IEEE Photovoltaics Specialist Conference2011: Seattle, USA.

13. Lu, P.H., et al., Anodic Aluminum Oxide Passivation For Silicon Solar Cells. IEEE J. Photovolt., 2013. 3(1): p. 143-151.

14. Grant, N.E. and K.R. McIntosh, Low Surface Recombination Velocity on (100) Silicon by Electrochemically Grown Silicon Dioxide Annealed at Low Temperature. Electron Device Letters, IEEE, 2010. **31**(9): p. 1002-1004.

15. Dimatix, F., Materials Printer & Cartridges DMP-2831 & DMC-11601/11610 Datasheet, 2006.

16. Lennon, A.J., A.W.Y. Ho-Baillie, and S.R. Wenham, Direct patterned etching of silicon dioxide and silicon nitride dielectric layers by inkjet printing. Solar Energy Materials and Solar Cells, 2009. **93**(10): p. 1865-1874.

17. Cui, J., Colwell, Jack., Li, Zhongtian., Lennon, Alison J., Localised Back Surface Field Formation via Different Dielectric Patterning Approaches, in Solar 2012 Conference2012: Melbourne, Australia.

18. Zhao, J., A. Wang, and M.A. Green, *Series resistance caused by the localized rear contact in high efficiency silicon solar cells*. Solar Energy Materials and Solar Cells, 1994. **32**(1): p. 89-94.

19. Murray, J. and A. McAlister, The Al-Si (Aluminum-Silicon) System. Bulletin of Alloy Phase Diagrams, 1984. 5(1).

20. Urrejola, E., et al., *Silicon diffusion in aluminum for rear passivated solar cells*. Applied Physics Letters, 2011. **98**(15): p. 153508.

21. Urrejola, E., et al., *Distribution of Silicon in the Aluminum Matrix for Rear Passivated Solar Cells*. Energy Procedia, 2011. 8: p. 331-336.