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Second Workshop on using Emerging Parallel Architectures

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Abstract

The Second Workshop on Using Emerging Parallel Architectures (WEPA), held in conjunction with ICCS 2010, provides a forum for exploring the capabilities of emerging parallel architectures such as GPUs, FPGAs, Cell B.E., and multi-cores to accelerate computational science applications.

Keywords: Computational Science, Parallel Computer Architectures, GPGPU, CUDA, Cell/BE, Reconfigurable Computing, Heterogeneous Multi-cores, High Performance Computing

1. Introduction

Welcome to the Second Workshop on Using Emerging Parallel Architectures (WEPA). This workshop has been motivated by the significant transformation of the computing landscape in recent years with the emergence of more powerful processing elements such as CUDA-enabled GPUs, FPGAs, and Cell/BE. On the multi-core front, Moore's Law has transcended beyond the single processor boundary with the prediction that the number of cores will double every 18 months. Going forward, the primary method of gaining processor performance will be through parallelism. Multi-core technology has visibly penetrated the global market. Accordingly to the Top500 lists, the HPC landscape has evolved from supercomputer systems into large clusters of multi-core processors. Furthermore, GPUs, FPGAs and heterogeneous multi-cores have been shown to be viable computing alternatives, where certain classes of applications witness more than one order of magnitude improvement over their GPP counterpart. Therefore, future computational science centres will employ resources such as FPGAs, GPUs and Cell architectures to serve as co-processors to offload appropriate compute intensive portions of applications from the servers. This workshop provides a forum for exploring the capabilities of emerging parallel architectures to accelerate computational science applications.

The technical program was put together by the Workshop Chairs Bertil Schmidt and Douglas Maskell and 21 members of a distinguished program committee. The workshop received 26 submissions. After an initial screening 25 submissions were reviewed by at least three experts in the field. Based on the reviews, 13 papers were selected

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for presentation at the workshop and inclusion in the workshop proceedings.

We wish to thank the program committee members for submitting thoughtful reviews and all authors who submitted high-quality manuscripts. We plan to continue the workshop next year.

2. Workshop Organizers

- Workshop Co-Chairs:
  - Bertil Schmidt (Nanyang Technological University, Singapore)
  - Douglas Maskell (Nanyang Technological University, Singapore)

- Program Committee:
  - Manfred Schimmler (University of Kiel, Germany)
  - Simon See (SUN Microsystems)
  - Neil Bergmann (University of Queensland, Australia)
  - Heiko Schröder (RMIT University, Australia)
  - Alexandros Stamatakis (TU Munich, Germany)
  - Dominique Lavenier (IRISA, France)
  - Jaroslav Zola (Iowa State University, USA)
  - Scott Emrich (University of Notre Dame, USA)
  - Ananth Kalyanaraman (Washington State University, USA)
  - Shi Haixiang (NTU, Singapore)
  - Gerrit Voss (Fraunhofer IGD, Germany and NTU, Singapore)
  - Weiguo Liu (NTU, Singapore)
  - Malcolm Low (NTU, Singapore)
  - Vipin Chaudhary (University of Buffalo, USA)
  - John Paul Walters (USC Information Sciences Institute East, USA)
  - Witold Rudnicki (University of Warsaw, Poland)
  - Mathieu Giraud (INRIA, France)
  - Stan Scott (QUB, UK)
  - Chris Clarke (University of Bath, UK)
  - Arpith Jacob (WUSTL, USA)
  - Rob Farber (PNNL, USA)

3. List of accepted Papers

2. PFFT: An improved fast Fourier transform for the IBM Cell Broadband Engine, A. Shaffer, B. Einfalt, P. Raghavan
3. Solving Boltzmann equation on GPU, Y.Y. Kloss, P.V. Shuvalov, F.G. Tcheremissine
4. 3D finite element numerical integration on GPUs, P. Maciol, P. Plaszewski, K. Banas
5. Parallel 3D fast wavelet transform on manycore GPUs and multicore CPUs, J. Franco, G. Bernabe, J. Fernandez, M. Ujaldon
6. Using the reconfigurable massively parallel architecture COPACOBANA 5000 for applications in bioinformatics, L. Wienbrandt, S. Baumgart, J. Bissel, C.M.Y. Yeo, M. Schimmler
7. Implementation of a linear programming solver on the Cell BE processor, M. Eleyat, L. Natvig
9. Efficient Stackless Ray Traversal for Bounding Sphere Hierarchies with CUDA, T. Toczek, D. Houzet, S. Mancini
11. Gravitational Tree-Code on Graphics Processing Units: Implementation in CUDA, E. Gaburov, J. Bedorf,
S.P. Zwart
