Nano Energy (2015) 16, 350–356

Available online at www.sciencedirect.com

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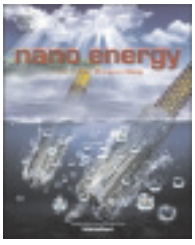

RAPID COMMUNICATION

# Efficient thermoelectric performance in silicon nano-films by vacancy-engineering

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Received 23 January 2015; received in revised form 19 June 2015; accepted 10 July 2015
Available online 20 July 2015

**KEYWORDS**
Thermoelectric;
Silicon;
Thermal conductivity;
Nano-film;
Vacancy

**Abstract**
The introduction of large concentrations of lattice vacancies in silicon nano-films creates more than a 20-fold reduction in thermal conductivity, while electrical conductivity and Seebeck coefficient are largely maintained. This results in thermoelectric performance comparable to silicon nanowires, but crucially leaves the silicon structure indistinguishable from bulk silicon, resulting in a robust material that is straight-forward to fabricate. This finding significantly advances the potential of silicon ultra-thin-films as a high-performance thermoelectric material.


## Introduction

Silicon (Si) is a remarkably useful element. Its abundance, low cost and low toxicity, combined with vast practical know-how means it is a leading material on which to base technologies. However for good reason, certain applications have under-utilised Si, with thermoelectrics (TE) being one example. Three material characteristics determine TE performance – thermal conductivity ($\kappa$), Seebeck coefficient ($S$) and electrical resistivity ($\rho$). These interlinked properties are often combined along with absolute temperature ($T$) to describe performance in terms of the dimensionless figure-of-merit ($ZT$), where $ZT=S^2T/\rho\kappa$. Compared to other materials, highly-doped Si (doping $\sim 10^{19}$-$10^{20}$ cm$^{-3}$) has desirably large $S$ and small $\rho$, but these are negated by high thermal conductivity, meaning that $ZT$ is relatively poor for bulk Si ($ZT\sim 0.01$ at 300 K [1]), about 100-fold worse than for popular TE materials such as bismuth telluride ($Bi_2Te_3$) ($ZT\sim 1$).

## Nanowires

Only in the past few years has it been demonstrated possible to vastly reduce Si's thermal conductivity with little or no effect on $S$ or $\rho$ [2,3]. In structures such as Si nanowires

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http://dx.doi.org/10.1016/j.nanoen.2015.07.007

(SiNWs), the long-wavelength phonon modes, which strongly contribute to the thermal transport in bulk Si, are successfully inhibited, leaving the electronic properties largely unaffected. This allows for higher $ZT$, improved TE efficiency, and makes nano-structured Si an attractive TE material. Subsequently this finding has been corroborated by several research teams worldwide, through both theoretical and experimental studies. The majority have looked to three parameters for SiNW optimisation [4-8] - (i) reduced SiNW diameter, (ii) increased SiNW surface roughness, and (iii) longer wire length. Theoretically, best performance arises for long, rough SiNWs with diameter $<10$ nm [4], however this geometry is hindered by practical problems such as dopant deactivation, low wire packing density and susceptibility to SiNW breakage and device failure [5,6]. So far only lab-scale demonstrator devices have been validated.

### Nano-films

An alternative approach – and one which overcomes some of the practical challenges associated with long, thin SiNWs – is to use Si nano-films, i.e. films that are macroscopic in two dimensions but have thickness at the nano-scale, such as silicon-on-insulator (SOI) films [9]. These are more robust, have better area coverage and are usually manufactured in a more scalable process than SiNWs. However, the major drawback until now has been that the nano-film geometry is far less effective at reducing $\kappa$ and so TE performance is significantly less for nano-films than it is for SiNWs [10]. Improved performance is possible in nano-films that are decorated with a high density of nanoscopic holes [11] or by phononic-crystal patterning [12]. Unlike the method we introduce here, the electrical properties of these 'holey' films deteriorate significantly with high porosity. Likewise, their porosity makes them fragile to handle, and given they are sensitive to variations in hole size/spacing, are more difficult to reliably fabricate at scale, with hole densities required of $10^{10}$-$10^{11}$ cm$^{-2}$ (estimated from [13]).

## Vacancy-engineering

In this *communication* a method is described to reduce $\kappa$ in Si nano-films by $\sim$90% compared to control samples, giving $ZT=0.2$ at 360 K. Crucially, unlike SiNWs or holey Si, our process leaves the Si structure almost indistinguishable from bulk Si and is more straight-forward to fabricate. Unlike other approaches that rely on nano-dimensions for their success, this method can be scaled to microscopic dimensions, and potentially beyond. Bulk properties of Si such as Seebeck coefficient, electrical resistivity, dopant activation, and electron mobility are largely retained, but with vastly reduced $\kappa$. This is done by creating vacancy-rich Si via a process of *vacancy-engineering*.

### Theory

Vacancies ($V$) are simple, intrinsic point-defects, which in basic form, are a missing Si atom within an otherwise tetrahedrally coordinated lattice [14]. This is in contrast to their counterpart – the self-interstitial ($I$) – which, for simplicity, can be considered as an extra Si atom in the lattice. Around a vacancy, lattice relaxation occurs, creating a lattice contraction [14] and additional scattering sites for phonons. Their presence can therefore influence thermal transport, however the equilibrium concentration of vacancies is extremely low in regular Czochralski-grown Si ($<10^{11}$ cm$^{-3}$ [14]) creating negligible impact. Large vacancy concentrations (1.5%) have been calculated theoretically to have a significant impact on the thermal conductivity of bulk Si, reducing $\kappa$ by up to 95% at 300 K [15-17]. This is explained by increased phonon scattering and a reduction in the mean-free-path length for phonons, due to the relatively high concentration of vacancy defects. However, the vacancy concentration required theoretically, equivalent to $\sim10^{21}$ cm$^{-3}$, is significantly at odds with the equilibrium vacancy concentration in practice. With vacancy-engineering it is possible to close this gap by artificially creating a super-saturation of vacancies, using self-implantation of Si ions to introduce high vacancy concentrations (0.1–4%) in the near-surface of Si nano-films. This approach has been previously successful in overcoming the problem of transient-enhanced boron diffusion in Si transistor devices [18].

### Design

Monte Carlo simulation software was employed to simulate a range of experimental conditions (different ion-energies/SOI substrates) to investigate the spatial distribution of point-defects (both vacancies and interstitials) created by ion-implantation of SOI. Ion-implantation was chosen as the method for vacancy introduction, since it gives controllable and repeatable results, and is a staple technique applied for Si technologies. SOI with a 100 nm-thick Si film and 200 nm-thick buried oxide was chosen for this experiment, with the oxide forming a physical barrier separating net vacancy and net interstitial concentrations from recombining during annealing, and allowing for straight-forward characterisation of the isolated top-layer. The "Stopping and Range of Ions in Matter" (SRIM) code [19] was used for the simulation to extract depth-concentration distributions of vacancy defects ($V(x)$), interstitial Si defects ($I(x)$) and implanted Si ions ($Si(x)$). The net defect distribution ($C(x)$) was calculated as $C(x)=Si+I-V$ [20], a modified version of the Net Recoil Density algorithm [21]. Here a net-positive value indicated a region of interstitial-rich material, and a net-negative value a vacancy-rich region.

## Results and discussion

Figure 1 shows the simulated defect depth-concentration distribution for an ion-implanted SOI substrate (100 nm Si/200 nm $SiO_2$/300 μm Si). A high concentration ($>10^{21}$ cm$^{-3}$) of vacancy defects is found immediately below the Si surface, which falls to a plateau at depths between 25 and 100 nm, where the vacancy concentration varies between $10^{19}$-$10^{20}$ cm$^{-3}$. Integrating under the curve for depths 0-100 nm gives a net vacancy density of $7.94\times10^{14}$ cm$^{-2}$, which equates to an average concentration of $7.94\times10^{19}$ cm$^{-3}$ or $\sim$0.16%, though the vacancy concentration reaches 4% in the top 10 nm of the nano-film. While the simulation considers mono-vacancies, known to be mobile at room temperature, di-vacancies and small vacancy-clusters – stable at ambient temperature – are likely to be present with an equivalent depth distribution [22,23]. A relatively high implant fluence of

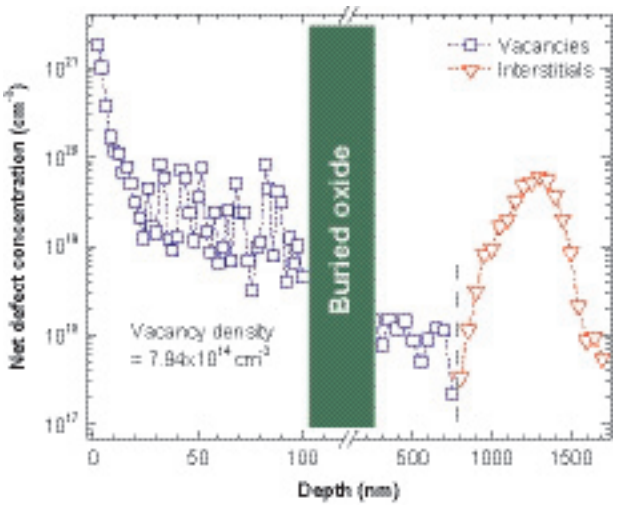


**Figure 1** Simulated net defect concentration as a function of depth in silicon-on-insulator substrate (100 nm Si/200 nm $SiO_2$/300 μm Si) subjected to Si ion-implantation (1 MeV, $4.5 \times 10^{15}$ $cm^{-2}$). Net vacancy (squares) and interstitial (triangles) regions are separated by the buried oxide leaving a vacancy-rich region in the Si overlayer with vacancy density of $7.94 \times 10^{14}$ $cm^{-2}$.

$4.5 \times 10^{15}$ $cm^{-2}$ was chosen to give as high a concentration of vacancy defects as possible in the 100 nm film, without causing complete amorphisation [20]. Likewise a relatively high implant energy of 1 MeV was chosen to ensure adequate separation of point-defect distributions, with a net concentration of vacancy defects in the Si nano-film and a net interstitial profile well below the buried oxide, i.e. beyond ~750 nm in this case. This separation of vacancies and interstitials is caused by the forward momentum transferred from implanted to host atoms creating a slight displacement between interstitial and vacancies, which on annealing, recombine locally but leave a net vacancy concentration near the surface and interstitials near the implant's projected range [24,25]. This is illustrated schematically in Supporting Information. Although demonstrated here through simulation, implantation-induced vacancy-engineering has been verified experimentally in several other studies, including confirmation of the close match between experiments and SRIM simulations [26-28].

## Electrical resistivity

Hall measurements and van der Pauw resistance measurements were made at 300 K in the in-plane direction. These revealed that control samples were n-type with doping concentration, $N = 1.31 \pm 0.02 \times 10^{19}$ $cm^{-3}$ and Hall mobility, $\mu_H = 112.3 \pm 1.5$ $cm^2 V^{-1} s^{-1}$, consistent with the nominally-stated resistivity of $\leq 5$ mΩ-cm. Seebeck measurements showed a room-temperature Seebeck coefficient (also in-plane) of $S = -402$ μV $K^{-1}$. Thermal conductivity was extracted by combining the resistance and Seebeck measurements with the Harman method to give $\kappa = 65.3$ W $m^{-1} K^{-1}$ (in-plane), which is lower than would be expected for bulk Si (~150 W $m^{-1} K^{-1}$ [29]), but is consistent with that expected for a 100 nm-thick Si nano-film [10]. The

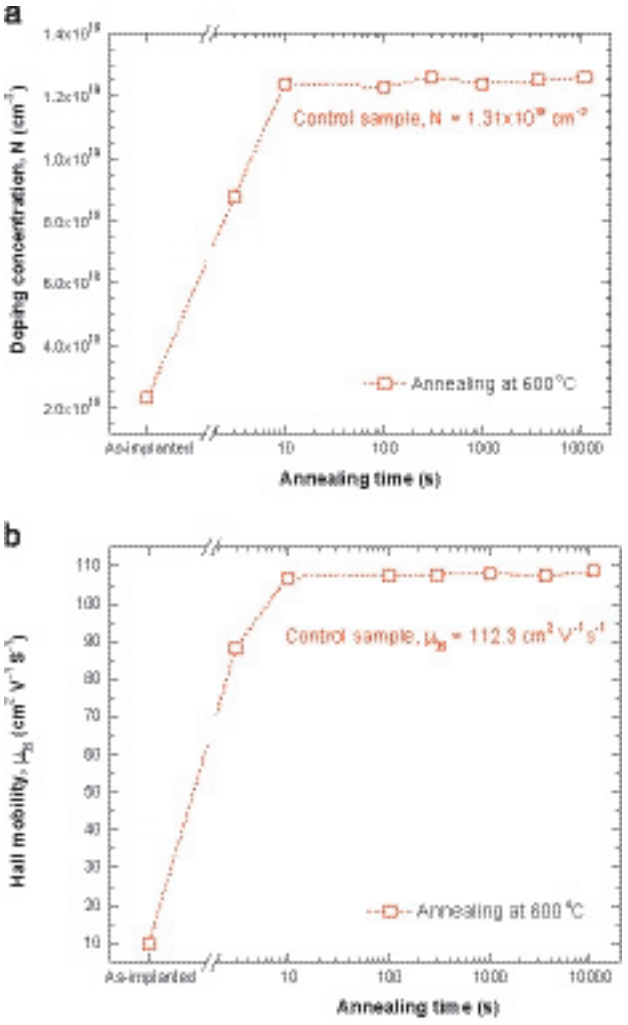


**Figure 2** (a) Carrier concentration and (b) Hall mobility as a function of annealing time at a temperature of 600 °C for 100 nm silicon-on-insulator samples (100 nm Si/200 nm $SiO_2$/300 μm Si) subjected to Si ion-implantation (1 MeV, $4.5 \times 10^{15}$ $cm^{-2}$). Measurements were made at 300 K.

Harman method indicated the *ZT* of control samples was ~0.01, as expected.

Figure 2 shows the change in carrier concentration and Hall mobility after ion-implantation, as a function of annealing time for rapid-thermal-annealing (RTA) at 600 °C. Immediately following ion-implantation the electron concentration in the Si nano-film is reduced by almost one order of magnitude. The Hall mobility is also significantly reduced. These reductions in electrical conductivity correspond to the introduction of implantation-induced damage in the Si lattice, which disturbs substitutional dopant atoms from lattice sites and increases the scattering of charge carriers. After RTA for 3 s, there is partial recovery of the doping and mobility properties, and following RTA for 10 s, both $N$ and $\mu_H$ have recovered almost in line with control samples. Literature on recrystallisation of Si following ion-implantation suggest that *V*/*I* recombination will have taken place following 10 s RTA with all dopant atoms returned to substitutional sites [30]. The small remaining reduction in electrical conductivity comparing vacancy-engineered and control

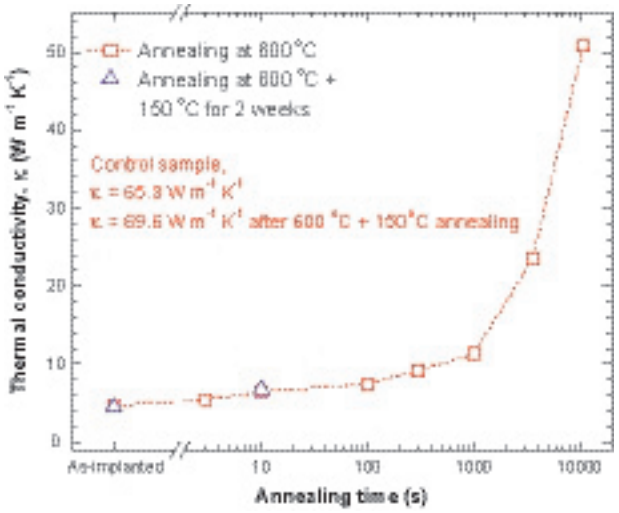


**Figure 3** Thermal conductivity (in-plane) as a function of annealing time at a temperature of 600 °C for 100 nm silicon-on-insulator samples (100 nm Si/200 nm $SiO_2$/300 μm Si) subjected to Si ion-implantation (1 MeV, $4.5 \times 10^{15}$ $cm^{-2}$). Triangles indicate samples that received additional post-annealing at 150 °C for 2 weeks. Measurements were made at 300 K.

samples, results from the near-surface region where the vacancy concentration is largest and where vacancy-induced scattering of electrons is significant. This is supported by differential Hall depth-profiling measurements (see Supporting Information). For extended annealing times up to 10800 s the electrical doping properties continue to improve gradually towards control values, as vacancies are removed.

## Thermal conductivity

Figure 3 shows the corresponding variation with annealing time for in-plane thermal conductivity at 300 K. $\kappa$ is found to decrease by more than an order of magnitude as a result of implantation-induced damage, falling to a value of 4.7 $W m^{-1} K^{-1}$ immediately after ion-implantation. Since, at this point, the Si lattice is highly damaged, it is unsurprising that $\kappa$ is only slightly greater than the amorphous limit [31]. Following RTA for 3 s, $\kappa$ increases slightly, but is still low. As previously described, the electrical properties in this film, as for the as-implanted film, are poor. Following 10 s RTA, $\kappa$ increases only slightly to 6.5 $W m^{-1} K^{-1}$ and is reduced by ~90% compared to the thermal conductivity of control samples. Here we know from electrical measurements that electronic properties are only modestly inferior to control samples despite the presence of vacancies. Since, compared to undoped Si, the electron mobility is already reduced in this sample by the presence of a large concentration of ionised impurities ($>10^{19}$ $cm^{-3}$), the addition of a similar concentration of vacancies has little effect on the mobility. In contrast, the vacancies have a significant impact on the thermal conductivity, since while phonons are weakly scattered by ionised impurities, they are strongly scattered by lattice defects.

Non-equilibrium molecular dynamics (MD) simulations have also shown a reduction in Si thermal conductivity after introducing $V_4$ clusters into the Si lattice [15], as a result of increased phonon scattering and reduced phonon mean-free-path length [2,3,32]. However a ~65% decline in $\kappa$ was found relative to bulk Si for a vacancy concentration of 0.15% [15], less than the ~90% $\kappa$ reduction for 0.16% vacancies found in experiments. Since the MD $\kappa$ reduction lessens as vacancy clusters grow in size, e.g. it is only ~25% for $V_{12}$ clusters, this difference can be partially explained considering that our sample contains di-vacancy clusters that will impact phonon transport more than $V_4$ clusters. Even accepting this premise, the experimental effect remains larger than that predicted theoretically.

For slightly longer annealing time, up to 1000 s, $\kappa$ remains $<12$ $W m^{-1} K^{-1}$ but for longer annealing times - with 10800 s being a clear example - $\kappa$ returns towards its initial value. The rise in $\kappa$ as a function of thermal budget is likely to correspond to two occurrences. Firstly, the removal of excess vacancies at the surface and buried-oxide interface [20], since at 600 °C vacancy-defects will be mobile and able to migrate to sinks. Therefore the overall vacancy concentration will be reduced as annealing ensues. The second contribution is the agglomeration and growth of vacancy-clusters [33,34]. Since dissolution of vacancy-clusters eventually occurs, this may also contribute to the overall reduction in vacancies [33,34]. As indicated previously, cluster size is important since phonon scattering was found in simulations to be a function of vacancy-cluster size, with the reduction in $\kappa$ calculated to be less as vacancy clusters grow [15]. Since cluster growth is driven by thermal budget, larger clusters are expected to be present after longer annealing times. The observed gradual rise in $\kappa$ as annealing time increases, reinforces the prediction that small vacancy clusters will reduce $\kappa$ more significantly than larger vacancy-clusters and/or that the $\kappa$ reduction is lessened by overall vacancy removal. Either explanation supports the hypothesis that vacancy defects are responsible for the $\kappa$ reduction.

It should be noted that $\kappa$ was also measured normal to the sample surface (see Supporting Information). When heat is driven perpendicular to the surface, $\kappa$ is on average, and systematically ~30% lower. This difference is likely a result of heat travelling through minimum impedance paths, and avoiding the vacancy-rich surface layer in the in-plane direction. When driven normal to the surface, heat is forced to cross the vacancy-rich, high-impedance region over a distance of ~10% of the total film thickness and the thermal conductivity is therefore reduced.

## Thermoelectric operating conditions

Since thermoelectrics generators (TEGs) operate at elevated temperatures, for practical applications it is important that the vacancy concentration should remain high, with clusters in small, stable form ($V_2$ or small clusters), in order to give a consistently reduced $\kappa$ value. This will inform the maximum temperature at which vacancy-engineered Si TEGs can be operated at. It should be noted that the RTA was carried out at 600 °C, which is a significantly higher temperature than we envisage Si TEGs would be exposed to during operation, i.e. <200 °C, similar to existing $Bi_2Te_3$-based devices. Therefore the evolution/removal of vacancies within Si TEGs is expected to be preventable, given that di-vacancies and small clusters, stable at room temperature, are only found to

become mobile for temperatures of 200-300 °C [33,34]. As an initial stability test, three samples - one control, one as-implanted and the other, a best-performing sample (10 s RTA) - were subjected to an extended low-temperature anneal for 2 weeks at a temperature of 150 °C. Following this treatment, thermal conductivities were again measured and were found to be unchanged within experimental uncertainty. Therefore, for TEGs operating at $<200$ °C, vacancy-engineered Si is expected to be a suitable material. Further investigation of material stability is important however, and is being carried-out in subsequent experiments.

## Seebeck coefficient

In-plane Seebeck coefficient measurements were carried out for each of the annealed samples. In all cases, $S$ values at 300 K were constant within experimental error ($\pm 5\%$) from sample-to-sample, at $\sim -400\ \mu V\ K^{-1}$ (see Supporting Information). The only exception was the sample that underwent 3 s RTA, which had a slightly improved Seebeck coefficient. This improvement is most likely related to the reduction in carrier concentration in this sample and the corresponding drop in Fermi level position, resulting in higher $S$ [32]. It appears that vacancy-engineering has no direct effect on the Seebeck coefficient of Si.

## Thermoelectric figure-of-merit

The in-plane figure-of-merit was measured for each of the samples at both 300 K and 360 K. These $ZT$ values are shown in Figure 4, with a best $ZT=0.2$ achieved for the sample having undergone 10 s RTA and measured at 360 K. This is $\times 20$ larger than the $ZT$ for bulk Si [1], is comparable with that of both SiNWs and holey Si films [2,3,11-13], and is approaching that of commercially available $Bi_2Te_3$-based devices. At 300 K the highest $ZT$ is slightly less ($ZT=0.16$), most likely as a result of

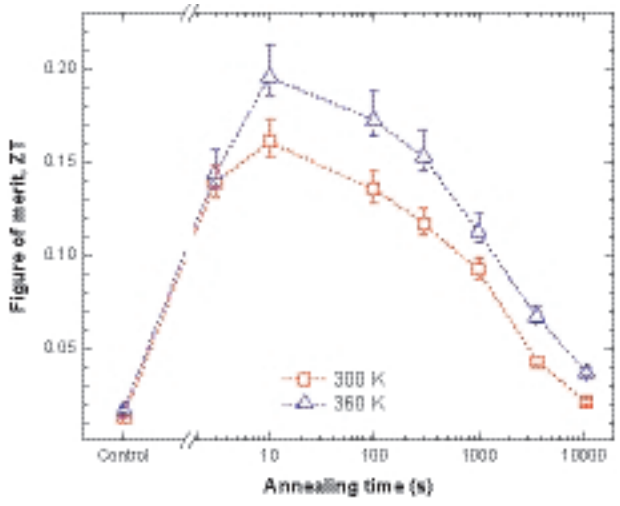


**Figure 4** Thermoelectric figure-of-merit (in-plane) as a function of annealing time at a temperature of 600 °C, for 100 nm silicon-on-insulator samples (100 nm Si/200 nm $SiO_2$/300 μm Si) subjected to Si ion-implantation (1 MeV, $4.5\times10^{15}\ cm^{-2}$), measured at 300 K and 360 K.

Si having lower $S$ and higher $\kappa$ at the lesser measurement temperature, which outweigh a reduction in $\rho$ [35].

Although demonstrated here for 100 nm Si nano-films, vacancy-engineering can be applicable to films of several microns in thickness by up-scaling the ion-implantation energy/fluence, using commercially available high-energy ion-implanters. For example, SRIM shows [19] that the creation of vacancy-rich layers $>3$ μm-thick are possible with implant energies $>5$ MeV - a beam energy that is routinely available. This approach is therefore a candidate for thin-film TEGs - predicted to be a major area of importance for TEs over the next decade [36]. Similarly, since both the vacancy- and doping-concentration in these samples could be optimised further, it is likely that the $ZT$ can be additionally extended using this method. Furthermore, the use of vacancy-engineered Si as the starting material for SiNW and/or holey Si TEGs could be trialled as a method for enhancing these other approaches to Si-based thermoelectrics. Likewise, vacancy-engineering is likely to be applicable to a number of other TE materials, since at high concentrations vacancy defects are often beneficial for reducing $\kappa$ [37-39].

## Conclusions

A method was described to reduce thermal conductivity in Si nano-films by $\sim 90\%$ compared to Si control samples, giving $ZT=0.2$ at 360 K. Bulk properties of Si such as Seebeck coefficient, electrical resistivity, dopant activation, and electron mobility were largely retained, but with vastly reduced $\kappa$. This was done by creating vacancy-rich nano-films via the process of vacancy-engineering. Unlike other approaches to nano-structuring of Si for thermoelectrics, vacancy-engineering left the Si structure almost indistinguishable from bulk Si and was straight-forward to fabricate. Crucially, this method is both scalable to microscopic dimensions and is compatible with other fabrication methods for Si thermoelectrics, such as nanowires and 'holey' Si TEGs. This finding advances the potential of silicon thin-films as a high-performance thermoelectric material and suggests achieving a more competitive figure-of-merit for Si materials may be achievable in the near-term.

## Material and methods

Samples were fashioned from commercially purchased $<100>$ 100 mm-diameter silicon-on-insulator (SOI) wafers consisting of a 100 nm Si layer (n-type, $\leq 5$ mΩ-cm) on top of a 200 nm $SiO_2$ buried-oxide, above a thick ($\sim 300$ μm) Si substrate. Overlayer thickness was confirmed by ellipsometry using a JS Woollam ellipsometer. Doping type, resistivity and doping concentration was confirmed by van der Pauw resistance and Hall measurements. Ion-implantation of Si ions was carried out on a Varian VIISta ion implanter at beam energy 1 MeV and fluence $4.5\times10^{15}\ cm^{-2}$ based on a simulation-defined specification, including a tilt angle of 7°. Wafers were then diced into smaller pieces, with all but several control samples receiving rapid-thermal-annealing in flowing nitrogen in an Ecopia RTP-1200 system. Samples were annealed at 600 °C for a time between 3 s and 10800 s. A small selection of

samples underwent post-annealing for 2 weeks at 150 °C in a Gallenkamp vacuum oven. The 100 nm Si film on each sample underwent characterisation as follows: (i) Electrical resistivity and Hall-effect measurements were made in air in the in-plane direction at 300 K in van der Pauw geometry, using a Biorad HL5900 tool. A magnetic field of 0.5 T from a permanent magnet was applied by the system. Ohmic contacts were made at the four corners of each sample by application of Ga-In eutectic. (ii) Temperature-dependent Seebeck measurements (300 K to 400 K) were made in-plane on a Linseis LSR-3 instrument with a manufacturer-supplied thin-film adaptor, in He ambient at $10^4$ Pa. (iii) Thermal conductivity (out-of-plane) was measured at 300 K under vacuum using an Ulvac TCM-2ω tool. This followed deposition of a 60 nm Au film on the sample surface which was used to apply periodic heating. Temperature-amplitude detection was done by thermo-reflectance, where the intensity of the reflected light depended on the temperature at the front side of the sample. Thermal conductivity for the Si overlayer was extracted by normalisation relative to an SOI control sample with the overlayer removed down to the top of the buried oxide (by etching in 25% KOH solution at 320 K) allowing one to negate the contribution of the $SiO_2$ and Si substrate and extract thermal conductivity for the top 100 nm Si film (See Supporting Information). (iv) Thermoelectric figure-of-merit (in-plane) was extracted at 300 K under vacuum for each sample by the Harman method. Both AC and DC currents were applied through two of the Ohmic contacts in (i) via a Keithley 6221 current source and the potential difference measured across the remaining two contacts using a Keithley 2400. DC measurements were recorded only once the thermoelectric response of the sample had stabilised (after ~5 min). DC and AC resistances ($R_{DC}$, $R_{AC}$) were obtained by linear fitting to current–voltage data (see Supporting Information). For each linear fit, $ZT$ was extracted by solving $(R_{DC}\text{-}R_{AC})-1$ [40]. Subsequent measurements were made with the temperature of each sample raised by coil-heater and held at 360 K, regulated using a Lakeshore 325 temperature controller. Error bars on $ZT$ were estimated based on measurement uncertainty (±5%) with additional margins of error due to radiative emission from each sample. From [41] this was estimated to lead to an underestimate of $ZT$ creating a total uncertainty above each data point of +7% at 300 K and +9% at 360 K. (v) Following the measurement of electrical resistivity, Seebeck coefficient and figure-of-merit (all in the in-plane direction) for all samples at 300 K, thermal conductivity (in-plane) was extracted, according to $\kappa = S^2/Z\rho$. (vi) Hall depth-profiling measurements were carried-out on a subset of samples, again using the Biorad HL5900. These were carried out at 300 K by native-oxide-stripping using buffered-HF dips for 5 s, followed by oxide regrowth in deionized water for 20 s. After each round of oxide-stripping the resistivity and Hall coefficient of the sample was measured in van der Pauw geometry. (vii) Finally room-temperature micro-Raman measurements were performed with a Jobin Yvon LabRam HR800 system in backscattering geometry using 325 nm He-Cd UV laser excitation with a spot size of approximately 1 μm. The UV laser was chosen specifically to give shallow (~10 nm) penetration into the samples. Spectra were dominated by the degenerate transverse optical Si-Si phonon mode, which appeared at a Raman shift of 520 $cm^{-1}$. The shape and intensity of this peak was monitored for each sample as a signature of defects present in the nano-film (see Supporting Information).

All data presented here, in the Supporting Information, and measurement-calibration data are freely available online from Heriot-Watt University's *Pure* data repository. The specific web-location is available via the corresponding author.

## Acknowledgement

We thank the School of Engineering & Physical Sciences at Heriot-Watt University for financial support of this work. NMW acknowledges financial support from the UK EPSRC by way of a doctoral training studentship (EP/M506333/1). Prof Patrick McNally of Dublin City University is gratefully acknowledged for access to Raman spectroscopy facilities.

## Appendix A. Supporting information

Supplementary data associated with this article can be found in the online version at http://dx.doi.org/10.1016/j.nanoen.2015.07.007.

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