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Reducing delay and quantum cost in the novel design of reversible memory elements

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Abstract

In a computational model, that uses transitions from one state of the abstract machine to another, a necessary condition for reversibility is that, the relation of the mapping from states to their successors must be one-to-one. In these works, the primary focus of design is to optimize number of reversible gates and garbage outputs. The calculation of number of gates is not a good option to check the complexity of a circuit as each gate has different architectural complexity decided by a parameter called quantum cost. Delay, hardly addressed in the existing works available in literature, is another good parameter to be optimized for fast reversible computation. In this work, we have presented novel designs of basic sequential circuits like latch that are optimum in terms of delay, quantum cost and garbage. We have also demonstrated quantum cost efficient D-FF, SR-FF, JK-FF & T-FF, along with their master slave configurations.

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Keywords: *Reversible Logic; Quantum Cost; Reversible Flip-Flop; Master Slave*.

1. Introduction

As chips become smaller and faster, they dissipate more heat, which is energy that is entirely wasted. By some estimates the difference between the amount of energy required to carry out a computation and the energy that today's computers actually use is some eight orders of magnitude. It suggests that there is a lot of room for improvements. According to the Rolf Landuaer, in 1961[1], each bit of information loss dissipates KTln2 joule of energy in conventional logic circuits. Information once loss cannot be recovered by any methods [2]. Charles Bennet, in 1973 [3] gave a solution to reduce KTln2 joule of heat dissipation from conventional logic circuits.

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Bennet proposed that in order to avoid heat dissipation the conventional logic circuit must be built by reversible logic gates since there is no information loss occur and hence no dissipation(or minimum dissipation).

Primary focus of reversible logic circuits was limited in the design of combinational circuits because of the convention that the feedback is not allowed in reversible computing [4]. Tomasso Toffoli, in 1980, has shown that the feedback is allowed in reversible computing. According to Toffoli, a sequential network is reversible if its combinational part is reversible [4]. Further it is shown that in order to construct a reversible finite automaton, one can construct a reversible realization of its transition function and use it as a combinational part of the desired sequential circuit. Fredkin has used this concept to propose the first design of the reversible sequential circuit called the JK-latch [Fredkin and Toffoli 1982] having the feedback loop from the output. We are presenting the design of reversible sequential circuit like Flip-flops considering important cost metrics in reversible logic circuits i.e. the quantum cost, delay and number of garbage outputs. Our designs minimize the quantum cost, the delay, and the number of garbage outputs, and are more efficient compared to the existing designs.

2. Literature Survey

A reversible memory cell, i.e., reversible sequential circuit was first designed by Fredkin and Toffoli [5], in 1982, in which design of JK latch was introduced. Later, in 1996, Picton [6] introduced the design of clock less SR-latch using two cross-coupled NOR gate, where NOR gates were designed from Fredkin gate. In 2005, Thapliyal et.al.[7] introduced for the first time all the reversible latches such as D-Latch, T-Latch etc. along with their flip-flop and master-slave configuration. In 2006, Rice [8] introduced a SR-latch without fan-out problem available in the design by Picton and subsequently designed other latches from SR. In 2007, Thapliyal and Vinod [9] proposed a better design of reversible flip-flops than by Rice in terms of number of reversible gates being used and garbage outputs. In 2008, a more detailed analysis of SR-latch is presented by Rice [10]. A better design of all reversible latches (except SR-latch) along with their flip-flops than that of Thapliyal (2005) and Rice (2006) were presented by Chuang and Wang [11]. In 2009, Hafiz [12] presented a novel design of reversible FPGA. In 2011, Morrison [13] designed a static and dynamic RAM arrays with reversible logic. Most of the previous works focused on optimization of number of gates and garbage output in the design, but in this work our goal is to optimize the proposed sequential circuit design in terms of three important parameters namely Quantum Cost, Delay and Garbage output.

3. Basic Reversible Gates

There are some reversible basic gates which we are going to use in design of Flip-Flops and are as follows.

3.1. Reversible NOT Gate

Reversible Not Gate is 1 input and 1 output gate (represented as 1x1), performs inversion of input. It has 0 quantum cost and unit delay (i.e. Δ). NOT gate and its quantum representation is shown in figure

Fig.1. (a) NOT gate; (b) NOT gate quantum representation

3.2. Feynman gate/CNOT Gate

This is a 2x2 reversible gate having the quantum cost 1 and delay Δ. It is also known as controlled-NOT gate. Feynman gate is used to overcome fan-out problem.

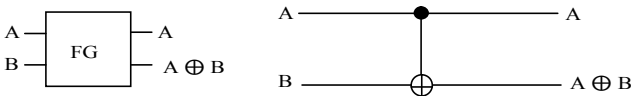

Fig.2. (a) FG gate; (b) Quantum representation of FG gate

3.3. Toffoli Gate/C-CNOT Gate

Toffoli Gate is a 3x3 reversible logic gate having the quantum cost 5 and delay 5Δ.It is also known as the controlled controlled-NOT Gate.

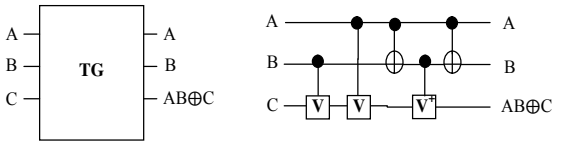

Fig.3. (a) TG gate; (b) Quantum representation of TG gate

3.4. Fredkin Gate

Fredkin gate is 3x3 reversible logic gate with quantum cost 5 and delay 5Δ. Any logic gate can be realized using Fredkin gate and hence it is also known as universal reversible gate.

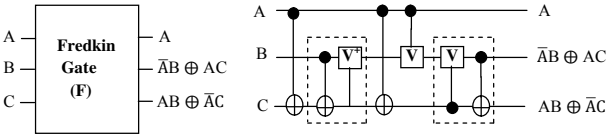

Fig.4. (a) F gate; (b) Quantum representation of F gate

3.5. Proposed Reversible Modified Fredkin Gate

Modified Fredkin Gate is 3x3 reversible gate having quantum cost of 4 and delay 4Δ. This reversible gate is modified form of Fredkin gate.

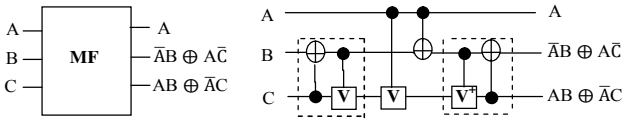

Fig.5. (a) MF gate; (b) Quantum representation of MF gate

4. Reversible Sequential Circuits

In this section, we are presenting some new design of reversible sequential circuits like Flip-Flop (FF) i.e. D-FF, SR-FF, T-FF and JK-FF using basic reversible logic gates.

4.1. Proposed Reversible D-Flip-Flop

Characteristic equation of reversible D-Latch can be written as $Q^{+}=D$ where output is equal to its input value. The characteristic equation of clock enabled reversible D-Latch (D-FF) can be written as

$$Q+=D.E+\overline{E}.Q \quad (1)$$

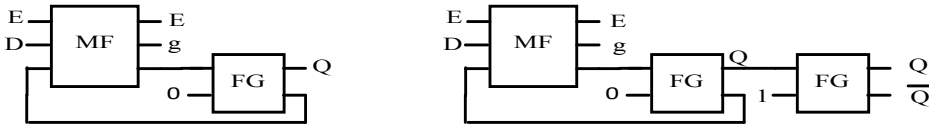

Fig.6. (a) Clock enabled D-latch; (b) D-FF with output Q and $\overline{Q}$

Figure 6(a) shows the clock enable D-latch where output $Q^{+}=D$ for E=1 and output $Q^{+}=Q$ for E=0 output remain in its previous state. For the input D=1 and Q=0, the output of MF gate when E=1 is Q+=1 which is applied to FG gate to provide feedback.

Table.1. A Comparison of Reversible D-FF with $\overline{Q}$

D-FF Comparison	Quantum Cost (Qc)	Delay (D)	Garbage Output(*G*)
[Thapliyal et al. 2005][7]	47	25	6
[Thapliyal and Vinod 2007][9]	10	10	2
[Thapliyal and Ranganathan 2010][14]	7	7	2
Proposed design	6	6	2
% improvement w.r.t. [14]	14	14	-

4.2. Proposed Reversible Master-Slave D-Flip-Flop

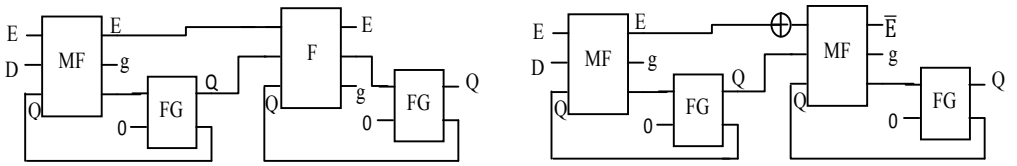

Fig.7. (a) Master-slave D-FF using Fredkin Gate in Slave FF; (b)Master-slave D-FF using MF gate in Slave FF

Figure 7 shows the Master-slave D-FF. When E=1 then master FF will work and for E=0 slave FF will work. The main difference between these 2 figures is that figure 7(a) has no inversion of clock after passing through the master section, but the inversion occurs in case of figure 7(b). Here, focussing on the figure 7(b) as it has lesser quantum cost.

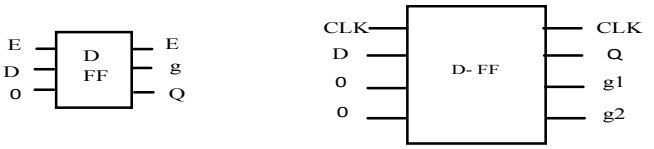

Fig.8. (a) Block diagram of D-FF; (b) Block diagram of Master-Slave D-FF

Figure 8 shows the block diagrams of D-FF and Master-slave D-FF. Block diagram of D-FF will be used as a

slave FF for other Flip-Flops and block diagram of Master-slave FF will be used in designing of Shift Registers.

Table.2. A comparison of Reversible Master-slave FF

D-FF Comparison	Quantum Cost (Qc)	Delay (D)	Garbage Output(*G*)
[Rice 2006] [8]	47	35	12
[Chuang and Wang 2008] [11]	13	13	3
[Thapliyal and Vinod 2007] [9]	13	13	4
[Thapliyal and Ranganathan 2010][14]	12	12	3
Proposed Design with MF only	10	11	3
% improvement w.r.t. [14]	16	8	-
Proposed design with MF and F	11	11	3
% improvement w.r.t. [14]	8	8	-

4.3. Proposed Reversible SR-Latch and Flip-Flop

Characteristic equation of SR-latch is defined as

$$Q+=S+R\overline{Q} \tag{2}$$

This equation produces an unstable state of SR-FF (for S=1 and R=1, Q+ cannot be determine) with this reversible SR-FF become complicated. With the assumption that for S=1 and R=1 the output Q+=Q a new characteristic equation has been made. New characteristic equation can be written as

$$Q+=(S \oplus Q).(S\oplus R)\oplus Q \tag{3}$$

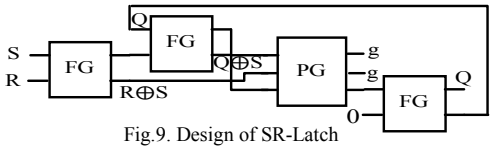

Fig.9. Design of SR-Latch

Characteristic equation of clock enabled SR-latch is

$$Q+=E.(S\oplus Q).(S\oplus R)Q+ \overline{E}.Q \tag{4}$$

The following figure 10 shows the clock enabled Reversible SR-latch. Figure 10(a) and figure 10(b) are the new design of SR-FF with reduced quantum cost and delay and both design have same working. As figure 10(b) is optimized more in terms of delay and garbage we are explain that.

Let us consider for the case in which S=1, R=0, E=1 and initially Q=0 for figure 12. Outputs of first FG is o/p1=1,o/p2=1. Outputs of second FG is o/p1=0, o/p2=1. Outputs of second FG are the input of PG gate and PG gate produces the outputs as o/p1=1, o/p2=0, o/p3=1. O/p3 of PG gate is applied as input of MF gate

produces the output as o/p1=1, o/p2=0, o/p3=1 and o/p3 is Q+ and final output Q+=1(desired output) and this is SET condition of SR-FF. The two FG gates are used to copying the output and provide feedback to the input.

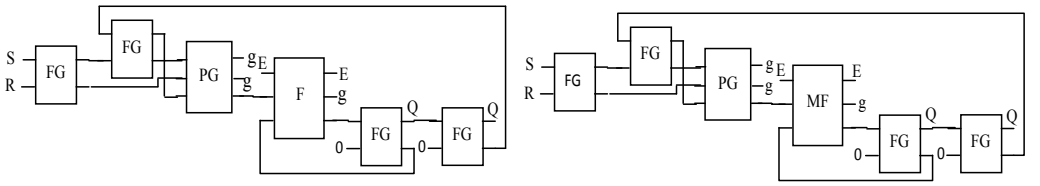

Fig.10.(a) Clock enabled SR-Latch (SR-FF) using PG and F gate ;(b)lock enabled SR-Latch (SR-FF) using PG and MF gate

Table.3. A comparison of clock enabled SR-Latch

D-FF Comparison	Quantum Cost (Qc)	Delay (D)	Garbage Output(*G*)
[[Thapliyal et al. 2005][7]	34	16	6
[Thapliyal and Ranganathan 2010][14]	16	16	3
Proposed Design using PG and F gate	13	13	3
% improvement w.r.t. [14]	19	19	-
Proposed design with MF and F	12	12	3
% improvement w.r.t. [14]	25	25	-

4.4. Proposed Reversible Master Slave SR-FF

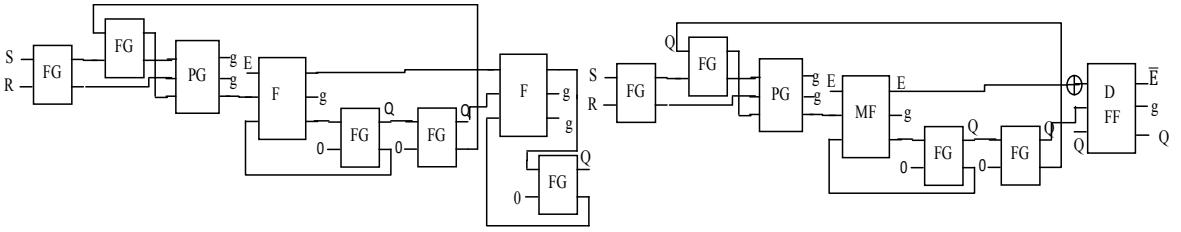

Fig.11.(a) Master-slave SR-FF using PG and F gate without clock inversion; (b) Master-slave SR-FF using PG and MF gate with clock inversion

Figure 11(a) shows the master-slave SR-FF. Fredkin gate is used to avoid the need of clock inversion. In figure 11(b) we used D-FF as a slave-FF and it needed clock inversion. When E=1 master-FF will work and for E=0 slave-FF work.

Table.4. A comparison of Master-slave SR-FF

D-FF Comparison	Quantum Cost (Qc)	Delay (D)	Garbage Output(*G*)
[Thapliyal and Ranganathan 2010][14]	22	22	4

Proposed Design using PG and F gate	19	19	4
% improvement w.r.t. [14]	14	14	-
Proposed design with PG and MF gate	18	17	4
% improvement w.r.t. [14]	18	23	-

4.5. Reversible JK-Latch and Flip-Flop

The characteristic equation of reversible JK-Latch is written as

$$Q^{+}=J\overline{Q}+\overline{K}Q \tag{5}$$

The following figure shows the design of JK-Latch**.** This proposed design has a quantum cost 5 and delay 5Δ.

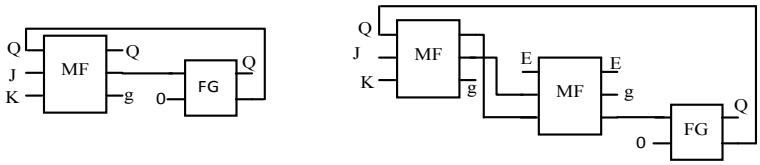

Fig.12.(a) Design of Reversible JK-latch; (b) Design of Clock enabled reversible JK-Latch

The characteristic equation of clock enabled reversible JK -latch can be written as

$$Q^{+}=E(J\overline{Q}+\overline{K}Q)+\overline{E}Q \tag{6}$$

The Flip Flop will store the input data only when E=1 and for E=0 FF remains in its previous state. Design of clock enable Reversible SR-Latch is shown in the figure 12(b).

Design of Clock enabled JK-Latch uses two MF gate and one FG gate. Let us consider a case for J=1, K=1 and Q=0. When clock signal goes high i.e. E=1 then output of first MF gate is o/p1=0, o/p2=1, o/p3=1. Two outputs of first MF gate are applied as input to the second MF gate. Outputs of second Mf gate are o/p1=1, o/p2=1, o/p3=1. O/p3 is the desired output i.e. Q+=o/p3=1, this is TOGGLE condition of JK-FF.FG gate is used to copy the output and provide feedback to the input.

Table 5. A comparison of Clock Enabled Reversible JK-Latch

D-FF Comparison	Quantum Cost (Qc)	Delay (D)	Garbage Output(*G*)
[Chuang and Wang 2008][11]	32	32	3
[Thapliyal and Ranganathan 2010][14]	12	12	3
Proposed Design	9	9	3
% improvement w.r.t. [14]	25	25	-

4.6. Reversible Master-Slave JK-Flip-Flop

The following figure shows the design of Master-Slave JK-FF

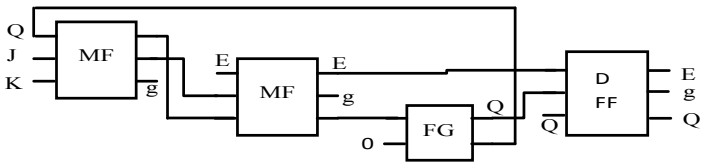

Fig.13. Design of Reversible Master-slave JK-FF

Master-FF works when E=1 and slave-FF will work for E=0, since there is clock inversion applied through NOT gate.

Table.6. A comparison of master slave JK-FF

D-FF Comparison	Quantum Cost (Qc)	Delay (D)	Garbage Output(*G*)
[Rice 2006] [8]	64	44	14
[Chuang and Wang 2008] [11]	39	39	4
[Thapliyal and Vinod 2007] [9]	23	22	5
[Thapliyal and Ranganathan 2010][14]	18	18	4
Proposed Design	15	14	4
% improvement w.r.t. [14]	21	26	-

4.7. Proposed Reversible T-Latch and Flip-Flop

The characteristic equation of T-Latch can be written as

$$Q^{+} = T \oplus Q \tag{7}$$

The design of reversible T-latch using this characteristic equation is shown in the following figure

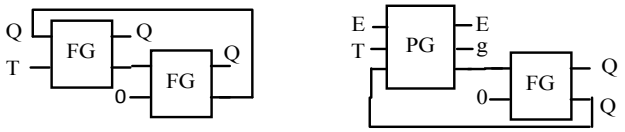

Fig.14.(a) Design of Reversible T-Latch; (b) Design of Clock enabled reversible T-Latch (T-FF)

The characteristic equation of clock enabled reversible T=latch (T-FF) can be written as

$$Q^{+} = T.E \oplus Q \tag{8}$$

When E=1 then T FF store the data at its input and for E=0, T-FF remains in its previous state. Figure 14(b)

shows the design of reversible T-FF.

Consider the case for T=1 and Q=1, when clock signal is high i.e. E=1 the PG gate produces outputs as o/p1=1, o/p2=0, o/p3=0. PG gate output O/p3 is desired output i.e. Q+=o/p3=0, this is the TOGGLE condition of T-FF. FG gate is used to copy the output and provide feedback to the input. For E=0 the FF remains in its previous state.

4.8. Proposed Reversible Master-Slave T-Flip-Flop

Design of reversible Master-Slave T-FF is shown in the following figure

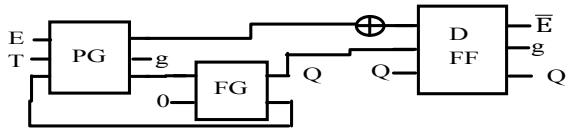

Fig.20. Design of reversible master-slave T-FF

5. Conclusion

Flip-flops are the basic building blocks of any sequential machine. Here, we have shown some novel designs of reversible flip-flops, briefly explains their operations and analyzed their cost metrics in a tabular form. The architectures have been compared with the existing designs available in literature which corresponds to our success in terms of quantum cost, ancilla and garbage. We have also analyzed the worst case delay, hardly addressed earlier of all the proposed designs. These designs could be a good option to be used as the data storage elements of the future quantum computers. We are currently focusing on the front end & back end design of these architectures to implement them in ASIC or FPGA applications.

References

[1] R. Landauer, “Irreversibility and heat generation in the computational process”, IBM Journal of Research. Dev. 5, 183-191, 1961.

[2] C. H. Bennett, R. Landauer, “The fundamentals physical limits of computation”.

[3] C. H. Bennett, “Logical reversibility of computation”, IBM Journal of Research. Devel. 17,525-532, 1973.

[4] Tommaso Toffoli, “Reversible Computing,” Automata, Languages and programming, 7th Colloquium of Lecture Notes in Computer Science, vol. 85, pp. 632-644,1980.

[5] E. Fredkin, T. Toffoli, “Conservative logic “, Int. J. Theor. Physics 21, 219-253, 1982

[6] P. Picton, “Multi-valued sequential logic design using Fredkin gates” MVL J. 1, 241-251, 1996.

[7] H. Thapliyal, M. B. Srinivas, M Zwolinski, A beginning in the reversible logic synthesis of sequential circuits. In proceedings of the Int. Conf. on the military & Aerospace Programmable Logic devices, 2005.

[8] J. Rice, “A new look at reversible memory elements”, In proceedings of the International Symposium on circuit and systems. 243-246, 2006.

[9] H. Thapliyal, A. P. Vinod, “Design of reversible sequential elements with feasibility of transistor implementation” In proceedings of the IEEE International Symposium on circuits and system, 625-628, 2007.

[10] J. Rice, “An introduction to reversible latches”’ Computation. J. 51, 6, 700-709,2008.

[11] M.L. Chuang, C.Y. Wang, “Synthesis of reversible sequential elememts” J. Emerg. Technol. Comput. Syst. 3, 4, 1-19, 2008.

[12] Hafiz Md., Md. M. A. Polash, a. S. Md. Sayem, "A novel design of a reversible field programmable gate array",silvar Jubilee conference on Comm. Tech. & VLSI Design (Comm V09), VIT University, Vellore, India. Oct 8-10, 2009, pp 502-503.

[13] Mathew Morrison, Matthew Lewandowski, Richard meana and Nagarajan Ranganathan, "Design of static and Dynamic RAM Arrays using a novel reversible logic gate and decoder", 11th IEEE Int. Conference on Nanotechnology, Oregon, USA, August 15-18, 2011.

[14] H. Thapliyal and N. Ranganathan Design of Reversible Sequential Circuits Optimizing Quantum Cost, Delay, and Garbage Outputs, ACM Journal on Emerging Technologies in Computer Systems, Vol. 6, No. 4, Article14, Pub. Dec. 2010.

[15] Michael a. Nielsen, Isaac L. Chuang, " Quantum Computation Information", Cambridge University Press, New York, USA 2010.

[16] Alak Majumder, Prasoon Lata Singh, Nikhil Mishra, Abir Jyoti Mondal, Barnali Chowdhury ,"A Novel Delay & Quantum Cost Efficient Reversible Realization of 2^i x j Random Access Memory", International Conference on VLSI Systems, Architecture, Technology and Applications (VLSI - SATA 2015), Sponsored by IEEE, Banglore.

[17] Prasoon Lata Singh, Alak Majumder, Barnali Chowdhury, Ranvijay Singh, Nikhil Mishra, "A novel Realization of Reversible LFSR for its application in Cryptography", SPIN 2015, Sponsored by IEEE. (Accepted)