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A new low cost cascaded transformer multilevel inverter topology using minimum number of components with modified selective harmonic elimination modulation

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KEYWORDS

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Abstract In this paper, a novel cascaded transformer multilevel inverter is proposed. The number of the switching devices is reduced in the proposed topology. This topology comprises of a DC source, several single phase low-frequency transformers, two main power switches and some bidirectional switching devices. In this topology, only one bidirectional switch is employed for each transformer. However, in conventional cascaded transformer multilevel inverter, four switching devices are required for each transformer. Therefore, more output voltage levels can be obtained using fewer switching components. Reduction in the number of switching devices which also means reduction in the number of gate drivers results in smaller size and low implementation cost. Switching power losses are also reduced in this topology. Selective harmonic elimination (SHE) technique is applied to the proposed inverter to obtain a high quality output voltage. Simulation and experimental results are also provided to verify the feasibility of the proposed converter.

1. Introduction

During the past few years, multilevel inverters have played a major role in most systems such as large motor drives, flexible AC transmission systems, power quality improvement devices and renewable energy converters [1–3]. Therefore, multilevel inverters have attracted great attention of power electronic engineers. Multilevel inverters benefit from various advantages such as lower switching losses, stepwise output voltage, smaller common mode voltage and lower peak inverse voltage (PIV)

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on switches [4–6]. These advantages make multilevel inverters favorable for many industrial applications.

There are primarily three multilevel converter topologies so-called diode-clamped [7], flying capacitor [8] and cascaded H-bridge with separate DC sources [9]. They provide stepwise voltage with high quality. However, their main disadvantage, which is the excessive number of switching components, restrains their applications. In diode-clamped configuration, regulating the capacitors voltages makes the control scheme complicated. Also, abundant numbers of clamping diodes are required in this topology. Ladder structure of capacitors is used in flying capacitor multilevel inverters. Therefore the volume of the system is enlarged for the necessity of more capacitors. Cascaded H-bridge structure has the advantage of being modular which makes this structure easily expandable for higher number of output voltage levels. However, the need for separate DC voltage sources for each module and the number of switching components are the main disadvantages for this configuration. For overcoming these problems, novel topologies of multilevel inverters are presented in recent years. The cascaded transformer multilevel topology is proposed [10,11]. This topology employs one single DC voltage source and several isolated low-frequency transformers. However, number of switching components is still to be reduced. In [12,13], new topologies are proposed in order to reduce the number of switches. Therefore, the main disadvantage of cascaded transformer inverter is that this topology has many switching components.

Switching strategies of multilevel inverters are categorized into high switching frequency methods such as SPWM strategy [14] and low switching frequency techniques, often equal to fundamental switching frequency of the components, which create stepwise output voltage waveform [15]. Second category comprises of three major switching strategies so-called optimized harmonic stepped waveform [16], selective harmonic mitigation PWM [17], and optimal minimization of the THD [18]. Selective harmonic elimination is as effective method to mitigate the low-order harmonic components.

In this paper, a cascaded H-bridge reduced switch multilevel inverter is proposed which comprises of several low-frequency transformers. The number of switching components and gate drivers are minimized in this topology which reduced the size and the cost of realization. Selective harmonic elimination technique is employed to reach to a high quality output voltage. Simulation and experimental results indicate the ability of the proposed topology in voltage generating.

2. Cascaded transformer H-bridge multilevel inverter

In this section the traditional topology and two new topologies introduced for transformer based multilevel inverters are reviewed. Traditional cascaded H-bridge cells multilevel inverter needs several numbers of semiconductors and separated DC sources, these several numbers of isolated sources and components are difficult to be provided and controlled so this is a serious drawback for this topology. To eliminate need for several isolated DC sources the cascaded transformer H-bridge multilevel was introduced in which the transformers are used instead of DC sources. Attempting reach to a less component topology and obtain an optimized topology have led to appear some new topology which utilize fewer semiconductors and

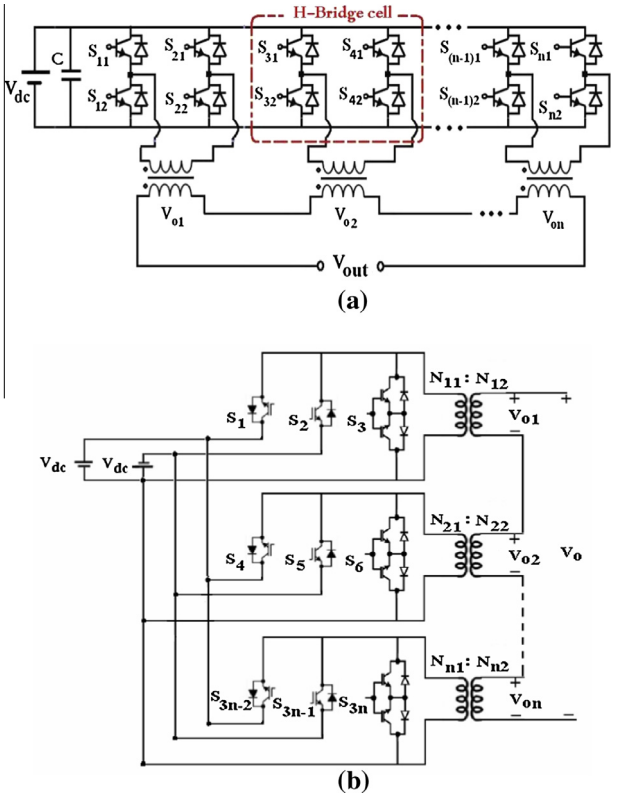

Figure 1 (a) The traditional cascaded transformer multilevel inverter, (b) the CTITS topology.

DC sources. Cascaded transformer inverter with two DC sources (CTITS) is one of the newest less component topologies of transformer based multilevel inverter which have been introduced in [19]. Fig. 1a and b show traditional topology of cascaded transformer multilevel inverter and the CTITS respectively.

3. Proposed inverter structure

Fig. 2 shows the proposed cascaded multilevel inverter. This topology consists of a DC voltage source and several single phase transformers. As it is shown in Fig. 2, two main switching devices are used to change the polarity of the input voltage and for each transformer a bidirectional power switch is used.

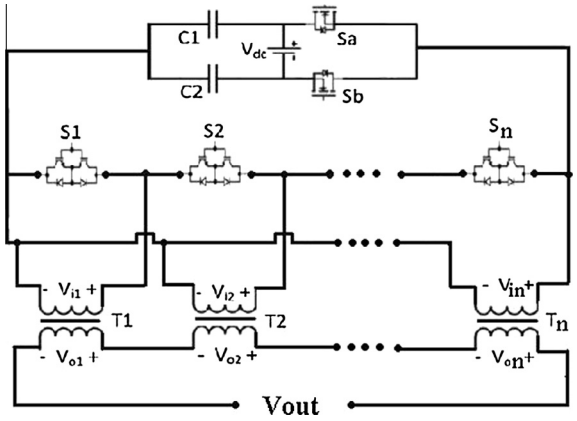

Figure 2 Circuit diagram of the proposed multilevel inverter.

Table 1 Switching pattern for 9 level inverter.

Steps	Switches position [1 = on & 0 = off]						V_{out}
	Main switches		Common switches				
	S_a	S_b	S_1	S_2	S_3	S_4	
1	1	0	1	1	1	0	V_{dc}
2	1	0	1	1	0	1	$2V_{dc}$
3	1	0	1	0	1	1	$3V_{dc}$
4	1	0	0	1	1	1	$4V_{dc}$
0	0	0	1	1	1	1	0
−1	0	1	1	1	1	0	$-V_{dc}$
−2	0	1	1	1	0	1	$-2V_{dc}$
−3	0	1	1	0	1	1	$-3V_{dc}$
−4	0	1	0	1	1	1	$-4V_{dc}$

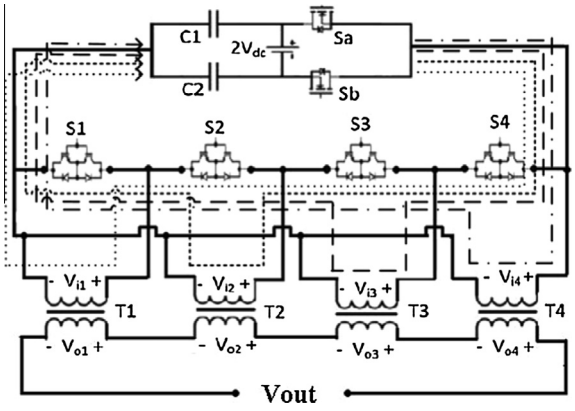

Figure 3 Current flow path in the proposed inverter.

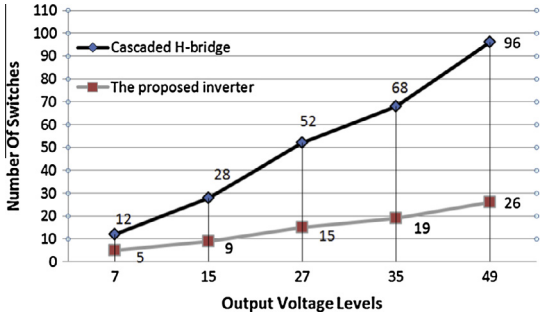

Figure 4 Number of power switches to realize m-level voltage.

In comparison with the conventional cascaded H-bridge multilevel inverter, numbers of switching devices are decreased. Respectively, the numbers of the gate drivers are reduced. Compare to the traditional transformer based multilevel inverters, using less switching devices as well as gate drivers in the proposed topology leads to cutting down in power losses, smaller size and low cost. In the proposed configuration, the number of switches required to obtain an m-level output voltage can be given as follows:

$$SW = (m+1)$$

$$D = \frac{(m+3)}{2}$$

$$N = \frac{(m-1)}{2}$$

where SW, D and N are the number of the unidirectional switches, gate driver circuits and transformers respectively.

The secondary sides of the transformers are connected in series to synthesize the stepwise output voltage. The output phase voltage can be given by summing the output voltages of the transformers as below:

$$V_{o_n} = \frac{1}{a} V_{dc}$$

$$V_{out} = \frac{1}{a}\sum_{m=1}^{n} V_{o_m} \quad (1)$$

where V_{o_n}, a, V_{out} and n are the secondary voltage of each transformer, transformer ratio of transformers, output voltage of the inverter and number of cascaded transformers.

3.1. Operation of the proposed inverter

In the proposed inverter, each transformer can generate three voltage levels zero, $+V_{dc}$ and $-V_{dc}$. The secondary sides of the transformers are series connected. Therefore, the maximum voltage can be generated from the configuration shown in Fig. 2 is $+nV_{dc}$ where n is the number of transformers. Different switching states and their corresponding output voltage for the proposed inverter are shown in Table 1. For symmetric operation of the inverter, turn ratios of the transformers are chosen to be the same. The current flow path of the proposed inverter is also shown in Fig. 3.

3.2. Voltage and current ratings of the switches

The most important criteria for selecting the proper power switches are peak inverse voltage (PIV) and current ratings of the switches. Assuming the input voltage as V_{dc}, in the proposed topology the maximum PIV of each bidirectional switches is $V_{dc}/2$, whereas each bidirectional switch is consists of two unidirectional switches it can be concluded that the maximum PIV of each switch is $V_{dc}/4$. However, the main switches have the maximum PIV of V_{dc}. Comparing the PIV of switches in the proposed topology to the traditional topology in which each switch is exposed to the maximum PIV of V_{dc} it is deducible that employing switches with a remarkable reduction on PIV is one of the most significant benefits of the proposed topology.

Table 2 Comparison study of mentioned topologies.

Inverter type	The traditional topology	The CTITS	The proposed topology
Numbers of levels	m	m	m
Transformers	$(m-1)/2$	$(m-1)/2$	$(m-1)/2$
Unidirectional switches	$2*(m-1)$	$2*(m-1)$	$(m+1)$
Gate driver circuits	$2*(m-1)$	$3/2*(m-1)$	$(m+3)/2$

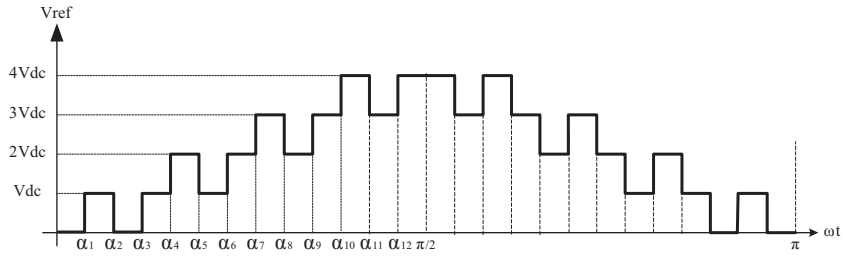

Figure 5 Half cycle phase voltage of a 9-level inverter.

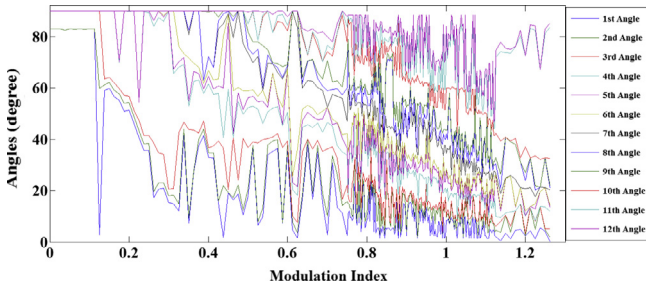

Figure 6 Optimum switching angles versus modulation index.

The current ratings of the switching devices are different from each other in the proposed inverter. Considering the load current as 1 Pu, the current ratings of the main switches are 4 Pu in the inverter shown in Fig. 3. The current ratings of the transformer switches vary from 1 Pu to 4 Pu. Using switches with higher and various current rating is the main disadvantage of the proposed inverter.

3.3. Comparison study

This paper aims to reduce the number of components used in multilevel inverters. Among the conventional cascaded multilevel inverters, cascaded H-bridge requires a few numbers of

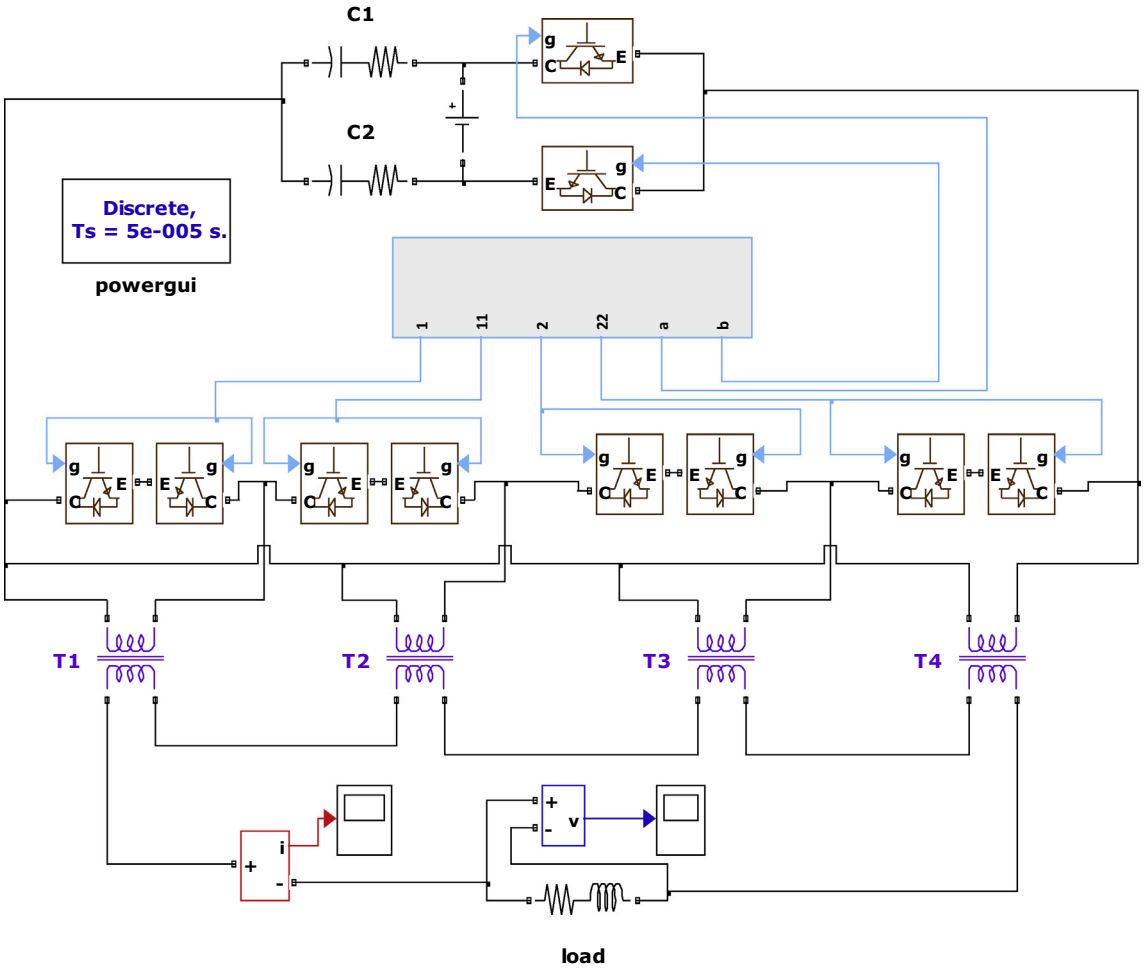

Figure 7 Simulation model of the proposed topology.

Table 3 Components specification of Simulation model.

Components	Specification
Input source	
DC source (V)	10
Switches	
Semiconductor	IGBT/Diod
Internal resistance Ron (Ohms)	1e−3
Snubber resistance Rs (Ohms)	1e5
Transformers	
Nominal power and frequency [Pn (VA) fn (Hz)]	[500 60]
Winding 1 parameters [V1 (Vrms) R1 (Pu) L1 (Pu)]	[12 0.072 9.1673e−004]
Winding 2 parameters [V2 (Vrms) R2 (Pu) L2 (Pu)]	[12 0.216 2.1e−6]
Magnetization resistance and inductance [Rm (Pu) Lm (Pu)]	[147.46 0.39114]
Load (series connected R–L)	
Resistance (Ohms)	100
Inductance (H)	0.18
Reference waveform	
Maximum magnitude (V)	40
Frequency (Hz)	60

components. Number of switching components in conventional cascaded transformers inverter and the proposed inverter is compared in Fig. 4. As it can be seen in Fig. 4, the proposed topology requires fewer switching components for realizing *m*-level output voltage. For instance, seven-level output voltage is obtained using five switches in the proposed inverter. However, twelve switches are required for the same output voltage in cascaded transformers multilevel inverter. Additionally, there is a gate driver for each switch. As we reduce the number of switching components, the number of gate drivers is decreased too. Therefore, reduction of switches minimizes the cost and the size of the system. To provide more investigation the proposed topology is compared with two other topologies of cascaded transformer inverters that are introduced before. Table 2 exhibits the comparison of the proposed topology, the CTITS and the traditional cascaded transformer inverter.

4. Switching strategy

In multilevel inverters, modulation methods are necessary to obtain a high quality output voltage [20]. Many modulation techniques have developed recently such as pulse with modulation (PWM) and space vector modulation (SVM). Among these techniques, selective harmonic elimination (SHE) and THD minimization approaches are applied to multilevel inverters in order to eliminate harmonic components of the output voltage. SHE method aims to select the switching angles so that the low-order harmonics of the output voltage could be eliminated [21]. In this paper, SHE–PWM method is applied to a 9-level inverter. In this method, each level in switched several times in a period in order to increase the degrees of freedom (DOF) in our equations [22]. Fig. 5 illustrates the half-cycle output voltage of the inverter. As it is shown in Fig. 5, the number of switching in each level is three. Fourier analysis of Fig. 5 is given as follows:

$$V_a = \sum_{n=1}^{\infty} \frac{4}{n\pi} V_{dc} \sin\left(\frac{n\pi}{2}\right)[\cos(n\alpha_1) - \cos(n\alpha_2) + \cos(n\alpha_3) + \cos(n\alpha_4) - \cdots + \cos(n\alpha_{12})]\sin(n\omega t) \quad (2)$$

The main purpose of SHE–PWM approach is to determine $a_1 - a_{12}$ such that the selected harmonic components are suppressed. In this paper, evolutionary algorithms are used to

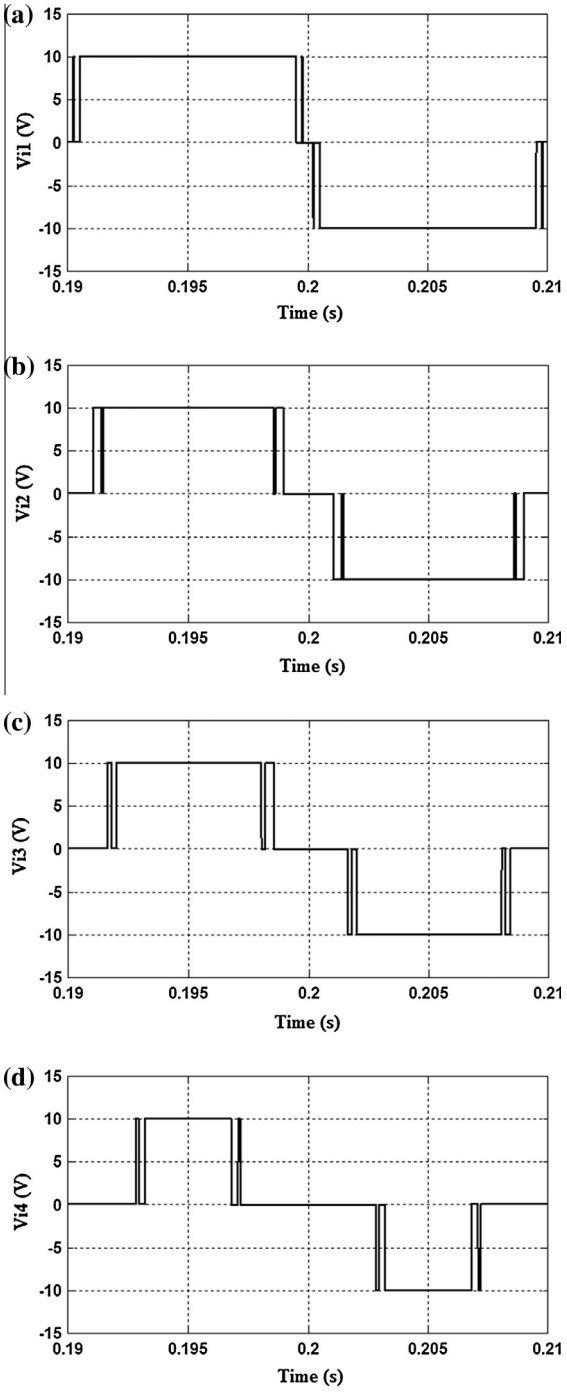

Figure 8 Input voltages of the transformers (a) V_{i1}, (b) V_{i2}, (c) V_{i3}, (d) V_{i4}.

determine the proper switching angles. A recently developed Imperialist Competitive Algorithm (ICA) is employed [23]. Using ICA algorithm, an objective function will be minimized and the optimum switching angles will be determined. The objective function is considered as follows:

$$\text{Objective}: \quad 100 * \left\{ \left| M - \frac{|V_1|}{nV_{dc}} \right| + \frac{|V_5| + |V_7| + \cdots + |V_{31}| + |V_{35}|}{nV_{dc}} \right\} \tag{3}$$

where M is the modulation index and n is the number of transformers. The corresponding optimum switching angles versus the modulation index is depicted in Fig. 6.

5. Simulation results

In order to demonstrate the operation of the proposed inverter, the configuration shown in Fig. 3 is simulated using MATLAB/Simulink software. Fig. 7 shows the simulation model of proposed topology. Specifications of the assumed structure for simulation acts are listed in Table 3 According to the optimum switching angles determined by ICA algorithm, the input voltages of the transformers are shown in Fig. 8a–d. As it is mentioned above to obtain a multilevel output voltage the secondary sides of the transformers are series connected. Therefore, the output voltage is the sum of the outputs of the transformers. The waveforms of the output voltage and load current are shown in Fig. 9. Because the magnitude of load current is much smaller than output voltage to make it explicit in the presence of output voltage its magnitude is multiplied to 50; the harmonic spectrum of the output voltage and current is depicted in Fig. 10a and b respectively. According to these figures the THD of output voltage is 11.52% however the simulated output voltage contain third harmonic and its submultiples which can be eliminated in three phase application this amount of THD is acceptable. Since the inductive feature of the load makes the waveform of the load current more sinusoidal the load current has lower THD.

6. Experimental results

The circuit configuration, shown in Fig. 2, is used to verify the operation of the proposed inverter. A hardware prototype 9-level inverter is implemented as shown in Fig. 11. This inverter consists of four transformers, two main switches and four bidirectional transformer switches. Prototype components specifications are summarized in Table 4. The input DC voltage is 20 V. Whereas the performances of an inverter are appraised in the presence of a load with inductive load a series connected RL load is considered in the simulation and experimental acts. The feature of employed RL load at the output stage of the inverter is $R = 140\ \Omega$ and $L = 260$ mH. In order to measure the load current voltage of a series resistance with $R = 75\ \Omega$ is shown. Fig. 12 shows the output voltage and output current

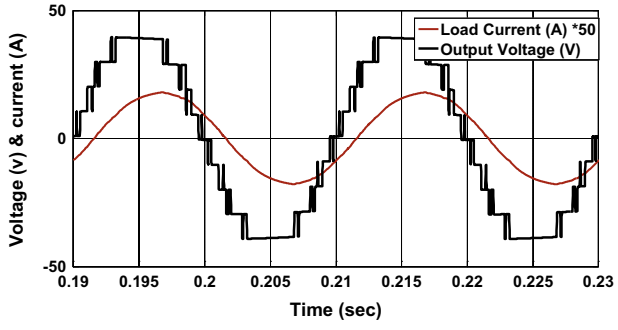

Figure 9 Waveforms of (a) output voltage, (b) output current.

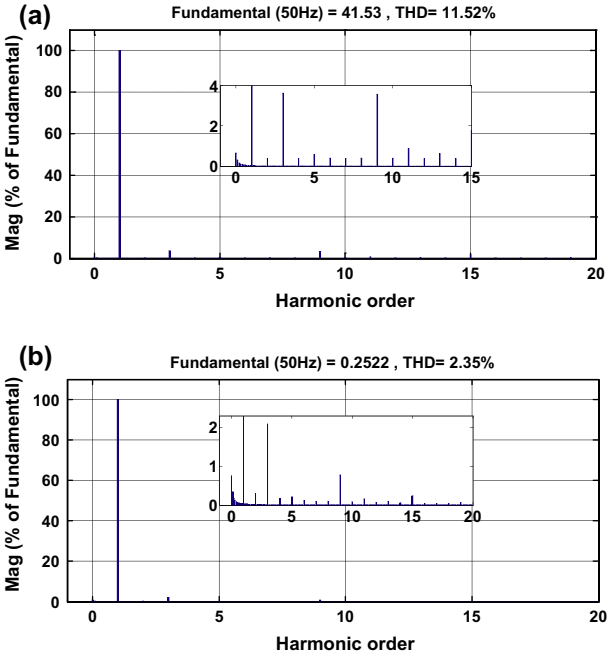

Figure 10 Harmonic spectrum of (a) output current, (b) output voltage.

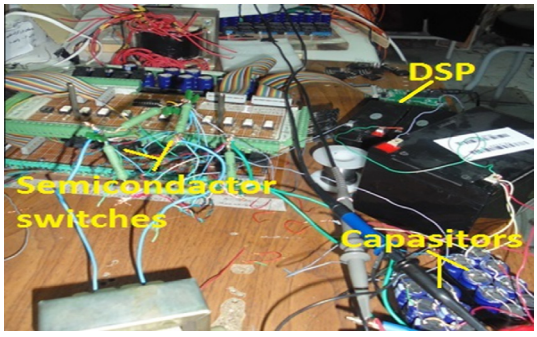

Figure 11 Picture of the hardware implementation.

Table 4 Prototype components specification.

Components	Specification
Switches	IRFP250
Gate insulator	TLP250
Buffer	HC573
Snubber	10 Ω + 20 μF
Processor	DSP TMS320F28335

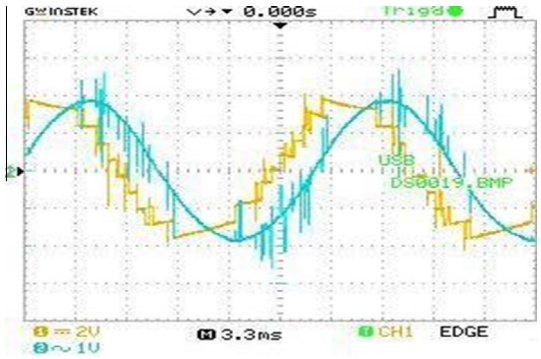

Figure 12 Measured (a) output voltage, (b) output current.

of the proposed inverter. As it is shown in Fig. 12, the output voltage is a stepwise symmetric waveform. The proposed inverter can efficiently minimize the number of components used in multilevel inverters. Also, results prove the ability of the proposed inverter in generating the desired output voltage. Furthermore according to Fig. 12 there appear some ramps on the steps of the output voltage these ramps are resulted from the dropped voltages over the leakage impedances of the transformers so they can be eliminated by using some optimized transformers that leads to obtain more high quality output voltage.

7. Conclusions

In this paper, a cascaded transformer multilevel inverter with reduced number of switching components is presented. The proposed topology utilizes low-frequency single-phase transformers and a DC voltage source. This configuration can reduce the number of switches in comparison with conventional cascaded transformer multilevel inverters. Selective harmonic elimination technique is applied to mitigate the low-order harmonic components. In order to verify the operation and performance of the proposed inverter, simulation and experimental results using a single-phase 9-level multilevel inverter prototype are provided.

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