A 1.36 μW 312–315 MHz synchronized-OOK receiver for wireless sensor networks using 65 nm SOTB CMOS technology

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Article info

Abstract

The paper presents a receiver design operating at 312–315 MHz frequency band for wireless sensor networks. The proposed architecture uses synchronized on-off-keying (S-OOK) modulation scheme, which includes clock information together with data, providing self-synchronization ability for the receiver without a separate clock and data recovery circuit. In addition, a new technique is also proposed to reduce active time of the RF front-end for better energy efficiency. The receiver architecture is verified by using discrete RF modules and FPGAs, then VLSI design is carried out on 65 nm Silicon-On-Thin-Buried-Oxide (SOTB) CMOS technology and simulated using SPICE models to illustrate effectiveness of the proposed architecture. Post-layout simulation shows –58.5 dBm sensitivity with 1.36 μW and 8.39 μW power consumption corresponding to 10 kbps and 100 kbps data rate, respectively.

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1. Introduction

In low-power, short-range wireless sensor networks, minimizing power consumption of RF transceivers in general and of receivers in particular is one of the most attractive issues. In RF receivers, usually RF front-ends and local oscillators consume most of power [1–3]. Therefore, many solutions were proposed to decrease power of the RF front-ends and the local oscillators. With the RF detection receivers, local oscillators, mixers and IF band pass filters are eliminated, simplifying structure and reducing power consumption significantly. However, the RF amplifiers still dissipate dominant power in those receivers such as in [4,5]. Their power consumption is around 60 μW with more than 50% of their power dissipated by the RF amplifiers.

The work in [6] demonstrated a receiver structure in which the RF amplifier is not employed. Alternatively, RF signal is sampled directly from output of the antenna by intermittent samplers, so that power consumption of the receiver is reduced to 38 μW. Similarly, the receiver in [7] uses an active RF detector to detect baseband signal directly, therefore it can achieve 10 μW power consumption. However, sensitivities of those receivers are limited, –55 dBm and –50 dBm in [6,7] respectively, because there is no RF amplifier before RF envelope detection.

In [8], a technique was used to overcome trade-off between power consumption and sensitivity, in which the receiver uses cascaded RF amplifiers to achieve high sensitivity and the RF amplifiers operate intermittently to decrease power consumption. However, speed of intermittent operation must be higher than data rate several times because of asynchronization between transmission and reception. As a result, data rate is limited and power consumption of the RF amplifier is still large in comparison with that of subsequent blocks.

In this paper, we propose a receiver architecture operating in the range of frequency 312–315 MHz with S-OOK modulation scheme, allowing received data to be synchronized with output clock using a simple digital circuit, no separate clock and data recovery circuit is required. Taking advantage of low carrier frequency, RF signal is converted to digital stream after the RF front-end by a comparator and then that stream is processed digitally. Therefore, no IF or baseband amplifier is needed. Furthermore, the RF front-end works intermittently with intermittent speed as double of data rate despite asynchronization between transmission and reception sides, improving energy efficiency of the receiver. By simulation, power consumption of the receiver can be reduced to 1.36 μW at data rate of 10 kbps. To the best of the authors’ knowledge, this number is the lowest power of the receivers ever reported.

The paper is organized as follows. Section 2 describes system architecture and operation of the receiver. Section 3 is architecture verification using discrete components and FPGAs. Section 4 presents VLSI design on 65 nm SOTB CMOS process with simulation.
results. Finally, discussion and conclusion are drawn in Sections 5 and 6, respectively.

2. Architecture and operation of the receiver

2.1. S-OOK signal

Transmission signal used for this receiver is synchronized-OOK (S-OOK) signal. The S-OOK pulse modulation was first proposed in [9] for Impulse Radio Ultra-Wide Band (IR-UWB) transceivers. Here we modify it for narrow band applications. Fig. 1 shows format of the transmission signal, in which \(T_b\) is bit duration. In the conventional OOK modulation, RF carrier occupies whole duration of bit “1” and absents in whole bit “0” (Fig. 1a). On the other hand, in the S-OOK modulation, RF signal is composed of two kinds of RF pulses, synchronization pulses and data pulses. Bit “1” corresponds to 2 RF pulses, the first one is synchronization pulse and the other is data pulse, whereas bit “0” corresponds to only synchronization pulse (Fig. 1b). The cycle of the synchronization pulses is \(T_p\) equal to the bit duration. Each RF pulse has the width of \(T_p\). \(T_p\) must be large enough so that the signal is still narrow-band, different from the signal described in [9], where each pulse is an ultra-wide band pulse. The distance between synchronization and data pulses in [9] is a certain value between 0 and \(T_p\), while this distance must be half of \(T_p\) in our architecture.

2.2. Receiver architecture

Fig. 2 is block diagram of the proposed receiver, consisting of a variable-gain RF amplifier, a comparator and a digital part. The digital part includes a baseband extractor, a window generator and a demodulator and synchronizer. After the multi-stage cascaded RF amplifier, input RF pulses including synchronization pulses and data pulses are clipped by the comparator to become pulse groups with rail-to-rail level. Magnitude of the RF amplifier output needs to be larger than threshold of the comparator, therefore high RF gain is necessary to achieve required sensitivity. To avoid strong non-linearity at large input level, the variable-gain RF amplifier is adopted instead of a fixed-gain amplifier. The baseband extractor generates baseband signal, which is fed to the window generator and the demodulator and synchronizer. The window generator uses the baseband signal to create a window (RFENA) which enables the RF front-end in the period that covers the beginning part of each input RF pulse and disables it in other time. The demodulator and synchronizer extracts output data and synchronization clock for next processing. In this architecture, the digital part operates continuously, while the RF front-end including the RF amplifier and the comparator operates only when the RFENA window is high. Therefore, power consumption of the circuits is reduced significantly.

![Fig. 1. (a) Conventional OOK signal. (b) S-OOK signal.](image-url)

![Fig. 2. Block diagram of the proposed receiver.](image-url)

![Fig. 3. Schematic of the digital part.](image-url)
2.3. Operation

Fig. 3 describes detailed schematic of the digital part, in which the baseband extractor, the LongPulse generator and the ShortPulse generator have same schematic as shown in Fig. 4. NComparator stands for numerical comparator, used to differentiate from the comparator of the RF front-end.

The timing chart in Fig. 5 describes operation of the receiver. When START goes up, RFENA is high, enabling the RF front-end. The receiver is ready to receive input RF signal from the antenna (Fig. 5b). The input RF signal is amplified by the RF amplifier, then directly converted to rail-to-rail pulse stream by the comparator (Fig. 5c and d).

2.3.1. Baseband extraction

After the comparator, the baseband pulse chain is detected by the baseband extractor. Considering Fig. 4, the COUNTER1 is triggered by a rising edge at the IN0 input. During the COUNTER1 counting, the OUT0 output is asserted and other incoming rising edges at IN0 are ignored. OUT0 is cleared only when the COUNTER1 reaches an upper limitation value, which is assigned by the CONST input. For the baseband extractor, CONST is set by A0 in Fig. 3. At the output of the baseband extractor, we get baseband signal named BBSIGNAL as shown in Fig. 5e. A0 is chosen so that the falling edge of BBSIGNAL is later than the last pulse of each input pulse group.

2.3.2. Window generation

The first rising edge of BBSIGNAL will start the COUNTER0 in the window generator, which operates based on SYSCLK (Fig. 5f). When the COUNTER0 reaches \( N - 1 \), where \( N = T_b/(2 \times T_{SYSCLK}) \), it will be restarted by the rising edge of a BBSIGNAL pulse, which can be data or synchronization pulse (Fig. 5g). In the case of bit "0", there is no data pulse, the COUNTER0 will restart automatically when reaching \( N / C_0 \). At first, RFENA raises together with START to listen the input RF signal (Fig. 5h). After that, RFENA is cleared if COUNTER0 \( \geq n \) and set again if COUNTER0 \( \geq (N - m) \), n and m are chosen so that the window RFENA has a desired width (Fig. 5i). By that way, RFENA is generated to enable the RF front-end every time the input RF pulse is incoming. Since operation of the window generator is
decided by the rising edge of the input RF pulse, the falling edge of RFENA can be set earlier than end of the input RF pulse to reduce active time of the RF front-end, resulting in further reduction of power consumption of the receiver.

2.3.3. Demodulation and synchronization

After getting baseband pulses, data and corresponding clock are generated by the demodulator and synchronizer. The timing chart in Fig. 6 describes demodulation and synchronization processes [9]. ShortPulse and LongPulse are generated by the Short-Pulse generator and the LongPulse generator, respectively (Fig. 4). Their operation is same as the baseband extractor. The difference is only upper limitation values of the COUNTER1 (CONST). In this case, CONST is set to N/2 and N + N/4 for ShortPulse and LongPulse respectively so that ShortPulse is shorter than T_by_2 and LongPulse lasts longer than T_by_2. The output data (ODATA) is latched by the falling edge of LongPulse and the data clock (DCLK) is simply inverse of LongPulse. Depending on desired data rate, N is assigned to a suitable value based on the equation N = T_by_2/(2 x TSYSCLK).

The solution that RF front-end is gated by a window pulse was presented in [10] for IR-UWB receivers. However, the receiver in [10] uses a delay-locked loop (DLL) with a digital controlled delay line, a SAR (successive approximation register) controller, a divider and a phase detector. It is very complex and consumes large amount of power. They have to transmit many sub-bits for both bit “1” and bit “0” with known sub-bit period and use a clock signal to track the input pulse chain, therefore energy efficiency is limited. Moreover, a preamble transmission is also required to establish synchronization. In contrast, the solution presented here requires only a counter and two numerical comparators. Hence the structure is very simple.

Although we do not use a close loop such as DLL to synchronize RFENA with the RF input, but RFENA is always generated timely by using S-OOK modulation. We will calculate maximum frequency error between transmitter clock source and receiver clock source with that the window RFENA is still generated properly.

RFENA is designed to rise at T_early before the input RF pulse (Fig. 5h). Assume that variation of frequency for both receiver clock source and transmitter clock source is δ. It means maximum error between the transmitter and receiver clock sources is 2δ. Since the COUNTER0 is reset and re-synchronized at least once after every bit duration of T_by_2, the maximum timing error is accumulated in only one bit duration. In the case that the incoming bit stream contains only bit “0”, after each bit duration, T_early changes a maximum amount:

\[
\Delta T_{\text{early max}} = \frac{1}{DR(1 - \delta)} - \frac{1}{DR(1 + \delta)} = \frac{2\delta}{DR(1 - \delta)}
\] (1)

where DR = 1/T by_2 is data rate. If the desired T_early = 2TSYSCLK and it is allowed to vary from 1TSYSCLK to 3TSYSCLK, following inequality is yielded:

\[
\Delta T_{\text{early max}} = \frac{1}{DR} \cdot \frac{2\delta}{1 - \delta^2} \leq TSYSCLK
\] (2)

For example, if SYSCLK is 25 MHz and data rate is 100 kbps, δ can be derived: \(\delta \leq 2E^{-3}\). In practice, this value is very relaxed. With typical crystals, frequency variation is around 20 ppm (part per million), i.e. 20E–6, much better than the allowed value as calculated above.

3. Architecture verification

In this section, we describe experiment to verify the proposed architecture using a variable gain amplifier, a comparator for the RF front-end and a FPGA for implementation of the digital part. Here the Analog Device amplifier AD8369 with maximum gain of 34 dB, the Texas Instruments comparator LMH7220 and the Altera Statix IV FPGA are used for experiment. The Maxim switch MAX4636 is used to switch supply for the RF front-end (Fig. 7). The digital part of the receiver is implemented to operate at data rates of 1 kbps, 5 kbps and 10 kbps. A 10 MHz clock is used for the system clock. The window RFENA has the width of 1.5 μs.

A 313 MHz all-digital transmitter is also implemented to communicate with the receiver. Fig. 8 shows block diagram of the transmitter. The power amplifier is switch-mode type (SMPA) [11], therefore the whole transmitter can be implemented completely on a FPGA. Figs. 9 and 10 are waveforms and envelope of the output spectrum of the transmitter respectively at 10 kbps data rate, each synchronization and data pulse has the width of 4 μs.

Fig. 11 shows experiment setup, in which the receiver and the transmitter communicate at a distance less than 1 m. Fig. 12 describes measured real-time waveforms of the receiver and corresponding transmitted data. It can be seen that the data is demodulated correctly with a delay smaller than one bit duration. Fig. 13 is the measured BER characteristic of the receiver with different data rates. At 1 kbps and 5 kbps, BER < 1E–3 with Pin ≥ -45 dBm.

![Fig. 7. Receiver for verification.](image)

![Fig. 6. Demodulation and synchronization.](image)
At 10 kbps, BER < $1E^{-3}$ with $P_{in} > -44$ dBm. We can see, when input power is larger than the minimum values, BER performance is almost same with different input levels. It can be explained that once the output of the RF amplifier is over threshold of the comparator, reliability of the receiver mostly depends on the digital part. The column diagram in Fig. 14 is current consumption breakdown from 3.2 V supply of the RF amplifier and the comparator according to data rates of 1 kbps, 5 kbps and 10 kbps. Currents at normal operation are also shown for comparison.

It can be seen that, the receiver works properly (BER < $1E^{-3}$) with the range of input power from $-44$ dBm to more than 5 dBm and the RF circuits dissipate power much smaller than that of the conventional operation.

4. VLSI design on 65 nm SOTB CMOS process

Silicon-On- Thin-Buried-Oxide (SOTB) CMOS technology, one of FD-SOI CMOS processes, has been developed recently with low
It has been proved that the SOTB CMOS process is one of the best candidates for ultra-low power, low voltage applications [13,14]. In previous section, the proposed architecture of the receiver was verified by using some discrete components and FPGAs. Experiment on the prototype system indicates that the architecture helps improve energy efficiency considerably. However, the power consumption of the prototype receiver is still large because of using the high voltage components. In addition, the window for the RF front-end is large and data rate is low because of long connections between the components. In order to illustrate effectiveness of the proposed architecture in comparison with state-of-art works, in this section, we present the receiver design on 65 nm SOTB CMOS process. Then simulation results will be shown for comparison.

4.1. Circuit design

Fig. 15 is schematic of the RF circuits. The RF amplifier is implemented by cascading 5 stages. Fully differential topology is employed to compensate transient caused by RFENA. The first stage is single-ended-to-differential converter, next stages are fully differential. CMOS switches are added below current sources of each stage. Gain of the RF amplifier can be controlled digitally by 3 bits, providing 4 gain settings. The variable resistor is composed of PMOS transistors as shown in Fig. 15. The 50 \( \Omega \) resistor is shunted to ground for input matching. This matching method causes high noise figure, however it is suitable for low power target. After the matching resistor, a resonant tank with loaded-Q factor larger than 10 is used for band selection. By post-layout simulation, the RF gain can be tuned from 26 dB to 58.4 dB at 315 MHz (Fig. 16). Fig. 17 shows noise performance of the amplifier with maximum gain. At 315 MHz, noise figure is 28.7 dB. The comparator includes a differential-to-single-ended converter and a variable-threshold inverter. When enabled, the RF amplifier and the comparator consume a total current of 103 \( \mu \)A from 1 V supply.

The digital circuit as described in Fig. 3 is designed using standard-cell libraries. SYSCLK is 25 MHz, the RFENA window has the width of 360 ns. Data rate can be set to 100 kbps, 50 kbps or 10 kbps. The digital circuit of the receiver is supplied a voltage of 0.6 V, smaller than supply voltage of the RF front-end to save power. It consumes a current of 0.98 \( \mu \)A. Fig. 18 is layout picture of the receiver. The active core occupies an area of 385 \( \times \) 188 \( \mu \)m\(^2\). The transient analysis result at 100 kbps data rate with input power of -50 dBm is shown in Fig. 19. It can be seen that RFENA, ODATA and DCLK are generated properly, agreeing with the timing charts in Figs. 5 and 6. The graph in Fig. 20 lists up power consumption of the receiver at different data rates based on physical layout simulation. At the data rate of 10 kbps, power consumption of the RF front-end is reduced to be comparable with that of the digital circuit, resulting in total 1.36 \( \mu \)W power consumption of the receiver.
To evaluate the effectiveness of the proposed architecture, we assume that the comparator and the digital circuit in Fig. 2 are replaced by an envelope detector and a baseband amplifier, the RF amplifier operates continuously. In this case, the receiver becomes a conventional RF detection receiver (Fig. 21). If power consumption of the envelope detector and the baseband amplifier is small, power consumption of the conventional OOK receiver approximates the power consumption of the RF amplifier (103 lW). The column chart in Fig. 22 shows the comparison between power consumption of the proposed S-OOK receiver and that of the conventional OOK receiver. It can be seen that at the data rate of 10 kbps, the proposed architecture provides 98.68% power reduction in comparison with the conventional receiver.

4.2. Sensitivity analysis

In fact, digital circuits have been known as highly immunity with noise. Hence, sensitivity of the receiver depends on how reliably the comparator differentiates desired signal and noise. Following [15], noise floor contributed by the stages before the input of the comparator is calculated:

\[ N_{\text{floor}} = -174 + 10 \log_{10}BW + NF, \]  

where \( N_{\text{floor}} \) is expressed in dBm, \( BW \) is input bandwidth (Hz), \( NF \) is noise figure (dB) of the RF amplifier. With 30 MHz bandwidth of the RF amplifier, the noise floor can be derived:

\[ N_{\text{floor}} = -174 + 10 \log_{10}(30 \times 10^6) + 28.7 \approx -70.5 \text{ (dBm)} \]

Typically, signal level is required to be higher 12 dB than noise floor to detect signal reliably. It means \( \text{SNR}_{\text{min}} \) is 12 dB, yielding:

\[ P_{\text{in, min}} = N_{\text{floor}} + \text{SNR}_{\text{min}} = -70.5 + 12 = -58.5 \text{ (dBm)} \]

Table 1 shows performance comparison between the proposed receiver and state-of-art works. It should be noticed that the receiver designed on 65 nm SOTB CMOS process with the proposed architecture consumes much smaller power than that of others in the table. In terms of energy efficiency, the receivers in [6,16] are better than our work, however their sensitivities are limited, -55 dBm and -50 dBm respectively.

5. Discussion

As can be seen from previous sections, the proposed receiver has some disadvantages, such as data rates can be set to only some predetermined values. With S-OOK modulation, the data rate is
also limited since one data bit needs two RF pulses. However, the proposed receiver can solve the trade-off between sensitivity and power consumption. High sensitivity can be achieved by using a high gain RF amplifier, but power consumption of the RF amplifier and other analog circuits is minimized because of low duty cycled operation. In this case, power consumption of the digital part contributes a significant portion in total power dissipation of the receiver. It suggests that power consumption of the receiver can be optimized by reducing supply voltage of the digital circuits. Because in general, digital circuits can work reliably at supply voltage lower than that of analog circuits.

6. Conclusion

In this paper, the S-OOK receiver operating in 312–315 MHz frequency band was presented. This is the first time S-OOK
Performance comparison.

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a Simulation results.

This work was performed as “Ultra-Low Voltage Device Project” funded and supported by the Ministry of Economy, Trade and Industry (METI) and the New Energy and Industrial Technology Development Organization (NEDO). The authors would like to thank VLSI Design and Education Center (VDEC), the University of Tokyo, Japan in collaboration with Synopsys, Inc., Cadence Design Systems, Inc.

Acknowledgments

References