Available online at www.sciencedirect.com

SciVerse ScienceDirect

Physics Procedia 37 (2012) 1594 – 1599

Physics Procedia

TIPP 2011 - Technology and Instrumentation in Particle Physics 2011

A non-linearity correction method for fast digital multi-channel analyzers

Ziru Sang[a,b], Feng Li[a,b], Yuan Yao[a,b],Ge Jin[a,b*]

[a]*State Key Laboratory of Particle Detection and Electronics*
[b]*University of Science and Technology of China, Jinzhai Road 96#, Hefei,230026, P.R.China*

Abstract

Fast digital multi-channel analyzers (FDMCA) which based on flash ADCs have been intensively used recently. The FDMCA is different from traditional MCAs which based on Wilkinson ADCs. The non-linearity, including the integral non-linearity (*INL*) and differential non-linearity (*DNL*), mainly arising from flash ADCs, degrade the accuracy of fast digital MCAs. To improve the non-linearity of FDMCA, a practical off-line correction method has been proposed in this paper. The non-linearity features of the FDMCA system is obtained by a special measurement previously. In light of that the non-linearity of a system is inherent; the non-linearity can be eliminated by comparing the data between the general measurement and the special one.

keywords: nonlinearity correction, multichannel analyzer, pulse-height analyzer, data processing;

1. Introduction

The multi-channel analyzer plays an important role in nuclear physics experiment. More and more flash ADCs have been used in MCAs, instead of Wilkinson ADCs, forming digital MCAs. The flash ADCs have higher sampling rate, lower dead time. Beyond that, any computational operation could be realized after the signal pulse has been converted into numerical data, which is more convenient than the conventional analog hardware. However, the strong non-linearity is reported when flash ADCs are widely used in digital signal processing system. A typical FDMCA's frame is showed in Fig.1.The analog signal should be digitalized as early as possible to reduce the interferences of the analog signal, while simplifying the circuit. The digital processing system completes the histogram measurement utilizing the

* Corresponding author. Tel.: +86-551-3606492; fax: +86-551-3606495.
E-mail address: sangzr@mail.ustc.edu.cn; goldjin@ustc.edu.cn.

1875-3892 © 2012 Published by Elsevier B.V. Selection and/or peer review under responsibility of the organizing committee for TIPP 11.
Open access under CC BY-NC-ND license. doi:10.1016/j.phpro.2012.02.484

data originated directly from flash ADCs. The non-linearity degraded the measure effort of digital system seriously, especially the accuracy of FDMCAs. To obtain the accurate data with FDMCAs, a correction method is developed to improve non-linearity mainly arising from flash ADCs. Actually, the non-linearity of system is dependent on many factors, such as ADC, preamplifier, anti-alias filter, and so on.

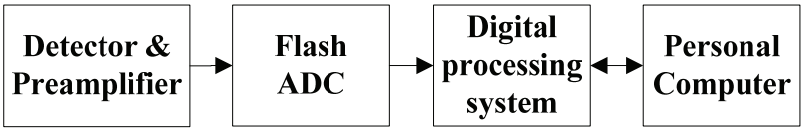

Fig.1. A typical FDMCA frame based on flash ADC as same as the most digital system.

2. The principle of non-linearity correction method

2.1. The Discrete Representation of INL and DNL

The non-linearity about ADC is defined after correcting the measured levels for gain and offset [1]. Such definition is followed in the discussion in this paper. In FDMCA, the output code of fast ADC is the channel of FDMCA. The non-linearity of FDMCA could be associated with the non-linearity of flash ADC, which is defined as $INL[k]$ and $DNL[k]$ respectively. The integral non-linearity error $DNL[k]$ associated with code transition level *k* is the difference between the measured and nominal code transition levels, after correcting the measured levels for gain and offset [1]. It can be expressed as

$$INL[k] = v_k - u_k, \quad k = 1,2...M; \tag{1}$$

Where, v_k is the transition level of code D_{k+1} in practical, and u_k is the nominal code transition level.

Similarly, the difference, after correcting for gain error, between the *k-th* code bin width *W[k]* and the nominal code bin width *Q*, divided by the nominal code bin width is called *DNL[k]*.

$$DNL[k] = \frac{W[k] - Q}{Q}, \quad k = 1,2...M; \tag{2}$$

$$W[k] = v_k - v_{k-1}, \qquad k = 1,2...M, \quad v_0 = 0V;$$

The *INL[k]* and *DNL[k]* are all expressed in *LSB*. The relationships between them can be described as

$$INL[k] = \sum_{1}^{k-1} DNL[k], \qquad k = 2...M; \tag{3}$$

2.2. Correcting formula

A graphical staircase representation (Fig.2) of a deterministic conversion law, where the abscissa reports the analogue input x, while the corresponding digital output codes are reported along the vertical axis. u_k in absolute units is reported as the nominal code transition level of code *k*, while the one in a real ADC which is different from the nominal one is reported as v_k. Fig.2 shows difference between ideal and actual transfer function. The analogue input voltage levels from u_k to u_{k+1} should be converted into digital code D_{k+1} by ADC in ideal. Actually, the output digital code D_{k+1} from the ADC reports the analogue input voltage level from v_k to v_{k+1}, which are not consistent with u_k and u_{k+1} because of non-linearity. So, the count of D_{k+1}, similarly, the counts of the *(k+1)-th* channel don't report the real count of pulse whose magnitude is from u_k to u_{k+1}. It needs to be corrected.

The inconformity of code transition level leads to the error in frequency histogram (Fig.3), where the abscissa reports the output code of the analogue input pulse-height, also called channel of MCAs, while the count of each code is reported along vertical axis. As Fig.3 shows, the count of D_{k+1} should report the

analogue input voltage levels from u_k to u_{k+1} in idea. However, the origin count of output code D_{k+1} reports the analogue input voltage levels from v_k to v_{k+1}. Corrected count which is more approximate to the real pulse-height count of analogue input voltage levels from u_k to u_{k+1} is the area surround by the dashed line in Fig.3. *f(u)* is defined as the probability density function of input analogue voltage, while *g(v)* is the frequency histogram of the origin data. So, the counts can be expressed as formula (4).

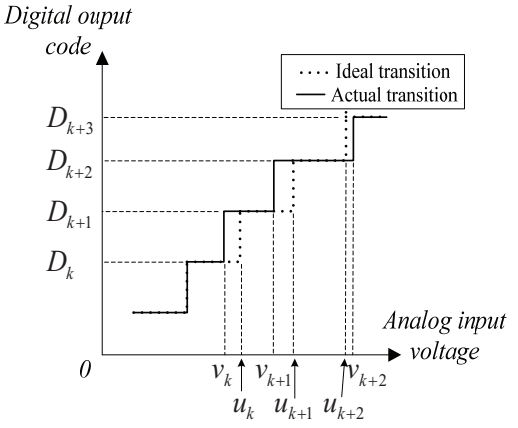

Fig.2. Transfer function of MCA

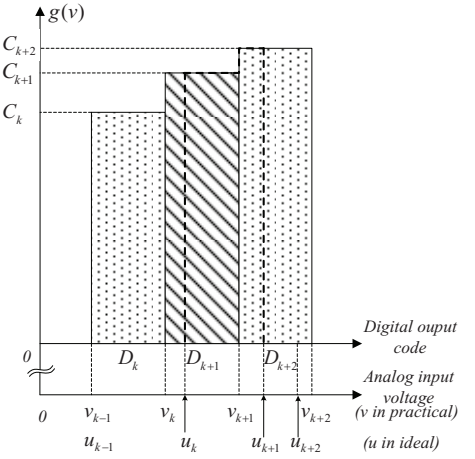

Fig.3. The non-linearity analysis in histogram.

$$F(u)=\int_{u_k}^{u_{k+1}} f(u)du=\int_{INL[k]+v_k}^{INL[k+1]+v_{k+1}} g(v)dv=\int_{INL[k]+v_k}^{INL[k]+v_k+Q} g(v)dv \tag{4}$$

Assuming the total count of all channels is *N* and *C(v)* depending on input analogue voltage is the count of each channel, Eq. (4) can be rewritten as

$$F(u)=\int_{INL[k]+v_k}^{INL[k]+v_k+Q}\frac{C(v)}{N}dv=\frac{1}{N}\int_{INL[k]+v_k}^{INL[k]+v_k+Q}C(v)dv. \tag{5}$$

Eq. (5) can be written in another expression depending on $DNL[k]$, which is more easily obtained by the Eq. (6) utilized a precise sliding pulse generator (SPG) calibrating the FDMCA, at the $C[k]$ is more than one million.

$$DNL[k]=\frac{C[k]-\frac{N}{M}}{\frac{N}{M}} \tag{6}$$

$$F(u)=\frac{1}{N}\int_{\sum_{i=1}^{k}DNL[i]+v_k}^{\sum_{i=1}^{k}DNL[i]+v_k+Q}C(v)dv \tag{7}$$

The count of *(k+1)-th* channel after correcting is,

$$F(u)*N=\int_{\sum_{i=1}^{k}DNL[i]+v_k}^{\sum_{i=1}^{k}DNL[i]+v_k+Q}C(v)dv \tag{8}$$

3. Experimental results

To evaluate this correction method, some tests with both FDMCA and a commercial MCA (Ortec® MCB Connections-32) have been made. The ADC is the commercially available chip which performs the analog-to-digital conversion of input signals. 12-bits data from ADC, equivalently 4096-channels are available. A FPGA is used as a digital processor completing the histogram.

Firstly, a special measurement should be completed to obtain the non-linearity data of the developed FDMCA system. A sliding pulse generator (SPG Model: FH-442H; the non-linearity error of the SPG is less than 0.15 %.) produced by Beijing Sixin Technology Company is used to make measurement of the $DNL[k]$. The output pulse-height is modulated by a slope voltage.

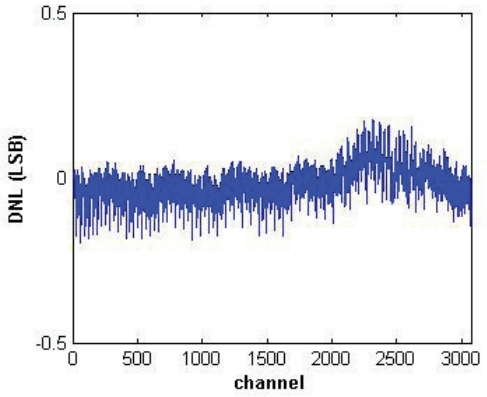

Fig.4. DNL of developed FDMCA system.

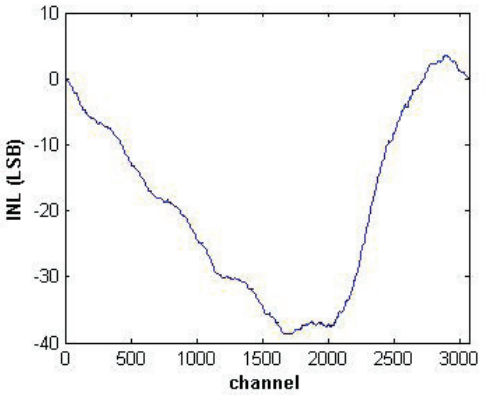

Fig.5. INL of developed FDMCA system.

3.1. Electrical Tests

A SPG is used to measure the FDMCA, while a commercial MCA for comparison described in Fig.6.

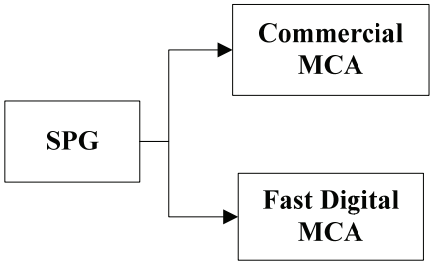

Fig.6. The electrical tests. A sliding pulse generator （SPG) is used. A commercial MCA is used for comparison.

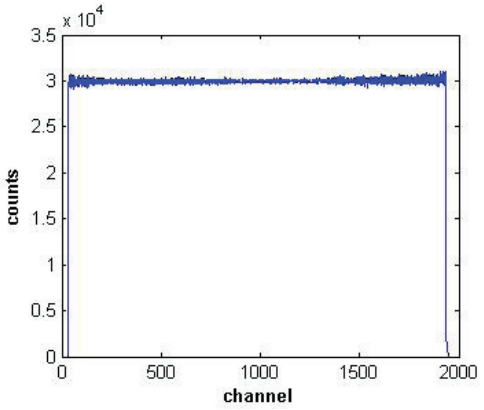

Fig.7. The SPG measured by commercial MCA.

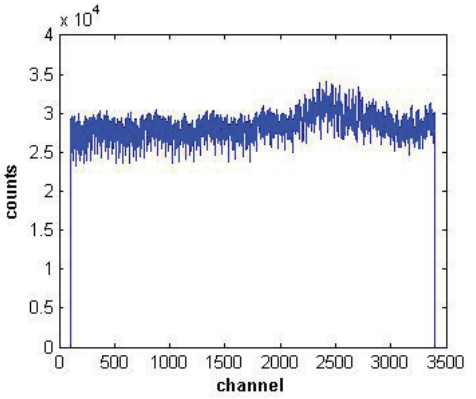

Fig.8. The SPG measured by developed FDMCA system without correction.

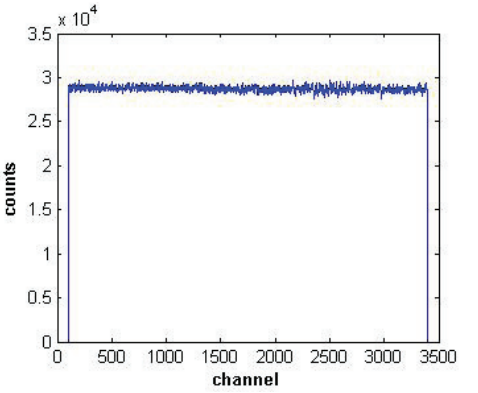

Fig.9. The SPG measured by developed FDMCA system with correction.

The Fig.9 is the corrected result with formula (10) utilizing the $DNL[k]$ obtained in Fig.4. A comparison data shows in table Ⅰ. The DNL of the FDMCA has been improved from 19.60% to 4.02% after correction, and the INL has been improved from 1.27% to 0.13% after correction. Which is closed to the commercial one's DNL is 3.70% and INL is 0.07% on the same condition.

TABLE Ⅰ
THE DNL & INL COMPARISON AMONG COMMERCIAL ONE, BEFORE CORRECTION AND AFTER CORRECTION WITH THE DEVELOPED MCA

	DNL	INL
Commercial MCA	3.70%	0.07%
Before correction	19.60%	1.17%
After correction	4.02%	0.13%

The results are the absolute value of the maximum among all the possible value of index *k*.
The data isn't precisely about the MCA, also including the statistical fluctuation and the nonlinearity of SPG.

3.2. Radiation Source Tests

Other measurements are made with radiation sources described in Fig.10. An Au-Si surface barrier semi-conductor detector (Model: GM40II2215) produced by CNNC Beijing Nuclear Instrument Factory is utilized to detect the alpha radiation from source. The energy resolution of the SSB detector is *22KeV* using ^{241}Am 5.486MeV alpha source, which is given by the specification of SSB detector. Certainly, synchronous tests are made with the commercial MCA for comparison. The mixed source is mixed with ^{239}Pu and ^{241}Am which is used to calibrate the system.

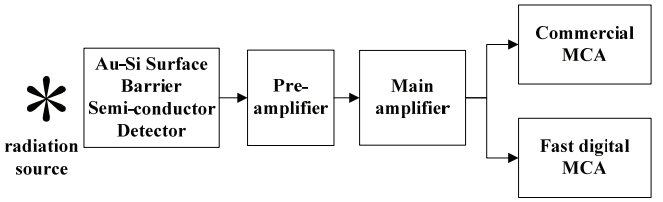

Fig.10. ^{241}Am is measured for radiation source tests. A commercial MCA is also used for comparison.

^{241}Am release the alpha particle mainly at 5.486Mev. The value from the commercial MCA is 5.485Mev. The value after correction is much closer to it. Also the energy resolution is higher with correction than before. The FDMCA's accuracy has been improved.

TABLE Ⅱ
A COMPARISON AMONG COMMERCIAL ONE, BEFORE CORRECTION AND AFTER CORRECTION

	radiation source	*FWHM (keV)*	*E (MeV)*	*Energy resolution (%)*
Commercial MCA	^{241}Am	43.7	5.485	0.80
before correction	^{241}Am	74.1	5.522	1.34
after correction	^{241}Am	71.1	5.488	1.30

4. Conclusion

The non-linearity mainly arising from flash ADC degrades the accuracy of FDMCA. A non-linearity correction method for FDMCA system is presented. Electronics tests and radiation tests are completed to evaluate this correction method. The electronics tests indicate that it's a great improvement to differential non-linearity and integral non-linearity. The radiation tests indicate that the correction method is more helpful in improving measure accuracy than precision. This result indicated that in the digital system with flash ADCs, the integral non-linearity is more obvious than the differential non-linearity.

Acknowledgements

This work was performed under the auspices of Natural Science Foundation of China under grant number NNSF11075152. The authors also thank Dr. Yinping Hao and Dr. Jinhua Sun who have given much help for tests and Dr. Minyang Zhen for advice in language.

References

[1] Dominique Dallet, Jose Machado da Silva, *Dynamic Characterisations of Analogue-to-Digital Converters.* 2005: Springer
[2] Herman P. Lima et al., "A Fast Multichannel-Analyzer for Radiation Detection Applications," *IEEE Trans. Instrumentation and Measurement*, vol. 53, pp. 378–383, April. 2004.
[3] S. Buzzetti et al., "High-Speed FPGA-Based Pulse-Height Analyzer for High Resolution X-Ray Spectroscopy," *IEEE Trans. Nuclear Science*, vol. 52, pp. 854–860, August. 2005.
[4] Hiroyuki Takahashi et al., "On the correction of the differential non-linearity arising from discrete values for a digital signal processing system," *Nucl. Instrum. Methods Phys. Res. A*, vol. 373, pp. 119–123, 1996.
[5] WANG Jingjin et al., *Nuclear electronics*. Volume One. Beijing: Atomic Energy Press, 1985, pp. 90-93.
[6] Yang Hua-ting, "An improvement in differential non-linearity of analog-digital conversion," *Nuclear Electronics & Detection Technology,* vol. 21, No. 6, pp. 423–426, November. 2001.
[7] João M. Cardoso et al., "A High Performance Reconfigurable Hardware Platform for Digital Pulse Processing," *IEEE Trans.on nuclear science* , vol. 51, pp. 921–925, June. 2004.
[8] V.V. Sushkov, "Differential non-linearity compensation in ADCs employing charge redistribution in an array of binary weighted capacitors," *Nucl .Instrum .Meth. Phys. Res. A, vol.450, pp.119–126, 2000.*
[9] D. Alberto, "FPGA implementation of digital filters for nuclear detectors," *Nucl .Instrum .Meth. Phys. Res. A, vol.611, pp.99–104, 2009.*
[10] Cosimo Imperiale, "On nuclear spectrometry pulses digital shaping and processing," *Measurement, vol.30, pp.49–73, 2001.*
[11] Dinh Sy Hien, "Development of a fast 12-bit ADC for a nuclear spectroscopy system," *Nucl .Instrum .Meth. Phys. Res. A, vol.457, pp.356–360, 2001.*