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Room temperature spalling of thin silicon foils using a kerfless technique

Pierre Bellanger and João Serra
Faculdade de Ciências da Universidade de Lisboa/SESUL, Campo Grande Ed-C8,1749-016 Lisboa, Portugal

Abstract
An important factor for cost reduction of solar electricity is the reduction of silicon material quantity used for making a solar cell. It is well known in the PV industry that kerf losses associated with wafering are a limiting factor in the efforts to reduce material usage and some techniques have been developed to address this issue. The kerfless wafering technique described in this paper provides both things: a thin silicon layer foil while avoiding the sawing step. This technique consists of three steps: (i) dispensing a stress inducing layer on the silicon surface of a slab; (ii) thermal processing to activate the stress and detach a thin silicon layer of silicon; (iii) a chemical cleaning to obtain a flat thin foil of silicon. This technique was used with an epoxy stress inducing layer to obtain thin silicon foils, demonstrating for the first time the capability to obtain several foils out of the same substrate and using only room temperature cooling step, unlike other authors who used dipping in liquid nitrogen. The relationship between epoxy layer and foil thickness is presented, along with foils with bulk minority carrier lifetimes of 80 μs.

Keywords: thin foils; kerfless, spalling

1. Introduction
An important factor for cost reduction of solar electricity is the reduction of silicon material quantity used for making a solar cell. It is well known in the PV industry that kerf losses associated with wafering are a limiting factor in the efforts to reduce material usage and some techniques have been developed to tackle this issue [1][2][3]. The kerfless wafering technique addressed in this paper provides both things: a thin silicon layer foil while avoiding the sawing step. This technique [4] consists of three steps: (i) dispensing a stress inducing layer on the silicon surface of a slab; (ii) thermal processing to activate the stress and detach a thin silicon layer of silicon; (iii) a chemical cleaning to obtain a flat thin foil of silicon. A stress inducing layer based on epoxy materials was used with this technique showing that large areas of silicon can be detached [5]. The SLIM-cut process was used here also with an epoxy
stress inducing layer to obtain several thin foils out of the same substrate using a room temperature cooling step. Previous work reported in the literature with epoxy stress inducing layers required dipping the samples in liquid nitrogen to produce the foils [5]. In this work we present the relationship between epoxy layer and foil thickness and also minority carrier lifetime measurements of the foils.

2. Experimental setup

The experimental setup used in this work is a very simple one. After manual dispensing, the thickness of the epoxy layer can be adjusted by a spinning technique. A thermal treatment is done at 150 C to cure the epoxy, giving it the mechanical properties that will induce enough stress, upon cooling, to initiate a crack propagation that will produce the thin foil by spalling. The parent substrate can be reused by applying a new epoxy layer and repeating the process.

2.1. Sample preparation

In these experiments, Czockralski (Cz) monocrystalline silicon samples with a <100> orientation and an original thickness of 720 μm were used. Both p and n-type wafers were tested. The silicon samples were diced in pieces of 3 x 5 cm² and a laser notch is performed below the sample, or on the side along the edge, to define the position where the crack initiation will take place.

![Process flow for foil extraction and substrate reuse.](image)

In this work, besides the normal sample preparation with one notch below the sample, near the edge, a sample with three notches at the edge was also prepared to demonstrate that several foils can be extracted from the same starting substrate. The process flow used for all samples is shown in Fig. 1.

3. Results

To study the relationship between epoxy layer thickness and resulting silicon foil thickness, samples with different epoxy thicknesses were prepared. In all studied cases the epoxy curing was performed at a temperature around 150ºC during 1h, using the lamp furnace shown in Fig. 1. Several foils were obtained by spalling at room temperature.
From Fig. 2 we can see that for thinner foils, a lower thickness epoxy must be used. However there is a limit for this, since the process will not start at room temperature for very low thickness of the epoxy layers. Although all results presented here were obtained by cooling at room temperature, the use of negative temperatures could be necessary to create enough stress to initiate crack propagation for very thin epoxy layers. Unlike previous published work on the use of an epoxy layer [5], in this study we didn’t use dipping in liquid nitrogen to induce spalling. Samples were simply cooled at room temperature. This is an important issue when considering possible industrial applications.

Fig. 3. Three foils obtained from the same parent substrate. The black line indicates where the parent substrate broke during the first SLIM-cut lift-off process.

To demonstrate that several foils can be extracted from the same parent substrate we prepared a sample with 3 laser notches at the edge, not below the sample. This geometry has a different relationship between epoxy layer thickness and silicon foil thickness. Numerical simulations of this case indicated that a 900 μm epoxy thickness was required to assure crack propagation at a depth close to 130 micron. Fig. 3 shows the starting parent substrate and the
3 foils that were obtained. We observed that in fact the first foil was the result of crack propagation starting from the notch located closer to the surface where the epoxy layer was deposited. The second and third foils followed the same behaviour. This result shows that the crack initiation is well controlled by these notches and that foil extraction starts from the notch that is closer to the upper surface. An additional interesting point is that no modification or polishing of the substrate was done between the SLIM-cut experiments, proving the process has sufficient margin to work even if the starting surface is not absolutely flat.

It was also observed that the thickness from the first to the third foil is decreasing from 130 to 110 micron, which is an expected trend, since the same epoxy thickness was used in these experiments. This result is in agreement with Hutchinson [6], which describes the relationship between stress inducing layers and resulting spalling foil thickness. Successive foils are thinner because the parent substrate is becoming thinner while the stress inducing layer thickness is unchanged between SLIM-cuts. By adjusting the epoxy thickness, this effect could be compensated in a real situation.

![Sinton lifetime (μs) measurements after etching](image)

**Fig. 4.** Effective minority carrier lifetimes in the three foils. Blue columns show foils before etching, while red columns show foils after 25 μm etching. In the two groups, columns represent foil 1 to foil 3 from left to right.

Fig. 4 shows the effective minority carrier lifetime results measured using SINTON equipment on foils after three SLIM-cut processes. Before the measurement, the samples were cleaned in a H2SO4, H2O2 mixture and HF deoxidation bath. Iodine ethanol solution with a concentration of 0.08 M is used to passivate the surface [7]. Lifetime results presented in Fig. 4 were measured with injection levels between 5x10^{15} and 1x10^{16} cm^{-3}.

The measured lifetime decrease on the samples can be explained by the slight dislocation density increase after several processes due to the high stress conditions, by the thickness decrease effect related to surface recombination and by a possible presence of defects close to the surface. This latter argument is reinforced by the results presented in Fig. 4 showing an increase in lifetime upon etching the samples a few microns. The reduction of lifetime is clearly seen as a new foil is extracted. While crystal defects are increasing, lifetime shows the opposite behavior. However we observed that upon etching, foil lifetime increases markedly, as shown in Fig. 4. This increase in lifetime after etching 25 μm of Si reinforces the connection to the presence of crystal defects close to the surface or possible surface contaminants that are removed upon etching. The foils show very good minority carrier lifetimes, namely the first foil. Assuming a recombination velocity of 100 cm/s provided by the passivation solution, the bulk lifetime is 80 μs. This value gives a diffusion length much larger than the foil thickness.
3.1. Large area foils

In Fig. 5, a large area thin foil is shown to demonstrate that large areas can be obtained using this technique. These thin foils exhibit a typical pattern of the crack propagation as we move away from the laser notch used to create the crack initiation point. Nevertheless, as it can be seen in Fig 5, a complete 5x5 cm$^2$ thin silicon foil (130 micron) can be produced, preserving the initial parent substrate shape.

![Fig 5. Large area (5cm x 5 cm) thin silicon foil. Left image: side where the sample has been lifted-off from the substrate. Right image: side where the epoxy was deposited during lift-off. The arrow indicates the edge where the laser notch was made.](image)

4. Conclusions

In this study we demonstrated that the SLIM-cut technique, using an epoxy based stress inducing layer can be used to obtain several thin foils from the same starting substrate. Unlike previous published results existing in the literature, reporting dipping in liquid nitrogen to induce spalling, only room temperature cooling was used in these experiments. Furthermore, very good minority carrier lifetimes were obtained in these foils, opening the door for good solar cell conversion efficiencies.

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