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Methodological Framework for NoC Resources Dimensioning on FPGAs

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Abstract

The two main challenges involved in prototyping a SoC (System-On-Chip) on a FPGA (field programmable gate array) are optimal tuning of the communication architecture according to the task graph of an application, and dimensioning the FPGA resources. In this paper, we present a methodological framework to estimate the number of resources required for a given communication architecture and task graph. Data analysis was based on a set of synthesized results for a given on-chip network. The most appropriate models were identified using a data mining approach. The evaluation of the models shows that the relative error is less than 5% in most cases. It is therefore possible to estimate the required resources in a short exploration time and without the synthesis steps.

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Keywords: NoC on FPGA, Mathematical models, resource dimensionning, methodological framework, area estimation

1. introduction

NoCs (Network On Chip) have emerged as efficient scalable and low power communication structures for many-core SoCs (System On Chip with several hundred or thousand cores). The designer has to configure the parameters of the NoC according to the application to optimize communication times between cores. Exploring all appropriate solutions is an intensive time process because of the sheer number of parameters required for the NoC. The Field Programmable Gate Array (FPGA) devices are widely used for prototyping systems. FPGA can then be used to emulate the time performances of NoC for each set of parameters in a rapid design space exploration.

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Indeed, emulation provides precise timing and power evaluations in a shorter cycle than simulation [1]. But before emulation, Each NoC candidate has to be synthesized then placed and routed to obtain the number of resources. Resources can be obtained either after the synthesis or after the place and route process. With large FPGAs, this process can take several hours for one NoC candidate. Usually, the designer selects the NoC parameters without exploring all the candidates, thereby saving a significant amount of time in the development process but the chosen solution is not always optimal. Area estimation is important in order to find architectural solutions that: 1) suit the target FPGA concerned 2) correspond to the requirements of the application 3) ensure efficient timing.

Design space explorations for NoCs are mainly based on power consumption and timing on ASIC [1,3,4,5,8]. The evaluation of the impact of various options on the area, the number of cycles and execution time on FPGA is described in [6]. A power area analysis of NoCs in FPGAs was proposed in [7], but was based on analysis of the router only, not of the complete NoC. The authors make the assumption that summing all results leads to the result of the SoC. In [9], the relationship between events occurring in the NoC and energy consumption is modelled using linear regression.

In this paper, we propose a methodological framework to extract the most appropriate mathematical model according to the selected NoC for FPGA resource dimensioning. The framework is based on data collection, data analysis and modelling of a selected NoC. The paper is organized into 3 sections. Section 2 presents the methodological framework and the 3 steps are described: 1. Choice of the structure, 2. Data collection and 3. Data analysis. Section 3 concludes the paper.

2. Methodological Framework

A model for system dimensioning requires accurate estimations of the resources required by the application. First, we describe the characteristics of the FPGA structures explored using our approach. Second, we present the methodological approach for resources dimensioning. The methodological framework is illustrated in figure 1. The methodological framework is split into three steps: 1) choosing the appropriate NoC structure for data analysis, 2) collecting the data required for data analysis, 3) analyzing the data to identify the most appropriate mathematical models.

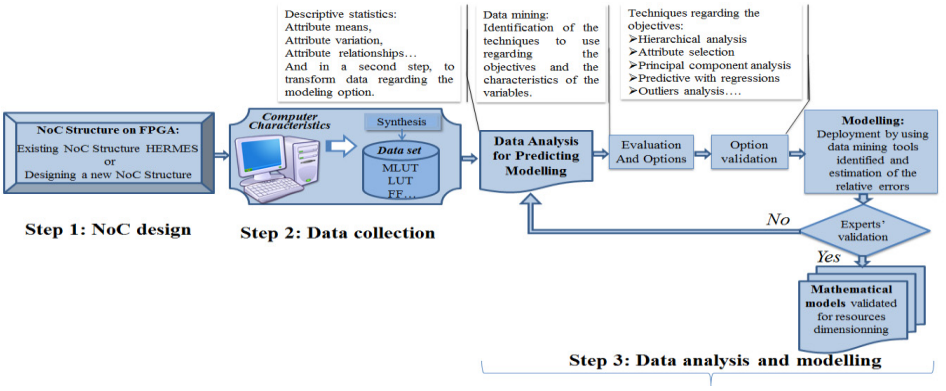


Fig 1. Methodological Framework

A resource usage model for NoC enables the optimization of design parameters under resource constraints. Today, NoC mapping heuristics do not cope with FPGA resources constraints. NoC dimensions are determined before the mapping step. Using mathematical models enables to quickly evaluate the impact of NoC parameters on FPGA resource usage as far as estimation errors are minimized. We now describe the three steps of our methodology.

Step 1: Choice of the structure

The first step is selecting the appropriate NoC structure. Any NoC structure designed in HDL language can be used. Our experiments were conducted on two NoCs, one designed especially for the purpose (AdOCNet –

Adjustable On-Chip Network) and one existing NoC that is, often used in the research community (Hermes) [2]. The NoC structure (topology, flow control, virtual channel, scheduling and routing algorithm) is fixed for a model. Table 1 shows the characteristics of the two NoCs used for resource modeling.
A 2D mesh topology is commonly used since it fits best to the FPGA's topology. The two NoCs differ in their flow control and the number of virtual channels. Such differences have a significant impact on FPGA resource usage.

Table 1. NoC characteristics

	Topology	Flow control	Virtual channel	Scheduling	Routing algorithm
Hermes	2D Mesh	Credit based	2	Round robin	XY
AdOCNet	2D Mesh	Handshake	No	Round robin	XY

Step 2: Data Collection

The data were the FPGA resources in the post synthesis report in the VIVADO 2012 development tool (integrating the Xilinx synthesis tool) according to the NoC parameters. These resources may differ for other software, but are basically of the same type. From each synthesis processes, the results stored in a database are:

- n_1: the number of routers in the X-axis.
- n_2: the number of routers in the Y-axis.
- n_3: the depth of the buffer.
- n_4: the size of the flit.
- *LUT*: the number of Look Up Table used.
- *MLUT*: the number of Memory LUT used.
- *FF*: the number of Flip Flop used.

Step 3: Data Analysis

The complete database of observed results was analysed to identify links between variables and LUT, MLUT, FF regarding the variables n_1, n_2, n_3 and n_4. The aim was to mathematically model the relation between the input configuration of the NoC and material resources used without going through the synthesizing step.

3a. Data mining

The aim of data mining is to automatically locate useful information among large quantities of data. Data mining can be both predictive and descriptive: when predictive, the aim is to predict the value of a particular attribute given existing data, when descriptive, the aim is to derive patterns that summarize underlying relationships in the data. Data mining is thus an integral part of knowledge discovery, which is the overall process of converting raw data into knowledge by obtaining selecting useful information from the data. Five core data mining tasks have been identified [10,12]: 1) *predictive modelling*, 2) a*ttribute selection, 3) association analysis*, 4) *cluster analysis*, 5) *anomaly detection*. In our approach, the most appropriate data mining task is *predictive modelling*. The task is to build a predictive model for a target variable, based on explanatory variables. Classification and regression are ways of predicting a discrete or continuous outcome. Regression analysis is a statistical tool for the investigation of relationships between variables. Usually, the investigator is looking for the causal effect of one variable on another.

First, we checked for linear relationships between variables using Pearson's correlation and variable clustering. The result of a cluster analysis is a binary tree, or dendrogram, with *n-1* nodes. The branches of the tree are cut at a level of similarities obtained -in our case using the correlation between all the variables. Second, for predictive modelling, when the outcome or class is numeric and all the attributes are numeric, linear regression is the logical choice. The standard way of dealing with continuous prediction is writing the outcome as a linear sum of attribute values with appropriate weights such that: $y_{pure} = w_0+w_1x_1+ w_2x_2+...+ w_nx_n$ where: y_{pure} is the class, $x_1, x_2, ..., x_n$ are the attribute values of the variable $X_1, X_2, ...$ and X_n, $w_1, w_2, ..., w_n$ are the weights of each variable $X_1, X_2, ...$ and X_n.

In this way, we obtained a regression equation to be used to determine the corresponding weights for each variable, a well-known procedure in statistics. The weights were calculated from the training data, the model minimizes this sum of squares by choosing the appropriate coefficients. Linear regression is an excellent, simple method for numeric prediction that has been widely used in statistical applications but is very sensitive to outliers.

The difference between the observed value of the dependent variable (y_{obs}) and the predicted value ($\hat{y}_{pure}$) is called the residual (e). Each data point has one residual: $e = y_{obs} - \hat{y}_{pure}$

Both the sum and the mean of the residuals are equal to zero. That is, $\Sigma\, e = 0$ and $\boldsymbol{e = 0}$.

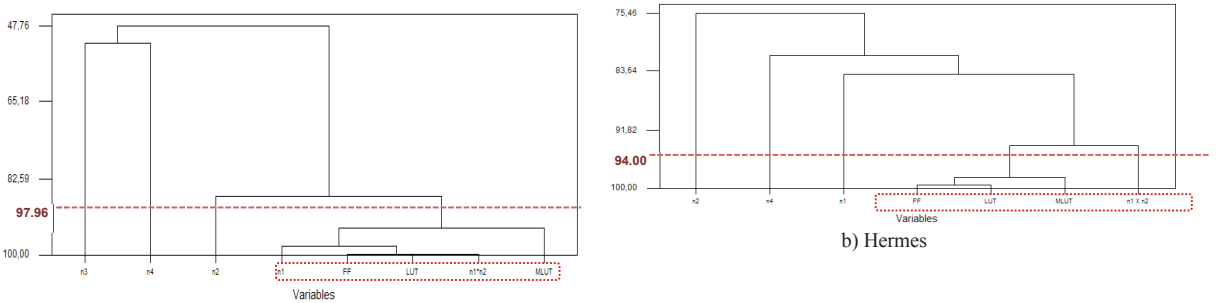
3b. Data analysis

Table 2 lists the respective Pearson's correlations for the AdOcNet (with 29 synthesis) and Hermes (with 152 Synthesis) [11].

Table 2.Pearson's correlation for AdOcNet (left) and for Hermes (right)

	AdOcNet							Hermes					
	n_3	n_4	n_2	n_1	FF	LUT	MLUT	n_4	n_2	n_1	FF	LUT	MLUT
n_4	0.033												
n_2	-0.045	-0.045						0.170					
n_1	-0.071	-0.071	0.551					-0.157	-0.237				
FF	-0.122	-0.124	0.731	0.954				0.364	0.509	0.531			
LUT	-0.093	-0.127	0.721	0.959	0.998			0.460	0.503	0.467	0.992		
MLUT	-0.340	-0.292	0.596	0.789	0.876	0.850		0.627	0.463	0.339	0.932	0.971	
$n_1 \times n_2$	-0.089	-0.089	0.733	0.959	0.997	0.999	0.834	-0.056	0.468	0.680	0.880	0.812	0.649

When Pearson's coefficient is greater than 0.7, the closer the points are located to one another on the line (a perfect correlation is 1, indicating that all points fall directly on a line). Concerning the two NoCs, there is a strong positive correlation between the observed resources. When similarities between groups were analyzed, the strongest correlation was found between FFs and LUTs (respectively 0.992 for Hermes and 0.998 for AdOcNet). Strong correlations were also found between MLUT and LUT, and between FF and MLUT. There is also a strong correlation (lesser but significant) between $n_1 \times n_2$ and the number of FF and LUT. One main difference between both NoCs is the use of resource according to n_3 parameter. AdOcNet only uses MUTs, LUTs and FFs for the NoC structure whereas the Hermes NoC uses BRAM to implement buffer (the number of BRAM does not change for the varying size of buffer). n_3 is respectively considered as a variable for AdOcNet and a constant for Hermes. Therefore $n_3$is not considered in the Person'correlation and hierarchical analysis for Hermes. Next, we identified strongly correlated group of variables by applying hierarchical analysis on the variables [10]. Fig 2 presents the dendograms respectively AdOcNet (Figures 2a.) and Hermes (Figure 2b.).



a) AdOcNet b) Hermes

Fig 2.Hierarchical analysis of similarities between the variables

For AdOcNet, a group contains five variables with 97.96 similarity (n_1, FF, LUT, MLUT, $n_1 \times n_2$). For Hermes, a group contains four variables with 94.00 similarity (FF, LUT, MLUT, $n_1 \times n_2$). In conclusion, there are strong linear

links between the variables (see Table 4). For each NoC, FF, LUT, MLUT are strongly correlated with $n_1 \times n_2$. Our objective was to identify possible linear relationships between these resources and $n_1 \times n_2$. Figure 3 validates the linear relationship between the number of FF and $n_1 \times n_2$. We then checked it on the other resources for both NoCs. The regression equation is: $\boldsymbol{FF = -1371 + 447\ n_1 \times n_2}$

Table 3. Identification of the highly correlated variables for each NoC.

NoC	Highly correlated variables	Similarity Level
AdOcNet	FF LUT $n_1 \times n_2$ n_1 MLUT	97.96
Hermes	FF LUT MLUT $n_1 \times n_2$	94.00

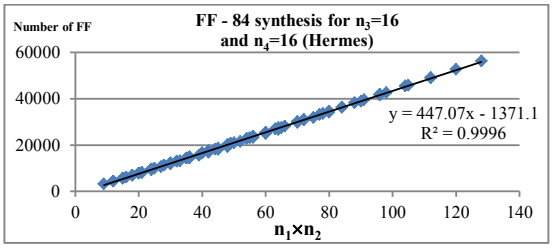


Fig 3. Number of FF regarding $\boldsymbol{n_1 \times n_2}$

Graphical analysis is a very effective way to investigate the adequacy of the fit of a regression model and to check the underlying assumption. The henry line test and histogram of residual values are depicted in Figure 4. The Henry line (left) is a graphical method for adjusting a gaussian distribution with that of a series of observations. The normal scores are not aligned, there are outliers amongst results. The histogram (right), used to check the variances, is not normally distributed around zero (a symmetric bell-shaped histogram evenly distributed around zero indicates that the normality assumption is likely to be true). We observe that the regression model does not completely fit the data. The model's underlying assumption may have been violated. Such results enable us to enter in the modeling stage.

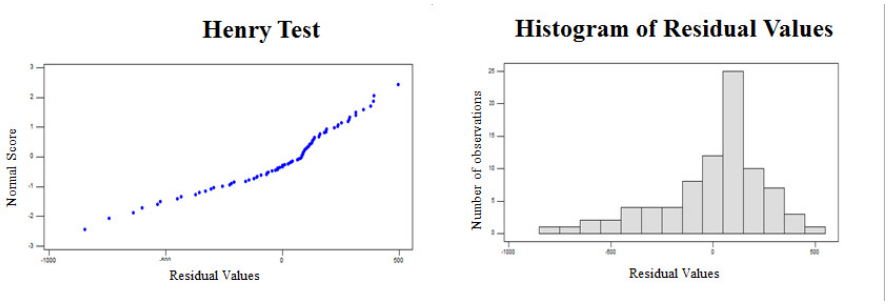


Fig 4. Analysis of residual values.

3c. Modelling

Hypothesis: from only 3 synthesis for 3 categories of NoC (Small, Medium, Large), it is possible to dimension the Hermes or AdOcNet?

Objective: to estimate the resources (LUT, MLUT, FF) according to $\boldsymbol{n_1 \times n_2}$.

Mathematical model: linear regression and the linear relationship are built on a straightforward model using the three points.

Validation: from a new synthesis, we calculated the relative errors.

Figure 5 shows the regression models of LUT usage, for Hermes and AdOcNet. The same approach was used for FF and MLUT and the models are similar to models for LUT. We estimated the resources using each corresponding equation and calculated the relative error. The mathematical model was validated on the same FPGA. A high error rate for FF (Hermes: 20.22%, AdOcNet: 13.24%) was observed for small (2×2) or (3×3) of NoCs, the error rate decreased to less than ± 2.5% for bigger sizes of NoC. This indicates that the analytically estimated results are a little bigger than the results obtained after synthesis (synthesized results) for small sizes of NoC. If the (2×2) or (3×3) router sizes of NoCs are not taken into account, the intervals of relative errors are [-7.90%; 6.90%] for Hermes and [-2.52%; 6.14%] for AdOcNet. Table 4 shows that the mean absolute percentage error is less than 2.3%.

Estimations for small sizes (2×2) or (3×3) of NoCs can be replaced by direct synthesis because the execution time is not prohibitive, in that cases. However, buses or point to point communication can be better suited for small designs.

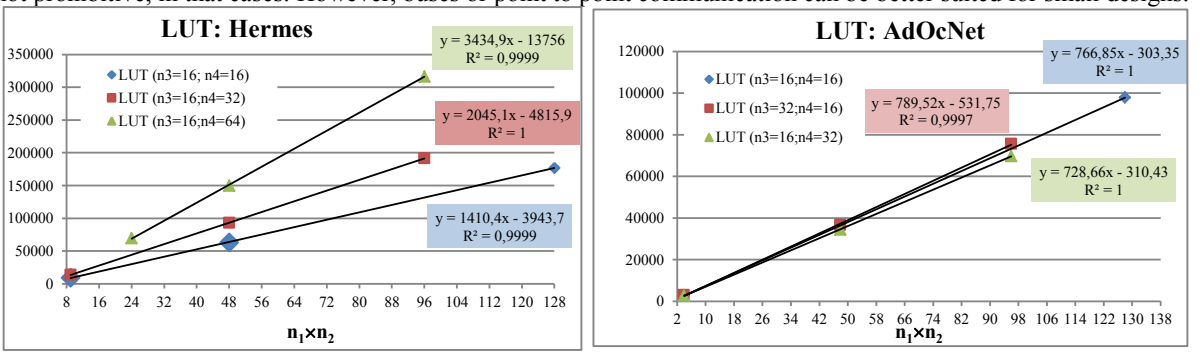


Fig 5. Regression models for LUT for each NoC (x in the equations corresponds to n1×n2).

Table 4. Mean absolute percentage error

	FF	LUT	MLUT
Hermes	1.684%	2.289%	1.832%
AdOcNet	1.999%	0.664%	0.000%

3. Conclusion

In this paper, we showed the feasibility of identifying a mathematical model for NoC dimensioning on FPGA. This model can be extracted from only 3 synthesis steps done using the same FPGA with one computer. Extracting 3 points is enough to provide a model of each FPGA resource (for each couple size of buffer and size of flits) according to the total number of routers. The resources estimated for Hermes are ±9% of the obtained resources. The resources estimated for AdOcNet are ±7% of the obtained resources. The AdOcNet structure is more regular than Hermes as the model is more precise. The model guarantees a reduction in the time needed for design space exploration (DSE) of NoCs. This model was validated by a comprehensive set of experimentations for a NoC using less than 10% of FPGA resources. More explorations concerning MPSoC or dedicated SoC will be explored (and the uses or not of memory blocks in the NoC structure according to the type of IP connected to the NoC).

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