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Resistance switching memories are memristors

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Abstract All 2-terminal non-volatile memory devices based on *resistance switching* are *memristors*, regardless of the device material and physical operating mechanisms. They all exhibit a distinctive "fingerprint" characterized by a *pinched hysteresis loop* confined to the first and the third quadrants of the v–i plane whose contour shape in general changes with both the amplitude and frequency of any periodic "sine-wave-like" input voltage source, or current source. In particular, the pinched hysteresis loop shrinks and tends to a straight line as frequency increases. Though numerous examples of voltage vs. current pinched hysteresis loops have been published in many unrelated fields, such as biology, chemistry, physics, etc., and observed from many unrelated phenomena, such as gas discharge arcs, mercury lamps, power conversion devices, earthquake conductance variations, etc., we restrict our examples in this *tutorial* to solid-state and/or nano devices where copious examples of published pinched hysteresis loops abound. In particular, we sampled arbitrarily, one example from each year between the years 2000 and 2010, to demonstrate that the memristor is a device that does not depend on any particular material, or physical mechanism. For example, we have shown that *spin-transfer magnetic tunnel junctions* are examples of memristors. We have also demonstrated that both *bipolar* and *unipolar* resistance switching devices are memristors.

The goal of this *tutorial* is to introduce some fundamental circuit-theoretic concepts and properties of the memristor that are relevant to the analysis and design of *non-volatile* nano memories where binary bits are stored as resistances manifested by the memristor's continuum of equilibrium states. Simple pedagogical examples will be used to illustrate, clarify, and demystify various misconceptions among the uninitiated.

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1 Pinched hysteresis loops

The *memristor* [1] is a 2-terminal circuit element characterized by a *constitutive relation* between two mathematical variables q and φ representing the time integral of the element's current $i(t)$, and voltage $v(t)$; namely,

$$q(t) \triangleq \int_{-\infty}^{t} i(\tau)\, d\tau \tag{1}$$

$$\varphi(t) \triangleq \int_{-\infty}^{t} v(\tau)\, d\tau \tag{2}$$

It is important to stress that "q" and "φ" are defined mathematically and need not have any physical interpretations. Nevertheless, we call q the *charge* and φ the *flux* of the memristor since (1) and (2) coincide with the formula relating charge to current, and flux to voltage, respectively. We say the memristor is *charge-controlled*, or *flux-controlled,* if its constitutive relation can be expressed by

$$\varphi = \hat{\varphi}(q) \tag{3}$$

or

$$q = \hat{q}(\varphi) \tag{4}$$

respectively, where $\hat{\varphi}(q)$ and $\hat{q}(\varphi)$ are *continuous* and *piecewise-differentiable* functions[1] with *bounded slopes*.

[1] A function is *piecewise-differentiable* if its derivative is uniquely defined everywhere except possibly at isolated points.

Differentiating (3) and (4) with respect to time t, we obtain

$$v = \frac{d\varphi}{dt} = \frac{d\hat{\varphi}(q)}{dq}\frac{dq}{dt} = R(q)i \tag{5}$$

where

$$R(q) \triangleq \frac{d\hat{\varphi}(q)}{dq} \tag{6}$$

is called the *memristance*[2] at q, and has the unit of Ohms (Ω), and

$$i = \frac{dq}{dt} = \frac{d\hat{q}(\varphi)}{d\varphi}\frac{d\varphi}{dt} = G(\varphi)v \tag{7}$$

where

$$G(\varphi) \triangleq \frac{d\hat{q}(\varphi)}{d\varphi} \tag{8}$$

is called the *memductance* at φ, and has the unit of Siemens (S). Observe that (5) and (6) can be interpreted as *Ohm's law* except that the resistance $R(q)$ at any time $t = t_0$ depends on the entire *past* history of $i(t)$ from $t = -\infty$ to $t = t_0$. Similarly the memductance $G(\varphi)$ in (8) depends on the entire *past* history of $v(t)$ from $t = -\infty$ to $t = t_0$. It follows from (5) that the charge-controlled memristor defined in (3) is equivalent to the charge-dependent Ohm's law

$$v = R(q)i \tag{9}$$

where $R(q)$ is just the *slope* of the curve $\varphi = \hat{\varphi}(q)$ at q. To show that (3) and (5) are equivalent representations, we can recover (3) by integrating both sides of (5) with respect to t:

$$\begin{aligned}\varphi \triangleq \int_{-\infty}^{t} v(\tau)\,d\tau &= \int_{-\infty}^{t} R\big(q(\tau)\big)i(\tau)\,d\tau \\ &= \int_{-\infty}^{t} R\big(q(\tau)\big)\frac{dq(\tau)}{d\tau}\,d\tau \\ &= \int_{q(-\infty)}^{q(t)} R\big(q(\tau)\big)\,dq(\tau) \\ &= \int_{q(-\infty)}^{q(t)} R(q)\,dq \\ &= \hat{\varphi}(q)\end{aligned} \tag{10}$$

It follows from (10) that

$$\hat{\varphi}(q) = \int R(q)\,dq \tag{11}$$

[2] Just as *memristor* is an acronym for *memory resistor*, *memristance* is an acronym for *memory resistance*. Similarly *memductance* is an acronym for *memory conductance*.

Similarly, a flux-controlled memristor is equivalent to the flux-dependent Ohm's law

$$i = G(\varphi)v \tag{12}$$

where

$$\hat{q}(\varphi) = \int_{\varphi(-\infty)}^{\varphi(t)} G(\varphi)\,d\varphi \tag{13}$$

Example 1 Consider the charge-controlled memristor shown in Fig. 1(a) along with the memristor symbol in the upper left corner. The memristor constitutive relation, shown in red, is described analytically by a cubic polynomial

$$\varphi = q + \frac{1}{3}q^3 \tag{14}$$

Let us apply a sinusoidal current source (blue sine wave in Fig. 1(c)) defined by

$$\begin{cases} i(t) = A\sin\omega t, & t \geq 0 \\ \quad\;\; = 0, & t < 0 \end{cases} \tag{15}$$

across this memristor, as shown in Fig. 1(c) for $A = 1$ and $\omega = 1$. To determine the corresponding voltage response $v(t)$ from the constitutive relation (14), we must calculate first the corresponding charge (shown in red in Fig. 1(c)). Assuming the initial charge $q_0 = q(0) = 0$, we obtain upon integrating (15) the following equation for $q(t)$:

$$q(t) = \int_0^t A\sin(\omega\tau)d\tau = \frac{A}{\omega}[1 - \cos\omega t], \quad t \geq 0 \tag{16}$$

Substituting (16) into (14), we obtain the corresponding flux (shown in magenta in Fig. 1(d))

$$\varphi(t) = \frac{A}{\omega}(1 - \cos\omega t)\left[1 + \frac{1}{3}\left(\frac{A^2}{\omega^2}\right)(1 - \cos\omega t)^2\right] \tag{17}$$

Differentiating (17) with respect to t, we obtain

$$v(t) = A\left[1 + \frac{A^2}{\omega^2}(1 - \cos\omega t)^2\right]\sin\omega t \tag{18}$$

Plotting the loci[3] of $(i(t), v(t))$ in the v–i plane, via (15) and (18), we obtain the *pinched hysteresis loop* shown in Fig. 1(b) for $A = 1$ and $\omega = 1$. The hysteresis occurs because the maxima and minima of the sinusoidal input current $i(t)$ in Fig. 1(c) do not occur at the same time as the corresponding memristor voltage $v(t)$ in Fig. 1(d). The *pinching* at the origin in Fig. 1(b) occurs because both $i(t)$ and $v(t)$ become zero *at the same time.* To show that the hysteresis

[3] Also known as a Lissajous figure.

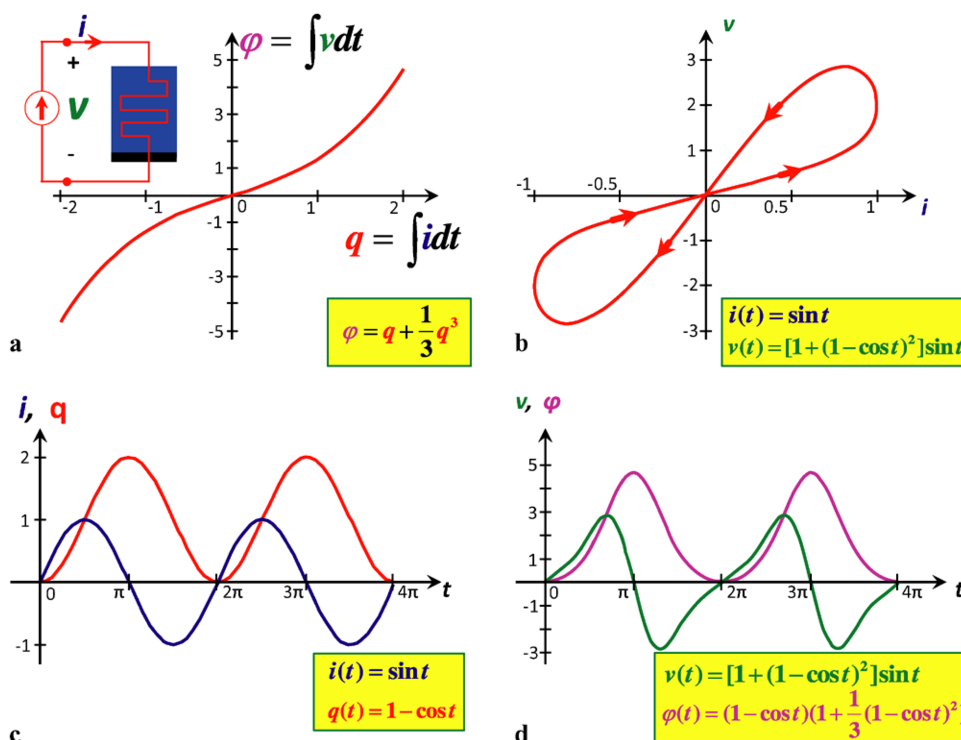


Fig. 1 Memristor symbol, constitutive relation, and pinched hysteresis loop associated with $(v(t), i(t))$ plotted for $A = 1$ and $\omega = 1$. (**a**) Memristor symbol and $\varphi = \hat{\varphi}(q)$ characteristic curve. (**b**) Pinched hysteresis loop: double-valued Lissajous figure of $(v(t), i(t))$ for all times t except when it passes through the origin, where the loop is pinched. (**c**) Periodic waveforms associated with $i(t)$ and $q(t) = \int_0^t i(\tau)\,d\tau$ plotted with $A = 1$ and $\omega = 1$. (**d**) Periodic waveforms associated with $v(t)$ and $\varphi(t) = \int_0^t v(\tau)\,d\tau$

loop is always pinched at the origin $(v, i) = (0, 0)$, let us calculate the *memristance* $R(q)$ from (6) and (14):

$$R(q) = \frac{d\hat{\varphi}(q)}{dq} = 1 + q^2 \tag{19}$$

Substituting $q(t)$ from (16) into (19), we obtain

$$R\big(q(t)\big) = 1 + \left[\frac{A}{\omega}(1 - \cos\omega t)\right]^2, \quad t \geq 0 \tag{20}$$

Observe from (19) and Fig. 2(c) that

$$R(q) > 0 \tag{21}$$

Substituting (20) and (15) in (9), we obtain the same expression for the memristor voltage $v(t)$ derived earlier in (18).

Now since $R(q)$ is *finite* for all finite q, it follows that

$$v(t) = 0 \quad \text{whenever } i(t) = 0 \tag{22}$$

for *any* input current $i(t)$. Similarly, for any φ-controlled memristor whose memductance $G(\varphi)$ is finite for all finite φ, we have

$$i(t) = 0 \quad \text{whenever } v(t) = 0 \tag{23}$$

for *any* input voltage $v(t)$.

The waveform of $R(t)$ given by (20) is shown in Fig. 2(d) for $A = 1$ and $\omega = 1$. The loci traced out by $(R(t), i(t))$ is shown in Fig. 2(b). Again we obtain a hysteresis loop, but it is *not* pinched since $R(t) > 0$ for all times.

It is important to observe from Fig. 1(d) and Fig. 2(d) that while $v(t)$ and $i(t)$ assume both positive and negative values, both $\varphi(t)$ and $q(t)$ are *non-negative*. It follows that only the memristor φ–q curve in the first quadrant is visited during every period of $i(t)$. Observe also that the pinched hysteresis loop in Fig. 1(b) is *odd symmetric* with respect to the origin.

Finally, observe that except for the *memristor constitutive relation* $\varphi = \hat{\varphi}(q)$ in Fig. 1(a), and its associated *memristance* $R(q)$ in Fig. 2(c), which remain unchanged, all other waveforms of Figs. 1 and 2 will change when we vary the amplitude A or the frequency ω of the input signal $i(t) = A\sin\omega t$. In particular, note from (16) and (17) that $q(t) \to 0$ and $\varphi(t) \to 0$ as $\omega \to \infty$. This makes perfect sense since as we increase the frequency ω of the sinusoidal input current $i(t) = A\sin\omega t$, while keeping the amplitude constant, the "area" accumulated from $t = 0$ to the first half period $t = \frac{\pi}{\omega}$ diminishes with ω. It follows therefore that the memristance

$$R(q(t)) \to R(0) = 1\ \Omega, \quad \text{as } \omega \to \infty \tag{24}$$

We can confirm this prediction via (18) by noting that

$$v(t) \to A\sin\omega t, \quad \text{as } \omega \to \infty \tag{25}$$

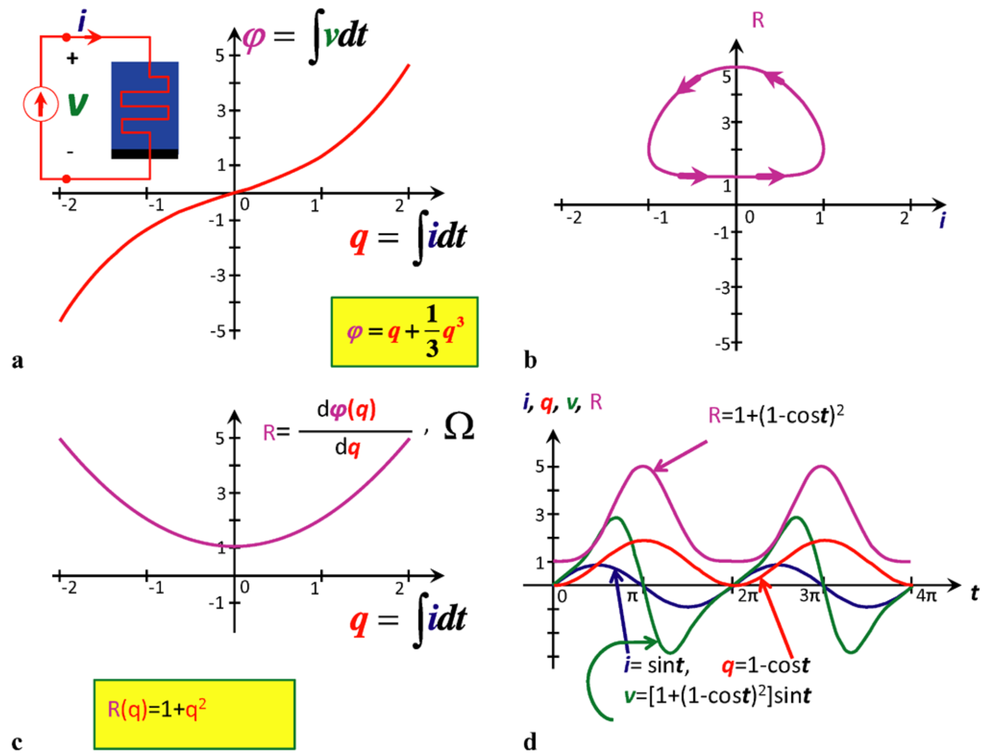


Fig. 2 (**a**) Memristor constitutive relation. (**b**) Resistance hysteresis loop associated with $(R(t), i(t))$. (**c**) Memristance plotted as a function of q. (**d**) Periodic waveforms of $i(t)$, $q(t)$, $v(t)$, and $R(t)$, plotted for $A = 1$, $\omega = 1$

In fact, this is one of the signature properties of a memristor, which we formalize as follows:

Memristor pinched hysteresis loop fingerprint

The loci (Lissajous figure) in the v–i plane of any *passive memristor* with positive memristance

$$R(q) = \frac{d\hat{\varphi}(q)}{dq} > 0 \tag{26}$$

and driven by a sinusoidal current source $i(t) = A \sin \omega t$ is always a *pinched hysteresis loop,* whose area shrinks with frequency and tends to a linear resistance equal to $R(0) =$ slope of the constitutive relation $\varphi = \hat{\varphi}(q)$ at $q = 0$.

We remark here that there exist degenerate cases where the v–i Lissajous figure is a single-valued function, such as the example shown in Fig. 3 when we drive the same memristor from Fig. 1 with the special input $i(t) = \cos t$ for $t \geq 0$. In fact, we can interpret the loci shown in Fig. 3(b) as a degenerate case where the hysteresis loop collapsed into a single-valued function, passing through the origin. Hence, the loci is still *pinched*, even in this degenerate scenario.

Another degenerate scenario can occur when the slope $R(q) = 0$ at some points on $\varphi = \hat{\varphi}(q)$ function, as illustrated in Fig. 4 for the constitutive relation

$$\varphi = \frac{1}{3}q^3 \tag{27}$$

In this case $R(0) = 0$. For the same input current source $i(t) = \cos t$ as in Fig. 3, we obtain a single-valued function in the v–i plane which touches the i-axis, as shown in Fig. 4(b). This represents another degenerate situation where the v–i Lissajous figure actually includes points on the i-axis, as it is impossible to cross the i-axis for any passive memristor where $R(q) \geq 0$.[4] In such situations, the v–i Lissajous figure must still pass through the origin (i.e., it is pinched), but it makes contact with the i-axis as well. In either case, the Lissajous figure ($R(q) \geq 0$) of a *passive* memristor must be confined to the *first* and the *third quadrants*, including possibly the i-axis, of the v–i plane [3].

2 Continuum of non-volatile memories

A cursory examination of the charge-controlled memristor constitutive relation $\varphi = \hat{\varphi}(q)$ in Fig. 2(a) shows that its memristance $M(q)$ varies from[5] $R(q_1) = 1\ \Omega$ to ∞, as depicted in the "Resistance vs. charge" curve in Fig. 2(c), henceforth called the *Resistance vs. State map*. In Fig. 2(c), *charge* is the *state variable*.

[4] Note the preceding memristor fingerprint property is stated for the case $R(q) > 0$.

[5] To avoid clutter, we will often write Memristance $M(q)$ and Resistance $R(q)$ interchangeably. Likewise, we will often write Conductance $G(\varphi)$ for Memductance $W(\varphi)$. Similarly, we use the terms memristance and resistance, as well as memductance and conductance, to mean the same thing.

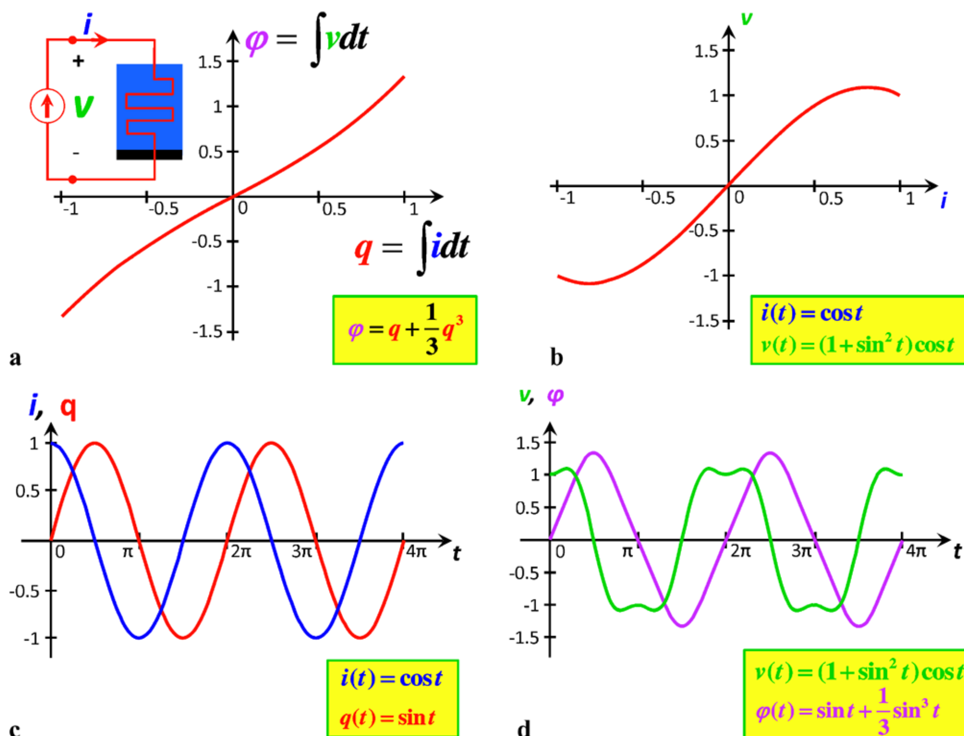


Fig. 3 Illustration of a *degenerate* scenario where the pinched hysteresis loop collapsed into a single-valued function when driven in this case with $i(t) = \cos t$, with the same $\varphi = \hat{\varphi}(q)$ constitutive relation as Fig. 1(a)

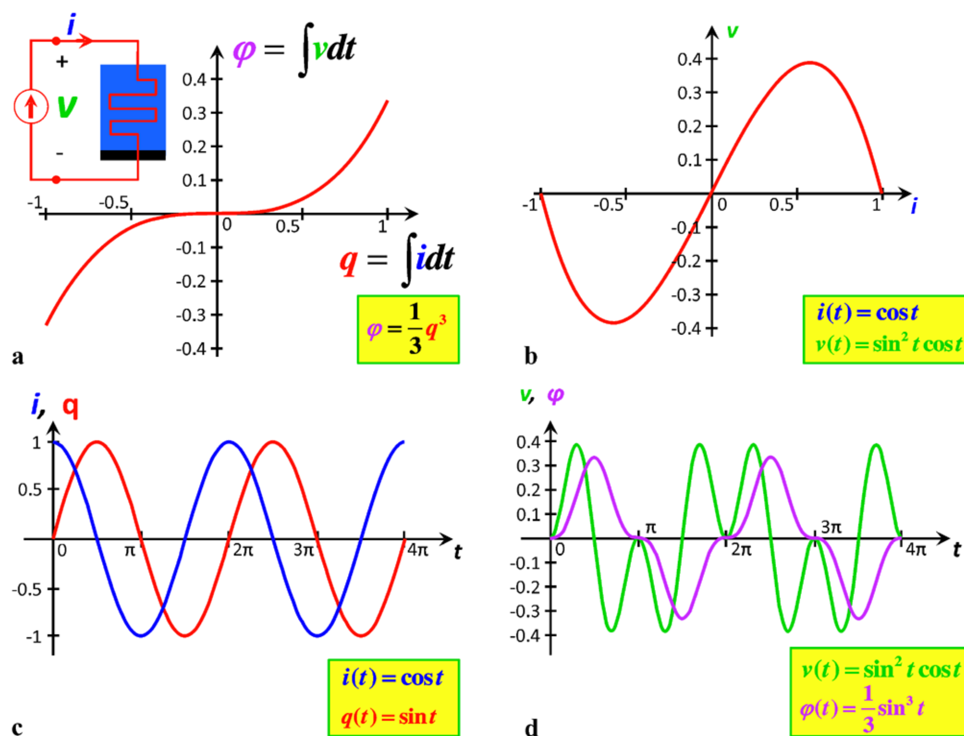


Fig. 4 Example illustrating the second degenerate scenario where the Lissajous figure in the v–i plane actually reaches the i-axis. This limiting case can occur when the memristor constitutive relation has $R(q) = 0$ at some q, as in Fig. 4(a) where $R(q) = 0$ at $q = 0$ [3]

The *Resistance vs. State map* is a very useful graph because it shows how to navigate from one memristance R_0 at state $q = q_0$ on the memristor φ vs. q curve to another memristance R_1 at state $q = q_1$ by simply applying a short current pulse $\Delta i(t)$ whose area is equal to the increment Δq needed to be added to the latest value of $q(t_0) = q_0$ in order to move from R_0 to R_1. The memristance vs. state map in Fig. 2(c) therefore allows one to tune the memristor's resistance continuously from $R = 1\ \Omega$ to $R = \infty$.

It is important to observe that if one opens or short circuits a memristor having a resistance R_0 at $t = t_0$ so that the memristor is *in equilibrium*, i.e., $v = 0$, and $i = 0$, at $t = t_0$, the memristor does not lose the value of φ and q when both voltage v and current i become zero at the instant when the power is switched off, but rather holds the value unchanged at q_0 and φ_0, forever! Hence the passive memristor exhibits *non-volatile* memory.

3 φ–q curve and memristance vs. state maps are equivalent memristor representations

Both the φ vs. q *constitutive relation* (such as Fig. 2(a)) and its associated *resistance vs. state map* (such as Fig. 2(c)) with the state equation $dq/dt = i$ are equivalent representations of a memristor in the sense that given any applied current source input signal $i(t)$ for all times from $t = -\infty$, or equivalently, for positive times from $t = 0$, plus the initial charge $q(0)$ which represents the time integral of $i(t)$ from $t = -\infty$ to $t = 0$, one can calculate the corresponding voltage $v(t)$. Conversely, given any $v(t)$, one can calculate the corresponding $i(t)$, assuming $R > 0$ so that the inverse constitutive relation $q = \hat{q}(\varphi)$ is a continuous function.

In contrast, all of the waveforms and hysteresis loops depicted in Figs. 1 and 2 are only *manifestations* of a *memristor*, and cannot be used to predict the voltage response given any other excitation waveforms different from the waveform $i = A\sin\omega t$, with $A = 1$ and $\omega = 1$, in Fig. 1(c). The reader should verify that changing the parameter A, or ω, or changing the waveforms of $i(t)$ would result in completely different responses. For example, it follows from (16), (18) and (19) that if we hold the amplitude $A = 1$ while increasing the frequency $\omega \to \infty$, we would find that $q(t)$ tends to zero, $v(t)$ tends to $\sin t$, and $R(t)$ tends to 1 Ω, as the hysteresis loop in Fig. 1(b) shrinks until it collapses into a unit-slope straight line through the origin. Indeed, as ω tends to ∞, the charge $q(t)$, and flux $\varphi(t)$ would both tend to the origin in Fig. 1(a), and remain motionless thereafter. Under this limiting situation, the memristor degenerates into a linear R Ω resistor where R is just the slope of the φ–q curve at the origin in Fig. 1(a); namely, $R = 1$.

Memristor lesson 1

Pinched hysteresis loops are not models!

While a *pinched* v–i hysteresis loop measured from an experimental 2-terminal device implies that the device is a memristor, the pinched loop itself is useless as a model since it cannot be used to predict the voltage response to arbitrarily applied current signals, and vice versa. The only way to predict the response of the device is to derive either the φ–q *constitutive relation*, or the *memristance vs. state map*.

4 Resistance vs. state map and state equation

When we write, or utter, the term *resistance*, or *conductance*,[6] we must always subconsciously remind ourselves that we are referring to a 2-terminal electrical device that obeys a *linear equation* called *Ohm's law*; namely,

$$\text{Ohm's law:} \quad v = Ri \tag{28}$$

where R is a constant, called the resistance of the resistor, where R has the unit of Ω. It is conceptually important to distinguish between the two words *resistance* and *resistor*: resistor is a device, while resistance is the slope of the straight line defined by Ohm's law. No harm is done when the device is linear-hence the sloppiness in current usage. However, for nonlinear devices, it is crucial to distinguish them!

The *resistance vs. state map* of a memristor also obeys Ohm's Law, except that the resistance R is not a constant, as illustrated by the example in Fig. 2(c), but depends on a dynamical state variable x ($x = q$ in the *ideal* memristor case considered so far) which evolves according to a prescribed ordinary differential equation, called the state equation. An ideal memristor is therefore defined by:[7]

State-dependent Ohm's law:

$$v = R(x)i \tag{29a}$$

Memristor state equation:

$$\frac{dx}{dt} = i \tag{29b}$$

Memristor lesson 2

A *memristor* is defined by a *state-dependent Ohm's law*.

5 Correspondence between *small-signal memristance* and *chord memristance*

Let us apply a sinusoidal current source $i(t) = A\sin\omega t$ across a charge-controlled memristor as in Fig. 1. The memristance $R(q(t_k))$ at $t = t_k$ as calculated from (6) is equal to the *slope* of the φ–q curve at $q = q(t_k)$. The slope at $q(t_k)$ will in general vary with the time-evolution of $\varphi(t)$.

[6] To avoid clutter, we usually write only the term resistance, or conductance, with the understanding, *mutatis mutandis,* that the same follows for the dual case.

[7] We henceforth adopt the standard notation x to denote a *state variable* in *mathematical system theory*, where x may be a vector $\mathbf{x} = (x_1, x_2, \ldots, x_n)$. This will be the case for many *non-ideal* memristors found in practice.

However, we can keep the slope at $q(t_k)$ approximately constant over time by choosing a sufficiently small amplitude A while fixing the frequency ω, assuming the φ–q curve is continuous at $q = q(t_k)$. Under this small-signal condition, the memristance, henceforth called the *small-signal memristance*, would be indistinguishable from that of a linear resistance, which obeys Ohm's Law with a constant resistance equal to $R(t_k)$ at all times. It follows that by applying a short current pulse signal of appropriate height, we can tune the memristance over a continuous range of values without introducing a third terminal, and without applying a continuous supply of power via a biasing circuit. For the example shown in Fig. 2(c), any small-signal memristance greater than 1 Ω can be easily programmed. In particular, observe that we have aligned the vertical axis of Figs. 2(a) and 2(c) so that the value of R (height of the resistance vs. state map) is equal to the slope of the φ–q curve in Fig. 2(a) at the point $(q(t_k), \varphi(t_k))$, i.e., both points must fall on the vertical projection line through $q = q(t_k)$.

In other words, the memristor can be designed to function as a *non-volatile* and continuously tunable resistance. Let us consider next the large-signal case where $A \gg 0$, e.g. $A = 1$ and $\omega = 1$, as shown in Fig. 2. In this case, a quick calculation using (17) shows that the flux φ(t) oscillates between $\varphi = 0$ and $\varphi = 14/3$, as shown in Fig. 1(d). The corresponding memristance calculated from (20) ranges from $R = 1$ to $R = 5$ Ω, as shown in Fig. 2(d). The corresponding v–i Lissajous figure is the pinched hysteresis loop shown in Fig. 1(b). At any time $t = t_k$, the memristance is equal to $R(t_k) = \frac{v(t_k)}{i(t_k)}$. This number can be interpreted simply as the slope of a straight line, i.e., a *chord*, connecting the origin to the point $(i(t_k), v(t_k))$ in the i–v plane. We will henceforth call this large-signal resistance at time $t = t_k$ the "chord memristance" at $t = t_k$.[8]

Observe that the chord memristance at $t = t_k$ is simply the memristance calculated from the pinched hysteresis loop in Fig. 1(b) at the point where $t = t_k$. This number is equal to the slope of a corresponding point on the φ–q curve in Fig. 1(a), traversed at the same time $t = t_k$; namely, the *small-signal memristance* calculated at the same point. In fact, had we plotted Fig. 1(a) and Fig. 1(b) on the same scale, the *chord* connecting the point $(i(t_k), v(t_k))$ to the origin at $t = t_k$ will be parallel to a corresponding line drawn tangent to the φ–q curve in Fig. 1(a).

For example, at $t = \frac{\pi}{2}$, $(i(\frac{\pi}{2}), v(\frac{\pi}{2})) = (1, 2)$, and the chord resistance is given by $R(\frac{\pi}{2}) = 2/1 = 2$ Ω, and the corresponding small-signal memristance is given by (19) for $q(\frac{\pi}{2}) = 1$, namely, $R(\frac{\pi}{2}) = 1 + 1 = 2$, as predicted and shown in Fig. 2(c). Let us summarize the above results as follow.

[8]The terminology "chord resistance" had been widely used by neurobiologists, including Hodgkin and Huxley [5], for similar geometrical interpretations.

Small-signal and chord memristance correspondence property

The large-signal *chord memristance* calculated at any point $(i(t_k), v(t_k))$ at time $t = t_k$ of a pinched hysteresis loop in the v–i plane is equal to the small-signal memristance at a corresponding point on the φ–q curve traversed at the same time. In particular, the slope of the chord connecting $(0, 0)$ to $(i(t_k), v(t_k))$ is equal to the slope of the line drawn tangent to the φ–q curve at the corresponding point $(q(t_k), \varphi(t_k))$.

Recall that the small-signal memristance $R(q(t))$ remains constant under any sufficiently small odd-symmetric periodic current input signals, such as $i(t) = A \sin \omega t$ where $i(-t) = -i(t)$ because every value of the state variable x (charge in Fig. 1) is a *stable equilibrium point* [9] and because the memristor is *locally passive* when $R(q) \geq 0$ [3]. The *local passivity property* is essential for small-signal memristor circuit analysis to make sense because a *locally active* memristor [3] could give rise to oscillations, and even chaos [6].

In contrast to the small-signal memristance, which does not depend on the input waveform of $i(t)$ other than it being sufficiently small, the chord memristance is always associated with a particular Lissajous figure, such as a pinched hysteresis loop corresponding to a periodic input signal. However, once the input current waveform is given, we can derive the associated pinched hysteresis loop, such as that shown in Fig. 1(b) when $i = A \sin \omega t$ with $A = 1$ and $\omega = 1$. In this case, we can interpret the two limiting chord memristances associated with the two hysteretic branches through the origin. In particular, the chord memristance of the lower limiting branch is equal in value to the small-signal memristance at the origin of the φ–q curve in Fig. 2(a), namely, $R(0) = 1$. This also follows upon substitution of $q = 0$ in (19) at time $t = 0$. The second chord memristance associated with the limiting upper branch through the origin in Fig. 2(b) is associated with the small-signal memristance at the point $q = q(\pi) = 2$, namely, $R(2) = 5$.

For the pinched hysteresis loop shown in Fig. 1(b), the chord memristance will sweep from the lower limit $R(0) = 1$ to the upper limit $R(2) = 5$ in a counterclockwise direction in the first quadrant during the first half cycle, and then reversing the sweep in a symmetrical manner in the

[9]A state $x = x_0$ is said to be an *equilibrium point* of a dynamical circuit if $\frac{dx(t)}{dt} = 0$ at $x = x_0$. It is said to be *locally asymptotically stable* if it always returns to its original position whenever subjected to small perturbations, such as a small current pulse. An equilibrium point is said to be *stable* if any drift from its original position due to any perturbation to the state variable x is confined to a neighborhood of radius of about the same size as that of the perturbation. In other words, it does not diverge to infinity, as would be the case for an unstable equilibrium point. Neither does it return to its original position, as would be the case if the equilibrium point is asymptotically stable [3].

third quadrant during the second half cycle, resulting in an odd-symmetric pinched hysteresis loop. The motion of the chord memristance in the first quadrant of Fig. 1(b) is similar to that of an automobile windshield wiper except that the length of the blade changes continuously in accordance to the square root of the sum of squares of $i(t)$ and $v(t)$, from $t=0$ to $t=\pi$ in the v–i plane.

6 Ideal memristor φ–q curves for binary memories

For digital computer applications requiring only two memory states, the memristor needs to exhibit only two sufficiently distinct equilibrium states R_0 and R_1 where $R_0 \gg R_1$, and such that the high-resistance state R_0 can be easily switched to the low resistance state R_1, and vice versa, as fast as possible while consuming as little energy as possible. In contrast to conventional memories, the memristor does not dissipate any power except during the brief switching time intervals because $v(t)=d\varphi(t)/dt=0$, and $i(t)=dq(t)/dt=0$ at both equilibrium states R_0 and R_1. Our goal in this section is to present two ideal memristors for mimicking two, among many, recently published resistance switching memories.

Memristor switching memory 1

Figure 5 shows a charge-controlled memristor characterized by a 3-segment odd-symmetric φ–q curve (Fig. 5(b)). This piecewise-linear function can be described by the equation

$$\varphi = \mathrm{R}_0 q + \left(\frac{1}{2}(R_1 - R_0)\right)\big[|q+B| - |q-B|\big] \tag{30}$$

where R_1 denotes the slope of the middle segment in Fig. 5(b), R_0 denotes the slope of the outer segments in Fig. 5(b), $q=-B$ denotes the left charge breakpoint in Fig. 5(b), and $q=B$ denotes the right charge breakpoint in Fig. 5(b). The corresponding memristance function $R(q)$ is derived by differentiating (30) with respect to q; namely,

$$R(q) = \mathrm{R}_0 + \frac{1}{2}(R_1 - \mathrm{R}_0)\big[\mathrm{sgn}(q+B) - \mathrm{sgn}(q-B)\big] \tag{31}$$

where sgn(.) is defined by

$$\begin{aligned} \mathrm{sgn}\, x &= 1, \quad \text{if } x>0 \\ &= -1, \quad \text{if } x<0 \end{aligned} \tag{32}$$

A graph of *the memristance vs. state map* is shown in Fig. 5(d) for the parameter values $R_0 = 6000\ \Omega$ and $R_1 = 2500\ \Omega$.

Applying the sinusoidal current source defined in (16) with $A = 2B\omega$ across the memristor, the corresponding memristor charge is given by

$$\begin{aligned} q(t) &= 2B(1-\cos\omega t), \quad t>0 \\ &= 0, \quad t<0 \end{aligned} \tag{33}$$

In this case, the memristor φ–q curve in Fig. 5(b) traverses from $q=0$ at $t=0$ to $q=4B$ at $t=\frac{\pi}{\omega}$. Observe that starting from $q(0)=0$ in Fig. 5(b) at $t=0$, the memristor charge $q(t)$ increases along the lower branch while maintaining a constant memristance value of R_1 until it reaches the right breakpoint at $q=B$ where it switches abruptly to the upper branch and continues to increase, with the constant high memristance value of R_0, until it reaches the maximum value of $q(t)=4B$ at $t=\frac{\pi}{\omega}$ corresponding to the end of the first half cycle of the sinusoidal current input $i(t)$. The corresponding chord memristance also remains constant at R_1 before the breakpoint $q=B$, and at R_0 after the breakpoint. During the next half cycle, the memristor input current $i(t)$ changes sign, and so does the corresponding memristor voltage $v(t)$. The loci in Fig. 5(b) then retraces the same route from $q=4B$ with a constant memristance R_0 at $t=\frac{\pi}{\omega}$ until it reaches the right breakpoint $q=B$ again, where the memristance switches to R_1, and continues to decrease until it returns to the initial departure point $q=0$ at $t=2\frac{\pi}{\omega}$. Since both $i(t)$ and $v(t)$ are negative during the return trip, the plot of the corresponding Lissajous figure in the v–i plane is an odd-symmetric pinched hysteresis loop, as shown in Fig. 5(c). Observe that it consists of only two chord memristances equal to R_1 for the lower branch, and R_0 for the upper branch. Observe also that the switching occurs instantaneously, in both directions, in this case in view of the discontinuity in slope of the φ–q curve at the two breakpoints $q=B$ and $q=-B$.

The corresponding memristance vs. state map shown in Fig. 5(d) for $R_1 = 2500\ \Omega$, and $R_0 = 6000\ \Omega$, also shows a discontinuous jump at the same breakpoints, as expected. If we transcribe the corresponding loci of the memristance $R(t)$ from the pinched hysteresis loop in Fig. 5(c) into the R vs. i plane, we would obtain the square resistance hysteresis loop shown in Fig. 5(e). This plot is the piecewise-linear analog of the smooth differentiable φ–q curve in Fig. 2(b).

A cursory glance at the figures from Ref. [7] reveals similarities in the respective rectangular resistance hysteresis loops. From a circuit-theoretic perspective, the non-volatile resistance switching memory device reported in [7] bears the fingerprint of a memristor, and should be modeled as a memristor. This example suggests that spin-transfer magnetic tunnel junctions are memristors. Indeed, unless a memristive device is properly identified and modeled as a memristor, no deep physical understanding of the rectangular *resistance hysteresis* mechanisms, let alone the development of a reliable commercial product, would be possible.

So far we have chosen charge-controlled memristors for illustrations. Let us now consider the dual case of a flux-

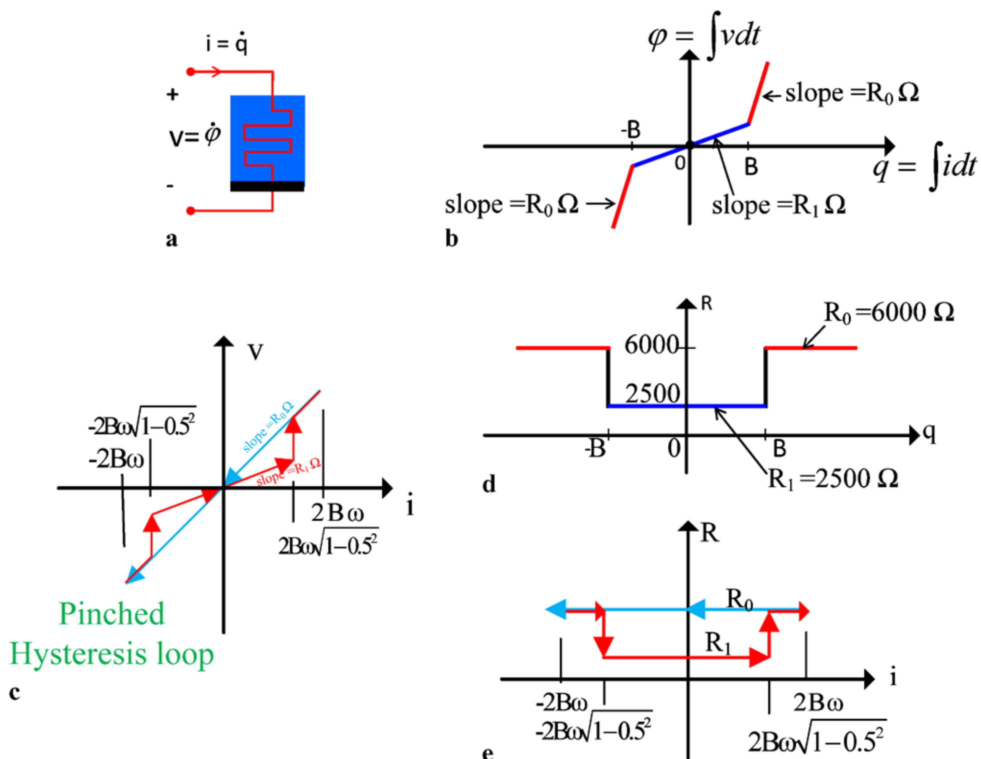


Fig. 5 A two-state pinched hysteresis loop resulting from driving a piecewise-linear charge-controlled memristor with a sinusoidal current source $i(t) = A\sin\omega t$, where $A > \omega B$, and B denotes the numerical value of the breakpoint in (**b**). Notice the *horizontal axis* is "q" in (**b**) and "i" in (**e**), which corresponds to the *vertical axis* in Fig. 6(f) and 6(c), respectively. Consequently, the slope of the piecewise-linear segments in (**b**) represents *memristance* in Ω. (**d**) Shows the relationship between the memristance as a function of q, assuming the slopes are given by $R_0 = 6000\ \Omega$ and $R_1 = 2500\ \Omega$

controlled memristor where the flux φ is the independent variable.[10]

Memristor switching memory 2

Consider the flux-controlled memristor q–φ curve shown in Fig. 6(f) where q (vertical axis) is the charge in nano Coulomb (nC), and φ (horizontal axis) is the flux in Webers (Wb). This odd-symmetric piecewise-linear function can be described exactly by an equation involving two absolute-value functions; namely,

$$q = \frac{1}{2}G_1\{2\varphi + |\varphi - B| - |\varphi + B|\} \tag{34}$$

where $G_1 = 800$ nS, and $B = 2.5$ Wb.[11]

Let us apply a sinusoidal voltage source

$$\begin{aligned} v(t) &= 5\sin t, \quad t > 0 \\ &= 0, \quad\quad\quad t < 0 \end{aligned} \tag{35}$$

shown in Fig. 6(a), across the memristor. Integrating (35) we obtain the flux

$$\begin{aligned} \varphi(t) &= 5(1 - \cos t), \quad t > 0 \\ &= 0, \quad\quad\quad\quad\quad t < 0 \end{aligned} \tag{36}$$

as shown in Fig. 6(b). Substituting (36) into (34), we obtain the corresponding charge

$$\begin{aligned} q(t) = 400\big\{&10(1-\cos t) + \big|5(1-\cos t) - 2.5\big| \\ &- \big|5(1-\cos t) + 2.5\big|\big\} \end{aligned} \tag{37}$$

as shown in Fig. 6(c). Differentiating $q(t)$ from (37), we obtain

$$\begin{aligned} i(t) = 4000 \cdot \sin t \cdot \big\{&1 + \theta\big(5(1-\cos t) - 2.5\big) \\ &- \theta\big(5(1-\cos t) + 2.5\big)\big\} \end{aligned} \tag{38}$$

as shown in Fig. 6(d), where

$$\theta(z) = \begin{cases} 1, & z > 0, \\ 0, & z < 0. \end{cases} \tag{39}$$

Plotting the Lissajous figure of $i(t)$ from Fig. 6(d), or (38), and $v(t)$ from Fig. 6(a), or (35), we obtain the *pinched hysteresis loop* shown in Fig. 6(e). Since the current i is chosen as the vertical axis, and the voltage v is chosen as the horizontal axis, we must now use the dual terminology of *chord memductance*, instead of chord memristance. Observe that the memductance in Fig. 6(e) switches abruptly from

[10] For a strictly-passive memristor, defined by $R(q) > 0$, there is no mathematical difference between a charge-controlled memristor and a flux-controlled memristor except for the choice of the independent variable. However, for a *locally-active* memristor, defined by $R(q) < 0$ at some point on the φ–q curve, the difference becomes important because the φ–q curve in this case is no longer a single-valued function, and therefore does not have an inverse function.

[11] This memristor is not charged-controlled because its memristance is infinite at all points on the horizontal segment where the memductance G_0 is equal to zero.

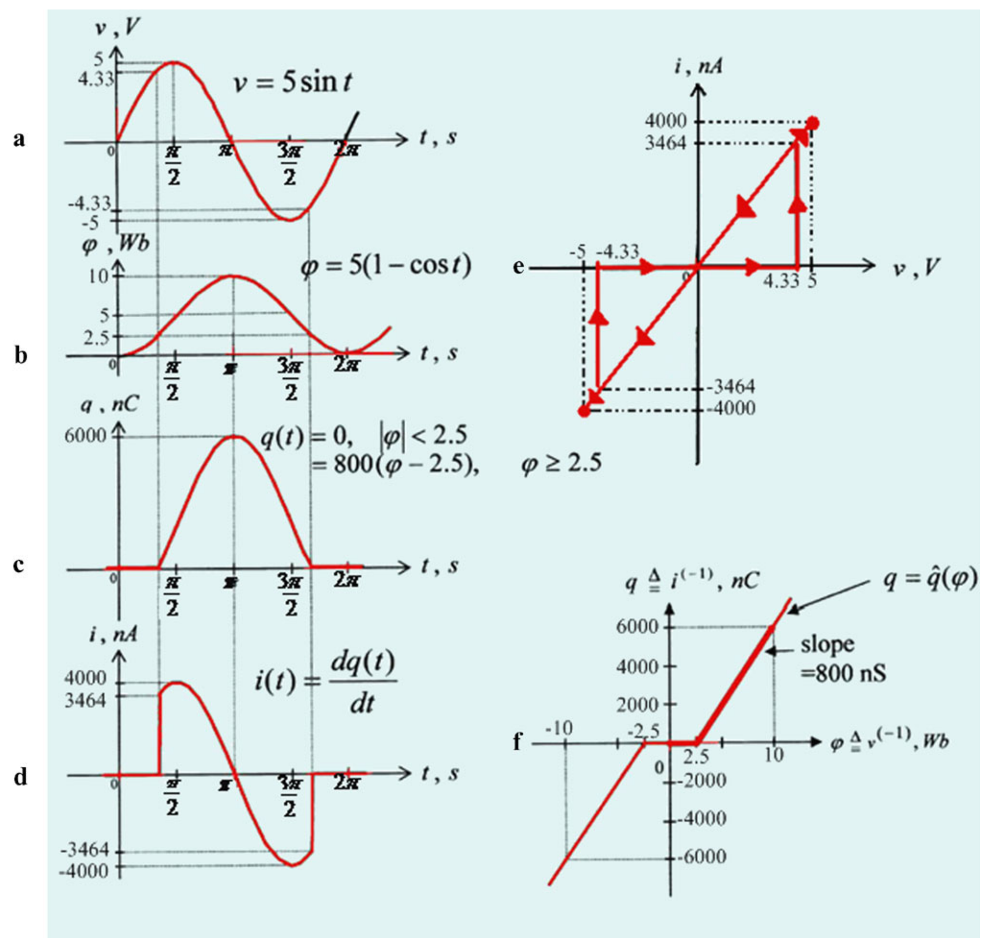


Fig. 6 A two-state *pinched hysteresis loop* resulting from driving a piecewise-linear *flux-controlled* memristor with a sinusoidal voltage source $v = 5\sin(t)$. The horizontal segment has a memductance $G(\varphi) = 0$ nS, and the two parallel outer segments have a memductance of $G(\varphi) = 800$ nS. (Reproduced from Fig. 26 of [4], except for a revision of the original *cartoon sketch* (**e**) which was drawn distorted in order to unfold portions of the pinched hysteresis loop, as well as to exhibit a typical return loci for other periodic input signals)

$G_0 = 0$ (horizontal segment) at the two breakpoint voltages $v = 4.33$ V, and $v = -4.33$ V, to $G_1 = 800$ nS. This switching is instantaneous because the slope of the q–φ curve in Fig. 6(f) changes abruptly at the corresponding breakpoints at $\varphi = 2.5$ Wb, and at $\varphi = -2.5$ Wb, respectively.

Observe that the pinched hysteresis loop in Fig. 6(e) has only two chord memductances. They correspond to the two small-signal memductances $G_0 = 0$ and $G_1 = 800$ nS of the flux-controlled q–φ curve in Fig. 6(f).

Let us now compare the dynamical behaviors of this memristor with the recent non-volatile nano-wire memory device reported by Professor Lieber's group from Harvard [8]. There seems to be little resemblance at first sight. This is because Lieber's group uses a square wave instead of a sinusoidal voltage source in their experiments. We have therefore repeated their experiments by applying the same voltage source, and parameters, across the flux-controlled memristor with the q–φ curve shown in Fig. 6(f), and enlarged in Fig. 7(a). Lieber's bipolar 10-volt square-wave input voltage $v(t)$ is shown in Fig. 7(b). Integrating $v(t)$, we obtain the flux waveform $\varphi(t)$ shown in Fig. 7(c), which is a triangular wave of the same frequency. Observe from Fig. 7(a) that the memductance is equal to zero for $|\varphi(t)| < 2.5$ Wb, and is equal to 800 nS elsewhere. It follows from Fig. 7(c) that the memductance $G(t)$ corresponding to the square wave voltage $v(t)$ in Fig. 7(b) will be a square wave of the same frequency, but delayed by 0.25 seconds. The memductance waveform predicted from the flux-controlled memristor constitutive relation is Fig. 7(a) is virtually identical to the experimental results reported in [8]. Moreover, by massaging the q–φ curve into a smooth function, it is easy to obtain almost the same pinched hysteresis loop in the 1st quadrant as reported in [8]. There is one discrepancy, however, between our memristor prediction, and the experimental pinched hysteresis loop in [8]; namely, the pinched hysteresis loop predicted from the memristor in Fig. 7(a) is odd-symmetric, whereas that reported in [8] is not. In the next section, we will show how to *unfold* our ideal memristor model into a more general form that would allow us to model non-symmetric pinched hysteresis loops as well. Finally, we remark that, although not reported in [8], a private conversation with Prof. Lieber had confirmed that their hysteresis loop will shrink in size as the frequency of the input voltage signal increases, consistent with one of the fingerprints of a memristor.

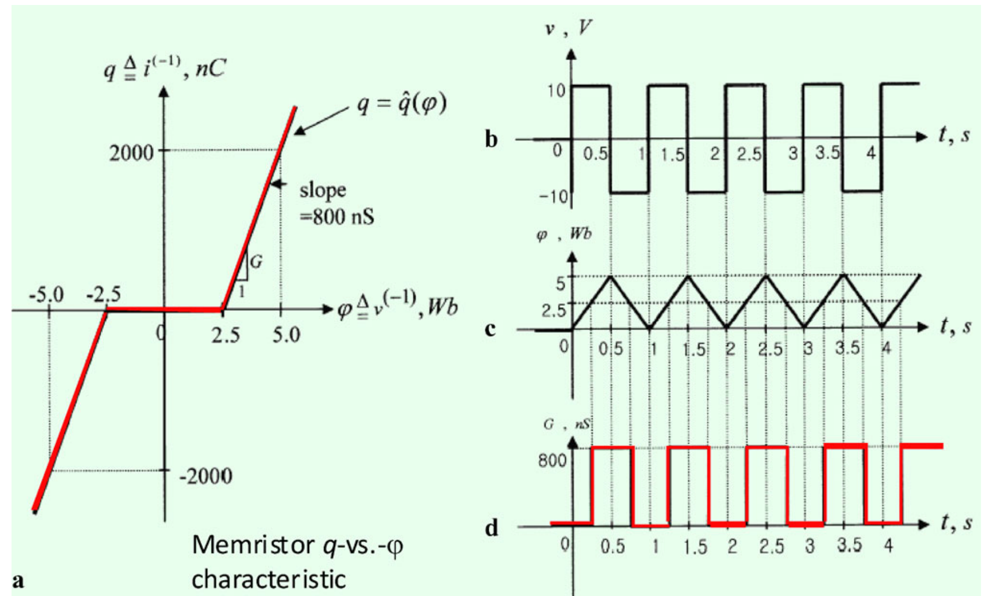


Fig. 7 Voltage and flux waveforms associated with the same memristor from Fig. 6(f), but enlarged in (**a**). The memristor is driven by a ±10-volt square wave in (**b**), whose associated flux is the *triangular* wave shown in (**c**). The conductance waveform is a positive 800 nS square wave of the same frequency but shifted in time by 0.25 s. Observe that the conductance is zero over all times when $\varphi(t)$ in (**c**) falls below 2.5 Wb

7 Unfolding the memristor

In order to develop a more precise quantitative model of non-volatile resistance switching memory devices, such as the nano-wire device cited in the preceding section, let us *unfold* the memristor's state-dependent Ohm's Law, and its associated state equation, defined earlier in (29a)–(29b), by introducing additional nonlinear terms, and parameters, while preserving the key properties of the memristor. Our approach is based on the mathematical theory of *unfoldings* of functions [9].

The foremost characteristic property of the memristor which distinguishes it from the other basic circuit elements defined axiomatically in [4] is its *pinched* hysteresis loop. The adjective "pinched" is chosen to emphasize that the loci, i.e., the Lissajous figure, of any bipolar current (resp., voltage) source waveform $i(t)$ (resp., $v(t)$), including chaotic signals, that is applied across the memristor, and its associated voltage (resp., current) response $v(t)$ (resp., $i(t)$), must pass through the origin $(v, i) = (0, 0)$. This mathematical constraint can be generalized by introducing additional state variables, and the current i, into the state-dependent Ohm Law and its associated state equation, defined in (29a)–(29b) as follows:

State-dependent Ohm's law:

$$v = R(\mathbf{x}, i)i \tag{40a}$$

State equation:

$$d\mathbf{x}/dt = \mathbf{f}(\mathbf{x}, i) \tag{40b}$$

where

$$R(\mathbf{x}, 0) \neq \infty \tag{41}$$

and

$$\mathbf{x} = (x_1, x_2, \ldots, x_n) \tag{42}$$

denotes a vector with n internal *state variables* $(x_1, x_2, \ldots, x_n)$. We stress here that the state variables are internal variables associated with the device material and its physical operating mechanisms, and *must not* be influenced by any external variable, such as a voltage or current applied to a third terminal, or a magnetic field generated from an external source. Observe that (41) is needed to ensure that $v = 0$ whenever $i = 0$. Indeed, if $R(\mathbf{x}, i)$ tends to infinity when $i = 0$, then $v = R(\mathbf{x}, 0)$ (0) $\neq 0$ and the hysteresis loop would not be pinched at the origin.

We will illustrate the mathematical concept of *unfolding* with the following example of memristor (40a)–(40b) where x is a scalar:

$$v = R(x)i \tag{43a}$$

$$\frac{dx}{dt} = a_1 x + a_2 x^2 + \cdots + a_m x^m + b_1 i + b_2 i^2 + \cdots + b_n i^n + \sum_{j,k=1}^{p,r} c_{jk} x^j i^k \tag{43b}$$

By assigning different numerical values to the parameters a_j, b_k, c_{jk}, we can generate a very large family of distinct memristors, all of them originating from the same ancestor, namely, the original memristor defining (29a)–(29b). Just like the unfolding of flower petals, different parameter values gives rise to memristors with a different pinched hysteresis loops. We will henceforth call these parameters the *memristor unfolding parameters*. Let us look at some special choices of these unfolding parameters.

Memristor unfolding example 1

$$a_j = 0, \quad j = 1, 2, \ldots, m$$

$$b_1 = 1, \quad b_k = 0, \quad k = 2, 3, \ldots, n$$

$$c_{jk} = 0, \quad j = 1, 2, \ldots, p, \ k = 1, 2, \ldots, r$$

In this case, (43b) reduces to the original memristor equation (29a)–(29b).

Memristor unfolding example 2

Let us choose the same unfolding parameters as above except b_1 where

$$b_1 = \mu_v \left[\frac{R_{\mathrm{ON}}}{D} \right]$$

In this case, (43b) reduces to (6) from [10] describing the famous HP titanium-dioxide memristor reported in a seminal paper in the May 1 2008 issue of Nature [10].

Memristor unfolding example 3

Let us choose

$$a_j = 0, \quad j = 1, 2, \ldots, m$$

and

$$c_{jk} = 0, \quad j = 1, 2, \ldots, p, \ k = 1, 2, \ldots, r$$

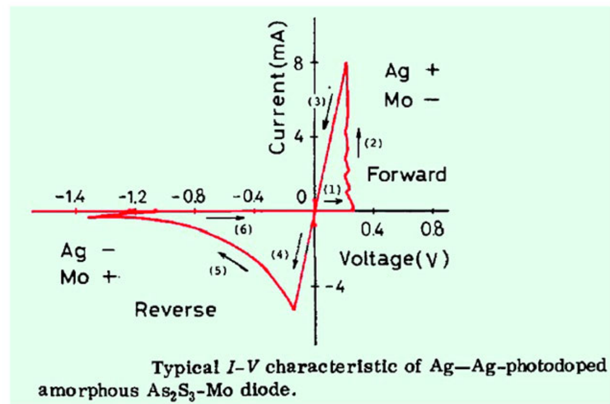
In this case, the memristor unfolding assumes the following form:
State-dependent Ohm's law:

$$v = R(x)i \tag{44a}$$

State equation:

$$dx/dt = m(i) \tag{44b}$$

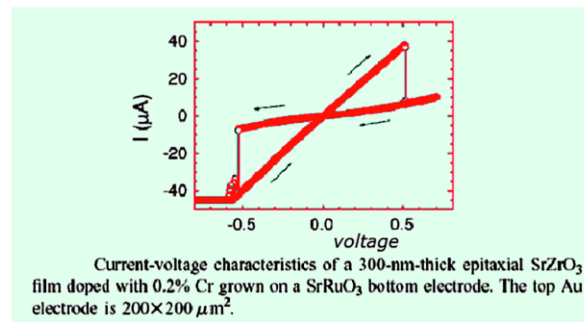
By choosing different values for the unfolding parameters b_k, the resulting nonlinear scalar function $m(i)$ in (44b) can be used to massage the corresponding pinched hysteresis loop into almost any shape which best approximates the experimental data. In particular, the odd-symmetric pinched hysteresis loops shown in Figs. 1(b), 5(c), and 6(e) can be deformed and morphed into other non-symmetrical shapes, such as the one alluded to [8] in the previous section. We will henceforth call the function $m(i)$ in (44b) the "memristor morphing function" since it can be chosen to approximate numerous non symmetrical pinched hysteresis loops measured experimentally from real resistance-switching devices, such as those exhibited in Figs. 8(a)–8(k), which were sampled from the literature on non-volatile resistance switching devices.



An example from year 1976

Yooichi Hirose and Haruo Hirose,
"Polarity-dependent memory switching and behavior of Ag dendrite in Ag-photodoped amorphous As_2S_3 films,"
J. Appl. Phys., Vol. 47, No. 6, p. 2767, 1976

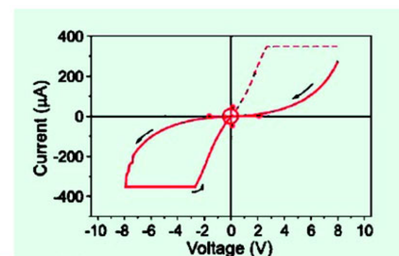
a



An example from year 2000

A. Beck, J. G. Bednorz, Ch. Gerber, C. Rossel, D. Widmer,
"Reproducible switching effect in thin oxide films for memory applications,"
APPLIED PHYSICS LETTERS, Vol. 77, No. 1, p. 140, 2000

b



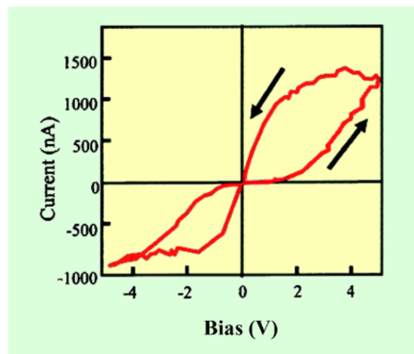
Sequence of EBIC images and the corresponding I–V characteristics for a Pt/$SrZrO_3$(0.2% Cr)/$SrRuO_3$ memory cell, 175 μm in diameter. I electrode thickness is 5 nm. $V_b = 0$ V, $V_{\mathrm{acc}} = 25$ kV.

An example from year 2001

C. Rossel, G. I. Meijer, D. Bre´maud, and D. Widmer,
"Electrical current distribution across a metal–insulator–metal structure during bistable switching,"
J. Appl. Phys., Vol. 90, No. 6, p. 2892, 2001

c

Fig. 8 A sample of 12 experimentally measured pinched hysteresis loops extracted from dozens of similar loops published in the literature on a large variety of resistance switching devices, made from different materials, processes and physical mechanisms



An example from year 2002

Xiangfeng Duan, Yu Huang, and Charles M. Lieber,
"Nonvolatile Memory and Programmable Logic from Molecule-Gated Nanowires,"
Nano Letters, Vol. 2, No. 5, p. 487, 2002

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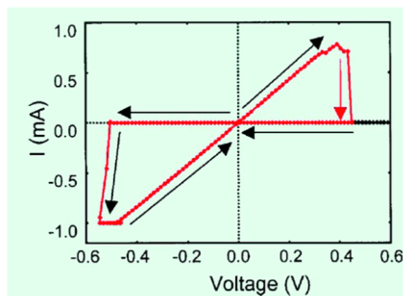

Current–voltage characteristic of a large area sample with 200-nm $Zn_{0.4}Cd_{0.6}S$ and Pt Schottky diode

An example from year 2003

P. van der Sluis,
"Non-volatile memory cells based on $Zn_xCd_{1-x}S$ ferroelectric Schottky diodes,"
Appl. Phys. Lett., Vol. 82, No. 23, p. 4089, 2003

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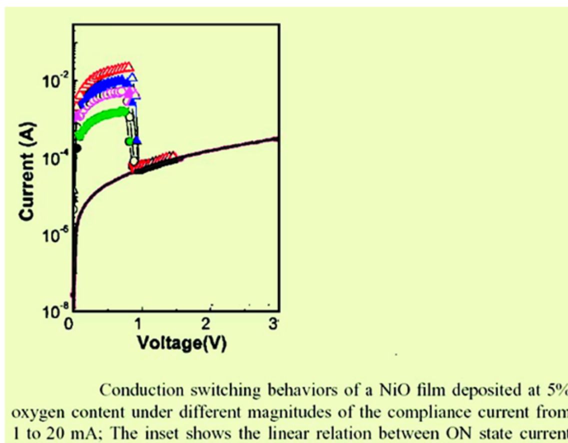

Conduction switching behaviors of a NiO film deposited at 5% oxygen content under different magnitudes of the compliance current from 1 to 20 mA; The inset shows the linear relation between ON state current

An example from year 2004

S. Seo, M. J. Lee et al,
"Reproducible resistance switching in polycrystalline NiO films,"
Appl. Phys. Letters, Vol. 85, No. 23, p. 5655, 2004

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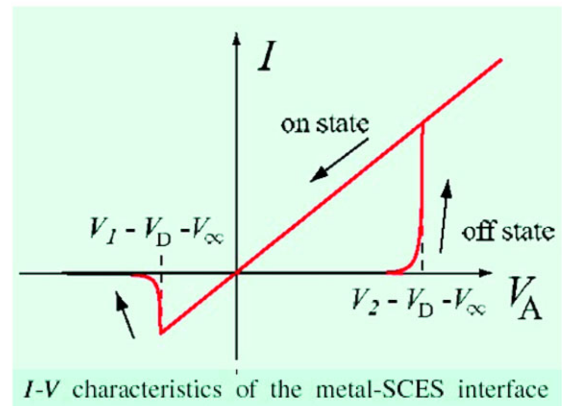
Fig. 8 (*Continued*)



I-V characteristics of the metal-SCES interface

An example from year 2005

Takashi Oka1 and Naoto Nagaosa,
"Interfaces of Correlated Electron Systems: Proposed Mechanism for Colossal Electroresistance,"
Physical Review Letters, Vol. 95, p. 266403, 2005

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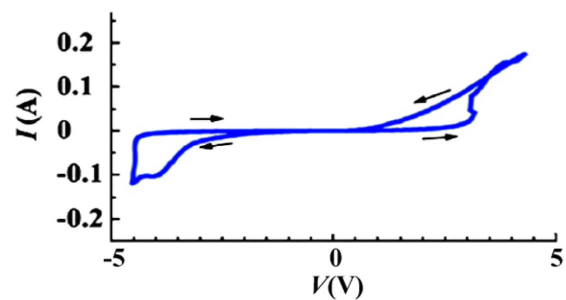

An example from year 2006

A. Sawa, T. Fujii, M. Kawasaki, Y. Tokura,
"Interface resistance switching at a few nanometer thick perovskite manganite active layers,"
APPLIED PHYSICS LETTERS, Vol. 88, p. 232112, 2006

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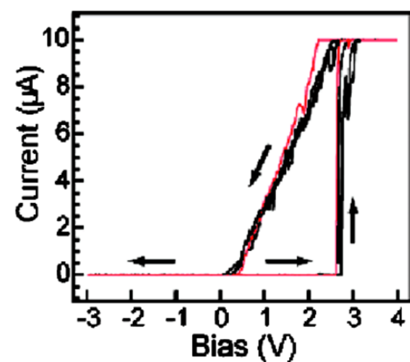

An example from year 2008

Yajie Dong, Guihua Yu, Michael C. McAlpine, Wei Lu, and Charles M. Lieber,
"Si/a-Si Core/Shell Nanowires as Nonvolatile Crossbar Switches,"
Nano Letters, Vol. 8, No. 2, p. 386, 2008

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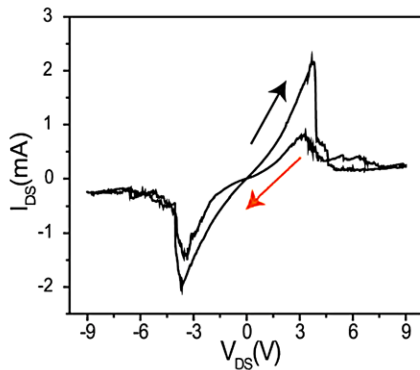
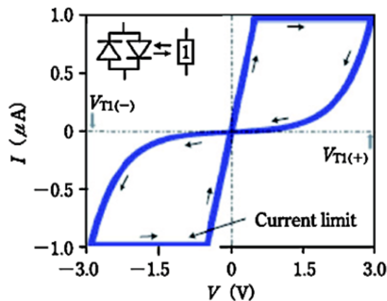
Fig. 8 (*Continued*)



An example from year 2009

Y. F. Li,T. Kaneko, and R. Hatakeyama
"High-performance negative differential resistance behavior in fullerenes encapsulated double-walled carbon nanotubes,"
J. Appl. Phys.,Vol. 106, No. 12, 124316, (2009)

j



An example from year 2010

Yoshihisa Fujisaki
"Current Status of Nonvolatile Semiconductor Memory Technology"
Japanese Journal of Appl. Phys.,Vol. 49, No. 10, pp., 100001, (2010)

k

Fig. 8 (*Continued*)

7.1 Non-volatile memristors

A careful examination of the 12 memristor pinched hysteresis loops exhibited in Figs. 8(a) to 8(k) shows that except for Figs. 8(a), 8(d), and 8(h), most of the loops can be reproduced approximately by the preceding simpler memristor (44a)–(44b). A few of the pinched hysteresis loops, such as Figs. 8(a), 8(d), 8(i) and 8(j) contains small oscillatory or noisy signal components superimposed upon them. Since the cited authors did not provide details on how their pinched hysteresis loops were measured, we can only conjecture that these small-signal components were either artifacts of their measurement systems, or they may represent genuine nonlinear dynamical phenomena. In the latter case, it may be necessary to use the generic memristor (40a)–(40b) to reproduce them. We wish to stress, however, that even this seemingly complex case would represent only the tip of an iceberg of vast nonlinear dynamical phenomena, such as chaos, which is not considered in this tutorial. Indeed, to build a non-volatile resistance switching memory exhibiting the fine details depicted in some of the pinched hysteresis loops shown in Fig. 8, we only need to consider a subclass of the memristor morphing function $\mathbf{f}(\mathbf{x}, i)$ in (40b), namely, the class satisfying the condition

$$\mathbf{f}(\mathbf{x}, i) = 0, \quad \text{whenever } i = 0 \tag{45a}$$

Under the constraint imposed by (45a), the memristor state equation is thereby endowed with the following *non-volatility property*:

$$d\mathbf{x}/dt = \mathbf{f}(\mathbf{x}, i) = 0, \quad \text{when } i = 0 \tag{45b}$$

In other words, $(\mathbf{x}, i) = (\mathbf{x}, 0)$ is an equilibrium point of the memristor state (40b), for *any* value of $\mathbf{x}$. Hence, we have a continuum of *stable equilibrium points*, when $i = 0$, just as in the case of the ideal memristor of yore. This means that when we switch off the power at $t = 0$, such that $i(t) = 0$, for $t > 0$, the *state* vector $\mathbf{x}$ in (42) does not have to tend to zero, but is held unchanged at $\mathbf{x}(t) = \mathbf{x}(0)$ for all $t > 0$, where $\mathbf{x}(0)$ can be set by applying an appropriate input switching signal. But since we can choose many state variables, along with their numerous unfolding parameters, the device engineer has many degrees of freedom to massage his memristor model and optimize a memristance function $R(\mathbf{x}, i)$, and a corresponding memristor morphing function $\mathbf{f}(\mathbf{x}, i)$, to develop a memristor model capable of reproducing almost any fine details observed from their experiments.

7.2 Negative resistance

Let us observe next that the pinched hysteresis loops shown in Fig. 8(h) and Fig. 8(k) contain a non-monotonic current-controlled region with a "negative" slope (i.e., a negative small-signal resistance), implying that the device is locally active [3], and is capable of oscillation under dc bias. Such a pinched hysteresis loop could not be realized by any ideal passive memristor [1], but it can be realized by connecting a locally active current-controlled nonlinear resistor in series with a passive *memristor* described by (44a), as shown in Fig. 9(a). Note that the resulting one-port in Fig. 9(a) is equivalent to a memristor described by the generic memristor (40a)–(40b).

To prove this equivalence property, let the memristor be described by

$$v_1 = R(\mathbf{x})i_1 \tag{46a}$$

Let the locally active current-controlled nonlinear resistor be described by

$$v_2 = h(i_2) \tag{46b}$$

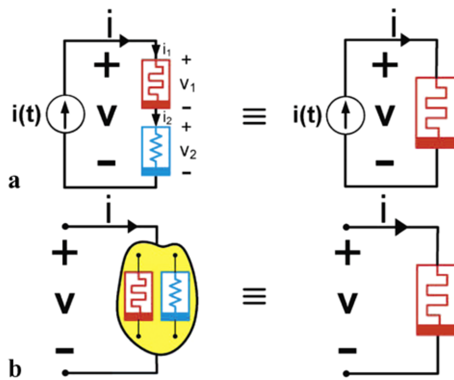


Fig. 9 The memristor-resistor series connected circuit in (**a**) is equivalent to another memristor with a transformed characteristic. In general, a one-port (2-terminal black box) made of arbitrary interconnections of arbitrary assortments of memristors and resistors is also equivalent to a memristor characterized by a more complex constitutive relation [3]

Applying Kirchoff Current Law (KCL), we obtain

$$i = i_1 = i_2 \tag{47}$$

Applying the Kirchoff Voltage Law (KVL), we obtain

$$v = v_1 + v_2 \tag{48}$$

Substituting (46a)–(46b) into (48), and making use of (47), we obtain the following equation for the one-port:

$$v = R(\mathbf{x})i + h(i) \tag{49}$$

Since (49) is a special case of (40a), the composite one-port in Fig. 9(a) is a memristor. The above example is but a special case of the following general result.

Memristor-resistor interconnection theorem

Any one-port made of an arbitrary interconnection of *memristors* and *passive* nonlinear *resistors*, is equivalent to a memristor described by either (40a)–(40b), or by an implicit system of equations, whose behavior seen from outside the composite one-port shown in Fig. 9(b) bears all of the fingerprints of a memristor [2].

7.3 Is memristor negative resistance real or artifact?

A careful examination of Figs. 8(a), 8(d), 8(h) and 8(k) reveals that these pinched hysteresis loops contain a small region with a negative slope. Assuming these regions are real measurements pertaining to the device, and not artifacts introduced via the measuring instruments, and/or their inflexible softwares, can we conclude that these devices are endowed with a *small-signal* (i.e., *differential*) *resistance* operating region, and hence is *locally active*, and can be designed to amplify small signals, and/or to function as an oscillator [3] via an external biasing circuit?

The answer is *no*! Indeed, in many cases, the negative slope is merely a manifestation of a *phase-lag* between the *maxima* (or, *peak*) of the response voltage $v(t)$ (resp., current $i(t)$) and the *peak* of its excitation current waveform $i(t)$ (resp., voltage waveform $v(t)$). This phenomenon is best seen in Figs. 1(b), 1(c), and 1(d) where the voltage peak in Fig. 1(d) lags behind the input current peak in Fig. 1(c). Observe that there is a short time interval where the voltage $v(t)$ in Fig. 1(d) increases while the input current $i(t)$ decreases. This phenomenon occurs after the pinched hysteresis loop in Fig. 1(b) reaches its peak at $i = 1$, and is the sole mechanism which gives rise to the negative slope. It has nothing to do with local activity [3]!

So how can we determine which of the pinched hysteresis loops in Fig. 8 with a negative-slope region is a *bona fide* small-signal resistance? The generic answer is we do not know unless we have already derived a realistic memristor circuit model, such as Fig. 9, or a memristor state equation, such as (40b), where we can find a point (V, I) on the negative-slope region of the pinched hysteresis loop which can be proved analytically to be an equilibrium point (otherwise known as a dc operating point in electronic circuit jargon), namely,

$$d\mathbf{x}/dt = \mathbf{f}(\mathbf{x}, I) = 0, \qquad V = R(\mathbf{x}(I), I)I \tag{50$'$}$$

for some state variable $\mathbf{x} = \mathbf{x}(I)$, which depends on I. This means that there exists a dc operating point (V, I) where, in the absence of noise, there is a state variable $\mathbf{x} = \mathbf{x}(I)$ where the *composite* memristor-biasing circuit is in *equilibrium*. This situation is usually not observable experimentally because the memristor small-signal resistance would usually make the circuit unstable, resulting in an *oscillation*. This alone suffices to conclude that the memristor is locally active. However, for pedagogical reasons, we can design an appropriate external stabilizing biasing circuit such that the composite circuit is *locally asymptotically stable* [3], whereupon the dc operating point (V, I) on the memristor pinched hysteresis loop can actually be measured. Alternately, we can determine whether the memristor is *locally active* by deriving first either a memristor circuit model, or a memristor state equation, and then apply standard nonlinear circuit analysis methods to determine whether there exists a *locally active* equilibrium point [3].

Observe that for an ideal memristor we have $x = q$, and the equilibrium state equation

$$dq/dt = I = 0 \tag{50$''$}$$

does not have a solution if $I \neq 0$. It follows that *an ideal memristor can have only one dc operating point*; namely, the origin $(v, i) = (V, I) = (0, 0)$. If the small-signal resistance at the origin is negative, this would imply that the

pinched hysteresis loop has a branch which crosses the origin into the 2nd and the 4th quadrants of the v–i plane, implying that the memristor is *not passive*. It follows therefore that *an ideal memristor cannot exhibit a small-signal negative resistance* unless it is locally active at the origin, which is possible only if the memristor has an internal source of power, such as light, chemical or nuclear reactions, or batteries, as demonstrated in Fig. 4(f), page 511 of [1], where a locally active memristor exhibiting a negative slope at the origin of the q vs. φ curve was built using transistors and op amps (see Fig. 2, p. 509 of [1]), powered by batteries. We can conclude therefore that if the pinched hysteresis loop of a physical device without internal power source exhibits a *bona fide* small-signal negative resistance, then that device cannot be an *ideal* memristor, and must therefore be an unfolded memristor sibling, characterized by (40a)–(40b).

8 Switching and sensing resistance memory

We have presented in the preceding section a very special subclass, albeit of great interests to the theme of this special issue, of memristors whose members are endowed with the priceless, and timeless, gift of *non-volatile memories*. This subclass is defined by the memristor constitutive relation

$$v = R(\mathbf{x}, i)i \tag{50}$$

$$d\mathbf{x}/dt = \mathbf{f}(\mathbf{x}, i) \tag{51}$$

where the *memristance function* $R(\mathbf{x}, i)$ satisfies the memristor passivity condition

$$R(\mathbf{x}, i) \geq 0 \tag{52}$$

and where the *memristor dynamical function* $\mathbf{f}(\mathbf{x}, i)$ satisfies the following condition.

Continuous non-volatility condition

$$\mathbf{f}(\mathbf{x}, i) = 0, \quad \text{if } i = 0 \tag{53}$$

The non-volatility condition (53) ensures that *any* state variable $\mathbf{x}$ is a stable, non-isolated, *equilibrium point* of the memristor state equation (51) when $i = 0$, or equivalently, when the power is switched off. In other words, (53) is the genesis of the memristor's memory non-*volatility*. Observe that since every $\mathbf{x}$ is an equilibrium state of (51) when $i = 0$, the subclass of memristors defined by (53) has a *continuum of equilibrium states*, where every equilibrium state is stable, but not asymptotically stable [3] in the sense that while small perturbations around each equilibrium state may perturb its location slightly, it will never diverge beyond its perturbed boundary [3]. Hence, in principle, every memristor satisfying (53) is endowed with an infinite memory store. In the context of this special issue, we will consider only the special case of *binary* memory where only two sufficiently distant memory states are of interest because they will be used to store the "0" and "1" states for digital electronics. In this case, the ideal memristor φ vs. q curve only needs to have two approximately linear regions, where one region should have as small a slope as possible, while the other region should have as large a slope as possible.

The *Continuous non-volatility condition* (53) guarantees a *continuum* of *tunable resistances*, which is essential for *synaptive learning applications*. For *non-volatile binary memory applications*, we can replace (53) by the following less restrictive condition.

Discrete non-volatility condition

$$\mathbf{f}(\mathbf{x}', 0) = 0 \quad \text{and} \quad \mathbf{f}(\mathbf{x}'', 0) = 0 \tag{53$'$}$$

where $\mathbf{x}'$ and $\mathbf{x}''$ denote two *locally asymptotically stable equilibrium points* of the memristor state equation (40b) with $i = 0$, i.e.,

$$d\mathbf{x}/dt = \mathbf{f}(\mathbf{x}, 0) \tag{40b$'$}$$

As an example, consider the state equation:

$$dx/dt = x - x^3 - i \tag{40b$''$}$$

Here, $x = x' = 1$ and $x = x'' = -1$ are two *isolated* locally asymptotically stable equilibrium points of

$$dx(t)/dt = x - x^3 \tag{40b$'''$}$$

obtained by setting $i = 0$ in (40b$''$).

Let us now pause to consider some examples.[12]

Any device capable of non-volatile memory is useless unless it is relatively easy and inexpensive to sense its memory state. One of the great virtues of the memristor is that since its memristance function in (44a) is a state-dependent resistance obeying Ohm's law, one only needs to inject a small sensing voltage (resp., current), and observe its response. Since in practice, the two resistance memory states R_{OFF} and R_{ON} are chosen so that their ratio is sufficiently large, one can easily determine the memory state by observing the magnitude of the current (resp., voltage) response, to a small ac sensing voltage (resp., current) signal, or a small doublet-like pulse signal with a zero average area. The reason for requiring the sensing signal to have a zero dc average is to prevent the location of a *non-isolated* memory state from slowly drifting away.

[12] The two memory states are chosen sufficiently far apart in practice to enhance robustness and reliability.

Memristor switching example 1: bipolar switching

Let us revisit the two-state charge-controlled memristor in Fig. 5. To switch from the low-resistance state R_1 corresponding to the middle segment with a small slope to the high-resistance state R_0 corresponding to the upper segment with the much steeper slope, we simply apply a sufficiently large current pulse so that its corresponding charge $q(t)$ would traverse beyond the charge breakpoint $q = B$. To switch back from a point on the upper segment (*high-resistance* state R_0, simply apply a similar pulse of the opposite polarity. This method of switching is usually referred to as *bipolar* resistance switching. Our next example illustrates how switching can be achieved by applying switching pulses of the same polarity, but of different amplitudes, often referred to in practice as *unipolar* resistance switching.

Memristor switching example 2: unipolar switching

Consider the flux-controlled memristor depicted in Fig. 10 with a 7-segment piecewise-linear φ–q curve (Fig. 10(a)). Here the three parallel red segments with a steep slope have a high conductance state G_{ON}, whereas the four parallel green segments with a much smaller slope have a much smaller conductance state G_{OFF}. For the memristor constitutive relation shown in Fig. 10(a), we can switch from a high conductance state to a low-conductance state with a relatively small-amplitude voltage pulse since it only needs a small increment $\Delta\varphi$ in φ to cross the breakpoint B_1 into the low-conductance state. In contrast, a much larger—amplitude voltage—pulse, but of the *same polarity*, and the *same pulse width*, would be needed in order to reach the next breakpoint B_2, and beyond, in order to switch back to a high conductance state G_{ON} again. The same switching sequence with the opposite polarity can also be executed to achieve the same results, as illustrated in Fig. 10(b). The corresponding switching loci plotted in the v–i plane is shown in Fig. 10(c). Here, to prevent the excessive current jump from a small current to a very high current, thereby damaging the device, measuring instruments are normally programmed to clamp the current at a maximum safe value, called the "compliance current level" in industry, as illustrated in Fig. 10(c). The above mode of using voltage pulses of the same polarity to switch between low- and high-resistance states has been reported in some so-called "*unipolar*" devices in industry [11].

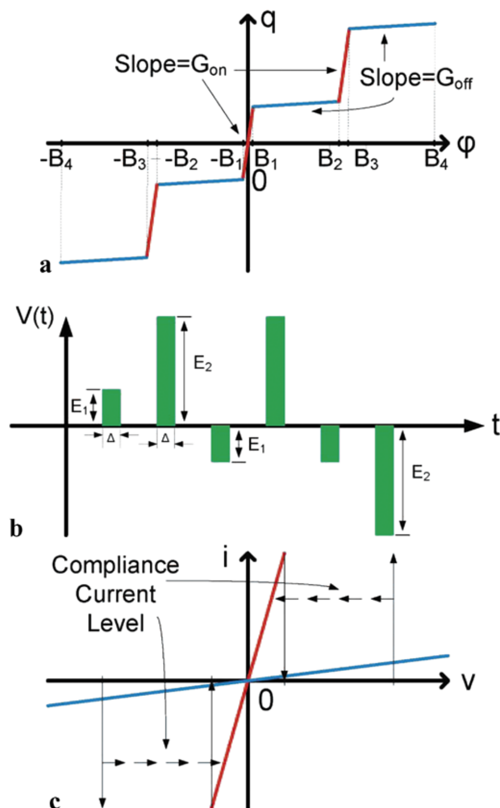


Fig. 10 A "staircase-like" flux-controlled memristor can switch from a high conductance to a low-conductance state using voltage pulses of the same polarity, somewhat reminiscent of the "unipolar" switching characteristic depicted in Fig. 1(a) of [7]

9 Concluding remarks

Any electronic device with only two electrical terminals is usually referred to in the semiconductor industry as a nonvolatile resistance-switching memory device if the device can exhibit one of two resistance values over a sufficiently long time period, without consuming any power, and can be switched from a low-resistance state to a high-resistance state, and vice versa, by applying either a short voltage pulse, or a short current pulse, of appropriate amplitude and polarity, across the two device terminals, and such that the resistance state at any time, either low or high, can be sensed by applying a relatively much smaller sensing voltage pulse, or current pulse, of some preset waveform, across the same terminals.

Implicit in the above definition is that at any time, the device can be modeled as a linear resistor obeying *Ohm's Law*, when the sensing signal amplitude is sufficiently small, for otherwise, the word resistance would be meaningless. The *linearity* property implies that the sensing voltage, or current, and its corresponding voltage response, or current response, have identical waveforms, and have the same zero-crossings in time. It follows that the loci in the v–i plane during sensing when observed from an oscilloscope will appear as a short linear segment through the origin whose slope will be small if the resistance being sensed is low, or much larger, if the resistance being sensed is high. In other words, the two resistance states can be depicted as two short straight line segments of slopes R_1 and R_2, crossing each other at the origin of the v–i plane. These two segments can be emu-

lated exactly by an *ideal* memristor having the memristance $R(q) = R_1$ at the origin, and $R(q) = R_2$ at another point, say $q = q_2$ of a smooth φ vs. q curve in the φ vs. q plane. By uncovering the physical operating mechanisms taking place internal to the device, one could construct a model that not only exhibits these two memristances, but also faithfully reproduces one or more pinched hysteresis loops, measured using different large-amplitude periodic signals [12]. The resulting mathematical expressions may be extremely complex, and may often be expressible only by implicit mathematical equations. Nevertheless, they would define a memristor of the generic form given by (40a)–(40b), by virtue of the characteristic property of the memristor.

The take-home lesson from this tutorial can be summarized succinctly as follow:

> Any 2-terminal electronic device devoid of internal power source and which is capable of switching between two resistances upon application of an appropriate voltage or current signal, and whose resistance state at any instant of time can be sensed by applying a relatively much smaller sensing signal, is a *memristor*, defined either by the ideal memristor equation, or by one of its unfolded siblings via (40a)–(40b).

Our final remark is concerned with the significance of the pinched hysteresis loop in the modeling of non-volatile resistance switching memories. Let us recall that while the *memristance vs. state map* tells us the complete set of *small-signal memristances* endowed upon a memristive device, it is rather difficult to measure them experimentally unless the memristor can be modeled by the ideal memristor equation $v = R(q)i$, where $dq/dt = i$. To extract such information from the generic memristor (40a)–(40b), we have to identify first the relevant state variable, or state variables in cases demanding a higher-order memristor state space. In contrast, the *chord memristances* associated with a pinched hysteresis loop can be readily extracted since it is simply the set of all slopes of a straight line anchored at the origin whose tips traces along the loci of a measured pinched hysteresis loop. Each such chord resistance is a true resistance indistinguishable from a linear resistor having the same resistance. The set of all such chord memristances associated with a pinched hysteresis loop therefore provides a subset of the memristor's endowed small-signal memristances. Since measuring pinched hysteresis loops associated with different periodic input voltage, or current, waveforms applied across a memristive device is a relatively simple task that could be automated,[13] it is a useful tool for uncovering a memristive device's nonlinear physical operating mechanisms, and for validating its memristive models. In the case of an *ideal memristor*, it is important to bear in mind that the *small-signal memristance*, and its corresponding *chord memristance*, represent exactly the same information. The main difference is that while the chord memristance is a long vector pinned at the origin of the v–i plane, its corresponding small-signal memristance is an infinitesimal tangent attached at each point on an ideal memristor's constitutive relation in the φ vs. q plane. It is also useful to note that unlike classical electronic circuit analysis, the small-signal memristor voltage associated with an applied small-signal memristor current represents the *actual total* solution, and is not superimposed upon some dc bias. We end this tutorial with the following terse characterization of a resistance switching memory device:[14]

If it's pinched, it's a memristor.

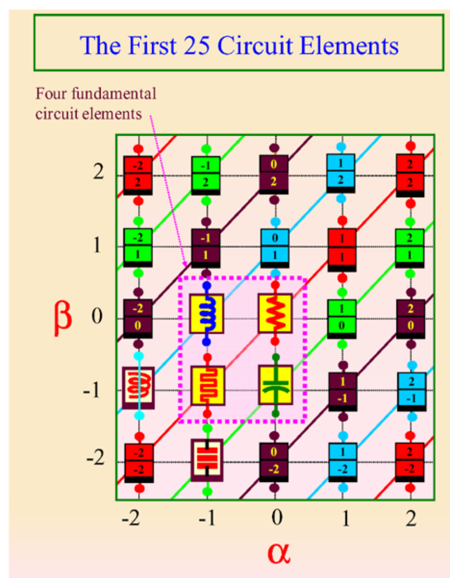


Fig. 11 An enlargement of the first 25 axiomatically defined circuit elements from the periodic table of circuit elements (Fig. 31 of [3]) where the four basic circuit elements (resistor, capacitor, inductors and memristor) are replaced by their symbols. The ***memcapacitor*** is located at $(a, b) = (-1, -2)$ and the ***meminductor*** is located at $(a, b) = (-2, -1)$. Observe that since these two elements require double time integrals of voltage and current, their dynamics are of a higher order than those of the four basic circuit elements enclosed inside the dotted *red box*

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[13]Measurement instrument companies could exploit the high market potentials of automated pinched-hysteresis-loop measuring instrumentations, and their memristance extractions.

[14]Exactly the same theory of the memristor can be used to identify a memcapacitor (acronym for memory capacitor), and a meminductor (acronym for a memory inductor), from the table of axiomatically-defined circuit elements [3] and [4], as depicted in Fig. 11, and presented at the 2008 Berkeley Symposium on Memristors and Memristive Systems (Part 1, towards the end of the opening lecture) on Nov. 21, 2008 (proceedings of this symposium were videotaped and available via YouTube), as well as further elucidated in [13] and [14].

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