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Wafer-scale graphene on 2 inch SiC with uniform structural and electrical characteristics

JIA YuPing, GUO LiWei*, LIN JingJing, CHEN LianLian & CHEN XiaoLong*

Research & Development Center for Functional Crystals, Beijing National Laboratory for Condensed Matter Physics, Institute of Physics, Chinese Academy of Sciences, Beijing 100190, China

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Wafer-scale graphene on SiC with uniform structural and electrical features is needed to realize graphene-based radio frequency devices and integrated circuits. Here, a continuous bi/trilayer of graphene with uniform structural and electrical features was grown on 2 inch 6H-SiC (0001) by etching before and after graphene growth. Optical and atomic force microscopy images indicate the surface morphology of graphene is uniform over the 2 inch wafer. Raman and transmittance spectra confirmed that its layer number was also uniform. Contactless resistance measurements indicated the average graphene sheet resistance was 720 Ω/□ with a non-uniformity of 7.2%. Large area contactless mobility measurements gave a carrier mobility of about 450 cm^2/(V s) with an electron concentration of about 1.5×10^{13} cm^{-2}. To our knowledge, such homogeneous morphology and resistance on wafer scale are among the best results reported for wafer-scale graphene on SiC.

graphene, wafer scale, resistivity, mobility, morphology

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Since the discovery of graphene in 2004 [1], it has received significant interest as a contender in post-CMOS applications [2], as well as a promising candidate for fundamental studies, even being considered as a substitute for silicon in future micro- and nanoelectronic device applications [3–6]. Thus, a flurry of research with the goal of obtaining large-area graphene is in progress to realize graphene applications. So far, the two typical, viable methods of fabricating large-area graphene are thermal decomposition of SiC and chemical vapor deposition (CVD) on metal substrates. Large-area graphene grown by CVD has potential applications in transparent electrodes and flexible displays [7–10], while wafer-scale epitaxial graphene (EG) grown on SiC has potential in high frequency devices [11] and integrated circuits (ICs) [12,13] because of its compatibility with current IC procedures. Currently, graphene grown by CVD has achieved a size of more than 30 inches [4]. However, graphene fabricated on metal substrates by CVD must undergo a transfer procedure to realize its application, and graphene quality can be deteriorated by the transfer process [9]. Thermal decomposition of SiC is a more feasible method to grow graphene on SiC as a fundamental material for radio frequency devices or ICs. This EG can be directly patterned using standard lithography methods without requiring transfer as in the case of graphene grown by CVD. Wafer-scale EG grown on SiC by thermal decomposition of SiC [5,6] has been reported repeatedly, but this has seldom been achieved by CVD [14]. In the thermal decomposition procedure, growth under argon at atmospheric pressure was considered to be better than that under ultra high vacuum to obtain a more homogeneous graphene sample [6]. However, EG with uniform structure and electronic properties on the macroscopic scale has never been reported. Furthermore, the reported values of carrier mobility on a wafer-scale substrate are extremely different [14,15]. We consider that this difference is related to the uniformity of the graphene sample. In this work, bi/tri-layers of EG were grown on a 2 inch 6H-SiC (0001) substrate that show macroscopic homoge-

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*Corresponding authors (email: lwguo@aphy.iphy.ac.cn; chenx29@aphy.iphy.ac.cn)

neous topography and uniform electrical properties. The possible factors governing the uniformity of the EG are discussed.

1 Experimental

In our experiments, graphene was grown using custom-built physical vapor transport (PVT) equipment by high temperature annealing of SiC under argon at ambient pressure. Prior to the growth of graphene, a 2 inch semi-insulating 6H-SiC (0001) wafer (Beijing TankeBlue Co., Ltd., Beiing, China) was carefully cleaned using acetone, ethanol and deionized water in sequence. After cleaning, the SiC wafer was loaded into a graphite crucible and placed in the PVT equipment. In a typical fabrication procedure, the sample was annealed at a temperature of about 1550°C under argon mixed with 10 vol% H_2 at ambient pressure for 5–10 min to prepare a smooth SiC surface, then an argon ambient for 5–8 min to grow graphene, followed by filling little argon/H_2 mixing gas to etch thicker graphene and power off. The graphene sample was cooled down to room temperature naturally and then removed for characterization. To obtain homogeneous graphene, the SiC wafer was etched with H_2 before and after graphene growth, which was critical to obtain smooth SiC terraces and uniform graphene.

The surface morphology of the graphene samples were analyzed by optical microscopy and atomic force microscopy (AFM), while Raman scattering and optical transmittance spectra were used to identify graphene and its number of layers. Contactless resistance (using LEI 1500 equipment) and Hall (using LEI 1600 equipment) measurements were performed to analyze its electrical properties.

2 Results and discussion

A photograph of the wafer-scale graphene on SiC is shown on the right side of Figure 1(a), and a bare SiC wafer used as a substrate for graphene growth is shown on the left as a reference. Figure 1(b) shows the morphology of the graphene on SiC. Straight, uniformly arranged steps were clearly seen, indicating a well-ordered SiC surface suitable for growth of high quality graphene. The morphology of the graphene grown on this 2 inch SiC wafer was analyzed by AFM measurements using a scale of 50 μm×50 μm at five positions, as shown in Figure 2. The five positions were at the center, top, bottom, left and right of the wafer with a relative distance to the wafer center of about 15 mm for the last four positions. The sample contained wide, smooth terraces that extend long distances (>mm). The terrace widths are uniform, about 10 μm wide, which is sufficient to fabricate an entire device on one smooth terrace. It has been confirmed that the performance of devices fabricated on smooth terraces is improved significantly [11]. The formation of smooth, wide SiC terraces is ascribed to etching the SiC wafer, which provides uniform, smooth SiC terraces for graphene nucleation and growth.

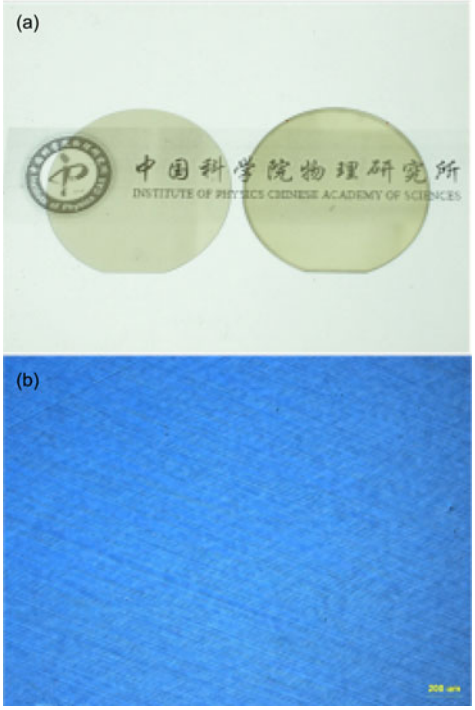


Figure 1 (Color online) (a) Photographs of a bare SiC wafer (left) and graphene-covered SiC wafer (right). (b) Optical microscope image of graphene (scale bar= 200 μm).

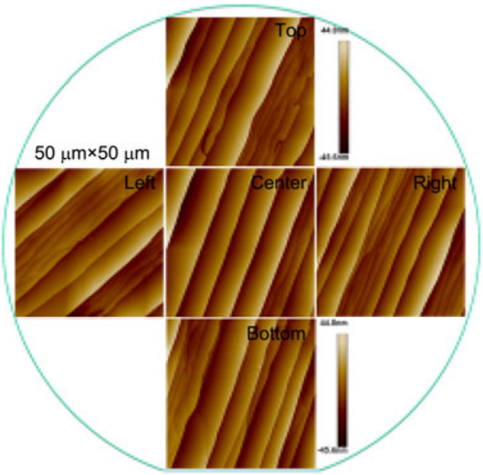


Figure 2 (Color online) Micromorphology of graphene observed by AFM using a scale of 50 μm×50 μm at 5 positions on the wafer: Center and top, bottom, left and right about 15 mm from the center of the wafer.

To determine the layer number of graphene, optical transmittance spectra of the SiC wafer with and without graphene were measured, as shown in Figure 3. The difference of transmittance between the bare SiC wafer and that covered with graphene was about 7.7% at λ=550 nm and 5.9% at λ=800 nm. This suggests that number of layers of

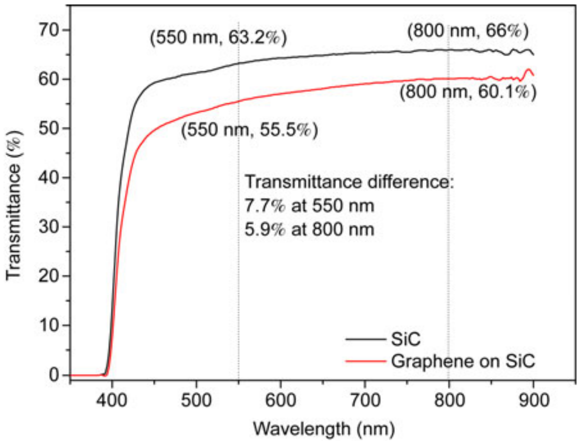


Figure 3 (Color online) Optical transmittance spectra of a bare SiC wafer (black line) and the graphene-covered SiC wafer (red line).

graphene is about 2 to 3, which was inferred from the assumption that the transmittance of a single layer of graphene is about 97.7% independent of wavelength [9–11]. The number of layers of graphene was confirmed by Raman measurements. It is well known that Raman scattering is a quick and facile method to characterize the number of layers and quality of graphene samples [16,17]. To check the uniformity of the number of layers and quality of the graphene sample, Raman scattering measurements were obtained along two lines across the 2 inch SiC wafer normal to each other (one was parallel to the steps, while the other was perpendicular to them) with 11 positions at even distance along each line. Figure 4(a) and (b) show the Raman data measured along the lines perpendicular and parallel to the SiC steps, respectively. The profiles of the Raman spectra are similar and there is no D peak, which is related to structural defects and domain boundaries. The G and 2D peaks are shifted with ranges of 19 cm^{-1} (P_{Gmin}=1593 cm^{-1} and P_{Gmax}=1612 cm^{-1}) and 48 cm^{-1} (P_{2Dmin}=2703 cm^{-1} and P_{2Dmax}=2751 cm^{-1}), respectively, in Figure 4(a), and with ranges of 21 cm^{-1} (P_{Gmin}=1589 cm^{-1} and P_{Gmax}=1610 cm^{-1}) and 55 cm^{-1} (P_{2Dmin}=2699 cm^{-1} and P_{2Dmax}=2754 cm^{-1}), respectively, in Figure 4(b). The peak shifts are quite similar for the two lines and are comparable to those reported in the literature [14]. The small shift of the peaks is probably induced by different strain or doping across the sample [18–20]. Here, we consider that strain is the main cause of the peak shift. The Raman peaks are well fitted by a single Lorentzian lineshape, and their full width at half maximum (FWHM) are 11–17 cm^{-1} for the G peaks and 29–42 cm^{-1} for the 2D peaks. These FWHM values are smaller than most reported for graphene grown on SiC; the FWHM is usually more than 40 cm^{-1} for the 2D peak of 2-layer graphene [21]. In addition, the intensity ratio of the 2D and G peaks ($I_{\mathrm{2D}}/I_{\mathrm{G}}$) is among 2.3–2.8. Considering the relation of $I_{\mathrm{2D}}/I_{\mathrm{G}}$ to the number of layers [22,23] and the relatively small FWHM together with symmetrical 2D peaks [24,25], it is inferred that the graphene sample is 2–3 layers thick over the whole surface of the 2 inch SiC substrate. This is consistent with the optical transmittance spectra shown in Figure 3. The similarity of the Raman profiles and the small FWHM values combined with the absence of a D peak suggest that the graphene fabricated here is highly uniform and suitable for fabricating high performance electronic devices on wafer-scale. The uniformity of the graphene is ascribed to etching the graphene after growth to remove the thicker regions, as well as using a SiC wafer with smooth, uniform terraces as a substrate.

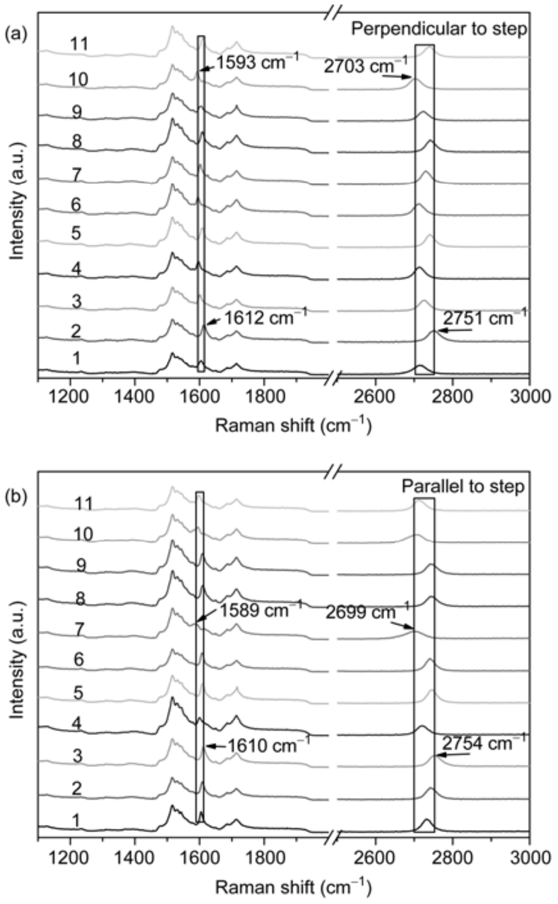
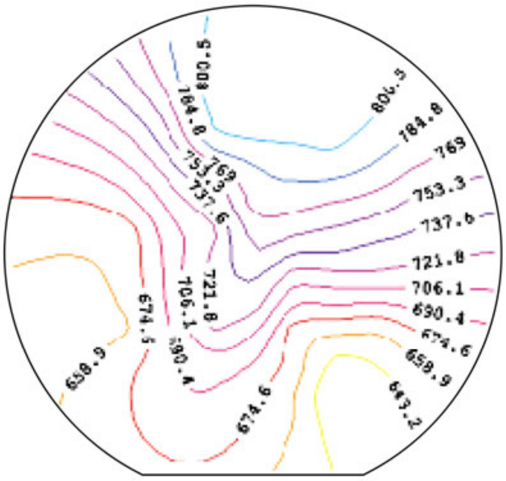


Figure 4 Raman scattering spectra taken along two lines normal to each other through the sample. (a) Perpendicular to the steps of the SiC wafer, and (b) parallel to the steps. Along each line, 11 positions were measured at even spacing.

The electrical properties of the graphene sample were determined by contactless sheet resistance and mobility measurements to confirm its high uniformity and quality. The sheet resistance measurements of the sample are shown in Figure 5. The average sheet resistance was about 720 Ω/□ and the non-uniformity of the sheet resistance was about 7.2% over the 2 inch wafer excluding a 3 mm edge. The uniformity is near that required for commercial application of a semiconductor material, and the best reported to date for wafer-scale graphene. Furthermore, the average Hall mobility was about 450 cm^2/(V s) with an electron concentration



Statistical summary

Number of test points	55
Average value	720.2
Maximum value	815.4
Minimum value	625.7
Sample spread (%)	26.33
Std dev value	51.9
Wafer uniformity value (%)	7.21

Figure 5 (Color online) Sheet resistance mapping of the graphene sample measured at room temperature.

1.5×10^{13} cm^{-2} measured at room temperature on a circular area with a diameter of 2.3 cm. The mobility is near that reported for small-sized devices on EG grown on SiC with the same carrier concentrations [26] and comparable to the recently reported results for wafer-scale graphene grown on SiC by CVD [14] with similar carrier concentration.

3 Conclusions

In summary, a high quality graphene with 2–3 layers was grown on a 2 inch SiC wafer with macro-uniform structural and electrical properties by etching before and after graphene growth. The non-uniformity of its sheet resistance of about 7% over the 2 inch wafer approaches the level required for commercial application of semiconductor materials. By further optimizing and improving this growth procedure, it may be possible to realize controlled fabrication of wafer-scale graphene suitable for commercial applications.

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