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Modeling and Characterization of VCOs with MOS Varactors for RF Transceivers

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As more broadband wireless standards are introduced and ratified, the complexity of wireless communication systems increases, which necessitates extra care and vigilance in their design. In this paper, various aspects of popular voltage-controlled oscillators (VCOs) as key components in RF transceivers are discussed. The importance of phase noise of these key blocks in the overall performance of RF transceivers is highlighted. Varactors are identified as an important component of LC-based oscillators. A new model for accumulation-mode MOS varactors is introduced. The model is experimentally verified through measurements on LC-based VCOs designed in a standard 0.13 μm CMOS process.

1. INTRODUCTION

In the recent years, the demand for wireless communications has increased considerably. Wireless communication systems encompass a wide variety of standards. Such systems include cellular phones (e.g., GSM, CDMA), wireless local area networks (WLANs), wireless personal area networks (WPANs), wireless metropolitan area networks (WMANs), and so forth. The adoption of any of these technologies depends on many variables such as cost and market demand. Over time, the implementation cost of the technologies goes down, which further accelerates their adoption. The high-tech market research firm, In-Stat, forecasts that the worldwide wireless market will grow to more than 2.3 billion subscribers by 2009.

Typical RF transceivers have a built-in frequency synthesizer, namely local oscillator (LO), to generate a signal with the desired frequency used for up and down conversions. Wireless standards strictly specify the minimum level of the received signal, the maximum level of unwanted signal, the channel bandwidth, and the spacing between two adjacent channels. Using these specifications and targeting the required signal-to-noise ratio (SNR) after downconversion, the maximum amount of acceptable phase noise on the LO can be calculated. This procedure is conceptually depicted in Figure 1 for the GSM-1800 standard. Using the information provided in the figure and knowing the desired SNR (e.g., 9 dB after downconversion), the maximum acceptable phase noise at 600 kHz offset from the carrier (which is at the center of the adjacent channel) is calculated to be −121 dBc/Hz [1].

Figure 2 illustrates the problems that may arise if the LO spectrum extends to the adjacent channel with relatively high-power spectral density: after downconversion, there will be an overlap between the spectra of the desired signal and the unwanted adjacent channel. Unless a special technique is used, the recovery of the data becomes almost impossible.

LOs are usually in the form of voltage-controlled oscillators (VCOs) and are placed inside a feedback loop as part of a phase-locked loop (PLL) system. As a result, they constantly align their zero-crossings with the reference clock. The amount of generated phase noise, within the bandwidth of the PLL, can be reduced by the loop characteristics. Table 1 compares the maximum allowable phase noise of some of the wireless standards at their nominal frequencies.

Figure 3 shows the block diagram of a PLL-based frequency synthesizer typically used in integrated wireless transceivers. This synthesizer comprises of phase (and usually frequency) detector (PD or PFD), charge pump, lowpass

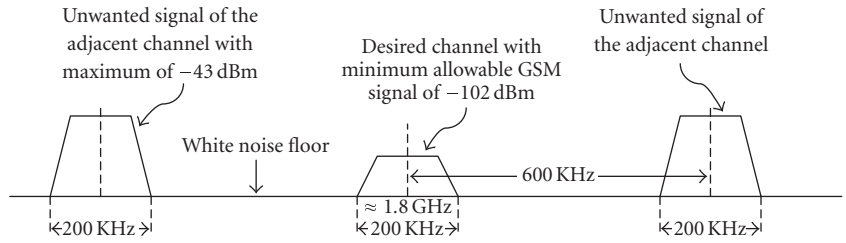


Figure 1: GSM channel around 1.8 GHz.

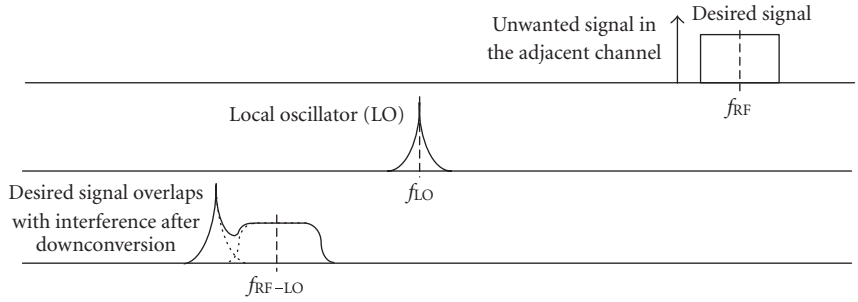


Figure 2: Channel interference in the case of larger-than-expected phase noise.

filter, voltage-controlled oscillator (VCO), reference, and feedback divider blocks (/M and /N). The output frequency of the block is N/M times the reference frequency. Therefore, by adjusting the N/M ratio, different multiples (integer or fractions) of the reference frequency can be generated.

The phase transfer function from the reference to the output of this system exhibits a lowpass characteristic. As a result, high-frequency phase noise[1] of the reference clock is attenuated by the loop, while its low-frequency (close-in) noise passes through the system to the output. On the other hand, phase jitter of the VCO will see a high-pass function to the output, which means that low-frequency jitter of the VCO is suppressed within the bandwidth of the phase-locked system.

The total output phase noise is a function of the phase noise of each of the PLL blocks, the input phase noise generated by the reference clock, and noise shaping characteristics of the loop. While there are different techniques for optimizing the performance of the synthesizers to reduce the total phase noise, VCO plays a key role in total phase noise of the system. This is because high-frequency perturbation on the VCO control line tends to appear at the output in the form of phase variations. In addition, any high-frequency (a.k.a. out-of-band) phase noise generated by the VCO due to supply, substrate, or device noise cannot be suppressed by the loop and directly travels to the output. In this paper, our main focus will be on VCO as a key block of RF transceivers.

[1] The time-domain counterpart of phase noise is jitter, which is a more common term in wireline applications.

Frequency synthesizer circuits have been predominantly implemented in technologies such as III-V, silicon bipolar, or SiGe BiCMOS due to their high-speed and low-noise characteristics. However, circuits implemented in these technologies are still expensive, and are not very area efficient. Moreover, they are not suitable for system-on-chip integration. Recent advances in CMOS technologies have made CMOS an attractive alternative for implementing high-speed systems, including their oscillators. Advantages of CMOS implementation include lower cost, higher manufacturing yield, lower power, and higher levels of integration, with the possibility of integrating analog and digital circuits on the same chip. Therefore, there is a growing trend in industry to extend the use of CMOS circuits to high-speed integrated digital and mixed-signal systems, system-on-a-chip (SoC), and system-in-a-package (SiP) designs. However, designing high-speed mixed-signal circuits (e.g., multi-gigahertz systems) in advanced CMOS technologies is very challenging. Issues such as speed, substrate noise coupling, reduced voltage headroom, and increased leakage current pose many difficulties in the design of high-speed CMOS circuits.

In the following sections, first, various aspects of some of the well-known VCO architectures, including their phase noise performance, are compared. LC VCO is identified as having the best performance in terms of phase noise. In Section 3, the building components of various LC VCOs are investigated and their effects on overall phase noise are studied. To facilitate this investigation, three forms of LC VCOs are used that are implemented in a standard 0.13 μm CMOS process. In addition, some varactor test structures are used to characterize the tuning curve of the LC VCOs and their

Table 1: Comparison between phase noises of different wireless standards.

Wireless standard		Frequency	Phase noise
GSM	850	850 MHz	−121 dBc/Hz at 600 KHz
	900	900 MHz	−121 dBc/Hz at 600 KHz
	1800	1800 MHz	−121 dBc/Hz at 600 KHz [1]
	1900	1900 MHz	−121 dBc/Hz at 600 KHz
WLAN	802.11a	5 GHz	Many WLAN transceivers specify "integral" noise in degrees rms over a frequency range, for example, integral of phase noise from 10 K to 10 M < 1.2° rms for the whole TX path, or 0.8° rms for the synthesizer. This may also be translated to an average phase noise spec, like P.N. < −90 dBc/Hz at < 100 KHz (in-band, or close-in)
	802.11b	2.4 GHz	
	802.11g	2.4 GHz	
WPAN	ZigBee (802.15.4)	900 MHz 2.4 GHz	−95 dBc/Hz at 5 MHz
	Bluetooth (802.15.1)	2.4 GHz	−94 dBc/Hz at 100 KHz [2]

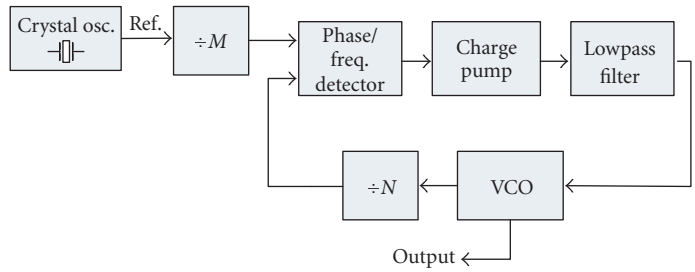


Figure 3: A block diagram of a frequency synthesizer.

relationship with the C-V curve of varactors. A new practical model for accumulation-mode MOS varactors is then introduced. Experimental results follow in Section 4 and concluding remarks in Section 5.

2. COMPARISON OF POPULAR VCO ARCHITECTURES

VCOs are one of the main building blocks of RF transceivers. They are utilized inside PLL-based circuits (e.g., frequency synthesizers as part of LO) to generate a clean and low-jitter clock signal for the operation of other blocks of the frequency synthesizer or transceiver. Typical oscillator circuits require some form of positive feedback around a gain stage in order to sustain their oscillation. This concept is illustrated in Figure 4. The closed-loop system (oscillator) has to fulfill the following two Barkhausen conditions at all times for continuous oscillation:

$$\begin{aligned} |H(j\omega)| &\geq 1, \\ \angle H(j\omega) &= 360^\circ. \end{aligned} \tag{1}$$

Three common categories of oscillator circuits are relaxation (Figure 5), ring (Figure 6), and LC-based (Figure 7) oscillators. In a relaxation oscillator (a.k.a., multivibrator), the oscillation relies on nonlinear switching that charges and discharges a capacitor with a time constant. The oscillation frequency is tuned by varying this time constant (e.g., through a current source). Relaxation oscillators are usually limited to moderate frequencies. Ring oscillators (Figure 6) are normally designed by cascading an odd number of inverters in a loop. Alternatively, an even number of differential delay cells can be used with an explicit polarity inversion in the feedback connection. A variable delay element (e.g., variable resistor or current source) is used for tuning. The frequency range

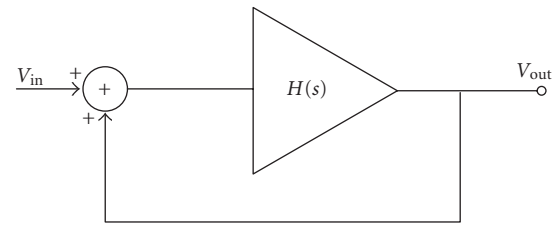


Figure 4: A gain stage with a positive feedback loop.

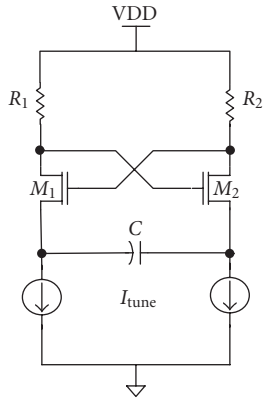


Figure 5: Relaxation oscillator.

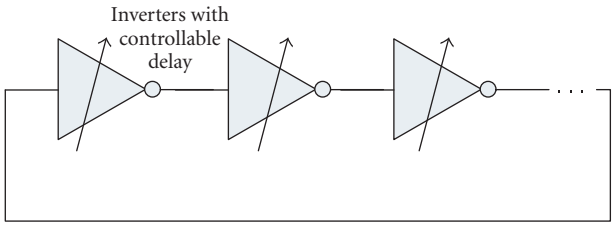


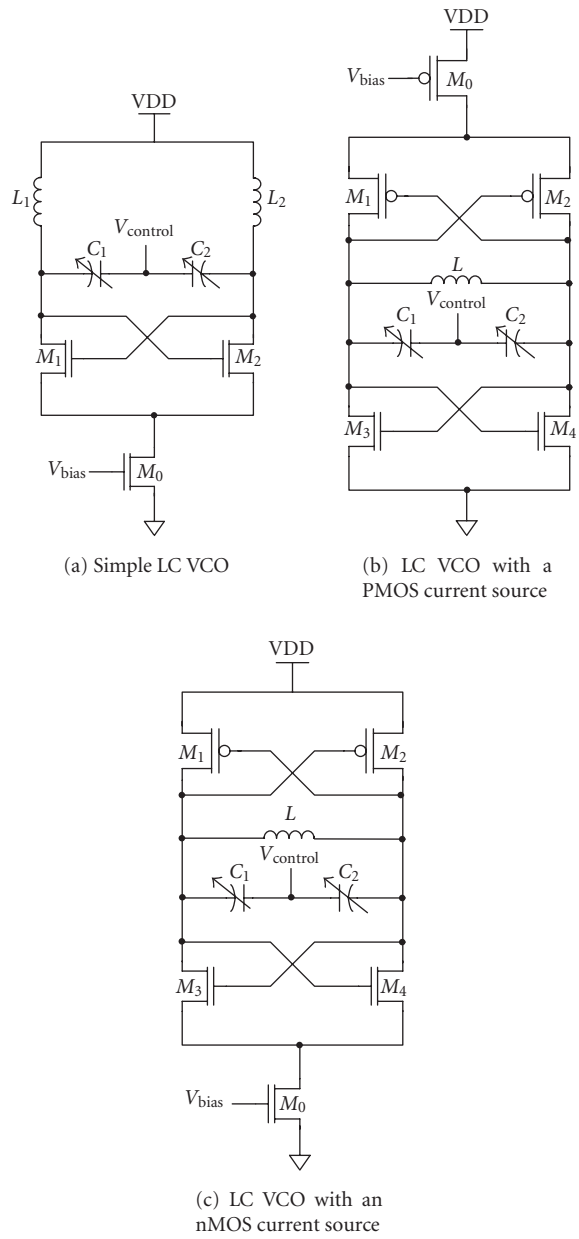
Figure 6: Ring oscillator.

can also be adjusted by digitally adding or removing inverters from the chain (coarse tuning). On the downside, the ring and relaxation oscillators suffer from a poor frequency stability, which manifests itself as higher phase noise.

LC-based oscillators are usually made with a differential pair amplifier, using LC tank as the load. By connecting the outputs to the inputs, the amplifier starts to amplify the noise at its inputs around the resonance frequency of the tank, provided that its open loop gain is greater than one (first of the two Barkhausen conditions). Noise at other frequencies gets filtered out by the LC tank. This filtering characteristic of LC-based oscillators has made them the best in terms of phase-noise performance. Furthermore, compared to the other two oscillator architectures, LC oscillators typically operate more reliably at higher frequencies, provided an LC tank of moderate- to high-quality factor. However, they suffer from their inherently narrower tuning range. Moreover, the integration of LC-based oscillators is more costly due to the large space allocated to on-chip inductors. It should be noted that, as technology advances, achieving higher frequencies becomes more feasible, which in turn requires smaller (less spacious) inductors. Table 2 summarizes the advantages and disadvantages of the three oscillator architectures [3].

3. LC-BASED VCOs

Figure 7 illustrates three forms of typical LC VCO implementations in CMOS. Figure 7(a) represents the simplest implementation, with an nMOS current source and an nMOS differential pair as the gain stage (also referred to as "negative resistance"), which cancels out the loss of the tank. A pair of varactors has been used for frequency tuning. The use of differential signaling is another advantage compared to single-ended VCOs (e.g., ring oscillator in Figure 6). It results in higher oscillation swing in a constantly shrinking supply voltage environment, and less susceptibility to environmental noise due to rejection of the common-mode component of the noise.



(a) Simple LC VCO

(b) LC VCO with a PMOS current source

(c) LC VCO with an nMOS current source

Figure 7: Different versions of LC-based oscillator.

Figures 7(b) and 7(c) represent two other popular implementations of LC VCOs, which result in lower overall phase noise compared to simple LC VCO in Figure 7(a). They have two differential pairs that generate negative transconductance to cancel the tank loss. According to [4], if the

Table 2: Comparison of existing popular oscillator architectures [3].

	LC oscillator	Ring oscillator	Multivibrator
Speed	Technology dependent (0.01–10 s of GHz)		
Phase noise	Good	Poor	
Integration	Poor (inductor and varactor)	Excellent	
Tunability	Narrow/slow	Wide/fast	
Stability	Good	Poor (needs acquisition aid with a PLL)	

oscillation waveform is symmetrical (i.e., equal rise and fall times), the DC component of the phase noise gets eliminated, which is the component that also carries flicker ($1/f$) noise. As a result, the two architectures shown in Figures 7(b) and 7(c) potentially have lower phase noise compared to the architecture in Figure 7(a), which has asymmetrical rise and fall times. The use of nMOS or pMOS current sources creates a level of shielding between substrate (ground) or power supply (VDD), respectively, which subsequently lowers the phase noise due to substrate or supply noise. In technologies where larger supply voltages are available, using voltage regulators is recommended for the VCO to further reduce the oscillator phase noise resulting from substrate and supply noise.

Other than noise components contributed by the oscillator's active elements (as well as supply and substrate), there are other sources of noise resulting from the losses in nonideal passive elements (inductors and varactors), which further degrade the overall phase noise performance of the LC oscillator. To reduce the noise floor due to the lossy inductors, inductors with higher quality factors (Q) need to be used, since they result in lower resistive loss and subsequently lower thermal noise and lower power dissipation. To some extent, however, this is limited by the technology, as the thickness of the metal layers and substrate losses are technology dependent, leaving the designer with fewer degrees of design freedom (e.g., increasing the width of inductor wires to lower the loss would degrade the self-resonance frequency). Various solutions are limited by other criteria, such as silicon-area usage. Although design of high-Q on-chip inductors is a topic of active research, our focus in the following sections remains on varactors as the tuning element of LC VCOs. The design, characterization, and modeling of the varactors significantly affect the overall performance of the LC VCO.

3.1. Varactors

Varactors are a principal component of LC VCOs used for frequency fine tuning. Digitally controlled switched varactors or switched capacitors could also be used for coarse tuning in some designs. Traditionally, reversed-biased pn junction diodes acted as the varactor for LC VCOs (this is still true in the case of bipolar VCOs). However, MOS-based varactors are gaining popularity over the reverse-biased diodes due to wider tuning range and higher Q factor, both of which improve with every new process generation. Higher doping levels in silicon, which in turn result in lower resistive losses and lower phase noise, have driven this improvement. It has become more evident in recent designs in advanced CMOS technologies (e.g., 0.18 μm, 0.13 μm, 90 nm) as implementation of monolithic high-speed VCOs becomes feasible.

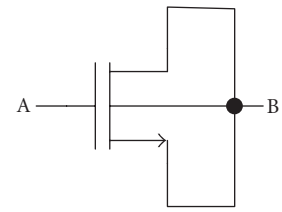


Figure 8: An nMOS transistor configured as a varactor.

An nMOS varactor can have the same structure as an nMOS transistor, with gate as the first terminal and drain, source, and bulk connected together to form the second terminal (Figure 8). MOS varactors operate in four main regions, based on the biasing point (voltage across the varactor terminals): accumulation, depletion, weak inversion, and strong inversion. Accumulation and strong inversion are two regions where most varactors are designed to operate in. Furthermore, a study on accumulation-mode and inversion-mode varactors reveals that LC oscillators based on accumulation-mode varactors demonstrate lower power consumption and lower phase noise at large offset frequencies from the carrier, compared to those based on strong inversion varactors [5].

In most applications, designers would like to ensure that the capacitance of the varactor is a monotonic function of the biasing voltage. For instance, in an LC VCO, it would be desirable, as mentioned earlier, to have the varactor operating predominantly in accumulation mode. However, using a regular nMOS, as in Figure 8, does not warrant this, as the operation region is voltage dependant. It is also worth noting that the C-V curve of a regular nMOS is frequency dependant. Figure 9 illustrates the cross-section of a varactor structure. It may seem similar to an nMOS transistor, however, the n+ regions have been buried in n-well, instead of p-well. This configuration guarantees that the device does not enter the inversion-mode at all; hence the name accumulation-mode MOS (AMOS) varactor.

The C-V characteristics of an MOS varactor can be predicted using 2D/3D numerical simulators. Unfortunately, these simulation tasks require precise knowledge of the underlying doping profiles, which usually are not readily available. An alternative is to perform capacitance measurements.

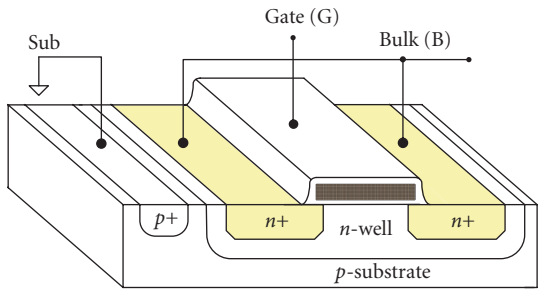


Figure 9: Cross-section of an accumulation-mode MOS (AMOS) varactor.

However, measuring subpico Farad capacitances is difficult and requires a fairly expensive S-parameter RF measurement setup. It is, therefore, very useful to predict the tuning characteristics of LC oscillators using standard foundry-supplied models for MOSFETs.

Recently, a lot of effort has been expended on modeling the C-V characteristics of MOS varactors, partly due to the increasing popularity of CMOS LC VCOs in which such varactors are used. One type of model is based on physically meaningful parameters [6] that describe the characteristics of the device with different equations for different regions of operation. Another model based on the physical parameters of the device is reported in [7]. However, simulating and using these types of models are not simple in SPICE or similar simulators, as they require defining mathematical functions inside the tool. Other models have been developed based on subcircuits utilizing BSIM SPICE models [8]. These models are suitable for simulator implementation within the circuit-design environment and could be easily adopted for future technologies. In the following sections, we introduce a SPICE-like model that takes advantage of already developed foundry models of transistors to create a practical model for accumulation-mode varactors. First we take a closer look at the tuning characteristics of LC VCOs, which further emphasizes the need for a good varactor model.

3.2. VCO design and tuning characteristics

For the following analysis, we used a standard LC VCO circuit with current source isolating the core of the oscillator from the ground, as shown in Figure 7(b). The structure is designed for 5–6 GHz operation. Inductance L is 1.5 nH, and the total equivalent capacitance is in the range of 0.35 pF to 0.65 pF. It may seem that the modeling of the tuning characteristics is a straightforward task, as the oscillation frequency is given by the following well-known formula:

$$f_{\text{osc}} = \frac{1}{2\pi\sqrt{L \cdot C(V)}}, \tag{2}$$

where L is the inductance and $C(V)$ is the equivalent capacitance for a given biasing point. However, a simple test indicates that the modeling process is more involved than it might initially appear. From the measured tuning characteristics (the experimental devices are described later in the paper) the equivalent capacitance can be extracted using (2):

$$C(V) = \frac{1}{4\pi^2 {f_{\text{osc}}}^2 L}. \tag{3}$$

Having determined $C(V)$ values (3), an extracted piecewise linear model of the voltage-dependent capacitance is reconstructed and fed back to SPICE for simulation. The results of this comparison, shown in Figure 10, indicate discrepancies up to 7%.

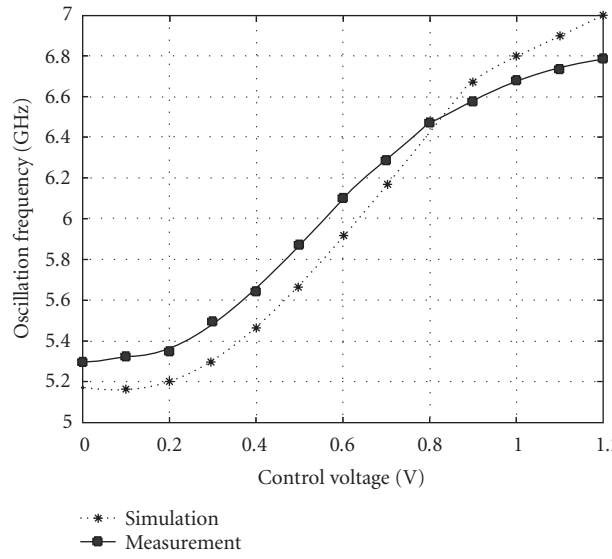


Figure 10: Measured versus modeled VCO tuning characteristics (extracted piecewise linear model).

These discrepancies can be attributed to the effective varactor capacitance. The varactor capacitance gets modulated in time depending on the signal swing of the oscillator output, which in turn changes the effective capacitance of the tank [9–11]. We have used a method similar to that reported in [9] to calculate the effective capacitance. In our calculations, we neglect the current components at harmonics of f_{osc} as they play only a small role in determining the frequency of oscillation. Equation (4) is the revised version of (2), used to obtain the VCO's tuning characteristic:

$$f_{\text{osc}} = \frac{1}{2\pi\sqrt{L \cdot \left(C_{\text{av}}(V) + C_{\text{par}}(V)\right)}}. \tag{4}$$

In this equation, C_{par} is the equivalent parasitic capacitance associated with input of the next buffer, interconnects, and device capacitances of M1–M4, the latter being somewhat voltage dependent. C_{av} is the average capacitance of C_1 and C_2 in series (Figure 7(b)), calculated according to the method described in [9]. The average capacitance is the ratio of the rms value of the varactor's current, $i(t)$, to the rms value of dV/dt, where $V(t)$ is the voltage across the varactor.

As shown in Figure 11, if the voltage swing is small (compared to nonlinearities of the C-V characteristics), then the

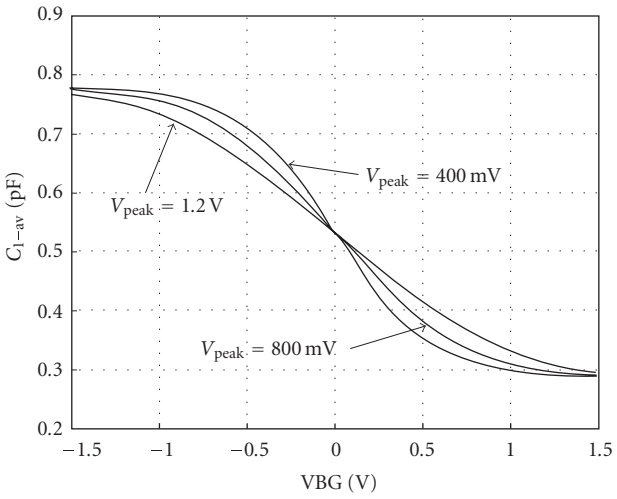


Figure 11: C-V characteristics for three different values of the oscillator voltage swing (V peak).

equivalent large-signal C-V characteristic closely resembles its small-signal counterpart. Here, C_{1-av} refers to average capacitance of C_1 calculated for different output swings. However, for large values of the voltage swing the equivalent characteristics get smoothed or averaged over larger voltage range. As a result, the tuning characteristic becomes dependent on the voltage swing, which in turn is affected by the magnetic and resistive losses in the tank.

Calculation of the equivalent large-signal C-V characteristics depends on the shape of the oscillator's output (rectangular, sinusoidal, etc.). However, at high frequencies the current waveform can be approximated by a sinusoid due to the finite switching time and limited gain [12]. Equation (5) shows the relationship between the swing and tank losses in this LC VCO:

$$V_{\text{Tank}} \approx I_{\text{tail}} \cdot R_{\text{loss}}, \tag{5}$$

where R_{loss} is the equivalent parallel resistance of the tank and I_{tail} is the drain current of the current source transistor (M0 in Figure 7(b)). The effective C-V characteristics (Figure 11) and their associated VCO tuning curves are obtained using (4) and (5) and the method proposed in [9].

3.3. Characterization

Several accumulation-mode varactor test structures are placed on a test chip. Other than varactors, a short structure and an open structure are also placed on the chip to facilitate the de-embedding procedure. For this experiment, two different varactors are characterized. Both varactors are made up of multiples of a unit varactor cell: one has 100 multiples ($m100$ array) and the other has 60 multiples ($m60$ array). The unit varactor cell has a width of 7.9 μm and a gate length of 0.13 μm. To reduce the effect of distributed gate resistance, contacts are used on both sides of the polysilicon gates. Figure 12 illustrates the three test structures: (a) the short structure, (b) the open structure, and (c) the device under test (DUT), that is, varactor array.

Figure 13 shows the micrograph of some of the test structures on the die. These test structures from left to right are: short, open (including dummy varactors), and the varactor array (DUT).

3.3.1. De-embedding technique

Agilent 8510C vector network analyzer (VNA) is used for two-port RF characterization. S-parameters of the varactors, open, and short structures are measured from 100 MHz up to 6 GHz. The varactor voltage is varied from −1.5 V to 1.5 V, with 100 mV resolution.

Different de-embedding techniques are currently used. In [13], a three-step de-embedding technique is used that employs two short structures, an open structure and a thru-structure instead of only short and open structures. A number of de-embedding techniques have been discussed in [14]. We used two-step open/short de-embedding (OSD). Figure 14 shows the equivalent circuit representation of the parasitic series impedance and shunt admittance of interconnects and contact pads, respectively. Z_1 and Z_2 are the interconnection series impedances from pads to the varactor. Y_1 and Y_2 are the equivalent shunt admittances between the signal and ground (pad capacitance, substrate capacitance, and resistance). We used signal-ground (SG or GS) probes. However, GSG probes are preferred, as they result in balanced electrical characteristics.

Figure 15 illustrates a different lumped model for OSD, as presented in [14]. Here Z_1' and Z_2' are the impedances between the probe tips and the pads on the CMOS chip as the probe calibration is performed on an impedance-standard-substrate (ISS). The ISS uses gold metallization instead of typical aluminum traces, and has a lower resistance.

Both approaches to de-embedding shown in Figures 14 and 15 were carefully considered. However, we concluded that in our setup, interconnection impedances are dominant. Based on the parasitic lumped model of Figure 14, Y_1 and Y_2 are extracted from the following equations:

$$\begin{aligned} Y_1 &= Y_{11,\text{open}}, \\ Y_2 &= Y_{22,\text{open}}. \end{aligned} \tag{6}$$

Z_1 and Z_2 can then be calculated using the following equations:

$$\begin{aligned} Z_1 &= \frac{1}{Y_{11,\text{short}} - Y_1}, \\ Z_2 &= \frac{1}{Y_{22,\text{short}} - Y_2}. \end{aligned} \tag{7}$$

$Y_{ii,\text{open}}$ and $Y_{ii,\text{short}}$ $(i = 1, 2)$ are the input or output admittances of the open and short structures, respectively.

3.3.2. Parameter extraction procedure

Figure 16 shows the circuit model of the accumulation-mode varactor [6]. In this figure, C_S represents the main variable

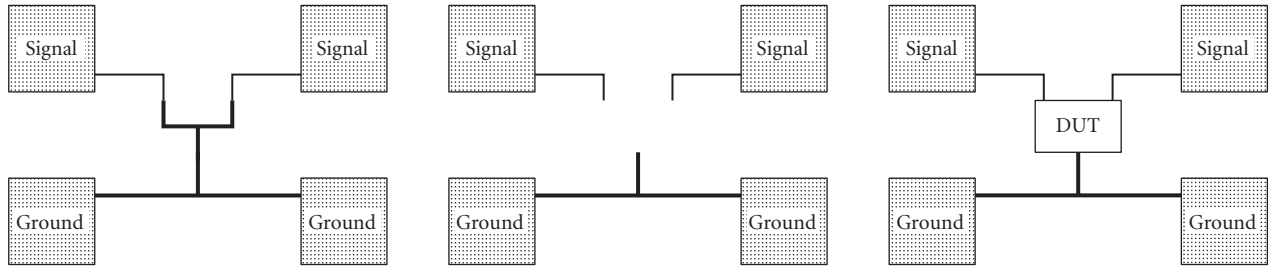


Figure 12: Top-view of the test structures: (a) short, (b) open, and (c) DUT (varactor array).

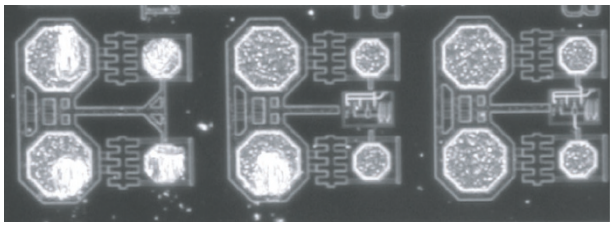


Figure 13: Micrograph of the test structures in 0.13 μm CMOS, from left to right: short, open, and the varactor array (DUT).

capacitance associated with the series capacitance of the gate oxide and the depletion region under the gate. C_f models the fringing capacitance related to the sidewalls of the gate. L_g is the inductance of the poly gate. R_s is the poly gate and channel resistance (the latter is voltage dependent), and R_{nwell} is the resistance of the n-well. C_{dep} is the depletion capacitance associated with the reversed biased p-sub/n-well diode. R_{sub} and C_{sub} are the substrate parasitics. R_{sd} is the resistance of the $n+$ regions (bulk electrode).

In order to verify the model shown in Figure 16, we need to characterize the de-embedded on-chip varactors ($m60$ and $m100$ arrays). Figure 17 shows the simplified form of Figure 16. In this figure, we have neglected R_{sd} (Z_c), as the impedance of the highly doped $n+$ regions is very small (less than 1 Ω in these test structures).

Using the simplified circuit shown in Figure 17, we extract Z_a and Z_b from the following two equations:

$$\begin{aligned} Z_a &= \frac{1}{Y_{11}} = Z_{11} - Z_{12}, \\ Z_b &= Z_{12} = Z_{21} = Z_{22}, \end{aligned} \tag{8}$$

where Z_{11}, Z_{12}, Z_{21}, and Z_{22} are the equivalent Z-parameters of the two-port varactor (Figure 17) and Y_{11} is the input admittance (gate-side) of the equivalent Y-parameters.

Z_a can be written as (neglecting C_f):

$$Z_a = R_S + \frac{1}{j\omega C_S} + j\omega L_g. \tag{9}$$

Using (9) and employing numerical methods, we extracted the elements of Z_a for both varactors ($m60$ and $m100$ arrays). R_s is equal to real part of Z_a (i.e., $\text{Re}(Z_a)$), and C_s is calculated from

$$C_S = \frac{1}{\omega^2 L_g - \omega \cdot \text{Im}\,(Z_a)}, \tag{10}$$

where L_g is also calculated at higher frequencies (e.g., 6 GHz) using

$$L_g = \frac{1 + \omega C_{\text{S-Low}} \cdot \text{Im}\,(Z_a)}{\omega^2 C_{\text{S-Low}}}, \tag{11}$$

$C_{\text{S-Low}}$ is the capacitance at lower frequencies (e.g., 100 MHz), where $\omega^2 L_g$ is insignificant and can be removed from (10).

The quality factor (Q) of the varactor, which is the ratio of the stored energy to the dissipated energy (resistive loss) in the varactor, can also be approximated by

$$Q = \left| \frac{\text{Im}\,(Z_a)}{\text{Re}\,(Z_a)} \right|. \tag{12}$$

The substrate effect (Z_b) is calculated using similar methods described for Z_a.

3.4. Varactor modeling

As indicated earlier, modeling of tuning characteristics using (2) is fairly complicated. Not only do the varactor C-V characteristics have to be measured, but also the losses of the tank have to be determined to properly find the oscillation swing and hence the effective tank capacitance. An alternative approach would be to use the equivalent circuit representation of the varactor created from foundry-supplied transistor models and SPICE simulation to predict the tuning range. If a varactor is operating in the strong inversion mode, an nMOS transistor with tied source and drain can be used as a primitive model, since the varactor structure is the same as that of an MOS transistor. However, varactors that are working in the accumulation mode are usually laid out as shown in Figure 9. This structure inhibits the formation of the inversion layer. Wider tuning range and lower parasitic resistance are other advantages of this implementation [5]. On the other hand, the use of a plain transistor for modeling this varactor is not viable because the device does not resemble a transistor.

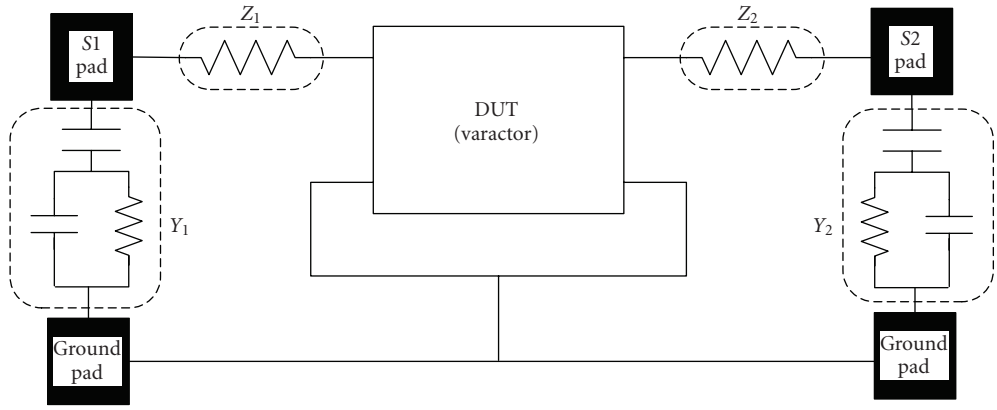


Figure 14: Equivalent lumped model of the varactor (DUT) with associated parasitics (open/short de-embedding).

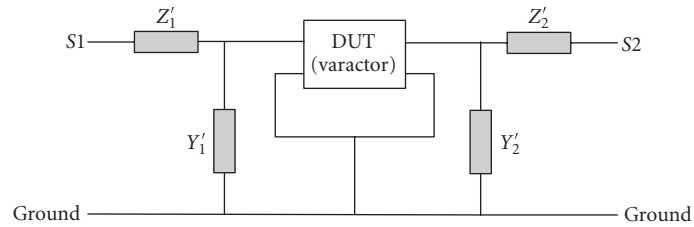


Figure 15: Alternative lumped model for open/short de-embedding (OSD).

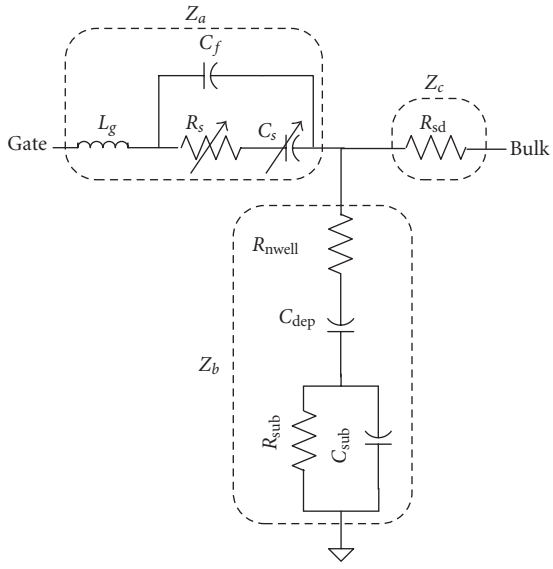


Figure 16: Equivalent lumped model of the integrated varactor.

Figure 16 illustrates the model of this varactor constructed with passive circuit elements, and based on physical parameters [6]. As mentioned above, this model requires the implementation of nonstraightforward equations (e.g., hyperbolic tangent) in the circuit-design environment and may involve other approximations as well. Moreover, the model cannot be easily scaled to future technologies.

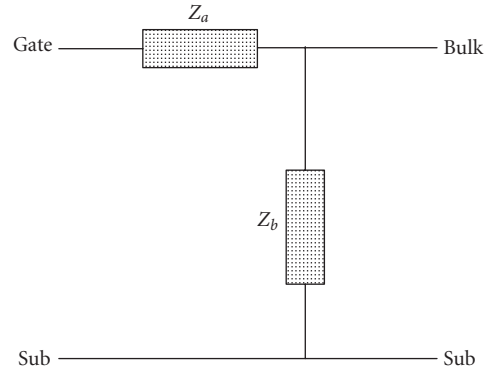


Figure 17: Simplified circuit of the two-port varactor in Figure 16.

We have considered a number of different equivalent models reported in the literature and developed a new model that closely approximates the measured characteristics of the VCO [15]. This improved model is shown in Figure 18, and is a modified version of that proposed in [8]. The overlap capacitance C_{ov}, a voltage source V_{offset}, and a voltage source (dashed lines) between the bulk and drain/source have been added in the new model.

To model the varactor capacitance, the equivalent circuit contains a voltage source V_{offset}, a capacitor C_{ov}, and a pMOS with its source and drain connected to the ground with a high impedance (e.g., 1 GΩ resistors) to resemble floating (nonexisting) source and drain. The open circuit for the

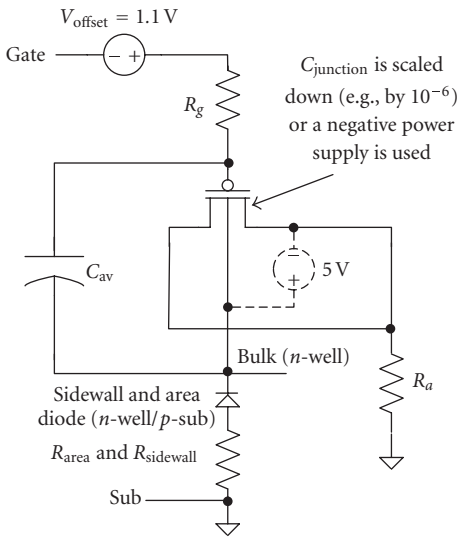


Figure 18: SPICE model developed for the varactor.

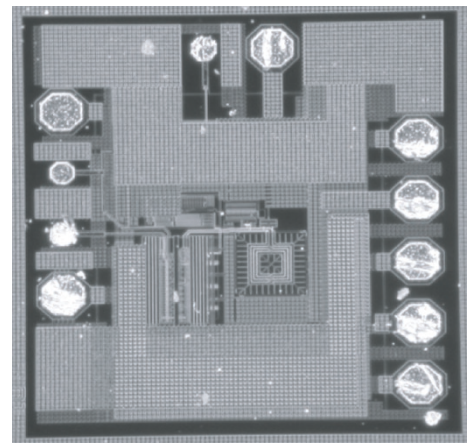


Figure 19: Micrograph of a VCO test structure in 0.13 μm CMOS.

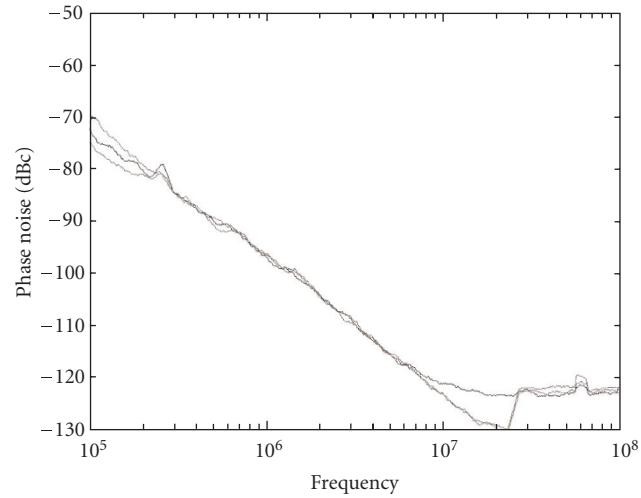


Figure 20: Measured phase noise of the VCO with pMOS tail current (Figure 7(b)) at three different supply voltages (1.2 V, and 1.2 V ± 5%).

source/drain terminal is required to eliminate the inversion layer capacitance present in the channel of the pMOS but absent in the varactor structure (see Figure 9). As a result, the gate to n-well (bulk) capacitance of pMOS represents the varactor capacitance properly with an additional channel length correction for LDD (lightly doped source/drain) regions. Unfortunately in this configuration, the gate-source and gate-drain overlap components of the varactor get neglected; as a result, they have to be added back by using the fixed capacitor, $C_{ov} \cdot V_{offset}$ represents a difference of the metal-semiconductor work function ϕ_{MS}, as the pMOS has p+ poly gate doping while the varactor has n+ poly doping due to their different source/drain diffusion. As doping levels in the polysilicon layer are typically close to degeneration, the V_{offset} is close to silicon bandgap ($E_g(T)/q$), which is about 1.1 V at room temperature. Finally, the junction capacitance of the pMOS transistor has to be scaled down. This can be done either by changing the scaling factor inside the SPICE model or adding a negative power supply between source/drain and the bulk (e.g., −5 V) to enlarge the depletion area and reduce the junction capacitance.

4. EXPERIMENTAL RESULTS

Three different VCO structures have been fabricated in a standard 0.13 μm CMOS process with a 1.2 V power supply. No special mixed-signal process options have been used. The micrograph of the chip is shown in Figure 19. Varactors are implemented as n+ accumulation-mode MOS capacitors with no additional mask required. Thus, the obtained designs are portable to various CMOS processes of different foundries.

The three implementations have similar architectures as those depicted in Figures 7(b) and 7(c), but with different varactor values. The tail current in all three versions is 1.5 mA; hence the DC power consumption is 1.8 mW, excluding output driver and biasing circuits. The one that incorporates an nMOS tail current source (Figure 7(c)) exhibits higher sensitivity to the power supply noise, while the one with a pMOS tail current source (Figure 7(b)) has the best power-supply-rejection ratio (PSRR), due to the extra isolation from the power supply by the current source.

In addition to the three VCO circuits, a biasing circuit and an output driver stage were added to drive external 50 Ω load. Individual varactor and inductor test structures were also included for S-parameter measurements. Open and short de-embedding structures were added for proper extraction of the equivalent circuit, as explained earlier in Section 3.3.1.

The phase noise of all three VCOs was measured using a spectrum analyzer with a phase noise module. Figure 20 compares the phase noise of the VCO with the pMOS tail current shown in Figure 7(b), for three different supply voltages (1.2 V, and 1.2 V ± 5%) at the nominal temperature with the control voltage set to the mid-point

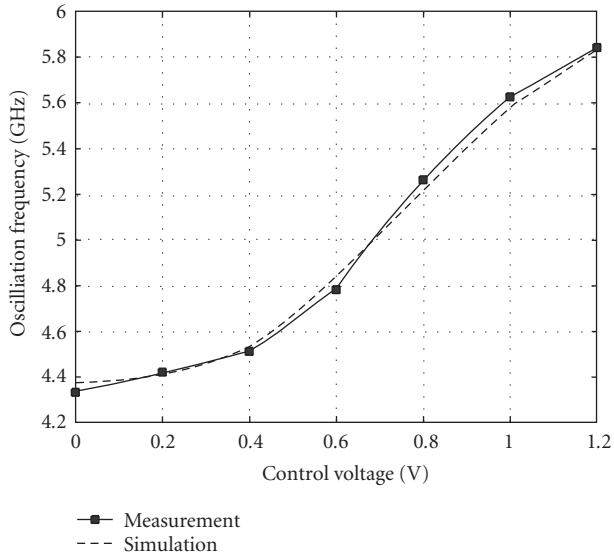


FIGURE 21: Measured versus modeled tuning characteristics (new SPICE model).

(600 mV). The phase noise at 1 MHz offset from the carrier is −95.8/−95.5/−95.5 dBc/Hz, respectively.

The tuning characteristics were simulated using the varactor model described in Section 3.4. Excellent agreement between the model and the measurement was obtained, as shown in Figure 21. The results in Figure 21 are for a VCO test structure with an increased number of varactor fingers (varactor with 100 fingers) and hence lower center frequency compared to the results shown in Figure 10.

5. CONCLUSION

VCOs are among the critical building blocks of wireless RF transceivers since their performance and phase noise potentially affects the overall transceiver performance. Among various VCO architectures, LC VCOs have superior phase noise performance and therefore are extensively used in RF transceivers. Varactors are the main tuning component of LC VCOs and play an important role in the phase noise performance and tuning capability of these types of VCOs. A new model for CMOS accumulation—mode varactors is presented. The model is used to predict the tuning curve of the LC VCOs. The shape of the tuning curve and the effective varactor capacitance were shown to depend on the losses of the tank and the magnitude of the tail current. The model is SPICE-based and has been verified experimentally in a standard 0.13 μm CMOS process with different VCO structures.

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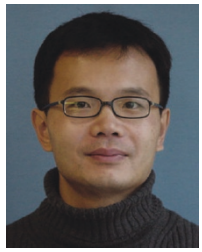

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