

High performance, low power 200 Gb/s 4:1 MUX with TGL in 45 nm technology

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Abstract The various analysis are established more on arithmetic circuits particularly with MUX design, this paper also explores with multiplexer to optimize the power. The CMOS transmission gate logic (TGL) is used to design a new 4:1 MUX with reduction in circuit complexity compared to conventional CMOS based multiplexer design. Based on TGL, it removes the degraded output, the NMOS and PMOS are combined together for strong output level with the gain in area, which is a central result of proposed MUX. The designed circuit is realized in 45 nm technology, with the power dissipation of 1.887 nW from a 0.7 V supply voltage. The MUX can operate well up to 200 Gb/s.

Keywords Multiplexers · CMOS · Low power · Transmission gate · Leakage current

Introduction

The low power consumption is one of the most important issues in the system SOC design, different techniques and technologies for low-power designs in high-speed interface applications are developed and also applied in the practical design projects (Hattori 2007). The various approaches have been proposed to reduce power consumption of MUX trees. Some of the papers contract it at the algorithm level (Narayanan et al. 1997; Chang et al. 2007; Kim et al. 2001) and some at the circuit level (Sebastian 2000; Douseki and

Ohmori 1988). Multiplexers are key components in CMOS memory elements and data manipulation structures. The increasing requirement for low-power very large scale (VLSI) can assigned at different design levels, such as the architectural, circuit, layout, and the process technology level (Chandrakasan and Brodersen 1995). At the circuit design level, the major part of potential for power stake exists by means of proper choice of a logic style for implementing combinational circuits. Exploration of low-power logic styles reported in the research so far, however, have mainly concentrated on particular logic cell, namely multiplexers, used in arithmetic circuits. At higher frequency than the frequency above, the CMOS logic can operate continuing with low power consumption.

In addition to this, it also reduces the layout area. Multiplexer abbreviated as MUX is the heart of any arithmetic circuit. MUX are a common building block for data paths and data-switching structures, and are used effectively in a number of applications including processors (Metzgen 2004), processor buses, network switches, and DSPs with resource sharing.

The battery essential for long battery back-up time for the miniature devices is a basic concern which always increases the presumption of the users for more and more backup time. Hence the power consumed by multiplexers is a key factor to control. In reconfigurable architectures such as FPGAs, the area and power of MUX and interconnect have by far balance the area and power of functional units and registers. For example, in the Altera Benchmark set of 120 real customer designs (FPGA Performance Benchmarking Methodology), it has been estimated that MUX normally account for over 25 % of the area of an FPGA design.

In the past decade, CML structure based multiplexer circuits is used in most international papers for high-speed

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systems in CMOS process (Kehrer et al. 2003; Chien and Lu 2006; Yazdi and Green 2009). In this paper, a 4:1 MUX using CMOS transmission gate logic (TGL) has been designed with the low power consumption in 45 nm CMOS process.

For high-speed MUX with a data rate far beyond 10 Gb/s, the resolution has been made in the design of high-speed MUX and CMOS technology. (Kanda et al. 2005; Kehrer et al. 2002).

Multiplexer

It quite often happens, in the design of large-scale digital systems, that a single line is required to carry two or more different digital signals. Of course, only one signal at a time can be placed on the one line. What is required is a device that will allow us to select, at different instants, the signal we wish to place on this common line. Such a circuit is referred to as Multiplexer. The graphical symbol and truth table of 4:1 MUX are shown in Fig. 1a, b, respectively. A multiplexer performs the function of selecting the input on any one of ‘n’ input lines and feeding this input to one output line.

Multiplexers are used as one method of reducing the number of integrated circuit packages required by a particular circuit design. This in turn reduces the cost of the system.

$$\text{Output} = X_0 \cdot \bar{C}_0 \cdot \bar{C}_1 + X_1 \cdot \bar{C}_0 \cdot C_1 + X_2 \cdot C_0 \cdot \bar{C}_1 + X_3 \cdot C_0 \cdot C_1 \tag{1}$$

Assume that we have four lines, X0, X1, X2 and X3, which are to be multiplexed on a single line, Output (M). The four input lines are also known as the Data Inputs. Since there are four inputs, we will need two additional inputs to multiplexer, known as the Select Inputs, to select which of the X inputs is to appear at the output, called as

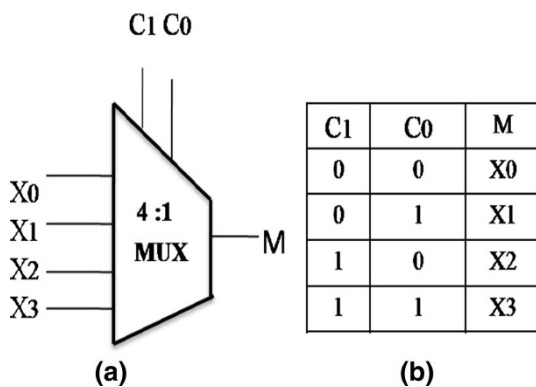


Fig. 1 4:1 MUX: graphical symbol (a), truth table (b)

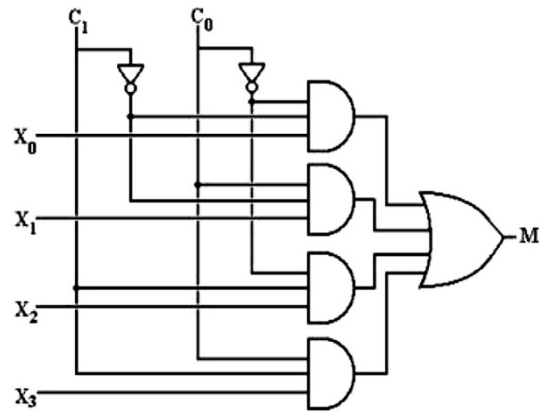


Fig. 2 Gate implementation of a 4:1 Multiplexer

select lines C0 and C1. The gate implementation of a 4:1 MUX is shown in Fig. 2. Equation 1 is given for 4:1 MUX.

CMOS transmission gate logic based 4:1 MUX

CMOS transmission gate logic

This section describes the purpose and basic operation of a transmission gate. The transmission gate can be used to quickly isolate multiple signals with a minimal investment in board area and with a negligible degradation in the characteristics of those critical signals. A transmission gate is defined as an electronic element that will selectively block or pass a signal level from the input to the output. The solid-state-switch is comprised of parallel connection of a PMOS transistor and NMOS transistor. The control gates are biased in a complementary manner so that both transistors are either on or off.

When the voltage on node A is a Logic 1, the complementary Logic 0 is applied to node active-low A, allowing both transistors to conduct and pass the signal at IN to OUT. When the voltage on node active-low A is a Logic 0, the complementary Logic 1 is applied to node A, turning both transistors off and forcing a high-impedance condition on both the IN and OUT nodes. The schematic diagram (Fig. 3) includes the arbitrary labels for IN and OUT, as the circuit will operate in an identical manner if those labels were reversed. This design provides true bidirectional connectivity without degradation of the input signal. The transmission gate graphical symbol and truth table are shown in Fig. 3.

General MUX design concept

This circuit is transistor level architecture of 4:1 MUX which consists of 44 transistors.

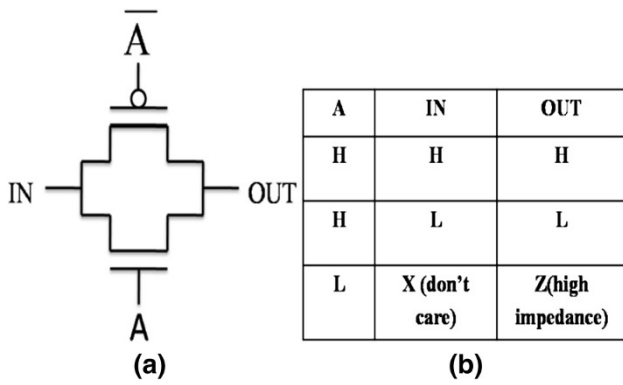


Fig. 3 Transmission gate: graphical symbol (a), truth table (b)

Due to excess of transistors, the required functionality will consume more power with abundant area. But as the technology is reducing, the circuit should perform with minimum power consumption. As a result, this design is not considered more advantageous for lower technology. So, this paper concentrated on transmission gate based 4:1 MUX design. This comprised of 12 transistors only. The power consumption is reduced with minimum area in proposed design. The general transistor level representation of a 4:1 Multiplexer is shown in Fig. 4.

Transmission gate logic based 4:1 MUX

This design is the transmission gate type of MUX structure implemented with very minimum transistors compared to

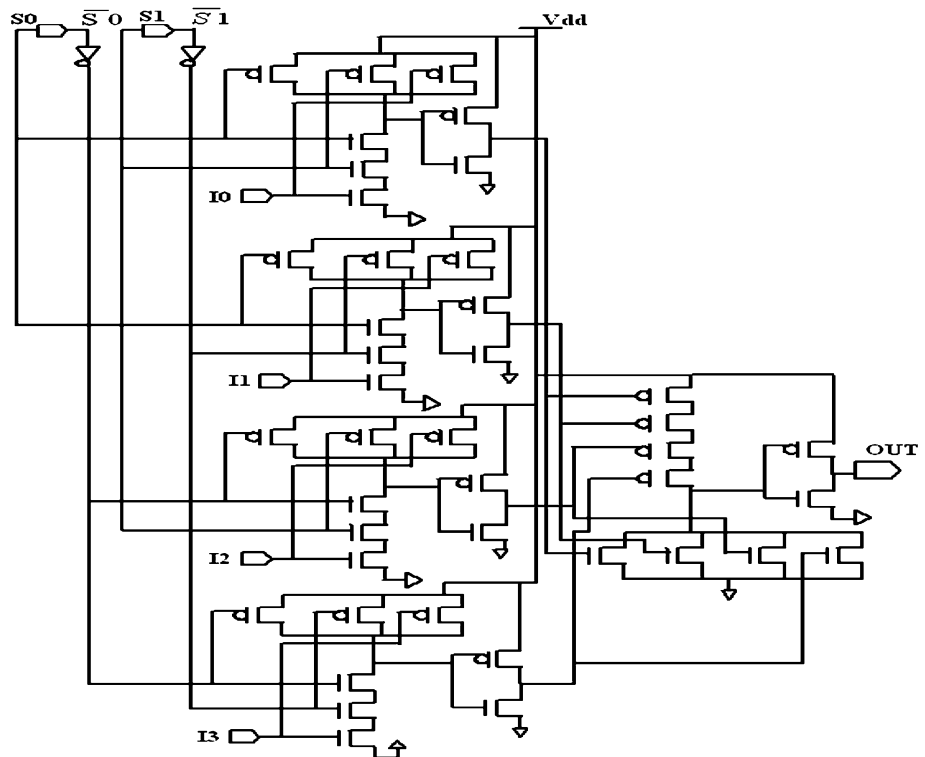
the conventional CMOS based design. The back-to-back connected PMOS and NMOS arrangement acts as a switch is so called transmission gate. NMOS devices pass a strong 0 but a weak 1, while PMOS pass a strong 1 but a weak 0. The transmission gate combines the best of both the properties by placing NMOS in parallel with the PMOS device. Four transmission gates are connected as in Fig. 5 to form a MUX structure.

Each transmission gate acts as an AND switch to replace the AND logic gate which is used in a conventional gate design of MUX. Hence, the device count is reduced. The transmission gate based 4:1 MUX is shown in Fig. 5.

Layout of transmission gate based 4:1 MUX

The advances in the CMOS processes are generally complex and somewhat inhibit the visualization of all the mask levels that are used in the actual fabrication process. Nevertheless, the design process can be abstracted to a manageable number of conceptual layout levels that represent the physical features observed in the final silicon wafer. An advantage of the new MUX design is the remarkable gain in terms of transistors count. To the best of our knowledge, no 4:1 MUX has been realized with so few devices. Hence, the gain in area is a central result for the proposed MUX. The layout of transmission gate based 4:1 MUX is shown in Fig. 6.

Fig. 4 Transistor level representation of a 4:1 Multiplexer



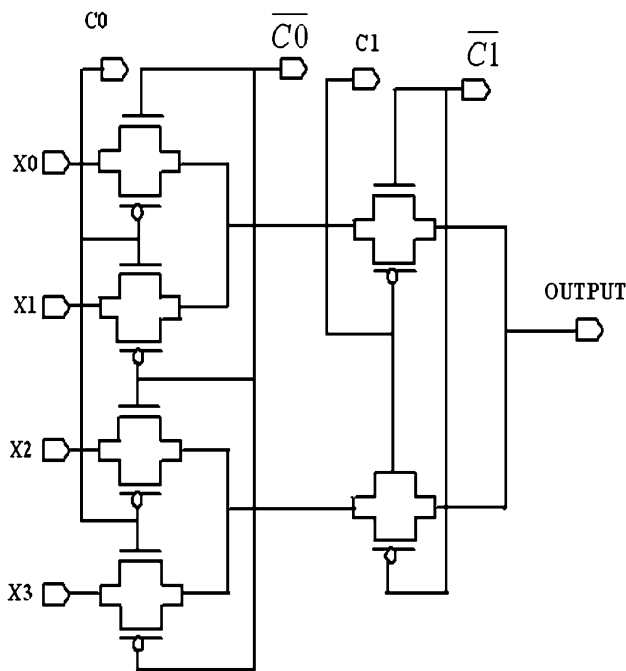


Fig. 5 Transmission gate based 4:1 MUX

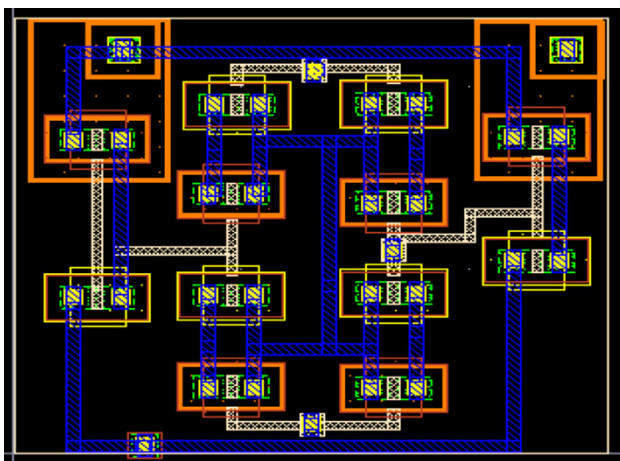


Fig. 6 Layout of transmission gate based 4:1 MUX

Simulation results

The Simulation result is measured by Cadence Virtuoso tool. The simulation result is summarized in Table 1 (Sun and Feng 2010).

MUX output pattern

The simulation waveform of proposed 4:1 MUX is shown in Fig. 7. The resultant waveform attains a single output during the power supply of 0.7 v, although the rise and fall

Table 1 Performance comparison of 4:1 Mux

Parameters	Conventional	Proposed
Function	4:1 MUX	4:1 MUX
Technology	0.18 μm	45 nm
Supply voltage	1.8 V	0.7 v
Output bit rate	10 Gb/s	200 Gb/s
Current consumption	29.6 mA	2.237 nA
Power consumption	53.3 mW	1.887 nW
Chip size	$0.575 \times 0.475 \text{ mm}^2$	$2.600 \times 2.375 \mu\text{m}^2$

time of simulation is 100 fs. The output pattern is shown in Fig. 7.

Power and current consumption

Digital CMOS circuit may have three major sources of power dissipation namely dynamic, short and leakage power. Hence, the total power consumed by every MUX style can be evaluated using the Eq. 2.

$$P_{\text{tot}} = P_{\text{dyn}} + P_{\text{sc}} + P_{\text{leak}} \quad (2)$$

$$= CL \cdot V_{\text{dd}} \cdot V \cdot f_{\text{clk}} + I_{\text{sc}} \cdot V_{\text{dd}} + I_{\text{leak}} \cdot V_{\text{dd}}$$

Thus, for low-power design, the important task is to minimize $CL \cdot V_{\text{dd}} \cdot V \cdot f_{\text{clk}}$ while retaining required functionality. The first term P_{dyn} represents the switching component of power, the next component P_{sc} is the short circuit power and P_{leak} is the leakage power. Where, CL is the loading capacitance, f_{clk} is the clock frequency which is actually the probability at which Logic 0 to 1 transition occurs (the activity factor). V_{dd} is the supply voltage, V is the output voltage swing which is equal to V_{dd} ; but, in some logic circuits, such as proposed transmission logic implementations, the voltage swing on some internal nodes may be slightly less (Yazdi and Green 2009).

The current I_{sc} in the second term is due to the direct path short circuit current which arises when both the NMOS and PMOS transistors are simultaneously active, conducting current directly from supply to ground (Rabaey et al. 2008). Finally, leakage current I_{leak} , which can arise from substrate injection and sub-threshold effects, is primarily determined by fabrication technology considerations.

The power and current consumption of proposed MUX are shown in Figs. 8, 9, respectively.

Eye diagram

Eye diagram of the output signal at a data rate of 200 Gb/s. The measured eye diagram is shown in Fig. 10.

Fig. 7 Simulation output pattern

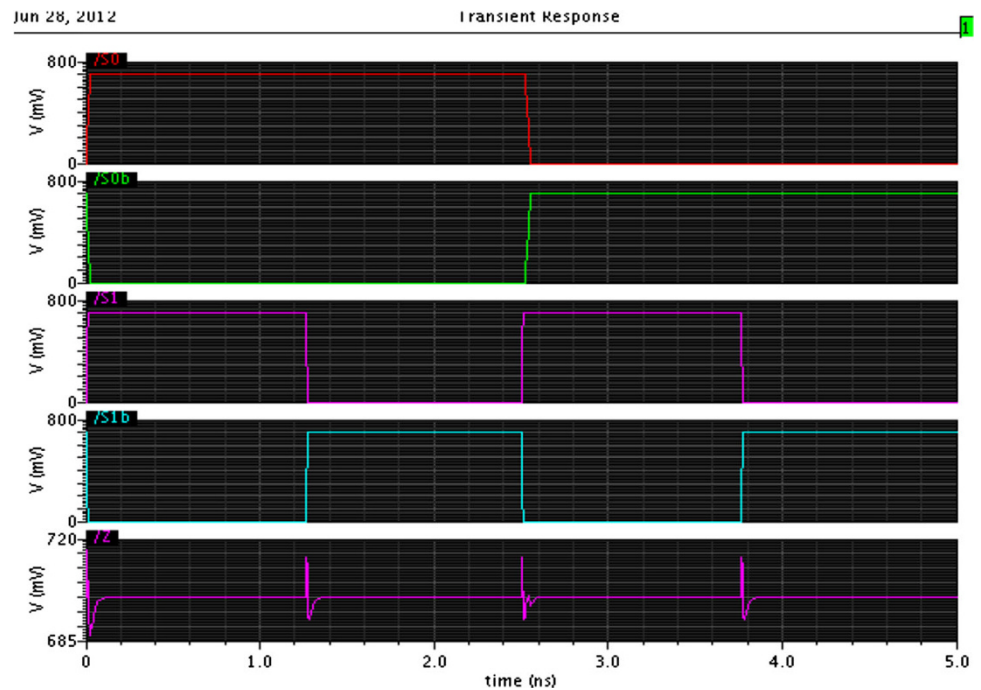
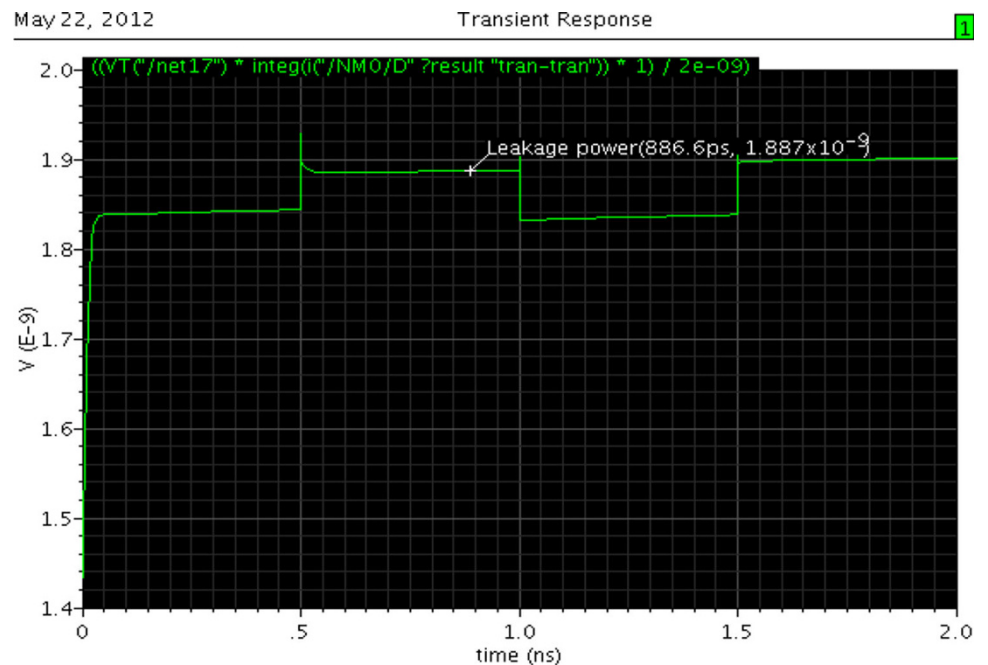


Fig. 8 Power consumption of proposed MUX



Conclusion

To remove degraded output, the NMOS and PMOS are combined together for strong output level. The CMOS TGL is used to design a new 4:1 MUX. The designed circuit is realized in 45 nm technology, with the power consumption of 1.887 nW from a 0.7 V supply voltage under 27 °C. The

leakage current is also reduced to 2.237 nA from 29.6 mA. The rise and fall time for the simulation is 100 fs. The MUX can operate well up to 200 Gb/s. Transistors are reduced to great extent, so that the overall area is minimized. The innovation ranges of many process and environment parameters will increase profoundly, results in strength of circuit which is becoming a key aspect in deep-submicron

Fig. 9 Current consumption of proposed MUX

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Transient Response

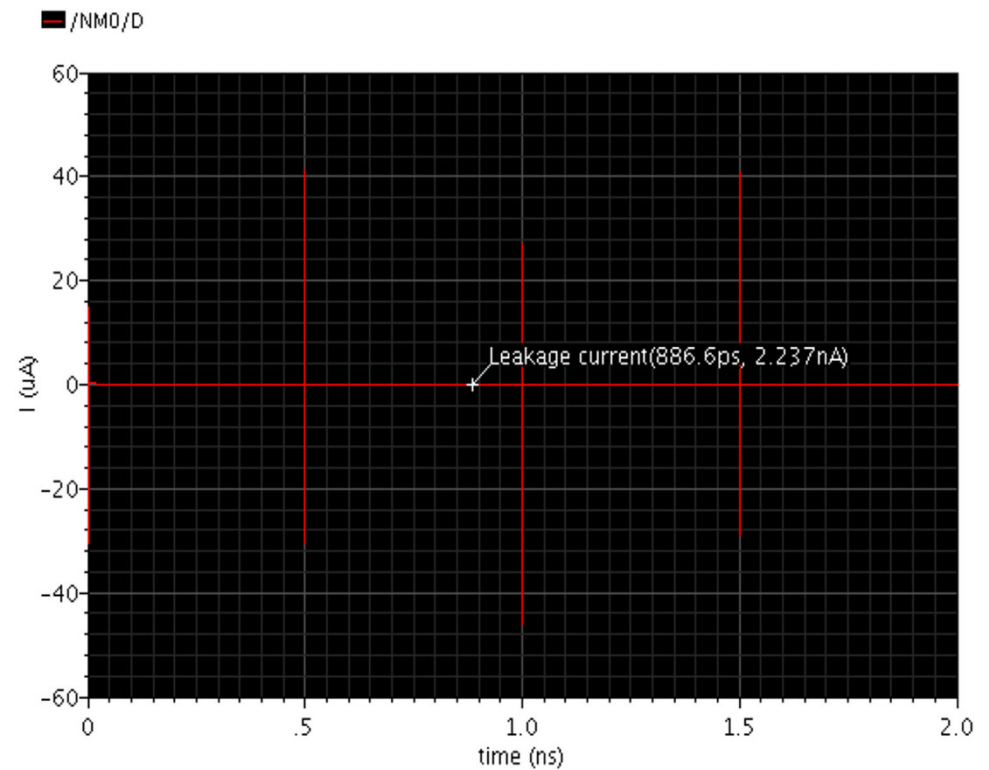
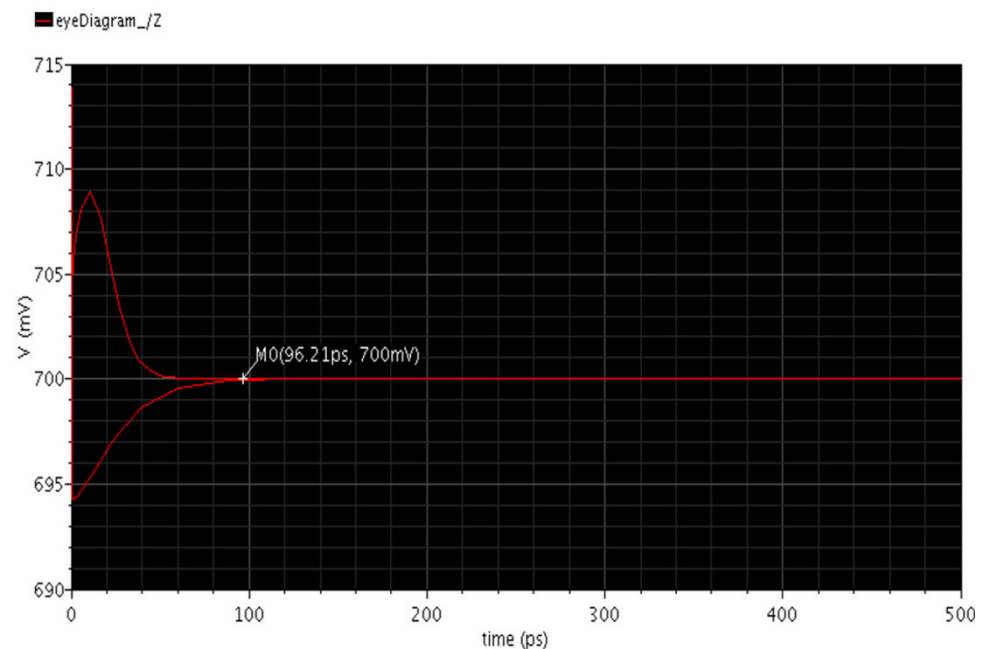


Fig. 10 Measured eye diagrams of MUX output at 200 Gb/s

May 15, 2012



VLSI (Meindl 1996). In the future, the complementary CMOS the logic style of choice for low-power, low-voltage implementation of arbitrary combinational circuits and for

design automation makes ease of use (Rabaey 1996). The TGL results to be the efficient design styles for MUX design (Vivijayakumar and Karthikeyan 2010).

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