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Influence of post-annealing on the off current of MoS_2 field-effect transistors

Seok Daniel Namgung[1,2], Suk Yang[1,2], Kyung Park[2], Ah-Jin Cho[1,2], Hojoong Kim[1,2] and Jang-Yeon Kwon[1,2*]

Abstract

Two-dimensional materials have recently been spotlighted, due to their unique properties in comparison with conventional bulk and thin-film materials. Among those materials, MoS_2 is one of the promising candidates for the active layer of electronic devices because it shows high electron mobility and pristine band gap. In this paper, we focus on the evolution of the electrical property of the MoS_2 field-effect transistor (FET) as a function of post-annealing temperature. The results indicate that the off current drastically decreased at 200°C and increased at 400°C while other factors, such as the mobility and threshold voltage, show little variation. We consider that the decreasing off current comes from the rearrangement of the MoS_2 film and the elimination of the surface residue. Then, the increasing off current was caused by the change of the material's composition and adsorption of H_2O and O_2.

Keywords: Molybdenum disulfide; MoS_2; Field-effect transistors; On/off current ratio; Field-effect mobility

Background

Two-dimensional (2D) materials, such as graphene and transition metal dichalcogenides (MoS_2, $MoSe_2$, WS_2, etc.), are widely used recently for fabricating next-generation nanoelectronics [1-10]. This is because of the high electron mobility of 2D materials, compared with the original bulk material. Typically, graphene shows over 5,000 cm^2/Vs of electron mobility [11], and this feature is valuable for applications such as sensors [12] and photovoltaic cells [13]. However, graphene has a fundamental disadvantage for electronic devices, which is the lack of an intrinsic band gap. This has resulted in several reports of insufficient on/off current ratio of field-effect transistors (FETs) [14-17].

Though engineering a band gap of graphene can be an answer for this technical issue, it increases the number of fabrication steps [18,19] and reduces the electron mobility of graphene [20]. As an alternative, MoS_2 has an intrinsic band gap, which leads to reduced off current. For example, MoS_2 FETs have in general recorded an on/off current ratio of $10^5 \sim 10^{10}$ [21-28], and some MoS_2 FETs with high-k dielectrics have recorded an electron mobility of 200 cm^2/Vs, which is higher than that of band gap-engineered graphene [21].

Many reports have announced that the annealing process is dispensable for improving the electrical property of various FETs using original IV semiconductors [29], oxide semiconductors [30,31], layered semiconductors [32-34], etc. In the case of 4H-SiC included in the original IV, the annealing process created a passivation layer at the interface, and device parameters were improved, such as the electron mobility and subthreshold swing (SS). In the case of InGaZnO included in oxide semiconductors, the annealing process rearranged defects, and all the device parameters improved, such as V_{th}, SS, mobility, hysteresis, and the on/off current ratio. For graphene included in a layered material, the annealing process eliminated the resist residue on the surface and increased conductance.

For MoS_2, a few results have been reported from the viewpoint of the post-annealing process [21,23,26]. One paper showed variation in the optical property, by observing the change of the photoluminescence (PL) peak of single-layer MoS_2 with respect to post-annealing [35]. Although it did not evaluate the electrical property of FETs, it reported that the annealing process induced structural rearrangement, and this could also

* Correspondence: jangyeon@yonsei.ac.kr
[1]School of Integrated Technology, Yonsei University, Songdo-dong, Incheon 406-840, Republic of Korea
[2]Yonsei Institute of Convergence Technology, Incheon 406-840, Republic of Korea

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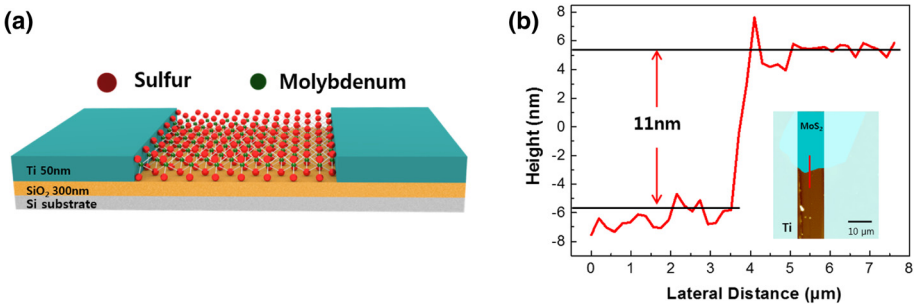

Figure 1 Schematic representation of MoS_2 FET and AFM image. (a) Schematic representation of MoS_2 FET with highly doped silicon as the back gate and **(b)** atomic force microscopy (AFM) height profile of multilayer MoS_2 that has a thickness of 11 nm. The inset is the corresponding AFM image.

affect the electrical properties of MoS_2. Another paper investigated the influence of vacuum annealing on MoS_2 FET during measurement of the electrical property [22]. It announced a drastic improvement of electrical performance by annealing, especially in the conductance of the device. However, it focused on the electrical characteristics caused by movement of carriers at elevated temperature, which consequently present the thermally activated characteristics of MoS_2 FET. Here, we summarize the evolution of the electrical performance of MoS_2 FET at room temperature, which is the conventional operating temperature, with various post-annealing temperatures.

Methods

MoS_2 flakes were prepared using a scotch-tape micromechanical cleavage technique, from bulk MoS_2 crystal (429ML-AB, SPI Supplies, Inc., West Chester, PA, USA), and were transferred to highly doped silicon substrates covered with 300-nm-thick SiO_2. Source and drain (S/D) were patterned by photolithography, and 50-nm-thick Ti was deposited by an e-beam evaporator. Then, a conventional lift-off process was accomplished for the patterning of the S/D electrode. The fabricated MoS_2 FET was annealed in a nitrogen environment for 2 h at various temperatures. The electrical characteristic was measured under atmospheric pressure at room temperature. Furthermore, the thicknesses of the MoS_2 flakes were measured using atomic force microscopy (AFM; XE-100, Park Systems, Suwon, South Korea).

Results and discussion

Figure 1a is a schematic diagram of the MoS_2 FET, and Figure 1b is an AFM profile that corresponds to the red line of the MoS_2 image from the inset. The thickness of the MoS_2 channel measured by AFM was 11 nm. While there has been controversy over whether using a single-layer MoS_2 channel is a requirement for getting higher device performance, some papers proved that a multilayer MoS_2 channel was also able to attain comparable device performance, such as a high electron mobility over 100 cm^2/Vs and a high on/off current ratio of over 10^6 [23,36]. Therefore, it is thought that the performance of the multilayer MoS_2 is sufficient to study the post-annealing effect.

Figure 2 shows the representative I_d-V_g characteristics under constant $V_d = 10$ V, with respect to the post-annealing temperature among the many multilayer MoS_2 FETs shown in Additional file 1: Figure S1. This representative flake has a channel length of 10 μm and a width of 20 μm. This represents the n-type nature of the MoS_2 channel that makes the accumulation layer of electrons at positive gate biases, and it is observed as increasing the drain current at positive gate biases.

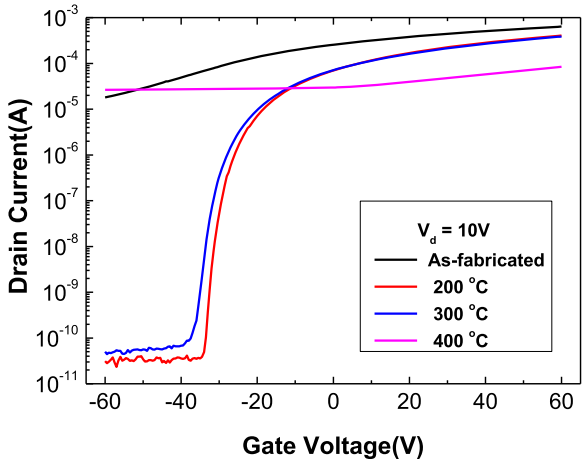

Figure 2 Transfer curves of the back-gated MoS_2 transistor according to the post-annealing temperature. Transfer curves at room temperature (black), 200°C (red), 300°C (blue), and 400°C (pink) of MoS_2 FET under various annealing temperatures, at V_d = 10 V.

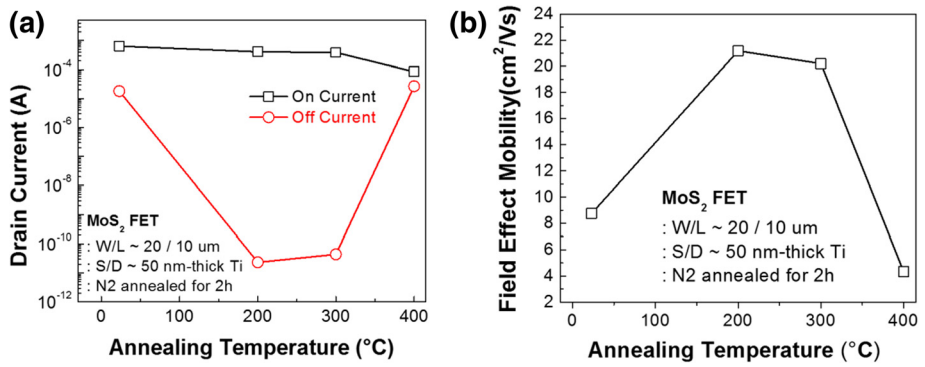

Figure 3 Trends of on current, off current, and field-effect mobility. (a) Details of I_{on} and I_{off} and **(b)** trends of field-effect mobility in terms of annealing temperature.

Theoretically, the drain current is supposed to be below 10^{-9} A at high negative gate biases, due to a depletion layer; however, a drain current of over 10^{-5} A was observed with various gate biases at room temperature (black line) and at 400°C (pink line). The drain current at the high negative gate biases drastically decreased by approximately 10^6, compared to that of the device under room temperature, and it seemed that MoS_2 has a depletion layer at both 200°C (red line) and 300°C (blue line).

In Figure 3a, the aforementioned transfer curves are arranged in terms of on and off current, with respect to post-annealing temperatures. The on current was defined as the highest drain current measured at high positive gate biases, and the off current was defined as the lowest drain current recorded at low negative gate biases. Figure 3a shows that the on current consistently decreases as the post-annealing temperature increases, while the off current decreases up to 200°C and increases with further increase of temperature. The lowest value of the off current was observed as approximately 10^{-11} A for the 200°C-annealed device, and this trend is in line with the transfer curve characteristics.

Figure 3b elaborates the field-effect mobility, which increased as the temperature rose and reached a high value of approximately 20.7 cm^2/Vs at 200°C and 300°C. The field-effect mobility with respect to the post-annealing temperature is also in accordance with the trend of the off current. Table 1 summarizes the details of the FET device performance parameters as annealing temperature.

Under those trends, the status of the device can be categorized into two regions. The first region, here termed region I, is that in which the device performance improves from room temperature to 200°C with decreasing off current and increasing field-effect mobility. The second region (region II) is that in which the device performance degrades from 200°C to 400°C with increasing off current and decreasing field-effect mobility.

In region I, the decrease of off current is thought to be caused by the atomic arrangement of MoS_2 atoms in local sites due to thermal energy. This kind of internal structural modification ends up with the release of a native point defect at the interface between the insulator and the channel material [30]. The interface properties between the MoS_2 and SiO_2 seemed to be improved, in that the subthreshold swing decreased from 36.20 to 0.91 [V/dec], as the post-annealing temperature increased to 200°C.

Table 1 Device performance summary

Temperature	On/off current ratio	On current (A)	Off current (A)	Field-effect mobility (cm^2/Vs)	Subthreshold swing [V/dec]
Room temperature	3.5×10^{01}	6.38×10^{-04}	1.80×10^{-05}	8.75	36.20
200°C	1.7×10^{07}	4.06×10^{-04}	2.34×10^{-11}	21.19	0.91
300°C	8.7×10^{06}	3.87×10^{-04}	4.43×10^{-11}	20.21	1.43
400°C	3.2×10^{00}	8.39×10^{-05}	2.66×10^{-05}	4.34	77.51

Exact values of the on/off current ratio, on current, off current, subthreshold swing, and field-effect mobility, at different temperatures.

Table 2 MoS_2 composition ratio change based on XPS data

Sample condition	Atom	Atomic %	Simplified ratio (let Mo be 1)
Non-annealed	S	63.14	1.712
	Mo	36.86	1
400°C-annealed	S	69.51	2.280
	Mo	30.49	1

Change of composition ratio between molybdenum and sulfur with respect to post-annealing.

Also, it is thought that the resist residue included during the fabrication process might be eliminated by the post-annealing process. The photoresist and organic materials from the 3M tape (3M, St. Paul, MN, USA) are one of the plausible candidates to be eliminated, and specifically, elimination of the photoresist residue of the graphene FET was observed with improvement of the device performance during the post-annealing process [33].

In region II, as mentioned, an increase of the off current by 5 or 6 orders was measured.

First, it is thought that such huge increase is caused by the change of the channel material itself. This is supported by the case of oxide semiconductors, such as $InGaZnO_4$ where desorption of Zn and O atoms over 700°C annealing and degradation in device performance were observed [30]. Similarly, the results of the X-ray photoelectron spectroscopy (XPS) proved that the S to Mo composition ratio significantly increased after annealing at 400°C in N_2 (Table 2). Furthermore, time-of-flight secondary ion mass spectroscopy (TOF-SIMS) depth profiles in Additional file 1: Figure S2 show that Mo decreased after annealing at 400°C in N_2, which correlated with the XPS data.

From Figure 4, Mo $3d_{5/2}$ and S $2p_{3/2}$ peaks were shifted in a higher energy by 0.6 and 0.5 eV, respectively, after annealing at 400°C. The molybdenum peak shift means that Mo^{4+} (228.98 eV) was changed into Mo^{5+} (230.3 eV) [37], and the S $2p_{3/2}$ peak shift toward a high binding energy (over 161.88 eV) has been ascribed to polysulfide or thiomolybdate species [38]. That is, one of the strong candidates for explaining the increase of the off current is the phase transformation of MoS_2 into Mo_2S_5 [39] by thermal energy. Furthermore, previous literature [40] provided evidence for this changed form to have high off current in terms of resistivity.

From a different point of view, adsorption of H_2O and O_2 on MoS_2 can also be one of the reasons for the increase of the off current. Under vacuum conditions, the off current actually decreased by average 10^2 level and this change is elaborated in Additional file 1: Figure S3. Therefore, it is guessed that adsorption was carried out after the high-temperature annealing process for the measurement of electrical characteristics at an atmosphere environment, and it was also supported by the case of graphene [41].

Conclusions

The evolution of off current for MoS_2 FET due to annealing temperature was systematically analyzed. As a result, the off current decreased up to 200°C annealing and increased for higher temperature annealing. Plausible explanations for the decrease in off current are the rearrangement of MoS_2 atoms and the elimination of the surface residue. Possible explanations for the increase in off current are the changes of the material's composition ratio and adsorption of H_2O and O_2. This research is meaningful in that the off current was controlled by the post-annealing temperature.

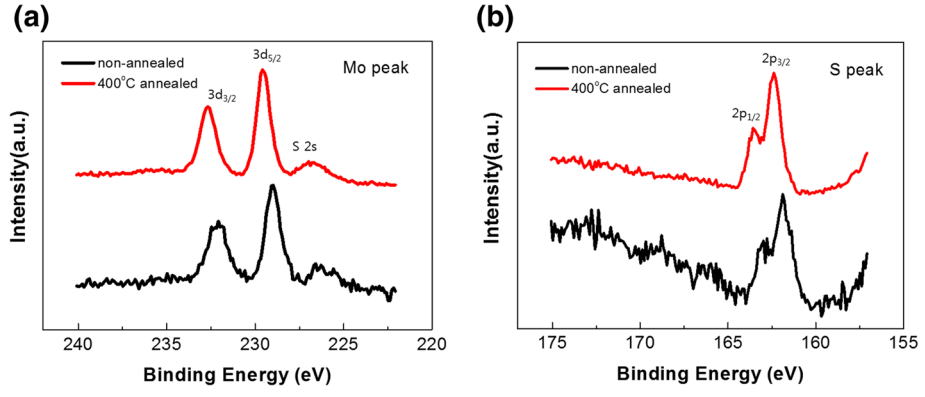

Figure 4 XPS data of the non-annealed and 400°C-annealed MoS_2. (a) Molybdenum peak and **(b)** sulfur peak of the non-annealed (black) and 400°C-annealed (red) MoS_2.

Additional file

Additional file 1: Supplementary figures. The file contains Supplementary Figures S1 to S3.

Competing interests
The authors declare that they have no competing interests.

Authors' contributions
SDN participated in the fabrication of the MoS_2 field-effect transistor, measured the electrical properties of the transistor, analyzed the results, and wrote the manuscript. SY helped fabricate the channel, drain, source, and gate of the transistor and participated in the interpretation of the result. KP, AJC, HK, and JYK participated in the analysis of the result. All the authors proofread and approved the final manuscript.

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References
1. Fengnian X, Damon BF, Yu-ming L, Phaedon A. Graphene field-effect transistors with high on/off current ratio and large transport band gap at room temperature. Nano Lett. 2010;10:715–8.
2. Thanasis G, Rashid J, Branson DB, Liam B, Roman VG, Sergey VM, et al. Vertical field-effect transistor based on graphene-WS2 heterostructures for flexible and transparent electronics. Nat Nanotechnol. 2013;8:100–3.
3. Podzorov V, Gershenson ME, Kloc C, Zeis R, Bucher E. High-mobility field-effect transistors based on transition metal dichalcogenides. Appl Phys Lett. 2004;84:3301–3.
4. Stefano L, Babk F, Emanuel T. Field-effect transistors and intrinsic mobility in ultra-thin $MoSe_2$ layers. Appl Phys Lett. 2012;101:223104.
5. Steven C, Corsin B, Angelica A, Stephen M, Jeong Seuk K, Xingtian Y, et al. MoS_2 P-type transistors and diodes enabled by high work function MoO_x contacts. Nano Lett. 2014;14:1337–42.
6. Song HS, Li SL, Gao L, Xu Y, Ueno K, Tang J, et al. High-performance top-gated monolayer SnS_2 field-effect transistors and their integrated logic circuits. Nanoscale. 2013;5:9666–70.
7. Debtanu D, John M, Sean S, Vincent Z, Arnold G, Haibing P. High on/off ratio field effect transistors based on exfoliated crystalline SnS_2 nano-membranes. Nanotechnology. 2013;24:025202.
8. Fucai L, Hidekazu S, Hui S, Thangavel K, Viktor Z, Neil D, et al. High-sensitivity photodetectors based on multilayer GaTe flakes. ACS Nano. 2014;8:752–60.
9. Roi L, Ora B, Gregory L, Reshef T, Ernesto J. Field-effect transistors based on WS_2 nanotubes with high current-carrying capacity. Nano Lett. 2013;13:3736–41.
10. Hui F, Steven C, Ting CC, Kuniharu T, Toshitake T, Ali J. High-performance single layered WSe_2 p-FETs with chemically doped contacts. Nano Lett. 2012;12:3788–92.
11. Geim AK, Novoselov KS. The rise of graphene. Nat Mater. 2007;3:183–91.
12. Schedin F, Geim AK, Morozov SV, Hill EW, Blake P, Katsnelson MI, et al. Detection of individual gas molecules adsorbed on graphene. Nat Mater. 2007;6:652–5.
13. Xinming L, Hongwei Z, Kunlin W, Anyuan C, Jinquan W, Chunyan L, et al. Graphene-on-silicon Schottky junction solar cells. Adv Mater. 2010;22:2743–8.
14. Damon BF, Yu-Ming L, Phaedon A. Graphene field-effect transistors with self-aligned gates. Appl Phys Lett. 2010;97:013103.
15. Moon JS, Curtis D, Bui S, Hu M, Gaskill DK, Tedesco JL, et al. Top-gated epitaxial graphene FETs on Si-face SiC wafers with a peak transconductance of 600 mS/mm. IEEE Electr Device Lett. 2010;31:260–2.
16. Jakub K, Pei-Lan H, Paul H, Peter WW, Craig LK, Mike S, et al. Epitaxial graphene transistors on SiC substrates. IEEE T Electron Dev. 2008;55:2078–85.
17. Wu YQ, Ye PD, Capano MA, Xuan Y, Sui Y, Qi M, et al. Top-gated graphene field-effect-transistors formed by decomposition of SiC. Appl Phys Lett. 2008;92:092102.
18. Melinda YH, Barbaros O, Yuanbo Z, Philip K. Energy band-gap engineering of graphene nanoribbons. Phys Rev Lett. 2007;98:206805.
19. Xiaolin L, Xinran W, Li Z, Sangwon L, Hongjie D. Chemically derived, ultrasmooth graphene nanoribbon semiconductors. Science. 2008;319:1229–32.
20. Obradovic B, Kotlyar R, Heinz F, Matagne P, Rakshit T, Giles MD, et al. Analysis of graphene nanoribbons as a channel material for field-effect transistors. Appl Phys Lett. 2006;88:142102.
21. Radisavljevic B, Radenovic A, Brivio J, Giacometti V, Kis A. Single-layer MoS_2 transistors. Nat Nanotechnol. 2011;6:147–50.
22. Qiu H, Pan LJ, Yao ZN, Li JJ, Shi Y, Wang XR. Electrical characterization of back-gated bi-layer MoS_2 field-effect transistors and the effect of ambient on their performances. Appl Phys Lett. 2012;100:123104.
23. Sunkook K, Aniruddha K, Wan-Sik H, Jong HL, Jiyoul L, Jaehyun Y, et al. High-mobility and low-power thin-film transistors based on multilayer MoS_2 crystals. Nat Commun. 2012;3:1011.
24. Jiang P, Yohei Y, Keng-Ku L, Lain-Jong L, Yoshihiro I, Taishi T. Highly flexible MoS_2 thin-film transistors with ion gel dielectrics. Nano Lett. 2012;12:4013–7.
25. Sung-Wook M, Hee SL, Hyoung JC, Min KP, Taewook N, Hyungjun K, et al. Nanosheet thickness-modulated MoS_2 dielectric property evidenced by field-effect transistor performance. Nanoscale. 2013;5:548–51.
26. Dominik L, Andras K. Breakdown of high-performance monolayer MoS_2 transistors. Acs Nano. 2012;6:10070–5.
27. Youngki Y, Kartik G, Sayeef S. How good can monolayer MoS_2 transistors be? Nano lett. 2011;11:3768–73.
28. Liu H, Neal TA, Ye DP. Channel length scaling of MoS_2 MOSFETs. Acs Nano. 2012;6:8563–9.
29. Junji S, Kazutoshi K, Shinsuke H, Ryoji K, Seiji S, Takaya S, et al. Excellent effects of hydrogen postoxidation annealing on inversion channel mobility of 4H-SiC MOSFET fabricated on (11 2 0) face. IEEE Electr Device Lett. 2002;23:13–5.
30. Se-Won L, Won-Ju C. Evaluation of the effects of thermal annealing temperature and high-k dielectrics on amorphous InGaZnO thin films by using pseudo-MOS transistors. J Korean Phys Soc. 2012;60:1317–21.
31. Mi RM, Sekwon N, Haseok J, Tae HL, Donggeun J, Hyoungsub K, et al. The effects of a combined thermal treatment of substrate heating and post-annealing on the microstructure of InGaZnO films and the device performance of their thin film transistors. Surf Interface Anal. 2012;44:1431–5.
32. Joshi P, Romero HE, Neal AT, Toutam VK, Tadigadapa SA. Intrinsic doping and gate hysteresis in graphene field effect devices fabricated on SiO_2 substrates. J Phys-Condens Mat. 2010;22:334214.
33. Zengguang C, Qiaoyu Z, Chenxuan W, Qiang L, Chen W, Ying F. Toward intrinsic graphene surfaces: a systematic study on thermal annealing and wet-chemical treatment of SiO_2-supported graphene devices. Nano lett. 2011;11:767–71.
34. Pirkle A, Chan J, Venugopal A, Hinojos D, Magnuson CW, McDonnell S, et al. The effect of chemical residues on the physical and electrical properties of chemical vapor deposited graphene transferred to SiO_2. Appl Phys Lett. 2011;99:122108.
35. Plechinger G, Schrettenbrunner F-X, Eroms J, Weiss D, Schüller C, Korn T. Low-temperature photoluminescence of oxide-covered single-layer MoS_2. Phys Status Solidi-R. 2012;6:126–8.
36. Saptarshi D, Hong-Yan C, Ashish VP, Joerg A. High performance multilayer MoS_2 transistors with scandium contacts. Nano Lett. 2012;13:100–5.
37. Weber T, Muijsers JC, Wolput JHMCV, Verhagen CPJ, Niemantsverdriet JW. Basic reaction steps in the sulfidation of crystalline MoO_3 to MoS_2, as studied by x-ray photoelectron and infrared emission spectroscopy. J Phys Chem. 1996;100:14144–50.
38. Peery AS, McIntyre NS. A Raman and XPS investigation of supported molybdenum oxide thin films. 2. Reactions with hydrogen sulfide. J Phys Chem. 1993;97:11031–6.

39. Wang HW, Skeldon P, Thompson GE. Thermogravimetric-differential thermal analysis of the solid-state decomposition of ammonium tetrathiomolybdate during heating in argon. J Mater Sci. 1998;33:3079–83.
40. Bensimon Y, Belougne P, Deroide B, Ducourant B, Giuntini JC, Zanchetta JV. Influence of oxygen on electrical conductivity of amorphous molybdenum sulfides. J Non-cryst Solids. 1991;134:239–48.
41. Ni HZ, Wang MH, Luo QZ, Wang YY, Yu T, Wu HY, et al. The effect of vacuum annealing on graphene. J Raman Spectrosc. 2010;41:479–83.

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