Chaotic memristor

T. Driscoll · Y.V. Pershin · D.N. Basov · M. Di Ventra

Abstract We suggest and experimentally demonstrate a chaotic memory resistor (memristor). The core of our approach is to use a resistive system whose equations of motion for its internal state variables are similar to those describing a particle in a multi-well potential. Using a memristor emulator, the chaotic memristor is realized and its chaotic properties are measured. A Poincaré plot showing chaos is presented for a simple nonautonomous circuit involving only a voltage source directly connected in series to a memristor and a standard resistor. We also explore theoretically some details of this system, plotting the attractor and calculating Lyapunov exponents. The multi-well potential used resembles that of many nanoscale memristive devices, suggesting the possibility of chaotic dynamics in other existing memristive systems.

1 Introduction

The class of memory circuit elements consisting of memristors, memcapacitors and meminductors [1, 2] is a relatively new paradigm based on the understanding that many

T. Driscoll · D.N. Basov · M. Di Ventra (✉)
Department of Physics, University of California,
9500 Gilman Drive, San Diego, La Jolla, CA 92093, USA
e-mail: diventra@physics.ucsd.edu

Present address:
T. Driscoll
Center for Metamaterials and Integrated Photonics,
Department of Computer and Electrical Engineering,
Duke University, Durham, NC 27708, USA

Y.V. Pershin
Department of Physics and Astronomy and USC Nanocenter,
University of South Carolina, Columbia, SC 29208, USA

physical realizations of basic circuit elements (resistors, capacitors and indicators) may involve an intrinsic memory mechanism, at least on certain time scales. Currently, a lot of attention is devoted to such elements and their potential applications—with a primary focus on memristive elements [3–5]. Physical manifestations of memristors range from thermistors [6] to complex oxide [7–11] and spintronic [12–14] materials. A number of possible intriguing applications of memristors have already been discussed including digital memory [15–17], neuromorphic systems [18–20], adaptive filters [21, 22], tunable and reconfigurable metamaterials [11], and others [23–25].

By definition [1, 4], an nth-order voltage-controlled memristive system is described by the relations

$$I(t) = R_M^{-1}(x, V_M, t) V_M(t) \tag{1}$$

$$\dot{x} = f(x, V_M, t) \tag{2}$$

where $V_M(t)$ and $I(t)$ denote the voltage across and current through the device, R_M is a scalar called the *memristance*, x is a vector representing n internal state variables, and f is an n-component vector function. Following present convention, we will call a device described by (1)–(2) a memristor, even though the latter was originally defined when R_M depends on charge or flux (time integral of voltage) only [3].

In this paper, we consider a specific type of second-order memristor described by (2) of the form

$$\frac{d}{dt} \begin{bmatrix} x \\ \dot{x} \end{bmatrix} = \begin{bmatrix} \dot{x} \\ -\frac{1}{m} \frac{\partial U}{\partial x} - \gamma \dot{x} + \frac{F(V_M)}{m} \end{bmatrix}, \tag{3}$$

where x and $\dot{x}$ are internal state variables, m is an effective mass associated with the internal state of the device, $U(x)$ is a multi-well potential such that $U(\pm\infty) = \infty$ (see schematic in Fig. 1), γ is a damping coefficient and F is

a driving force that depends on the voltage applied to the memristor.

It is important to note that (3) describes the classical dynamics of an effective particle in a multi-well potential and has a close connection to physical processes in certain nanoscale memristors [26]. In particular, oxygen vacancy migration in TiO_2 memristors can be described as a hopping process between potential minima [26]. Moreover, a strained elastic membrane memcapacitor (memory capacitor) [27] is also described by equations similar to (3). These connections give physical grounding to our choice of memristive function.

An important consequence of (3) is the existence of a chaotic regime within a certain range of parameters. This approach to chaos with memristors is unique and radically different from previous proposals [22, 28–30] that are based on modified Chua's circuits [31, 32] with *active* elements. We emphasize also that our realization of chaos results from the simplest single-element nonautonomous chaotic circuit consisting of the chaotic memristor directly connected to a voltage source. The presence of chaos in such a simple system certainly has potential applications in cryptography and communications, as well as other areas. It is also conversely true, however, that chaotic behavior can be a detriment in memory or computation systems—areas where memristors are currently pushing toward prototype devices. Thus, understanding the origins of chaos in memristive systems may be critical to avoid or eliminate chaos.

The layout of this paper is as follows: In Sect. 2, the chaotic regime is demonstrated experimentally. For the experiment, we have built a memristor emulator [20, 23, 33], namely a simple circuit that can emulate essentially any memristive function f, and has been used by two of the present authors (YVP and MD) to build memcapacitor and meminductor emulators [33], discuss learning and associative memory [20], build programmable analog circuits [23], and even perform logic and arithmetic operations [34]. In this work we have implemented the double-well potential of (3). Applying ac-pulse sequences, we explicitly show chaotic behavior within a certain range of applied voltage amplitudes. Then, in Sect. 3, we connect our experiment to a theoretical investigation of this system, including exploration of the phase space and Lyapunov exponents for such double-well potentials. Our main results and conclusions are summarized in Sect. 4.

2 Experimental demonstration of chaos

For our experiment, the simple electronic circuit shown in Fig. 1(a) was constructed. A programmable voltage source $V(t)$ is connected in series with the memristor M and a
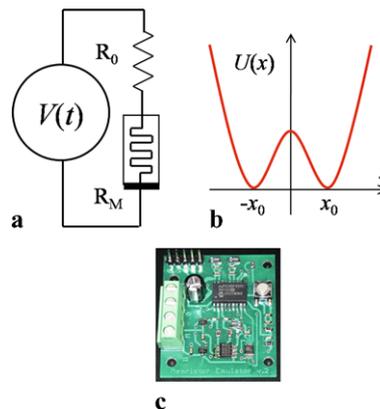

Fig. 1 (**a**) Electronic circuit used in chaos measurements consisting of the programmable voltage source $V(t)$, 510 Ohms resistor R_0 and memristor M. The memristor specifications are given in the text. (**b**) Schematic of the double-well potential governing the memristor. (**c**) Optical photograph of memristor emulator

current-sensing resistor R_0. A memristor emulator [20, 23, 33] whose circuit image is shown in Fig. 1(c) was employed for the memristor. At the electronic component level, the memristor emulator consists of a digital potentiometer, analog-to-digital converter (ADC) unit and control unit (microcontroller). The control unit reads the digital code from the ADC (corresponding to the applied voltage) and generates (and writes) a code for the digital potentiometer according to the predefined algorithm. For the case of the double-well potential we have re-written (3) in the form

$$\ddot{x} = -c_1\dot{x} - c_2 x(x^2 - 1) + c_3 V_M(t), \qquad (4)$$

where $c_1 = 2\,\text{s}^{-1}$, $c_2 = 100\,\text{s}^{-2}$ and $c_3 = 30\,\text{V}^{-1}\,\text{s}^{-2}$. The function $R_M(x)$ was then chosen as $R_M = (4875 + 1560x)$ Ohms. According to (4) at $V_M = 0$ the potential minima $\pm x_0$ are located at ± 1.

We also make use of a control memristor, programming our emulator with a standard threshold-type model [19]

$$I(t) = x^{-1} V_M(t), \qquad (5)$$

$$\dot{x} = -\beta V_M + 0.5\beta(|V_M + V_T| - |V_M - V_T|) \qquad (6)$$

with the parameters $\beta = 62\,\text{k}\Omega/(\text{V·s})$, $V_T = 0.625\,\text{V}$, and the memristance can change only between $R_1 = 1\,\text{k}\Omega$ and $R_2 = 10\,\text{k}\Omega$. In the actual microcontroller's software implementation, the value of x is monitored at each time step and in the situations when $x < R_1$ or $x > R_2$, it is set equal to R_1 or R_2, respectively.

In this circuit, the applied voltage and the voltage across R_0 are both measured at 800 Hz, in hardware-timed synchronization with the update rate of $V(t)$. The sequence of the applied voltage $V(t)$ is as follows: starting from zero applied voltage, we apply a large negative voltage $(-2.25\,\text{V})$ for 2 seconds, followed by zero voltage for 1 second. This
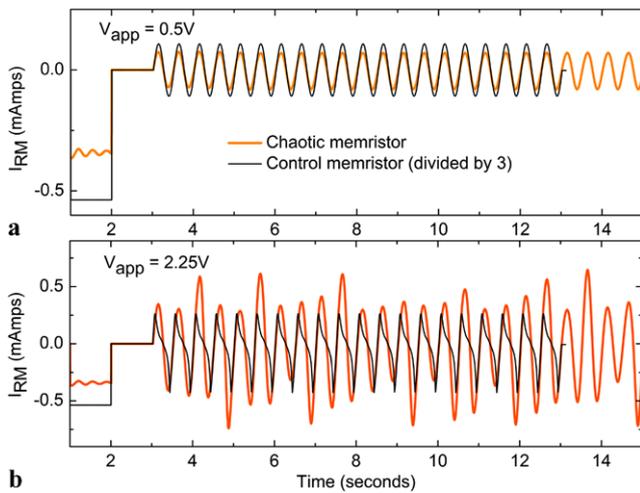
Fig. 2 Traces showing current through the memristor for two cases: a control memristor and our chaotic memristor. The chaotic memristor operates according to (1, 4) with R_M defined below (4). The control memristor operates according to (5 and 6). Traces are shown for two voltages: (**a**) The applied voltage amplitude is below the threshold where both systems behave linearly. (**b**) The applied voltage amplitude is above threshold. In the above-threshold region for our chaotic memristor, notice that the amplitude of any peak follows no pattern, while the control memristor peaks remain constant even though it follows an un-harmonic wave-shape. In each case the initial low voltage is a "reset" procedure to verify the state of the memristor is known at the onset of applied oscillations

acts as a reset, ensuring we know the initial state of the memristor. After this reset, a sinusoidal voltage of 2 Hz is applied with a peak amplitude V_{app}. This is applied for 10 seconds for the control memristor, and 20 seconds for the chaotic memristor. After this, the voltage is returned to zero, and the system is allowed to rest for 5 seconds. Then the complete sequence (including a reset each time) is repeated for increasing values of V_{app} between 0.1 V and 2.9 V with 1000 steps. It is important to include a reset in each sequence, as the memristor retains information about previous voltages applied to it. By utilizing such a reset we can insure that initial conditions are known, a very important point for chaotic systems.

From the measured V_{R_0} the instantaneous current $I(t)$ through the circuit can be calculated at any time. As indicated in (1), $I(t)$ is a critical parameter for understanding the behavior of R_M. Figure 2 plots such current for four important cases. In Fig. 2(a), current traces are plotted for our control memristor (black) and chaotic memristor (orange) for $V_{app} = 0.5$ V, which is below the threshold voltage for both systems. For such sub-threshold voltages, the response of both systems is nearly linear, and we observe periodic sinusoidal currents. In Fig. 2(b) we repeat this for $V_{app} = 2.25$ V, which is above threshold voltage. In this case we observe the control memristor (black) circuit exhibits very nonlinear currents. However, despite the un-harmonic shape, the amplitudes of the current peaks (both positive and negative)
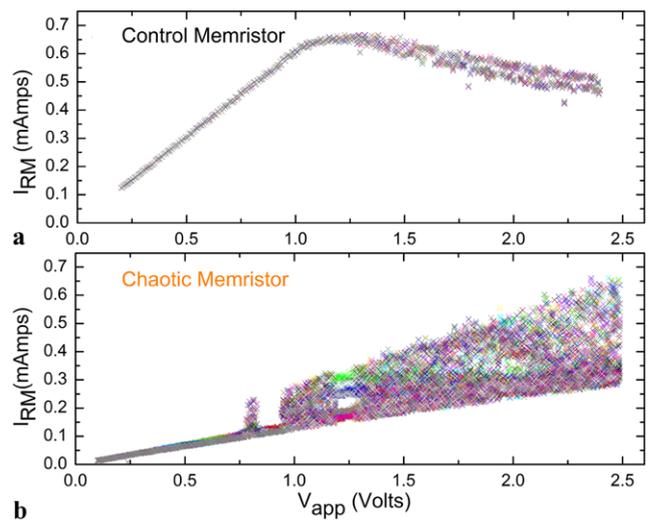

Fig. 3 Poincaré graphs constructed from the oscillation peaks from the $I-V$ datasets (such as those in 2). For the control memristor (**a**), the graph shows no chaotic behavior anywhere. For the chaos memristor (**b**), above a certain threshold (about 1 V) the behavior is chaotic. The threshold at which this chaos onset is determined by the potential barrier between the double well. The colors used for sequential points follows a repeating rainbow colormap. This further helps to show the lack of any pattern, as no color pattern/structure is evident

are nearly constant and predictable from one to the next. In contrast, for the chaotic memristor the current-peak amplitude from one cycle to the next can be very different, and change in an unpredictable (pattern-less) manner. This is a fingerprint of chaotic behavior.

In order to better illustrate this chaotic behavior, we construct Poincaré plots from the complete $I(t)$ dataset. To do this, the amplitude of $I(t)$ is extracted at periodic times of the driving frequency, selecting the positive peak of each oscillation. All peaks in each V_{app} dataset are plotted as a function of the V_{app}, except the first three periods from each V_{app} are omitted to exclude any transient effects. This procedure gives 37 values for the chaotic memristor and 17 for control memristor for each V_{app}. These are plotted in Fig. 3.

Looking at the Poincaré plots, we see very different behavior between the control memristor and the chaotic memristor. In the low voltage region (<1 V) of the control memristor (Fig. 3a), the 17 points overlap almost exactly, creating a linear response. Above 1 V, two narrowly split branches emerge. Most probably, these branches are a result of the finite resistance discretization in our memristor emulator. For the rapid $\dot{x}$ above threshold, errors stemming from the relatively slow internal update rate of the emulator causes the resistance value to jitter two neighboring digital values. This small effect (only $\sim$1% changes in R) comes only from our emulator implementation and not the memristive dynamics itself. The negative differential resistance also stems from the function (6) of our control memristor [19]. The Poincaré plot for the chaotic memristor looks very different. At low

voltages, it also behaves as a normal linear resistor. However, above a threshold voltage of about 1 V, the linear structure disintegrates into complete filling of the phase space between a lower and an upper bound. On a Poincaré plot, this is clear evidence of chaotic behavior. The space filling is a graphic representation of the fact that even when subjected to a periodic potential, the response of the system at later times is unpredictable (within system bounds, as well as restrictions of harmonic driving). There is some interesting fine-structure within part of the chaotic-memristor Poincaré plot, including one sub-voltage peak at about 0.8 V, and the existence of what appears to be a tri-stable region near 1.25 V. This is typical of chaotic systems (see, e.g., Ref. [35]).

3 Theoretical analysis

One simple way to understand the chaotic nature of the response seen in Fig. 3 is to look at the instantaneous resistance value of the memristor after some fixed time. Because the memristance value is so sensitive to the complete history of applied voltage, memristors with certain state-response functions—including, but likely not limited to, the double-well function used in this work—can enter a chaotic region where a small change in initial conditions produces a radically different value after a fixed time; the so called "butterfly effect". We can illustrate this quite nicely numerically. To do so, we repeat the procedure of our experiment, driving the system with sinusoidal $V(t)$ and solving for a final value $R_M(t_f)$ at $t_f = 19.875$ seconds. In a non-chaotic system, small changes in the driving voltage amplitude V_{app} would cause small changes in $R_M(t_f)$. In our chaotic-memristive system, however, small changes produce a pseudo-random value of $R_M(t_f)$, within certain bounds. This is shown in Fig. 4. One advantage of illustrating this numerically is that it eliminates noise or other experimental errors from affecting the long-time value of $R_M(t_f)$, which can give the false impression of chaotic behavior even when none exists.

One final theoretical tool which is often employed to help understand chaotic systems is the phase-space attractor plot and accompanying calculation of the Lyapunov exponents. For the double-well function of (4) which we use, the phase space can be plotted as $\dot{x}(x)$. This is shown in Fig. 5 for two voltages, one below threshold (0.5 V) and one above (1.6 V). Below threshold (Fig. 5a) we observe that the phase-space trajectory quickly moves from initial conditions into a steady orbit. This is non-chaotic behavior. Above threshold (Fig. 5b), there is no single steady orbit, but instead the system circles around two attractors and explores almost an entire available phase space (determined by both V_{Rm} and system properties).

The Lyapunov exponent is a measure of how quickly two orbits in the phase space, originating from infinitesimally
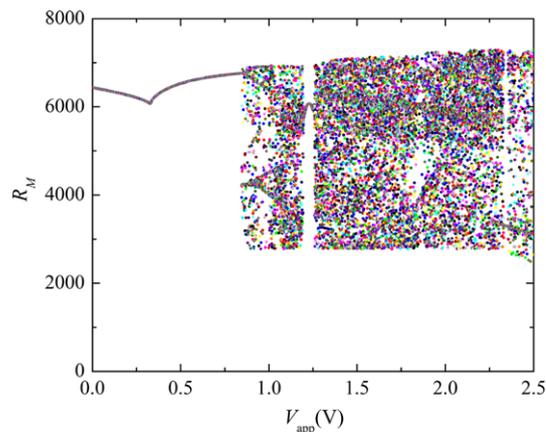

Fig. 4 Numerically calculated value of memristance $R_M(t_f)$ at $t_f = 19.875$ s. This is plotted as a function of the amplitude of the applied voltage V_{app}. The fact that small changes in V_{app} (i.e., neighboring x-axis points) result in large changes in $R_M(t_f)$ is an indicator of chaos
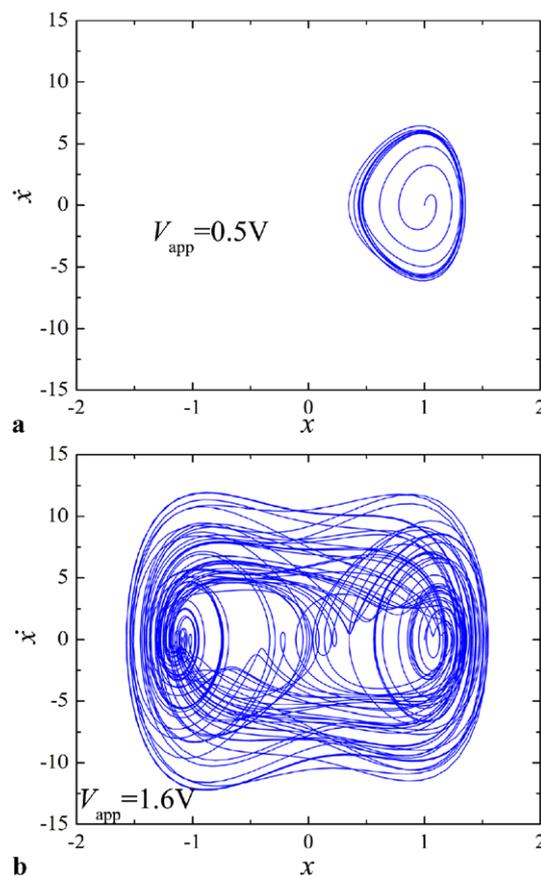

Fig. 5 System trajectories below (**a**) and above (**b**) the chaos onset. These plots represent 50 s of system evolution driven by an applied ac voltage of 2 Hz frequency. The voltage amplitude is shown on the plots for each case

close initial conditions, will diverge in time, as expressed in the equation:

$$|\delta R_M(t)| \approx e^{\lambda t}|\delta R_M(t_0)| \qquad (7)$$

We calculate the maximum Lyapunov exponent for our system using the common numerical method described in [36, 37]. For the two voltages in Fig. 5a,b (above and below threshold), we obtain values for the maximum Lyapunov exponent of $\lambda = -2.1 \text{ s}^{-1}$ and $\lambda = 0.15 \text{ s}^{-1}$, respectively. As the latter (above-threshold) value is greater than zero, it proves the chaotic nature of the double-well system above threshold voltage. Although it would be gratifying to see a similar result obtained from our experimentally collected data, noise and limited data make this difficult. This is not surprising, as unambiguous Lyapunov exponent calculation from data is often a difficult matter.

4 Summary and conclusions

In this work, we have proposed a model of chaotic memristor whose internal state dynamics is described by an equation of a particle in multi-well potential. As an example of such a model, a nonautonomous chaotic circuit based on a memristor governed by a double-well potential was investigated both experimentally and theoretically. This simple circuit consists only of a memristor and a series current-sensing resistor. Using a memristor emulator, we have experimentally demonstrated the chaotic operation of this circuit, and contrasted it to the observed non-chaotic response when a traditional control memristor is used. By subjecting our chaotic-memristive circuit to periodic applied voltages, we have constructed a Poincaré map for our system which clearly identifies a region of chaotic behavior above a threshold voltage. The simplicity of this chaotic circuit should entice opportunities in many applications. Also, awareness of the existence of a chaotic region which may potentially exist in many memristive systems is critical for avoiding (or utilizing) this region as necessary.

Moreover, the similarity between our model of chaotic memristor and a wide range of physical systems, including TiO$_2$ memristors [7], suggests that our results can be realizable in certain material systems. Indeed, the oxygen vacancies' migration in TiO$_2$ memristors can be considered as a hopping of a classical particle between potential minima [26]. Such a process, for a single vacancy, is exactly described by (3), where x is the vacancy's position and $U(x)$ is the potential energy profile along the vacancy's path. As the vacancies' positions define the transport properties of memristive devices [7], chaotic features of vacancies motion should be visible in $I-V$ response. In fact, the experimentally observed noise in periodically driven TiO$_2$ memristors (see, for example, Fig. 1c of Ref. [7]) may be related to chaotic dynamics of oxygen vacancies.

References

1. M. Di Ventra, Y.V. Pershin, L.O. Chua, Proc. IEEE **97**(10), 1717 (2009)
2. Y.V. Pershin, M. Di Ventra, Adv. Phys, (2010, in press). arXiv:1011.3053
3. L.O. Chua, IEEE Trans. Circuit Theory **18**, 507 (1971)
4. L.O. Chua, S.M. Kang, Proc. IEEE **64**, 209 (1976)
5. D.B. Strukov, G.S. Snider, D.R. Stewart, R.S. Williams, Nature **453**, 80 (2008)
6. M. Sapoff, R.M. Oppenheim, Proc. IEEE **51**, 1292 (1963)
7. J.J. Yang, M.D. Pickett, X. Li, D.A.A. Ohlberg, D.R. Stewart, R.S. Williams, Nat. Nanotechnol. **3**, 429 (2008)
8. S.H. Jo, K.H. Kim, W. Lu, Nano Lett. **9**, 870 (2009)
9. N. Gergel-Hackett, B. Hamadani, B. Dunlap, J. Suehle, C. Richter, C. Hacker, D. Gundlach, IEEE Electron Device Lett. **30**, 706 (2009)
10. T. Driscoll, H.T. Kim, B.G. Chae, M. Di Ventra, D.N. Basov, Appl. Phys. Lett. **95**, 043503 (2009)
11. T. Driscoll, H.T. Kim, B.G. Chae, B.J. Kim, Y.W. Lee, N.M. Jokerst, S. Palit, D.R. Smith, M. Di Ventra, D.N. Basov, Science **325**, 1518 (2009)
12. Y.V. Pershin, M. Di Ventra, Phys. Rev. B **78**, 113309 (2008)
13. Y.V. Pershin, M. Di Ventra, Phys. Rev. B **79**(15), 153307 (2009)
14. X. Wang, Y. Chen, Y. Gu, H. Li, IEEE Electron Device Lett. **31**, 20 (2010)
15. P. Kuekes, D. Stewart, R. Williams, J. Appl. Phys. **97**(3), 034301 (2005)
16. E. Lehtonen, M. Laiho, in *Proceedings of the 2009 International Symposium on Nanoscale Architectures (NANOARCH'09)* (2009), pp. 33–36
17. D.B. Strukov, R.S. Williams, Proc. Natl. Acad. Sci. USA **106**, 20155 (2009)
18. G.S. Snider, SciDAC Rev. **10**, 58 (2008)
19. Y.V. Pershin, S. La Fontaine, M. Di Ventra, Phys. Rev. E **80**, 021926 (2009)
20. Y.V. Pershin, M. Di Ventra, Neural Netw. **23**, 881 (2010)
21. T. Driscoll, J. Quinn, S. Klein, H.T. Kim, B. Kim, Y. Pershin, M. Di Ventra, D.N. Basov, Appl. Phys. Lett. **97**, 093502 (2010)
22. B. Muthuswamy, P.P. Kokate, IETE Tech. Rev. **26**, 417 (2009)
23. Y.V. Pershin, M. Di Ventra, IEEE Trans. Circuits Syst. I **57**, 1857 (2010)
24. S.H. Jo, T. Chang, I. Ebong, B.B. Bhadviya, P. Mazumder, W. Lu, Nano Lett. **10**, 1297 (2010)
25. M. Itoh, L.O. Chua, Int. J. Bifurc. Chaos **19**, 3605 (2009)
26. D.B. Strukov, R.S. Williams, Appl. Phys. A, Mater. Sci. Process. **94**, 515 (2009)
27. J. Martinez-Rincon, Y.V. Pershin, in preparation (2010)
28. M. Itoh, L.O. Chua, Int. J. Bifurc. Chaos **18**, 3183 (2008)
29. B.C. Bao, Z. Liu, J.P. Xu, Electron. Lett. **46**, 228 (2010)
30. B. Bao, Z. Liu, J.P. Xu, Chin. Phys. B **19**, 030510 (2010)
31. T. Matsumoto, IEEE Trans. Circuits Syst. **31**, 1055 (1984)
32. R.N. Madan, *Chua's Circuit: A Paradigm for Chaos* (World Scientific Publishing Company, Singapore, 1993)
33. Y.V. Pershin, M. Di Ventra, Electron. Lett. **46**, 517 (2010)
34. Y.V. Pershin, M. Di Ventra, arXiv:1009.6025 (2010)
35. M. Zwolak, D. Ferguson, M. Di Ventra, Phys. Rev. B **67**, 081303 (2003)
36. A. Wolf, J. Swift, H. Swiney, J.A. Vastano, Physica D **16**, 285 (1985)
37. A.R. Zeni, J.A. Gallas, Physica D **89**, 71 (1995)