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Catastrophic Fault Diagnosis of a Certain Class of Nonlinear Analog Circuits

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Abstract This paper deals, for the first time, with catastrophic fault diagnosis of nonlinear analog circuits containing bipolar and MOS transistors having multiple operating points (DC solutions). The faults are cuts of some connecting paths and short-circuits of some pairs of points. Simulation-before-test approach is applied for detection and identification of a single catastrophic fault. To build a fault dictionary, a diagnostic test is arranged based on DC analysis. In the discussed circuits having multiple DC solutions, the tested output voltage may assume different values for fixed value of the input voltage. This fact considerably complicates the fault diagnosis. The crucial point of the proposed approach is tracing large number of nonlinear multivalued input–output characteristics at different values of circuit parameters within their tolerance ranges. For this purpose an efficient and fast algorithm is developed, based on the theory known under the name a linear complementarity problem. To illustrate the proposed approach and show its efficiency, four numerical examples are given.

Keywords Analog circuits · Catastrophic faults · Fault diagnosis · Nonlinear circuits

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1 Introduction

Fault diagnosis of analog circuits is a fundamental problem for design validation [8,10,11]. A fault can be soft if a parameter is drifted from its tolerance range, but does not lead to any topological changes, or catastrophic which is defined as cut (open-circuit) of some connecting path or short-circuit of some pair of points. They are caused by contaminated phototools, defective raw material, improper solder leveling, mechanical damage, etc. [8].

If circuit simulations take place before any testing, the diagnosis approach is termed a simulation-before-test (SBT). The results of circuit simulations are stored as patterns in a fault dictionary [1,6,9,13,18,19]. Comparing the voltages measured at testing nodes with the information contained in the dictionary, the faulty element can be identified. During the last decades a number of methods, concepts, and techniques have been proposed to build and exploit fault dictionary, e.g., sensitivity analysis [13], neural networks [1,2,6,18], and Householder formula in matrix theory [24,26]. The fault masking by component tolerances is a difficult problem faced by SBT approach.

Diagnosing of analog circuits can be performed in DC, time and frequency domains. For example, reference [16] offers a method for parametric and catastrophic fault detection and location of linear circuits in the frequency domain, whereas the papers [14,20,21,29] bring diagnostic methods using the time-domain features.

Most work devoted to SBT approach has been focused on detection and identification of a single catastrophic fault. Building a fault dictionary usually requires a very large computing power, especially in the case of multiple faults in nonlinear networks, where the amount of computations increases dramatically [24,26].

In this paper, fault diagnosis of nonlinear circuits using SBT approach, based on DC analysis, is considered. A method is proposed for detection and identification of a single catastrophic fault in BJT and MOS circuits having multiple operating points. The circuits are used, e.g., in signal conditioning applications, function generators and switching power supplies. Even if the tested circuit does not contain any capacitors and inductors, some parasitic capacitances and inductances exist. In DC analysis they are ignored and the circuit is considered as purely resistive. The DC operating points of the resistive circuit are the equilibrium points of the original circuit. Some of them are unstable and cannot occur. Generally, to indicate the unstable operating points among all operating points, the distribution and values of parasitic capacitances and inductances are required. If a circuit has multiple DC operating points the tested output voltage may assume different values for fixed value of the input voltage. The question which of the possible values actually occurs depends on the transient state which precedes the DC steady state. Since it is unknown, all the operating points should be taken into account during fault diagnosis. According to our knowledge, no work has been focused on fault diagnosis of such class of analog circuits till now. The crucial point of the proposed approach is tracing a large number of nonlinear multivalued input-output characteristics. For this purpose, an efficient algorithm is developed, based on the theory known under the name a linear complementarity problem [5,7,27], considering the deviations of the circuit parameters within their tolerance ranges. To perform diagnostic test, a DC input voltage source is applied at the node accessible for excitation and output voltages are read at the nodes accessible for measurement

(usually one node). This is why the problem of selecting testing points of the circuit under test is not considered in this paper. Since the method usually needs only one node accessible for measurement it can be applied both to integrated circuits and PCB-based circuitries.

2 The Theoretical Background

This section gives the theoretical background of the method proposed for tracing of input–output characteristics in nonlinear circuits comprising bipolar and MOS transistors, having multiple DC solutions. Since large number of the characteristics is required by the diagnostic method, developed in Sect. 5, a fast and efficient algorithm for tracing the characteristics is necessary. If a circuit has multiple DC solutions, the input–output characteristic is not necessarily a single-valued function of the input, usually it is multivalued or even multibranched. The characteristic can be traced using a brute-force method which is capable of finding all the solutions for different values of the input voltage. Unfortunately, this method is very time-consuming and can be applied to small-sized circuits only. There are several more efficient methods, e.g., [3,28,30]. However, they are rather difficult to implement and usually suffer from major shortcoming due to sharp-turning-point problem. The method proposed in [23] overcomes this problem, but it is dedicated to just BJT circuits. On the other hand, SPICE simulator usually provides incomplete characteristics and often exhibits a sharp hysteresis loop, whereas the actual characteristic is Z-type.

In this section, an efficient algorithm for tracing input–output characteristics in circuits having multiple DC solutions is proposed, based on the theory known under the name a linear complementarity problem [5,7]. The algorithm, which extends some ideas presented in [27], is described using BJT circuits, but it can be directly adapted to MOS circuits.

Consider a circuit consisting of bipolar transistors, diodes, resistors, and voltage sources. The transistors are characterized by the Ebers–Moll model [4,27] shown in Fig. 1. We approximate the exponential characteristics of the diodes included in the model or acting alone using piecewise-linear functions similarly as in [27]. N-segment piecewise-linear characteristic is shown in Fig. 2a. The diode specified by this characteristic can be modeled by the circuit shown in Fig. 2b including $N-1$ ideal diodes having the characteristic shown in Fig. 3a. It is convenient to choose reversed reference direction of the voltage across the ideal diode. Then the characteristic is as shown in Fig. 3b and the diode is described by relations

$$i \geq 0, \quad v \geq 0, \quad iv = 0. \tag{1}$$

To trace transfer characteristic $v_0 = f(y)$, where v_0 is the output voltage and y is the input voltage, we select from the circuit all the ideal diodes, the source y, and the open-circuited branch with the output voltage v_0 as shown in Fig. 4. As a result an m-port is created ($m = n + 2$) consisting of linear resistors, current-controlled current sources, and independent voltage sources.

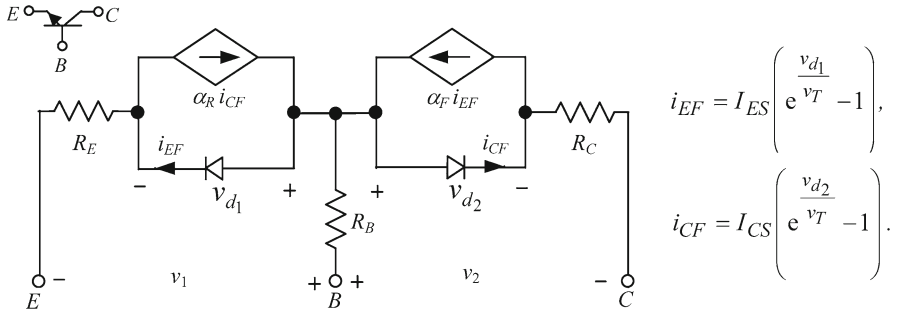

Fig. 1 Ebers–Moll model of NPN transistor

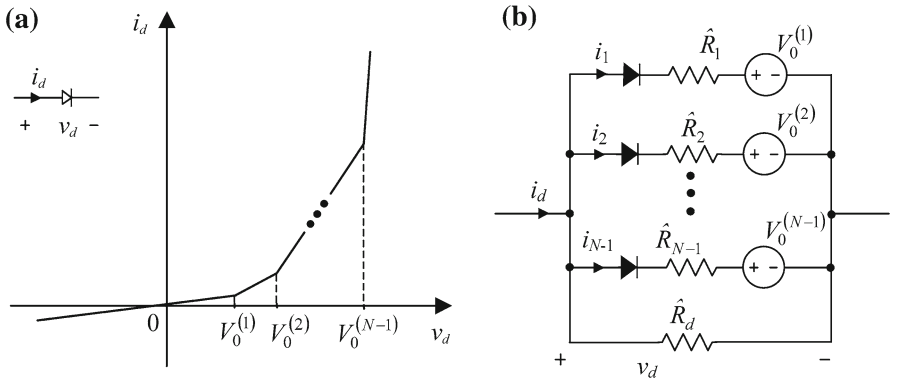

Fig. 2 N-segment characteristic of diode (**a**) and its model (**b**)

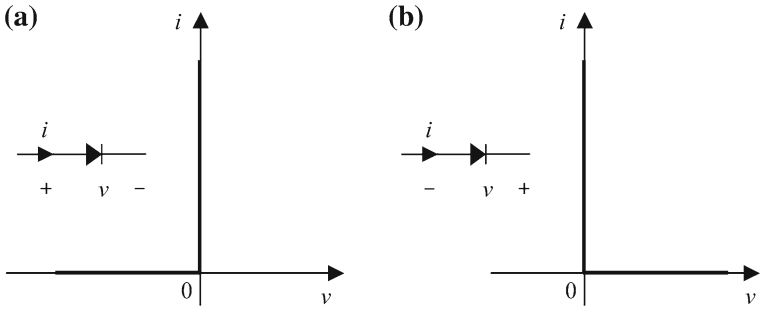

Fig. 3 Characteristic of the ideal diode

To form the hybrid representation of the circuit, we replace the ideal diodes by voltage sources and connect to the output terminals a zero current source $i_{n+2} = 0$ (see Fig. 5).

Using the hybrid representation of the m-port, we write

$$\begin{bmatrix} \hat{\boldsymbol{i}} \\ v_{n+2} \end{bmatrix} = \boldsymbol{H} \begin{bmatrix} \hat{\boldsymbol{v}} \\ i_{n+2} \end{bmatrix} + \boldsymbol{s}, \tag{2}$$

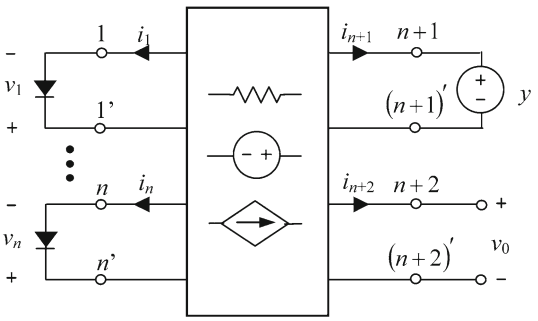

Fig. 4 Circuit with extracted ideal diodes, input voltage source and the output open circuited branch

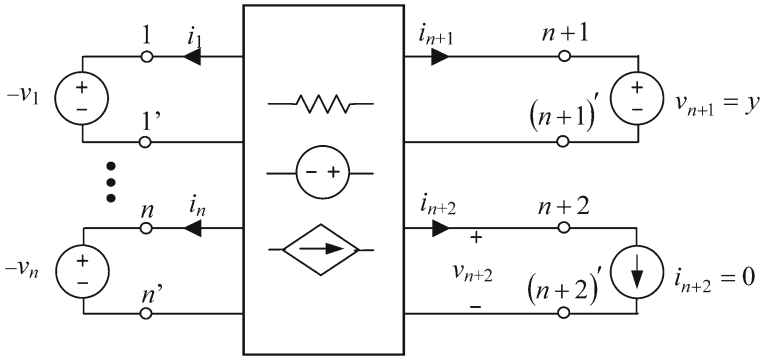

Fig. 5 Rearranged circuit of Fig. 4

where

$$\hat{\boldsymbol{i}} = \begin{bmatrix} i_1 \\ \vdots \\ i_n \\ i_{n+1} \end{bmatrix}, \hat{\boldsymbol{v}} = \begin{bmatrix} -v_1 \\ \vdots \\ -v_n \\ v_{n+1} \end{bmatrix}, \boldsymbol{s} = \begin{bmatrix} s_1 \\ \vdots \\ s_{n+2} \end{bmatrix}$$

$$\boldsymbol{H} = \begin{bmatrix} h_{11} & \cdots & h_{1n} & h_{1,n+1} & h_{1,n+2} \\ \vdots & \cdots & \vdots & \vdots & \vdots \\ h_{n1} & \cdots & h_{nn} & h_{n,n+1} & h_{n,n+2} \\ h_{n+1,1} & \cdots & h_{n+1,n} & h_{n+1,n+1} & h_{n+1,n+2} \\ h_{n+2,1} & \cdots & h_{n+2,n} & h_{n+2,n+1} & h_{n+2,n+2} \end{bmatrix}.$$

Since $i_{n+2} = 0$, we remove the column $n + 2$ of the hybrid matrix $\boldsymbol{H}$. Moreover, we remove $(n + 1)$-st equation of the hybrid representation because we are not interested in current i_{n+1} and extract $(n + 2)$-nd equation. As a result, we obtain

$$\boldsymbol{i} = \boldsymbol{M}\boldsymbol{v} + \begin{bmatrix} h_{1,n+1} \\ \vdots \\ h_{n,n+1} \end{bmatrix} y + \begin{bmatrix} s_1 \\ \vdots \\ s_n \end{bmatrix}, \tag{3}$$

$$v_0 = v_{n+2} = -\begin{bmatrix} h_{n+2,1} \cdots h_{n+2,n} \end{bmatrix} \boldsymbol{v} + h_{n+2,n+1}\, y + s_{n+2}, \tag{4}$$

where

$$\boldsymbol{i} = \begin{bmatrix} i_1 \\ \vdots \\ i_n \end{bmatrix}, \boldsymbol{v} = \begin{bmatrix} v_1 \\ \vdots \\ v_n \end{bmatrix}, \boldsymbol{M} = -\begin{bmatrix} h_{11} \cdots h_{1n} \\ \cdots\cdots\cdots\cdots \\ h_{n1} \cdots h_{nn} \end{bmatrix}.$$

Letting $z = [z_1 \cdots z_n]^{\mathrm{T}} = \boldsymbol{i}$, $\boldsymbol{x} = [x_1 \cdots x_n]^{\mathrm{T}} = \boldsymbol{v}$, $\boldsymbol{b} = \left[h_{1,n+1} \cdots h_{n,n+1}\right]^{\mathrm{T}}$, $\boldsymbol{q} = [s_1 \cdots s_n]^{\mathrm{T}}$, where T denotes transposition, we rewrite Eq. (3) in the form

$$\boldsymbol{z = q + b}y + \boldsymbol{M x}. \tag{5}$$

Since for each ideal diode, the relations (1) are fulfilled, we can write

$$\boldsymbol{x} \geq \boldsymbol{0}, \quad \boldsymbol{z} \geq \boldsymbol{0}, \quad \boldsymbol{z}^{\mathrm{T}}\boldsymbol{x} = 0. \tag{6}$$

To trace the multibranched characteristic $v_0 = f(y)$ for $y \in [0, Y]$, we propose an algorithm sketched in Sect. 3.

3 The Proposed Algorithm

Step1 Set $y = 0$ and write on the basis of (5) and (6)

$$\begin{aligned} &\boldsymbol{z} = \boldsymbol{q} + \boldsymbol{b} \cdot 0 + \boldsymbol{M x}, \\ &\boldsymbol{x} \geq \boldsymbol{0}, \quad \boldsymbol{z} \geq \boldsymbol{0}, \quad \boldsymbol{z}^{\mathrm{T}}\boldsymbol{x} = 0. \end{aligned} \tag{7}$$

Although $\boldsymbol{b} \cdot 0 = \boldsymbol{0}$, we retain this term in (7). The problem specified by (7) is called a linear complementarity problem (LCP) [5,7,27]. To solve this problem, we choose a positive vector $\boldsymbol{d} \in R^n$ such that $\boldsymbol{d} + \boldsymbol{q} > \boldsymbol{0}$, using the procedure described in [7], and define the homotopy [7,27]

$$\begin{aligned} &\boldsymbol{z}^{\mathrm{T}}\boldsymbol{x} = 0, \quad \boldsymbol{x} \geq \boldsymbol{0}, \quad \boldsymbol{z} \geq \boldsymbol{0}, \\ &\boldsymbol{z} = \boldsymbol{p} - \lambda \boldsymbol{d} + \boldsymbol{b} \cdot 0 + \boldsymbol{M x}, \end{aligned} \tag{8}$$

where $\boldsymbol{p} = \boldsymbol{d} + \boldsymbol{q} > \boldsymbol{0}$ and λ is a variable. At $\lambda = 0$ Eq. (8) reduces to $\boldsymbol{z} = \boldsymbol{p} + \boldsymbol{M x}$ and the solution $\boldsymbol{x} = \boldsymbol{0}$ ($\boldsymbol{z} = \boldsymbol{p} > \boldsymbol{0}$) of the homotopy system is obtained. At $\lambda = 1$, we have the original LCP (7). To trace the homotopy path and find the solution, we combine the homotopy approach with Lemke's method as described in [7,27]. During

the computation process, we execute the same operations on both terms $\boldsymbol{p}$ and $\boldsymbol{b}$, although the last one does not affect the solution. On any stage of the procedure, some elements of vectors $\boldsymbol{z}$ and $\boldsymbol{x}$ are interchanged and $\boldsymbol{q}$, $\boldsymbol{b}$, and $\boldsymbol{M}$ are rearranged. At the end, when $\lambda = 1$, we obtain an equation equivalent to (7)

$$\boldsymbol{w} = \hat{\boldsymbol{q}} + \hat{\boldsymbol{b}} \cdot 0 + \hat{\boldsymbol{M}}\boldsymbol{u}, \tag{9}$$

where vector $\boldsymbol{w}$ consists of some elements of vector $\boldsymbol{z}$ and some elements of vector $\boldsymbol{x}$, whereas $\boldsymbol{u}$ consists of their complements. Equation (9) has the solution $\boldsymbol{u} = \boldsymbol{0}$ ($\boldsymbol{w} = \hat{\boldsymbol{q}} > \boldsymbol{0}$). Next we use Eq. (4), where vector $\boldsymbol{v}$ is composed of all elements x_i selected from $\boldsymbol{u}$ and $\boldsymbol{w}$. As a result, we find voltage v_0 at $y = 0$. To find other possible solutions at $y = 0$, we continue the procedure as described in [27]. In this way, we can find several solutions at $y = 0$ and the corresponding descriptions of the form (9).

Step 2 Similarly, we find the solutions at $y = Y$. For this purpose, we modify Eq. (5)

$$\boldsymbol{z} = \tilde{\boldsymbol{q}} - \boldsymbol{b}\tilde{y} + \boldsymbol{M}\boldsymbol{x}, \tag{10}$$

where $\tilde{\boldsymbol{q}} = \boldsymbol{q} + \boldsymbol{b}Y$, set $\tilde{y} = 0$ and write on the basis of (10) and (6)

$$\begin{aligned} &\boldsymbol{z} = \tilde{\boldsymbol{q}} - \boldsymbol{b} \cdot 0 + \boldsymbol{M}\boldsymbol{x}\,, \\ &\boldsymbol{x} \geq \boldsymbol{0}\,, \quad \boldsymbol{z} \geq \boldsymbol{0}\,, \quad \boldsymbol{z}^{\mathrm{T}}\boldsymbol{x} = 0\,. \end{aligned} \tag{11}$$

Repeating the approach described in Step 1, we find the solutions at $\tilde{y} = 0$ (or $y = Y$).

Step 3 Form a new homotopy corresponding to the first solution provided by Step 1 (using (9)) with new homotopy parameter $\lambda = y$, as follows:

$$\begin{aligned} &\boldsymbol{w}^{\mathrm{T}}\boldsymbol{u} = 0\,, \quad \boldsymbol{u} \geq \boldsymbol{0}\,, \quad \boldsymbol{w} \geq \boldsymbol{0}\,, \\ &\boldsymbol{w} = \hat{\boldsymbol{q}} + \hat{\boldsymbol{b}}\lambda + \hat{\boldsymbol{M}}\boldsymbol{u}. \end{aligned} \tag{12}$$

At $\lambda = y = 0$, the solution of (12) is known. We apply again the method being a combination of the homotopy approach and the Lemke method [7,27] adapted to (12). Each step of this procedure leads to such value of $\lambda = y$ that one of the complementary pairs is $x_k = 0$, $z_k = 0$. It corresponds to a breakpoint of the piecewise-linear characteristic. To find this breakpoint, we select all $x_i \quad (i = 1, \ldots, n)$, create the vector $\boldsymbol{v} = [x_1 \cdots x_n]^{\mathrm{T}}$ and use (4) to find v_0 at this breakpoint. To find other branches of the characteristic, we repeat the described approach taking into account in succession all the solutions found in Step 1 of the algorithm. In this way, all the branches which start from $\lambda = y = 0$ are traced.

Step 4 Repeat the approach described in Step 3 for (10) with $\lambda = \tilde{y}$ starting in succession from these solutions obtained in Step 2 which have not been found in Step 3. As λ is increased, $y = Y - \tilde{y}$ decreases.

This step is applied to find the possible branches which cannot be traced starting with $y = 0$, like the branch (c) in Fig. 6.

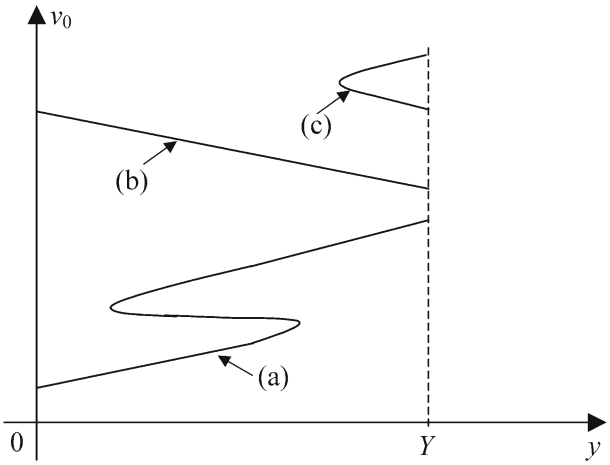

Fig. 6 Characteristic $y - v_0$ consisting of three branches (a), (b), and (c)

4 Circuit Example

The proposed method has been implemented in MATLAB 2012a and tested using PC Pentium i7-2600, 4GB.

Example 1 Let us consider the BJT circuit shown in Fig. 7, being a connection of the flip–flop circuit and the line receiver. Nominal values of the resistors are indicated in this figure. The parameters of the Ebers–Moll model of the transistors are as follows: $\alpha_{\mathrm{F}} = 0.99, \alpha_{\mathrm{R}} = 0.5$, $I_{\mathrm{ES}} = 7.07$ fA, $I_{\mathrm{CS}} = 14.00$ fA, $V_{\mathrm{T}} = 25.86$ mV, $R_{\mathrm{E}} = 10\ \Omega$, $R_{\mathrm{C}} = 10\ \Omega$, and $R_{\mathrm{B}} = 3\ \Omega$. The emitter and collector diodes are modeled by the circuit shown in Fig. 2, with $N = 8$ and the following parameters

Emitter diode

$$\hat{R}_d = 25.308\ \mathrm{M}\Omega; \quad \hat{R}_1 = 11.044\ \mathrm{k}\Omega, \quad V_0^{(1)} = 0.475\ \mathrm{V}; \quad \hat{R}_2 = 2.060\ \mathrm{k}\Omega,$$
$$V_0^{(2)} = 0.535\ \mathrm{V}; \hat{R}_3 = 430\ \Omega, \quad V_0^{(3)} = 0.576\ \mathrm{V}; \quad \hat{R}_4 = 77.3\ \Omega,$$
$$V_0^{(4)} = 0.618\ \mathrm{V}; \hat{R}_5 = 13.4\ \Omega, \quad V_0^{(5)} = 0.665\ \mathrm{V}; \quad \hat{R}_6 = 2.34\ \Omega,$$
$$V_0^{(6)} = 0.711\ \mathrm{V}; \quad \hat{R}_7 = 0.54\ \Omega, \quad V_0^{(7)} = 0.749\ \mathrm{V}.$$

Collector diode

$$\hat{R}_d = 19.752\ \mathrm{M}\Omega; \quad \hat{R}_1 = 16.256\ \mathrm{k}\Omega, \quad V_0^{(1)} = 0.445\ \mathrm{V}; \quad \hat{R}_2 = 2.885\ \mathrm{k}\Omega,$$
$$V_0^{(2)} = 0.510\ \mathrm{V}; \quad \hat{R}_3 = 428\ \Omega, \quad V_0^{(3)} = 0.554\ \mathrm{V}; \quad \hat{R}_4 = 76.3\ \Omega, \quad V_0^{(4)} = 0.600\ \mathrm{V};$$
$$\hat{R}_5 = 13.8\ \Omega, \quad V_0^{(5)} = 0.648\ \mathrm{V}; \quad \hat{R}_6 = 2.26\ \Omega, \quad V_0^{(6)} = 0.694\ \mathrm{V};$$
$$\hat{R}_7 = 0.53\ \Omega, \quad V_0^{(7)} = 0.732\ \mathrm{V}.$$

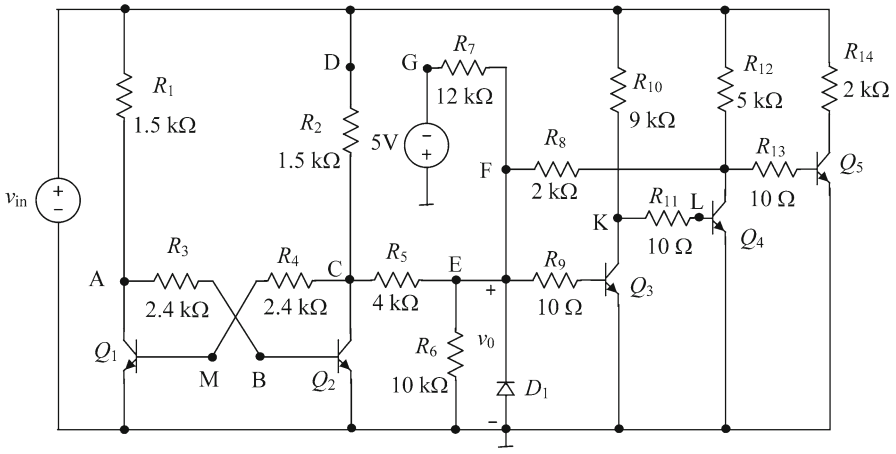

Fig. 7 BJT circuit for Example 1

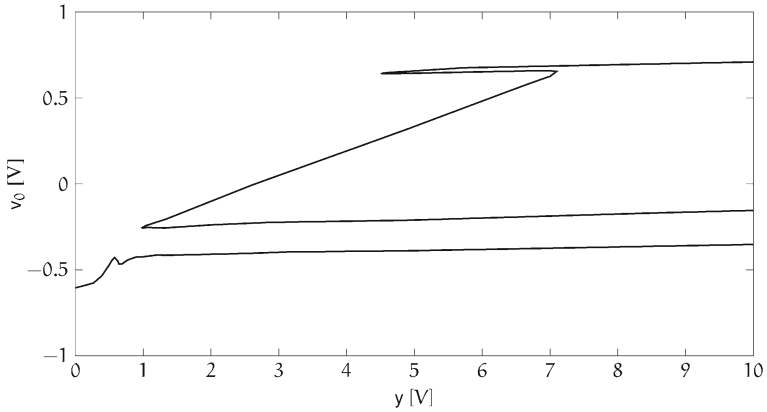

Fig. 8 Input–output characteristic obtained using the method described in Sect. 2

The diode D_1 is represented by the same model as the emitter diode with the series resistance equal to 4 Ω.

In this circuit, we trace the input–output characteristic $v_0 = f(y)$, where $y = v_{\text{in}}$. For the nominal values of the resistors, we obtain the multivalued and multibranched characteristic shown in Fig. 8. The time consumed by the method is 0.32 s.

To verify this characteristic we use the brute-force method [25] enabling us to find all the solutions of the circuit for any value of the input voltage without any piecewise-linear approximation. Plot of the characteristic obtained in this way is identical as the one provided by the proposed method. On the other hand the characteristic traced by PSPICE simulator, using up and down DC sweep analyses, is depicted in Fig. 9. A comparison of the characteristics manifests that PSPICE gives a fragmentary characteristic. Figure 10 shows a family of the characteristics traced by the proposed method

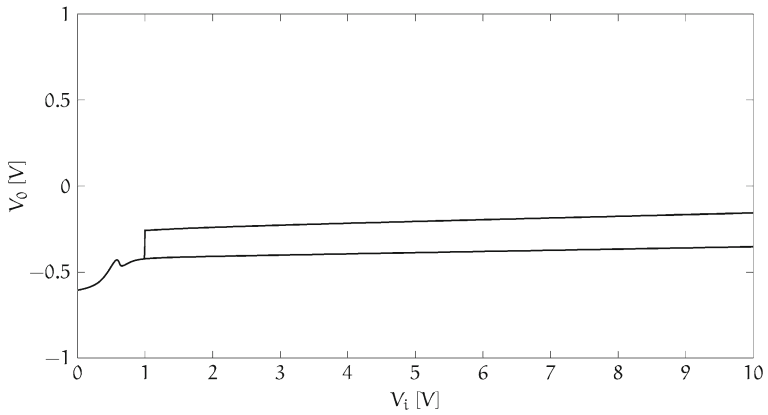

Fig. 9 Input–output characteristic obtained using SPICE simulator

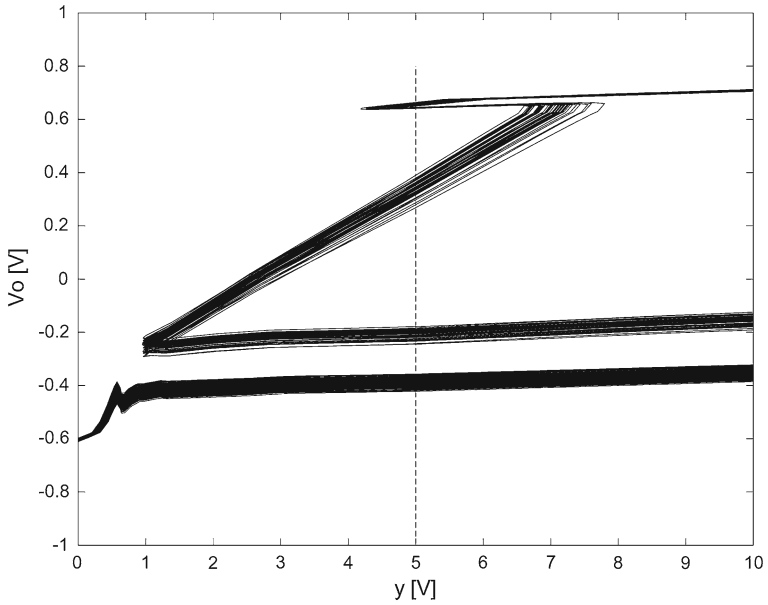

Fig. 10 Banded input–output characteristic

for 100 sets of the parameters values $\{R_1, \ldots, R_{14}\}$. They are obtained by random selection from their tolerance ranges ($\pm 5\%$), assuming uniform distribution.

The algorithm above-discussed can be adapted to the circuits containing MOS transistors, characterized by the Shichman-Hodges model built in Level 1 of SPICE [17]. For this purpose, the equivalent model, described in [22,27] having the structure similar to the Ebers–Moll model of bipolar transistors, should be applied.

Table $\boldsymbol{F}$

		Ranges of v_0 variation			
k	y_k	F_0	F_1	· · ·	F_M
0	y^-				
1	$y^- + h$				
2	$y^- + 2h$				
· · ·	· · ·	· · ·	· · ·	· · · · · ·	· · ·
N	y^+				

Fig. 11 Structure of table $\boldsymbol{F}$

5 The Fault Dictionary

A method of building a fault dictionary for catastrophic fault diagnosis of circuits containing bipolar and MOS transistors, having multiple DC operating points, is developed in this section. The method is based on input–output characteristics of the circuit under test, traced for all considered catastrophic faults and fault-free circuit. Every time the deviations of the circuit parameters within their tolerance ranges are considered.

For fault-free circuit and for each circuit with a single fault, we trace a family of the input-output characteristics $v_0 = f(y)$ for different values of the circuit parameters randomly selected from their tolerance ranges assuming uniform distribution. If the number of faults is M, we obtain $M + 1$ families of the characteristics. Each of the families has banded branches like the characteristic depicted in Fig. 10. We choose an interval $[y^-, y^+]$ of y, divide it into N equal subintervals and consider the points $y_k = y^- + kh, h = (y^+ - y^-)/N, k = 0, 1, \ldots, N$ of this interval. For any of the families of characteristics, we find and store the ranges of v_0 variation at all these points. For example, in the case shown in Fig. 10 at $y = 5$ V, we obtain four ranges of v_0 variation: $[-0.421, -0.357]$, $[-0.245, -0.179]$, $[0.268, 0.390]$, and $[0.642, 0.664]$, all in volts. The results are summarized in a table having the structure shown in Fig. 11, labeled $\boldsymbol{F}$, where $F_i, i = 1, \ldots, M$, denotes ith fault and F_0 means fault-free circuit.

In the place specified by ith row $(i \in \{0, 1, \ldots, N\})$ and jth column $(j \in \{0, 1, \ldots, M\})$, the ranges of v_0 variation at $y_i = y^- + ih$ in the circuit with fault F_j are stored. On the basis of table $\boldsymbol{F}$, we create $N + 1$ tables labelled $T_0, T_1, \ldots, T_N$ having the structure shown in Fig. 12. Each of the tables exploits the information contained in one row of table $\boldsymbol{F}$. For example, table T_l takes into account the information contained in lth row of table $\boldsymbol{F}$, where the ranges of v_0 variation at $y_l = y^- + lh$ are stored for all faults and fault-free circuit. The blank spaces of T_l in Fig. 12 are filled in as follows. At the crossing of ith row, corresponding to F_i $(i \in \{0, \ldots, M - 1\})$ and jth column corresponding to F_j $(j \in \{1, \ldots, M\}, j > i)$, we insert 1 if the ranges of v_0 variation for faults F_i and F_j (at $y_l = y^- + lh$) have a common part, or 0 otherwise.

Table T_l

F_0	F_1	F_2	$\cdots$	F_{M-1}	F_M
F_0			$\cdots$		
	F_1		$\cdots$		
		F_2	$\cdots$		
			$\cdots$	F_{M-1}	

Fig. 12 Structure of table T_l

Next we consider tables T_0 and T_1 and form a new table T_{01} as follows. If in table T_0, the element which appears in ith row ($i \in \{0, \ldots, M-1\}$) and jth column ($j \in \{1, \ldots, M\}$, $j > i$) equals 1 and in table T_1, the element located in the same place equals 0, then in table T_{01} the element equal to zero is inserted in this place. Otherwise, the element of table T_0 is transferred invariable to table T_{01}. Similarly, we consider other pairs of the tables: T_0 and $T_2, \ldots, T_0$ and T_N and create tables $T_{02}, \ldots, T_{0N}$. This procedure is continued leading to tables: $T_{12}, \ldots, T_{1N}, \ldots, T_{N-1,N}$.

If at any stage of this procedure, a table having all entries equal to zero arises, the algorithm is terminated and a fault dictionary enabling us to identify all the considered faults is built. Let table T_s ($s \in \{0, 1, \ldots, N\}$) have all elements equal to zero. Then at point $y_s = y^- + sh$ (corresponding to this table) all ranges of v_0 variation relating to all the faults are disconnected (no of them overlaps other one). Thus, having the value of the measured tested voltage $v_0 = \tilde{v}_0$ at this point, we take into account sth row of table $\boldsymbol{F}$ and find such column j that $\tilde{v}_0$ belongs to a range located in sth row and jth column. Index j defines the fault F_j. In this case, the fault dictionary consists of sth row of table $\boldsymbol{F}$. If table T_{pr} contains all elements equal to zero, the fault dictionary consists of pth and rth rows of table $\boldsymbol{F}$. If none of the tables is satisfactory (the sum of the entries is not sufficiently small), we can repeat the described above procedure taking into account for each table T_{ij} the tables T_m ($m \neq i, m \neq j$) and create tables T_{ijm}. This procedure can be continued as long as the sum of the entries decreases. Otherwise, the procedure terminates. Since the applied model of transistor employs the piecewise-linear approximated characteristics (Fig. 2), the obtained regions of the output voltage variation appeared in the fault dictionary are corrected. For this purpose, the original transistor model is used, with the smooth characteristics described in Fig. 1, and the Newton–Raphson algorithm applied.

Suppose that the built dictionary consists of two rows of table $\boldsymbol{F}$. Then in order to detect and identify the actual fault, we find all regions of v_0 variation at the first of the rows which include the measured voltage (at the point corresponding to this row) and form a set of the corresponding potential faults. Similarly we treat the second of the rows. As a result, we obtain two sets of potential faults and choose the common part of the sets. If the fault dictionary has been built on the basis of a table having some entries equal to one, the corresponding faults may be distinguishable or undistinguishable as explained in Example 4.

		Ranges of v_0 variation in volts			
k	y_k [V]	F_0	F_1	F_2	F_3
7	0.70	-0.4997 – -0.4194	-0.3805 – -0.3019	-0.2794 – -0.2081	-0.6047 – -0.5920
28	2.80	-0.4336 – -0.3712 -0.2646 – -0.1967 -0.0268 – 0.0585	-0.0241 – 0.0556	0.2774 – 0.3914 0.6277 – 0.6488	-0.5777 – -0.5301

		Ranges of v_0 variation in volts			
k	y_k [V]	F_4	F_5	F_6	F_7
7	0.70	0.0727 – 0.0786 0.2281 – 0.2470 0.5282 – 0.6192 0.6660 – 0.6759	-0.5464 – -0.4621	-0.3683 – -0.2937	-0.3769 – -0.2889
28	2.80	0.0541 – 0.0579 0.2319 – 0.2579 0.5127 – 0.5806 0.6269 – 0.6299 0.6627 – 0.6666	-0.0944 – -0.0238 0.0854 – 0.1556 0.3338 – 0.4238	-0.3071 – -0.2210	-0.2130 – -0.1296

Fig. 13 Fault dictionary for Example 2

6 Numerical Examples

Example 2 Let us consider the BJT circuit shown in Fig. 7. The transistors models and the circuit parameters are as described in Example 1.

We want to diagnose fault-free circuit (F_0) and $M = 7$ catastrophic faults: cuts of the branches AB (F_1), CE (F_3), FG (F_4), KL (F_5), and short-circuits of the pairs of points CD (F_2), BM (F_6), AM (F_7). To build the fault dictionary, the procedure described in Sect. 5 has been applied. We trace eight families of input–output characteristics $v_0 = f(y)$, where $y = v_{in} \in [0, 10]$ V with $h = 0.1$ V, as described in Sect. 3. To compute each of the families, 100 sets of the parameters values $\{R_1, \ldots, R_{14}\}$ are randomly selected, assuming uniform distribution, within the tolerance ranges $\pm 5\%$. The size of table $\boldsymbol{F}$ is 101×8. We perform the procedure described in this section and find table T_{ij}, where $i = 7$, $j = 28$ having one entry equal to 1, appeared in row 0 and column 5. The index $i = 7$ corresponds to $v_{\text{in}} = 0.70$ V, whereas $j = 28$, $v_{in} = 2.80$ V. Hence, the fault dictionary consists of the rows 7 and 28 of table $\boldsymbol{F}$ as shown in Fig. 13. It allows identifying all the discussed catastrophic faults except F_0 and F_5, which may be undistinguishable or distinguishable. To verify the proposed method, the circuit was built using 5 % tolerance resistors and several catastrophic faults were considered experimentally. Two of them are described below. In the case of fault F_6, the measured voltages were -0.328 V for the input voltage $y = 0.7$ V and -0.230 V for $y = 2.8$ V. They allow identifying the fault correctly. In another fault F_5, the measured voltages were: -0.523 and -0.093 V, respectively, leading to correct diagnosis.

The most time-consuming part of the algorithm is tracing input–output characteristics for each of the circuit states considering a large number of sets of the parameters values. Average time of tracing one input–output characteristic is 0.32 s. Since the

number of the families of the characteristics, for fault-free circuit and 7 catastrophic faults, is 8 and each of them consists of 100 characteristics corresponding to 100 sets of the parameters values, the total number of the characteristics is 800. Hence, the time consumed for their tracing is 256 s = 2.27 min. This time dominates the others, used for selecting the test voltages (62 s) and correcting the voltage ranges using the Newton–Raphson algorithm (2.8 s).

Example 3 Consider the operational amplifier-based Schmitt trigger shown in Fig. 14, where the Ebers–Moll model parameters of the transistors are as in Example 1. The emitter and collector diodes are modeled by the circuit shown in Fig. 2, with $N = 4$ and the following parameters:

Emitter diode

$$\hat{R}_d = 3250\ \text{M}\Omega; \quad \hat{R}_1 = 51.5022\ \Omega, \quad V_0^{(1)} = 0.61\ \text{V}; \quad \hat{R}_2 = 11.5745\ \Omega,$$
$$V_0^{(2)} = 0.672\ \text{V}; \quad \hat{R}_3 = 4.7551\ \Omega, \quad V_0^{(3)} = 0.7077\ \text{V}.$$

Collector diode

$$\hat{R}_d = 2663\ \text{M}\Omega; \quad \hat{R}_1 = 54.2765\ \Omega, \quad V_0^{(1)} = 0.6\ \text{V}; \quad \hat{R}_2 = 11.0595\ \Omega,$$
$$V_0^{(2)} = 0.6651\ \text{V}; \quad \hat{R}_3 = 4.0290\ \Omega, \quad V_0^{(3)} = 0.7000\ \text{V}.$$

We want to diagnose fault-free circuit (F_0) and $M = 9$ catastrophic faults: cuts of the branches DJ (F_1), BC (F_2), and short-circuits of the pairs of points HI (F_3), CK (F_4), GL (F_5), AL (F_6), IL (F_7), EL (F_8), and FM (F_9). To build the fault dictionary, the procedure described in Sect. 5 has been applied. We trace 10 families of the input–output characteristics $v_0 = f(y)$, where $y = v_{\text{in}} \in [0, 10]$ V, with $h = 0.2$ V. To create each of the families, 100 sets of the parameters values $\{R_1, \ldots, R_8\}$ are randomly selected, assuming uniform distribution within the tolerance limits $\pm 5\,\%$. The size of table $\boldsymbol{F}$ is 51×10. Performing the procedure described in Sect. 5, we find Table T_0, having all elements equal to zero. The corresponding input–output voltage is $v_{\text{in}} = 0$ V. Hence, the fault dictionary consists of the row 0 of the table $\boldsymbol{F}$, as shown in Fig. 15. It allows identifying all the aforementioned catastrophic faults.

Average time of tracing one input–output characteristic of the circuit shown in Fig. 14 is 7.6 s. Since the number of the families of the characteristics, for fault-free circuit and 9 catastrophic faults, is 10 and each of them consists of 100 characteristics corresponding to 100 sets of the parameters values, the total number of the characteristics is 1,000. Hence, the time consumed for their tracing is 126.7 min. This time dominates the others, used for selecting the test voltages (42 s) and correcting the voltage ranges using the Newton–Raphson algorithm (101 s). The total time is 129 min., but it is the off-line operation.

Although the proposed diagnostic method has been explained in detail for BJT circuits, it can be directly adapted to MOS circuits characterized by the Shichman–Hodges model built in Level 1 of SPICE [17]. It can be shown [22,27] that this model is equivalent to the circuit having the structure of the Ebers–Moll model of bipolar

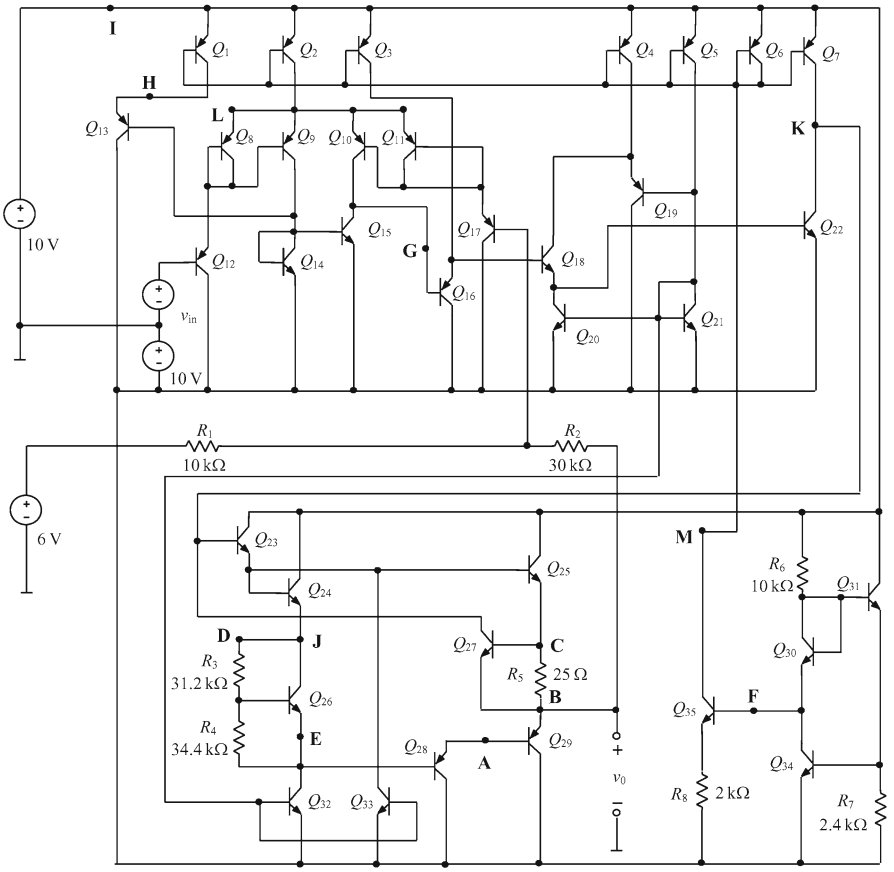

Fig. 14 Circuit for Example 3

		Ranges of v_0 variation in volts				
k	y_k [V]	F_0	F_1	F_2	F_3	F_4
0	0	8.8212 – 8.8261	-8.3853 – -8.3567	7.0295 – 7.1862	-9.2831 – -9.2751	-8.8165 – -8.8119

		Ranges of v_0 variation in volts				
k	y_k [V]	F_5	F_6	F_7	F_8	F_9
0	0	-9.2983 – -9.2922	-9.2694 – -9.2625 1.2833 – 1.2843 2.1850 – 2.2150	-9.2567 – -9.2478	2.9711 – 3.0134	-5.3324 – -5.3022

Fig. 15 Fault dictionary for Example 3

transistors, with the gains of the controlled sources $\alpha_F = \alpha_R = 1$ and the diodes described by the equations

$$i_1 = i_{\mathrm{EF}} = \begin{cases} k(v_{\mathrm{gs}} - |v_{t_0}|)^2 & \text{for } v_{\mathrm{gs}} \geq \begin{vmatrix} v_{t_0} \\ v_{t_0} \end{vmatrix} \\ 0 & \text{for } v_{\mathrm{gs}} < \begin{vmatrix} v_{t_0} \\ v_{t_0} \end{vmatrix} \end{cases},$$

$$i_2 = i_{\mathrm{CF}} = \begin{cases} k(v_{\mathrm{gd}} - |v_{t_0}|)^2 & \text{for } v_{\mathrm{gd}} \geq \begin{vmatrix} v_{t_0} \\ v_{t_0} \end{vmatrix} \\ 0 & \text{for } v_{\mathrm{gd}} < \begin{vmatrix} v_{t_0} \\ v_{t_0} \end{vmatrix} \end{cases}.$$

In the above equations v_{t_0} is the threshold voltage, $k = \frac{K_p}{2}\frac{W}{L}$, where K_p is the transconductance parameter, W and L are the channel width and length, respectively. Using this model, we can apply the theory developed in this paper. In the case of MOS circuits, however, the circuit parameters are not resistances, but the threshold voltages v_{t_0} and the coefficients k, dissipated within their tolerance ranges.

Example 4 Let us consider the waveform-reshaping circuit [12] shown in Fig. 16. The nominal values of the channel width W and length L in μm are indicated in Fig. 16. Nominal values of the other parameters are as follows: PMOS$-K_p = 19.485\ \mu\mathrm{A/V}^2$, $v_{t_0} = -0.8351$ V, $R_d = 16.4\ \Omega$, $R_s = 16.4\ \Omega$, $R_g = 0$; NMOS$-K_p = 79.173\ \mu\mathrm{A/V}^2$, $v_{t_0} = 0.5705$ V, $R_d = 16.4\ \Omega$, $R_s = 16.4\ \Omega$, $R_g = 0$. Having W, L and K_p, the coefficient $k = \frac{K_p}{2}\frac{W}{L}$ can be calculated. In this circuit, we wish to detect and identify $M = 8$ catastrophic faults: cuts of the branches AB (F_1), EM (F_2), and short-circuits of the pairs of points HK (F_3), GA (F_4), MC (F_5), GH (F_6), HA (F_7), and LM (F_8), as well as fault-free circuit (F_0). MOS transistors are characterized by the model described above where the diodes are approximated by a piecewise-linear 8-segment functions (see Fig. 2). To build a fault dictionary, we trace families of the characteristics $v_0 = f(y)$, as described in Sect. 3, and consider $y = v_{in} \in [0.8, 4]$ V with $h = 0.1$ V. To compute each of the families, 20 sets of values of the parameters k and v_{t_0} are randomly selected assuming uniform distribution within the tolerance ranges $\pm 5\,\%$. The family corresponding to the fault-free circuit is shown in Fig. 17.

The size of the table $\boldsymbol{F}$ is 33×9. We perform the procedure described in Sect. 5 and find T_{17} having two entries equal to one, appeared in row 0 and column 3 and row 1 and column 6. It enables us to identify all the discussed faults except the fault-free circuit and the fault F_3, as well as F_1 and F_6, which may be undistinguishable, on the basis of the measured output voltages at $v_{\mathrm{in}} = 0.9$ V and $v_{\mathrm{in}} = 1.5$ V corresponding to table T_{17}. Hence, the fault dictionary consists of rows 1 and 7 of table $\boldsymbol{F}$, as illustrated in Fig. 18. This dictionary shows that faults F_0 and F_3 are undistinguishable, whereas F_1 and F_6 can be undistinguishable or distinguishable depending on the measured output voltages. For example, if $\tilde{v}_0 = 4.9998$ V at $v_{\mathrm{in}} = 0.9$ V then fault F_1 is identified. Average time of tracing one input–output characteristic of the circuit shown in Fig. 16 is 1.4 s. Since the number of the families of the characteristics, for fault-free circuit and 8 catastrophic faults, is 9 and each of them consists of 20 characteristics corresponding to 20 sets of the parameters values, the total number of the characteristics is 180. Hence, the time consumed for their tracing is 252 s = 4.2 min. This time dominates the others, used for selecting the test voltages (12 s) and correcting the voltage ranges using the Newton–Raphson algorithm (6.8 s).

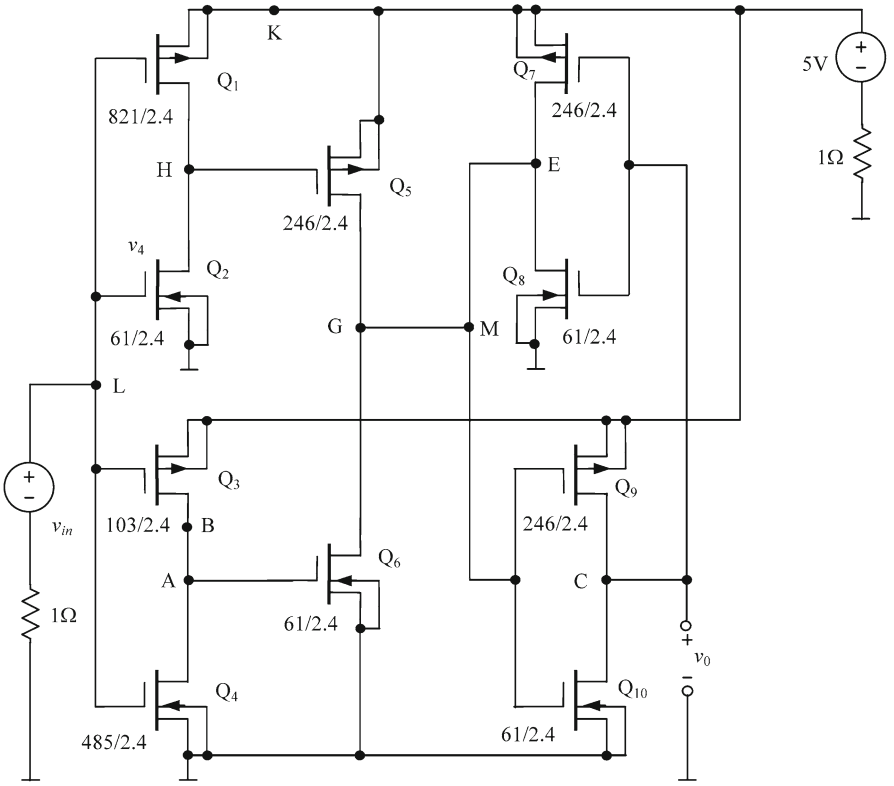

Fig. 16 MOS circuit for Example 4

7 Discussion and Concluding Remarks

This paper is focused on catastrophic fault diagnosis of nonlinear circuits containing bipolar and MOS transistors using simulation-before-test approach. Unlike the other works which deal with the circuits having a unique operating point, this paper, for the first time, is devoted to the circuits having multiple operating points (DC solutions).

The proposed approach to the problem of fault diagnosis of analog circuits has a general meaning, because a catastrophic fault changes the circuit topology and forms a new circuit. The faulty circuit may possess multiple DC solutions, even if the original circuit has a unique solution. For example, the universal preamplifier circuit with the test voltage source $v_{\text{in}} = 0.8$ V connected to the node accessible for excitation, shown in Fig. 19 with the following transistors parameters: $\alpha_F = 0.9975$, $\alpha_R = 0.8$, $I_{\text{ES}} = 10.22$ fA, $I_{\text{CS}} = 12.75$ fA, $V_{\text{T}} = 25.86$ mV, $R_{\text{E}} = 0.81\ \Omega$, $R_{\text{C}} = 0.33\ \Omega$, and $R_{\text{B}} = 3.3\ \Omega$, has a unique DC solution $v_0 = 19.473$ V at $v_{\text{in}} = 0.8$ V. However, if the catastrophic fault, being short-circuit of points AB, occurs then the circuit possesses three DC solutions $v_0^{(1)} = 0.438$ V, $v_0^{(2)} = 10.052$ V, and $v_0^{(3)} = 19.473$ V at the same input voltage $v_{in} = 0.8$ V. In the real circuit built for verification purpose, with

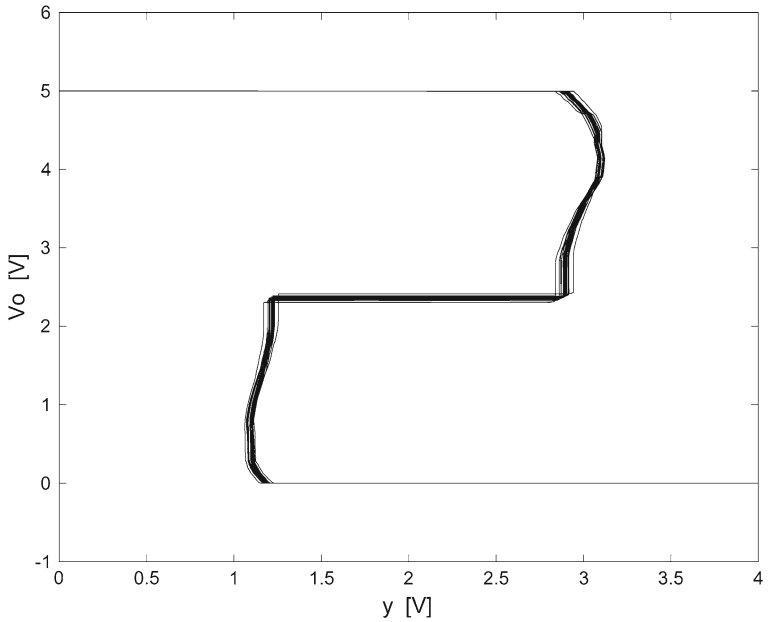

Fig. 17 Family of the characteristics of fault-free circuit shown in Fig. 16

		Ranges of v_0 variation in volts				
k	y_k [V]	F_0	F_1	F_2	F_3	F_4
1	0.9	4.9989 – 4.9992	0.0000 – 0.0000 2.3056 – 2.4149 4.9998 – 4.9998	4.9989 – 4.9992	4.9989 – 4.9992	0.0288 – 0.0456 2.2831 – 2.4839 4.9954 – 4.9958
7	1.5	0.0000 – 0.0000 2.3040 – 2.4131 4.9963 – 4.9965	0.0000 – 0.0000 2.3053 – 2.4146 4.9991 – 4.9991	0.8551 – 1.1790	0.0000 – 0.0000 2.3040 – 2.4131 4.9963 – 4.9965	0.1858 – 0.2682 1.2568 – 1.6019 4.9963 – 4.9965

		Ranges of v_0 variation in volts			
k	y_k [V]	F_5	F_6	F_7	F_8
1	0.9	1.6228 – 1.7268	0.0000 – 0.0000	4.9989 – 4.9992	4.9751 – 4.9841
7	1.5	2.3040 – 2.4131	0.0000 – 0.0000	4.9930 – 4.9940	4.7804 – 4.8297

Fig. 18 Fault dictionary for Example 4

5% tolerance resistors, the measurements gave two output voltages: $v_0^{(1)} = 0.452$ V and $v_0^{(3)} = 19.460$ V.

The input–output characteristic $v_0 = f(v_{\text{in}})$ of the original circuit depicted in Fig. 20a is a single-valued curve, whereas the characteristic of the faulty circuit, shown in Fig. 21a is a multivalued curve. These characteristics obtained experimentally are shown in Figs. 20b and 21b. Since usually we do not know whether the circuit possesses multiple DC solutions, the fault dictionary should be built using a method which allows finding multiple solutions. Such a method works correctly also in the case of a unique

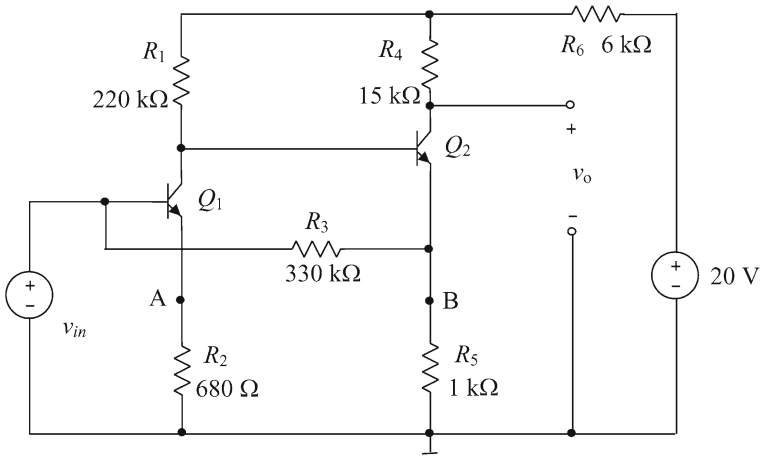

Fig. 19 Circuit possessing a unique DC solution

solution. The approach developed in this paper fulfills this requirement and leads to reliable results. This is the main achievement of this paper.

Fault diagnosis of the circuits possessing multiple solutions is much more complex and requires larger computing power. This is why the CPU time is much longer than in the case of circuits having a unique solution. Although the method developed in this paper for tracing input–output characteristics is very efficient, necessity of finding a great number of the characteristics makes the diagnostic approach time-consuming. Fortunately, in the applied simulation-before-test approach this is the off-line operation. Consequently, the CPU time is not as crucial as in the simulation after test approach. The method is based on the concept of linear complementarity problem and is an extension of the idea presented in reference [27] devoted to finding multiple DC operating points. Since tracing multivalued and multibranched characteristics is a basic problem of the analysis of nonlinear dynamic circuits [15] the method is a contribution to nonlinear circuit theory.

The fault dictionary, built using the proposed approach, allows detecting and identifying the faults on the basis of a diagnostic test, which usually exploits measurements at one accessible node only. The method does not make very restricted demands about accuracy of the measurements. If the obtained fault dictionary is not satisfactory another testing node should be taken and the procedure repeated.

The algorithm of the fault diagnosis, proposed in this paper, does not accept the node approach, which is commonly used in user-oriented circuit analysis programs, including SPICE. Instead, it exploits the hybrid analysis [4] to formulate the linear complementarity problem. The hybrid representation of electronic circuits is employed in almost all methods which allow finding all the DC solutions and is required by many other methods in this field.

The proposed algorithm is difficult to implementation in a computer program, what is a disadvantage. In addition the Level 1 transistors models have to be used and their piecewise-linear representations exploited. Transistors of CMOS circuits manufac-

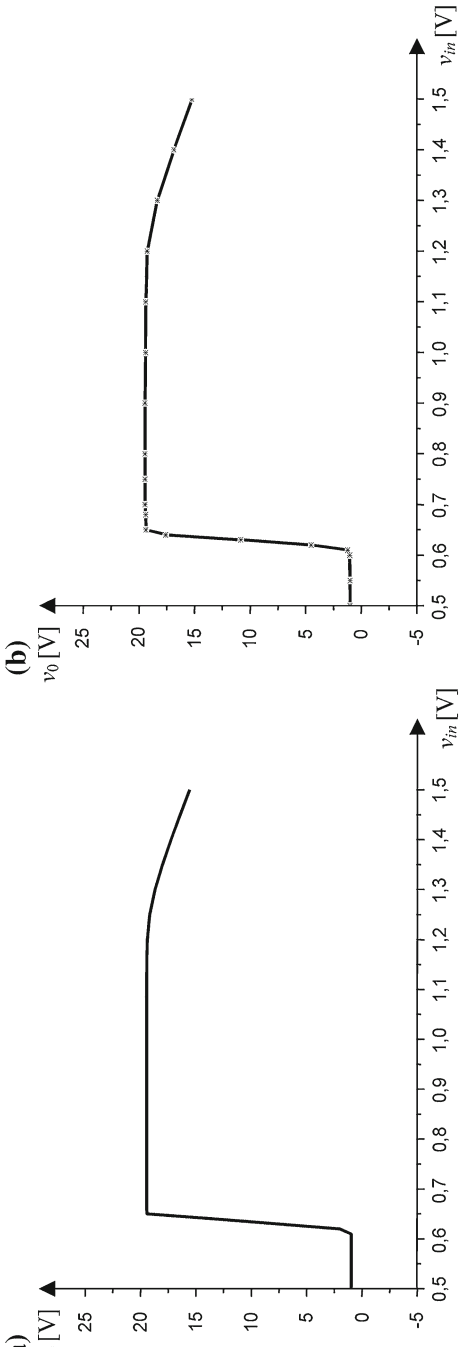

Fig. 20 Input–output characteristic of the circuit shown in Fig. 19 traced numerically (**a**) and experimentally (**b**)

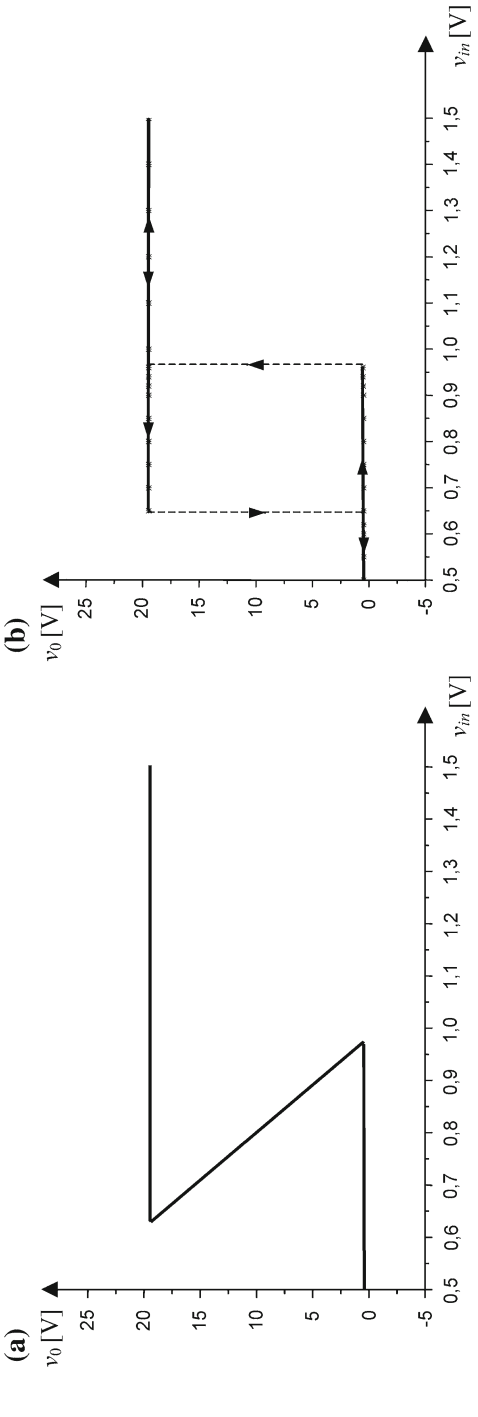

Fig. 21 Input–output characteristic of the faulty circuit traced numerically (**a**) and experimentally (**b**)

tured in nanometer technology should be characterized by very complex BSIM 4 or PSP 103 model. Each of these models is specified by several hundred equations, mostly nonlinear. Methods for tracing input–output characteristics applied to this class of circuits are very time-consuming and inefficient. Since the proposed approach needs huge number of the characteristics, it is not suitable for fault diagnosis of CMOS circuits manufactured in nanometer technology.

Because in the circuit having multiple DC operating points, we do not know in advance to which region of the output voltage variation belongs the measured voltage we consider all of them. In some cases, it is possible to identify the fault, even if the ranges corresponding to this fault and another one have common parts. The approach can be also useful for generating the training data for neural networks if they are used as the fault classifiers.

References

1. F. Aminian, M. Aminian, Fault diagnosis of analog circuits using bayesian neural networks with wavelet transform as preprocesor. J. Electron. Test. **17**, 29–36 (2001)
2. M. Aminian, F. Aminian, A modular fault-diagnosis system for analog electronic circuits using neural networks with wavelet transform as a preprocesor. IEEE Trans. Instrum. Meas. **56**, 1546–1554 (2007)
3. L.O. Chua, A.C. Deng, Canonical piecewise linear analysis: part II-tracing driving-point and transfer characteristics. IEEE Trans. Circuits Syst. **32**, 417–444 (1985)
4. L.O. Chua, P.M. Lin, *Computer-Aided Analysis of Electronic Circuits, Algorithm and Computational Techniques* (Prentice Hall, Ehglewood Cliffs, 1975)
5. R.W. Cottle, J.S. Pang, R.E. Stone, *The Linear Complementarity Problem* (Academic, New York, 1992)
6. M. El-Gamal, M.D.A. Mohamed, Ensembles of neural networks for fault diagnosis in analog circuits. J. Electron. Test. **23**, 323–339 (2007)
7. C.B. Garcia, W.I. Zangwill, *Pathways to Solutions, Fixed Points, and Equilibria*, Series in Computational Mathematics (Prentice-Hall, New York, 1981)
8. D. Gizopoulos, *Advances in Electronic Testing. Challenges and Methodologies* (Springer, Dordrecht, 2006)
9. W. Hochwald, J.D. Bastian, A DC approach for analog fault dictionary determination. IEEE Trans. Circuits Syst. **26**, 523–529 (1979)
10. J.L. Huertas, in *Proceedings of the ECCTD, Test and Design for Testability of Analog and Mixed–Signal Integrated Circuits: Theoretical Basis and Pragmatical Approaches* (Elsevier, Amsterdam, 1993), pp. 75–151
11. P. Kabisatpathy, A. Barua, S. Sinha, *Fault Diagnosis of Analog Integrated Circuits* (Springer, Dordrecht, 2005)
12. D. Kim, J. Kih, W. Kim, A new waveform-reshaping circuit: an alternative approach to Schmitt trigger. IEEE J. Solid-State Circuits **28**, 162–164 (1993)
13. F. Li, P.Y. Woo, The invariance of node voltage sensitivity sequence and its application in a unified fault detection dictionary method. IEEE Trans. Circuits Syst. I **46**, 1222–1226 (1999)
14. B. Long, M. Li, H. Wang, S. Tian, Diagnostics of analog circuits based on LS-SVM using time domain features. Circuits Syst. Signal Process. **32**, 2683–2706 (2013)
15. M.J. Ogorzalek, Multivalued characteristics in electronic circuits: a unifying approach. IEEE Trans. Cir. Syst. II **47**, 726–735 (2000)
16. M. Peng, C.K. Tse, M. Shen, K. Xie, Fault diagnosis of analog circuits using systematic tests based on data fusion. Circuits Syst. Signal Process. **32**, 525–539 (2013)
17. T.L. Quarles, A.R. Newton, D.O. Pederson, A. Sangiovanni-Vincentelli, *SPICE-3, Versin 3F5 User's Manual* (Department of EECS, University of California, Berkeley, 1993)

18. J. Rutkowski, in *Proceedings of ECCTD, A DC Approach for Analog Fault Dictionary Determination* (Elsevier, Amsterdam, 1993), pp. 877–880
19. H.H. Schreiber, Fault dictionary based upon stimulus design. IEEE Trans. Circuits Syst. **26**, 529–537 (1979)
20. A.D. Spyronasios, M.G. Dimopoulos, A.A. Hatzopoulos, Wavelet analysis for the detection of parametric and catastrophic faults in mixed-signal circuits. IEEE Trans. Instrum. Meas. **60**, 2025–2038 (2011)
21. V. Stopjakova, P. Malosek, M. Matej, V. Nagy, M. Margala, Defect detection in analog and mixed circuits by neural networks using wavelet analysis. IEEE Trans. Reliab. **54**, 441–448 (2005)
22. M. Tadeusiewicz, Global and local stability of circuits containing MOS transistors. IEEE Trans. Circuits Syst. I **48**, 957–966 (2001)
23. M. Tadeusiewicz, S. Hałgas, Computing multivalued input-output characteristics in the circuits containing bipolar transistors. IEEE Trans. Circuits Syst. I **51**, 1859–1867 (2004)
24. M. Tadeusiewicz, S. Hałgas, A method for fast simulation of multiple catastrophic faults in analogue circuits. Int. J. Circuit Theor. Appl. **38**, 275–290 (2010)
25. M. Tadeusiewicz, S. Hałgas, Some contraction methods for locating and finding all the DC operating points of diode-transistors circuits. Int. J. Electron. Telecommun. **4**, 331–338 (2010)
26. M. Tadeusiewicz, S. Hałgas, M. Korzybski, Multiple catastrophic fault diagnosis of analog circuits considering the component tolerances. Int. J. Circuit Theor. Appl. **40**, 1041–1052 (2012)
27. M. Tadeusiewicz, A. Kuczyński, A very fast method for the DC analysis of diode-transistor circuits. Circuits Syst. Signal Process. **32**, 433–451 (2013)
28. A. Ushida, L.O. Chua, Tracing solution curves of non-linear equations with sharp turning points. Int. J. Circuit Theor. Appl. **12**, 1–21 (1984)
29. Y. Xiao, Y. He, A novel approach for analog fault diagnosis based on neural network and improved kernel PCA. Neurocomputing **74**, 1102–1115 (2011)
30. C.W. Yun, K.S. Chao, Simple solution curves of nonlinear resistive networks. Int. J. Circuit Theor. Appl. **11**, 47–55 (1983)