Analytical study of Dual Material Surrounding Gate MOSFET to suppress short-channel effects (SCEs)

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1. Introduction

Increased short-channel effects (SCEs) appear as a major roadblock to maintain the performance enhancement in conventional bulk Si MOSFETs with deca-nanometer technology node. According to ITRS [1], incorporation of new technologies is becoming crucial for deep sub-micron CMOS devices. Among different possible solutions, non-conventional MOSFET device structure employing the gate-material engineering [2] improves the gate transport efficiency by modifying the electric field pattern and the surface potential along the channel, resulting in higher carrier transport efficiency, higher transconductance and SCEs suppression. In 1999, a new type of FET structure, proposed by Long et al. [3] is that the dual-material gate (DMG) FET, employing “gate-material engineering” to improve both carrier transport efficiency and SCEs. The gate material with higher workfunction near the source end acts as the “control gate”, while the gate material with lower workfunction near the drain end acts as the “screening gate” that prevents any changes in the drain bias to affect the channel region under the first gate. In the DMG MOSFET, two metals M1 and M2 of different workfunction are amalgamated together laterally. The workfunction of M1 is greater than M2 i.e. $\Phi_{M1} > \Phi_{M2}$. Such a configuration introduces a step function in the potential along the channel such that the electric field distribution is enhanced at the source side to increase the carrier velocity while the drain potential change will be screened. Work function in M2 is chosen greater than M1 for a p-channel MOSFET and vice-versa for an n-channel MOSFET. In spite of the several benefits offered by gate-material engineering, the major issue of concern is the viability of fabrication. Recently, Sarkar et al. [4] has emphasized the challenges and current status of the fabrication of DMG MOSFET.

Recently, the multiple gate MOSFETs like Double-gate (DG) [5], triple gate [6], FINFET [7] and surrounding gate (SG) [8] MOSFETs has manifested themselves as the most popular candidate for nanoscale design for providing a better scalability option [9]. Excellent short channel effects (SCEs) immunity, high transconductance and near ideal subthreshold slope have been reported by many theoretical and experimental studies on this device [10].

A dual-material double-gate (DM-DG) SOI MOSFETS proposed by Reddy et al. [11] employs gate-material engineering to reduce SCEs significantly when compared to with the DG SOI MOSFET. To get further improvement against SCEs Tiwary et al. [12] proposed TM-DG MOSFET and also developed an analytical subthreshold model. It is inevitable that all variants of FinFETs will finally change to surrounding gate nanowire FETs, because of their best electrostatic gate-control, higher control of SCEs and larger channel area for the nanowire surface per unit area [13–15].
Yu et al. [16] reported an accurate 2-d analytical model of surrounding gate MOSFET using Bessel functions. On the other hand, surface- potential based model with moderate accuracy such as [17–19] uses the simple polynomial approximation of the potential profile to offer reduced computational burdens and is suitable for the circuit simulation and the device design as compared to Fourier series based approaches [20]. On the other hand, superposition technique based modeling approach was also reported [21], requiring a large computational burden. A computationally efficient modeling based on pseudo-2d approach using Gaussian box in circular coordinates was also proposed [22,23]. Recently Sharma et al. [24] reported a more accurate isomorphic polynomial potential distribution based modeling approach. However, in this study we have chosen parabolic potential based approach due to its simplicity and reduced computational complexity.

To incorporate the advantage of the gate engineering techniques combined with the structural advantage of surrounding gate MOSFET, a novel device structure called Dual Material Surrounding Gate (DMSG) MOSFET is proposed [25]. Later, Chiang et al. reported an analytical subthreshold model using superposition technique [26]. On the other hand, Wang et al. developed a model for triple material surrounding gate MOSFET using superposition method [27]. Another superposition based model was reported for cylindrical surrounding gate MOSFET [28]. Recently, parabolic potential approach based model of triple material surrounding gate MOSFET was also reported [19]. In this paper, an analytical subthreshold model has been developed to study the effect of gate engineering on surrounding gate MOSFET to reduce SCEs by modeling surface potential, Electric Field, threshold voltage and drain current. Moreover, the effect of radius downscaling on the device performance was observed has also been studied. The analytical modeling of DMSG MOSFET structure exhibits significantly enhanced performance in terms of threshold voltage roll-off and DIBL makes it a potential candidate for future generation n-MOSFET based circuits. The results are validated with numerical 2-D device simulation.

2. Model derivation

2.1. Device structure

Fig. 1 shows the 3-d structure of the DMSG n-channel MOSFET considered in this study. In this structure two different gate materials (M1 and M2) having different workfunctions (fM1 and fM2) with lengths L1 and L2 are amalgamated together to form the gate terminal with total gate length defined as L = L1 + L2. The gate materials are chosen in such a way (fM1 > fM2) so that the material with higher workfunction is kept near the source end functioning as the “control gate” and the material with lower workfunction is kept near the drain end to function as a “screen gate”. Gold (Au fM1 = 4.8 eV) and Cadmium (Cd) are used as two gate metals to from the gate terminal with their workfunctions 4.8 eV and 4.0 eV respectively. The p-type channel doping level is kept at 6 × 1016 cm⁻³ and for n⁺ source/drain regions doping region is chosen as 5 × 10¹⁹ cm⁻³ with an abrupt doping profile at the drain/source to channel edges. Hafnium dioxide (HfO2) is chosen as gate oxide material, in place of conventional SiO2 (3.9e0) due to its higher permittivity (22 ε0) due to its higher permittivity (22 ε0) due to its higher permittivity (22 ε0) due to its higher permittivity (22 ε0) due to its higher permittivity (22 ε0) due to its higher permittivity (22 ε0). In this study, the effect of gate engineering on surrounding gate MOSFET is studied using the subthreshold model of the device.

Neglecting the influence of mobile charge carriers and fixed trapped charges within the oxide, the 2-d Poisson’s equation before the onset of strong inversion can be written as [35]

\[
\frac{1}{r} \frac{\partial}{\partial r} \left( r \frac{\partial \phi(r,z)}{\partial r} \right) + \frac{\partial^2 \phi(r,z)}{\partial z^2} = \frac{qN_A}{\varepsilon_{Si}}
\]

Where N_A is the acceptor doping concentration of the thin silicon film in (cm⁻³), ε_Si is the relative permittivity of silicon, q is the unit electron charge (1.6 × 10⁻¹⁹Coulomb), \( \phi(r, z) \) is the 2D potential distribution in the channel, r is radius of the cylindrical Si film and z is the distance along the channel with reference to the source.

As proposed by Young [36] the potential profile in the axial direction, i.e., the z-dependence of \( \phi(r,z) \) can be approximated as simple parabolic function and can be written as

\[
\phi(r,z) = c_1(z) + c_2(z)r + c_3(z)r^2
\]

Where the arbitrary coefficients c₁(z), c₂(z) and c₃(z) are to be determined from the following boundary conditions;

1. Surface potential at \( r = R \) is a function of z only.

\[
\phi(R, z) = \phi_S(z)
\]

Where, \( \phi_S(z) \) is the surface potential at the Si/SiO₂ interface.

2. Due to radial symmetry the electric field in the center of the cylindrical channel is considered as zero.

![Fig. 1. 3-d structure of a dual material cylindrical surrounding gate MOSFET.](image-url)
\[ \frac{\partial \phi(r, z)}{\partial r} \bigg|_{r=R} = 0 \]  

(4)

3. The electric field at \( r = R \) (Si/SiO\(_2\) interface) is continuous.

\[ \frac{\partial \phi(r, z)}{\partial r} \bigg|_{r=R} = \frac{C_f}{\epsilon_{Si}} (V_{GS} - \phi_5(z) - V_{FB}) \]  

(5)

Where \( C_f = \epsilon_{ox} / [(R + t_{ox})] \) is the oxide capacitance (per unit area) for the cylindrical coaxial geometry with external radius equal to \((R + t_{ox})\) and internal radius equal to \( R \). \( V_{GS} \) is the gate to source voltage, \( V_{FB} \) is the flat band voltage, \( t_{ox} \) is the effective oxide thickness (in nm), \( \epsilon_{ox} \) is permittivity of the oxide.

4. Potential at the source end is

\[ \phi(0, 0) = \phi_b(0) = V_{bi} \]  

(6)

Where \( V_{bi} \) is the built-in potential between source and channel junction.

5. Potential at the drain end is

\[ \phi(L, 0) = \phi_S(L) = V_{bi} + V_{DS} \]  

(7)

Where \( L \) is the device channel length and \( V_{DS} \) is drain to source voltage.

By solving (3)–(5), we get arbitrary coefficients \( c_1(z), c_2(z) \) and \( c_3(z) \) to be

\[ c_1(z) = \phi_S(z) \left[ 1 + \frac{C_f R}{2 \epsilon_{Si}} \right] - \frac{C_f R}{2 \epsilon_{Si}} (V_{GS} - V_{FB}) \]  

(8a)

\[ c_2(z) = 0 \]  

(8b)

\[ c_3(z) = \frac{C_f}{2 \epsilon_{Si}} (V_{GS} - \phi_5(z) - V_{FB}) \]  

(8c)

So by substituting (8) into (2), the 2-D potential in the cylindrical surrounding gate may be expressed as follows

\[ \phi(r, z) = \phi_5(z) \left[ 1 + \frac{C_f R}{2 \epsilon_{Si}} \right] - \frac{C_f R}{2 \epsilon_{Si}} (V_{GS} - V_{FB}) + \frac{C_f}{2 \epsilon_{Si}} (V_{GS} - \phi_5(z)) \]  

\[ - V_{FB})^2 \]  

(9)

Substituting this value of \( \phi(r, z) \) from (9) in (1), a second order differential equation can be obtained as

\[ \frac{d^2 \phi_5(z)}{dz^2} - \lambda^2 \phi_5(z) = \beta \]  

(10)

Where \( \lambda^2 = 2C_f/\epsilon_{Si}R \) and \( \beta = qN_A/\epsilon_{Si} - \lambda^2 (V_{GS} - V_{FB}) \)

The solution of the differential equation in (10) is of the form.

\[ \phi_5(z) = A e^{\lambda z} + B e^{-\lambda z} - \frac{\beta}{\lambda^2} \]  

For the two regions under the gate material \( M_1 \) and \( M_2 \), the solution of the Poisson's equation can be written as

\[ \text{Region 1 : } \phi_{S1}(z) = A e^{\lambda z} + B e^{-\lambda z} - \frac{\beta_1}{\lambda^2} \text{ for } 0 \leq z \leq L_1 \]  

(12)

\[ \text{Region 2 : } \phi_{S2}(z) = C e^{\lambda z} + D e^{-\lambda z} - \frac{\beta_2}{\lambda^2} \text{ for } L_1 < z \leq (L_1 + L_2) \]  

(13)

The constant \( \beta_1 \) and \( \beta_2 \) are different for two different gate metals. The Flatband voltages for two different regions are given by

\[ V_{FB1} = \phi_{S1} - \phi_{Si} \]

\[ V_{FB2} = \phi_{S2} - \phi_{Si} \]

Where \( \phi_{S} \) denotes the workfunction of Silicon.

The differentiation of surface potential is carried out with respect to \( Z \) direction (along the channel) to obtained the distribution of the Electric Field given by

\[ E_{z1} = \frac{d\phi_{S1}(z)}{dz} = \left[ A e^{\lambda z} - B e^{-\lambda z} \left[ 1 - e^{-\lambda z} \right] \right] \]  

(14)

\[ E_{z2} = \frac{d\phi_{S2}(z)}{dz} = \left[ C e^{\lambda z} - D e^{-\lambda z} \left[ 1 - e^{-\lambda z} \right] \right] \]  

(15)

The coefficients \( A, B, C \) and \( D \) in the above equations are given by

\[ A = \frac{V_1 e^{-\frac{\beta}{2}} - V_2 - \frac{\beta}{2} \left[ 1 - e^{-\frac{\beta}{2}} \right]}{e^{\frac{\beta}{2}} - e^{-\frac{\beta}{2}}} \]  

(16)

\[ B = \frac{V_1 e^{\frac{\beta}{2}} - V_2 - \frac{\beta}{2} \left[ 1 - e^{\frac{\beta}{2}} \right]}{e^{\frac{\beta}{2}} - e^{-\frac{\beta}{2}}} \]  

(17)

\[ C = \frac{V_2 e^{-\frac{\beta}{2}} - V_3 - \frac{\beta}{2} \left[ 1 - e^{-\frac{\beta}{2}} \right]}{1 - e^{-\frac{\beta}{2}}} \]  

(18)

\[ D = \frac{V_2 e^{\frac{\beta}{2}} - V_3 - \frac{\beta}{2} \left[ 1 - e^{\frac{\beta}{2}} \right]}{1 - e^{\frac{\beta}{2}}} \]  

(19)

Using the continuity of the Electric Field by equating (14) and (15) for \( z = L_1 \)

\[ \frac{d\phi_{S1}(z)}{dz} \bigg|_{z=L_1} = \frac{d\phi_{S2}(z)}{dz} \bigg|_{z=L_1} \]  

(20)

The value of surface potential \( V_2 \) at the junction of two-materials can be obtained and is given by

\[ V_2 = \frac{V_1 + V_3}{} \left[ 1 - \cosh \frac{\beta}{2} \right] + \frac{\beta}{2} \left[ 1 - \cosh \frac{\beta}{2} \right] \]  

(21)

2.3. Threshold voltage model

In a dual material gate structure, the position of the minimum surface potential is always located under the gate material having higher workfunction \( (M_1) \) [37]. Therefore, the position of the minimum surface potential can be found by equating the derivative of the surface potential under \( M_1 \) to zero. By equating \( d\phi_4(z)/dz = 0 \), we obtain

\[ z_{min} = \frac{1}{2\lambda} \ln \left( \frac{B}{A} \right) \]  

(22)

By substituting (22) i.e. the value of \( z_{min} \) in (12) the value of minimum surface potential can be calculated as
φ₅,min = 2√(AB) \cdot \frac{β₁}{2}

(23)

The threshold voltage Vₜh is defined as the gate voltage for which the minimum surface potential is twice the bulk potential to induce a conducting channel at the surface of the MOSFET. Therefore, to determine the expression of threshold voltage, minimum surface potential φ₅,min is equated to 2φ_F.

φ₅,min = 2φ_F

(24)

Here φ_F is the difference between the extrinsic Fermi level in the bulk region and the intrinsic Fermi level. Therefore, substituting V₉G = Vₜh in (24) and solving for Vₜh, the threshold voltage can be expressed as

Vₜh = \frac{u₁ ± \sqrt{u₁^2 - 4u₂u₃}}{2u₂}

(25)

The coefficients u₁, u₂ and u₃ are given in Appendix-A.

2.4. Current model

The electron current along the channel of a Surround gate MOSFET can be written as described in [23]

I_D(z) = \int_0^R 2πRj(z)dr

(26)

Subthreshold conduction is dominated by the diffusion current and is given by presented in [26, 38]

J(z) = \frac{\mu_n}{1 + \vartheta(V₉G - Vₜh)} qn_{min}(r, z) \frac{dV(z)}{dz}

(27)

Where n_{min} = \frac{qφ_{F,inv} - V}{V_F}, Substituting this value of the inversion charge carriers

I_D(z) = \frac{\mu_n}{1 + \vartheta(V₉G - Vₜh)} πqn_R^2 \frac{dV(z)}{dz} \vartheta \left(1 - e^{-φ_{min}}\right)

(28)

Integrating the above equation along the channel and applying boundary conditions with the boundary conditions at source V(0) = 0 and drain V(L) = V_D, we obtain

I_D = \frac{πR²}{L} \vartheta \frac{\mu_n}{1 + \vartheta(V₉G - Vₜh)} πqn_R^2 \frac{dV(z)}{dz} \vartheta \left(1 - e^{-φ_{min}}\right)

(29)

Where μ_n is the doping dependent mobility given by [39]

μ_n = \frac{μ_n}{\sqrt{\left(1 + \frac{N_s}{N_{sd} + N_{so}}\right)}}

(30)

Where μ_n is the electron mobility, S₁ and θ are the fitting parameters required to obtain a fit between the modeled expression and simulated results. The value of S₁ and θ considered in this study equals to 350 and 0.04 respectively [40]. In TCAD simulation, the threshold voltage (Vₜh) is measured considering a constant current method, with reference drain current equal to 1 × 10⁻⁷ A/μm [41].

3. Model verification and result

To verify the proposed analytical model, a graph of surface potential distribution versus the channel length was plotted using MATLAB and was compared with the results obtained from numerical TCAD device simulator ATLAS [42]. Fermi-Dirac carrier statistics model with Drift-Diffusion (DD) model has been employed to model carrier transport in 2-D device simulation. In spite of the fact that DD model fails to capture velocity overshoot effect and fails in ballistic limits, according to a recent work [43], DD model is chosen for the simplification it offers for modeling nanoscale devices. Concentration dependent mobility model (CONMOB) ad Field dependent mobility models (FLDMOB) have also been used. To model carrier recombination, Shockley–Read–Hall (SRH) recombination model combined with Auger recombination model has been chosen. Newton and Gummel methods are chosen to obtain numerical solution coupled differential equations.

A. Surface Potential variation for DMG and SMG MOSFETs

Fig. 2 shows the plot of the variation of the surface potential profile as a function of position along the channel from the source side to the drain side for DMSG and SMSG MOSFETs as obtained from modeled expression and TCAD simulation. As the gate of the DMSG materials is made up of two metals with different work function, a potential step change near the junction of the two metals is observed. This step change in the potential profile indicated in Fig. 2 is responsible for an increased carrier velocity and hence in increased carrier transport efficiency causing an increase in the Drain current I_D.

Fig. 3 shows the plot of the variation of surface position as a function of the position along the channel for different values of radius R = 10 nm and 20 nm. From Fig. 2, it is observed that as radius R decreases, the minimum value of surface potential (φ₅,min) decreases, and shifted towards the source side, thus indicating higher band-bending, higher gate-controllability, resulting in decreased effect of drain-induced barrier lowering (DIBL) and decrease of Vₜh roll-off. Thus, it may be concluded that a reduction in channel radius causes in decrease of SCEs.

B. Electric Field variation for DMSG and SMSG MOSFETs

Fig. 4 shows the comparison of the variation of the lateral Electric Field for DMSG and SMSG MOSFETs as a function of the...
position along the channel from the source side to the drain side with the results obtained from modeled expression and numerical TCAD simulation. Fig. 4 reveals that a step change in the potential profile causes a step change in the Electric Field profile located at the junction of the two metals. The increase in the Electric Field near the junction of the two-metals, leads to an increase in the carrier transport efficiency. Moreover, from Fig. 4, a reduction of the Electric Field near the drain end for DMSG MOSFET is evident. In contrast, for SMSG MOSFET, an increased value of Electric Field as compared to DMSG MOSFET is also evident. A high Electric Field near the drain side may results in the formation of highly energetic and accelerated “hot-carrier”, which under the influence of transverse Electric Field may tunnel into the oxide, gets trapped into the oxide region and damage the interface, thus causing concerns about device reliability. The reduction in the drain side Electric Field indicates a reduction in the deleterious Hot-Carrier Effects (HCEs).

C. Threshold Voltage variation for DMG and SMG MOSFETs

D. DIBL variation for DMG and SMG MOSFETs

Fig. 5 plots the threshold voltage ($V_{TH}$) variation as a function of channel length for DMSG and SMSG MOSFETs. From Fig. 5, it is evident that DMSG MOSFET provides higher efficacy to $V_{TH}$ roll-off as compared to SMSG MOSFETs. The distributed profile of the Electric Field along the channel for gate-engineered MOSFETs causes a screening of the drain potential variation to the source side of the channel, which leads to a reduction in source-channel side barrier modulation, thus leading to a reduction in Drain Induced Barrier Lowering (DIBL), and in turn a reduction in $V_{TH}$ roll-off is achieved for DMSG MOSFETs.

Fig. 6 plots the threshold voltage ($V_{TH}$) variation as a function of channel radius $R$ for DMSG and SMSG MOSFETs. From Fig. 6, it is evident that DMSG MOSFET provides higher efficacy to $V_{TH}$ roll-off as compared to SMSG MOSFETs for increase in channel radius with a fixed channel length. Fig. 6 reveals that as the Si channel thickness increases for both SMSG and DMSG devices, the gate loses its control over the channel carriers while the drain gains more control on the same leading to decrease in the threshold voltage. Therefore, in order to achieve a small reduction of threshold voltage with gate-length downscaling, the Si channel thickness needs to be optimized to a small value.

D. Subthreshold Current variation for DMG and SMG MOSFETs

Fig. 7 shows the comparison between modeled expression and TCAD simulation of the variation of subthreshold Drain current ($I_{DS}$) as a function of the $V_{GS}$ for DMSG and SMSG MOSFETs. Fig. 7 indicates that DMSG provides higher $I_{DS}$ as compared to SMSG devices, owing to its higher carrier transport efficiency attributed by the increase in the average Electric Field produced by the gate-material engineering. The peak in the electric field profile leads to a rapid acceleration to the carriers at the interface of metals, resulting in enhanced carrier transport efficiency to supply more and more carriers to reach the drain terminal. However, it is worth mentioning that an increase in the subthreshold drain current causes an increase in the subthreshold leakage current and a decrease in the subthreshold swing, which needs to be minimized for ultra low power device applications.
From Figs. 8 and 9, it is evident that DMDG MOSFET show better performance than SMDG devices with respect to DIBL, which is defined as

\[
DIBL = \frac{\Delta V_{Th}}{\Delta V_{DS}} = \left( \frac{V_{Th1} - V_{Th2}}{V_{DS1} - V_{DS2}} \right)
\]

(31)

Where \( V_{Th1} \) and \( V_{Th2} \) are threshold voltages extracted at drain bias \( V_{DS1} = 0.1 \) V and \( V_{DS2} = 1.0 \) V. Fig. 8 shows the variation of DIBL as a function of channel length. Fig. 8 shows that DMSG device outperforms SMDG device due to the higher gate-controllability, increased screening of the threshold voltage defining region (Region under \( M_1 \) near the source) from the variation of the drain bias caused by the step pattern in the potential profile. On the other hand, Fig. 9 shows that DMDG shows better performance than SMDG for the variation of DIBL as a function of radius \( R \). From Figs. 6 and 3 it is evident that that thicker Si film exhibits higher \( V_{Th} \) roll-off with a reduced gate-controllability indicating a reduced SCEs, thus justifying higher DIBL for increase in radius \( R \) (Fig. 9).

### 4. Conclusion

For the first time, this paper reports a comprehensive comparative study of the effect of the gate engineering on the short-channel effect performances between a DMSG MOSFET and an SMSG MOSFET of same dimension. Physics based analytical model of the surface potential, Electric Field, threshold voltage and drain current has been developed to find the influence of gate engineering on the SCEs. It has been demonstrated that DMSG MOSFET provides a better immunity to SCEs as compared to SMSG MOSFET. In order to validate and verify our model, the modeled expressions have been compared with the simulated results obtained from the 2-D device simulator ATLAS. A nice agreement is achieved with a reasonable accuracy over a wide range of device parameter and bias condition. This work provides an intensive and guide for further research and experimental investigation of the critical aspects of the gate-engineered surrounding gate MOSFET.
Appendix A

\[ u_1 = (p_5 + p_8 + p_9); \quad u_2 = (2l_1 p_5 + p_6 + p_7 + 2l_2 p_6 + l_3 p_9 + l_2 p_9); \]
\[ u_3 = \left( \frac{1}{L} p_5 + p_6 + p_7 + 2l_2 p_6 + l_3 p_9 - p_7 \right); \quad p_{10} = \left( -V_i^2 - p_2^2 - p_3 V_i g_4 \right); \]
\[ p_8 = \left( g_1^2 + p_4^2 + g_3 p_4 \right); \]
\[ p_4 = \left( k_1 n_1 p_1 - 2k_1 p_1 + k_1 n_1^2 p_1 \right); \]
\[ p_3 = \left( -2k_2 p_1 + k_2 m_1^2 p_1 + k_2 m_2 p_1 \right); \]
\[ p_{2} = \left( 2V_i k_2 p_1 + 2V_i k_1 p_1 \right); \]
\[ p_1 = \frac{1}{\left( k_1 e^L \right)} + k_1 e^L + k_2 e^L + \frac{L_2 - L_1}{L} + \frac{L_3 - L_2}{L}; \]
\[ g_1 = \frac{1}{\left( n_1 L \right)} - \frac{1}{\left( n_1 L \right)} - \frac{2}{\left( n_1 L \right)}; \]
\[ g_2 = \frac{1}{\left( V_i n_1 L \right)} - \frac{2}{\left( V_i n_1 L \right)}; \]
\[ g_3 = \frac{1}{\left( n_1 L \right)} - \frac{1}{\left( n_1 L \right)} - \frac{1}{\left( n_1 L \right)}; \]
\[ n_3 = \frac{1}{\left( n_1 L \right)} - \frac{1}{\left( n_1 L \right)} - \frac{1}{\left( n_1 L \right)}; \]
\[ n_4 = \frac{1}{\left( n_1 L \right)} - \frac{1}{\left( n_1 L \right)} - \frac{1}{\left( n_1 L \right)}; \]
\[ n_5 = \frac{1}{\left( n_1 L \right)} - \frac{1}{\left( n_1 L \right)} - \frac{1}{\left( n_1 L \right)}; \]
\[ n_6 = \frac{1}{\left( n_1 L \right)} - \frac{1}{\left( n_1 L \right)} - \frac{1}{\left( n_1 L \right)}; \]
\[ L_1 = \frac{1}{V_i n_1 L} - \frac{q e}{\lambda T_{Si}}; \]
\[ C_2 = \left( \frac{e^L}{L^2} - \frac{e^L}{L^2} - \frac{e^L}{L^2} \right) \left( \frac{e^L}{L^2} - \frac{e^L}{L^2} - \frac{e^L}{L^2} \right); \]
\[ C_3 = \frac{e^L}{L^2}; \quad C_4 = \frac{e^L}{L^2}; \quad C_5 = \frac{e^L}{L^2}; \]

References


