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GUEST EDITORIAL

Special issue on selected papers from the NORCHIP 2009 conference

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In this special issue of the journal, eight selected papers from the 27nd NORCHIP conference are presented in extended versions. The selection of papers was based on conference review scores and feedback from the sessions chairs on the presentations of the conference papers. NORCHIP is an annual conference alternating between the Nordic and Baltic countries. In 2009, the conference was held in Trondheim, Norway on November 16 and 17.

There were 120 participants and 67 papers were presented during the 2 days in 14 regular sessions and two poster sessions. The guest editor feels that the following eight papers selected from the 26 analog papers all contain contributions that will be of interest to the readers.

The first two papers are devoted to integrated receivers. In the first paper, Atef et al. present an optical receiver for multilevel data communication over plastic optical fiber. A measured sensitivity of −31 dBm at 250 Mb/s was presented for a binary signal, and a data rate of 500 Mb/s and a sensitivity of −25 dBm were achieved with four-level pulse amplitude modulation. In the second paper Camponeschi et al. present a thorough analysis and the design of a complete 2.2 GHz quadrature receiver front-end. The circuit, fabricated in a 90 nm CMOS process, features a stacked single-ended low-noise amplifier and a self-oscillating mixer. The oscillator LC tank is designed to provide gain at low frequency without decreasing the quality factor at the oscillating frequency. Measurement results show a conversion gain of 27.1 dB with a 14 MHz bandwidth, a noise figure ranging from 12.4 to 13.2 dB with a flicker corner frequency of 200 kHz and an input referred 1 dB compression point of −23.7 dBm.

Two papers related to data converters are presented in this issue. The first one by Korhonen and Kostamovaara describes an on-chip offset generator for testing the integral nonlinearity (INL) of A/D converters with up to 12 bits of resolution without an accurate test stimulus. The second paper by Wulff and Ytterdal presents a differential comparator-based switched-capacitor (CBSC) pipelined ADC with comparator preset and comparator delay compensation. Measured results of a prototype fabricated in 90 nm CMOS show that the compensation of the comparator delay by digitally adjusting the comparator threshold improves the ADC resolution 23 times. The ADC has an ENOB of 7.05-bit at a sampling rate of 60 MS/s.

In the paper by Shen et al., the authors present a 1.5 GHz UWB low noise amplifier in a 0.18 μm CMOS technology. To achieve wide-band input match a common-gate topology is used for the first stage, while a cascode stage was used as the second-stage. Interestingly, two inductors were used to obtain a small chip area.

Lee et al. present a 2.4 GHz quadrature VCO designed in a 65 nm CMOS technology and operating at a supply voltage of only 0.6 V. By using a high LQ inductor, a very low power consumption of below 300 μW was obtained in post-layout simulations. The phase noise figure of merit was better than 182.5 dB at all supply voltages of interest. This number is competitive to other state-of-the-art QVCOs.

At 60 GHz, standard device models obtained from the foundries are not accurate enough. The paper by Tao et al. addresses this issue and presents a modeling solution for active and passive devices implemented in 65 nm CMOS and targeted for operation at 60 GHz. The approach uses existing foundry models for the intrinsic devices and

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EM-simulations are used to extract models for parasitic elements due to, for example, wire stacks. The modeling approach has been verified by designing a 60 GHz receiver front-end in 65 nm CMOS.

In the article of Cenkeramaddi et al., inverter-based front-end LNAs for 30 MHz medical ultrasound imaging applications are presented. Both continuous-time and discrete-time charge-sampling topologies were designed and fabricated in a 90 nm CMOS technology. Measured results of both topologies were presented. The charge-sampling LNA was clocked at frequencies up to 100 MHz. By implementing the sample-and-hold function as early as in the front-end LNA, pre-beamforming can be implemented in the discrete-time domain which is inherently wideband.

The eight papers have undergone normal review. We would like to express our gratitude to the reviewers for the comments and suggestions that have improved the quality of the papers.

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Trond Ytterdal was born in Trondheim January 26, 1964. He received his M.Sc. and Ph.D. degrees in electrical engineering from the Norwegian Institute of Technology, University of Trondheim in 1990 and 1995, respectively. He was employed as a research associate at the Department of Electrical Engineering, University of Virginia (1995–1996) and as a research scientist at the Electrical, Computer and Systems Engineering Department, Rensselaer Polytechnic Institute in Troy, New York (1996–1997). From 1997 to 2000 he worked as a senior ASIC designer at Nordic VLSI in Trondheim, Norway. Since 2001 he has been on the faculty of the Norwegian University of Science and Technology (NTNU), where he is a Professor at the Department of Electronics and Telecommunications. Trond Ytterdal's present research interests include design of analog integrated circuits, behavioral modeling and simulation of mixed-signal systems, modeling of nanoscale MOSFETs and other field-effect transistors and novel device structures for application in circuit simulators. He has published more than 130 scientific papers in international journals and conference proceedings. He is a co-author of the books Semiconductor Device Modeling for VLSI (Prentice Hall, 1993), Introduction to Device Modeling and Circuit Simulation (Wiley, 1998) and Device Modeling for Analog and RF CMOS Circuit Design (Wiley, 2003), and has been a contributor to several other books published internationally. He is also a co-developer of the circuit simulator AIM-Spice. Prof. Ytterdal is a member of The Norwegian Academy of Technological Sciences and a Senior Member of IEEE.