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Diffractive Backside Structures via Nanoimprint Lithography

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Abstract

For decreasing thicknesses of wafer based silicon solar cells, photon management structures to maintain high quantum efficiencies will gain importance. Diffractive gratings on the wafer back side can be designed to achieve very high path length enhancements, especially for weakly absorbed infrared radiation. This technologically demanding concept has to be realised using processes with upscaling potential. Therefore, we present a fabrication process for producing photonic structures in silicon based on interference lithography and nanoimprint lithography (NIL).

We realised linear as well as crossed gratings of different depths, which were etched into the wafer back side. Polarisation dependent reflection measurements were made to get information about potential absorption enhancement as well as the occurrence of parasitic absorption in the metal reflector. This is conducted for a PECVD silicon oxide buffer layer between grating and reflector as well as a spin coated silicon oxide layer. Besides these optical characterisations, we further investigated the electrical properties of the back surface, where we applied a concept in which electrical and optical properties are decoupled. This is realised by a layer stack on the wafer back side, consisting of a thin Al_2O_3 passivation and a doped amorphous silicon layer.

Keywords: Light Trapping; Nanoimprint Lithography; Texturing

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1. Introduction

Light trapping or photon management will gain importance for thinner silicon solar cells. Besides commonly used textures on the front side of solar cells with feature sizes of several microns [1], the fabrication of diffractive elements on the wafer back side has been investigated by several groups [2, 3, 4]. There are some aspects that make the realization of diffractive elements demanding as well as potentially undo the positive optical effect on the solar cell performance: (i) high resolution processes are required; (ii) solar cell fabrication requires the patterning of full-wafer areas with high throughput. Therefore, processes like e-beam lithography are not applicable; (iii) surface recombination velocity at the rear side increases due to a surface enlargement; (iv) the high definition pattern transfer is typically combined with plasma etching processes. It is challenging to achieve anisotropic etching profiles without introducing plasma damages and thus reducing the electrical quality of the rear side; and (v) the combination of back side gratings and metal back reflectors might go hand in hand with increased parasitic absorption.

To realise diffractive patterns on large areas, we chose a process chain based on interference lithography as the mastering and nanoimprint lithography (NIL) as the replication technology [5]. After imprinting the etching masks, plasma etching was applied for the pattern transfer into the silicon substrates. Between the grating and the metal back reflector, a dielectric buffer layer has to be realised. We investigated the PECVD deposition of silicon oxide as well as the spin coating of a dispersion of silicon oxide nanoparticles. Besides SEM characterisation to gather information about the topography of the back reflector for both approaches, we determined the polarization dependent optical absorption. These optical measurements were conducted with gratings directly etched into the wafer back side. In this paper, we also present a novel structure in which the flat rear side is first passivated by a thin Al_2O_3 layer and then an amorphous silicon layer is deposited and subsequently patterned. In this way, electrical and optical properties can be tuned separately, and the introduction of the grating need not increase the surface recombination velocity. Lifetime measurements of these structures were conducted to get insight about potential degradation of the rear surface passivation due to the applied plasma etching processes.

2. Texturing process chain

For the fabrication of stamps for the NIL process, we used interference lithography. In this study we fabricated linear and crossed gratings of a period of 1 µm and a depth of about 350 nm on 75 x 75 mm² glass substrates. The grating period was chosen to be 1 µm according to theoretical considerations published in [6]. There, electro-optical simulations were performed for silicon solar cells with a linear grating on the wafer back side. For 40 µm thick cells, a gain in j_{sc} of up to 1.85 mA/cm² and in η of up to 1 % absolute was predicted for a grating with a period of 990 nm and a pattern depth of 160 nm. In [7] and [8], optical simulations confirm the optimum structure periods around 1 µm and lead to the conclusion that bi-periodic gratings are superior to linear gratings.

The master structures were then replicated into an addition-curing polydimethylsiloxane (PDMS) material by cast molding. The elastomeric PDMS replications are used as stamps in the NIL process. The flexibility of this material is essential for large area processing in NIL [9]. The stamp is pressed into a low viscous resist and, whilst maintaining the pressure, the resist is cured by a UV-exposure through the transparent stamp. After the curing process, the stamp is demoulded and a patterned resist layer remains on the silicon substrate. The pattern was replicated on an area of 70 x 70 mm² as a consequence of the master structures used within this study. The up-scaling for full wafer processing on 4 inch wafers is not expected to be critical. What's more, we have already reported on the realization of a novel Roller-NIL tool to potentially fabricate etching masks with these small features in an industrially feasible way [10].

Finally, the imprinted polymer layer can be used as an etching mask to transfer the grating structures into the silicon. We applied an anisotropic reactive ion etching (RIE) process to generate preferably binary patterns. This RIE process was conducted in a capacitively coupled parallel plate reactor with sulphur hexafluorine (SF_6) and oxygen (O_2) as process gases. For the resist stripping, we investigated two possible routes. One is based on plasma ashing using O_2 as a process gas and the other is based on a lift-off of resist residues after the RIE process by dissolving a sacrificial layer. Fig. 1 shows an image of an imprinted pattern as well as two SEM micrographs after the etching processes.

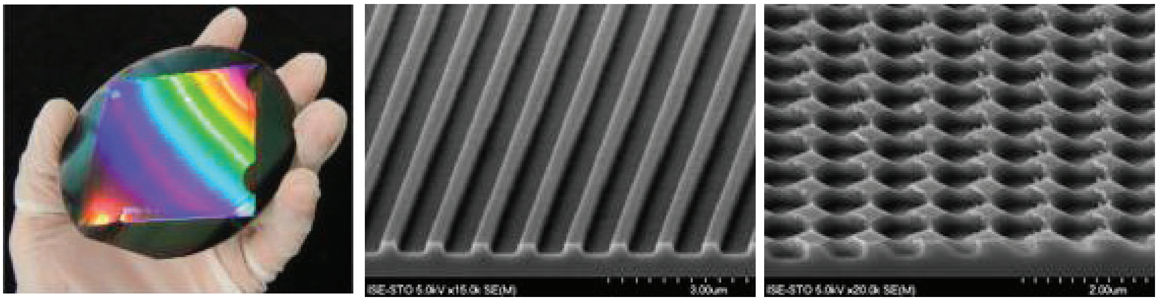

Fig. 1. Left: Imprinted linear grating on a silicon wafer. Middle and Right: SEM micrographs of a linear and a crossed grating after etching and resist removal of depths of about 230 nm and 300 nm, respectively

3. Sample preparation and characterization

Samples for optical characterization of absorption enhancements introduced by the gratings were processed on FZ c-Si substrates. The flat front side was coated with a silicon nitride ARC. On the back side, the grating was directly etched into the silicon. After the patterning process, first a 450 nm thick silicon oxide layer was deposited via PECVD, which was supposed to level the interface onto which the aluminum is then applied by evaporation. Samples of different etching depths for the linear and the crossed grating as well as a flat reference were processed. These samples were characterized by reflection measurements.

As can be seen in Fig. 2, considerable absorption enhancements can be introduced by the realisation of diffractive back side structures. An upper bound for estimating the potential gain in j_{sc}, is an integration of all additionally absorbed photons (from 900 – 1180 nm). This is introduced as a gain in photocurrent Δj_{ph}, also shown in the legend in Fig. 2 (left). This value represents an upper bound because it considers all absorption enhancement in the sample, including possible enhancement of parasitic absorption in the reflector, which would not generate extra photocurrent. The fact that absorption enhancement occurs for photon energies below the silicon bandgap, confirms that parasitic absorption is indeed enhanced. This deduction is reinforced by polarisation dependent reflection measurements for the linear grating samples. It can be observed that p-polarised light experiences a very pronounced absorption enhancement (see Fig. 2 (right)). This polarisation dependent parasitic absorption is typical of corrugated metal patterns.

Besides these negative effects, a distinct peak in absorption enhancement close to the E_g can be observed. This corresponds to the design of the photonic structure to achieve a maximum path length enhancement in the silicon at these wavelengths. Another conclusion that can be drawn from Fig. 2 (left) is that the crossed grating reveals a higher potential for absorption enhancement than the linear grating. This is in agreement to the theoretical results published in [8].

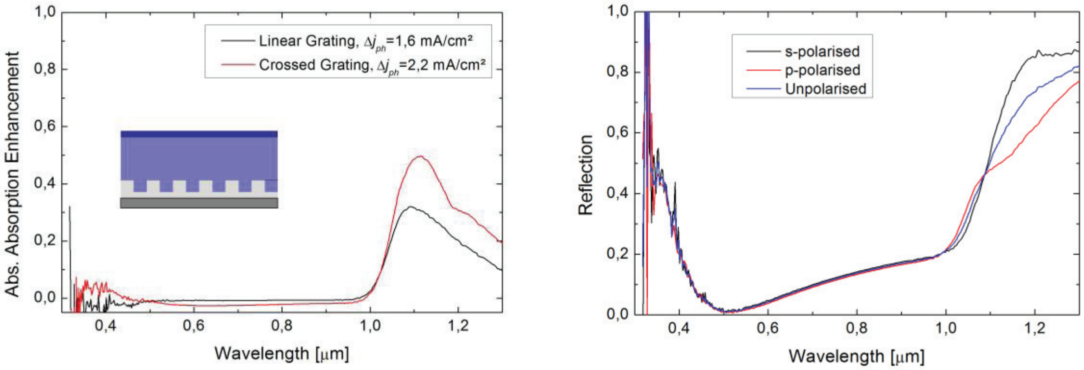

Fig. 2. Left: Measured absolute absorption enhancements of a linear and a crossed grating. The depths of the gratings were 190 nm and 230 nm, respectively. Right: Polarisation dependent reflection measurement of the linear grating

SEM images of these samples show that the PECVD deposited buffer layer has grown conformally with the grating leading to a modulated oxide-aluminum interface (Fig. 3, left). This is known to increase parasitic absorption in the reflector [6]. To reduce parasitic absorption, we investigated an alternative means of applying a dielectric buffer layer, which leads to a better planarization of the oxide-aluminum interface. This is based on spin coating of a dispersion of silicon oxide nanoparticles onto the textured rear surface. The very level surface resulting from this technology is also shown in Fig. 3 (right).

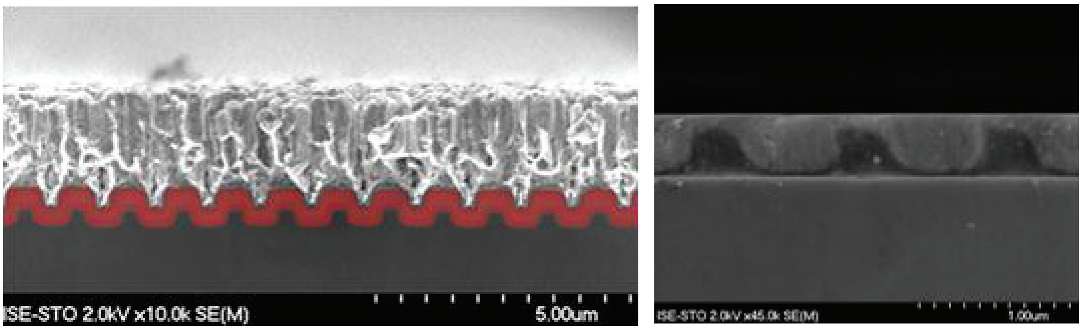

Fig. 3. Left: SEM image of the wafer rear side. The PECVD silicon oxide is dyed red to visualize the patterned aluminium back reflector (top). The depth of the etched grating is 230 nm. Right: Spin coated silicon oxide nanoparticles on top of an imprinted resist layer

Fig. 4 shows measurements of absolute absorption enhancements for wafers with crossed gratings on the rear side and both SiO_x buffer layer types: spin coated (dotted curve) and PECVD applied (solid curve). Looking at wavelengths above the silicon band edge (photons with energy less than E_g), it can be seen that the grating induced parasitic absorption is lower for the spin coated buffer layer, but is still present. It is reasonable to presume that this is also true in the region in which silicon absorbs. Still, the shape of the grating induced absorption enhancement as well as current simulation results leave us optimistic that there is a useful absorption enhancement in silicon for the spin coated sample that correspond to a Δj_{ph} above 1.5 mA/cm².

The origin of parasitic absorption might be related to difficulties when drying the spin coated SiO_2 dispersion. During the drying, macroscopic cracks appear due to tensions in this layer induced by shrinking. Parameters for optimizing this behaviour are related to properties of the solvent in which the nanoparticles are diluted. The vapor pressure, surface tension and the wetting behavior to the a-Si surface might influence the homogeneity of the SiO_x layer. Also, the spin coating process itself has influence on the layer quality, since a drying already begins within this step.

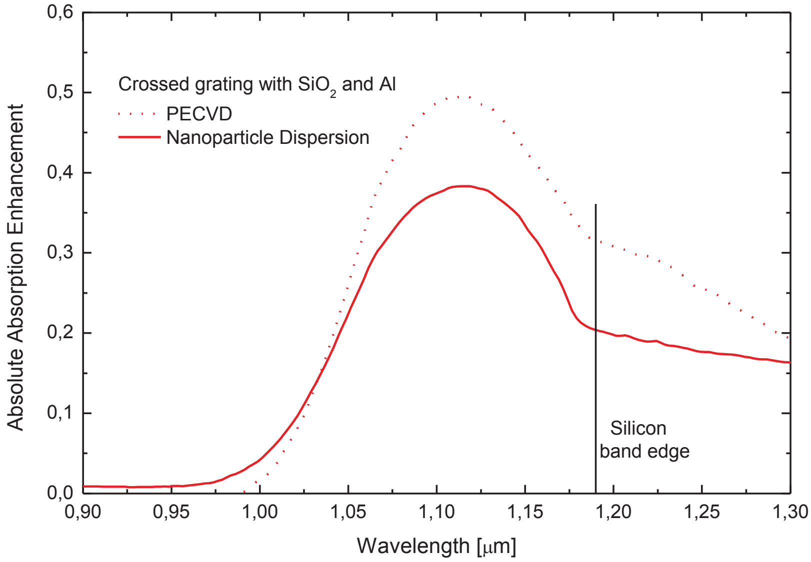

Fig. 4. Measured absolute absorption enhancement in silicon wafers with a flat front introduced by crossed gratings on the rear side. Two different silicon oxide buffer layers on the rear are compared. One is applied via PECVD, the other by spin coating of nanoparticles

In addition to enhancing the optical properties of the solar cell, it must be ensured that the introduction of the grating does not harm the electrical properties. To this end, a novel structure has been fabricated. A very thin Al_2O_3 is grown on the un-textured rear side of the silicon wafer followed by an amorphous silicon (a-Si) layer. The a-Si layer is textured as described above and solely serves as an optically active layer (since it is electronically isolated from the absorbing region of the solar cell). In this context, lifetime samples were processed to evaluate the potential degradation of the passivation due to the plasma etching processes. First very promising results indicate that the RIE process does not reduce the passivation quality of the Al_2O_3 layer. Samples made of p-type FZ 1 Ωcm silicon were passivated symmetrically with Al_2O_3 deposited by ALD. On the Al_2O_3 layer on the rear side, a 300 nm thick a-Si layer was deposited by PECVD, which was then textured using the presented process chain. Values extracted for the surface recombination velocity on the back side S_{back} were as low as 7 cm/s before and 18 cm/s after the texturing process. Calculating these values, it has been assumed that the bulk lifetime is infinitively high and S_{front} is not affected by the texturing process. This constitutes the worst case in which all additional recombination takes place on the rear side. The preservation of a low S_{back} confirms the effectiveness of the presented concept for decoupling electrical passivation from the optically active texture.

4. Conclusion

An upscaleable method for the fabrication of photonic structures for silicon solar cell applications is presented. Nanoimprint Lithography allows realization of nano-scale features on large areas. Optical absorption measurements of samples with back side gratings show the potential of this concept. The problem of inducing a corrugated metal pattern (the aluminum back reflector) on the wafer rear is identified and a solution is presented. The technology of spin coating a silicon oxide nanoparticle dispersion is well suited for this purpose and parasitic absorption was reduced thereby. However, there is still room for optimization concerning the spin coating and the drying of the dielectric buffer layer.

Concerning the electrical quality of such finely textured rear surfaces, a very promising approach is presented. A planar rear is passivated with a very thin Al_2O_3 layer. Onto this passivation layer, an amorphous silicon layer is deposited, which is subsequently textured and solely serves as an optically active layer. Thus, electrical and optical properties of this layer stack are decoupled. First promising tests on lifetime samples confirmed the applicability of this concept. Excellent values for S_{back} of samples with a textured rear sides about 18 cm/s were achieved. In future work, tests concerning the contacting of the base through this layer stack have to be performed before solar cells with photonic structures and this novel layer stack on the rear can be fabricated.

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