New low power adders in Self Resetting Logic with Gate Diffusion Input Technique

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Received 17 April 2013; accepted 24 March 2014

Abstract The objective vividly defines a new low-power and high-speed logic family; named Self Resetting Logic with Gate Diffusion Input (SRLGDI). This logic family resolves the issues in dynamic circuits like charge sharing, charge leakage, short circuit power dissipation, monotonicity requirement and low output voltage. In the proposed design structure of SRLGDI, the pull down tree is implemented with Gate Diffusion Input (GDI) with level restoration which apparently eliminated the conductance overlap between nMOS and pMOS devices, thereby reducing the short circuit power dissipation and providing High Output Voltage $V_{OH}$. The output stage of SRLGDI has been incorporated with an inverter to produce both true and complementary output function. The Resistance Capacitance (RC) delay model has been proposed to obtain the total delay of the circuit during precharge and evaluation phases. Using SRLGDI, the primitive cells and 3 different full adder circuits were designed and simulated in a 0.250 $\mu$m Complementary Metal Oxide Semiconductor (CMOS) process technology. The simulated result demonstrates that the proposed SRLGDI logic family is superior in terms of speed and power consumption with respect to other logic families like Dynamic logic (DY), CMOS, Self Resetting CMOS (SRCMOS) and GDI.

1. Introduction

With continual technology scaling and improvements in lithography, the integrated system has become faster and thus it is employed in diverse real-time applications like mobile, digital signal processing, multimedia application and scientific computation. To support high-performance applications, proper choice of technology selection and topology for implementing various logic are the mandatory issues in designing low-power devices (Uma and Dhavachelven, 2012a).

The Pass Transistor Logic (PTL) (Chatzigeorgiou and Nikolaidis, 2001) circuit offers better characteristics than static CMOS. PTL can implement most functions with fewer transistor counts, thus reducing the overall capacitance, which results in faster switching times and low power dissipation. The general issue pertaining to this PTL logic is voltage variation due to threshold drop owing to series resistance between input and output. These demerits were surmounted using...
Complementary Pass-Transistor Logic (CPL) and Swing Restored Pass-Transistor Logic (SRPL) (Parameswar et al., 1994; Sasaki et al., 1996). However this logic produced larger short circuit currents, high transistor count to realize a simple gate and high wiring overhead due to the dual-rail signals.

The GDI (Morgenshtein et al., 2002; Uma and Dhavachelvan, 2012b; Agrawal et al., 2009) is the lowest power design technique, which is suitable for designing fast, low-power circuits, using reduced number of transistors (as compared to Transmission Gate and CMOS). The main drawbacks associated with GDI include: The bulk terminals are not properly biased thereby the circuit exhibits threshold drop and variation in $V_T$. Because of floating bulk, the cells can be implemented in SOI process which would increase the cost of the fabrication. These demerits can be overcome by permanently connecting the bulk terminals pMOS to VDD and nMOS to GND which resolves the threshold variation. This configuration provides suitability for fabricating the logic cells in CMOS p-well and n-well process. Until today static CMOS has been the design style of choice for IC designers due to its robustness against voltage scaling and transistor sizing (high noise margins) and thus the operation is reliable at low voltages (Bisdounis et al., 1996). The disadvantage of CMOS is the substantial number of large pMOS transistors, resulting in high input loads and when the operating frequency increases the circuit dissipates more power. The propagation delay is slightly higher when compared to other logic family due to its larger node capacitances.

Dynamic logic families are a good candidate for high speed and high performance circuit than the conventional static CMOS. Dynamic logic requires fewer transistors to implement a given logic function, less area and faster switching speed due to its reduced load capacitance (Yee and Sechen, 1996; Balsara and Steiss., 1996; Srivastava et al., 1998). However this circuit suffers from charge sharing, charge leakage, loss of noise immunity, timing problem due to clock input and feed through. These issues can be suppressed using an asynchronous dynamic circuit named Self Resetting CMOS (Kim, 2001). Asynchronous SRCMOS circuit operation has a separate pre-charge and evaluation phase which discharges the dynamic storage nodes to evaluate the desired logic function and then resetting these nodes back to their original charged state by a local feedback timing chain instead of a global clock. One of the advantages of self-resetting logic is that when the data presented at the evaluation phase does not require dynamic node to discharge, which makes the precharge device inactive thereby reducing power (Litvin and Mourad, 2005; Uma, 2011. However this scheme endures from short circuit power and low output voltage due to nMOS pull down network producing conductance (direct path between) overlap between nMOS and pMOS. So the primary objective of this work focuses to resolve the problem incurred in the existing SRCMOS to support low-power and high-speed applications.

2. Various dynamic logic

The group of dynamic logic family offers good performance over traditional CMOS logic. The basic operation of dynamic logic is normally done with charging and selectively discharging capacitance. The logic operation needs two sub-cycles to complete (precharge and evaluation). During the precharge phase the clock signal charges the capacitance and during the evaluation phase the clock discharges the capacitance depending upon the condition of logic inputs.

Various dynamic logic circuits are portrayed in Fig. 1. The logic circuit in Fig. 1(a) leads to contention problem during precharge and this problem is resolved by incorporating an nMOS stack at the bottom as shown in Fig. 1(b). The demerits associated with circuit as shown in Fig. 1(a) are loss of noise immunity and a serious restriction on the inputs of the gate (monotonicity problem) and only the non-inverting logic can be implemented. These problems are surrogated using the NORA CMOS circuit as shown in Fig. 1(d). But the problem with the logic is global clock presenting clock distribution grid and routing to dynamic gates that presents a problem to CAD tools and introduces issues of delay and skew into the circuit design process. Domino logic with charge-keeper circuit has been developed to combat this problem. The circuit realization is shown in Fig. 1(e), but the demerits of the circuit are: a slow clock slope leading to conductance overlap between nMOS and pMOS devices resulting in dc power dissipation and high sensitivity to noise. An asynchronous dynamic logic self-resetting CMOS (SRCMOS) circuit technique is shown in Fig. 1(f). In this logic no global clock is required and all the operation is controlled through the inverter chain between pMOS and output. The general issue related to this logic is static power consumption and if the width of the pulses must be controlled carefully or else there may be contention between nMOS and pMOS devices, or even worst, oscillations may occur.

3. Proposed Self Resetting Logic with Gate Diffusion Input (SRLGDI)

3.1. Problem statement

Self-resetting circuitry automatically precharges themselves (i.e., reset themselves) after a prescribed delay by conditionally charging the dynamic nodes to evaluate the desired logic function using a local feedback timing chain instead of a global clock. Although this SRCMOS logic inherits lot of merits, it still suffers from static power dissipation due to the nMOS logic structure. As stated earlier, during precharge the nMOS stack is completely open and the output is fed back to the pMOS block to charge the capacitor $C_y$. During this period the nMOS transistors operate in cut-off region exhibiting sub-threshold current. Moreover during the evaluation phase when the entire nMOS transistor in the n-block and $P_{reset}$ transistor is ON direct impedance path exists between the VDD of $P_{reset}$ transistor and nMOS block leading to static power dissipation. The width of the pulses must be controlled carefully or else there may be contention between nMOS and pMOS devices, or even worst, oscillations may occur. These demerits can be surmounted using GDI technique. The change done in the existing SRCMOS, instead of nMOS logic pull down tree, it is replaced by GDI logic with level restoration.

3.2. Circuit topology of SRLGDI logic

In the existing SRCMOS logic the pull-down tree is realized using nMOS block which consumes lot of static power. To surrrogate this issue the proposed SRLGDI has been replaced by
A Gate Diffusion Technique Input (GDI) inherits the properties of Pass Transistor Logic and Complementary Metal Oxide Semiconductor. The basic structure realization resembles the CMOS inverter and the operational feature resembles the PTL logic. The GDI basic cell and general block diagram are depicted in Fig. 2. The basic cell structure realization is similar to CMOS inverter containing series connected to pMOS and nMOS. Each GDI cell contains three inputs: \( V_G \) is the shorted gate input common to pMOS and nMOS, \( V_P \) is the drain/source P-diffusion input at the pMOS terminal and \( V_N \) is the source/drain N-diffusion input at the nMOS terminal. Any Boolean function in GDI technique which is simple or complex is realized using this basic structure.

Boolean function using GDI logic is a \( Y = \frac{Y}{Y} \) network in which each control signal (variable) connects to a pair of series connected to pMOS and nMOS. Each GDI cell contains three inputs: \( V_G \) is the shorted gate input common to pMOS and nMOS, \( V_P \) is the drain/source P-diffusion input at the pMOS terminal and \( V_N \) is the source/drain N-diffusion input at the nMOS terminal. Any Boolean function in GDI technique which is simple or complex is realized using this basic structure.

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A logic expression in GDI can be implemented by applying the Shannon’s expansion theorem to decompose \( Y \) with respect to one of its input variable. For example to implement a 2-input OR logic gate, namely, \( Y = a + b \), apply Shannon’s expansion theorem to decompose \( Y \) with respect to variable \( a \),

\[
Y = a + b = \overline{a} \cdot b + a \cdot \overline{1}
\]

where \( a \) is the control variable connected to the gate terminal of pMOS and nMOS (\( V_G \)), the P-diffusion terminal is connected to input \( b \) and n-diffusion input is connected to VDD. The logic-1 signal at the input will be deteriorated by either pMOS or nMOS switch due to threshold drop. To obtain a full swing voltage a buffer should be added at the output terminal. In GDI technique both pMOS and nMOS are given with independent inputs so as to accommodate more number of logic function thereby minimizing transistor count. For any combination of input there is no chance that all the transistors are ON at the same time. So the subthreshold power is very nominal in the proposed logic technique. The primitive cells of GDI are shown in Fig. 3. The circuit is realized with restoration buffer for full swing output.

The general structure of Self Resetting Logic with Gate Diffusion Input technique (SRLGDI) is shown in Fig. 4. The
structure consists of GDI block to realize any Boolean function. The transistors $P_{\text{preset}}$ and $P_{\text{reset}}$ are used to charge and discharge the dynamic node capacitor $C_y$ during precharge and evaluation phases. The noteworthy aspect of $P_{\text{reset}}$ transistor is that it acts as charge keeper to resolve the charge sharing problem which is the significant issue in dynamic circuit. The $P_{\text{reset}}$ transistor will pull the voltage level high even after the precharge phase to hold the output value high in the existence of charge sharing. The output is fed back to the precharge control input and, after a specified time delay, the pull-up is

Figure 2  (a) Basic GDI cell using inverter structure (b) alternate basic GDI cell representation using PTL (c) general block diagram of GDI logic.

Figure 3  2-Input primitive cells in gate diffusion input with level restoration buffer. AND gate, (b) OR gate, (c) NAND gate, (d) NOR gate, (e) XOR gate and (f) XNOR gate.
reactivated. The inverter INV1 and the internal inverter in the GDI block completely eliminates the contention problem and provides compatibility to cascade the output from one node to another.

The output of the gate provides a pulse if the logic function becomes true. This output is buffered and it is connected to pMOS structure to precharge. The delay line is implemented as a series of inverters. The signals that propagate through these circuits are pulses. The inverter (INV2) present at the output side provides both true and complementary output and also it acts as level restoration circuit to cascade more number of circuits without logical degradation. By using a buffered form of input, the loading (input) is kept almost low when compared to normal dynamic logic while local generation of the reset assures that it is properly timed and occurs only when required. This modification produces less power consumption and high \( V_{OH} \), while apparently maintaining the logical functionality.

### 3.3. Operational feature of SRLGDI logic

The general behaviour of SRLGDI logic can be portrayed as an ability of a logic block to reset its output pulse after it has been asserted. The reset signal is often generated within the block based on the output pulse. The circuit operation is defined in two phases as precharge and evaluation. The switching behaviour is elucidated in Fig. 5, where \( P_{reset} \) and \( P_{reset} \) define the pMOS precharge and reset transistor. During the precharge phase \( CLK = 0 \) in Fig. 5a, the GDI block is open, the transistor \( P_{reset} \) is ON so a direct impedance path exists between node \( y \) and \( VDD \) thereby charging the capacitance \( C_y \) to \( VDD \). The output node \( V_{out} \) is discharged and makes the reset voltage \( V_{reset} \) to be ‘0’ insuring that \( P_{reset} \) is cut-off during this time. For the evaluation phase \( CLK = 1 \) as shown in Fig. 5b, the GDI logic is closed, the transistor \( P_{reset} \) is OFF, in this case \( V_y \rightarrow 0 \) V and the output capacitance charges to give an output voltage \( V_{out} \rightarrow V_{DD} \).

This voltage is fed through the delay path and produces \( V_{reset} \rightarrow V_{DD} \) and the transistor \( P_{reset} \) is active after the specified delay path. The \( P_{reset} \) transistor recharges the node capacitor \( C_y \) back up to a voltage of \( V_y \rightarrow V_{DD} \). This action resets the output voltage to its original precharge value of \( V_{out} \rightarrow 0 \) V. The timing diagram of SRLGDI is shown in Fig. 6.

### 3.4. Primitive cell design in SRLGDI logic

Basic SRLGDI logic gates (AND, OR, NAND, NOR, XOR, and XNOR) are shown in Fig. 7. Each gate consists of a GDI logic tree, half-latch circuits, \( P_{reset} \) device, and a diagnostic (static_evaluate) weak pMOS (\( P_{reset} \)) device. The GDI tree is a parallel/series network of nMOS and pMOS devices between ground and the inputs to the output inverters (the dynamic storage nodes). The GDI network is incorporated with level restoration circuit for full swing output. The delay path is limited with one inverter in order to have smaller pulse width to avoid the contention problem between the GDI network and the dynamic nodes. This structure produces equal fall and rise delay. The delay line should be implemented with odd number of inverters in order to ensure the correct transition (ON and OFF) for \( P_{reset} \) transistor charging and discharging the dynamic capacitor \( C_y \). The inverter at the output node produces both true and complementary outputs.

The illustration and the working principle of SRLGDI AND cell are shown in Fig. 8. The GDI block is constructed using (P1, P2, P3) and (N1, N2, N3) pMOS and nMOS transistors which are used to realize the function A.B. The transistors P4 and N4 which are connected between the dynamic and output node eliminates the contention and cascading problem. The delay path is formed by the transistors P5 and N5 which control the ON/OFF transition of \( P_{reset} \) charge keeper circuit. The output inverter constructed using the transistors P6 and N6 provides the true output of the function A.B. During the precharge phase (\( CLK = 0 \)) the \( P_{reset} \) transistor is ON, which makes the dynamic node to be high and in turn it makes N4 to be ON and P4 to be OFF. The output of the dynamic inverter is low, making the transistors P5 ON and N5 OFF resulting in high output which in turn it ceases the conduction of \( P_{reset} \) transistor. During the precharge phase there will not be any conduction path between GDI block and dynamic node. The gate level representation of SRLGDI AND gate during the precharge phase is portrayed in Fig. 8a.
During the evaluation phase (CLK = 1) the \( P_{\text{preset}} \) transistor is OFF, so the dynamic node gets discharged due to the non-existence of path between \( P_{\text{preset}} \) transistor, which makes the transistors P4 ON and N4 OFF exhibiting high logical level, in turn the delay inverter (P5 is OFF and N5 is ON) is OFF thereby the \( P_{\text{reset}} \) transistor becomes ON and holds the dynamic node high. Throughout this period, for the inputs “00”, “01” and “10” there will not be any conduction path existing between GDI block and dynamic node which makes the output to remain at a low logical level. The switching behaviour during the evaluation phase for the inputs “00”, “01” and “11” is illustrated in Fig. 8b. For the input “11” the output of GDI block is high which connects the dynamic node to output node resulting in a high logical level. During this time, the inverter between the dynamic node and output node is low; in turn it makes the delay inverter ON thereby restoring the \( P_{\text{reset}} \) transistor its initial condition. The switching behaviour during the input transition “11” is elucidated in Fig. 8c. The input/output wave form of SRLGDI AND gate is shown in Fig. 9. Only for CLK = 1 and input \( A = 1 \) and \( B = 1 \), the output is high and for the remaining cases the output remains low.

### 3.5. RC delay model for SRLGDI logic

SRLGDI supports pulse-mode operation; therefore it is necessary to formulate the static timing analysis to find the rising and falling transition. To ensure the correct operation of pulse based circuit, the pulses arriving at different inputs must be active for a specified period of time. For SRLGDI the gate will generate an output pulse only if the inputs are valid or the
output will remain at zero. The timing parameters used in the derivation of rise and fall time are:

\[ t_{\text{preset}} = \frac{R_{\text{preset}} \cdot C_Y}{V_{DD}} \]  
\[ t_{\text{reset}} = (C_Y + C_{\text{out}}) \frac{R_{\text{reset}} R_{\text{GDI}} + R_{\text{eq}} (R_{\text{reset}} + R_{\text{GDI}})}{R_{\text{reset}} + R_{\text{GDI}}} \]  
\[ R_{\text{eq}} = \frac{R_{\text{inv}} \cdot R_{\text{delay}}}{R_{\text{inv}} + R_{\text{delay}}} \]

where \( R_{\text{eq}} \) is the equivalent resistance of the inverter and delay line.

The RC switching delay during precharge and evaluation phases is shown in Fig. 10. During precharge the \( I_{\text{preset}} \) transistor is ON and makes the dynamic capacitor to charge to \( V_{DD} \). Thus the output pulse will be zero due to open circuit behaviour of GDI block and the output inverter. During the evaluation phase a combination of active high inputs creates a conduction path between the bottom of the GDI block tree and ground. This forces the node at the top of the logic tree to its active low state and switches the output inverter to create an active high output signal. The active high output causes the reset transistor to be ON and conditionally discharge the dynamic storage nodes to evaluate the desired logic function thus resetting these nodes back to their original charged state due to the delay inverter chain.

During precharge:

\[ t_{\text{preset}} = \frac{R_{\text{preset}} \cdot C_Y}{V_{DD}} \]  

During evaluation when grounding \( V_{DD} \):

\[ t_{\text{reset}} = (C_Y + C_{\text{out}}) \frac{R_{\text{reset}} R_{\text{GDI}} + R_{\text{eq}} (R_{\text{reset}} + R_{\text{GDI}})}{R_{\text{reset}} + R_{\text{GDI}}} \]  

where \( R_{\text{eq}} = \frac{R_{\text{inv}} \cdot R_{\text{delay}}}{R_{\text{inv}} + R_{\text{delay}}} \)

To generalize Eq. (4)
So the total delay of SRLGDI circuit is 

\[ t_d = \frac{t_{\text{preset}} + t_{\text{reset}}}{2} \]  

The width of the output pulse \( W_p \) depends strongly on the characteristics of the output stage of the gate. So the delay of SRLGDI gate depends on the width of the output pulse, delay of the feedback inverter chain and delay of the GDI block.

**Figure 8** Operational characteristics of SRLGDI AND gate (a) switching behaviour during precharge phase (b) switching behaviour during evaluation phase for the inputs “00”, “01” and “11” (c) switching behaviour during the input transition “11”.

\[ t_{\text{reset}} = W_p + t_{\text{df}} + t_{\text{gd}} \]  

So the total delay of SRLGDI circuit is 

\[ t_d = \frac{t_{\text{preset}} + t_{\text{reset}}}{2} \]
4. General virtues of the proposed SRLGDI logic

The subsequent topics explain the general merits of the proposed SRLGDI logic with the existing dynamic SRCMOS logic in terms of subthreshold leakage, charge sharing and monotonicity requirements.

4.1. Reduction of subthreshold current in SRLGDI

The proposed structure realized using GDI technique will reduce the subthreshold leakage during precharge and evaluation phases. As in the case of nMOS structure the subthreshold leakage is predominant due to ON state of nMOS and pMOS stack. Nevertheless in the case of the proposed SRLGDI there is no chance that all the transistors are ON at the same time whatever may be the input combination. To elucidate this condition the switching activity of basic GDI cell is presented. Consider the case when the control input at terminal $V_G$ is low, P-diffusion input $V_P$ is high and N-diffusion input $V_N$ is low, which makes the pMOS device to enter into linear region and the device is set to be in ON state, while nMOS enters into cut-off region and the device is OFF which produces direct path between $V_P$ and output (refer Fig. 2). Consequently the output of the multiplexer will be high. The switching characteristic of basic GDI cell is shown in Fig. 11. The transistor behaviour for various input combinations along with the pMOS and nMOS device characteristics is listed in Table 1.

The subthreshold current is high for nMOS device. During the precharge phase when the entire nMOS device is OFF the effect of leakage current between the nMOS stack to VDD of pMOS stack is predominant. The leakage current for SRCMOS and the proposed SRLGDI is calculated for various $V_{gs}$ using Hspice and its result is depicted in Fig. 12. The graph is plotted against gate-source voltage ($V_{gs}$) and subthreshold current (Ids). Fig. 12(a) shows the subthreshold leakage of series nMOS stack with properly biased substrate input. Similarly Fig. 12(b) presents the subthreshold leakage of series GDI stack with different substrate ($V_b$) inputs. It is noticed that the subthreshold leakage is 4.0 mA for $V_{gs}$ nearly equal to 0.8 which is very high when compared to GDI block with the same applied condition having 2.0 mA. This shows that the proposed SRLGDI consumes nominal leakage current when compared to the existing dynamic SRCMOS logic (see Fig. 12).

4.2. Monotonicity requirement

A fundamental difficulty with dynamic circuits is a loss of noise immunity and a serious timing restriction on the inputs of the gate. During the evaluation phase the input signal must never change to validate the correct operation of logic function, which is addressed as the monotonicity problem. In the proposed logic the inverter between the dynamic node and the output node will completely eliminate the timing restriction. Consider the case, when the CLK = 0 the output voltage of the dynamic gate is elevated by the $P_{preset}$ transistor, thereby the output of the inverter will necessarily be low. Therefore, during evaluation, the signal can only remain low or change from low to high, so the undesirable high to low transition is prevented. During cascading one circuit to another circuit the timing restriction is nullified due to the presence of a reset circuit (the delay path) which commands the precharge transistor to a ready state so that it can accept input signals and perform the logical operation correctly.

4.3. Reduction of charge leakage in SRLGDI

The main limitation in the existing dynamic logic is the potential logic upset due to the charge sharing effects. This charge sharing problem occurs internally due to the charge inversion under the gate oxide region and cascading the load and driver

![Input/output simulation waveform of SRLGDI AND gate for the input voltage of 5 V.](image-url)
connected between two dynamic circuits. In the proposed SRLGDI the charge sharing problem is minimized using the pMOS transistor \( P_{\text{reset}} \). After precharge, the \( P_{\text{reset}} \) pMOS device is ON and it continues to pull up the node even after the precharge phase is complete. The other added features of the proposed SRLGDI logic are:

- The signals that propagate through these circuits are pulses to ensure the correct operation when it is cascaded with multiple devices.
- The data present at evaluation does not require dynamic node to discharge, the precharge device is not active hence reducing power.
- The stringent timing constraints encountered in pulse mode circuits can be relaxed without affecting circuit robustness.
- By using a buffered form of the input, the input loading is kept almost as low as in the normal dynamic logic while local generation of the reset assures that it is properly timed and occurs only when needed.
- Fast cycle time and minimum delay are observed when compared to dynamic SRCMOS logic.
- No global clock is required thus it reduces the synchronization problem.

To fulfill the requirement of monotonicity, charge sharing and cascading effects, multiple inverters, delay path inverters and level restoration circuit have been incorporated which slightly increase the total gate count of the circuit, which is the only deficit of the proposed SRLGDI logic.

5. Simulated results

The proposed SRLGDI primitives are simulated using Tanner EDA with BSIM 0.250 \( \mu \)m technology with supply voltage ranging from 0 V to 5 V in steps of 0.2 V. All the primitive gates are simulated with same setup. The test bed is supplied with a nominal voltage of 5 V in steps of 0.2 V and it is invoked with the technology library file Generic 025. To establish an unbiased testing environment, the simulations have been carried out using a comprehensive input signal pattern, which covers every possible transition for a logic gate. All the primitive structures are implemented in CMOS, Dynamic logic (DY), SRCMOS and SRLGDI with the same set up.
Table 1 Operational characteristics of basic GDI cell.

<table>
<thead>
<tr>
<th>Input $V_G$</th>
<th>Input $V_N$</th>
<th>Input $V_P$</th>
<th>PMOS device characteristics</th>
<th>NMOS device characteristics</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>0</td>
<td>0</td>
<td>Linear: $V_P - V_{TP} &lt; V_{out} &lt; V_{DD}$</td>
<td>Cut-off: $V_N &lt; V_{TN}$</td>
</tr>
<tr>
<td>0</td>
<td>0</td>
<td>1</td>
<td>Linear: $V_P - V_{TP} &lt; V_{out} &lt; V_{DD}$</td>
<td>Cut-off: $V_N &lt; V_{TN}$</td>
</tr>
<tr>
<td>0</td>
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<td>Linear: $V_P - V_{TP} &lt; V_{out} &lt; V_{DD}$</td>
<td>Cut-off: $V_N &lt; V_{TN}$</td>
</tr>
<tr>
<td>0</td>
<td>1</td>
<td>1</td>
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<tr>
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<td>0</td>
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<td>Linear: $0 &lt; V_{out} &lt; V_N - V_{TN}$</td>
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<tr>
<td>1</td>
<td>0</td>
<td>1</td>
<td>Cut-off: $V_P &gt; V_{DD} + V_{TP}$</td>
<td>Linear: $0 &lt; V_{out} &lt; V_N - V_{TN}$</td>
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<td>1</td>
<td>1</td>
<td>Cut-off: $V_P &gt; V_{DD} + V_{TP}$</td>
<td>Linear: $0 &lt; V_{out} &lt; V_N - V_{TN}$</td>
</tr>
</tbody>
</table>

Figure 11 Switching activity of GDI cell.

Figure 12 Subthreshold leakage current (a) nMOS stack (b) pMOS stack.
providing the same temperature, biasing, aspect ratio and testing condition.

All transitions from one input combination to another have been tested, and the delay at each transition has been measured. The average has been reported as the cell delay. The power consumption is also measured for these input patterns and its average power is reported. Table 2 shows the performance of SRLGDI.
with other logic like CMOS, GDI, SRCMOS and Dynamic logic.

6. Proposed full adders

Addition is an indispensable operation for any high speed digital system, digital signal processing or control system. The primary issues in the design of adder cell are area, delay and power dissipation. Several adder topologies have been reported by Uma and Dhavachelven (2012a,b,c), Shubin (2011), Aguirre-Hernandez (2011), Mirzaee et al. (2010), Ghardiry et al. (2010) and Navi et al. (2008). The proposed adder circuit realizations are shown in Fig 13. Adder1 is implemented with XOR and multiplexer. The sum logic is evaluated by XOR gate and carry logic is realized using MUX. Adder2 is designed using XNOR and MUX with sum realization using XNOR and MUX, while carry logic is structured using

Table 2: Performance of self-resetting logic with gate diffusion input primitive cells with other logic families. (Delay in ns, Power (PWR) in μW, Transistor count (#tr).

<table>
<thead>
<tr>
<th>Library</th>
<th>CMOS</th>
<th>DY</th>
<th>SRCMOS</th>
<th>GDI</th>
<th>Proposed SRLGDI</th>
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<tr>
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<td>99.28</td>
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<tr>
<td>NAND</td>
<td>19.98</td>
<td>140.12</td>
<td>4</td>
<td>17.45</td>
<td>120.12</td>
</tr>
<tr>
<td>NOR</td>
<td>10.04</td>
<td>89.69</td>
<td>4</td>
<td>8.65</td>
<td>82.69</td>
</tr>
<tr>
<td>XOR</td>
<td>5.21</td>
<td>96.74</td>
<td>14</td>
<td>4.04</td>
<td>98.74</td>
</tr>
<tr>
<td>XNOR</td>
<td>5.054</td>
<td>98.23</td>
<td>14</td>
<td>4.456</td>
<td>102.23</td>
</tr>
</tbody>
</table>

Complementary Metal Oxide Semiconductor (CMOS), Dynamic logic (DY), Self Resetting Complementary Metal Oxide Semiconductor (SRCMOS), Gate Diffusion Input (GDI) and proposed Self Resetting Logic with Gate Diffusion Input (SRLGDI).

Figure 14: Input/output transition of self-resetting logic with gate diffusion input adder1 with different inputs operating at 100 MHz clock frequency, time in ns and Voltage ranging from 0 V to 5 V.
MUX. Adder3 is proposed with XNOR and MUX with sum evaluation using XNOR and carry using MUX. To test the performance of the proposed and existing adders, detailed comparisons were performed. The simulations were run with the Tanner software. All the schematics are based on TSMC 0.250 μm technology with supply voltage ranging from 1.2 V to 5 V in steps of 0.2 V. All the full adders are simulated with multiple design corners (TT, FF, FS, and SS) to verify that operation across variations in device characteristics and environment. The W/L ratios of both nMOS and pMOS transistors are taken as 2.5/0.25 μm. The circuits are simulated with a 100 MHz clock frequency. The operation of the proposed SRLGDI adders is based on dynamic logic characteristics, the input should be changed in the precharge phase and the results are obtained during the evaluation phase. The delay parameter is calculated from all the transitions from an input combination to another, and the delay at each transition has been measured from the time when the clock signal reaches 50% of the supply level.

Power delay product (PDP) has been calculated by taking the product term of delay and average power consumption. The input/output waveform generated for SRLGDI adder1 with clock frequency of 100 MHz is shown in Fig 14. The waveform indicates the complete transition characteristics of SRLGDI adder with the three inputs A, B and C having the bit patterns (000, 001, 010, 011, 100, 101, 110 and 111). The input patterns are changed only during the precharge phase. The output shows the full swing voltage because of the level restoration circuit in GDI network.

In this study the performance evaluation of the proposed adders is compared with the different logic families and the existing adders. Table 3 presents the performance of adder1, adder2, and adder3 with different logic families in terms of delay, power and transistor count. Table 4 shows the performance comparison of the proposed and existing adders.

### Table 3 Performance comparison of the proposed adders with different logic families (Delay in ns, Power in μW, Transistor count #tr, Power–delay product (PDP) μW × ns in fW-s).

<table>
<thead>
<tr>
<th>Present study</th>
<th>SRLGDI</th>
<th>GDI</th>
<th>CMOS</th>
<th>DY</th>
<th>SRCMOS</th>
</tr>
</thead>
<tbody>
<tr>
<td>Adder1</td>
<td>Delay</td>
<td>22.2</td>
<td>33.1</td>
<td>35.4</td>
<td>28.2</td>
</tr>
<tr>
<td></td>
<td>PWR</td>
<td>200.1</td>
<td>188.9</td>
<td>402.2</td>
<td>350.2</td>
</tr>
<tr>
<td></td>
<td>#tr</td>
<td>34</td>
<td>18</td>
<td>38</td>
<td>40</td>
</tr>
<tr>
<td></td>
<td>PDP</td>
<td>4442.22</td>
<td>6252.59</td>
<td>14237.88</td>
<td>9875.64</td>
</tr>
<tr>
<td>Adder2</td>
<td>Delay</td>
<td>29.1</td>
<td>36.5</td>
<td>40.3</td>
<td>30.2</td>
</tr>
<tr>
<td></td>
<td>PWR</td>
<td>212.4</td>
<td>202.6</td>
<td>531.4</td>
<td>459.7</td>
</tr>
<tr>
<td></td>
<td>#tr</td>
<td>44</td>
<td>22</td>
<td>48</td>
<td>46</td>
</tr>
<tr>
<td></td>
<td>PDP</td>
<td>6180.84</td>
<td>7394.9</td>
<td>21415.42</td>
<td>13882.94</td>
</tr>
<tr>
<td>Adder3</td>
<td>Delay</td>
<td>23.3</td>
<td>36.2</td>
<td>38.8</td>
<td>26.3</td>
</tr>
<tr>
<td></td>
<td>PWR</td>
<td>235.4</td>
<td>210.9</td>
<td>545.3</td>
<td>434.2</td>
</tr>
<tr>
<td></td>
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<td>34</td>
<td>18</td>
<td>38</td>
<td>40</td>
</tr>
<tr>
<td></td>
<td>PDP</td>
<td>5484.82</td>
<td>7634.58</td>
<td>21157.64</td>
<td>11419.46</td>
</tr>
</tbody>
</table>

Self Resetting Logic With Gate Diffusion Input (SRLGDI), Gate Diffusion Input (GDI), Complementary Metal Oxide Semiconductor (CMOS), Dynamic logic (DY) and Self Resetting Complementary Metal Oxide Semiconductor (SRCMOS).

### Table 4 Performance comparison of the proposed and existing adders (Delay in ns, Power in μW, Transistor count #tr, Power–delay product (PDP) μW × ns in fW-s).

<table>
<thead>
<tr>
<th></th>
<th></th>
<th></th>
<th></th>
<th></th>
<th></th>
<th></th>
<th></th>
<th></th>
<th></th>
<th></th>
<th></th>
</tr>
</thead>
<tbody>
<tr>
<td>Delay</td>
<td>22.2</td>
<td>29.1</td>
<td>23.3</td>
<td>36.34</td>
<td>35.67</td>
<td>32.31</td>
<td>32.87</td>
<td>37.2</td>
<td>40.23</td>
<td>39.78</td>
<td>38.45</td>
</tr>
<tr>
<td>Power</td>
<td>200.12</td>
<td>212.45</td>
<td>235.45</td>
<td>196.78</td>
<td>203.67</td>
<td>194.35</td>
<td>275.98</td>
<td>315.67</td>
<td>215.13</td>
<td>234.56</td>
<td>387.65</td>
</tr>
<tr>
<td>#tr</td>
<td>34</td>
<td>44</td>
<td>34</td>
<td>18</td>
<td>18</td>
<td>14</td>
<td>15</td>
<td>14</td>
<td>15</td>
<td>26</td>
<td>16</td>
</tr>
<tr>
<td>PDP</td>
<td>4442.664</td>
<td>6182.295</td>
<td>5486.218</td>
<td>7150.985</td>
<td>7264.909</td>
<td>6729.449</td>
<td>9071.463</td>
<td>11742.92</td>
<td>8654.68</td>
<td>9330.797</td>
<td>14905.14</td>
</tr>
</tbody>
</table>

7. Discussion

A new family of self-resetting logic (SRL) cells implemented with GDI technique is presented. The proposed primitive cells have been tested against its existing techniques in terms of delay, power and PDP which are report in Table 2. The comparison result is shown in Fig. 15. The proposed SRLGDI primitive cells and the adder cells perform better than different logic and existing counterparts. Table 5 depicts the percentage of improvement in delay, power and PDP of adder1, adder2, and adder3 with respect to different logic. The analysis of the proposed study illustrates progressive improvements with CMOS logic in terms of delay, power and PDP when compared...
with other logic families. The negative sign in the table indicates an increase in power consumption factor. The overall delay improvement is 32.45%, achieved with different logic families. Expect for GDI logic the proposed adders have nearly 60% of power improvement. The PDP improvement of the proposed adders with different logic families is shown in Fig 16. Table 6 elucidates the performance improvement for PDP of the proposed SRLGDI adders with the existing adders.

![Delay of Primitive cell in various logic](image)

![Power consumption of primitive cell](image)

![Power-Delay Product of Primitive Cell](image)

**Figure 15** Performance of primitive cell of SRLGDI logic (a) delay performance (b) power comparison (c) Power-delay product.

**Table 5** Percentage of improvement in delay, power and PDP of adder1, adder2, and adder3 with respect to different logic.

<table>
<thead>
<tr>
<th>Logic</th>
<th>Present Study</th>
<th>Percentage of improvement in delay, power and PDP with respect to different logic</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>GDI</td>
<td>CMOS</td>
</tr>
<tr>
<td>Adder1</td>
<td>32.93</td>
<td>5.929</td>
</tr>
<tr>
<td>Adder2</td>
<td>20.27</td>
<td>-5.929</td>
</tr>
<tr>
<td>Adder3</td>
<td>35.64</td>
<td>-11.62</td>
</tr>
</tbody>
</table>

Self-Resetting Logic with Gate Diffusion Input (SRLGDI), Gate Diffusion Input (GDI), Complementary Metal Oxide Semiconductor (CMOS), Dynamic logic (DY) and Self Resetting Complementary Metal Oxide Semiconductor (SRCMOS).
study it is examined that the PDP improvement of adder1 is well enunciated when compared to the proposed adder2 and adder3. The performance improvement in PDP in the proposed adders with existing adders is illustrated in Fig. 17. It is recognized that for all the proposed adders the PDP is much better in Navi et al. (2008); when compared to the other existing adders. To consolidate this study adder1 designed with XOR and MUX produces significant improvements in terms delay, power and PDP with its existing counterparts.

8. Conclusion

The proposed structure does not require global clock therefore the SRLGDI structure will not encounter into any clock distribution problem. The transistor incorporated between dynamic node acts as a charge keeper circuit to pull the output node high in order to maintain the signal integrity. The loading effect and the monotonicity requirement have been surrogated by the proposed SRLGDI logic. The performance of these proposed primitive cells in SRLGDI presents 62% of power reduction when compared to other logic families with a slight increase in transistor count. About 38% of delay reduction has been achieved using this SRLGDI logic. Three adders have been proposed and its performance have been evaluated with different logic families and existing adders. The proposed SRLGDI adder cell performs better than different logic and existing counterparts. While comparing the three adders, adder1 designed with XOR and MUX presents low power

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**Figure 16** Performance improvement of PDP with Gate Diffusion Input (GDI), Complementary Metal Oxide Semiconductor (CMOS), dynamic logic (DY) and Self-resetting (SRCMOS).

**Figure 17** Performance improvement of Power Delay Product (PDP) between present study and existing adders.

---

**Table 6** Percentage of improvement in power delay product (PDP) of adder1, adder2, and adder3 with respect to existing adders.

<table>
<thead>
<tr>
<th>Existing adders</th>
<th>Present study adder1 % PDP improved</th>
<th>Present study adder2 % PDP improved</th>
<th>Present study adder3 % PDP improved</th>
</tr>
</thead>
<tbody>
<tr>
<td>Uma and Dhavachelvan (2012a)</td>
<td>37.87</td>
<td>13.55</td>
<td>23.28</td>
</tr>
<tr>
<td>Uma and Dhavachelvan (2012b)</td>
<td>38.85</td>
<td>14.9</td>
<td>24.48</td>
</tr>
<tr>
<td>Uma and Dhavachelvan (2012c)</td>
<td>29.25</td>
<td>15.47</td>
<td>12.63</td>
</tr>
<tr>
<td>Shubin (2011)</td>
<td>51.03</td>
<td>31.85</td>
<td>39.52</td>
</tr>
<tr>
<td>Aguirre-Hernandez (2011)</td>
<td>62.17</td>
<td>47.35</td>
<td>53.28</td>
</tr>
<tr>
<td>Mirzaee et al. (2010)</td>
<td>48.67</td>
<td>28.57</td>
<td>36.61</td>
</tr>
<tr>
<td>Ghadiry et al. (2010)</td>
<td>52.39</td>
<td>33.74</td>
<td>41.2</td>
</tr>
<tr>
<td>Navi et al. (2008)</td>
<td>70.19</td>
<td>58.52</td>
<td>63.19</td>
</tr>
</tbody>
</table>
and less delay when compared to adder1 and adder2. On the whole about 32% of improvement in delay, 58% of power and 60% of PDP have been achieved using this proposed SRLGDI logic. To fulfill the requirement of monotonicity, charge sharing and cascading effects, multiple inverters, delay path inverters and level restoration circuit have been incorporated which slightly increase the total gate count of the circuit, which is the only deficit of the proposed SRLGDI logic.

References


