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Design of Low Noise Amplifier for IEEE standard 802.11b using Cascode and Modified Cascode Techniques

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Abstract

This paper presents the performance comparison of two Low Noise Amplifiers (LNA), a basic Cascode and a modified cascode LNA for IEEE 802.11b protocol, WLAN. A modified cascode LNA with dual Common source transistors is designed and the performance parameters are compared with a designed basic cascode stage. The modified cascode stage has a high gain of 19.2dB and an optimized noise figure of 0.416dB at 2.4GHz and at a supply voltage of 1.8V. The S11 is -13.74dB, S22 is -0.87dB and S12 is -43.63dB. The P1dB is -18.35dBm and the IIP3 is -84.42dBm. The LNA is designed to be stable over 2-3GHz range. The power consumption of the circuit is 8.1mW. The modified cascode LNA is having around 10% improvement in gain and a 40% reduction in noise figure compared to the basic Cascode LNA. The simulations are done in cadence virtuoso Spectre RF using 180nm technology.

Keywords: third order intercept point; Stability; Noise Figure; 1dB compression point

1. Introduction

The recent development in the field of wireless technologies have raised the importance of broadband wireless access systems in which the performance of Wireless Local Area Network (WLAN) is of great importance. The prevalent WLAN protocol, IEEE 802.11b is in the 2.4GHz industrial, scientific and medical (ISM) band. To increase

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the system sensitivity a Low Noise Amplifier (LNA) with good performance is mandatory since it is the first stage amplifier in the receiver. According to Frii’s formula, the first stage of the receiver contributes mainly to the overall Noise Figure (NF) of the receiver. So it is important to design LNA’s with minimum NF. The main performance parameters of LNAs are gain, Noise Figure (NF), linearity, Impedance matching and stability [1]. The forward gain of the LNA is defined by the S parameter, S21. The NF is defined as the ratio of signal to Noise Ratio (SNR) at the input to the SNR at the output. Third-Order intercept point (IP3) and 1dB compression point (P1dB) are the measures of linearity. The stability of an LNA is also important. An LNA is stable if it satisfies the condition Rollet’s stability factor, K>1. But always there will be a tradeoff between the design parameters.

This paper presents the design and analysis of a cascode LNA with low noise figure and high gain. Further the design has been modified using dual common source transistors to further improve the gain and optimize the noise figure.

The organization of the paper is as follows. Section 2 deals with the specifications formulated for the LNA design and the design aspects of cascode and modified cascode LNA. Section 3 discusses about the simulation results. Section 4 describes the conclusion.

2. Low Noise Amplifier Design considerations

The design specifications formulated for the design of IEEE 802.11b is shown in Table I. The LNA designed for WLAN should have high gain greater than 15dB and a low NF less than 3dB. It should also have good linearity especially in an environment with weak signal strength. The minimum signal power at which a receiver can detect a signal while providing an adequate SNR at analog receiver output is called receiver sensitivity. For a typical WLAN, the sensitivity ranges from -76dBm to as good as -92dBm [2].

<table>
<thead>
<tr>
<th>Design Parameters</th>
<th>Range</th>
</tr>
</thead>
<tbody>
<tr>
<td>Frequency(GHz)</td>
<td>2.4</td>
</tr>
<tr>
<td>Technology</td>
<td>180nm</td>
</tr>
<tr>
<td>Supply Voltage</td>
<td>1.8V</td>
</tr>
<tr>
<td>Noise Figure (dB)</td>
<td>&lt;3dB</td>
</tr>
<tr>
<td>Gain(dB)</td>
<td>&gt;15dB</td>
</tr>
<tr>
<td>Power consumption(mW)</td>
<td>&lt;10mW</td>
</tr>
<tr>
<td>Third Order Intercept Point(dBm)</td>
<td>&gt;-10 dBm</td>
</tr>
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</table>

2.1. Basic Cascode with inductive degeneration(L-CSLNA)

All the inductively degenerated topology [3], is narrow-band since the input matching circuit consisting of the source inductors and the gate to source capacitance, Cgs, resonates at a single frequency. The input of an L-CSLNA forms a series RLC network as shown in Fig 1(a). The inductively degenerated LNA is the dominating topology for narrowband systems due to its advantages such as low NF, ease of input matching, high gain, and low-power consumption. The input impedance of the stage is given by the equation,

\[ Z_{in} = s(L_1 + L_g) + \frac{1}{sC_{gs}} + \left(\frac{g_m}{C_{gs}}\right)L_1 \]  

(1)

The most commonly used topology for LNA design is the cascode amplifier with inductive source degeneration [4]. The cascode topology has a higher gain, due to the increase in the output impedance. The cascode transistor suppresses the Miller capacitance of the input device thereby increasing the reverse isolation.
Fig 1(b) shows the basic cascode LNA with parallel resistor for stabilization. The NF of the LNA is given by the equation,

\[ NF = 1 + \frac{g_m R_S}{R_1} \left( \frac{\omega_0}{\omega_T} \right)^2 + \frac{4 R_1}{R_1} \left( \frac{\omega_0}{\omega_T} \right)^2 \]  

(2)

From the equation of NF the noise contribution of R1 is negligible, if the operation frequency (\(\omega_o\)) is lesser than \(\omega_T\) of the transistor. The gain of the LNA is given by the equation,

\[ \frac{V_{out}}{V_{in}} = \frac{\omega_T R_1}{2\omega_o R_s} = \frac{R_1}{2L_1\omega_o} \]  

(3)

The equations from (4) to (9) are used to design the source inductor \(L_1\), gate inductor \(L_g\), drain inductor \(L_d\) and width of the input device \(W\).[5]

\[ L_1 = \frac{g_m}{C_{gs}} = \frac{R}{\omega_T} \]  

(4)

\[ \omega_T = 2\pi f_T \]  

(5)

\[ L_g = \frac{q_1 R_s}{\omega_0} - L_1 \]  

(6)

\[ L_d = \frac{1}{\omega_0 2C_L} \]  

(7)

\[ C_{gs} = \frac{1}{\omega_0^2 (L_g + L_1)} \]  

(8)

\[ W = \frac{3 C_{gs}}{2C_{ox} L_{min}} \]  

(9)

where \(g_m\) is the trans conductance of the device, \(C_{gs}\) is the gate source capacitance and \(R_s\) is the source resistance which is equal to 50\(\Omega\) in equation (4). \(f_T\) in equation (5) is the unity gain frequency of the MOS transistor. \(Q_L\) (equation (6)) is the Q factor of the inductance which is chosen as 2.67. \(\omega_o\) is the centre frequency which is chosen to be 2.4GHz. In equation (9) \(C_{ox}\) is the oxide capacitance and \(L_{min}\) is the minimum channel length which is 180nm in this design.

2.2 Modified Cascode with dual Common Source Transistors

In the cascode amplifier design, the common source stage is the most important part for high performances, because the noise figure of the amplifier depends on this stage. The gate width and gate-source voltage of the common source stage transistor are adjusted for good performances. But the multiple demands like NF and linearity of LNA cannot be achieved by optimizing only the gate width and voltage of the transistor. To fulfill the multiple demands, the cascode amplifier is modified by adding an additional transistor to the common source stage [6] as shown in Fig 2(a). This LNA makes use of dual CS transistors in the CS stage. For optimizing the design parameters the two transistors Q1 and Q2 have different gate width and gate source voltage. The noise figure can be improved by minimizing the size of the input device. The advantage of the circuit is that the gate source capacitance and the device currents are paralleled as shown in the equivalent circuit in Fig. 2(b). The total drain current is given by,

\[ I_{total} = I_{D1} + I_{D2} = \beta \left[ W_1 (V_{GS1} - V_T)^2 + W_2 (V_{GS2} - V_T)^2 \right] \]  

(10)
3. Simulation Results and Discussion

3.1 Basic Cascode LNA

To evaluate the performance of the modified cascode circuit, initially a cascode circuit with parallel resistive stabilizing network is designed as a benchmark circuit as shown in Fig. 3(a). Here \( L_{\text{min}} \) is chosen to be 180nm. \( \omega_0 \) is the centre frequency which is 2.4 GHz and \( R_s \) is chosen to be equal to 50\( \Omega \). The aspect ratio of the input device is 50\( \mu \)/180\( \mu \). The aspect ratio of the cascode device is chosen to be half of the input device for good performance. Using the I-V characteristics in Fig. 3(b), the gate voltage is fixed to 0.72V, corresponding to a drain current of 3.35mA. From Fig. 4(a), the gain of the cascode stage is 17.49dB and the NF is 0.7dB. The stability parameter, \( K_f \) is greater than one over 2-3GHz which shows that the designed LNA is stable over the specified frequency range. The S12 of the cascode LNA is -46.12dB. The S11 and S22 are -3.6dB, -0.68dB respectively which is shown in Fig. 4(b). The power consumption of the circuit is 5.96mW.
The periodic steady state analysis (PSS) is done to plot the output power with the two tones at 2.4GHz (f1) and 2.5GHz (f2). The input power is swept from -30 to 0dBm. To plot the IIP3 the 1st order and 3rd order frequency is chosen as 2.4 and 2.3GHz respectively. The P1dB of the circuit is -18.19dBm (Fig. 5(a)). The IIP3 measured at a Pin of -20dBm is -8.45dBm as shown in Fig. 5(b).

3.2 Modified Cascode LNA

Fig.6 (a) shows the circuit diagram of the modified cascode LNA. The width of the added transistor, M2 is chosen to be 20µ which is less than the cascode device for better performance. The S parameters and NF of the LNA is shown in Fig. 6(b). The LNA is designed to be stable over the 2-3GHz range which is shown by the Kf parameter. The gain of the circuit is 19.2dB which shows an improvement of 1.7dB. The NF is 0.416dB which shows a reduction of 40% from the basic cascode. The periodic steady state analysis (PSS) is done to plot the output power with the two tones at 2.4GHz (f1) and 2.5GHz (f2). The P1dB is calculated from Fig.7 (a). The input power is swept from -30 to 0dBm. To plot the IIP3 the 1st order and 3rd order frequency is chosen as 2.4 and 2.3GHz respectively. From Fig 7(b) it is evident that the output plot is fairly flat up to around -40dBm. The IIP3 measured at a Pin of -20dBm is -8.4dBm.

Fig.6. (a) Circuit diagram of modified cascode LNA; (b) Performance parameters of modified cascode LNA

Fig 7. (a)P1dB (b) IIP3 of modified cascode LNA
4. Conclusions

From Table II, it is evident that the designed modified cascode LNA with dual CS transistors is having 10% improvement in gain and 40% reduction in noise figure compared to the basic cascode stage. The modified cascode LNA is having a very low noise figure of 0.416dB and a high gain of 19.2dB. The return loss, S11 is reduced to -13.74dB. The circuit is also having a very low reverse isolation, S12 which is -43.63dB. The IIP3 of the modified stage is -8.4dBm. Unlike the cascode stage the modified cascode LNA is having a constant output power up to an input power of -40dBm. Table III shows the comparison of the modified cascode LNA with state-of-the-art LNA’s designed at 180nm technology. From the comparison it can be shown that the designed modified cascode LNA is having a very low noise figure. Since the WLAN applications require an excellent LNA which can work in the noisy environment, the modified cascode LNA with minimum noise figure, high gain, good linearity and low power consumption will be apt in the receiver module of IEEE 802.11b.

Table II. Comparison of cascode and modified cascode LNA

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<tr>
<th>Design Parameters</th>
<th>Basic Cascode</th>
<th>Modified Cascode</th>
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<tr>
<td>VDD(V)</td>
<td>1.8V</td>
<td>1.8V</td>
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<tr>
<td>Kf</td>
<td>1.33</td>
<td>1.61</td>
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<tr>
<td>S21(dB)</td>
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<tr>
<td>NF(dB)</td>
<td>0.7</td>
<td>0.416</td>
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<tr>
<td>S11(dB)</td>
<td>-3.6</td>
<td>-13.74</td>
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<tr>
<td>S22(dB)</td>
<td>-0.68</td>
<td>-0.87</td>
</tr>
<tr>
<td>S12(dB)</td>
<td>-46.09</td>
<td>-43.63</td>
</tr>
<tr>
<td>P1dB(dBm)</td>
<td>-18.19</td>
<td>-18.35</td>
</tr>
<tr>
<td>IIP3(dBm)</td>
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<tr>
<td>Power(mW)</td>
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Table III. Comparison of Performance Parameters of Modified Cascode with Existing LNAs at 180nm Technology

<table>
<thead>
<tr>
<th>Ref</th>
<th>Freq(GHz)</th>
<th>NF(dB)</th>
<th>Gain(dB)</th>
<th>IIP3(dBm)</th>
<th>Power(mW)</th>
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<tr>
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<td>8</td>
<td>2.2</td>
<td>3.53</td>
<td>16.7</td>
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<td>9</td>
<td>2.2</td>
<td>1.92</td>
<td>8.4</td>
<td>-2.55</td>
<td>9</td>
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<tr>
<td>10</td>
<td>2.4</td>
<td>2</td>
<td>18.9</td>
<td>2.42</td>
<td>4.3</td>
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<td>11(IEEE 802.11a)</td>
<td>5</td>
<td>2.2</td>
<td>25.4</td>
<td>-</td>
<td>-</td>
</tr>
<tr>
<td>This Work(Simulated modified cascode)</td>
<td>2.4</td>
<td>0.416</td>
<td>19.2</td>
<td>-8.42</td>
<td>8.1</td>
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References


