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A charge-metering method for voltage-mode neural stimulation

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HIGHLIGHTS

- A fully integrated charge-metering system was proposed to facilitate voltage-mode neural stimulation.
- Experiments are conducted with discrete model, platinum electrodes in ringer solution and extracted Xenopus sciatic nerve.
- The system operates only on 1.8 V power supply achieving a 5.2% charge delivery error when 10 nC is required to for stimulation.

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ABSTRACT

Electrical neural stimulation is the technique used to modulate neural activity by inducing an instantaneous charge imbalance. This is typically achieved by injecting a constant current and controlling the stimulation time. However, constant voltage stimulation is found to be more energy-efficient although it is challenging to control the amount of charge delivered. This paper presents a novel, fully integrated circuit for facilitating charge-metering in constant voltage stimulation. It utilises two complementary stimulation paths. Each path includes a small capacitor, a comparator and a counter. They form a mixed-signal integrator that integrates the stimulation current onto the capacitor while monitoring its voltage against a threshold using the comparator. The pulses from the comparator are used to increment the counter and reset the capacitor. Therefore, by knowing the value of the capacitor, threshold voltage and output of the counter, the quantity of charge delivered can be calculated. The system has been fabricated in 0.18 μm CMOS technology, occupying a total active area of 339 μm × 110 μm. Experimental results were taken using: (1) a resistor–capacitor EEI model and (2) platinum electrodes with ringer solution. The viability of this method in recruiting action potentials has been demonstrated using a cuff electrode with Xenopus sciatic nerve. For a 10 nC target charge delivery, the results of (2) show a charge delivery error of 3.4% and a typical residual charge of 77.19 pC without passive charge recycling. The total power consumption is 45 μW. The performance is comparable with other publications. Therefore, the proposed stimulation method can be used as a new approach for neural stimulation.

1. Introduction

Electrical neural stimulation (ENS) provides a means of effectively interfacing to sensory and cognitive pathways within the human nervous system, in particular for neuro-rehabilitation applications. This technique has already demonstrated a significant impact in neuroprosthetics by improving the quality of life in individuals with neural damage or dysfunction. To date over 219,000 people with profound hearing impairment have and are benefiting from cochlear implants (NID, 2011), and a further 80,000 with cognitive disorders (such as Parkinson's and dystonia) benefiting from deep brain stimulation therapy (de Paor and Lowery, 2009). Fundamentally, ENS is based on injecting charge extracellularly to the proximity of the target neuron to evoke action potentials (AP) as a means of modulating neural activity. The charge is delivered through electrodes positioned in close proximity to the target site (neuron somas or neural tissue) using one of three methods: current-mode stimulation (CMS) (Constandinou et al., 2008), voltage-mode stimulation (VMS) and charge-mode stimulation (ChgMS) (Ghovanloo, 2006). In CMS, the charge is delivered by a constant current source with its quantity easily controlled by the stimulation duration, but a voltage headroom must be maintained to ensure the output transistor is in saturation. Therefore it has the lowest power efficiency among the three (Simpson and Ghovanloo, 2007; Liu et al., 2012). However, work has been done to reduce this voltage headroom using a dynamic power supply. At least 53% of power can be saved (Kelly, 2011; Williams and Constandinou, 2012). In VMS, a constant voltage source is used,

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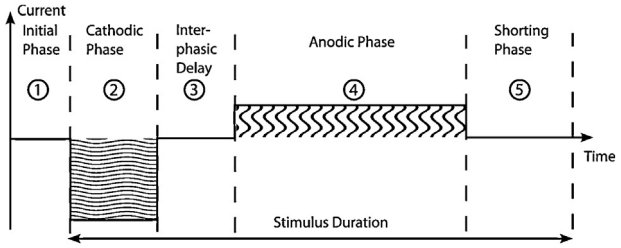

Fig. 1. Typical current mode stimulation waveform with a zero net charge, i.e. the cathodic and anodic shaded areas should be equal (and opposite).

eliminating the voltage headroom constraint. But it cannot control the amount of charge delivered. As a trade-off between the two, ChgMS uses a capacitor to set the charge quantity and does not need a voltage headroom. However, the capacitor typically required is large and has to be implemented off-chip. More comparison of the three methods can be found in the work of Simpson and Ghovanloo (2007) and Liu et al. (2012). Irrespective of which method is used, the charge delivered must be recycled (balanced) such that the residual charge is below a safety limit. Otherwise, the residual charge will form a DC potential across the electrode–electrolyte interface (EEI) that is large enough for Faradaic reactions (Weiland et al., 2003) that lead to electrode degradation and tissue damage. Typically, this is achieved by using a charge-balanced stimulation waveform, where a cathodic phase firstly delivers the stimulus while an anodic phase balances the charge. Fig. 1 shows a typical waveform in CMS (Simpson and Ghovanloo, 2007; Constandinou et al., 2008). In practice it is challenging to achieve a perfectly balanced biphasic charge profile due to circuit non-idealities such as mismatch and non-linearities. To date, most work has concentrated on achieving good charge-balancing for CMS (Sit and Sarpeshkar, 2007; Ortmanns et al., 2007) but limited progress for VMS. One approach for VMS, uses a sense resistor to monitor the stimulation current and track the charge so as to control the balance pulse (Fang et al., 2007, 2008).

This study develops a novel technique for charge-metered VMS that achieves good charge balancing using two small capacitors. This technique has been adopted from an application in nuclear science for charge monitoring (Mazza et al., 2005). It has more recently been applied in a mixed signal integrator design (Bryant et al., 2012). Following the preliminary work (Luan and Constandinou, 2012), this paper presents the manufactured fully integrated system as a proof of concept. The methodology and system architecture will be detailed in the following sections and evaluation has been performed using resistor–capacitor (RC) EEI model, buffered saline solution and *ex vivo* Xenopus sciatic nerve.

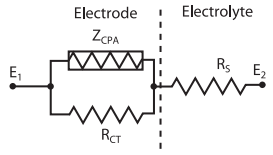

Fig. 3. Typical electrical model for the electrode–electrolyte interface used in the ENS design.

2. Materials and methods

The system architecture is shown in Fig. 2. It can be divided into two sub-systems: an analogue front-end for the charge sensing, and a digital back-end for the charge measuring and system control. R_S and C_e form a simplified electrical model of EEI and will be detailed in Section 2.1. The required charge quantity is set by the controller which sequences the switches to deliver the stimulation current via two paths formed by C_{unit1} and C_{unit2} alternatively. The two comparators and counter will track the number of times that these paths are taken, hence the total amount of charge injected/recycled. The method will be explained in detail in Sections 2.2 and 2.3. Its integrated circuit implementation and evaluation setup up are described in Sections 2.4 and 2.5, respectively.

2.1. Electrode–electrolyte interface

EEI is formed on the surface where an electrode contacts electrolyte. The electrode can be made of any electrical conductive material. Electrical properties of EEI are complex, time-variant and non-linear. A lot of studies have been done in electrochemistry aiming to understand and model (Bard and Faulkner, 2001; Cantrell et al., 2008; Franks et al., 2005; Woods et al., 2011). Typical equivalent circuit models of EEI for ENS system design include only three components as shown in Fig. 3 (Sooksood et al., 2010; Chun et al., 2010; Sit and Sarpeshkar, 2007). They represent the paths for charge transfer (Cogan, 2008). Z_{CPA} is a constant phase angle component representing capacitive charge transfer via the interface capacitance with inhomogeneous surface. R_{ct} represents the Faradaic charge transfer and R_S the electrolyte spreading resistance.

In this paper, three assumptions are made to simplify the EEI model. Firstly, the counter electrode has a large surface area comparing to the working electrode. It can be guaranteed through selection (or design) of the electrodes. Therefore, Z_{CPA} of the counter electrode can be ignored. Secondly, no Faradaic reactions happen during normal operation. This is true as Faradaic operation must be avoid for any stimulator as described in Section 1. Therefore, R_{ct} of both electrodes can be ignored. Thirdly, the surface of the interface

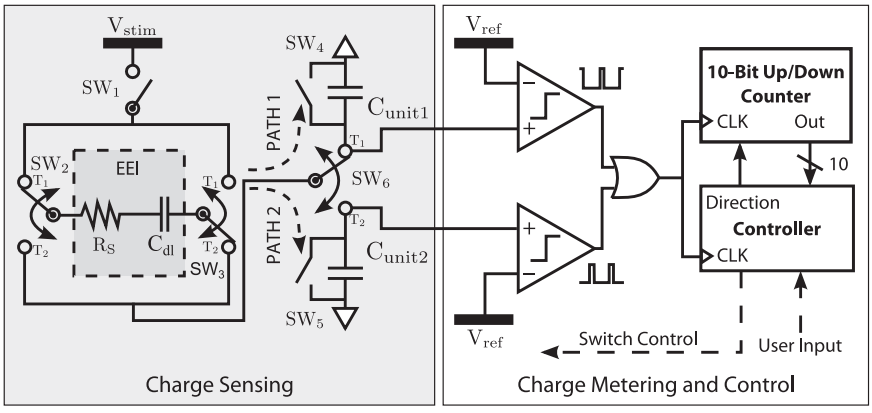

Fig. 2. System architecture of the proposed charge-metering system. (R_S represents the tissue spreading resistance and C_{dl} the electrode–electrolyte-tissue double layer capacitance. V_{ref} for the two comparators are the same.)

capacitance is homogeneous. This simplifies Z_{CPA} to a pure capacitor (C_e) (Sooksood et al., 2010; Sit and Sarpeshkar, 2007; Fang et al., 2007, 2008; Ghovanloo, 2006). The final model is shown in Fig. 2.

2.2. Method of charge-metering

The essence of charge-metering is integration of the current over the stimulation/recycling period. One straight forward method would be using a capacitor. To measure 10 nC charge is the same as measuring 10 V across the two plates of a 1 nC capacitor. However, integrating 1 nF on-chip is generally unfeasible due to area requirements. Therefore, a small value capacitor must be used. A simple analogy is measuring a large quantity of water using only a small measuring cup. The method presented here measures a small quantity of charge each time with a small measuring capacitor and using a digital counter to record the number of the total measurements made. A similar architecture is used to measure the current in the frequency domain (Ahmadi and Jullien, 2009). The circuit operates as follows. In *Path 1* (Fig. 2), C_{unit1} is charged until the comparator tells the controller to start discharging it. The maximum amount of charge can be stored before discharging is $C_{unit1} \times V_{ref}$. This amount will hereon be referred to as the *unit charge*. This charge and discharge sequence is repeated continuously under the control of the controller. It should be noted that *Path 1* will be broken during the discharge of C_{unit1} to prevent the stimulation current bypassing C_{unit1}. However, the break is undesirable as its physiological effect is unknown. Therefore, the circuit is replicated such that a second current path (*Path 2*) operates in a complementary fashion such as to maintain a continuous current flow.

If V_{ref} = 1 V, the *unit charge* quantitatively equals to the value of C_{unit1} and C_{unit2}. From hereon, these two capacitors will be referred as the *unit capacitors* (C_{unit}). Each *unit charge* delivered to the electrode is counted and thus the total charge (Q_{total}) delivered can be determined by:

$$Q_{total} = \sum_{1}^{N} C_{unit} \times V_{ref} \quad (1)$$

where N is the output of the counter.

The system comprises of 6 switches: SW_1 enables both paths; SW_2 and SW_3 determine the polarity of the stimulus and are used to short the electrodes; SW_4 and SW_5 are used to discharge the *unit capacitors*; SW_6 steers the stimulation current between *Path 1* and *Path 2*.

2.3. Stimulus generation

The system generates a biphasic stimulus (e.g. as Fig. 1) using five phases as described below. The detailed current path and switch positions are shown in Fig. 4.

Phase 1 – Initial/shorting phase. The system is reset and the C_{unit} are discharged. The stimulation path is broken and the electrodes are shorted. SW_6 can be at either T_1 or T_2. This phase can also used for shorting after a stimulation cycle to further reduce the residual charge.

Phase 2 – Cathodic phase. The stimulation path is established and current is integrated on C_{unit}. The charge is delivered by continuously alternating between *Path 1* and *Path 2* as described in Section 2.2. During this phase, the counter counts upwards till the target value is reached.

Phase 3 – Inter-phasic delay. A short delay is introduced between the cathodic and the anodic phases to avoid blocking the propagation of the induced AP (Constandinou et al., 2008). The stimulation path is broken and the switches are set as for the anodic phase.

Phase 4 – Anodic phase. The charge delivered previously is recycled in this phase. The operation is similar to that of cathodic phase, with SW_2, SW_3 and SW_6 inverted and the counter down counting until reaching zero. Note that the position of T_1 and T_2 determines polarity of the stimulation.

At the end of the anodic phase, the system will cycle back to the initial/shorting phase to further reduce the residual charge and wait for the new stimulation cycle to start.

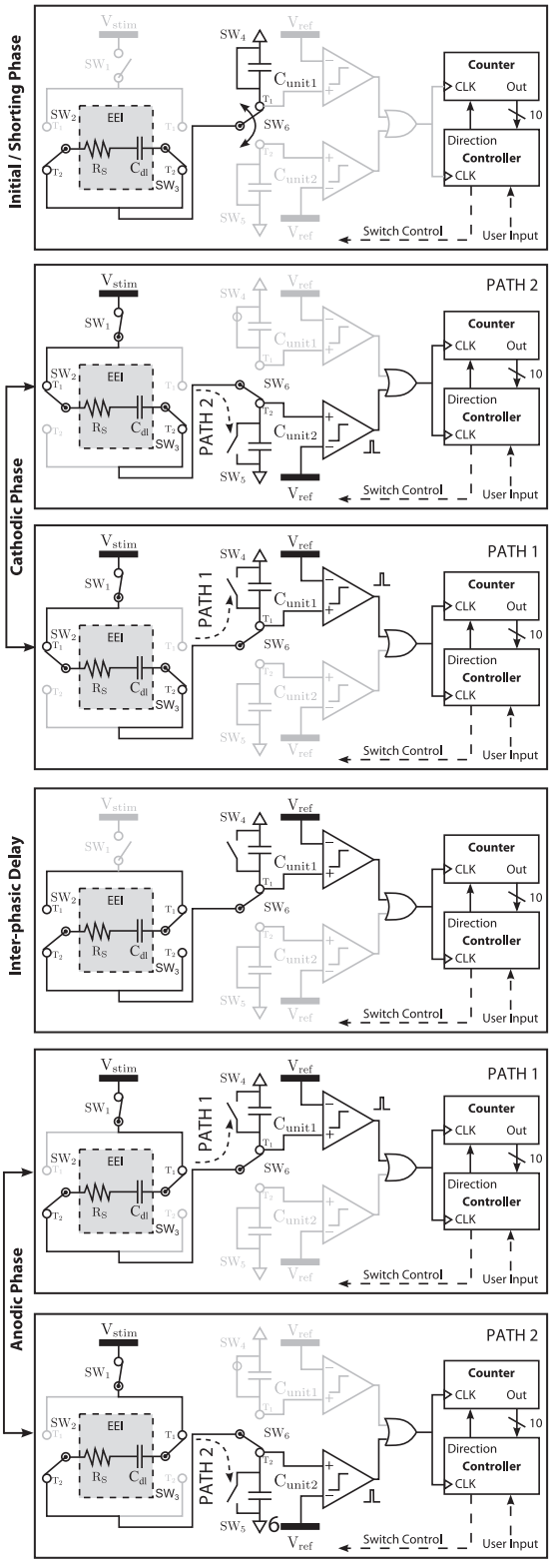

Fig. 4. Positions of the 6 switches during different phases of stimulus generation.

The stimulus parameters can be programmed as follows: the quantity of charge needs to be delivered is set by the controller; the stimulation duration is coarsely tuned by V_{stim}; the inter-phasic delay is defined externally via a RC delay network.

2.4. Circuitry

The circuit has been implemented in *Austriamicrosystems* 0.18 μm 1P4M CMOS technology. This section details specific design aspects of the circuit implementation.

2.4.1. Switch design

All the switches are implemented using transmission gates with equal device sizes (W/L = 10 μm/0.18 μm) for both NMOS and PMOS. The width are designed same so as to mitigate the charge injection effect during switching. The calculated turn-on resistance is between 80 Ω and 330 Ω with associated gate capacitance of 28 fF. Parametric simulation confirm that the drop-out voltage on the switch does not change significantly by further increasing their width for the required stimulation current. Each single pole, double throw (SPDT) switch ($SW_{2,3,6}$) is implemented using two transmission gates. Switch charge injection is not expected as a challenge because: (1) transmission gates significantly reduce any switch-related charge injection; (2) the symmetry between switches in *Path 1* and *Path 2* ensures any injected charge is recycled.

2.4.2. Unit capacitor selection and comparison threshold (V_{ref})

The value of C_{unit} and V_{ref} are crucial design parameters. They not only define the measurement resolution ($V_{ref} \times C_{unit}$) but also set the scale and power requirements of the system.

For a fixed V_{ref}, a smaller C_{unit} is preferable for a finer resolution and reduced area. However, this is at the expense of an extended counter range (for a fixed target charge quantity). In addition, this requires the counter to operate at a higher frequency as C_{unit} is charged and discharged faster. Moreover, the smaller the capacitor is the greater the mismatch effect. Therefore, there is a power/area/resolution/mismatch trade-off. To allow multiple stimulation channels on a single chip, both the power consumption and silicon area should me minimised. Initially, C_{unit} = 1 pF has been tested as this has two desirable effects, increasing the stimulation resolution and also reducing the silicon area. However, this also increases the operating frequency (Eq. (2)) to 100 MHz, which is comparable to the delay of the continuous time comparator designed (Section 2.4.3). Therefore, a C_{unit} = 10 pF has been selected (using 10× 1 pF capacitors) to relax timing constrains and provide a charge resolution of 10 pC. With a 10-bit counter, a maximum charge of 10.24 nC can be delivered, meeting the requirement for intra-cortical stimulation for human vision prosthetics (Cogan, 2008) and intraspinal microstimulation (Zimmermann et al., 2011). For other applications, for example, retinal stimulation using an IrOx electrode requiring a stimulus of 800 nC (800–200 μA within 1–4 ms) (Kelly, 2011), the counter needs to extend its range. The time constant for charging C_{unit} is:

$$\tau \approx R_s \times (C_{dl}^{-1} + C_{unit}^{-1})^{-1} \quad (2)$$

where C_{dl} is in the order of 10–100 nF and R_s the order of 10 s of kΩ. Therefore the overall capacitance is determined by C_{unit}. This sets the time constant τ to be approximately 100 ns and the operating frequency of the digital controller to be approximately 10 MHz.

On the other hand, V_{ref} also affects the resolution. It, however, also sets the common mode of the comparator and it is preferable to set this to around half the supply voltage (0.9 V). To simplify the design, V_{ref} is set to 1 V so that the stimulation resolution is numerically equal to C_{unit}. However, because of the control loop delay, V_{ref} is actually smaller than 1 V (see Section 3.1.1) and is determined via simulation so that the C_{unit} will be discharged when its voltage reaches 1 V.

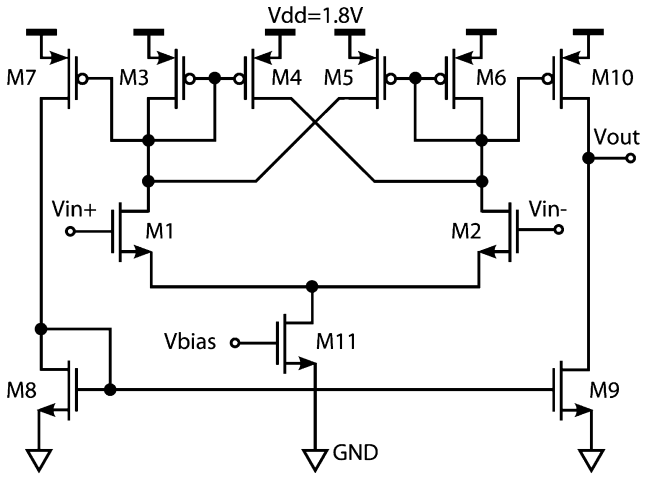

Fig. 5. Schematic of the comparator using a regenerative load.

2.4.3. Comparator

A continuous time comparator is designed (Fig. 5). A regenerative load is used to increase the gain. The strength of positive feedback formed by M5 and M6 is given by $\alpha = (W/L)_5/(W/L)_6 = 1$. This means the comparator works as a latch. Since the load of the comparator is an OR gate whose input capacitance is ≈2 fF, the delay is limited mainly by the parasitic capacitance observed at the drains of M1 and M2. In order to minimise this parasitic capacitance and thus reduce power consumption, $(W/L)_{1-6}$=1 μm/1 μm, $(W/L)_{7,10}$ = 0.4 μm/1 μm. This is at the cost of introducing larger input offset voltage. However, this offset voltage can be compensated by tuning the threshold voltage V_{ref}. The bias current is set to 6 μA (determined through simulation) such that the delay is around 10 ns. This delay cannot be improved much further without significantly increasing the power consumption. Although the output swing of the comparator is limited by the headroom of the output transistors, a full swing can be achieved at the output of the OR gate following.

2.4.4. Controller and counter

The controller is implemented using a Finite State Machine (FSM) coded in Verilog Hardware Description Language to achieve the operating sequence described in Section 2.3. A 10-bit up/down binary counter is used to record the charge delivered. The circuit comprises of 10 flip-flops with supporting combinational logic. Fig. 6 shows the least significant 3-bits. The counter operates synchronously and counts upwards when *Direction* is HIGH and downwards when LOW. Calculated from the specifications of the

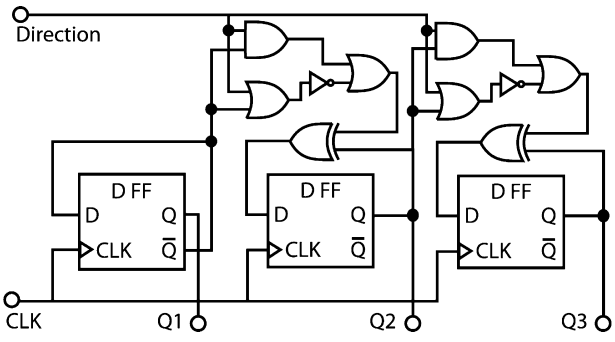

Fig. 6. Schematic of the bi-directional counter (3-bits shown).

Table 1
Evaluation matrix for each type of test.

Test name	Simulation	RC model	Saline tank	*Ex vivo* [a]
Charge metering	√	√	√	
Charge balancing	√	√	√	
Process variation and mismatch	√	√	√	
Nerve stimulation		√		√

[a] Only one chip is tested.

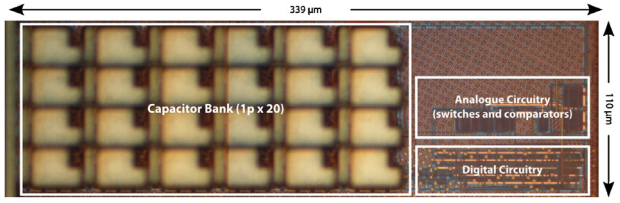

Fig. 7. Chip microphotograph showing the core circuit fabricated in *Austriamicrosystems* 0.18 µm 1P4M CMOS technology.

standard cells provided by the foundry, the counter consumes between 360 nW and 840 nW (varies with load and input transition time) at 10 MHz with a stimulation period of 1 ms and an duty cycle of 20 %. This is negligible compared to that of the comparator.

2.5. Evaluation methods

The system has been tested using 4 different methods to evaluate its performance on charge-metering, charge-balancing, process variation and mismatch, and its physiological effect. The evaluation matrix is shown in Table 1.

The circuit is simulated using Cadence IC 5.1.41ISR2 with foundry-supplied PSP (Penn State-Philips) models. C_{dl} and R_s of the EEI model are set to 100 nF and 10 kΩ, respectively, based on values modelled for a platinum electrode with a diameter of 430 µm (Chun et al., 2010).

The fabricated circuit (core) is shown in Fig. 7. C_{unit} are implemented using 10× 1 pF Metal-Insulator-Metal Capacitors (CMIM), each with a dimension of 22.2 µm × 22.2 µm. The capacitor arrays are interleaved. One important point to note is that in the fabricated design, the target charge is hard-wired to 10 nC with the inter-phasic delay and stimulation voltage controlled externally.

Test configuration with RC EEI model is shown in Fig. 8.(a). The measurements were taken from 7 randomly selected chips (within the same wafer/batch). V_{ref} is 920 mV, which is the same as in the simulations. To calculate how much charge is delivered, a 8.2 Ω resistor (R_0) is connected in series between V_{stim} and the chip. A differential probe (Lecroy AP034) is used so as to minimise the offset between the two channels of the oscilloscope (LeCroy WaveSurfer 434). This configuration is aiming to minimise the parasitic capacitance on the EEI model. Additional parasitic capacitance of PCB tracks has been removed by soldering the EEI model directly onto the pins of the chip. Therefore, the charge can be obtained by integrating the voltage across R_0 over time and divided by 8.2. To monitor the stimulation current more clearly, the probes are placed across the resistor (10 kΩ) in the EEI model as shown in Fig. 8(b) providing an increased signal-to-noise ratio. However, this introduces the capacitance of the probes to the stimulation path. Therefore, this configuration is not used to measure the charge. The current waveform is then verified using NEURON® with Hodgkin-Huxley model. The response is compared with a normal charge-balanced current stimulus.

In saline tank tests, two end exposed platinum wire electrodes are used. The working electrode has a diameter of 200 µm while the counter electrode has a diameter of 1 mm. This forms a bipolar configuration which is different from usual settings where a common

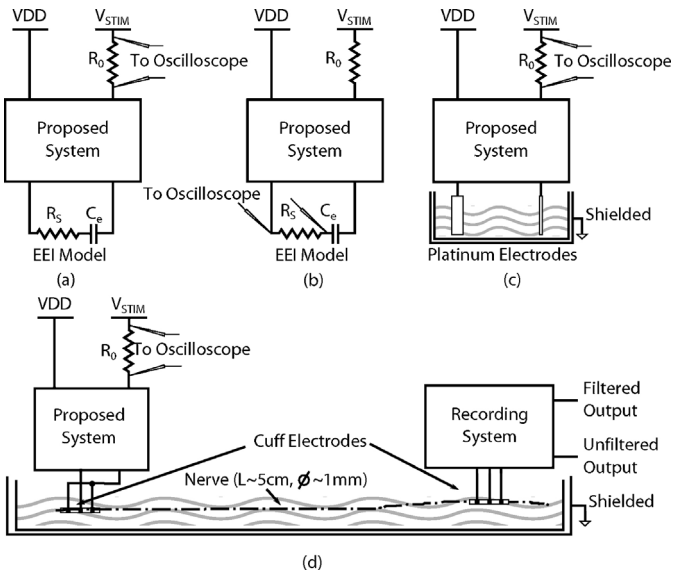

Fig. 8. (a) Test setup for charge-metering with lumped elements; (b) test setup for measure stimulation current with lumped elements; (c) saline tank test setup; and (d) *in vitro* setup with extracted Xenopus sciatic nerve.

return path is used. Fig. 8 (c) shows the configuration for saline tank test. The tank is shielded from interferences. Other setups are the same as the measurement using lumped elements except V_{stim} is 1 V as the impedance of the electrodes is lower than the RC model.

The *ex vivo* experiment was conducted using Xenopus sciatic nerve within 6 h of its extraction. The setup is shown in Fig. 8 (d). The stimulation and recording electrodes are both cuff electrode (1 mm diameter) provided by IMTEK, University of Freiburg. The effective cathode area is 0.01 cm^2. The extracted nerve was bathed in normal ringer solution within a tank which is enclosed by a Faraday cage which is connected to the ground. The recording amplifier has been realised using off-the-shelf components and configured to have a total gain of 2000 with output bandwidth from 500 to 2000 Hz. It also provides an unfiltered output to confirm the genuine nerve response. As a reference point, a standard current stimulator with an amplitude of 500 µA is used.

2.6. Effects of interference, noise and drift

Other factors such as interference/drift/noise will also affect the charge measurement. The interference may cause a sudden voltage change on the electrode which provides an extra path for the charge. Depending on whether the magnitude of the voltage interference is higher or lower than the solution voltage, the comparator will either flip more frequently or less frequently. This means the charge is not accurately measured. Therefore, in the tests presented in Section 2.5, the tank has been shielded.

Unlike in neural recording, noise is not a concern for ENS. But this will affect the resolution of charge measurement because the input of the comparator is connected to the electrode. According to Liu et al. (2008), the noise power spectra density at 10 kHz is ~15nV for a platinum wire with exposed area of $\pi \times 38^2$ μm^2. This can be used as an worst case estimation for the noise floor of the current system because the cathode area of the cuff electrode used is 10,000 μm^2 which means a lower noise floor (Lempka et al., 2011). Thus, the worst case noise for an operational bandwidth from 0 to 10 MHz is about 47 µV_RMS corresponding to 0.47 fC RMS error with each 10 pC charge packet delivered which is negligible.

The drift of the electrode with respect to ground of the circuit can cause similar problem as the sudden interference. However, drift occurs at a larger time scale (seconds) than each stimulation

Table 2
Simulated delivered and residual charges for different target charge stimulus. V_{ref} = 920 mV.

Target charge (nC)	10	9	8	7	6	5	4	3	2	1	0.01
Delivered charge (nC)	10.04	9.072	8.067	7.061	6.054	5.047	4.039	3.031	2.021	1.011	0.0104
Residual charge (pC)	−70.33	−56.91	−45.32	−34.25	−25.05	−17.25	−10.887	−5.94	−2.4	−0.3057	0.3011
Delivery difference (nC)	0.04	0.072	0.067	0.061	0.054	0.047	0.039	0.031	0.021	0.11	0.0004
Delivery error (%)	0.40	0.80	0.84	0.87	0.90	0.94	0.97	1.03	1.05	1.10	4

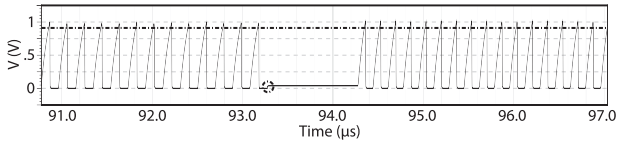

Fig. 9. Simulation results shows the overshoot of the voltage on the measuring capacitor due to control loop delay and offset of the comparator. The dashed line is V_{ref} while the circle part shows extra charge injected at the end of the stimulation phase.

(milliseconds), and therefore the electrode potentials are reset to the circuit ground during each shorting phase.

3. Results and discussion

3.1. Charge metering and balancing

3.1.1. Simulation

Simulation results are shown in Table 2. The delivered and residual charges are calculated by integrating the stimulation current. For 10 nC target charge, which is the hard-wired setting for the fabricated chip, the delivered and residual charge is calculated to be 10.04 nC and −70.33 pC, respectively. Note the differences in charge delivery increase with the target charge quantities but reduce for the 10 nC run. This is caused by both the control loop delay and the charge accumulated on C_{dl} in the EEI model as explained below.

Because the digital circuits are clocked by the comparator output (comparison of the $V_{C_{unit}}$ and V_{ref}), it is essentially an asynchronous circuit and is therefore sensitive to timing. During the time from $V_{C_{unit}} = V_{ref}$ to the time the current path is steered away, extra charge is injected, as shown in Fig. 9. This also happens at the end of each phase (the circled portion in Fig. 9). This delay is caused by the offset of the comparator and the inherent delay in the system and introduces two errors.

The first is the difference between the target and the actual quantities of charge delivered. In detail, *unit charge* comprises of a fixed part set by V_{ref} and a variable part set by the control loop delay (Δt) and stimulation current (I_{stim}) as well as the system offset (Fig. 10). The fixed part is given by

$$Q_{\text{Unit Charge fixed}} = V_{ref} \times C_{unit} \tag{3}$$

While the variable part is given by

$$Q_{\text{Unit Charge variable}} = (I_{stim} \times \Delta t) + (V_{offset} \times C_{unit}) \tag{4}$$

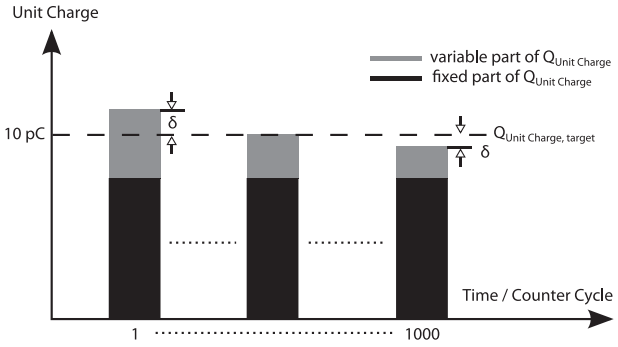

Fig. 10. Charging error showing the unit charge is comprised of two components. The variable portion is decreasing due to the reason stated in Section 3.1.1.

Here Δt and V_{offset} are fixed as they depend on the circuit design. However,

$$I_{stim} = \frac{(V_{stim} - V_{C_e})}{R_S} \tag{5}$$

where V_{C_e} is the voltage on C_{dl}. Therefore, with V_{C_e} increases as the stimulation carries on and V_{stim} fixed, $Q_{\text{Unit Charge}}$ decreases as shown in Fig. 10. Here, an error δ is defined:

$$\delta = Q_{\text{Unit Charge}} - Q_{\text{Unit Charge target}} \tag{6}$$

Here, $Q_{\text{Unit Charge target}}$ = 10 pC as designed. The accumulation of δ introduces the charge delivery difference.

The second error is in the residual charge. This is a result of mismatch of the charge delivery difference between the stimulation and the recycling phases. As identified in the above, the charge delivery difference depends on the initial value of V_{C_e}. Since the initial values are different for the stimulation and recycle phases, the charge is not perfectly recycled.

For a positive δ at the beginning of the stimulation and a negative δ at the end, the charge delivery difference will first increase and then decrease as observed in the simulation (delivery difference in Table 2). To reduce the errors, the ideal solution is to design an adaptive system that can compensate any control loop delay rising from either tissue impedance changes or V_{C_e} changes. Such a system would give a δ close to (but not equal to) zero. The predictive comparator (MeVay and Sarpeshkar, 2003) may be used for such a task. A simpler solution is to calibrate V_{ref} before stimulation.

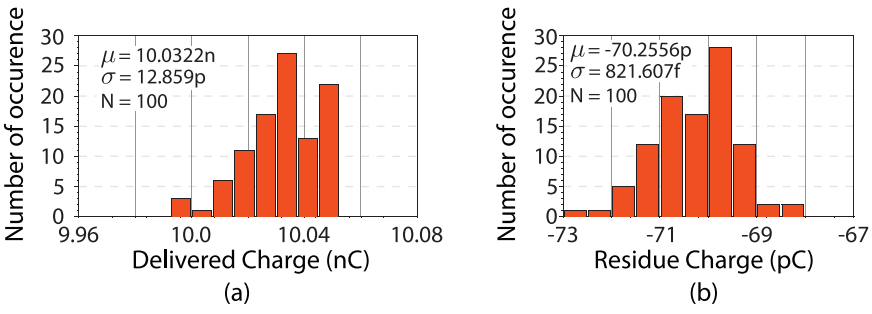

Fig. 11. Monte-Carlo analysis for: (a) charge delivered and (b) residual charge.

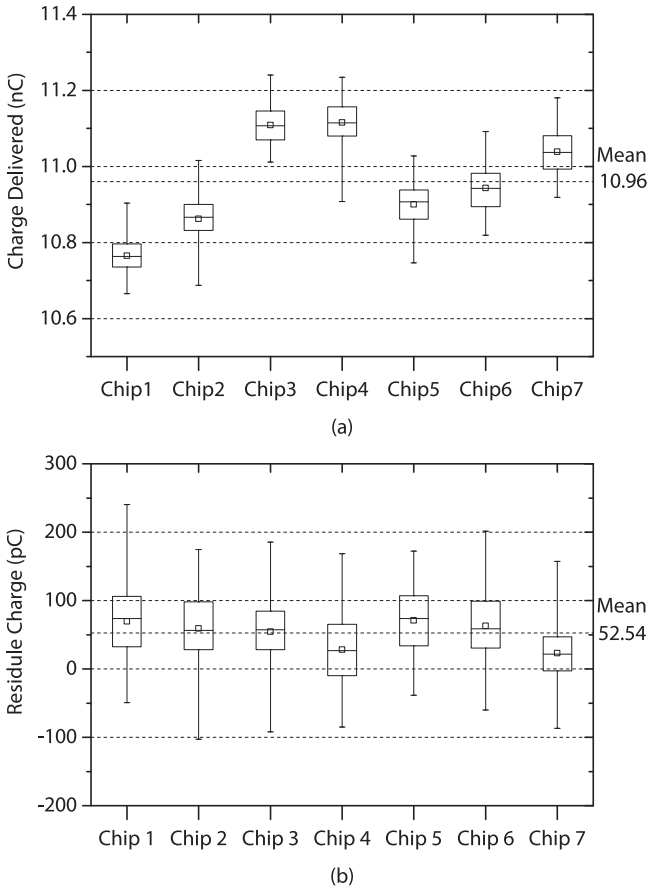

Fig. 12. Measured results of 7 chips with RC EEI model and V_{ref} = 920 mV, $V_{Stimulation}$ = 1.8 V for (a) the charge delivered; (b) the residue charge after active charge recycle. 100 measurements have been taken for each chip. The target charge is 10 nC. The box shows the interquartile range; with whiskers showing the minimum and maximum; and centre line showing the medium and centre square is the average.

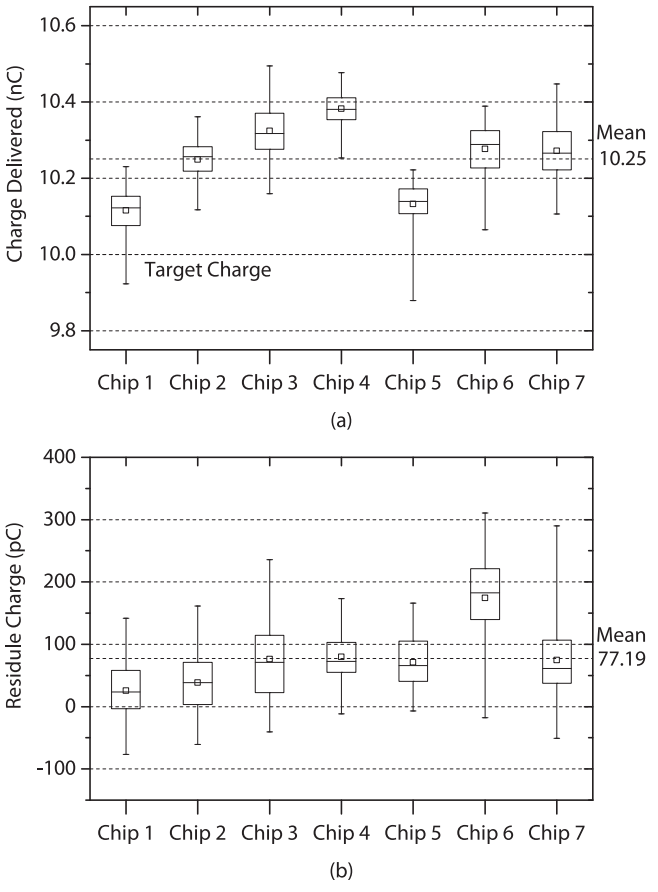

Fig. 13. Measured results of 7 chips in the saline tank with platinum electrodes with V_{ref} = 920 mV, $V_{Stimulation}$ = 1 V for (a) the charge delivered; (b) the residue charge after active recycle. 100 measurements have been taken for each chip. The target charge is 10 nC. The box shows the interquartile range; with whiskers shows the minimum and maximum; and centre line showing the median and centre square is the average.

Monte-Carlo simulation was done for 10 nC target charge. The results for delivered and residual charge are shown Fig. 11. Although this shows small variation, in practice, it is not the case as will be shown.

3.1.2. Lumped element RC model test

The results are post processed to removed the DC offset from the probe and shown in Fig. 12. The average charge delivered for the whole test is 10.96 nC which is higher than the simulation, which can be explained from three aspects.

Firstly, the absolute value of C_{unit} has a 10% error. Secondly, parasitic capacitance is added by the ESD protection and chip package. Thirdly, the overshoot error δ is different from the simulation. The first two factors are process limited while the third one can be tuned as the value of the RC EEI model are externally controlled. Considering only these two factors, the actual C_{unit} is between 10.06 pF and 12.45 pF with a typical value of 11.3 pF. This means an error of ±10%. Therefore, any result between 10.06 pF and 12.45 pF are valid. Since this error is process limited, it cannot be improved unless the capacitor can be build more accurately on chip or δ is tuned to compensate after fabrication. The latter one can be done by changing V_{ref} or V_{stim}. In case the mean charge delivered is tuned to 10 nC, the maximum spreading of the charge delivered is 328.6 pC, corresponding to an delivery error of 3 % which cannot be further reduced after fabrication.

The measured residue charge shows a mean value below 100 pC but a larger spreading than the simulation. For 1 ms stimulation period, this translate to a mean DC error of 52.54 nA and maximum 290 nA using only active charge recycling. This is not safe for neural stimulation without further passive shorting phase. For example, the safety limit for a commercial cochlear implant is 25 nA (Sit and Sarpeshkar, 2007). However, the result is comparable to the published active recycling systems without including their passive shorting phase as shown in Table 3. To reduce the DC error, the electrodes need to be shorted. The required shorting time depends on the impedance of the EEI. In this test, the time constant is τ_{short} = 10 kΩ × 100 nF = 1 ms. The shorting time required in this test for reaching a DC error is 25 nA is 0.77 τ_{short} (maximum 4.27 τ_{short}). Another method to reduce the DC error in chronic application is to apply background calibration so that the residue charge has a zero mean value and remains within a safe range during stimulation (Sooksood et al., 2010).

3.1.3. Saline tank test

The results for the saline tank test is shown in Fig. 13. For charge delivery, the mean value is lower than the results using RC EEI model because V_{stim} is 1 V instead of 1.8 V. But, it presents the similar charge delivery error of 3.4% to that of using RC EEI model. The residue charge also gives similar results which has an mean DC current error of 77.19 nA and maximum 311 nA. This corresponds to a shorting phase of 1.14 τ_{short} (maximum 4.58 τ_{short}).

With configuration in Fig. 8(b), the stimulation current is measured as shown in Fig. 14(d). Note that the envelop of the current seems to be constant. However, this "constant" envelope is made of very small ripples (Fig. 14(e)) that follows the profile of constant

Table 3
Performance comparison with existing work assuming 1 ms stimulation period.

	This work[a]	Sit and Sarpeshkar (2007)	Ortmanns et al. (2007)	Fang et al. (2008)[b]
DC current error (nA)	77.19 (Max 311)	120	Not state, $\propto C_{dl}$	160
Stimulation mode	Voltage	Current	Current	Voltage
Full-scale stimulus	–	10 mA	1 mA	–
Charge delivery error	5.2%	–	–	0.5%
Voltage rails (V)	1.8	+6, −9	3.3, 22.5	1.8/3.3
Power	45 μW	47 μW	198 μW	50 μW
Technology	0.18 μm	0.7 μmHV	0.35 μmHV	0.18 μm
Area[c]	0.037 mm^2	1.44 mm^2	0.15 mm^2	–

[a] Saline tank test..
[b] Simulated value..
[c] Core area of single channel only..

voltage stimulation. The ripples are caused by switching between the two stimulation paths. A similar current profile can be found in Kelly (2011). Nevertheless, the neuron can still be stimulated as confirmed by both NEURON® and *ex vivo* setup. The reason is that the ripple has a much more smaller time constant (90 ns) than that required for sodium channel activation (100-200 μs) Koch (2004).

3.2. Ex vivo test

The aim of the *ex vivo* test is to demonstrate that the nerve can be successfully stimulated as predicted. A comparison between this work and a direct current stimulator with 500 μA amplitude, 500 μs pulse width and zero inter-phasic delay is shown in Fig. 15. The charge injected by the current stimulation is 250 nC giving a charge density of 9.88 μC/cm^2. The proposed system delivered 10 nC charge resulting a charge density of 0.4 μC. Although the two stimulation differs by 25 times, their charge density are in the range

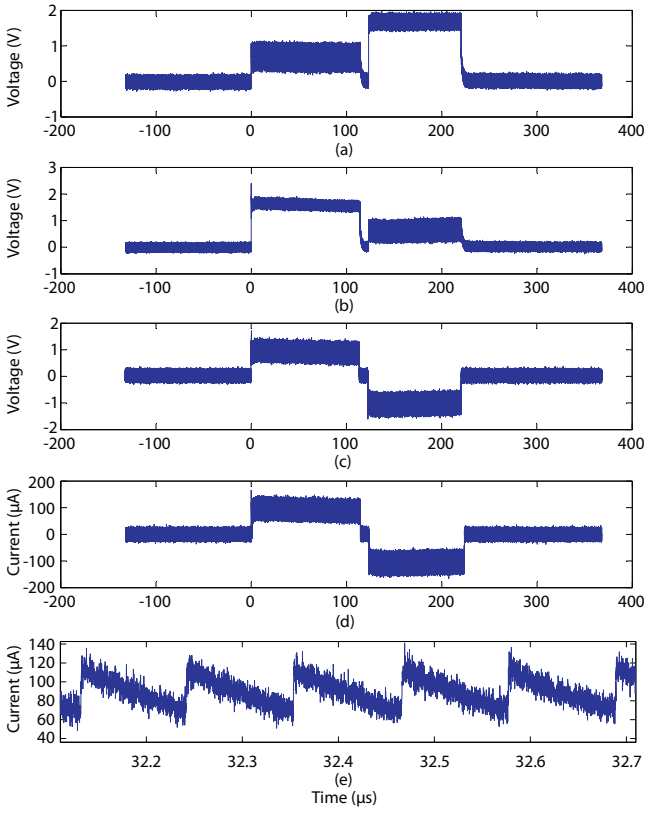

Fig. 14. (a and b) Single ended voltage on the two terminals of EEI model (c) differential voltage across the EEI model (derived from (a) and (b)); (d) stimulation current derived from the differential voltage across the resistor in the EEI model; (e) detail of (d).

for recruiting mainly the fast nerve fibres, Aα and Aβ according to the experiments by Woods (2011). The conduction velocity of Aα and Aβ is between 14 and 38 m/s (Khayutin et al., 1991). Therefore, for 5 cm distance, the compound action potential composed of potentials from Aα and Aβ should be observed within 1.32∼3.57 ms after stimulation. This is illustrated in Fig. 15. The large stimulation artefact here is a result of direct voltage stimulation. Therefore, the system is able to induce action potentials as predicted by the NEURON® package.

3.3. Temporal control

Temporal control of the stimulus is an important aspect of ENS as it affects the neural stimulation efficacy (Macherey et al., 2006; Cogan et al., 2006). In the presented system, the ability of temporal control is limited and empirical as the user has to change the stimulation voltage and check if the stimulation time meets the requirement. For example, in the saline tank test (Section 3.1.3), V_{stim} = 1 V is used to prolong the stimulation time.

The temporal resolution can be described as

$$\text{Temporal resolution} = \frac{V_{ref} \times C_{unit} \times Z(t)}{V_{stim}} \quad (7)$$

where $Z(t)$ is the time-varying impedance of the EEI interface. As a result, the temporal resolution improves with smaller V_{ref}, C_{unit} and $Z(t)$. However, V_{ref} and C_{unit} are limited by the common mode voltage of the comparator and process variation, respectively (Section 2.4.2). $Z(t)$ complexes equation by making it time dependant. More accurate temporal control would be possible if charge were delivered discretely within a predefined period larger than $V_{stim}/Z(t)$ so that it becomes time-independent. Nevertheless, the present system can deliver asymmetric waveform by setting different stimulation voltage for charge/discharge phase.

3.4. Power efficiency

The power consumption of a stimulator can be split into three portions. The first is the power consumed by the circuitry delivering the charge and controling the system, P_{sys}. The second is the power

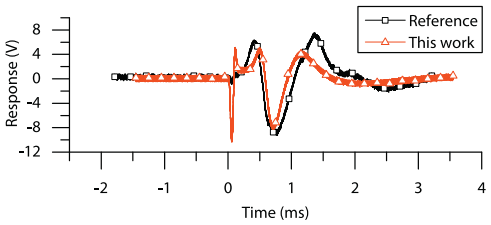

Fig. 15. Comparison of response between this work with V_{stim} = 1.8 V and an conventional direct current stimulator using 500 μA with 500 μs pulse-width and zero inter-phasic delay.

consumed on the driver path (i.e. switches), P_{driver}. The third part is the power consumed at the electrode, $P_{electrode}$, i.e. the stimulus. Therefore, the efficiency is defined as

$$\eta = \frac{P_{electrode}}{(P_{sys} + P_{driver})} \quad (8)$$

where P_{sys} is the power measured from the system power supply which was 45 μW (averaged over the stimulation cycle, 220.5 μs). P_{driver} is calculated by averaging the integrated product of the current across the EEI model and the maximum voltage level recorded at the stimulation terminal over one stimulation cycle (the voltage across the EEI and C_{unit}). The result is 177.5 μW. Similarly, $P_{electrode}$ is calculated by averaging the integrated product of the voltage and current across the EEI model over one stimulation cycle. The result is 94.23 μW. Therefore the power efficiency (η) is 42.35% when delivering a 10 nC biphasic pulse. If P_{driver} includes the power consumed on the switches in the stimulation path. The result is 36.4%. This is the result of connecting a capacitor in the stimulation path for charge-metering. Although the efficiency is lower that the method proposed in Fang et al. (2007, 2008), no additional op-amp is required here for integration. Also note that the efficiency here is calculated based on the power consumption of the whole system while Fang et al. (2007, 2008) and Simpson and Ghovanloo (2007) only consider the efficiency on the electrode which is the ratio of the voltage across the electrode to the stimulation voltage.

4. Conclusions

This paper has presented a novel method for charge-balanced VMS using charge-metering with the first reported experimental results. The system architecture and circuit implementation have been presented with the key design considerations. The concept and system viability has been demonstrated through measured experimental results using the discrete RC EEI model, and platinum electrodes within ringer solution as well as *ex vivo*. The results show a charge delivery error of 3.4% with a typical DC current error of 77.19 nA for 1 ms stimulation period. The total power consumption is 45 μW. The core area is 110 μm × 339 μm in a 0.18 μm CMOS technology. The circuit performance is compared to the state-of-the-art charge balancing and charge metering systems in Table 3.

Future work will be concentrated on reducing the process limited error by introducing on-chip calibration. Another area for improvement is to reduce the static power consumption (currently is about 60% of the total power consumption). In addition, it is also useful to extend the common mode input range of the comparator so as to extend the tuning range of V_{ref}.

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