Effect of different low temperatures on current transport mechanisms and frequency effect on capacitance-voltage curves for MOS-diodes

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Abstract

Thin SiO\textsubscript{2} films with thickness 5-10 nm were grown at 700 °C in dry ambient. The devices with oxide 5 nm approach ideality case at room temperature, in this case thermoionic emission over the barrier is dominate mechanism with traps was dominate. Capacitance-voltagedata in the form of 1/C\textsuperscript{2} verse voltage plot has been used to extract doping on the space charge region. The barrier height from I-V calculated 0.65, 0.64 V for devices with oxide 5, 10 nm respectively, this value difference from values extract from C-V plot which found 0.57, 0.64 V.

Keyword:SiO\textsubscript{2}, electrical properties, MOS-diodes,thin film;

1. Introduction

Insulating films play an important role in semiconductor devices operation \cite{1} and solar cells. Metal-thin-film insulator structure is currently receiving much attention in solar cells, this structure overcoming low open-circuit photovoltage of schottky barrier solar cells \cite{2}. Insulators films may serve to isolate one part of circuit from another or, as in the case of field effect transistor, prevent direct current flow into gate while allowing control over the current between source and drain \cite{3, 4}. Silicon dioxide films most common and has much attention due to easy grown on silicon wafers, the superior insulating quality of this film, a stable SiO\textsubscript{2}/Si interface and simply processing requirements \cite{5}. The purpose of our study is to investigate effect thin oxide layer on MOS capacitor characteristic, effect different low temperatures on current transport through devices and studding capacitance-voltage curves at different frequencies.

1. Experimental procedure

P-type wafers boron-doped were cleaned in both organic and inorganic solvents and chemically polished in 10:1 H\textsubscript{2}O: HF to 30 second, rinsed in de-ionized water, and immediately oxidized in dry oxygen at 700 °C for time 10, 30 min. to grown oxide layer with thickness 5, 10 nm. The oxide from back wafer removed by hydrofluoric acid, 200 nm Aluminum metal evaporated to the back wafer and
Results and discussion

Figure (1) indicate forward and reverse current pass through device with 5 nm oxide layer at low different temperatures 300, 400 K. For thin insulator insert between semiconductor and metal gate Schottky theory may be applied [6]. Figure (1) show that thermoionic emission is dominate at low temperatures, by increasing forward biasing we see sharp increase of current until the current began saturated and don’t increase by same rate, this is due to effect of series resistance which indicate the mechanism transport is thermoionic emission and device approach ideality case [7]. By increase temperature ideality factor approach one unity due to many carriers have enough energy to overcome the potential barrier and this value calculated from equation (1). In reverse biasing leakage current was very little due to thin oxide layer for MOS device. Diodes of MS and MIS with thin oxide layer have rectification factor with different values depending on type contact, insulator and fabrication conditions, this device has rectification factor greater than for device with oxide layer 5 nm, this is very large if comparable with other authors [8, 9].

\[ n = \frac{e}{K_B T} \left[ \frac{\partial v}{\partial \ln I} \right] \]  

(1)


Figure (2) and (3) show current-voltage characteristics at different low temperature for devices with oxide layer 5, 10 nm respectively. These curves indicate that the current pass through devices decrease with decreasing the temperature, at very low temperature less than 200 K thermoionic emission don’t happened and other mechanism as recombination or tunneling may happen, it this case the device behavior became so far from ideality case.
Barrier height of devices calculated from I-V curves and by using equation (2), ideality factor and barrier height values shown in table (1).

\[ I_s = A A^* T^2 \exp \left( -\frac{\varphi_B}{kT} \right) \]  

(2)

\( I_s \): saturated current, \( A \): area devic, \( A^* \): Richardson constant, \( \varphi_B \): barrier height.

<table>
<thead>
<tr>
<th>Oxide thickness (nm)</th>
<th>I-V measurements at 300 K</th>
<th>C-V measurements at 300 K</th>
</tr>
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<tbody>
<tr>
<td></td>
<td>Ideality factor</td>
<td>Rectification factor</td>
</tr>
<tr>
<td>5</td>
<td>1.18</td>
<td>10⁵</td>
</tr>
<tr>
<td>10</td>
<td>2</td>
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Figure (4, 5) showed capacitance-voltage curves at different frequencies, this curves indicate three regions; for large negative voltage AL gate, majority carrier accumulated at Si-SiO₂ interface, electric field attracts holes to the surface region and the surface is made more p-type and most of the holes are very close to the surface, the capacitance saturated at maximum value and don’t increase with increasing negative voltage, at small negative voltage majority carriers repels from surface region, and capacity begin decrease, when applied positive voltage most of holes depletes from region and create depletion region, the capacity more decrease and reach minimum when depletion region reach maximum width [10, 11]. To find doping density and built in potential we plots \( 1/C^2 \) verses applied voltage in figure (6) from intercept of straight line with voltage at point \( 1/C^2 = 0 \) we determine built in potential and from slope and
by using equation (3) [12] we calculated doping density which agrees with data manufacture, these values shown in table (1).

\[
N_d = \frac{2}{eA^2\varepsilon_0\varepsilon_{ox}(dC^{-2}/dv)}
\]  

(3)

Where \(N_d\): Doping density

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Fig. (4) Capacitance-voltage characteristics measured at frequencies 4, 10, 100 for device with oxide film 5 nm.

Fig. (5) Capacitance-voltage characteristics measured at frequencies 4, 10, 100 for device with oxide film 10 nm.

Fig. (6) Reciprocal square capacitance verse applied voltage for two devices.
Conclusions

Grown a thin silicon dioxide films on silicon substrates leads to fabricate MOS diodes have rectification factor, this means the device may operate switch in electronic circuits and device approach ideality properties with ideality factor 1.18 at room temperature and approach unity at 400 K, with increasing oxide films leads to disappear rectification properties and device has ideality factor 2 at room temperature, thin oxide films enhancements C-V properties which superior properties of MS contacts, C-V data indicate that MOS capacitors may operate as avarctor.

References