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Research Article

Lithography-Free Fabrication of High Quality Substrate-Supported and Freestanding Graphene Devices

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ABSTRACT

We present a lithography-free technique for fabrication of clean, high quality graphene devices. This technique is based on evaporation through hard Si shadow masks, and eliminates contaminants introduced by lithographical processes. We demonstrate that devices fabricated by this technique have significantly higher mobility values than those obtained by standard electron beam lithography. To obtain ultra-high mobility devices, we extend this technique to fabricate suspended graphene samples with mobilities as high as 120 000 cm²/(V·s).

KEYWORDS

Suspended graphene, shadow mask, mobility, lithography-free, e-beam evaporation

Since its experimental isolation on insulating substrates in 2004, graphene has attracted tremendous attention, as its unusual electronic, thermal, and mechanical properties [1–6] promise both novel fundamental phenomena and device applications. Yet, some of the most fascinating predictions, such as Veselago lensing [7, 8], fractional quantum Hall effects [9], and ballistic transistors, are yet to be experimentally demonstrated. This is partly due to the limited mobility, which ranges from ~ 5000 to 50 000 cm²/(V·s) for substrate-supported devices, and up to 250 000 cm²/(V·s) for suspended devices [10, 11]. The exact origin(s) of the mobility bottleneck is still under debate, but lithographical processes, which have been used to fabricate almost all graphene devices to date, are known to be an important contributing factor. As graphene consists of a single atomic layer, it is particularly sensitive to surface contaminants, including resist residues left by lithographical processes, which locally modify the electrochemical potential and provide extra scattering sites. Though annealing techniques have been demonstrated to improve device mobility [12, 13], they are not well controlled and do not always produce consistent results. Lithography-free fabrication techniques have been reported [14, 15]; however, the procedures are complicated and yield devices that are restricted to simple geometries.

Here we report a lithography-free device fabrication technique for graphene devices, via metal evaporation through silicon hard masks. This technique is simple, inexpensive, and does not require any resist processing; thus, it greatly increases device throughput, produces transparent contacts between graphene and electrodes, and yields high quality graphene devices. Additionally,

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hard masks, and hence devices, with complex patterns can be readily fabricated. Using this technique, we fabricate both substrate-supported and suspended devices, whose high mobilities are characterized by electrical transport measurements.

The first and most crucial step in our fabrication procedure is the synthesis of hard silicon shadow masks, as illustrated in Fig. 1(a). Here we use 500 μm double-side-polished, {100} orientation silicon wafers that are 1 cm × 1 cm in size. Firstly, a 200-nm layer of chromium is evaporated on one side of the wafer, followed by the deposition of a thin layer of poly(methyl methacrylate) (PMMA) e-beam resist. This chromium layer will serve as an etching mask for later KOH and inductively coupled plasma (ICP) etching processes. Since controllable etching of thick (> 100 μm) Si layer is difficult, we reduce the thickness for the final pattern etching by using photolithography and KOH etching to open a large, 400-μm deep window on the back of the wafer, leaving a 100-μm thick Si layer to be etched in the final step. The shadow mask structure is then patterned on the front side using e-beam lithography. After exposing and developing the resist, we use a chromium etchant (1020AC) to remove the exposed chromium layer. Finally, the shadow mask is completed by using ICP to etch through the exposed silicon layer, creating a Si wafer with patterned openings.

Scanning electron microscope (SEM) images of two ready-to-use silicon shadow masks with different geometries are shown in Figs. 1(b) and 1(c). Features as small as 500 nm can be reliably fabricated. The masks typically also contain alignment windows that assist with precision alignment during device fabrication, as indicated by the arrows in Fig. 1(c). These shadow masks are exceedingly robust, and can be used more than 20 times. We note that traditional shadow masks, which consist of silicon nitride Si_3N_4 membranes that are partially released from Si substrates [16–19], often exhibit distorted edges [16, 18]. In contrast, our silicon shadow mask has a flat sample-contacting surface, and is sufficiently rigid for complicated structures such as Hall bar geometries.

To fabricate graphene devices, we exfoliate single layer graphene sheets on standard Si/SiO_2 wafers. With the help of alignment windows, we use micromanipulator *XYZ* translation stages to carefully

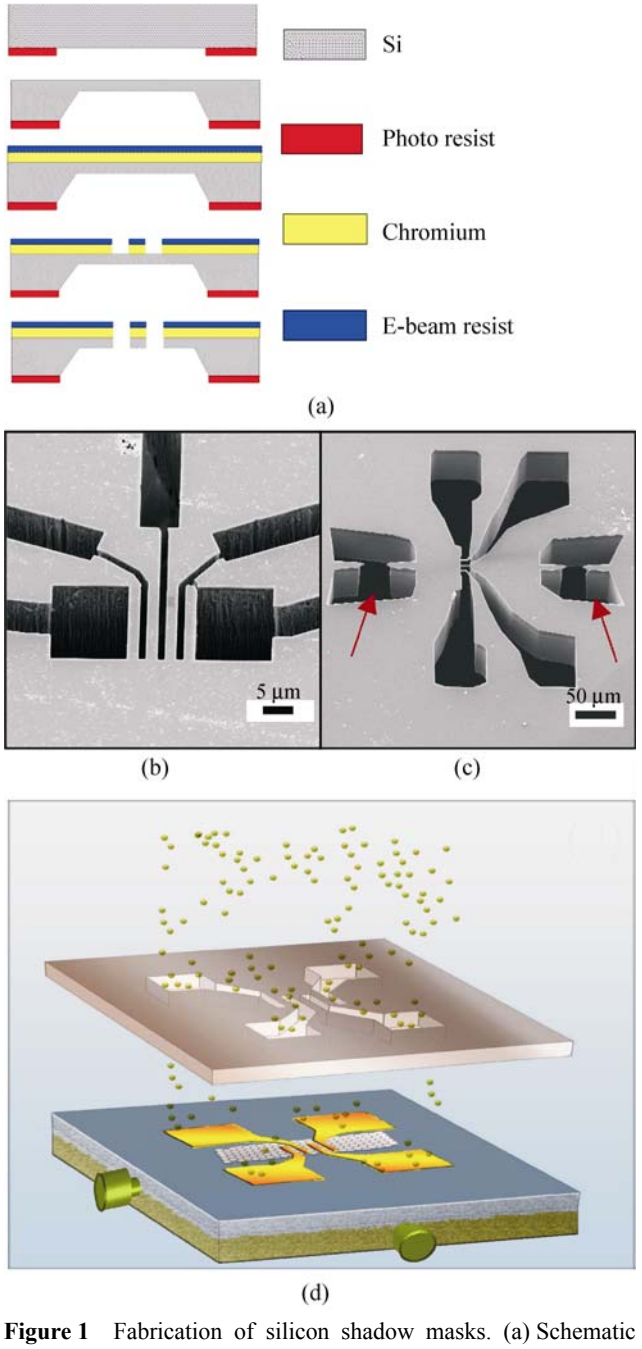

Figure 1 Fabrication of silicon shadow masks. (a) Schematic illustration of the fabrication process. (b and c) SEM images of two silicon shadow masks. The red arrows in (c) indicate the alignment windows. (d) Graphene devices can be fabricated by direct deposition of metallic electrodes through these masks

align the shadow mask to identified graphene sheets, and then place the entire assembly in a vacuum chamber (Fig. 1(d)) for metal deposition. The mask nominally rests on the substrate, though the effective mask–substrate separation—which is typically about few hundred nanometers—is determined by the

thickness of graphite residues on the substrate surface. In completed devices, we find that the metal electrodes typically extend beyond the shadow mask openings by ~ 0.3–0.5 μm, due to the extended size of the metal source and the finite mask–device separation.

To compare the qualities of graphene devices made by conventional e-beam lithography and shadow mask evaporation, we fabricate devices using both techniques on the same graphene sheet. To this end, we use a shadow mask to deposit four electrodes (labeled A, B, C, and D in Fig. 2(a)), and subsequently e-beam lithography to deposit three additional electrodes (E, F, and G in Fig. 2(a)), on a single-layer graphene sheet. The electrodes are designed to yield devices with similar aspect ratios. After each fabrication, the device was characterized by atomic force microscope (AFM) imaging and electrical measurements.

The right panel of Fig. 2(a) displays an AFM image of the graphene surface after lithography, revealing a thin layer of resist residue. The device was annealed in an H_2/Ar atmosphere at 200 °C for 45 min to remove the contaminants [12]. Using standard lock-in techniques, the two-terminal conductance, G, of the devices was measured as a function of the back gate voltage, V_g, that controls the density n and type of the charge carriers. The device mobility μ was calculated from the slope of the plots of G vs. V_g and the relation $\mu = \sigma/(ne)$, where σ is the device conductivity, and e is the electron charge. For a typical device fabricated by lithography, μ was found to be 1500 and 3000 cm²/(V·s) at room temperature and 4.2 K, respectively (Fig. 2(c)).

In contrast, for devices fabricated by shadow mask evaporation, the graphene surface remains clean after evaporation, as shown by the AFM images (left panel, Fig. 2(a)). Atomic resolution images of the honeycomb lattice over large areas can be obtained using scanning tunneling microscopy, without any annealing treatment (Fig. 2(b)). From transport measurements, the device mobility is ~ 4000 cm²/(V·s) at room temperature, and increases to ~ 7000 cm²/(V·s) at 4.2 K (Fig. 2(d)). Thus, eliminating lithography yields devices with significantly higher mobility.

This shadow mask technique can be applied to fabricate devices with a variety of geometries. As another demonstration of its power and versatility, we extend it to the fabrication of suspended devices

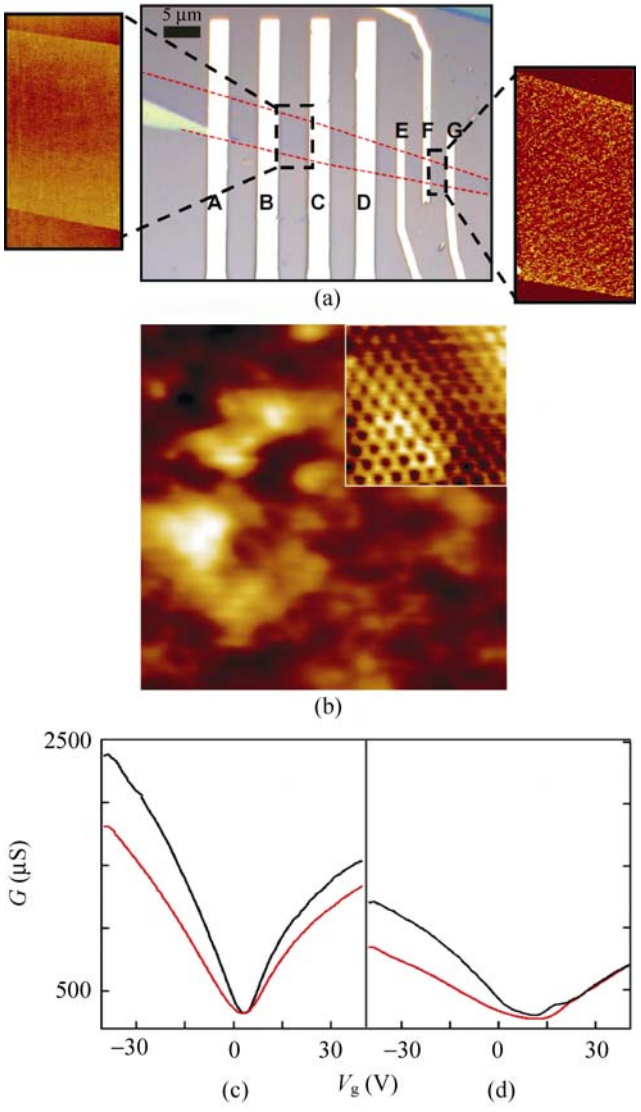

Figure 2 (a) Optical image of a single-layer graphene sheet device. The electrodes A, B, C, and D were deposited by evaporation through a shadow mask, and E, F, and G were fabricated using standard electron beam lithography. (b) STM images of an as-fabricated device using the shadow mask technique. The main panel displays an image of 85 nm × 85 nm area, and the inset shows the atomic lattice over an area of 2.5 nm × 2.5 nm. Plots of two-terminal conductance (G) vs. back gate voltage (V_g) for the electrode pairs (c) B, C and (d) F, G at room temperature (red) and 4.2 K (black)

via two complementary methods. In the first technique (Figs. 3(a)–3(c)), a completed device supported on a substrate was fabricated on the substrate, followed by hydrofluoric acid (HF) etching, which releases the graphene sheet from the SiO_2 layer, and critical point drying. Here the Cr/Au electrodes double as etch masks, and HF etches anisotropically and preferentially

along graphene [11], resulting in suspension of the entire graphene sheet. The HF-etched devices are annealed using current-induced Joule heating [13]. The mobilities were found to be 20 000 and 120 000 cm²/(V·s), respectively, at room temperature and 4.2 K. The plots of G vs. V_g display pronounced sub-linear curvature, indicating the high mobility of the material [10, 11] (Fig. 3(d)). Up to 5 V can be applied to the gate voltage; above 5 V, buckling of the partially suspended thin-film electrodes leads to device failure. Notably, the plots of G vs. V_g display non-uniform variation at temperature T: for highly doped regimes, G increases as T decreases; at the Dirac point, G decreases with decreasing temperature. Both the mobility values and the gate-dependent $G(T)$ relation are consistent with previous measurements [11], and may also be related to the formation of ripples due to graphene's negative thermal expansion coefficient [5].

Using the second technique to fabricate suspended devices, a graphene sheet is directly exfoliated across pre-defined trenches on the substrate; electrodes are deposited by evaporating through shadow masks that are carefully aligned with the trenches (Figs. 3(e)–3(g)). The inset in Fig. 3(h) shows the image of a bi-layer

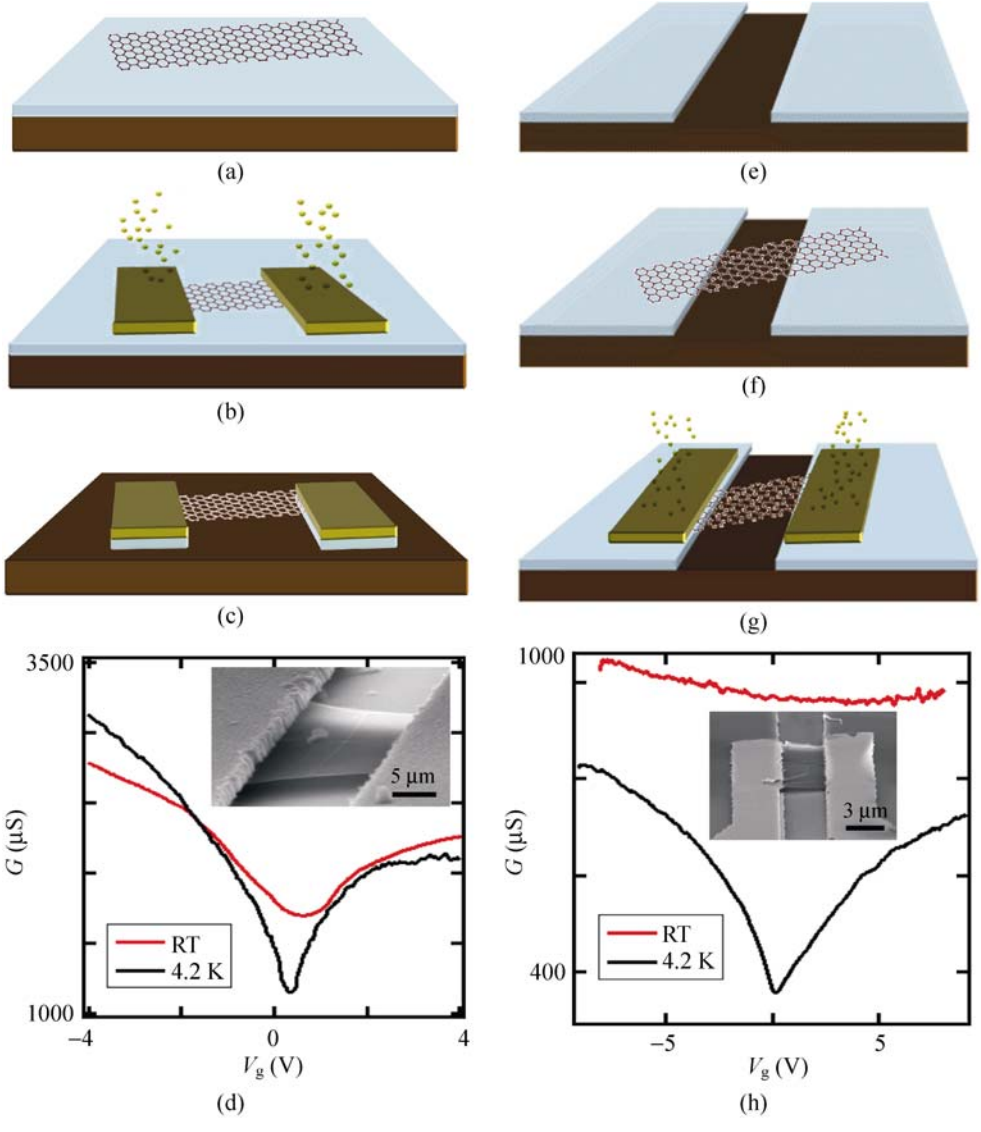

Figure 3 (a–c) Fabrication of suspended graphene devices via HF etching. (d) Plots of two-terminal conductance (G) vs. back gate voltage (V_g) for an HF-released single-layer graphene device at room temperature (red) and 4.2 K (black). Inset: SEM image of such a device. (e–g) Fabrication of suspended graphene devices over pre-defined trenches on the substrate. (h) Plots of G vs. V_g for a bi-layer graphene device over a trench at room temperature (red) and 4.2 K (black). Inset: SEM image of such a device

device fabricated using this technique. Since these suspended devices do not undergo any chemical processing, they are extremely clean. A gate voltage of up to 30 V can be applied to such a device, since graphene is supported by the banks of the trench, not by partially suspended thin film electrodes. The mobility of this bi-layer device was measured to be ~ 2000 $cm^2/(V \cdot s)$ at room temperature, and 60 000 $cm^2/(V \cdot s)$ at 4.2 K (Fig. 3(h)).

In conclusion, we have demonstrated a lithography-free technique for fabrication of high quality graphene devices, which may be either substrate-supported or suspended. Applications of this technique include ultra-clean devices for scanning tunneling microscope (STM) and optical measurements, or devices coupled to specialized (e.g., superconducting or ferromagnetic) electrodes. In particular, it provides an especially powerful approach for investigation of the mobility bottleneck for graphene devices, as it allows fabrication of ultra-clean devices that are free of both lithography contaminants and substrates.

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