View metadata, citation and similar papers at core.ac.uk

brought to you by CORE

provided by NASA Technical Reports Server

X-711-67-437

NASA TM X- 55949

SOME VARIATIONS OF TUNNEL DIODE PULSE GENERATOR CIRCUITS

NORMAN M. GARRAHAN

FACILITY FORM 602

N67 38535 (ACCESSION NUMBER)

22 (PAGES)

TMX-55949 (NASA CR OR TMX OR AD NUMBER)

(THRU) 1

(CODE) 09

(CATEGORY)

SEPTEMBER 1967

NASA

GODDARD SPACE FLIGHT CENTER

GREENBELT, MARYLAND

X-711-67-437

SOME VARIATIONS OF TUNNEL DIODE PULSE GENERATOR CIRCUITS

N67-30535

Norman M. Garrahan

September 1967

GODDARD SPACE FLIGHT CENTER
Greenbelt, Maryland

PRECEDING PAGE BLANK NOT FILMED.

ABSTRACT

This report describes a few of the new tunnel diode pulse generation circuits to be used on an x-ray investigation rocket experiment. Circuit component values are given with a brief explanation of the choice of input versus output pulse polarities. The reader is referred to NASA TN D-3558 for an in-depth analysis of these circuits.

PRECEDING PAGE BLANK NOT FILMED.

CONTENTS

LIST OF ILLUSTRATIONS

SOME VARIATIONS OF TUNNEL DIODE PULSE GENERATOR CIRCUITS

INTRODUCTION

During the past few years, part of the Explorer-series satellite activity has centered on scientific experiments for outer-space cosmic and x-ray particle detection and measurement. These experiments involved pulse-level detection, measurement, and coincident/anti-coincident logic circuits. This has necessitated designing increasingly complex nanosecond pulse-width logic circuits. Also, as the input requirements for identifying specific particle characteristics have expanded, so has the number of logic-identifier channels. This increase in equipment capacity carries with it a concomitant need for circuits with diminished power requirements.

The early approach for logic pulse generation circuits favored the use of power consuming blocking oscillators, but an effort was directed to finding a lower power "gentler" technique, particularly without the spike radiation and ringing problems of blocking oscillators.

The characteristically rapid impedance change-of-state of a tunnel diode when the current through it exceeded a certain switching point suggested an improved method of pulse generation. Subsequently, a circuit was developed having lower power consumption plus the capability of permitting presetting of the output pulse width simply by proper selection of a paralleling inductance across a tunnel diode.

Using this parallel-inductance-across-tunnel-diode technique to preset the turn-off time of a tunnel diode—hence output pulse width—a whole new family of fast-acting low-power pulse generation and threshold detection circuits were developed. These greatly simplified the designing of logic pulse coincident and inhibiting circuits in satellite, rocket, and balloon-borne equipment.

This report presents a compilation of a few of these circuits showing how each particular circuit configuration depends on the input pulse polarity and output pulse requirements; the reader is referred to NASA TN D-3558 for additional circuit specifics and design criteria.

BASIC CIRCUIT

Figure 1 shows the basic tunnel diode circuit wherein a tunnel diode is connected in the output leg of an emitter-coupled transistor pair to take advantage

of the well-known 'see saw' action between the conduction and nonconduction states of Q1-Q2 when the base bias of either is changed. The resistor bias network is chosen to favor a quiescent 'ON' state for Q1 and an 'OFF' state for Q2. An input trigger pulse into Q1 of proper polarity and above minimum amplitude overrides the hold-on bias on Q1, turning it off and switching the emitter current flow through R5 from Q1 to Q2; this pulse of current through tunnel diode CR1 causes it to change from a low impedance to a high impedance state resulting in either an approximate 0.6v pulse for germanium or an approximate 0.8v pulse for silicon appearing across it.

This exchange of on-off states exists for the duration of time that the input pulse exceeds the trigger-level bias setting of Q1, and which may be preset for a trigger sensitivity range of approximately 150-400 millivolts by varying the value of R6 between the bases. Hence, the output pulse width essentially follows the input pulse width while it remains above the threshold trigger level. This forms the basic pulse-level threshold-detection circuit. Where it is desired to limit the output pulse width, the technique mentioned earlier of paralleling the tunnel diode with a suitable inductance may be used—with the assumption that a value of 'L' would be chosen to insure that the output pulse width would always be less than the input pulse width.

In the case where an input trigger pulse embodies a variable risetime and random amplitude, the addition of an inductance across CR1 (Figure 1) may produce a minor but unacceptable fluctuation in the threshold detection point, hence CR1 is normally used sans the inductance but followed by a second threshold detector-type circuit, Q3-Q4, which includes small-paralleling-inductance L1 across tunnel diode CR2 to obtain a narrow-width pulse (about 47 microhenries for a 100 nanosecond pulse). Thus, the output width is now no longer input-pulse-width dependent and may be interfaced with succeeding logic circuits.

PULSE GENERATING CIRCUITS

The post-threshold detection and pulse-generating circuits generally assume the availability of fast-risetime trigger pulses of at least 0.5v amplitude (the typical output of a preceding similar tunnel-diode pulse generator). In some cases this is divided down to 0.4v with the 'sink-pulse' generator trigger point set at 0.3v; this effectively masks the sink-pulse generator from flutter turn-on by the source tunnel diode and insures that the source tunnel diode is close to full-on before the sink triggers. This has a net beneficial effect of 'tightening' the overall triggering action when carried through several stages. A small value of series coupling resistor (1-3 K ohm) will serve this purpose (e.g., R8 shown in Figure 1).

The most generally useful pulse generator configuration is the one shown in Figure 2 where the output is ac coupled back to the input*; once it is triggered by a narrow input pulse, conduction through the tunnel diode is maintained for the duration set by paralleling inductance 'L1'. As shown in the included waveforms when two tunnel diodes, CR1-CR2, are placed back-to-back, a negative input pulse will switch the current from Q1 to Q2 producing a bipolar pulse across CR1 and a unipolar negative pulse across CR2. By inverting the polarity of CR1-CR2, the positive pulse alone will be present at OUTPUT 2, delayed by time t1 from the leading edge of the trigger; thus a controlled-delay output is available (R5 isolates the feedback voltage from the input trigger source).

Where a positive pulse in phase with the leading edge of a negative trigger pulse is desired, the circuit of Figure 3 may be used. In this configuration, the tunnel diodes have been moved over to the collector leg of Q1 and the bias network altered to maintain Q2 in conduction and Q1 cutoff. The transistors have been changed to PNP types and the supply voltage to +3 volts. With this setup, a negative pulse into Q1 will turn Q1 'on' and the indicated pulses will appear at OUTPUTS 1 and 2. Again, by inverting the polarity of CR1-CR2, a choice of unipolar pulses is available at OUTPUT 2, the negative pulse being delayed by the width of the positive one. Silicon tunnel diodes were used here for a slightly greater output voltage of 0.8 volts. Figure 4 presents a case where the desired output in-phase pulse must be negative for a positive input trigger. Transistor Q2 is held 'on' by the bias network; the input pulse turns Q1 'ON', the tunnel diodes being in the normally off Q1 leg. Cascaded tunnel diodes are used to achieve twice the usual pulse amplitude; this output configuration requires a slightly greater drive because if lightly triggered only one of each pair of tunnel diodes is inclined to turn on.

A ready reference table (Table 1) showing the relationship between desired OUTPUT 1 pulse-polarity and the existing INPUT pulse-polarity together with OUTPUT 2 unipolar pulse variations is displayed. The bias network will, of course, have to be altered for each option.

Frequently in logic design, it is desired to inhibit a given pulse generator; Figure 5 shows how this may be accomplished for nanosecond-range pulses by placing a transformer in series with the emitter resistor. The transformer is polarized to null out the trigger pulse appearing across R4. Figure 6 shows another inhibiting variation using PNP transistors; the transformer input winding is reversed compared to Figure 5, which permits inhibiting from the same pulse-polarity source—an advantage of using this method of transformer

*As suggested by Ciro A. Cancro, Spacecraft Technology Division.

inhibiting when the pulse duration permits. The leading and trailing edges of the inhibit pulse should not be too sharp to avoid injecting spurious spikes into adjacent components.

Two inductors, L1 and L2 in Figure 6, are used, one across each tunnel diode. This permits setting the OUTPUT 2 pulse to a width smaller than the OUTPUT 1 positive pulse width. At Q1 turn-on, only L1 appears across CR1 because CR2 shorts L2 to ground; for the negative pulse, CR1 is shorted and L1 is in parallel with L2 across CR2.

Figure 7 also shows a variation of the versatile pulse-generator circuit where a positive-going input pulse is present and it is desired to generate an output trigger pulse of some specific width from its trailing edge. The feedback network between the output and input is omitted and the conduction duration of Q2 is set strictly by the input pulse width. Again, two inductors are used across the tunnel diodes; L1 is used to set the first positive pulse to a value less than the input but greater than the OUTPUT 2 pulse, then L2 sets the required OUTPUT 2 width. There is, of course, some interaction between L1 and L2 but this is easily resolved by trial and error experimenting.

In the circuit of Figure 8(a), the output pulse width is set by the RC time of C5, R2, R8, and R9. With R5 bypassed by C2 to speed up switching time and with R2 in the collector leg of Q1, gain is provided for the input trigger; hence the threshold trigger level is lowered. Resistor R8 may be used to raise the threshold level to the former trigger level of about 150 millivolts, if desired. Waveforms showing the function of C5 are included in Figure 8(b). Both sides of the capacitor rest at approximately -1.7v, set by the voltage divider and current thru R2. When an input trigger is applied, the inverted pulse on the collector of Q1 drives C5 towards ground, switching Q2 'on' and Q1 'off'. Then C5 begins to charge thru R9 to the potential level of Point 'X' (as set by the voltage divider), holding Q2 in conduction by virtue of the charging-current drop across R9 which subtracts from the hold-off bias at 'X'.

When C5 charges to about -1.2v, the charging drop across R9 is insufficient to counteract the hold-off bias of 'X', which now reasserts control of the switching action and drives the base of Q2 rapidly into cutoff. At this time, the voltage appearing from junction 'Y' to ground includes the charged value of 1.2v plus the 1.7v drop across R1. Capacitor C5 is now overcharged and will discharge thru R9, adding to the hold-off bias until it stabilizes at about - 1.7 volts. This 'overcharge' tail inserts a dead time wherein any new trigger pulse appearing during this period must overcome the additional hold-off bias. In the case shown in Figure 8, a silicon tunnel diode in series with a small 180 ohm resistor is used; this provides about 1 volt instead of the 0.8v which is typical with the silicon type.

Another version of this circuit is shown in Figure 9 in which the output requirement is for a pulse delayed from the trigger by time t1. This is set by the RC time of R1R5C1, a parallel example just discussed in the previous circuit. A unipolar and bipolar pulse pair are available at the two outputs and the widths of the individual pulses are still determined by the shunting-inductance L1. This circuit and that of Figure 8 are more restrictive on input-pulse polarity per given output-pulse polarity requirement than the circuit of Figure 2 because input transistor Q1 must always be 'on'. Hence, Options (A) and (D) of Table 1 will not apply to Figures 8 and 9. However, the output variations are still available.

SUMMARY

A new method of low-power tunnel-diode pulse generation has thus been reviewed together with several different configurations shown to illustrate specific output versus input pulse polarity and phasing. Pulse widths from 50 nanoseconds to several microseconds may be easily obtained by using the proper choice of circuits and Table 1. Figure 10 shows the approximate pulse widths which can be obtained in the circuit of Figure 2 for a given value of shunting inductance. As previously stated, a more detailed analysis may be found in previously published NASA Technical Note TN D-3558.

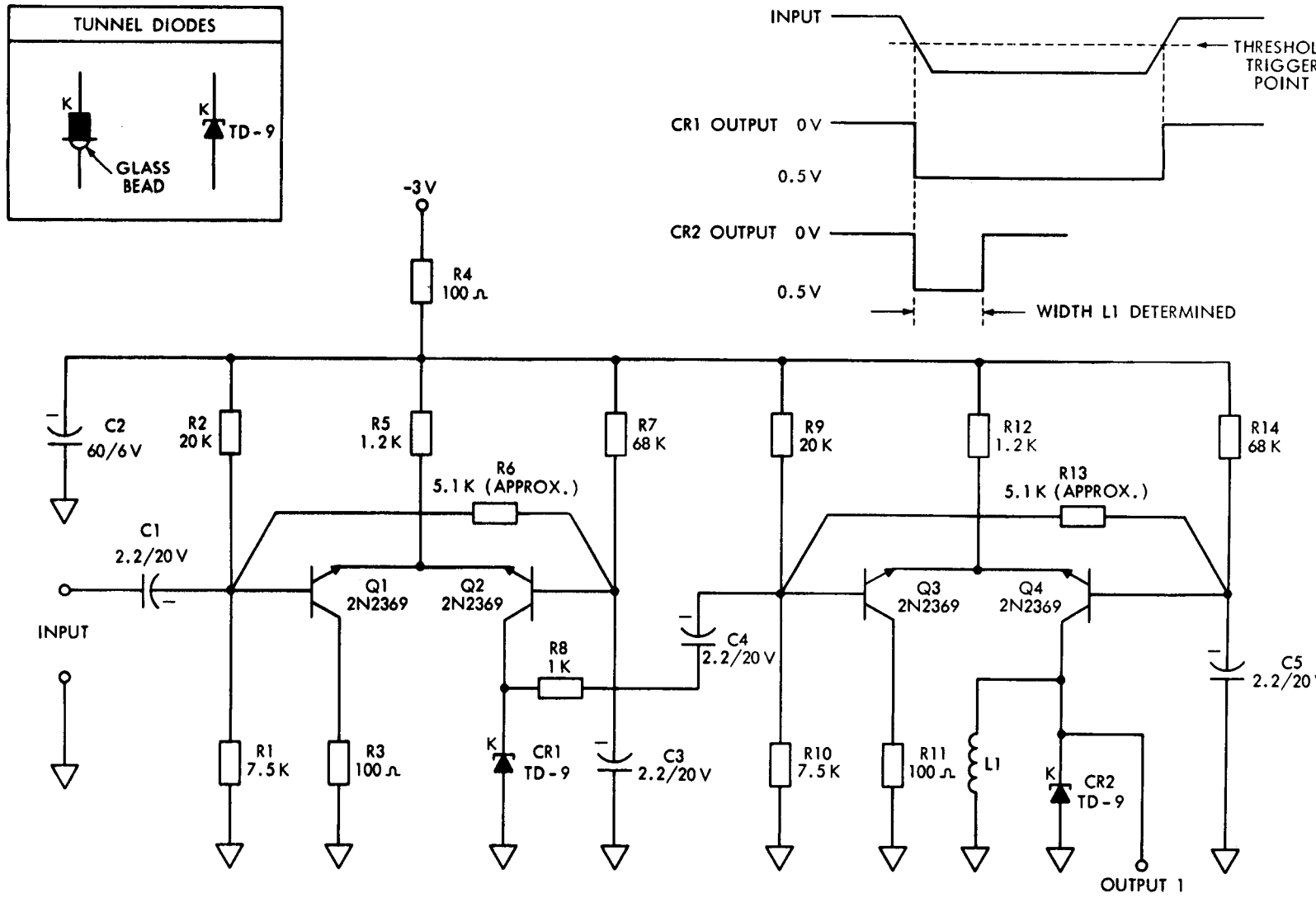
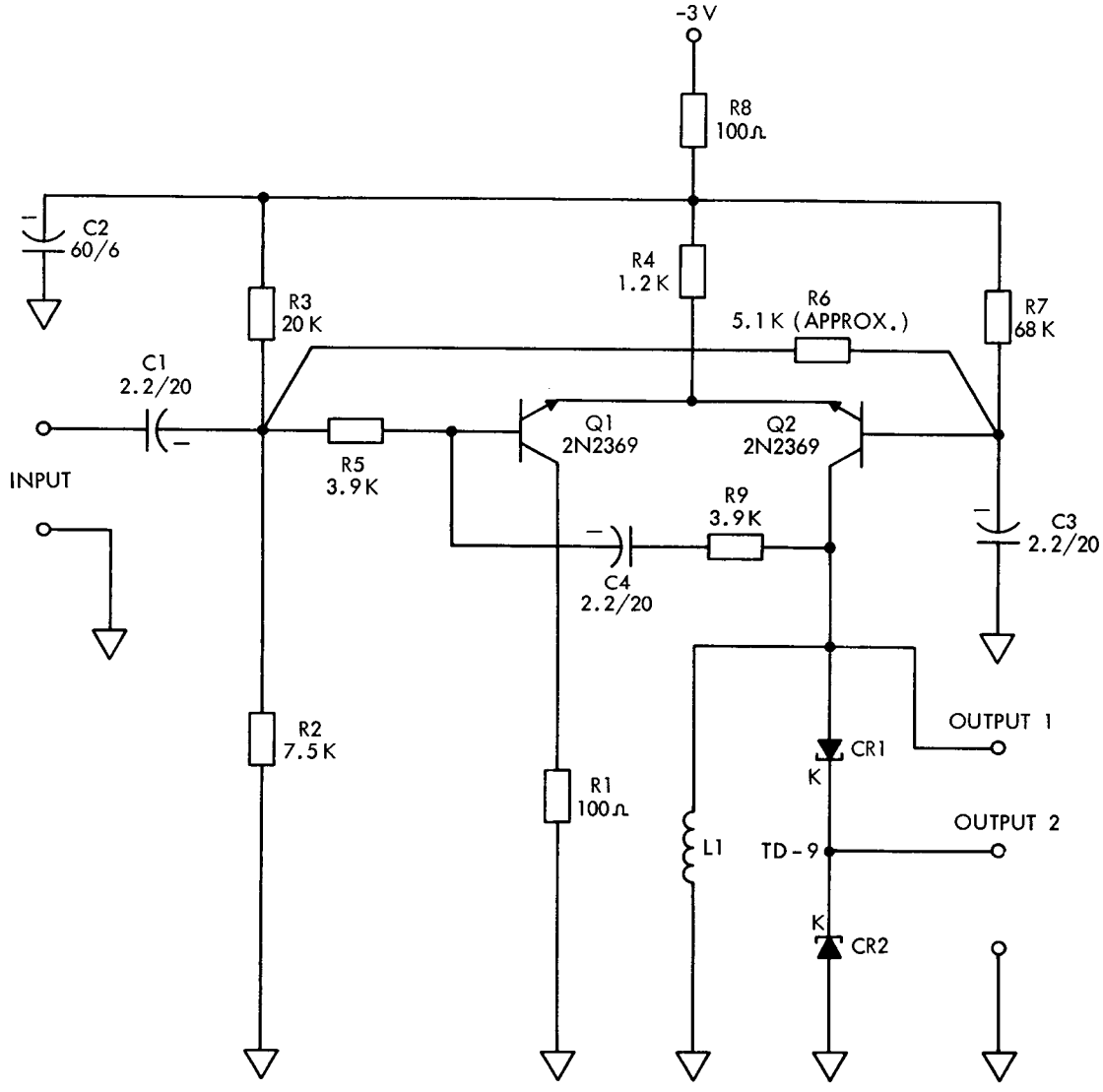
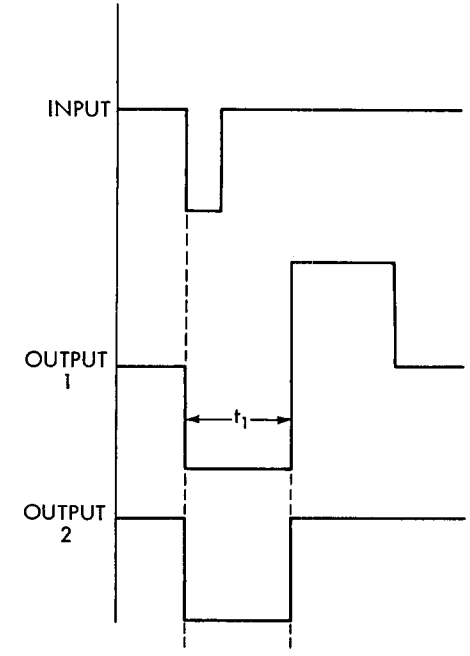


Figure 1. Threshold Detector





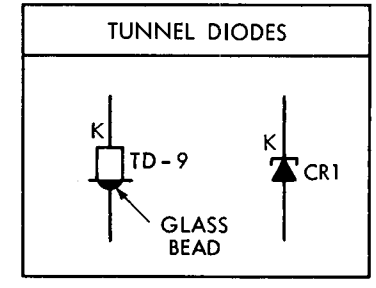


Figure 2. Pulse Generator, Type E

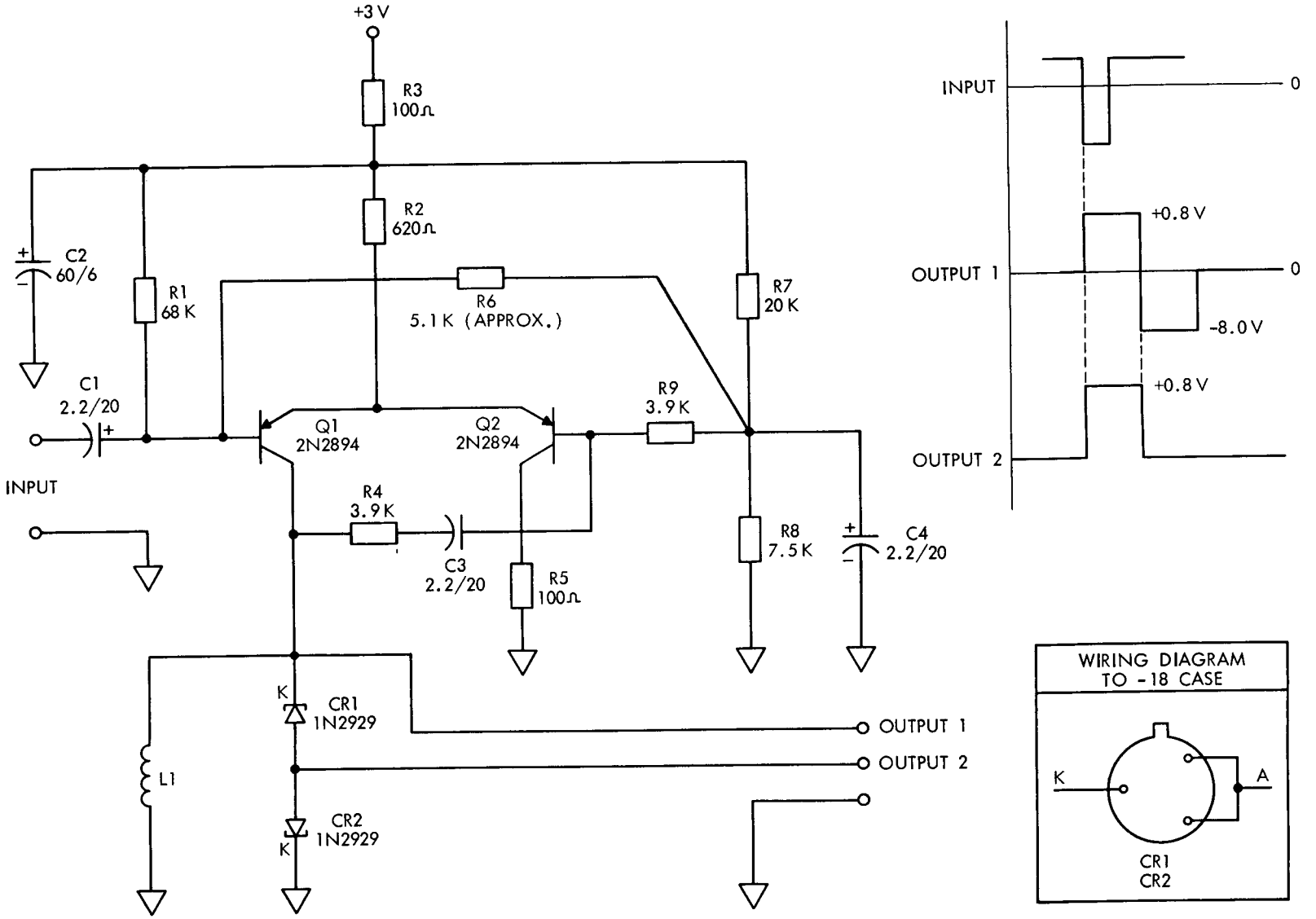
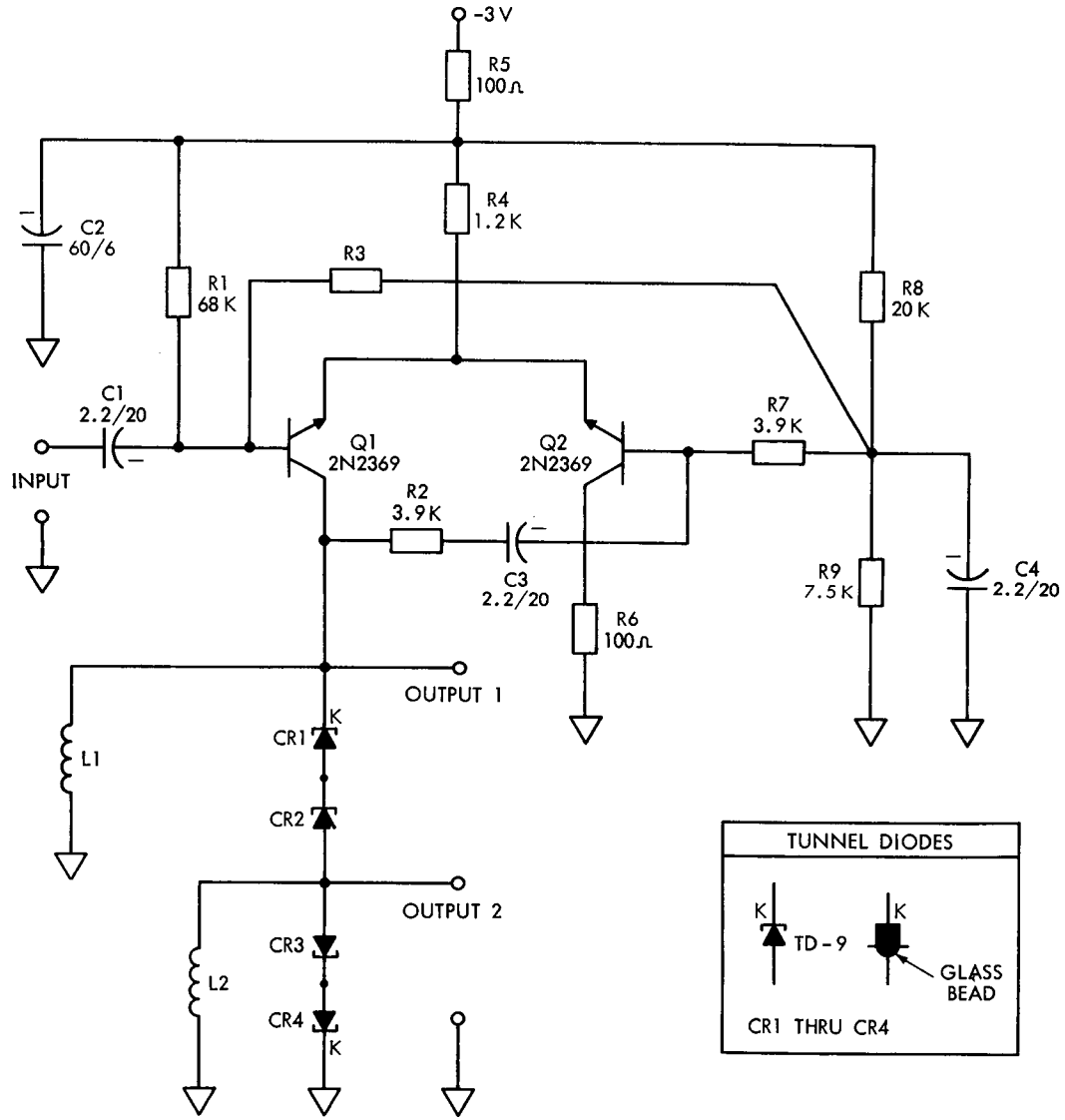


Figure 3. Pulse Generator, Type K



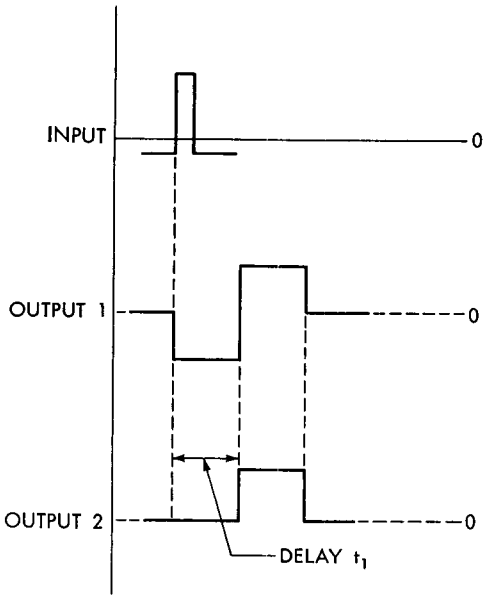


Figure 4. Pulse Generator, Type M

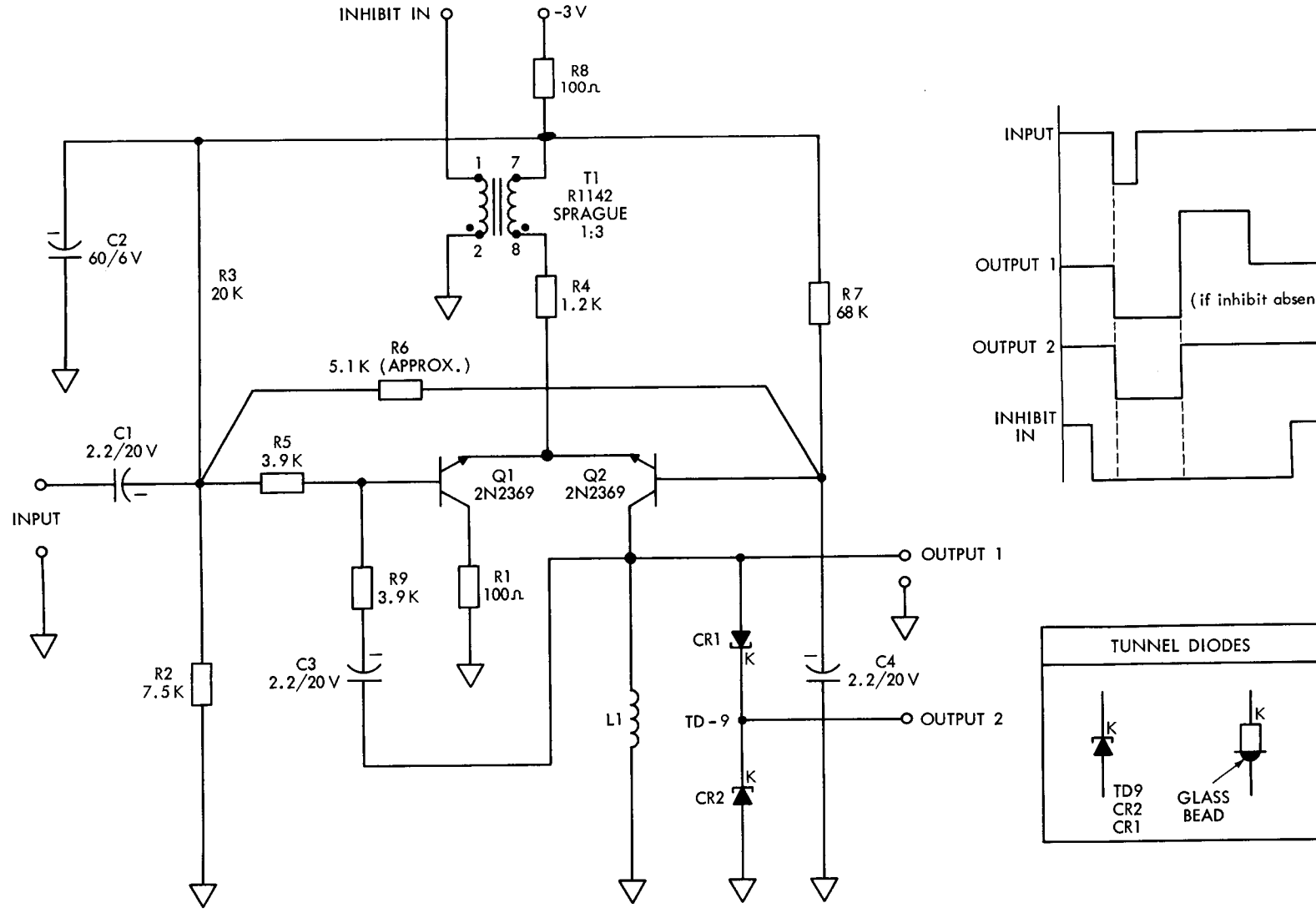


Figure 5. Pulse Generator, Type B

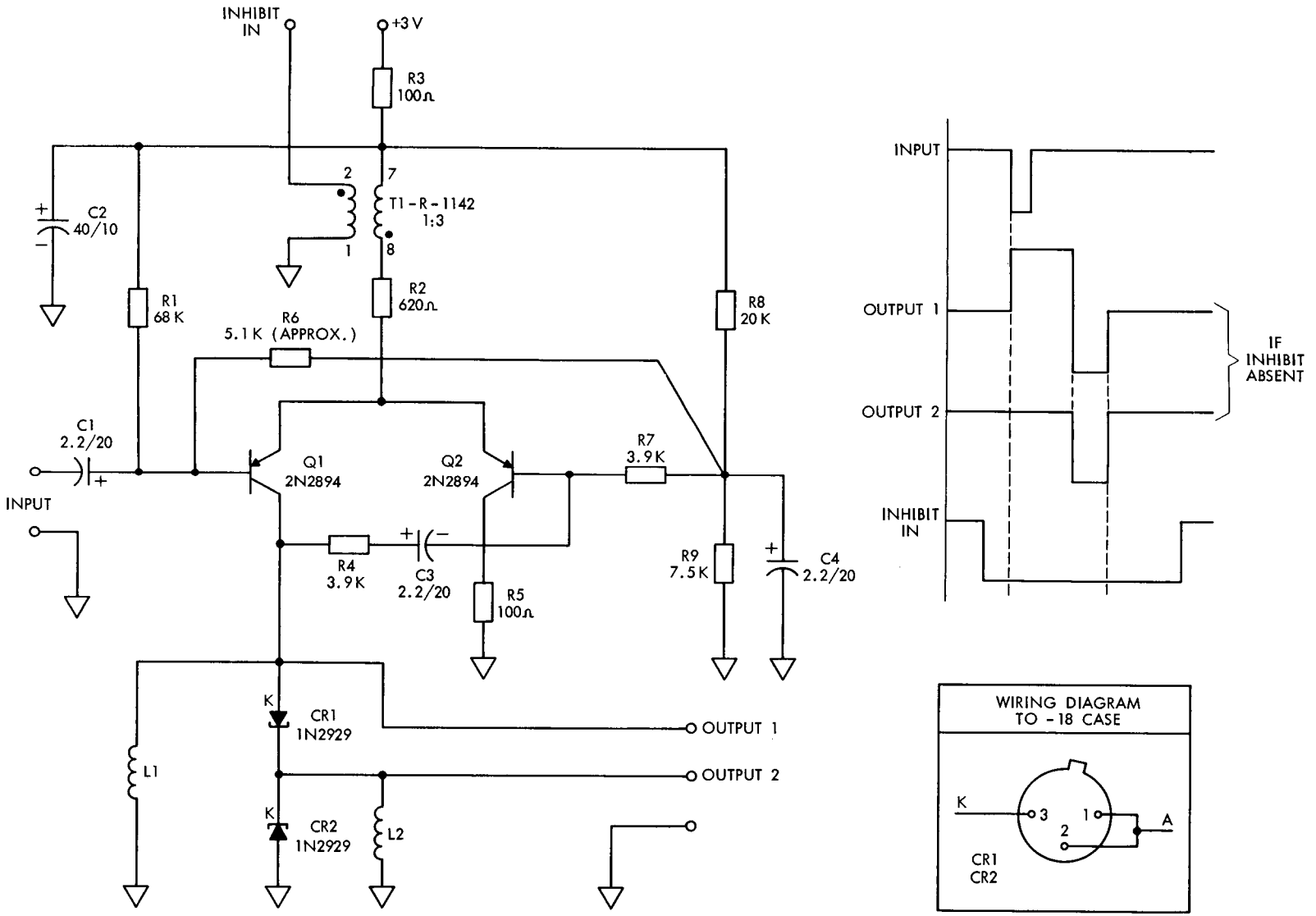
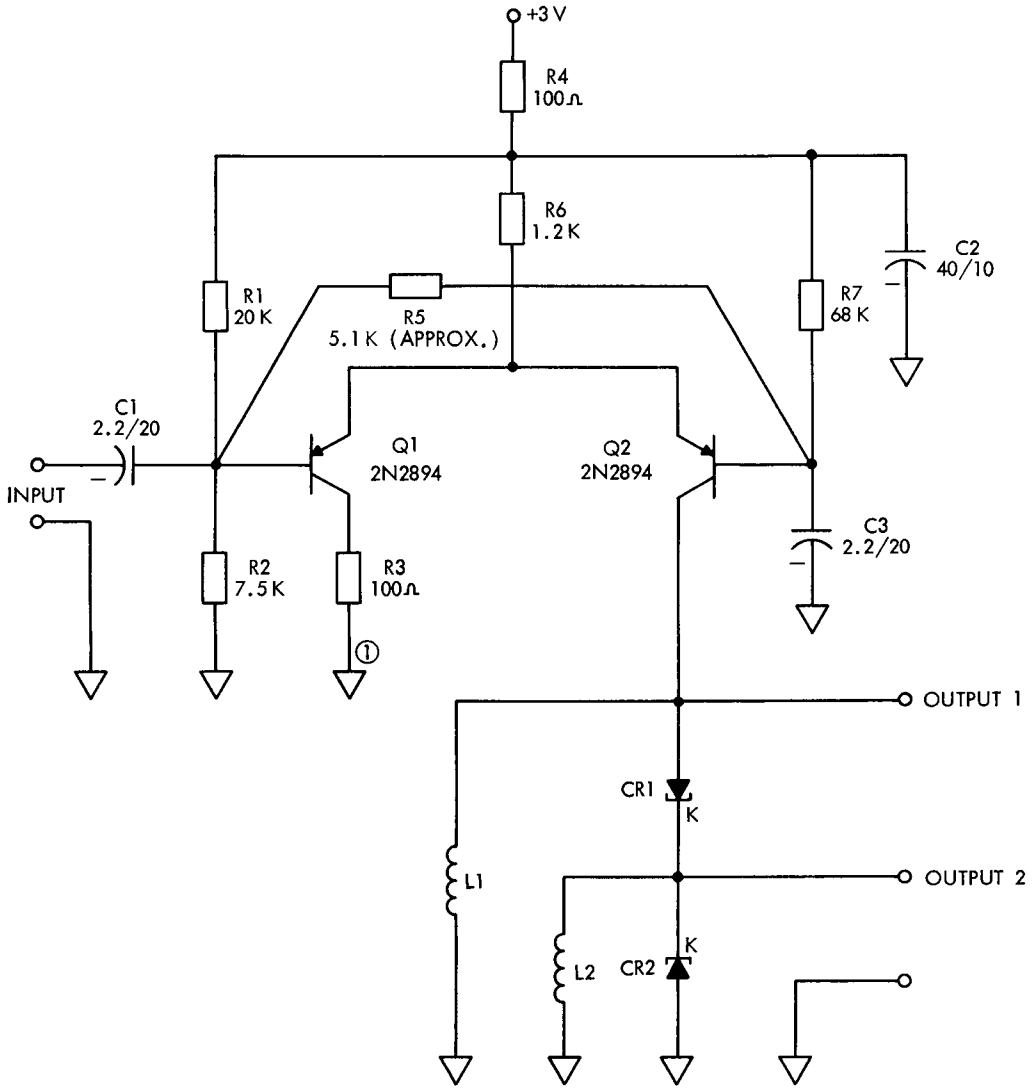
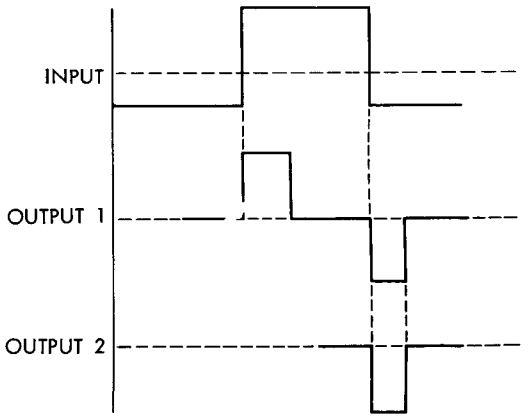


Figure 6. Pulse Generator, Type H





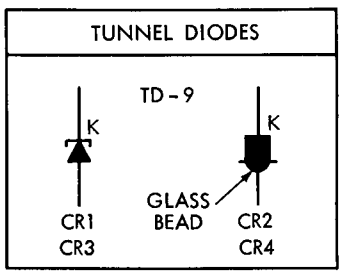
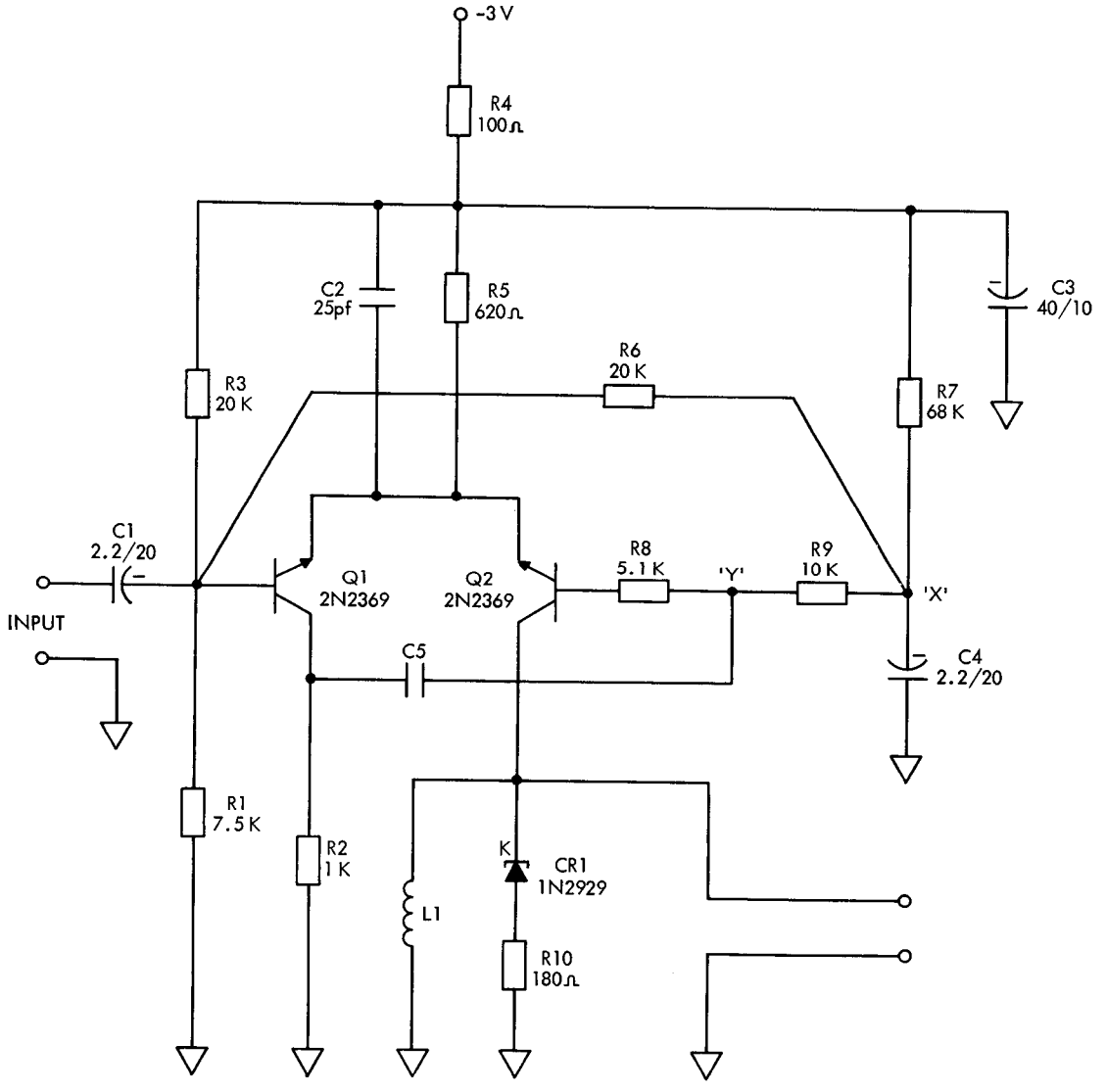
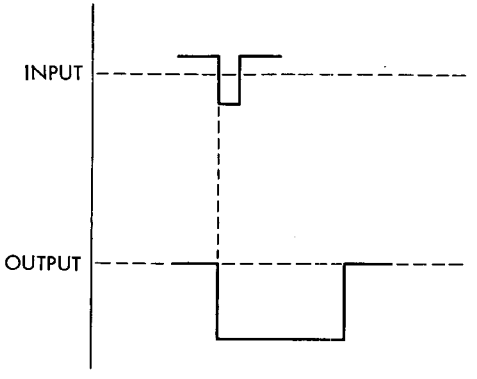


Figure 7. Pulse Generator, Type L





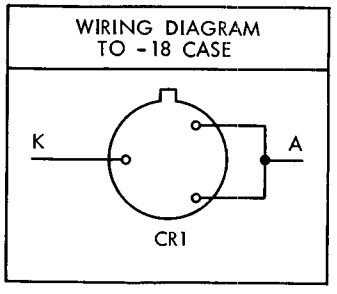


Figure 8(a). Pulse Generator, Type N

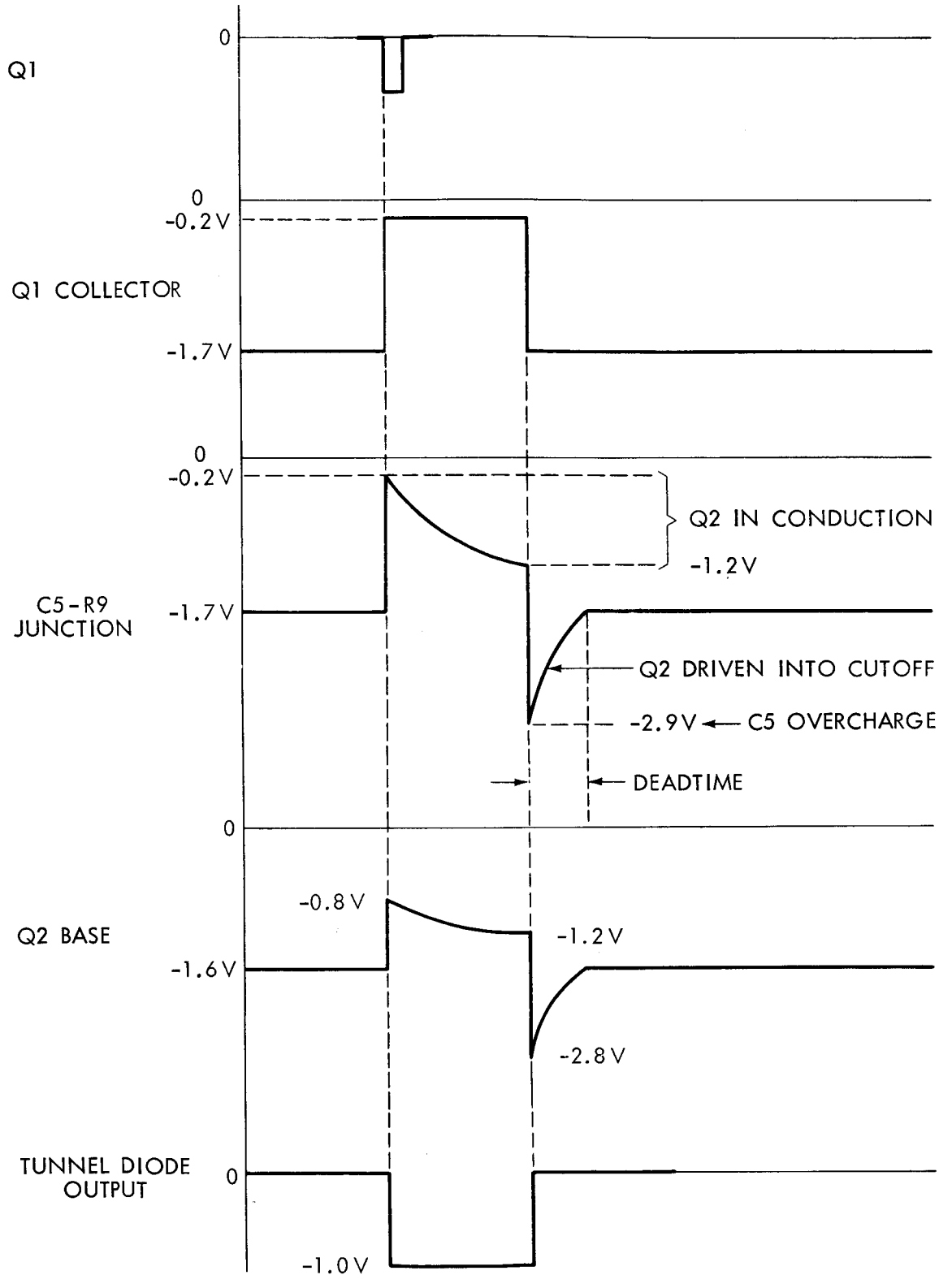
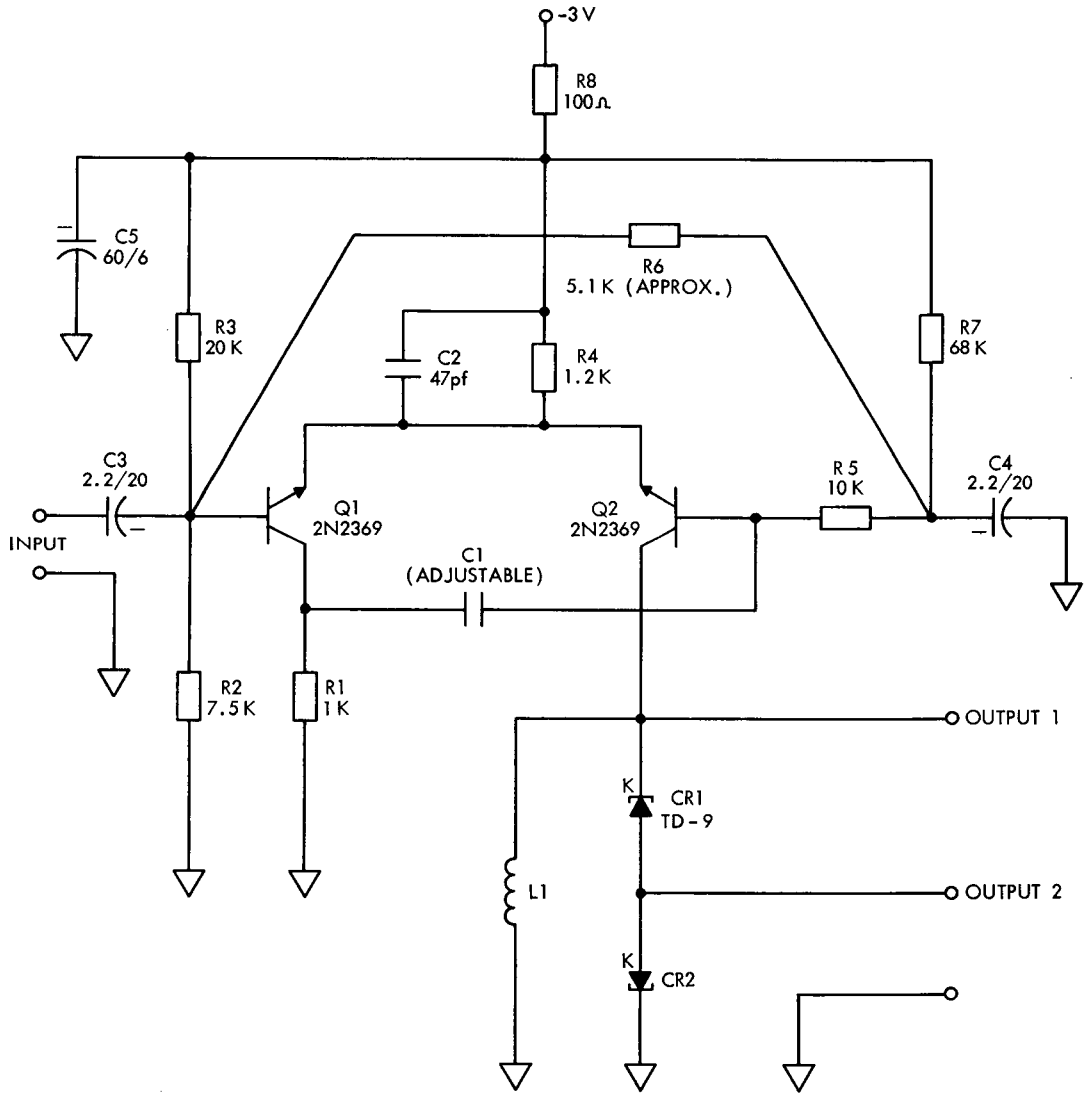
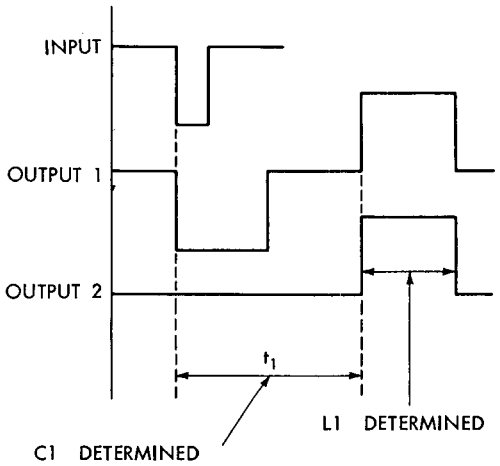


Figure 8(b). Pulse Generator, Type N, Waveforms





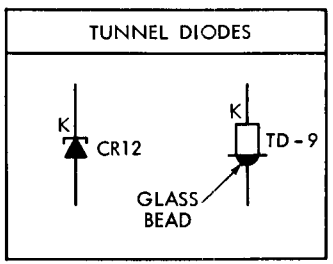


Figure 9. Pulse Generator, Type A

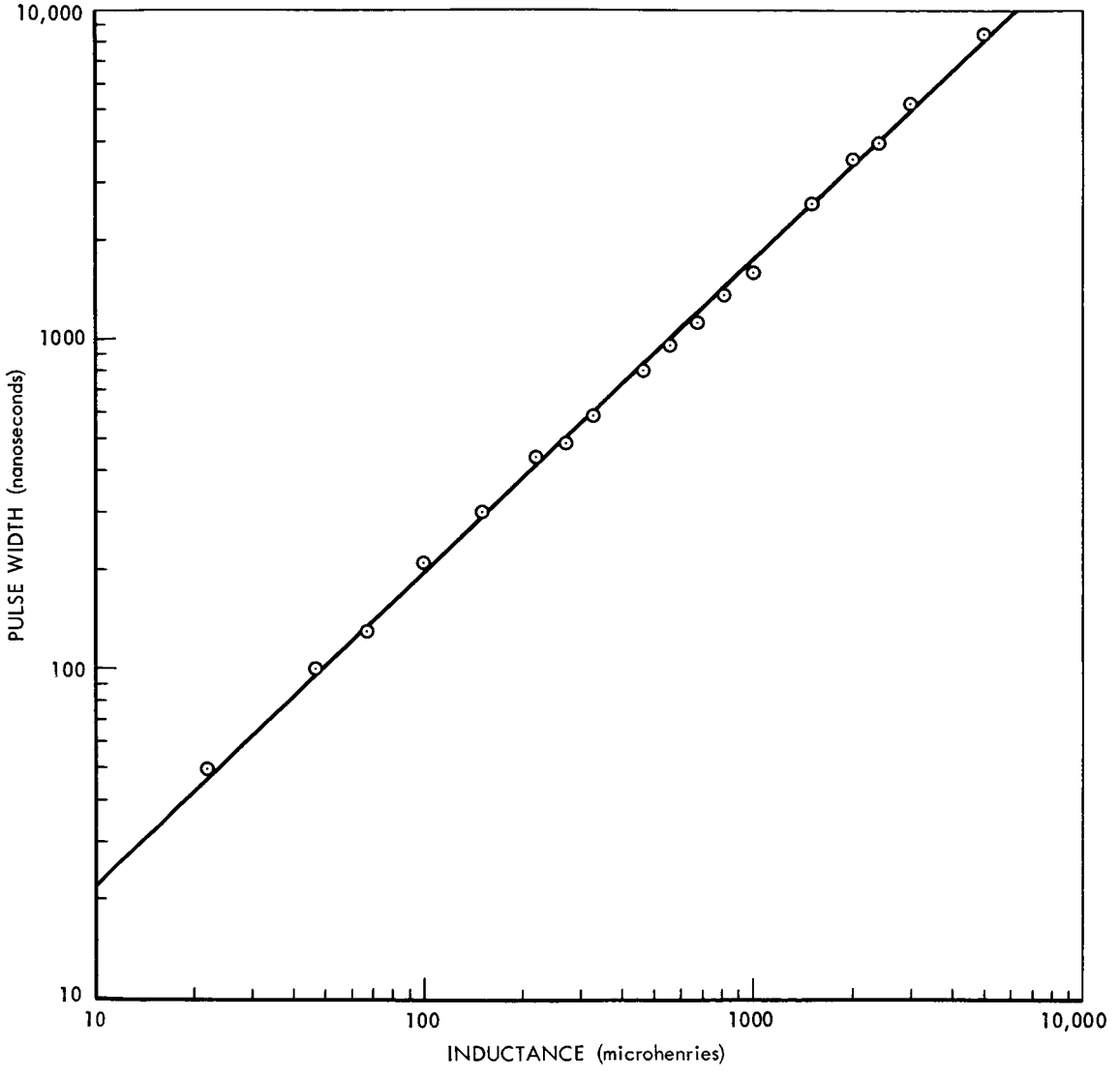
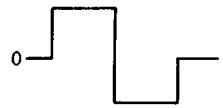
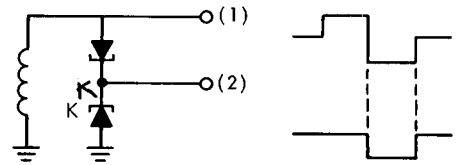
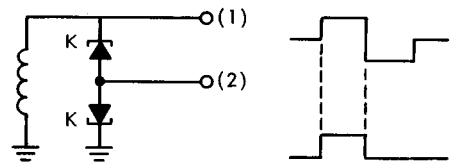
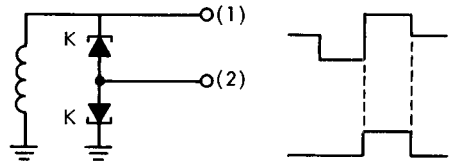


Figure 10. Typical Pulse Widths Obtained in Figure 2 for a 22 Microhenry to 5 Millihenry Inductance Range of L1

Table 1

Relationship Between Desired OUTPUT 1 Pulse-Polarity and Existing Input-Pulse Polarity Together with OUTPUT 2 Unipolar Pulse Variations

TRANSISTOR TYPE AND POLARITY OF PRIMARY POWER SUPPLY	INPUT PULSE POLARITY		DESIRED OUTPUT 1 PULSE	OUTPUT 2 VARIATIONS
	−	+		
PNP (+)	OPTION A	OPTION B		
	Q2 Biased "on" Tunnel Diodes in Q1 leg. Input pulse turns Q1 "on".	Q1 Biased "on" Tunnel Diodes in Q2 leg. Input pulse turns Q1 "off".		
NPN (−)	OPTION C	OPTION D		
	Q1 Biased "on" Tunnel Diodes in Q2 leg. Input pulse turns Q1 "off".	Q2 Biased "on" Tunnel Diodes in Q1 leg. Input pulse turns Q1 "on".