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NASA Contractor Report CR-1213

MAGNETIC AND ELECTRICAL MATERIALS CAPABLE OF OPERATING IN THE 800^{o} to 1600^{o} F TEMPERATURE RANGE

by R. E. Stapleton

December 1968

The main title of the report was inadvertantly omitted. It should be inserted as follows:

HIGH-TEMPERATURE CAPACITOR FEASIBILITY

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Prepared by
WESTINGHOUSE ELECTRIC CORPORATION
Lima, Ohio
for Lewis Research Center

NATIONAL AERONAUTICS AND SPACE ADMINISTRATION • WASHINGTON, D. C. • DECEMBER 1968

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MAGNETIC AND ELECTRICAL MATERIALS CAPABLE OF OPERATING IN THE 800° TO 1600° F TEMPERATURE RANGE

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Prepared under Contract No. NAS 3-6465 by
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PREFACE

This topical report on high-temperature capacitor feasibility was prepared at the Aerospace Electrical Division of the Westinghouse Electric Corporation under NASA Contract NAS3-6465. It represents part of the technical work being sponsored by NASA on the Development and Evaluation of Magnetic and Electrical Materials Capable of Operating in the 800° to 1600° F Temperature Range. Mr. R. A. Lindberg, Space Power Systems Division, NASA-Lewis Research Center, has provided the Project Management for the program. The program is administered for Westinghouse by Mr. P. E. Kueser as the overall program manager. The report was originally issued as Westinghouse Report WAED 67.24E, May 1967.

SUMMARY

Four candidate high-purity dielectric materials were fabricated into thin wafer, test capacitors and their electrical properties were measured in vacuum at temperatures up to 1100° F. These materials include: pyrolytic boron nitride (Boralloy), single crystal Al_2O_3 (Linde Sapphire), hot-pressed BeO (Atomics International) and polycrystalline Al_2O_3 (Lucalox).

The data shows that pyrolytic boron nitride (PBN) has superior electrical properties over the temperature range and can be fabricated into very thin (<0.001 inch) large area capacitor wafers.

A number of multi-layer capacitors (pyrolytic boron nitride dielectric) have been designed and evaluated at temperatures up to 1100° F. Sputtered, thin film electrodes were used on all devices. The feasibility of interconnecting these electrodes without supplementary metal foil tabs has been demonstrated. Thus, a volume parameter ($\mu F \cdot volts/in^3$) equivalent to most conventional low temperature (200° to 400° F) capacitors has been achieved.

An extended life test was successfully completed on a five wafer pyrolytic boron nitride (PBN) capacitor at 1100° F in vacuum. The unit was energized at 500 Vd-c/mil for 259 hours, 750 Vd-c/mil for an additional 218 hours, and 1000 Vd-c/mil for another 643 hours. Electrode instabilities caused by diffusion bonding of electrodes on adjacent wafers and a partial loss of electrode adherence contributed to a decrease in capacitance (~3%) and increase in $\tan\delta$ (0.0023 to 0.0035 @ 1 kc/sec) after a total of 1120 test hours. These results indicate where improvements can be made in the fabrication process.

Some typical properties measured for pyrolytic boron nitride capacitors are as follows:

1.	Minimum Wafer Thickness	0.4 to 1.0 mils
2.	Maximum Capacitance Change (R.T. to 1100° F)	-1.7%
3.	Tan δ @ 1100° F (50 cps to 50 kc/sec	0.0018 to 0.007
4.	RC Product @ 1100° F (Megohm x μF)	10 to 25
5.	DC Breakdown Voltage 1100° F, 1-mil wafer	7000 V/mil [$<10^{-6}$ torr]
6.	Volume Parameter - uncased μF x volts d-c/in^3	400 to 870 @ 500 Vd-c

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SECTION I

INTRODUCTION

This Topical Report is the result of work conducted on Contract NAS3-6465 for the Development and Evaluation of Magnetic and Electrical Materials Capable of Operating in the Temperature Range from 800° to 1600° F. The contract consists of three programs as follows:

Program I - Magnetic Materials for High-Temperature Operation

Program II - High-Temperature Capacitor Feasibility

Program III - Bore Seal Development and Combined Materials Investigations Under a Space Simulated Environment

Program II is the subject of this report which presents the results of an investigation to determine the feasibility of building a lightweight compact capacitor suitable for operation up to 1100° F in vacuum with low electrical losses. One type of application for such a device is in static power conditioning apparatus for space applications.

A lightweight capacitor capable of operating in the 1100° F temperature range without supplemental cooling must have low electrical losses, high capacitance stability, and a volume parameter ($\mu F \cdot volts/in^3$) comparable to equivalent capacitor types designed for considerably lower operating temperatures. These considerations have lead to several specific program goals which include:

1.	Volume Parameter: ($\mu F \cdot volts/in^3$)	50 to 150
2.	Dissipation Factor (max.) at 1100° F:	0.005 to 0.02 (60 cps to 50 kc/sec)
3.	Capacitance Change:	$\pm$5% (R.T. to 1100° F)

An experimental program was initiated because capacitors presently available from commercial sources have limited maximum operating temperatures (up to 700° F for a few types) and they are usually bulky and have rather high electrical losses at elevated temperatures. In addition, it was recognized that several promising high-temperature dielectric materials were available but not in a form required for efficient capacitor design.

The overall objective of this program is to demonstrate methods of fabricating single-wafer capacitors from this group of candidate dielectric materials and then select the most promising material for more detailed study in the form of thin parallel interconnected capacitor wafers to achieve capacitor units of greater total capacitance. The program is concluded with a life test performed at 1100° F in vacuum using multi-layered test capacitors.

The results obtained on this program are presented in Sections II and III and the conclusions and recommendations for further work are listed in Section IV. Section II details the results of a dielectric material screening process and is concluded with the selection of a single capacitor dielectric for further evaluation in a multi-layer configuration. The methods used to lap and polish various candidate materials are outlined, (Appendix A shows the design of the lapping fixtures used to prepare one-mil pyrolytic boron nitride wafers), the "triode" method of sputtering thin film electrodes is discussed, and the electrical data obtained for each of the materials in the form of single wafer capacitors is presented and evaluated.

Section III of this report contains the work performed during the next phase of the program on multi-layer capacitors. Included in this section are: 1) a description of the interconnection approach used to electrically connect thin electrodes on individual wafers in a stacked capacitor, 2) the results of a study to demonstrate this concept with an evaluation of two different wafer geometries and a discussion of factors contributing to a-c losses, 3) the methods used to control and measure sputtered electrode thicknesses, 4) the results of electrical measurements to 1100° F in vacuum, and 5) an analysis of endurance tests performed at 1100° F in vacuum for times up to 1120 hours.

Section V lists the references specifically cited in this report and a group of general references including all quarterly reports prepared on Contract NAS3-6465.

SECTION II

PROCESSING AND EVALUATION OF SINGLE WAFER CAPACITORS

This section of the report contains the results of a comparative evaluation of the electrical properties of several dielectric materials. A final material selection is made on the basis of these data and the relative fabricability of different materials is discussed. To achieve a high capacitance per unit volume it is evident that the capacitor dielectric must be made as thin as possible. Therefore, the first goal of the program was to devise methods of fabricating thin (0.002 to 0.006 inch) high-quality capacitor wafers from "as received" materials so that a meaningful comparison could be made. This approach is illustrated in outline form in figure 1.

A. CANDIDATE MATERIAL PROPERTIES

Five dielectric materials were selected for single-layer capacitor evaluation from the group of ten candidate materials shown in table 1. Three different process forms of aluminum oxide were initially selected including:

1) A hot-pressed material prepared from Linde A powder (on AF33(615)1360)

2) A single crystal sapphire made by the Verneuil process (Linde Division, Union Carbide Corp.)

3) A polycrystalline, sintered material (G.E. Lucalox)

Hot-pressed beryllium oxide (Atomics International) and a pyrolytic form of boron nitride (Boralloy, High Temperature Materials Inc.) were also selected. Significant property data available at the beginning of this program are shown in table 1.

Table 2 shows a typical spectrochemical analysis for each of these materials. It is noteworthy that although all the materials listed have very low impurity contents, pyrolytic boron nitride (PBN) has a total metal impurity level of less than 0.003%.

B. FABRICATION OF SINGLE WAFER CAPACITORS

1. Slicing

All candidate materials received in bulk form as indicated in table 1 were sliced into thin wafers with a water-cooled diamond cut-off wheel (WMSA Precision Wafering Machine,

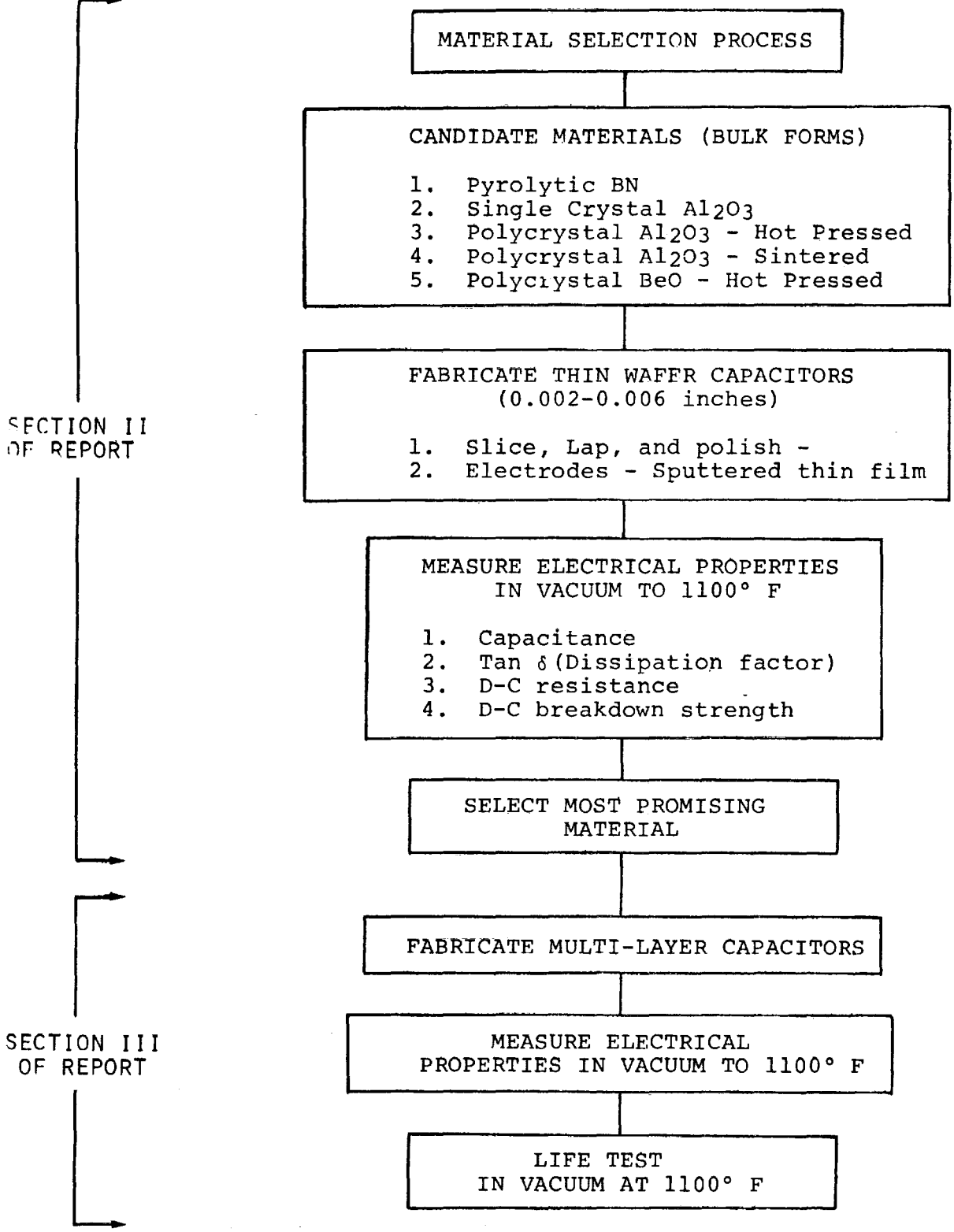


FIGURE 1. Outline of Approach to Determine High Temperature Capacitor Feasibility

TABLE 1. Tabulation of Candidate Dielectric

Material	Microstructure	Process Method	Mfg. or Source and Trade Name	Form (as received)	Purity	Density - % of Theoretical
Al_2O_3	Single Crystal	Verneuil (flame fusion)	Linde Div. Union Carbide Corp.	"Boule" ~ 3/4 in. Diam. x 3 in. long	< 100 ppm impurities (1)	~100
Al_2O_3	Polycrystalline	Pressed and Sintered	General Electric "Lucalox"	Rods 3/4 to 1-1/4 in. diam.	99.9% Al_2O_3 (1)	~100
Al_2O_3	Polycrystalline	Hot Pressed	(W)AED (experimental)	Disks: 0.416" dia. 0.020" thick	Starting Material Linde A < 100 ppm impurities	~100
BN	Hexagonal layer High degree of orientation	Pyrolylic decomposition of BCl_3 and NH_3	High Temperature Materials Inc. "Boralloy"	Plates 1 x 1 x 1/8 in. 2 x 2 x 1/4 in.	Total impurities ≅ 100 ppm (1)	~ 98
BN	Polycrystalline	Hot Pressed	Carborundum Company	None Ordered	97% BN	> 93.4
BN	Polycrystalline	Hot Pressed	National Carbon Company	None Ordered	~ 95 to 97% BN	~ 90
BeO	Polycrystalline	Pressed and Sintered	Coors BD 99.5	None Ordered	99.5% BeO	~ 95
BeO	Polycrystalline	Pressed and Sintered	American Lava Corp. Alsimag 754	None Ordered	99.5% BeO	
BeO	Polycrystalline	Hot Pressed	Atomics International (experimental)	Disks: 0.470" dia. 0.006" thick	Starting material - Minox AAA (1)	~99.7
MgO	Single Crystal	Cooled Melt	Norton Co. "Magnorite"	None Ordered	99.9% MgO	~100

(1) See table 2 for spectrochemical analysis of materials.

Material Properties-[Published]

PUBLISHED ELECTRICAL PROPERTIES					
DC Resistivity Ohm-Cm (approximate values)	Tan δ	Dielectric Constant	Electric Strength (voltage breakdown)	Remarks	Data Reference
400°C - 7 x 10^{12} 600°C - 7 x 10^{10}	@ 10^5 cps ⊥ to optic axis 400°C - 0.0002 600°C - 0.001	@ 10^5 cps 60° to optic axis K@20°C - 9 K@900°C - 10	1700 volts/mil @ 60 cps, 20 mil thick sample (Room temperature)	No electrical breakdown strength at elevated temperature. Tan δ and dielectric constant data not given for 60 cps to 50 kc freq. vs. temp.	F-814-C (2/1/62) F-917-B (10/2/61)
400°C - 1 x 10^{13} 600°C - 3 x 10^{10}	@ 9720 mc 20°C - 0.000025	@ 9720 mc 20°C - 9.9	1700 volts/mil @ 20°C, 20 mil thick sample	Low frequency (60 cps to 50 kc) tan δ and dielectric constant not given. High temperature voltage breakdown not given.	General Electric Lamp Dept. Data Bulletin, L-2-R January 1963
400°C - 5 x 10^{12} 600°C - 9 x 10^{10}	Not Measured	Not Measured	Not Measured	Disks hot pressed between graphite spacers - some contamination from graphite.	Final Report, March 1965, AFAPL-TR-65-22 (AF33(615)1360)
400°C - 10^{14} 600°C - 10^{13}	@ 4kmc, "a" direction RT to 649°C, approximate 0.0004 over the temperature range	K=3.4 "c" direction @ RT, not measured at elevated temperature	4000 volts/mil in "c" direction, d-c 10 to 20 mil sample (not measured at elevated temperature)	Low frequency data not available (vs. temperature) (60 cps to 50 kc)	Materials in Design Eng., Feb. 1964 (M. Bosche & D. Schiff)
420°C - 1.7 x 10^{11} 550°C - 8.3 x 10^8 660°C - 3.4 x 10^7	@ 10^3 cps 400°C - 0.012 600°C - 0.14	@ 10^3 cps 400°C - 4.5 600°C - 6.5	1450 volts/mil @ RT, sample 10 mils thick	Not selected as candidate material because of low density.	Carborundum Co. Data Sheet, Electronic Div., Latrobe Plant, Latrobe, Pa. (no date)
482°C - 5 x 10^8 1000°C - 1 x 10^7	@ 10^3 cps 300°C - 0.015 575°C - 1.0	@ 10^3 cps 21°C - 4.4 300°C - 4.52	500-1000 volts/mil, thickness not known	Not selected as candidate material because of low density.	National Carbon, Catalog Section H-8745 (no date)
300°C - >10^{15} 500°C - 5 x 10^{13} 700°C - 1.5 x 10^{10}	No low frequency data given	@ 1 mc 6.7	700 volts/mil average RMS at RT, 10 mil sample thickness	Not selected as candidate material because of lower density and purity compared to hot pressed BeO. (A. I.)	Coors Porcelain Co. Data Sheet 0001 Revised Aug. 1964
400°C - 10^{13} 600°C - 10^{12}	No low frequency data given	~7	None given	Not selected as candidate material because of lower density and purity compared to hot pressed BeO. (A. I.)	Am. Lava Corp, Chart No. 671, Mech. and Elect. Properties of Alsimag Ceramics
No measurements	No measurements	No measurements	No measurements	Sample requested.	Letter dated March 10, 1965 (65AT-1660) from R. L. McKissen, Atomics International
600°C - 1.6 x 10^{12} 1000°C - 10^8	@ 100 cps 25°C - 0.0003	@ 100 cps 25°C - 9.65	No data given	Not selected as candidate material because of hygroscopic characteristics.	Norton Co. Refractories Div. Experimental Product Memorandum, Feb. 1963

TABLE 2. Spectrochemical Analysis

MATERIAL	ELEMENTS													
	Al	Fe	Mg	Ti	Mn	V	Na	Cu	Ni	Ca	Cr	Ga	Si	Mo
	Percent (%)													
Lucalox (General Electric Co.)	Major	0.002	0.15	(1)	(1)	(1)	(1)	(1)	(1)	0.004	(1)	(1)	0.03	(2)
	Parts Per Million (ppm)													
Linde Sapphire (Single Crystal Al_2O_3)	(1)	< 2	< 2	(2)	(2)	(2)	(2)	(2)	(2)	9	(2)	(2)	6	(2)
	Percent (%)													
Boralloy, Pyrolytic Boron Nitride(3) (High Temperature Materials Inc.)	(1)	(1)	(1)	(1)	(1)	(1)	(1)	0.0001	(1)	0.0001	(1)	(1)	0.0001	(1)
	Parts Per Million (ppm)													
Minox AAA BeO powder used to prepare hot pressed materials by Atomics International	75	35	50	1	1	--	75	1	7	80	15	--	25	< 3
	Parts Per Million (ppm)													
Linde A Powder (Al_2O_3) used to prepare hot pressed disks by Westinghouse	Major	1.4	1.5	--	(1)	--	--	2.6	--	11.0	(1)	--	8.0	--

(1) Not detected.
(2) These elements not listed.
(3) Total impurities less than 0.0003%. Besides the elements shown, 34 additional ones were listed as not detected.
(4) Determined by polarographic and calorimetric techniques.

of Candidate Dielectrics

B	Zr	Cd	Pb	Ba	Bi	Co	Sm	Li	Sn	Ag	As	Pb(4)	REFERENCE SOURCE
(2)	(2)	(2)	(2)	(2)	(2)	(2)	(2)	(2)	--	--	--	--	ASD TR-61-628, Part II. Studies of the Brittle Behavior of Ceramic Materials, April 1963 - Contract AF33(616)7465
(2)	(2)	(2)	(2)	(2)	(2)	(2)	(2)	(2)	--	--	--	--	Letter from B. G. Benak, dated March 1965 (Linde Co.)
Major	(1)	(1)	(1)	(1)	(1)	(1)	(1)	(1)	--	--	--	--	High Temperature Materials, Inc. Data Sheet, dated February 1, 1965.
<1	<30	<1	<2	<5	<5	<1	<5	<5	--	--	--	--	Letter from R. L. McKisson, dated March 10, 1965 (Atomics International)
(1)	--	(1)	--	--	--	--	--	--	(1)	0.6	< 0.03	50-200	Letter from P. S. Whipple dated February, 1968 (Union Carbide)

Micromesh Manufacturing Corporation). Lucalox rod was sliced into wafers ranging in thickness from 8 to 15 mils. Pyrolytic boron nitride was sliced into 10- to 12-mil thick wafers. A yield of five wafers per 1/8-inch thick block was obtained. Sapphire was more difficult to slice into 10-mil wafers but wafers in the 20-mil thickness range could be reproducibly made.

Table 1 lists the "as received" sizes of each of these materials. The materials were mounted and sliced by the following general procedure:

a) Mounting: Figure 2 shows a 3/4-inch diameter by 3-inch long Lucalox rod cemented to a glass plate with LOC-Wax 20 (Geoscience Instrument Co.). Pyrolytic boron nitride and sapphire were similarly prepared.

b) Slicing Machine: WMSA Precision Wafering Machine.

c) Diamond Wheel: Metal Bonded Diamond Wheel manufactured by Norton Co., Abrasives Div. Wheel Diameter - 5 inches.
Wheel Thickness - 0.017 inches
Manufacturer's Identification 1-5 x 0.015 x 5/8, D220-N100M-1/8, ME 73082

d) Travel Speed: Wafers were cut at longitudinal table speeds in the range from 0.059 to 0.111-inch per minute.

e) Coolant & Wheel RPM: Water was used as a coolant. The wheel was rotated at 3800 rpm during all cutting operations.

Later in the program thin wafers of pyrolytic boron nitride were prepared by several different methods. The method outlined above was satisfactory for the harder aluminum oxides, but because pyrolytic boron nitride is a relatively soft material (hardness, Moh's scale-2) it can be easily machined without water cooling. Two alternate approaches gave good results.

a) dry slicing completely through blocks of material with a thin diamond wheel or a rubber bonded silicon carbide wheel (Norton, Type 37C240,-V8R-30) and

b) cleaving wafers from a prenotched block.

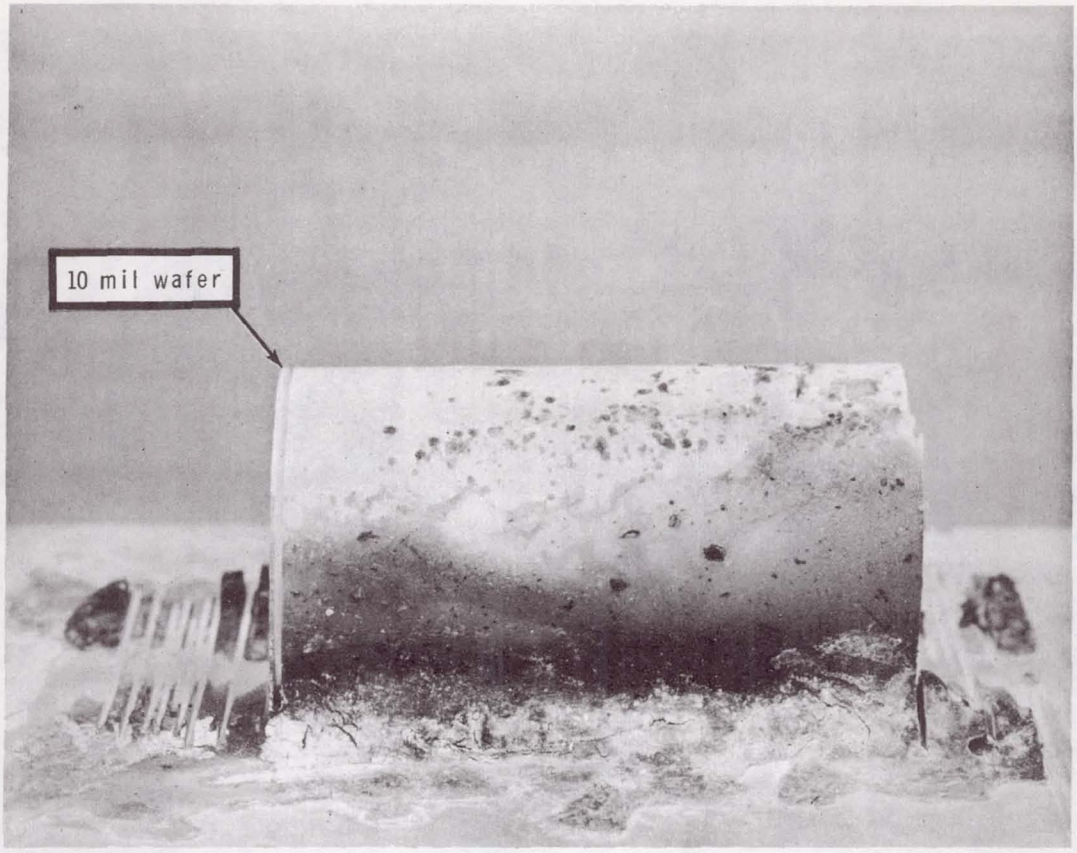


FIGURE 2. Lucalox Rod Stock (0.750-inch diameter) With 10-Mil Sliced Wafer Held in LOC-Wax 20 (Geoscience Instrument Co.)

The cleavage method is illustrated in figure 3 which shows a photograph of a one-inch square block of pyrolytic boron nitride that has been partially sliced with a series of multiple slits on one edge. Individual wafers were cleaved from this block by positioning a single edged razor blade in one of the slits and applying a light uniform pressure. Using this technique, a yield of about 15 wafers per 1/4-inch-thick block was obtained compared to a yield of about 9 wafers by completely slicing thru the block with a 0.016-inch-thick diamond wheel.

All wafers (1 inch by 1 inch by 0.008 inch) used during the later phases of the program were prepared by making slits from 1/8- to 1/4-inch deep along one edge of PBN blocks 1/8- or 1/4-inch thick. The slits were made with a rubber bonded silicon carbide wheel 0.006-inch thick mounted on

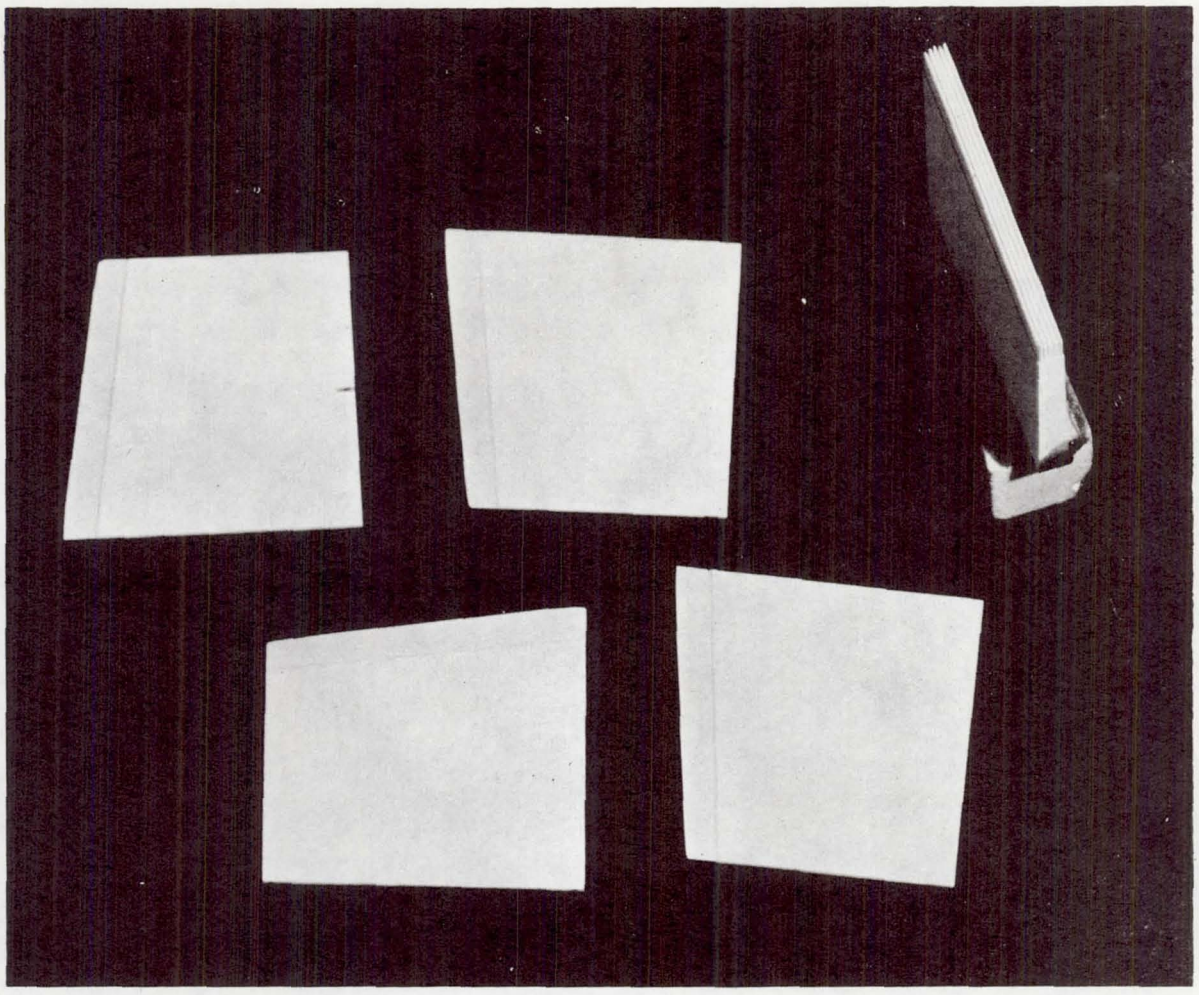


FIGURE 3. Photograph of a Cleaved Pyrolytic Boron Nitride (PBN) Block (1 x 1 x 1/4 inch)

the precision wafering machine (Micromesh Mfg. Co.). Best results were obtained without any water coolant, a feed rate of 0.1-inch per minute, and a wheel speed of 4000 rpm. Seven slits were made in a 1/8-inch-thick block approximately 0.008-inch apart.

A yield of eight wafers was expected from a 1/8-inch-thick block but generally the first two wafers cleaved did not part parallel to the major block surfaces and would break out before reaching an opposite edge. The remaining six had a variation of from 0.005- to 0.010-inch measured across the surface. The difficulties may be related to the layered

structure of pyrolytic boron nitride with respect to the major surfaces of the block.

2. Lapping and Polishing

In general, wafers were bonded to a 3- by 3-inch piece of plate glass having a lightly frosted surface to improve adhesion. A low melting point wax (Pyseal, Fisher Scientific Co.) was used as the adhesive. The glass plate was heated on a hot plate to the flow temperature of the wax ~158° F (~70° C). After applying a thin coating of wax, the preheated wafers were positioned on the plate and the excess was then squeezed out from under the wafers by applying light and uniform pressure to each individual wafer.

Controlled wafer thicknesses were achieved by cementing metal (steel) shim strips along two edges of the glass. An epoxy cement was used to permanently bond the shim strips to the glass. A series of glass plates with different thickness shims were made ranging from 2 to 10 mils. Each set of wafers were sequentially lapped by transferring them to thinner shimmed plates until the desired thickness was obtained (2 to 6 mils).

Most lapping and polishing operations were performed with a Mazur Lapping/Polishing Machine manufactured by Westinghouse Electric Corporation, Scientific Equipment Department. The machine operation is based on a variable-speed, eccentrically-rotating plate with interchangeable trays that contain different grades of abrasives. Each tray has a plate glass removable base. Lapping and polishing can be done directly on the glass plate or the plate can be covered with a variety of bonded surfacing materials. Some materials were polished with a vibratory machine (Syntron Lapping and Polishing Machine, Type LP010). The following discussion on different materials details the particular equipment and techniques that were used.

a. SAPPHIRE AND HOT-PRESSED LINDE A

The Syntron Lapping Polishing Machine was used in preparing surface polishes on sapphire wafers and hot-pressed Linde A (Al_2O_3) wafers. Two sapphire wafers, about 1-inch in diameter and from 3- to 4-mils thick, were polished on both sides and three hot-pressed Linde A wafers were similarly prepared. The polishing sequence was as follows:

1) Rough polish on a nylon lap surface impregnated with nine micron diamond powder and

sparingly lubricated with Dymo fluid.[1] Vibration amplitude was set in the range from 0.020 to 0.040 inch by adjusting the power control rheostat. The vibration amplitude varies with the number of holders placed in the bowl and is set at a level below that which causes the holders to vibrate. The holders weigh about one pound and the wafers were wax-mounted on the bottom of the holders using the methods previously discussed.

The time required to complete the rough polishing phase depended upon the area of the sample, its initial flatness, and the degree of surface roughness. About 100 hours on the machine were necessary to produce a uniform polish over the entire surface of the sapphire wafers and about 40 hours was required for the hot-pressed material.

2) Final polishing was done on a nylon lap surface with three and then one micron diamond particles. These operations required about 10 hours for each wafer. It should be noted that the machine time was essentially unattended except for an occasional inspection and application of additional lapping fluid.

b. LUCALOX

Table 3 shows a lapping and polishing sequence with the Mazur machine which was found to yield the least number of grain pullouts in Lucalox wafers. In many instances, large areas of the Lucalox wafer surfaces were free from pullouts; however, occasional grain voids were found in all wafers when their surfaces were scanned at high magnification. In general, the highest concentration of voids or pullouts were found in the central area of a wafer. Wafers that were lapped to 2 mils had voids that penetrated the entire thickness of the wafer resulting in pin holes. It appears, that 5 to 6 mils is a minimum practical thickness.

Although the measured thickness of these wafers is in the range of 5 to 6 mils their effective thickness

[1] Dymo Fluid - Elgin National Watch Company, Industrial Products Division, Elgin, Illinois.

TABLE 3. Lapping and Polishing Operations for Lucalox Wafers

Lucalox Wafers: 10 to 12 mil starting material, 3/4 inch diameter						
Operation Sequence	Abrasive	Lapping Fluid	Lap Plate Surface	No. of Wafers Per Holder and Applied Pressure	Machine(1) Speed (Dial Setting)	Comments
1	600 Grit Boron Carbide (Norton Co.)	Elgin Watch Company (Dymo)	Plate glass	6 wafers 3 lbs.	2	Lapped to ~6 mils
2	30 micron diamond (Geoscience Instrument Co.)	same	same	same	same	pre-finish 1/2 hr. each side
3	15 micron diamond	same	same	same	same	same
4	same	same	Pre K, bonded surface material (Geoscience Instrument Co.)	same	3	rough polish 1/2 hr. each side
5	6 micron diamond	same	Fine K bonded surfacing material (Geoscience Instrument Co.)	same	4	final polish 1 hr. each side
6	1 micron diamond	same	Fine K	same	4	remove scratches 1 hr. each side

(1) Mazur Lapping/Polishing Machine, Westinghouse Scientific Equipment Department

(due to large grain pullouts) is probably in the 4- to 5-mil range. In addition, surface voids would contribute to high-voltage stress concentrations during electric strength tests causing premature breakdown.

Mechanical stresses that occur during machining of brittle materials cannot be entirely eliminated but they can be minimized. Table 4 contains a listing of possible causes of grain pullouts together with appropriate corrective actions.

A procedure similar to the one described for sapphire and hot-pressed Linde A using the Syntron machine was also evaluated in an attempt to obtain pit-free and highly polished Lucalox wafers. Satisfactory results could not be obtained with this material. The only polycrystalline material that could be polished to a mirror-like finish and remain essentially free of grain pullouts and pits was the hot-pressed Linde A material. This is apparently due to significant differences in microstructure (grain size and shape).

The estimated grain size of the Lucalox used is approximately in the range from 30 to 40 microns with occasional grains as large as 70 microns. Each of the crystallites are equiaxed. Hot-pressed Linde A, however, has a distinctly different microstructure. The grains are long and slender (needle-like) with their length direction normal to the direction of hot pressing (parallel to the wafer surfaces). Grain width is about 10 to 12 microns with length-to-width ratios of about 2.5 to 4.0. A grain pullout, therefore, results in a much more shallow surface depression.

c. HOT-PRESSED BERYLLIUM OXIDE

A group of six hot-pressed BeO specimens were received from Atomics International with "as ground" or lapped surface finishes. The wafers were 0.470-inch diameter with a thickness ranging from 5 to 6 mils. These wafers had been sliced (in a direction perpendicular to the pressing axis) from a core sample taken from the center of a hot-pressed slug three inches in diameter by one inch thick. The hot-pressed slug was pressed in a graphite die from Minox AAA powder (99.85% purity). An analysis of Minox AAA (Mineral Concentrates and Chemical Co.) is given in table 2.

R. L. McKisson of Atomics International reported that the material is >99.9% dense with an average grain size

TABLE 4. Possible Causes of Grain Pull Outs in Machined Lucalox Wafers

Cause	Corrective Actions
1. a) Excessive mechanical stress as a result of wafering operations b) Surface initiated fractures due to abrasion damage c) Frictional heating	a) Improve coolant efficiency at cutting interface (higher flow rates, direct impingment of coolant at cutting surface) b) Increase cutting wheel rpm c) Decrease feed rate d) Use smaller grain size diamonds in slicing wheel e) Anneal wafers after slicing or heat and quench
2. a) Mechanical stress exceeding cohesive strength of individual crystallites during lapping and polishing operations. b) Abrasion surface damage-excessive stress concentrations at point contacts between abrasive and wafer surface c) Frictional heating-thermal stress gradients	a) Use smaller grain size abrasives for all stock removal and polishing operations b) Determine best compromise between stock removal rates, abrasive size and type, applied pressure and lap speed c) Determine if hardness of lap surface is a significant factor (glass vs. metal and cloth) d) Investigate low amplitude, high frequency lap motion
3. a) Non-uniform grain size material with a large number of excessively large grains b) High mean grain size - decreased grain boundary stresses with decreasing grain size c) Non-uniform density distribution from center to outer edges of wafer d) High internal stresses due to crystal anisotropy in expansion coefficients and elastic moduli	a) Obtain smaller mean grain size material b) Investigate hot pressed material with controlled-uniform grain size. The microstructure of hot pressed Al_2O_3 shows that the long axis of individual crystallites lie in a direction parallel to wafer surfaces. Thus, an occasional grain pull out would result in a more shallow surface depression

of 12 microns. The purity of the hot-pressed material is probably very close to the purity of the starting raw material except for any impurities that may have diffused into the charge during hot pressing. However, since the sample wafers were obtained from a core sample, this source of contamination would be minimal.

An effort was made to lap and polish these wafers to a minimum practical thickness. The techniques and equipment used are the same as those that have been described for Lucalox and sapphire wafers except as noted in the following discussion.

Two BeO wafers were wax-bonded to individual metal holders (~1 lb. each) and lapped and polished on the Syntron machine with nine micron diamond on a nylon lap surface. Periodic inspection of the wafers was made. After about 10 hours on the machine, circumferential cracks were noted at the wafer edges. Two additional wafers were selected and each wafer was gently hand-lapped on both sides with six micron diamonds on a glass plate. These wafers were then remounted on metal holders (~1 lb. each) and lapped and polished on the Syntron machine with nine micron diamonds on a nylon lap surface. One of these wafers was successfully polished (semi-polish; grain pullouts were evident) on both sides. The other wafer was polished on one side but developed circumferential cracks around its edge during polishing on the reverse side. The final thickness of the polished wafer was about three mils.

Comparing the workability of hot-pressed BeO wafers with Lucalox, hot-pressed Linde A or synthetic sapphire, indicates that BeO is mechanically weaker than the various forms of aluminum oxide and cannot be lapped and polished to thin sections much less than about 4 to 6 mils. This observation is based on similar lapping and polishing techniques used for each of these materials.

d. PYROLYTIC BORON NITRIDE

The techniques used to lap and polish pyrolytic boron nitride from "as-sliced" thicknesses ranging from 10 to 12 mils down to a final thickness in the one-mil range were continually improved during the program. During the early phases of the program, one-mil thick specimens for single-wafer capacitors were prepared as follows:

1) Reduce thickness from 10 to 12 mils to 3 to 4 mils by transferring wafers to thinner shimmed holding plates and lapping with Norton 600 grit boron carbide abrasive. (Dymo fluid - Mazur Lapping/Polishing Machine.)

2) Lap on one side of the wafer to a final thickness of about 2-1/2 mils using 15 micron diamonds on a glass lapping plate.

3) Remove wafers and remount on a plain glass holder (4- by 4-inches square, total weight two pounds - three wafers per holder). Mounting is critical to insure that all entrapped air pockets are squeezed out from under the wafers.

4) Lap and polish using six micron diamonds on Pre K lap surface until all surfaces are polished uniformly. Scratches are still visible at 100X magnification. (Polishing cloths or lap surfacing materials manufactured by Geoscience Instruments Corporation, New York City, New York.)

5) Final polish with Linde A on Fine K lap surface.

6) Reverse mount and repeat step 3 until a thickness of approximately 1-1/2 mils is achieved.

7) Repeat step 4 until a thickness of one mil is obtained.

Dymo lapping fluid was used in all the above operations. The quality of the final polished surface using Linde A (0.3 micron particle size) is good but a few very fine scratches can still be observed. The cause of these scratches is probably abrasive contamination from previous polishing and lapping operations.

Mounting of PBN wafers is a precise operation particularly after the material has been reduced to two mils in thickness. If the wafer is not mounted flat against the mounting plate or if air pockets greater than approximately 1/16 of an inch in diameter remain between the wafer and plate surface, high sections or bulges develop and the material will wear away completely or will be reduced to very thin sections when an attempt is made to achieve an overall one mil thickness. This procedure, however, was only used to prepare wafers for single layer capacitor tests.

An improved method was developed to prepare additional quantities of wafers for multi-layer capacitors. This approach has:

1) reduced rejects,
2) improved thickness uniformity,
3) reduced the depth and number of surface scratches on polished wafers,
4) simplified techniques, and
5) reduced preparation time.

One of the major improvements was the elimination of wax-bonding during the final stages of the process. Details of the method are as follows:

1) Cleaved wafers with uneven surfaces are wax-bonded to a metal holder and lapped with 400-grit alumina abrasive (Norton Co.) on a glass plate until a flat uniform surface is obtained. The wafers are reverse mounted and the opposite face is lapped until flat and uniform. Wafer thicknesses at this point range from 5 to 7 mils. This step is unnecessary for wafers that have been sliced completely through.

2) From 5 to 7 mils down to one mil, it is not necessary to bond the wafers to holding fixtures. A series of fixtures are used that have different thickness steel shim strips resistance welded to their flat sides. Each fixture consists of a solid steel disk 3 inches in diameter and 1/2- to 1-inch thick. The surfaces of these disks have previously been surface ground and then lapped flat and smooth. The shim strips are 1/2-inch wide by 12-inches long and are cut into short lengths to form a square opening slightly larger than the wafer to be lapped (approximately 1/16-inch on a side).

   These strips are then laid out on the flat surface of a steel disk and resistance welded at a number of points to the disk. A 4-mil thick shim strip, for example, forms a raised stop on the surface of the lapping fixture whose height difference is very close to four mils and uniform at all points after the cutting burrs have been lapped. In this manner, a number of lapping fixtures have been made with four, three, two, and one mil shim stops. (See Appendix A for fixture details.)

3) Starting with a 6-mil-thick, one-inch-square wafer, the wafer is first set into a 4-mil shim opening with a small amount of lapping fluid applied to the interface between the wafer and the fixture. The fixture and wafer are then carefully set on a glass lap plate (wafer side down) mounted on the Mazur Lapping/Polishing Machine. The machine is started at its slowest speed setting and the wafer is lapped (figure 8 motion) until it reaches the thickness of the raised stop (4 mils). A 400-grit size alumina abrasive plus Dymo lapping fluid is used for all lapping down to four mils. From four mils down to one mil, 10 micron alumina (S.S. White Co.) and de-ionized water are used. After a wafer is lapped to four mils, it is reset into a 3-mil fixture and the procedure is repeated until a final thickness in the one-mil range is achieved. An alternate method is to lap each wafer between a fixed and floating glass plate using five micron alumina abrasive and water. Wafers about 2-mils thick are simply laid on a large fixed glass plate with a small amount of abrasive slurry and covered with a 3- by 3-inch-square glass plate. The smaller plate is moved by hand in a figure 8 motion and periodically removed for thickness measurements (micrometer). One-inch square wafers have been lapped to thicknesses in the range from 0.4 to 1 mil with good yields (approximately 80%).

The results using this technique have been very satisfactory. One-mil wafers are flat and do not exhibit the type of camber or warping characteristic of one-mil wafers produced by the "wax-bonding method". Yield is high and the tedious and time consuming task of squeezing out air bubbles (necessary for "wax-bonding") at the wafer-holder interface is eliminated.

A matte wafer surface finish is normally produced by this method. To polish one-mil wafers an extension of the lapping techniques described above was used. The motion mechanics are the same except that 0.3 micron Linde A abrasive is used and the surface of the fixed and moving plates (three-inch diameter steel disk, one-inch

thick) are covered with Pre K polishing paper. Wafers that have been thoroughly cleaned to remove the five micron alumina abrasive are laid between the fixed and moving plate. The cover plate is rapidly moved by hand which effectively polishes both surfaces of the wafer simultaneously in approximately two to three minutes. The major advantages of this approach are a high degree of wafer flatness and an overall simplification of the polishing process compared to wax-bonding wafers to a holding plate. The elimination of organic materials (wax) during these final stages of wafer preparation facilitates the subsequent cleaning process and greatly minimizes the possibility of residual organic or carbon particles remaining on the wafers after cleaning.

3. Sputtered Electrodes

a. PRECLEANING

Most single wafer capacitors were prepared with sputtered platinum -20% rhodium alloy electrodes. Sputtering details will be outlined in the next section; however, prior to sputtering the following wafer cleaning sequence was used:

1) Remove mounting wax by boiling in trichloroethylene for five minutes followed by 30 second ultrasonic agitation.[2] Rinse three times with clean trichloroethylene with 30 second ultrasonic agitation during each rinse.

2) Rinse three times with clean methyl alcohol.

3) Rinse three times with clean acetone.

4) Dry-boil in Alconox solution (1 gram per 250 ml of de-ionized water) followed by 30 second ultrasonic agitation.

[2] Ultrasonic agitation not used for one mil pyrolytic boron nitride.

5) Pour off Alconox solution and rinse in flowing demineralized water for 30 minutes (Barnstead Demineralizer Cartridge, Mixed Resin Type).

6) Pour off water and rinse with six washes of clean acetone.

7) After cleaning, wafers are heated in air (platinum crucible) to 1112° to 1290° F (600° to 700° C) for 20 minutes.[3]

8) Soak cooled wafers in hot 140° to 156° F (60° to 70° C) concentrated HF for about 10 minutes.

9) Rinse in flowing de-ionized water for 10 minutes followed by three clean rinses in methyl alcohol and three clean rinses in acetone.

10) Clean in vapors of isopropyl alcohol and dry at 302° F (150° C) before loading into sputtering masks.

Fisher spectranalyzed methanol, acetone, and reagent grade trichloroethylene were used. The lot analysis for each of these solvents is shown in table 5.

b. TRIODE SPUTTERING METHODS

The fixturing used to sputter alloy electrodes of 20 percent rhodium, 80 percent platinum, and pure noble metals on a capacitor wafer is shown in figure 4. This assembly is located within an 18-inch diameter glass bell jar. All the essential parts and their functions are identified in figure 4.

The sputtering power supply, necessary feedthroughs, and accessory items comprise the AST-100 Low Energy Sputtering Unit manufactured by Consolidated Vacuum Corporation. The bell jar is evacuated by a CV-18 pumping system made by the same company.

This unit is equipped as follows:

1) Six-inch diffusion pump (Convalex 10 fluid)
2) Liquid nitrogen baffle (BCN-61A)

[3] Steps 7, 8 and 9 used for pyrolytic boron nitride only.

TABLE 5. Lot Analysis of Fisher Spectranalyzed Solvents Used to Clean Capacitor Wafers

Acetone	**Lot #750564**
Density (g/ml)	0.7853
Boiling range	56.0-56.3°C
Residue after evaporation	0.000%
Acidity (as CH_3COOH)	0.002%
Alkalinity (as NH_3)	0.000%
Aldehyde (as HCHO)	Pass Test
Methanol (as CH OH)	0.05%
Substances reducing permanganate	Pass Test
Trichlorethylene	**Lot #750063**
Boiling range	86.7-86.9°C
Specific gravity at 25/25 C	1.460
Residue on evaporation	0.0001%
Acidity (as HC1)	None
Alkalinity (as NaOH)	0.000%
Heavy metals (Pb)	0.000005%
Free Halogens	None
Methanol	**Lot #75047**
Water H_2O	0.05%
Boiling range	64.5-64.8°C
Residue after evaporation	0.0001%
Acetone, aldehydes	0.000%
Acidity (as HCOOH)	0.002%
Alkalinity (as NH_3)	0.0001%

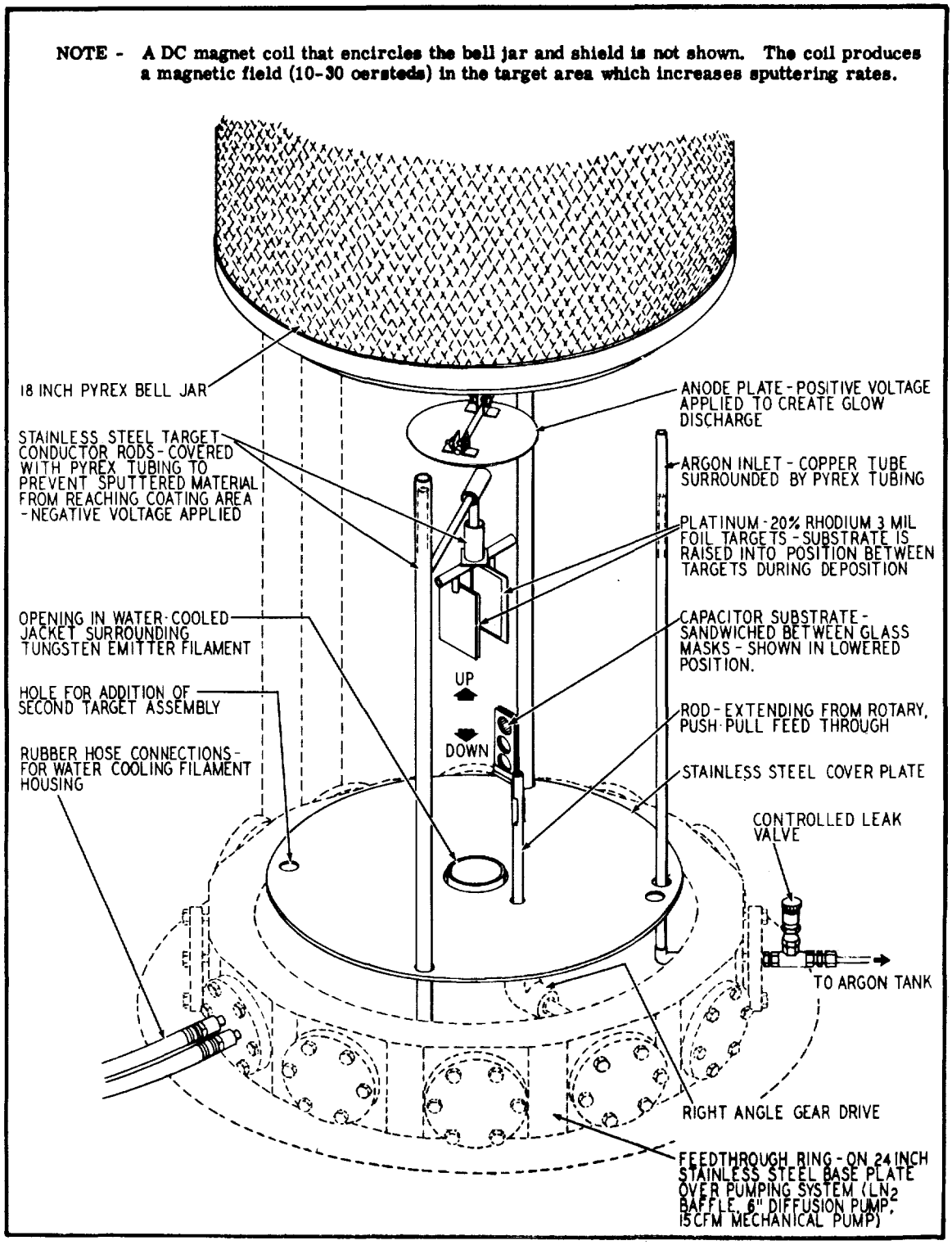


FIGURE 4. Three Element Sputtering Assembly and Associated Fixturings

3) Welch 15 cfm mechanical pump

4) Pirani gauge, 2 station (GP 145)

5) Ionization gauge (Gic-110A)

6) Two push-pull rotary seals

7) Work heater power supply and a 2-kVA filament power supply.

8) Twenty-four inch diameter stainless steel baseplate with a variety of feedthrough seals.

The capacitor substrate (wafer) is located between two glass microscope slides that have coincident holes ultrasonically drilled into each slide to mask off a small margin (approximately 0.025-inch around the circumference of the disk). The major area of the disk is exposed on both surfaces to the bombarding metal atoms sputtered from the target. Aluminum clips are used to clamp the two glass slides together and hold the capacitor wafer in proper orientation with respect to the holes in the glass. Ordinary soda-lime glass microscope slides have been used for masks, as well as alkali-free glass (Corning 7059), and pyrolytic boron nitride to minimize any possible contamination from impurities that may be sputtered from the masks.

The AST-100 sputtering system is a three element unit as compared to a conventional two element sputtering geometry using only a cathode and anode. In the conventional system, the cathode must perform a dual function by providing a source of electrons to maintain a glow discharge or plasma as well as providing a source of material which is to be deposited on the substrate. The AST-100 system uses a separate hot-filament electron source for gas ionization at pressures as low as 5×10^{-4} torr and separate ion targets to provide the source material for deposition. The major advantages of the latter system are:

1) Control: Over deposited dimensions and composition.

2) Flexibility: A wide range of materials can be deposited and variety of targets and substrate geometries can be used.

3) Adherence: Improved film adherence is obtained because of the higher arrival energy

of sputtered atoms and a capability to pre-clean the substrate in a glow discharge prior to deposition.

The general sputtering process used to deposit platinum and platinum-rhodium alloy electrodes on PBN wafers is as follows:

1) Register substrate between glass mask, clamp, and position substrate holder on rotary, push-pull feedthrough arm as shown in figure 4.

2) Evacuate bell jar to 5×10^{-7} torr with a CV-18 pumping system.

3) Activate tungsten filament (~49 amperes)

4) Back-fill bell jar with pure argon and adjust chamber pressure to approximately three microns. (Argon analysis: less than 10 ppm of oxygen, 5 ppm of hydrogen, 40 ppm nitrogen and a dew point of < -80° F.)

5) Set anode voltage control to ~70 percent full scale.

6) Turn on anode switch and adjust anode current to 3.5 amperes. A glow discharge will appear. The discharge phase is maintained for about 50 minutes to clean the target and substrate surfaces.

7) With the substrate in a lowered position (as shown in figure 4) apply voltage to the target to sputter clean the target surfaces (~15 minutes).

8) Raise substrate-mask assembly as shown by the arrows in figure 4 so that the substrate is positioned equidistant (~3/4 inch) from each target face. Voltage is then reapplied to the target. During the sputtering phase, the magnet coil is energized to achieve a higher plasma density (increased deposition rate).

4. Preliminary Capacitor Evaluation

A series of preliminary tests were performed on PBN wafers, aluminum and beryllium oxide wafers, and single wafer capacitors to determine some of the characteristics of these materials prior to conducting more extensive tests in vacuum.

Electrical test equipment used for capacitance, tan δ, and d-c resistance measurements are discussed in the next section. Complete processing details for all test capacitors are shown in table 6. Included are:

a) capacitor dimensions (wafer diameter, thickness, and electrode diameter),

b) surface finish, and

c) sputtering data.

Single wafer capacitors are identified in table 6 and in subsequent data discussion as PBN capacitor No. 2, sapphire No. 1 etc.

a. PYROLYTIC BORON NITRIDE

(1) Thermal Shock and Microstructure

The first single layer capacitor made from pyrolytic boron nitride was coated with sputtered pure platinum (99.9 percent) electrodes for preliminary evaluation. The electrode diameter was 0.383 inches. Electrodes were sputtered onto a 1/2-inch wide strip of lapped and polished pyrolytic boron nitride that varied in thickness from 1-1/4 to 1-1/2 mils (micrometer measurement). A calculated average thickness of 1.12 mils was obtained based on the measured capacitance at 1 kc/sec, the electrode diameter and a dielectric constant of 3.4 using the formula:

$$T = \frac{KA}{4.45\ C}$$

where:

T = thickness (inches)
K = dielectric constant
A = electrode area (inches^2)
C = measured capacitance (picofarads)

Table 7 shows the measured capacitance and dissipation factor at 1 kc/sec. Also shown are the results of a d-c resistance measurement and voltage test made before and after thermal cycling. As noted, the capacitor appeared to be unaffected by thermal cycling in air to 1100° F, both physically and electrically. Table 8 shows capacitance and dissipation factor measurements made as a function of frequency (50 cps to 10 kc/sec) for

PBN capacitor No. 2. This capacitor was also examined under a microscope and photomicrographs were made of a selected area on the surface (figure 5). A small circular crack can be seen near the edge of the capacitor wafer (electrode margin area). This crack is coincident with a nodular growth pattern that was found to be characteristic of the microstructure of pyrolytic boron nitride. This particular nodule is approximately 0.055 inch in diameter. Further examination of the area at higher magnification (200X) showed that the crack extends completely through the dielectric and might be considered analogous to a knot hole in a piece of wood. It was not possible to determine if this crack existed at the time the electrodes were applied or if it occurred during subsequent handling. It appears, however, that this crack could account for the erratic changes in capacitance and dissipation factor observed at elevated temperatures (figure 8) and discussed later in this section.

These results prompted a further study of the microstructure of pyrolytic boron nitride. Several one-mil thick wafers of pyrolytic boron nitride were examined with transmitted light. These photomicrographs are shown in figure 6. A nodular pattern can be seen with an average nodule diameter of about 0.015-inch. An occasional, larger diameter nodule was found with diameters ranging from 0.050-to 0.060-inch. It was apparently one of these larger nodules that caused the defect observed in PBN capacitor No. 2.

The larger nodules were not a problem with later PBN capacitors as long as precautions were taken to eliminate relief polishing. Relief polishing was minimized or eliminated by using a low-nap polishing cloth.

The nodule diameter increases at greater distances from the deposition substrate. This effect has been observed by L. F. Coffin, Jr. (ref. 1) in pyrolytic graphite. Large nodules in pyrolytic graphite are reported to originate from nucleation centers around foreign particles or surface irregularities on the deposition substrate. These nodules grow outward from the substrate in a conical shape.

TABLE 6. Complete History of

Group No.	Substrate Wafer Material	Capacitor Materials, Dimensions, Electrical Tests					Electrode	Electrode Diameter
		Substrate Surface Finish	Substrate Dimensions	Capacitor Test Designation Number	Electrical Tests Performed at 7×10^{-8} to 4×10^{-7} torr	Other Tests		
1	Pyrolytic Boron Nitride (Boralloy)	Polished	0.750" dia. ~ 1.1 mils thick	BN capacitor No. 2	3 Test Runs: RT to 1100°F, Tan δ & capacitance versus temperature & frequency	Microstructure	PT-20%Rh 99.9% purity	0.683"
2	Sapphire - Single Crystal Al_2O_3 (Linde Co.)	Polished	~ 1.0" dia. 3.25 mils thick (0.383" electrode dia.)	Sapphire capacitor No. 1	2 Test Runs: RT to 1100°F, Tan δ & capacitance versus temperature & frequency: Breakdown voltage at 1100°F	Heat treat in air at 1652°F (900°C) before electrical tests in vacuum	PT-20%Rh 99.9% purity	0.383"
3	Sapphire - Single Crystal Al_2O_3 (Linde Co.)	Polished	~ 1.1" dia. 3.2 mils thick (0.683" electrode dia.)	Sapphire capacitor No. 2	1 Test Run: RT to 1100°F, Tan δ & capacitance versus temperature & frequency & d-c resistance	----	PT-20%Rh 99.9% purity	0.683"
4	Beryllium Oxide - Hot Pressed (Atomics International)	Semi-polished	0.470" dia. ~ 3.0 mils thick	BeO capacitor No. 1	1 Test Run: RT to 1100°F, Tan δ & capacitance versus temperature & frequency	----	PT-20%Rh 99.9% purity	0.383"
5	Beryllium Oxide - Hot Pressed (Atomics International)	As Lapped	0.470" dia. ~ 4.5 mils thick	BeO capacitor No. 2	2 Test Runs: RT to 1100°F, Tan δ, capacitance, d-c resistance & d-c voltage breakdown at 1100°F	Heat treat in air at 1760°F (960°C)	PT-20%Rh 99.9% purity	0.383"
	Pyrolytic Boron Nitride (Boralloy)	As Lapped (Matte)	0.750" dia. ~ 1.0 mils thick	Tabbed BN capacitor No. 2	No measurement made	Heat to 1100°F in vacuum, RT electrical measurements		0.683"
6	Lucalox-Poly-crystalline Al_2O_3 (General Electric Co.)	As Lapped	0.750" dia. 5 mils thick	Lucalox capacitor No. 1	1 Test Run: RT to 1100°F, Tan δ, capacitance, d-c resistance	Heat treat in air at 1652°F (900°C)	PT-20%Rh 99.9% purity	0.683"
	Pyrolytic Boron Nitride (Boralloy)	Polished	0.750" dia. ~ 0.7 mils thick	Tabbed BN capacitor No. 1	No measurement made	RT, Tan δ & capacitance		
7	Lucalox-Poly-crystalline Al_2O_3 (General Electric Co.)	Semi-polished	0.750" dia. ~ 5 mils thick	None	None	Electrode adherence	PT-20%Rh top layer & titanium base layer	0.383"
	Pyrolytic Boron Nitride (Boralloy)	Polished	0.750" dia. ~ 1.5 mils thick	None	None	Electrode adherence		0.383"
8	Sapphire Single Crystal Al_2O_3 (Linde Co.)	Polished	Broken piece 3 mils thick	None	None	Electrode adherence	PT-20%Rh top layer & tungsten base layer	0.200"
	Pyrolytic Boron Nitride (Boralloy)	Polished	0.750" dia. ~ 1.0 mils thick	BN capacitor No. 3	DC voltage breakdown at 1100°F, d-c resistance	Electrode adherence		0.383"

Each Capacitor Fabricated and Tested

Sputtered Electrodes - Process History					Sputtering Data			
Substrate Mask	Target Geometry	Target to Substrate Distance	System Pressure Before Backfill	Glow Discharge Cleaning Time	Target Voltage	Time On (minutes)	Anode	Magnet (amps)
Glass microscope slides 1" x 3" (Corning Brand)	Rectangular: 1-1/2" x 3"	3/4"	4×10^{-7} torr	53 min. at 4 to 0.5 microns argon pressure	900 V at 60 ma	35	34 V. at 3.6 amps	3
Glass microscope slides 1" x 3" (Corning Brand)	Rectangular: 1-1/2" x 3"	3/4"	4.5×10^{-7} torr	58 min. at 4 to 1 micron argon pressure	700 V. at 70 ma	9	35 V. at 3.5 amps	1.3
Pyrolytic BN mask clamped with 7059 glass (Corning) & SS screws	Rectangular: 1-1/2" x 3"	3/4"	3×10^{-7} torr	57 min. at 4.8 to 0.2 micron argon pressure	600 V. at 68 ma	6	47 V. at 3.5 amps	1.0
Pyrolytic BN mask clamped with 7059 glass (Corning) & SS screws	Rectangular: 1-1/2" x 3"	3/4"	4.5×10^{-7} torr	82 min. at 5 to 0.3 micron argon pressure	600 V. at 65 ma	15	53 V. at 3.5 amps	1.1
Pyrolytic BN mask clamped with 7059 glass (Corning) & SS screws Corning 7059 glass 2" x 3"	Rectangular: 1-1/2" x 3"	3/4	5.6×10^{-7} torr	55 min. at 5 to 0.5 micron argon pressure	700 V. at 50-70 ma	10	45 V. at 4 amps	1
Corning 7059 glass 2" x 3". Clamped with SS screws	Rectangular: 1-1/2" x 3"	3/4"	7×10^{-7} torr	81 min. at 5 to 0.5 micron argon pressure	700 V. at 50-70 ma	11	49 V. at 36 amps	1.3
Corning 7059 glass 2" x 3".	1-1/2" x 3" PT-20%Rh (Target No. 2)	3/4"	4.6×10^{-7} torr	62 min. at 1 to 0.5 micron argon pressure	500 V. at 26 to 31 ma (Target No. 2)	10	42 V. at 3.5 amps	1.4
Pyrolytic BN	2" x 3" Titanium (Target No. 1)	1-1/4"			500 V. at 70 to 80 ma (Target No. 1)	10		
Corning 7059 glass 2" x 3"	1-1/2" x 3" PT-20%Rh (Target No. 2)	3/4	1.4×10^{-7} torr	43 min. at 10 to 0.5 micron argon pressure	600 V. at 35 ma (Target No. 2)	7	47 V. at 3.5 amps	2
	0.060" dia. tungsten wire spiral (Target No. 1)	1-1/4" (No. 2)			600 V. at 60 ma (Target No. 1)	5		

TABLE 7. Preparation and Evaluation of Pyrolytic Boron Nitride Capacitor No. 1

Sample	Preparation	Capacitance at 1 kc/sec Room Temperature[a]	Dissipation at 1 kc/sec Room Temperature[a]	Insulation Resistance at 500V d-c, Room Temperature[b]	Voltage Test	Thermal Cycling	Remarks
Pyrolytic Boron Nitride Capacitor No. 1	1) Sliced wafer from 1 x 1 x 1/8 inch block[d]	78.56 pF	0.000298	10^{15} ohms	Withstood 1000V d-c before and after thermal cycling (4 complete cycles)	1) Sample placed in cold furnace on thin Al_2O_3 slab-heated to 1100°F (>1000°F/Hr)	No evidence of electrode agglomeration or lifting from substrate after thermal cycling (800X magnification)
	2) Lapped to approximately 1.5 mil					2) Withdrawn from hot furnace-cooled (> 4000°F/Hr)	
	3) Cleaned					3) Inserted into 1100°F furnace - withdrawn (> 2000°F/Hr)	
	4) Sputtered platinum[c] electrodes in argon partial pressure. Electrode diameter 0.383 inch					4) Repeat 3, two additional cycles (4 complete cycles)	

(a) - Capacitance and dissipation factor measured with a General Radio Type 1620-A Capacitance Measuring Assembly (Digital Readout)
(b) - Insulation resistance measured with a Keithley Multi-Range Electrometer, Model 610B
(c) - Platinum foil target, Englehard Industries, 99.9% Purity
(d) - "Boralloy" Pyrolytic Boron Nitride, High Temperature Materials, Inc., Lowell, Mass.

TABLE 8. Pyrolytic Boron Nitride Capacitor No. 2 - Capacitance and Dissipation Factor Versus Frequency[a] At Room Temperature

Frequency	Capacitance - pF (picofarads)	Dissipation Factor (tan δ)
50 cps	263.720	0.000130
60 cps	263.791	0.000582
100 cps	263.684	0.000267
120 cps	263.701	0.000320
200 cps	263.701	0.000443
500 cps	263.647	0.000412
1 kc/sec	263.609	0.000440
5 kc/sec	263.513	0.000450
10 kc/sec	263.628	0.000440

(a) All measurements made on a General Radio Type 1620-A Capacitance Measuring Assembly - no corrections made for capacitance of jig ($\sim 1 pF$)

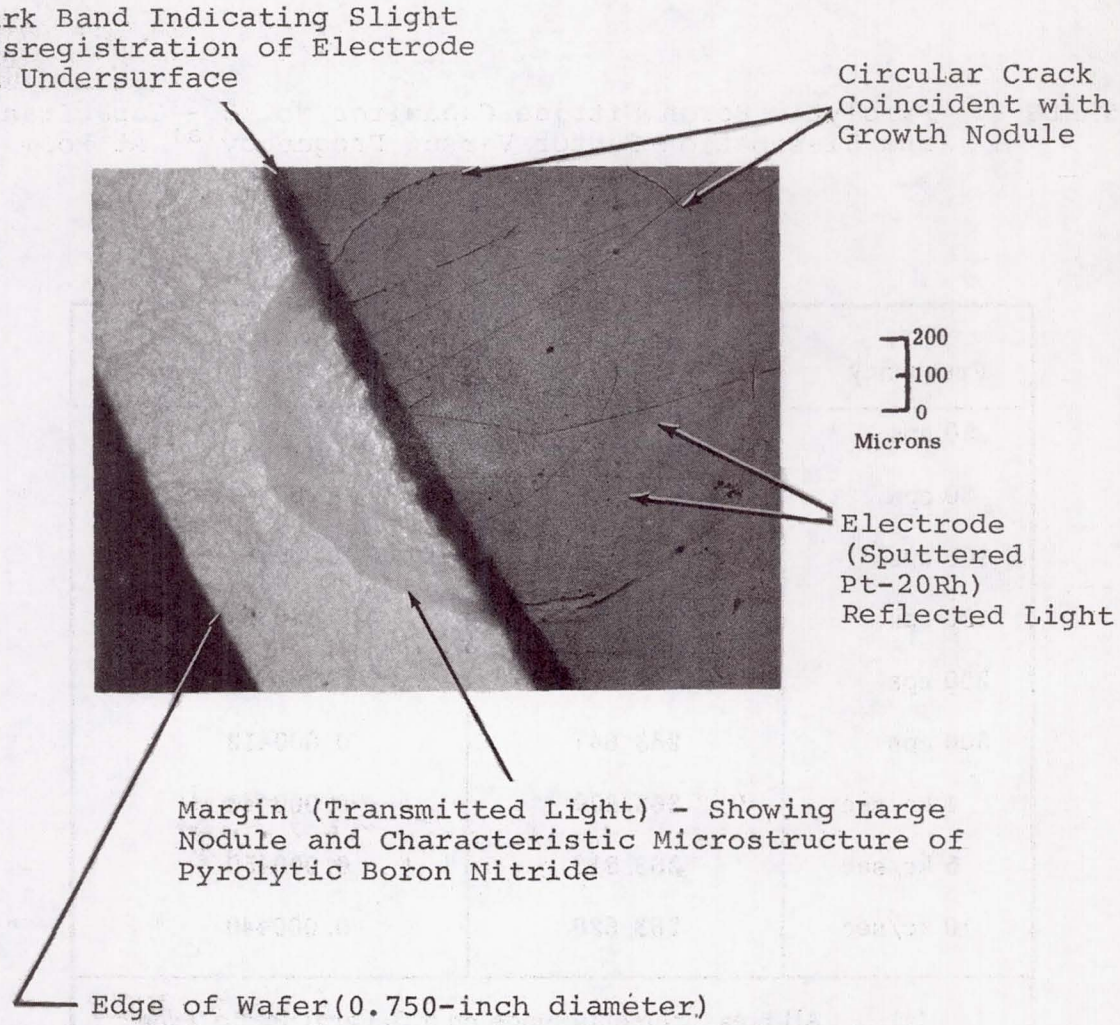
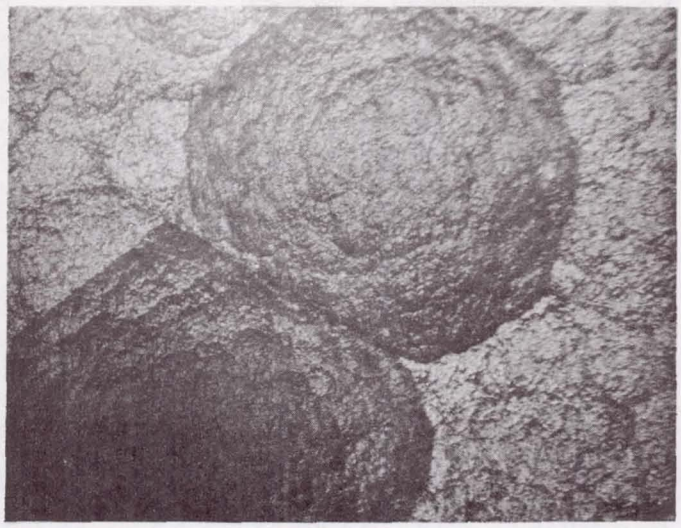
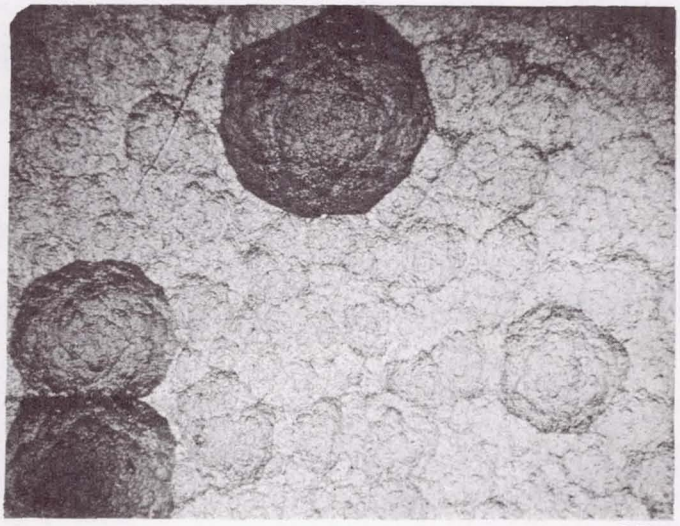


FIGURE 5. Photomicrograph of the Surface of Pyrolytic Boron Nitride Capacitor No. 2 Using a Combination of Transmitted and Reflected Light, 50X



50X



25X

FIGURE 6. Typical Microstructure (with Transmitted Light) of Thin (~0.001 Inch) Pyrolytic Boron Nitride Polished Wafers at Two Different Magnifications

(2) DC Breakdown Voltage at Room Temperature

Following the thermal cycling test, the d-c voltage breakdown strength of PBN capacitor No. 1[4] was determined. The test was performed at room temperature with the capacitor immersed in Dow Corning Electronic Grade Silicone Oil. Voltage was increased at a rate of about 500 volts per second to 7000 volts and held at this level for five minutes. The voltage was then increased until breakdown occurred. At 13,000 volts the power supply (DC Power Supply, Model PSP 30-5, Research-Cottrell, Inc., Electronics Division, Bound Brook, New Jersey) relay tripped indicating a short circuit or a current flow in excess of 10 milliamperes. No indication of leakage current was detectable on the power supply milliammeter at any voltage level up to 13,000 volts. After resetting the power supply relay, voltage could be reapplied with no leakage current indication until 13,000 volts was reached. At this voltage level the dielectric punctured premanently.

Examination of the capacitor electrodes showed several areas where the platinum had vaporized. A section near the center of the capacitor was blackened and a hole was visible. The volts per mil breakdown voltage was calculated at 10,400 (4.1 by 10^{-6} volts/cm) based on the minimum measured thickness. This value in terms of volts per mil or volts per cm is about 2-1/2 times higher than the value reported for thicker pyrolytic boron nitride of same vendor and purity (10 to 20 mils thick, table 1).

[4] PBN Capacitor No. 1 has no tabs and is not the same capacitor identified as tabbed BN Capacitor No. 1 in group 6, table 6.

b. EFFECTS OF DIFFERENT PROCESS CONDITIONS

(1) Post Electrode Deposition Heat Treatment

Three hot-pressed, Al_2O_3, Linde A wafers (0.416-inch diameter) were made with platinum -20% rhodium alloy electrodes. The capacitance and dissipation factor of these capacitors were measured immediately after applying electrodes. Abnormally high values of dissipation factor was noted for capacitors No. 1 and No. 2. It was found that by heating these capacitors in air to temperatures of 1472° to 2012° F (800° to 1100° C), a substantial improvement in the room temperature losses could be obtained. Previous history and the electrical properties of these units before and after heat treatment is shown in table 9. Capacitors No. 2 and 3 were processed using the same methods and masking material. The essential differences in the methods used to sputter electrodes on capacitor No. 1 versus No. 2 and No. 3 are as follows:

a) Glass masks (microscope slides) were used for capacitor No. 1 and PBN masks were used for capacitors No. 2 and No. 3.

b) Capacitor No. 1 received no bake-out treatment whereas capacitors No. 2 and No. 3 were preheated to 482° F (250° C) for 20 minutes at 3×10^{-7} torr prior to backfilling the sputtering chamber with pure argon.

c) Glow discharge cleaning was maintained for 50 minutes for capacitors No. 2 and No. 3 versus only 25 minutes for capacitor No. 1.

It had been expected that the treatment received by capacitors No. 2 and No. 3 prior to sputtering would result in better electrode adherence, cleaner margin areas and improved electrical properties. Dissipation factor measurements made before heat treatment indicate that some improvement was obtained (compare capacitor No. 1 with No. 2 and No. 3 of table 9). However, the heat treatment process performed after the electrodes were applied resulted in the greatest reduction in dissipation factor for all three capacitors.

TABLE 9. Effect of Post Electrode Deposition Heat Treatment on Hot-Pressed Alumina (Linde A) Capacitors

Group	Capacitor Number	Wafer & Electrode Dimensions	Cleaning and Deposition Procedure	Heat Treatment	Capacitance and Dissipation Factor @ 1 kc/sec, Room Temperature			
					Before Heat Treat		After Heat Treat	
					Capacitance	Dissipation Factor	Capacitance	Dissipation Factor
A	1	Wafer: 0.416 in. dia. 0.004 in. thick Electrode: 0.366 in. dia. Pt-20Rh	Glass mask No preheat in vacuum Glow discharge clean for 25 minutes Electrodes sputtered for 15 minutes at 600V	2012°F (1100°C) in air - Pt foil holder	73.636 pF	0.00440	69.567 pF	0.00025
B	2	Wafer: 0.416 in. dia. 0.004 in. thick Electrode: 0.377 in. dia. Pt-20Rh	Pyrolytic BN Mask Pre-heat wafers to 250°C at 3×10^{-7} torr 20 minutes hold Glow discharge clean for 50 minutes Electrodes sputtered for 10 minutes at 900V	1562°F (850°C) in air - Pt foil holder	71.426 pF	0.00119	70.879 pF	0.00022
	3	Wafer: 0.416 in. dia. 0.005 in. thick Electrode: 0.377 in. dia. Pt-20Rh	Pyrolytic BN Mask Pre-heat wafers to 250°C at 3×10^{-7} torr 20 minutes hold Glow discharge clean for 50 minutes Electrodes sputtered for 10 minutes at 900V	1562°F (850°C) in air - Pt foil holder	58.130 pF	0.00055	58.035 pF	0.00013

(2) Sputtered Electrode Adherence

The adherence of sputtered electrodes has generally proven to be satisfactory. However, when a pointed steel scribe is run across the electrode surface the metal is sometimes separated from the substrate under the scribe line (100X magnification). Using this basis of comparison for electrode adherence, the following process variations were investigated:

(a) Post Electrode Deposition Heat Treatment in Air

No definite effect was observed for Pt-20% Rh electrodes on pyrolytic boron nitride after heating in air in the 1112° F (600° C) temperature range. Since the hardness of pyrolytic boron nitride is only two on the Mohs scale, the scribe penetrates the substrate surface as well as the metal electrode making a comparison difficult.

A definite improvement in electrode adherence was observed after wafers of sapphire, Lucalox, and hot-pressed BeO were heated in air in the 1172° to 1832° F (800° to 1000° C) temperature range. Table 3 lists the capacitors that were heat treated in this manner following electrode deposition. The most important effect observed is the change in electrical properties which are discussed later.

(b) Sputtered Active Metal Base Layer

A sapphire wafer and a PBN wafer were prepared with multi-layered electrodes consisting of a thin-base coating of sputtered tungsten overcoated with Pt-20% Rh. The scribe tests showed no difference in adherence for pyrolytic boron nitride; however, the adherence of the electrodes on the sapphire wafer appeared to be significantly improved over Pt-20% Rh electrodes without the tungsten base layer. Sputtering process conditions are shown in table 6 under group 8.

Titanium was sputtered on a Lucalox and a PBN wafer followed by an overcoating of Pt-20% Rh. Again, the adherence was apparently unchanged on the PBN substrate but was

improved on Lucalox. Refer to group 7 under table 6 for sputtering details.

The preparation and evaluation of these multilayered electrodes has only been preliminary and the effect on electrical properties is inconclusive. In general, however, it appears that titanium and tungsten have little or no effect in promoting adherence between noble metals and pyrolytic boron nitride under the conditions evaluated. The bond between Pt-Rh and metal oxide type substrates is improved probably because the interface energy is lowered by the formation of an oxide transition zone at the substrate and titanium or tungsten interface.

C. CAPACITANCE AND TAN δ VERSUS TEMPERATURE TO 1100° F

1. Test Apparatus and Methods

All capacitance and dissipation factor (tan δ) measurements were made using a three terminal coaxial connection technique as described in section 3.7.3 and 4.2.2 of the General Radio Operation Instruction Manual for the type 1620-A Capacitance Measuring Assembly (Form 1615-A-0100-C, 1D887, April 1966). The assembly consists of a Type 1615-A capacitance bridge with six digit capacitance readout and four digit dissipation factor readout, a Type 1311-A Audio Oscillator, and a Type 1232-A tuned amplifier and null detector.

Elevated-temperature measurements in vacuum were made in a small resistance heated furnace insulated with tantalum radiation shields. Figure 7 shows a cut away view of the test furnace which was designed to be used within the same glass bell jar system used for sputtering electrodes. The capacitor is placed on top of a columbium disk as shown in figure 7. Several trial runs were made without a test sample in the furnace to outgas the parts. A d-c power supply was used to energize the furnace winding since it was believed that there would be less 60 cycle interference during capacitance measurements. There appears to be no difficulty in achieving a consistent vacuum level in the low 10^{-7} torr range when the furnace is at 1100° F.

D-C resistance measurements were made with a Keithly Model 610B Electrometer and a Keithly Model 240 Regulated D-C Power Supply. The d-c resistance of the test furnace insulators (less test specimen) was measured at 1000 Vd-c in vacuum (3×10^{-7} torr) up to 1100° F and found to be in the range 10^{17} to 10^{14} ohms from 72° to 1100° F. Test methods used to measure d-c breakdown voltages are described in detail in a later section of this report.

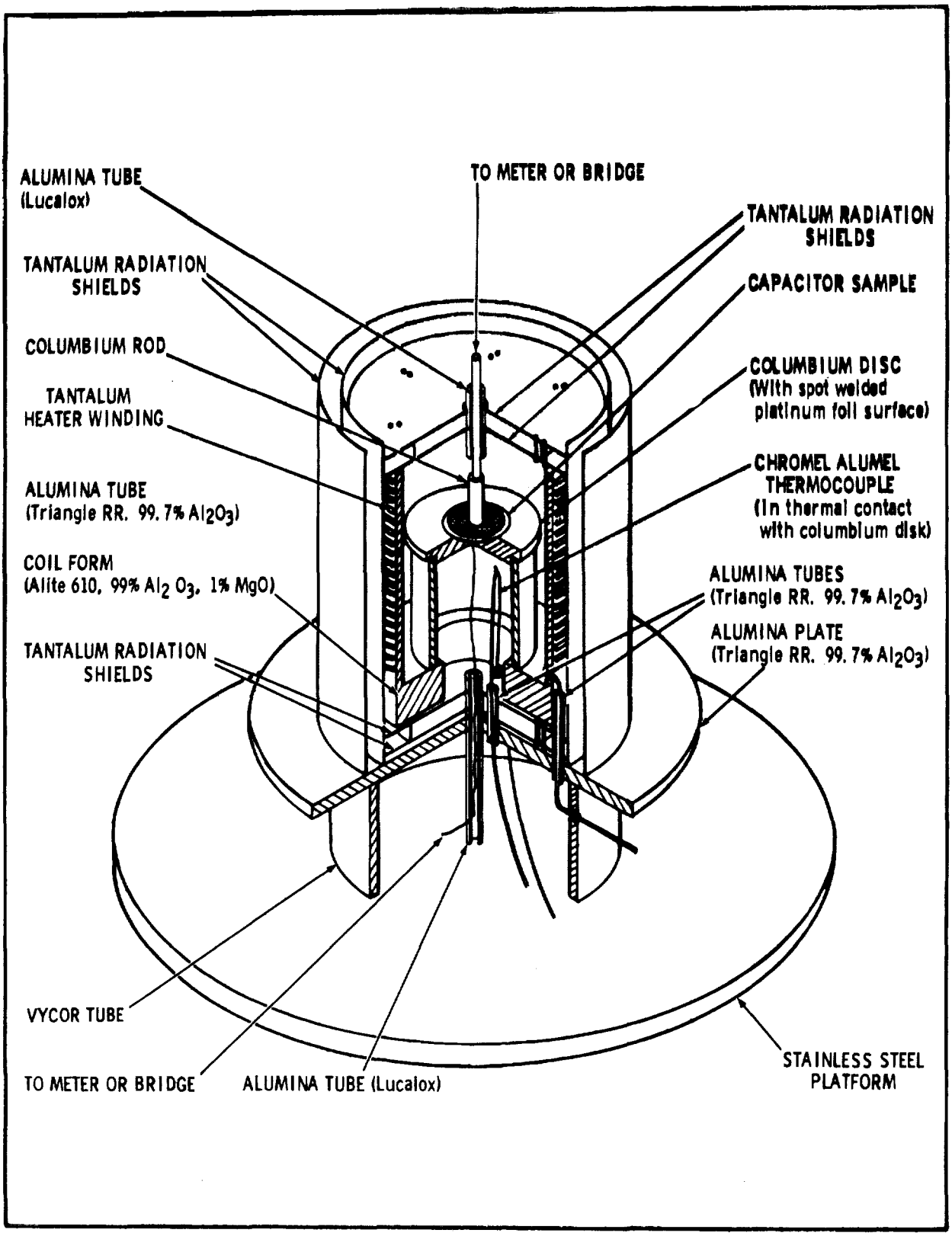


FIGURE 7. Cutaway View of 1100°F Vacuum Furnace Constructed for Electrical Testing of Single Layer Capacitors

2. Discussion of Results

a. PYROLYTIC BORON NITRIDE CAPACITORS

Figure 8 shows capacitance and dissipation factor (tan δ) for PBN capacitor No. 2 versus temperature in vacuum. It is apparent that the dissipation factor remains essentially unchanged from its room temperature value up to about 600° F and then gradually increases up to 850° F. From 850° to 1100° F the dissipation factor increases at a faster rate. The capacitance value decreases uniformly with increasing temperature up to approximately 750° F. Above this temperature the capacitance increases slightly and then begins to decrease again.

It was believed that these deviations from linearity were not characteristic of the dielectric material. Therefore, the capacitor wafer was carefully examined under a microscope. Cracks at the periphery of the "nodules" were suspected as the cause for the deviation as mentioned previously and shown in figure 5. These cracks may have developed during the test (figure 8) and are responsible for the erratic behavior in electrical properties particularly above 900° F.

Figure 9 shows the capacitance and dissipation factor change with temperature of the same capacitor wafer after it had been examined and the defective area removed (about 40 percent of the effective dielectric area) with an air-abrader (S.S. White Industrial Airbrasive Unit, Model F). It is apparent that the dissipation factor measured at elevated temperatures was not improved by the process. The increased losses are probably due to mechanical damage and possible contamination of the margin area.

The negative value of the ratio of $\Delta C/C_{72}$° F x 100 (~1.7%) for pyrolytic boron nitride at 1100° F is very close to the value that would be expected from the decrease in capacitance due entirely to thermal expansion because pyrolytic boron nitride has a reported thermal expansion ($\Delta L/L$ in/in) at 1100°F of 0.020 (2%) measured in the "c" direction from 32° to 1100° F. Since capacitance is inversely proportional to thickness, the correlation is very good.

These results are consistent with the extremely low impurity level reported for pyrolytic boron nitride (table 2). An ideal dielectric would show no change in dielectric constant or capacitance with temperature. If the dielectric contains impurities, they can act as

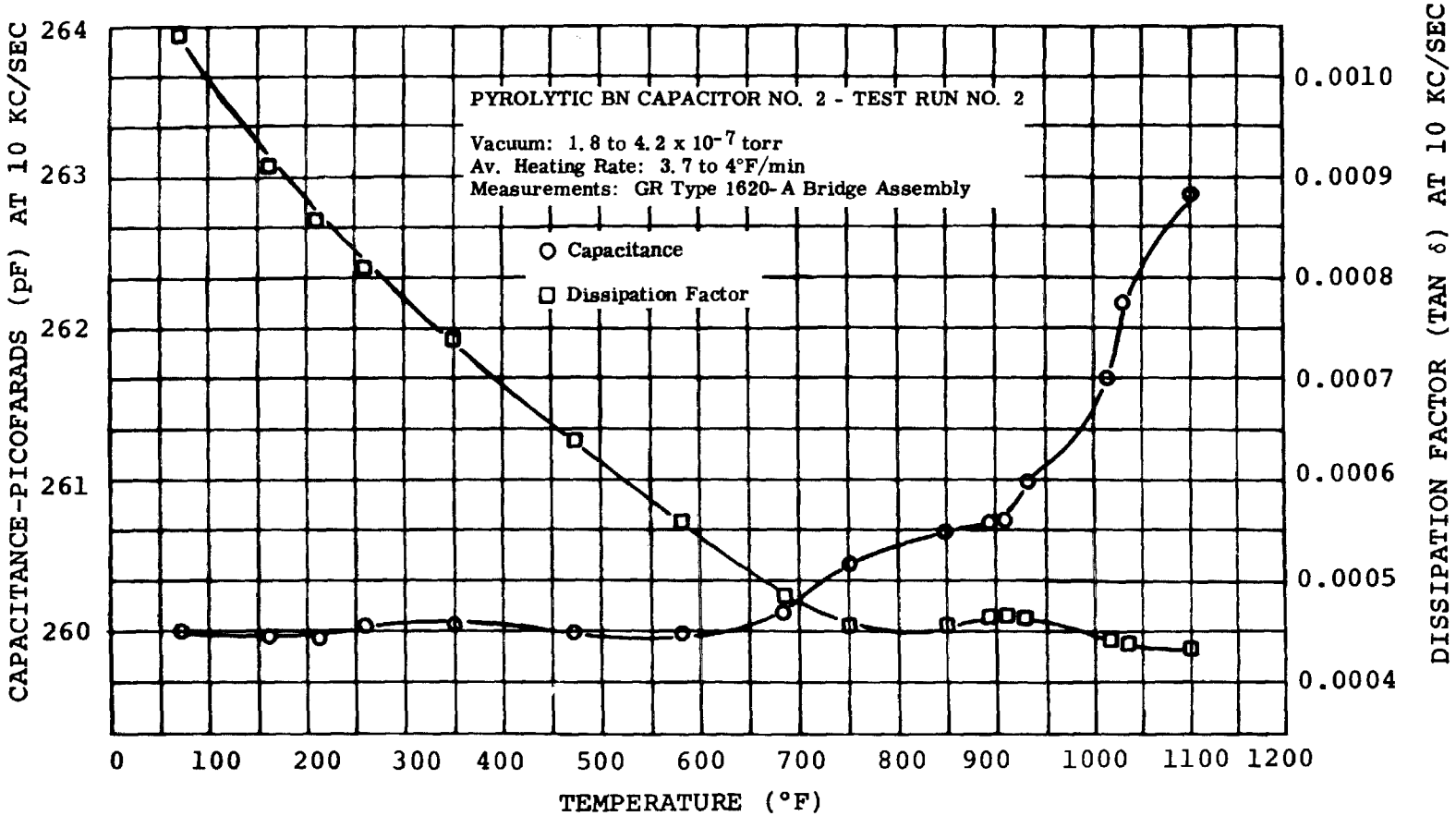


Figure 8. Capacitance and Dissipation Factor Versus Temperature of Pyrolytic Boron Nitride Capacitor No. 2

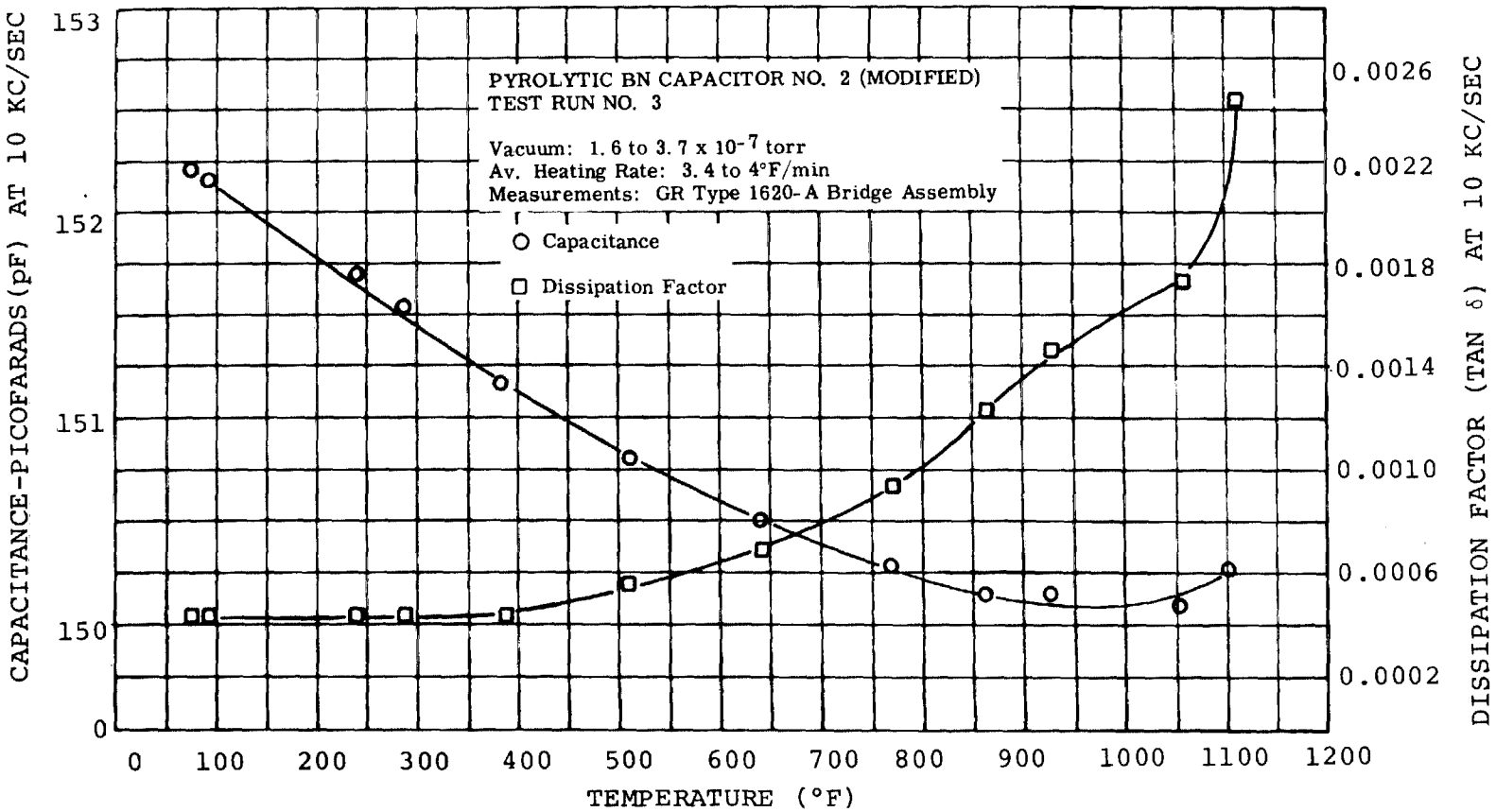


Figure 9. Capacitance and Dissipation Factor Versus Temperature of Pyrolytic Boron Nitride Capacitor No. 2 (modified)

charge carriers and increase the polarizability (measured dielectric constant) of the material (ref. 2). At higher temperatures ion mobility, for example, is increased causing increased polarization effects and, therefore, an increase in the measured capacitance. It would appear that pyrolytic boron nitride is approaching the characteristics of an ideal dielectric over a wider temperature range than any other solid dielectric material presently available.

b. SAPPHIRE

The change in capacitance and dissipation factor was measured for sapphire capacitor No. 1. This capacitor has sputtered platinum-20% rhodium alloy electrodes 0.383-inch diameter. The dielectric thickness averages about 3.0 mils. (Refer to table 6.)

Figure 10 shows the data obtained for two frequencies (1 kc/sec and 10 kc/sec) in vacuum at ~1 x 10^{-7} torr. The capacitance increased linearly over the temperature range (room temperature to 1100° F) with a total increase of about 6.8 percent at 1100° F. Figure 11 shows similar data for sapphire capacitor No. 2 which is about one inch in diameter (refer to table 6 for process and dimensional details). The capacitance change as a function of temperature (figure 11) is shown as actual capacitance values. Dissipation factor (tan δ) as a function of temperature is shown in figures 12 and 13 at 100 cycles/sec, 1 kc/sec, and 10 kc/sec. The hysteresis effects noted in figure 13 are discussed in a later section.

c. BERYLLIUM OXIDE (BeO), LUCALOX (Al_2O_3 plus 0.25 MgO), AND HOT-PRESSED LINDE A (Al_2O_3)

Figures 14 and 15 show the change in capacitance and the ratio of $\Delta C/C_{72° F} \times 100$ for BeO capacitor No. 2 and Lucalox capacitor No. 1. It is evident that the BeO capacitor shows the least change in capacitance up to 1100° F and also exhibits lower losses at 1100° F (refer to figures 16 and 17).

Figure 18 shows the capacitance and dissipation factor for hot-pressed alumina capacitor No. 2 (Linde A). The dielectric losses increase rapidly at temperatures over 300° F. These observations were not unexpected because the wafers contained a few dark spots which resulted from contaminants that diffused into the wafers during hot-pressing and no attempt has been made, as yet, to refine the hot-pressing techniques to eliminate these impurities.

SAPPHIRE CAPACITOR NO. 1

Electrodes: Pt-20% Rh, 0.383 inch diameter
Dielectric Thickness: ~0.003 inches
Vacuum: 7.4×10^{-8} to 2×10^{-7} torr
Av. Heating Rate: 3.4 to 4°F/min.
Measurements: GR Type 1620-A Bridge Assembly

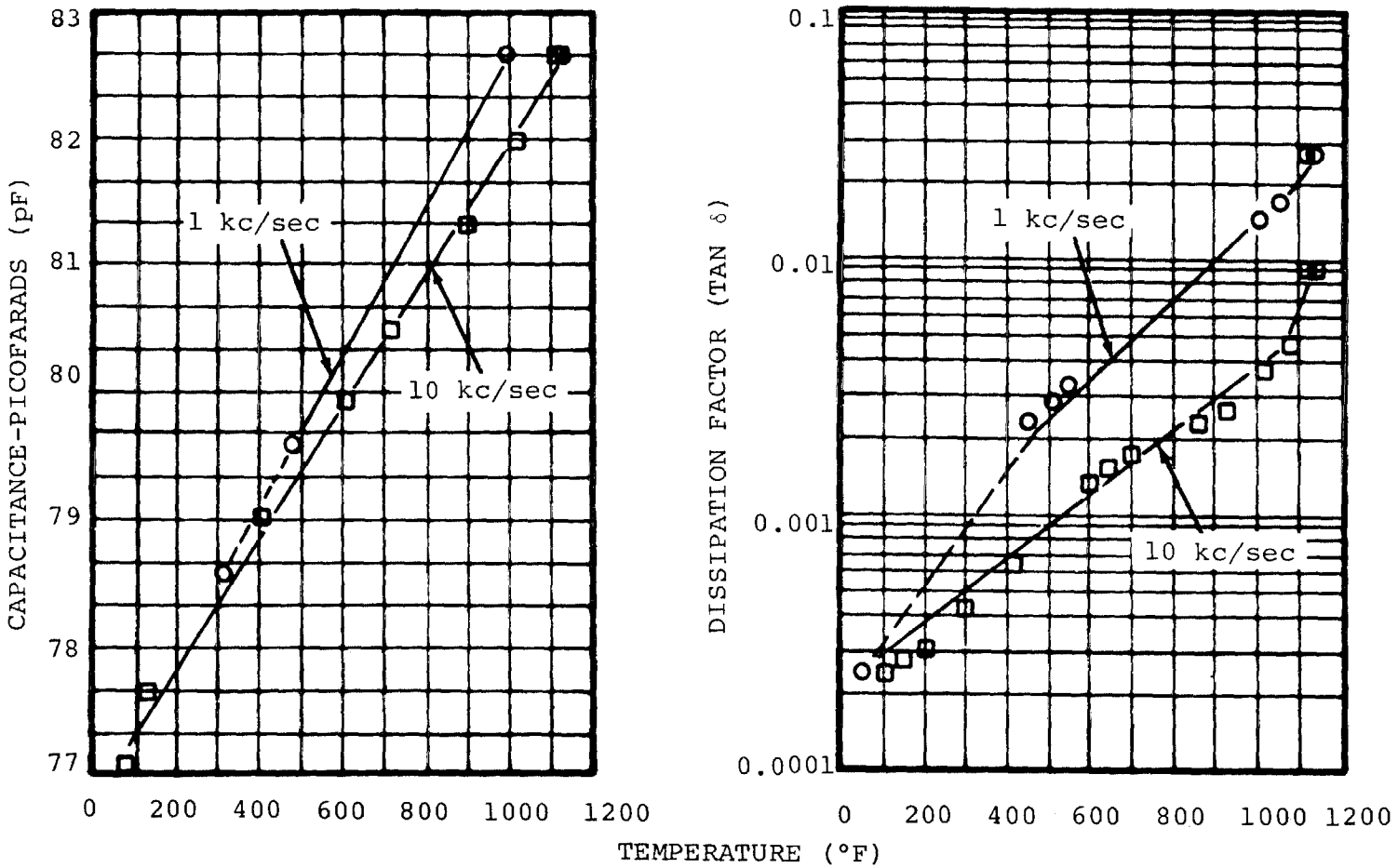


Figure 10. Capacitance and Dissipation Factor (tan δ) at Temperature for Sapphire Capacitor No. 1 (Measured in Vacuum)

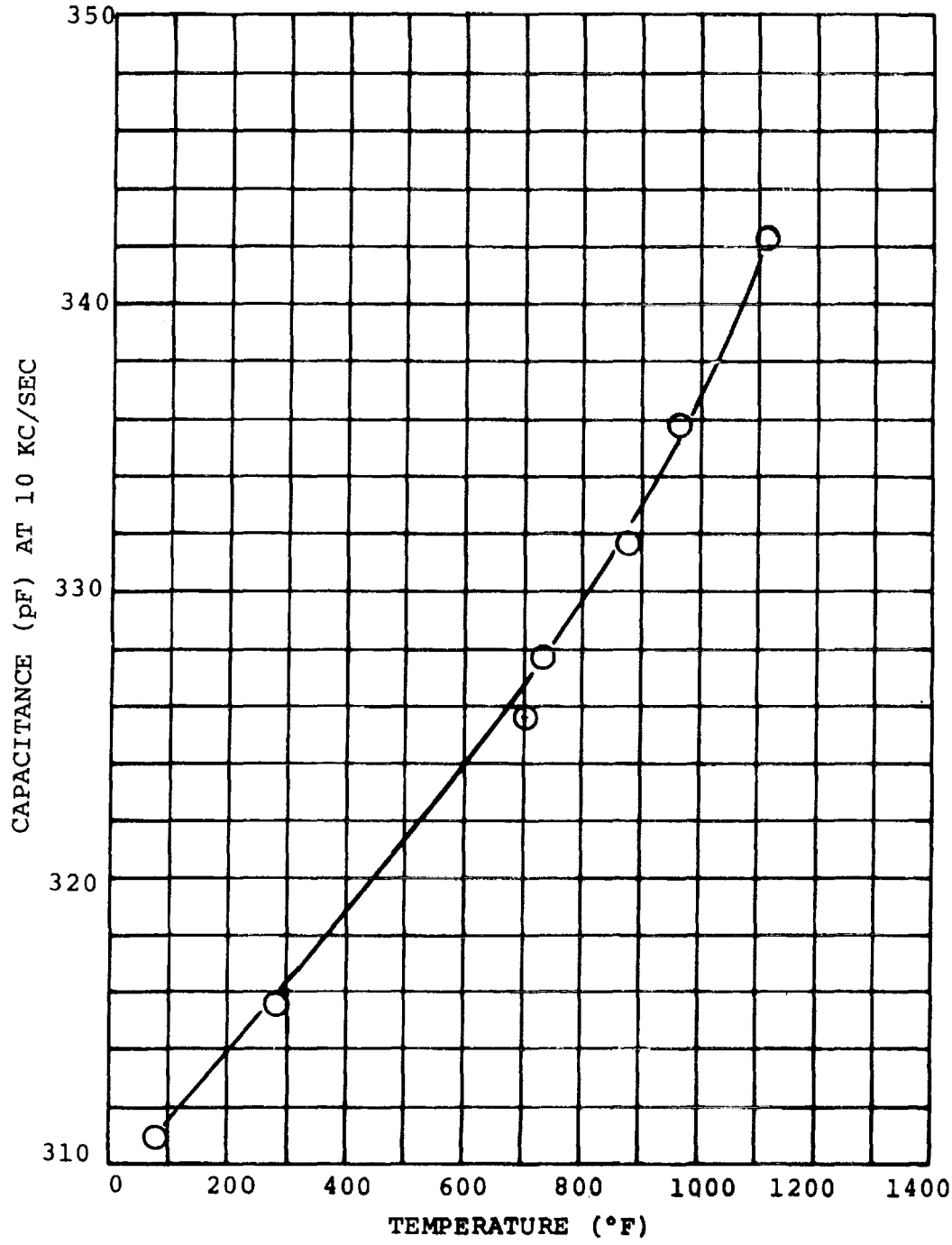


FIGURE 11. Capacitance Change Versus Temperature at 10 kc/sec for Sapphire Capacitor No. 2 (Measured in Vacuum at $1\text{-}3\text{x}10^{-7}$ torr)

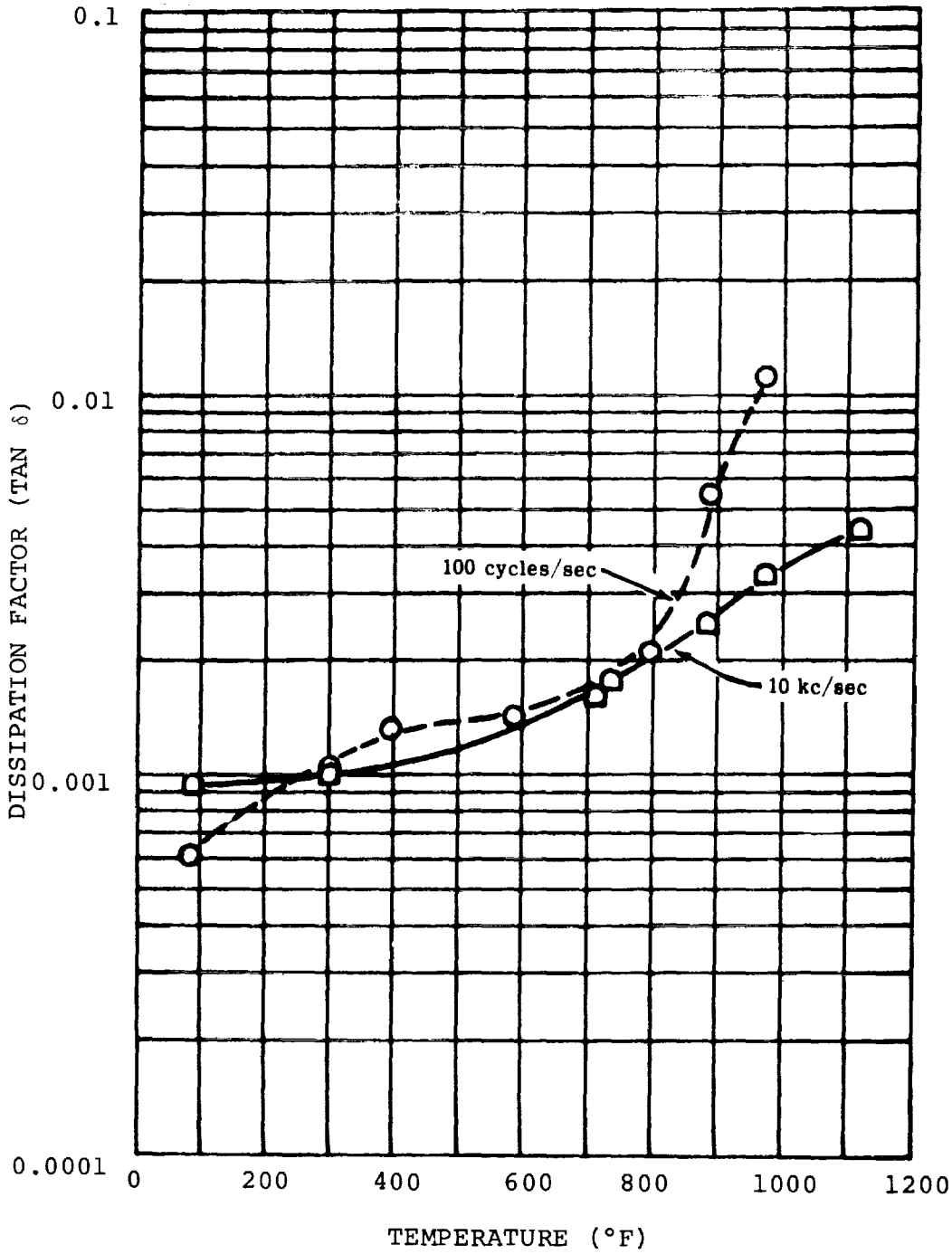


FIGURE 12. Dissipation Factor (tan δ) of Sapphire Capacitor No. 2 at 10 kc/sec and 100 cycles/sec Versus Temperature (Measured in Vacuum at 1-4x10^{-7} torr)

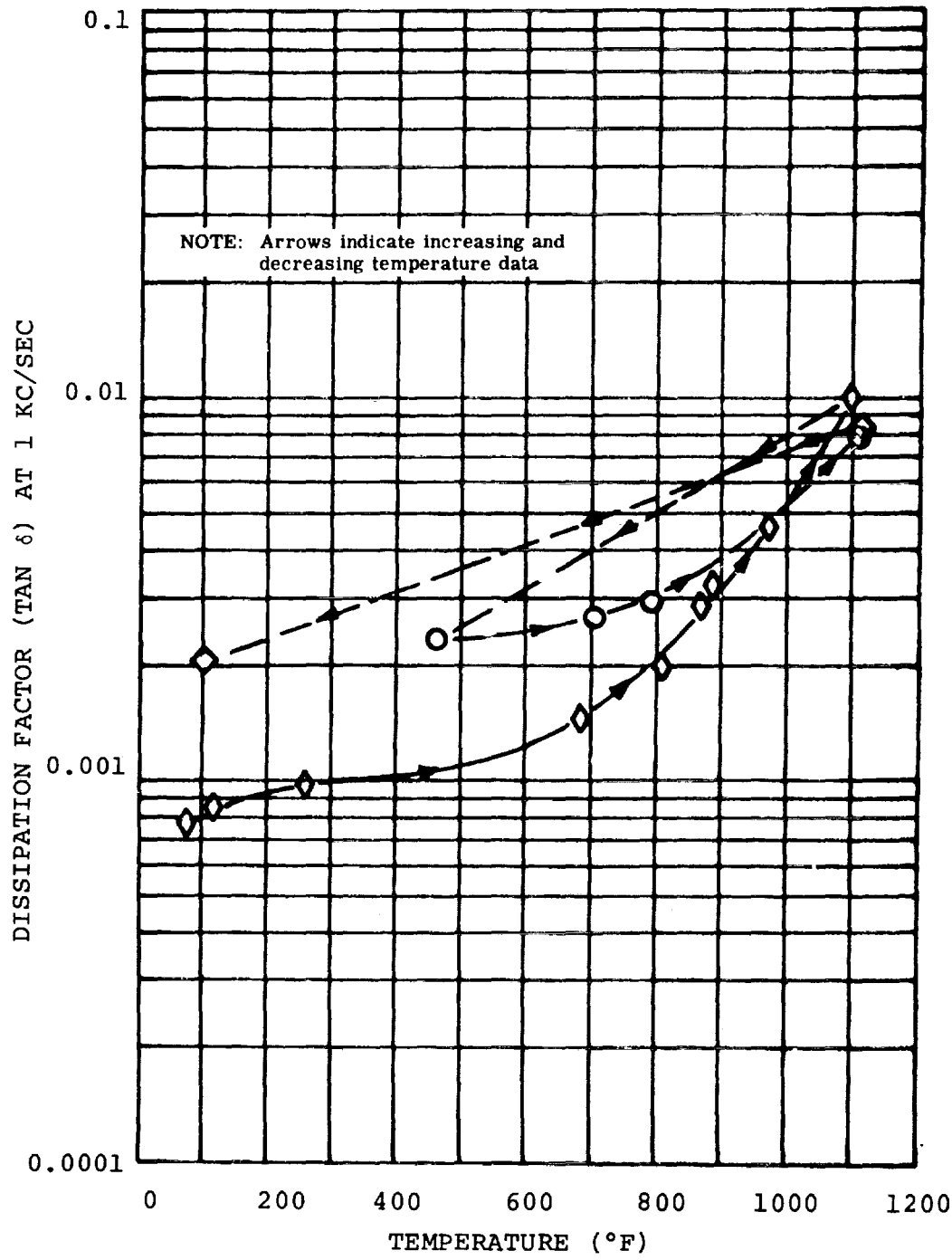


FIGURE 13. Dissipation Factor (tan δ) Versus Increasing and Decreasing Temperature for Sapphire Capacitor No. 2 at 1 kc/sec (Measured in Vacuum at $1\text{-}4 \times 10^{-7}$ torr)

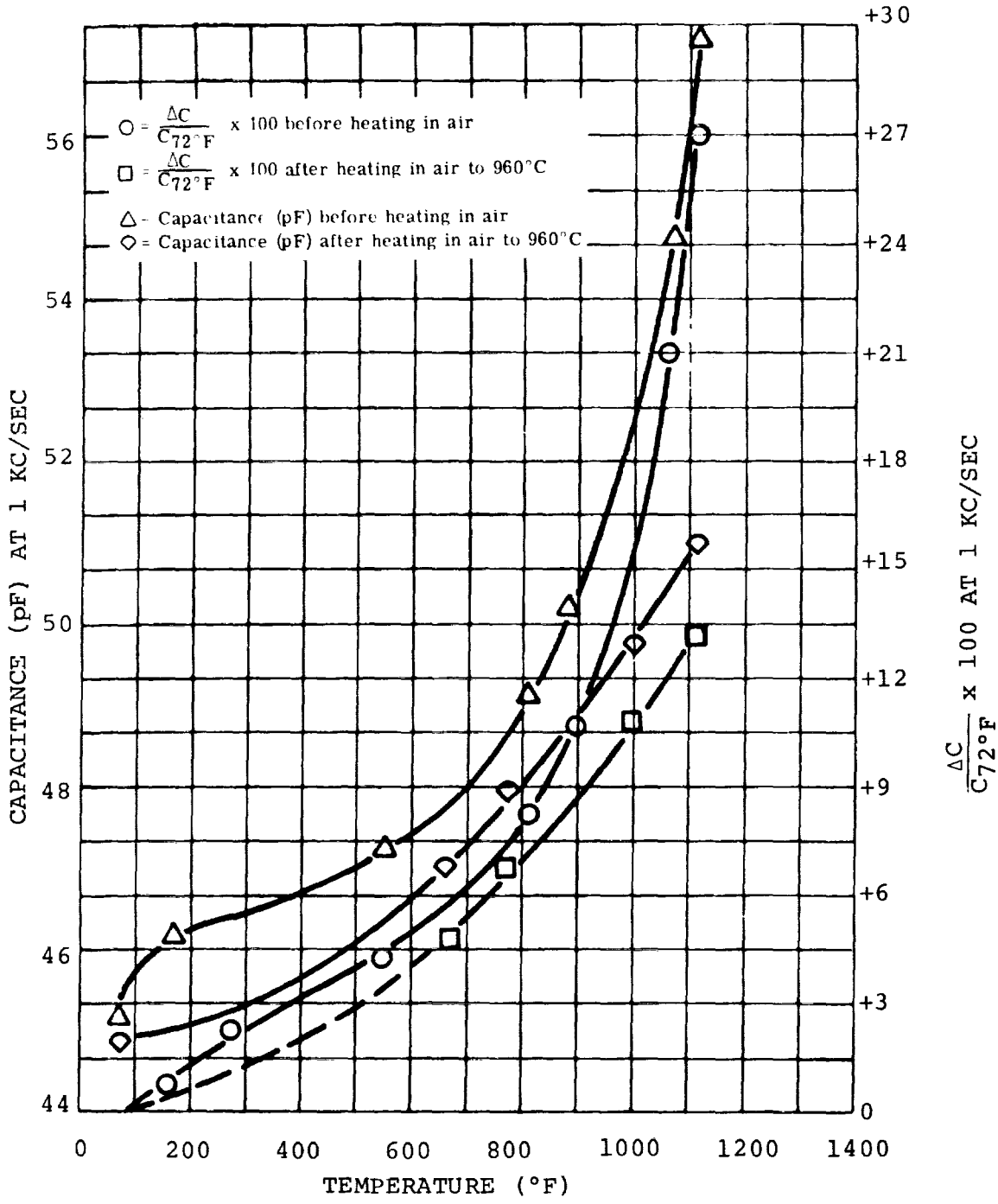


FIGURE 14. Capacitance Change Versus Temperature for BeO Capacitor No. 2 Before and After Heat Treatment in Air (Run No. 1 Versus Run No. 2) (Measured in Vacuum at $1\text{-}3\times10^{-7}$ torr)

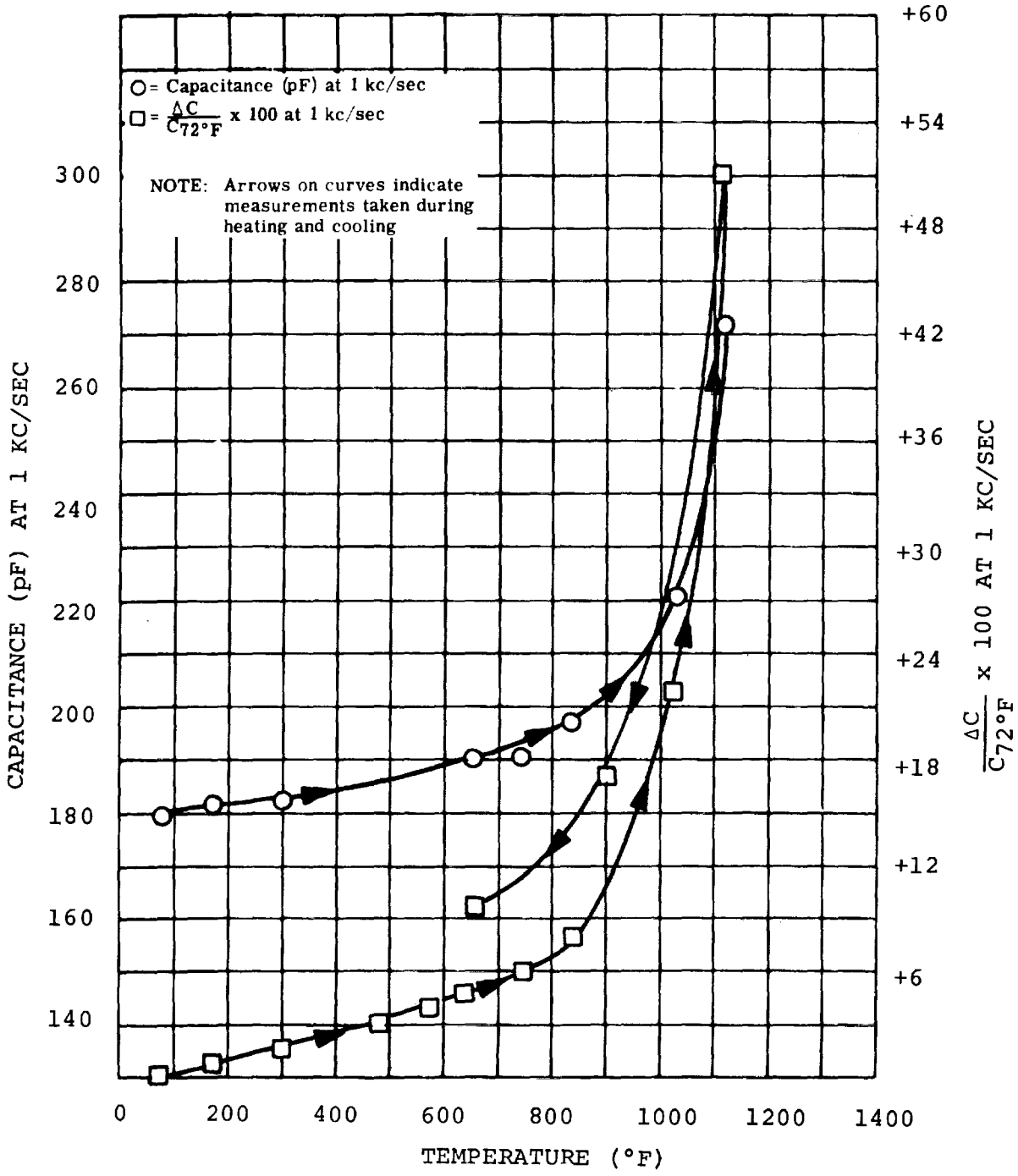


FIGURE 15. Capacitance Change Versus Temperature for Lucalox Capacitor No. 1 at 1 kc/sec (Measured in Vacuum at $1\text{-}3\times10^{-7}$ torr)

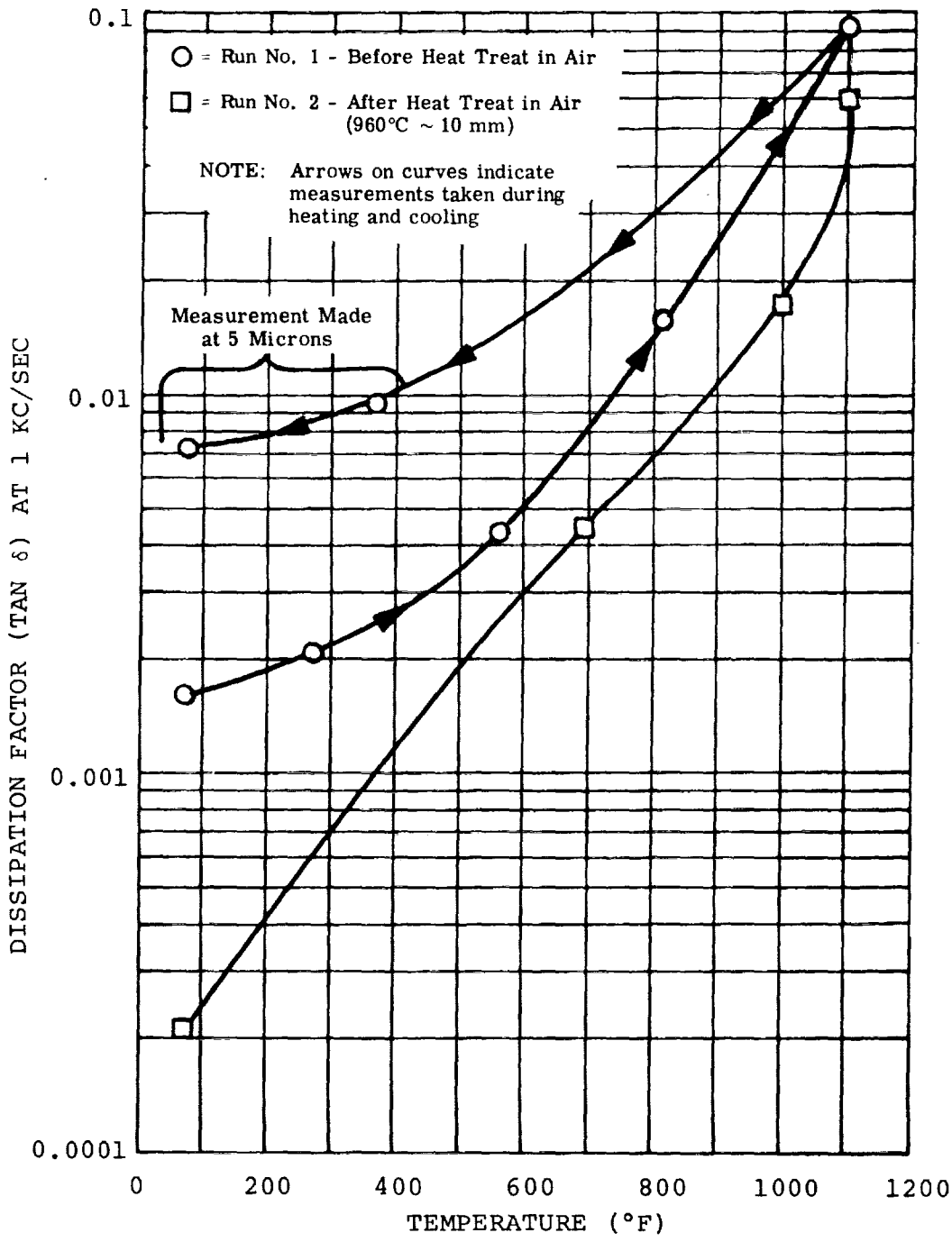


FIGURE 16. Dissipation Factor (tan δ) Versus Temperature for BeO Capacitor No. 2 Showing Hysteresis Effects on Cooling and the Effects of Heat Treatment in Air After Completion of Run No. 1 (All measurements made at $1\text{-}3\times10^{-7}$ torr except as noted)

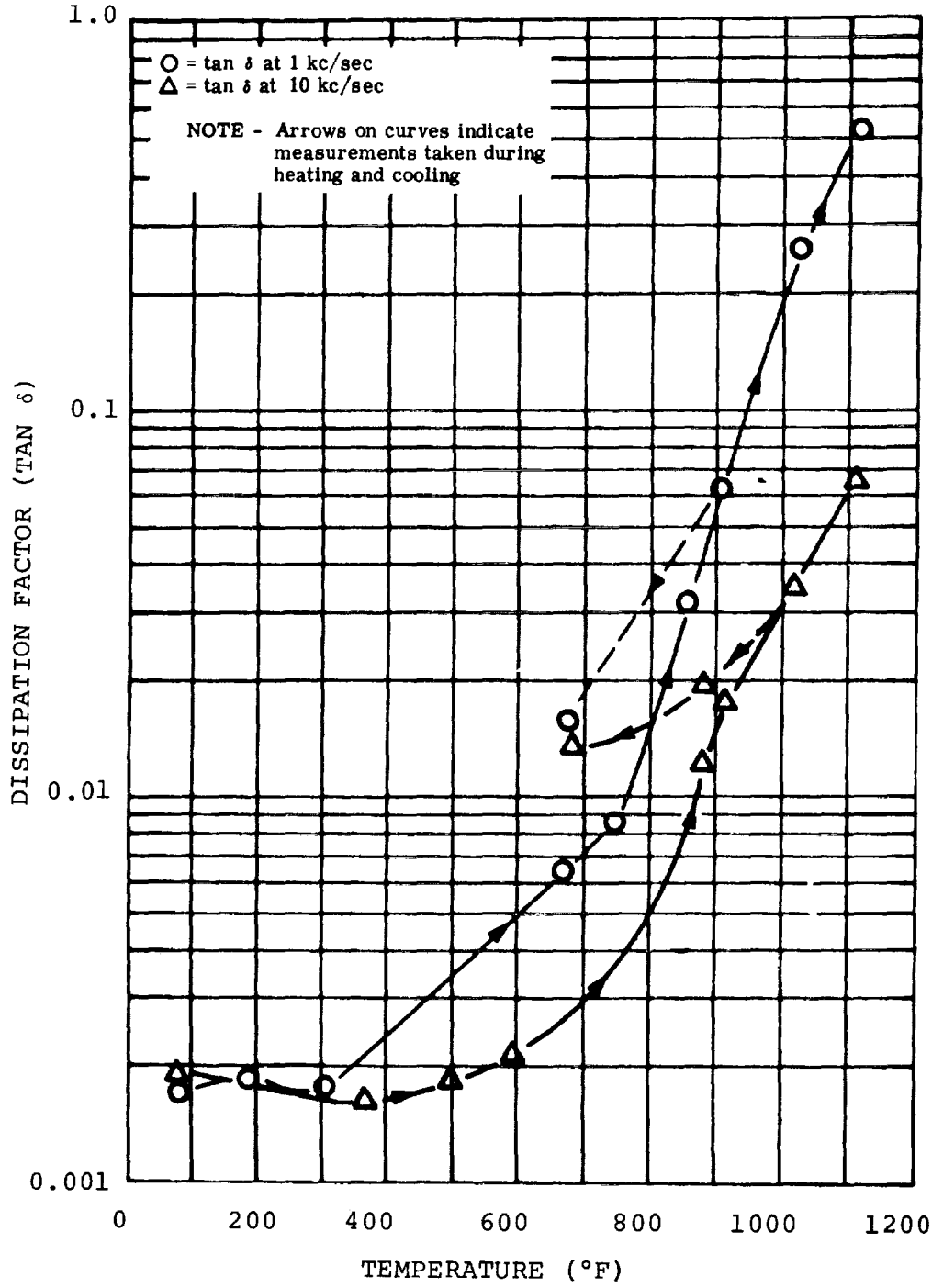


FIGURE 17. Dissipation Factor (tan δ) Versus Temperature for Lucalox Capacitor No. 1 Showing Hysteresis Effects on Cooling (Measured in Vacuum at $1\text{-}3\times10^{-7}$ torr)

HOT PRESSED Al_2O_3 CAPACITOR NO. 2

Electrodes: Pt-20% Rh, 0.377 inch diameter
Wafer: 0.416 inch diam., ~0.004 inch thick
Vacuum: 1.2 to 3 x 10^{-7} torr
Measurements: GR Type 1620-A Bridge Assembly

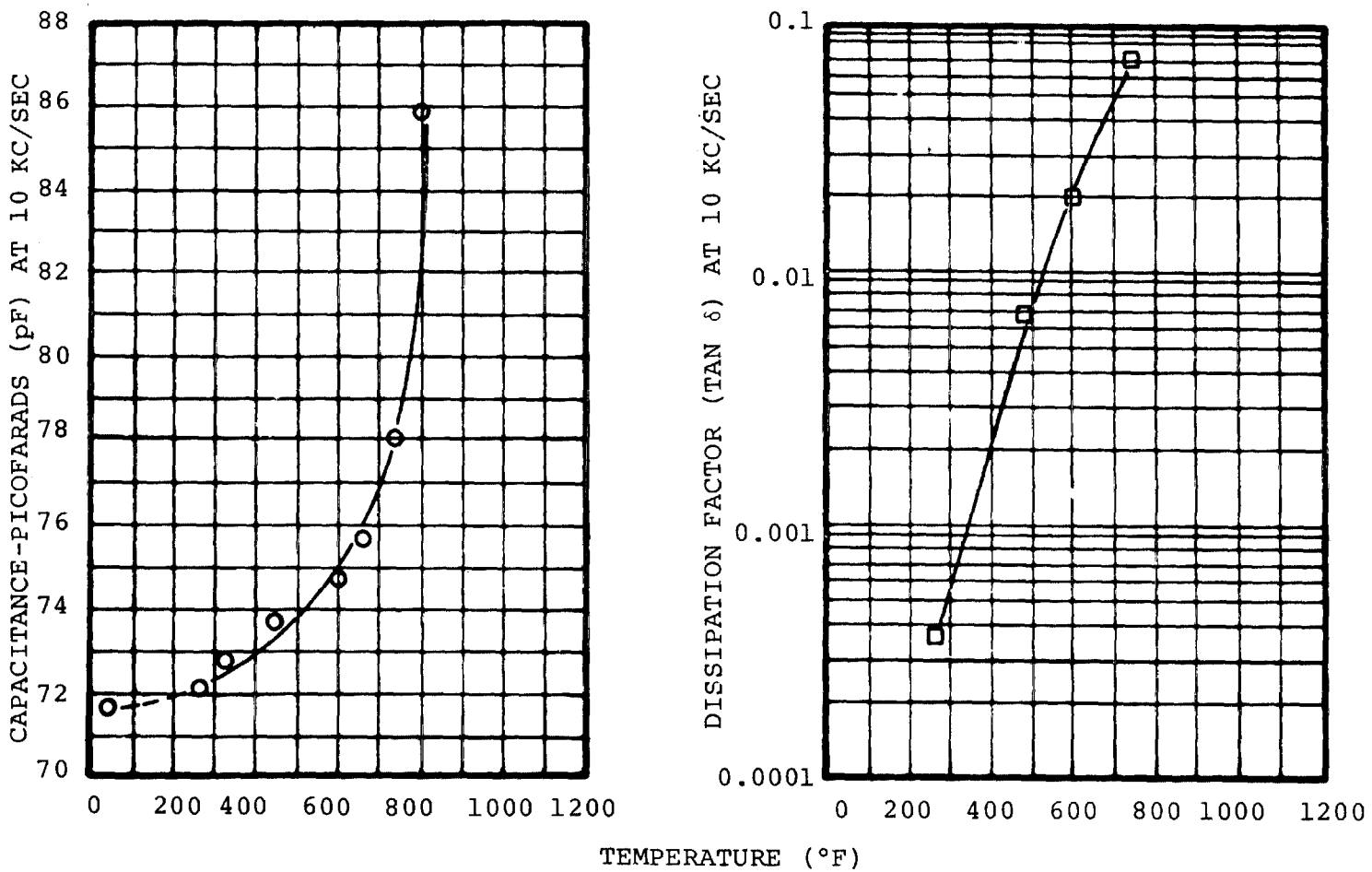


FIGURE 18. Capacitance and Dissipation Factor (tan δ) Versus Temperature of Hot-Pressed Al_2O_3 Capacitor No. 2 (Measured in Vacuum)

d. HYSTERESIS AND AGING EFFECTS

Several of the curves presented for tan δ and capacitance changes with temperature show a hysteresis effect after measurements were made during increasing temperature versus those recorded during cooling. In all instances, the measured capacitance and tan δ values were higher on the cooling curve than on the corresponding heating curve. This effect was not observed to any significant degree with pyrolytic boron nitride (see figure 33, section III) but appeared to be most pronounced for metal oxide type dielectrics (Lucalox, BeO, and sapphire).

Several explanations have been considered to explain this effect. The one that seems reasonable at present is somewhat analogous to spontaneous polarization in ferroelectric materials or to the concept of an electret. An electret (ref. 3) results from a "frozen in" polarization and can be made synthetically by cooling molten wax under an applied field. For the measurements shown in this section, tan δ and capacitance readings were made alternately with d-c resistance measurements. A d-c voltage ranging from 100 to 1000 volts was applied to the specimens at temperatures up to 1100° F. It seems reasonable to expect that some degree of orientation polarization occurred particularly at the higher temperatures where charge carriers (from impurities etc.) are more mobile. On cooling, this induced polarization persists in a non-equilibrium state and then gradually relaxes possibly by bulk or grain boundary diffusion or surface adsorption. Examples of these effects are shown in figures 13, 15, 16, and 17 for sapphire, BeO and Lucalox capacitors at different measuring frequencies.

Figure 19 shows an aging effect on tan δ and capacitance for BeO capacitor No. 2 after it was heated in air to 1760° F (960° C). A very marked decrease in tan δ at room temperature is evident after 200 hours of aging time. The capacitance is also shown to decrease with time. This effect is similar to that observed in ferroelectric barium titanate.

Figures 20 and 21 show the effect of heat treatment on the ratio of $\frac{\Delta C}{C_{50\ cps}} \times 100$ and the ratio of $\frac{\Delta \tan \delta}{\tan \delta_{50\ cps}} \times 100$ as a function of frequency for BeO

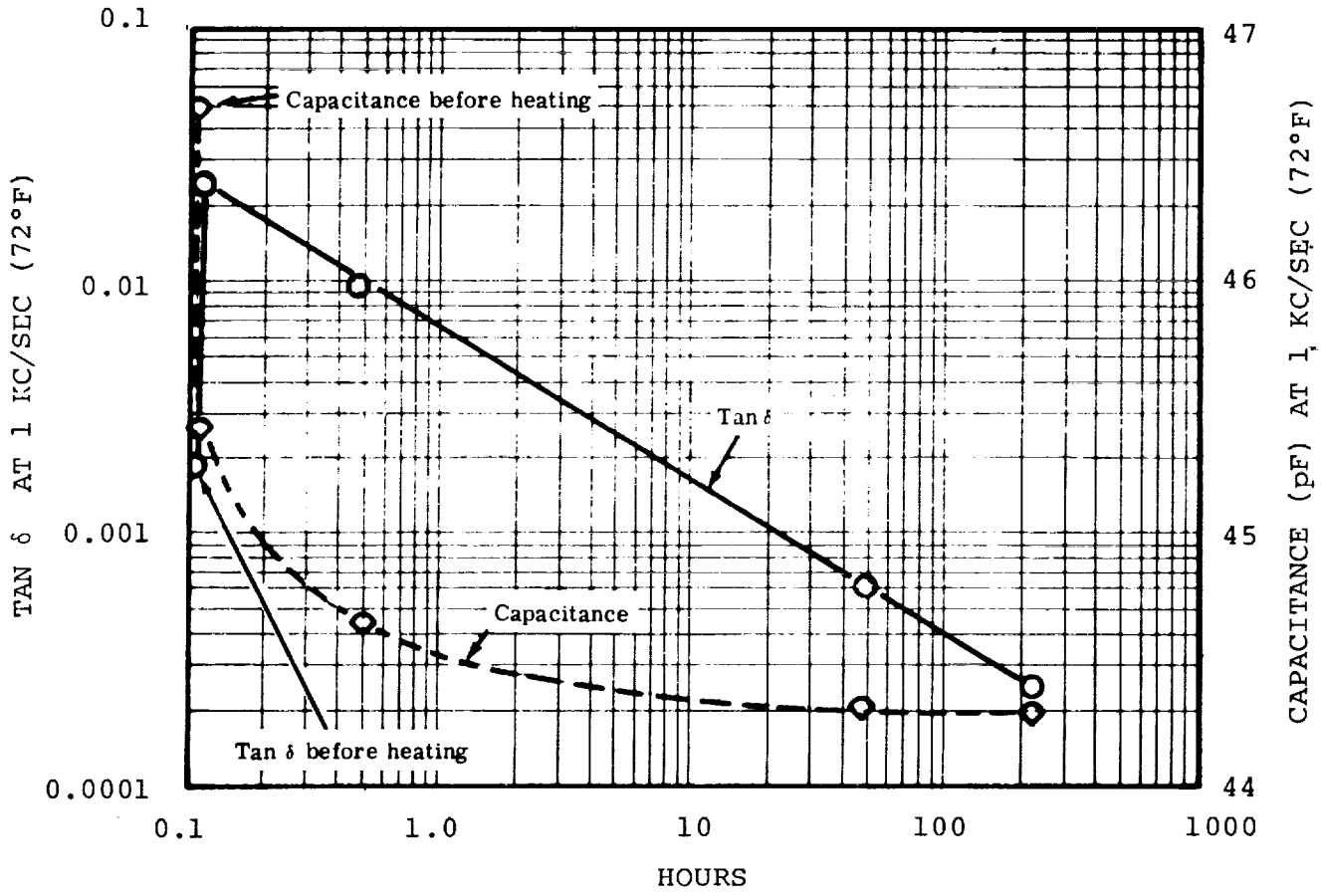


FIGURE 19. Dissipation Factor (tan δ) and Capacitance Versus Time After Heat Treating BeO Capacitor No. 2 in Air to 960° C (Cooled and Aged in Air, 72° F)

Capacitor No. 2. Volatilization of impurities is indicated by a flattening of the ΔC curve after heating the capacitor to 1760° F (960° C) in air (figure 20) and the effective series resistance of the electrodes may have been decreased. Another contributing factor may be the diffusion of oxygen in the platinum electrodes and the effects of an oxygen barrier layer at the electrode/dielectric interface.

D. COMPARISON OF DIELECTRIC MATERIALS AND FINAL SELECTION

1. DC Resistivity Versus Temperature

The d-c resistivity was calculated using the relationship:

$$\rho = RA/T$$

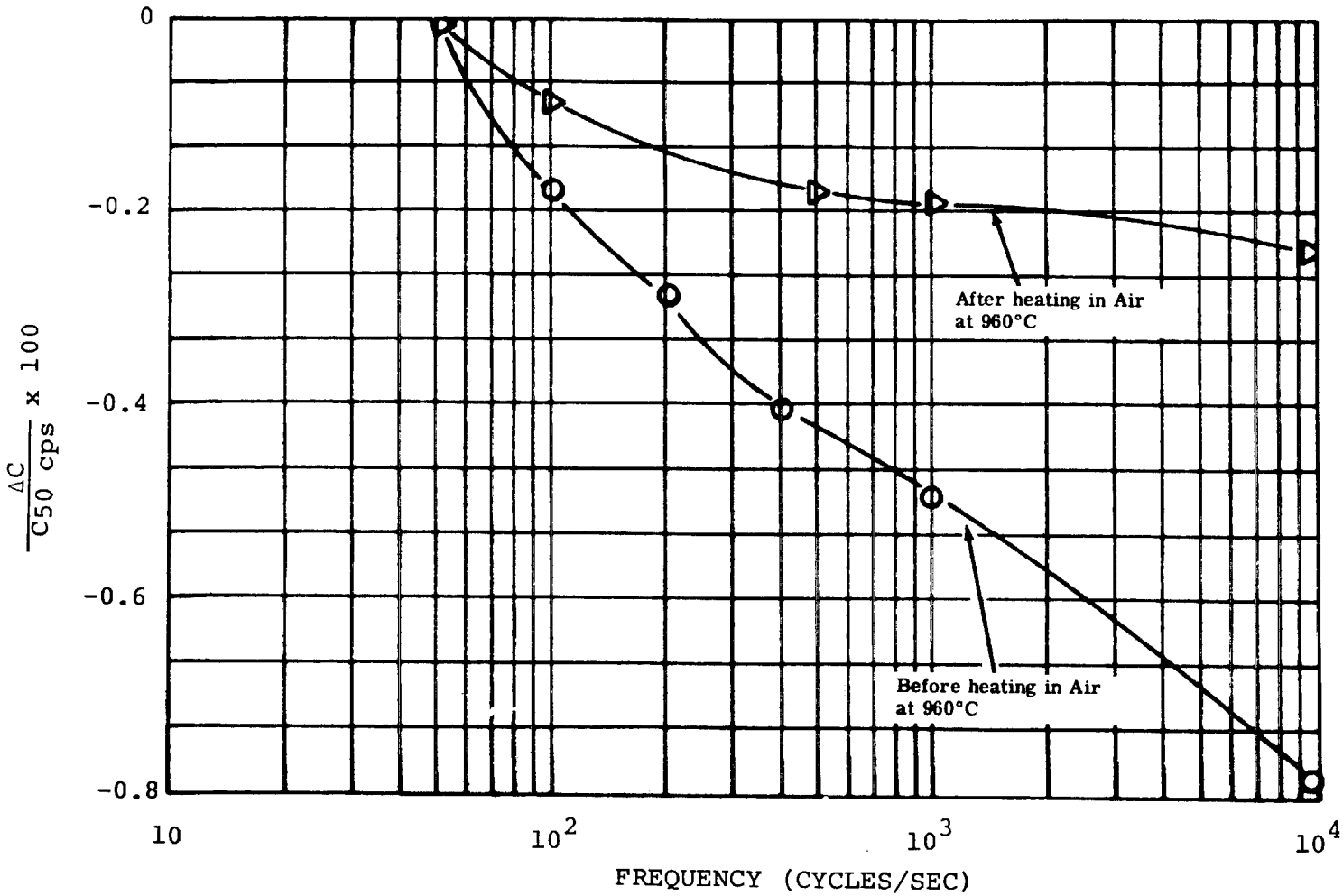


FIGURE 20. Effects of Heating BeO Capacitor No. 2 in Air at 960°C on the Ratio of $\frac{\Delta C}{C_{50\ cps}} \times 100$ Versus Frequency (Measured in Air at 72°F)

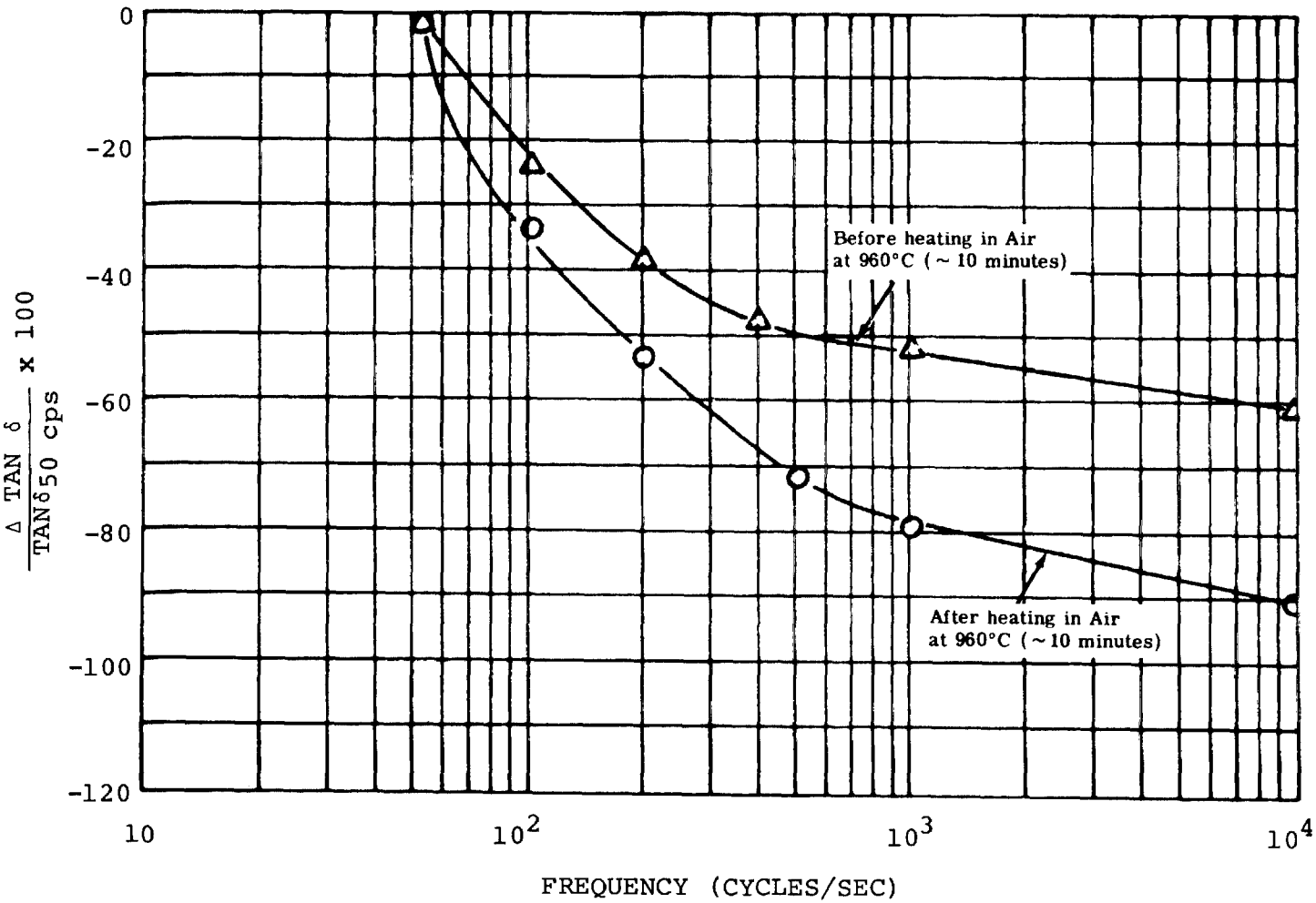


FIGURE 21. Effects of Heating BeO Capacitor No. 2 in Air at 960°C on the Change in the Ratio of $\frac{\Delta \tan \delta}{\tan \delta_{50 \text{ cps}}}$ x 100 Versus Frequency (Measured in Air at 72°F)

where

ρ = resistivity (ohm-cm)

R = measured d-c resistance (volume and surface contributions)

A = area of capacitor electrodes (cm^2)

t = thickness of dielectric (cm)

Resistivity values were determined for pyrolytic boron nitride (PBN capacitor No. 3), single crystal Al_2O_3 (sapphire capacitor No. 2), hot-pressed polycrystalline BeO (BeO capacitor No. 2), and polycrystalline Al_2O_3 (Lucalox capacitor No. 1). These data are shown as a function of increasing temperature in vacuum (1 to 4 x 10^{-7} torr) in figure 22. Capacitor wafer dimensions and electrode sizes used to calculate ρ are listed in table 6 for each of these capacitors. The data shown in figure 22 was obtained using specimens having no prior heat treatment or conditioning except that which was received during application of sputtered electrodes (refer to table 6). The d-c resistance was measured with a Keithly Model 610B Electrometer and a Keithly Regulated D-C Power Supply. In most instances 200 V d-c was applied to the specimens.

The values obtained for d-c resistance include the shunt effects of surface leakage currents. The magnitude of these currents is a variable that must be considered for a more precise analysis. However, for comparison purposes, the curves shown in figure 22 indicate that pyrolytic boron nitride has a higher d-c resistivity over most of the temperature range. At temperatures in the neighborhood of 1100° F, the resistivities of all the materials do not show as wide a divergence as indicated for temperatures in the 300° to 900° F range. This is particularly evident for pyrolytic boron nitride which has resistivities several orders of magnitude greater than the other materials tested in this range of temperatures.

2. Capacitance and Tan δ to 1100° F

Figure 23 shows tan δ measured at 10 kc/sec as a function of temperature for five different capacitor dielectrics (hot-pressed Al_2O_3, Lucalox, beryllium oxide, sapphire, and pyrolytic boron nitride). It is evident from a comparison of these curves that the pyrolytic boron nitride capacitor (PBN capacitor No. 2) has substantially lower losses.

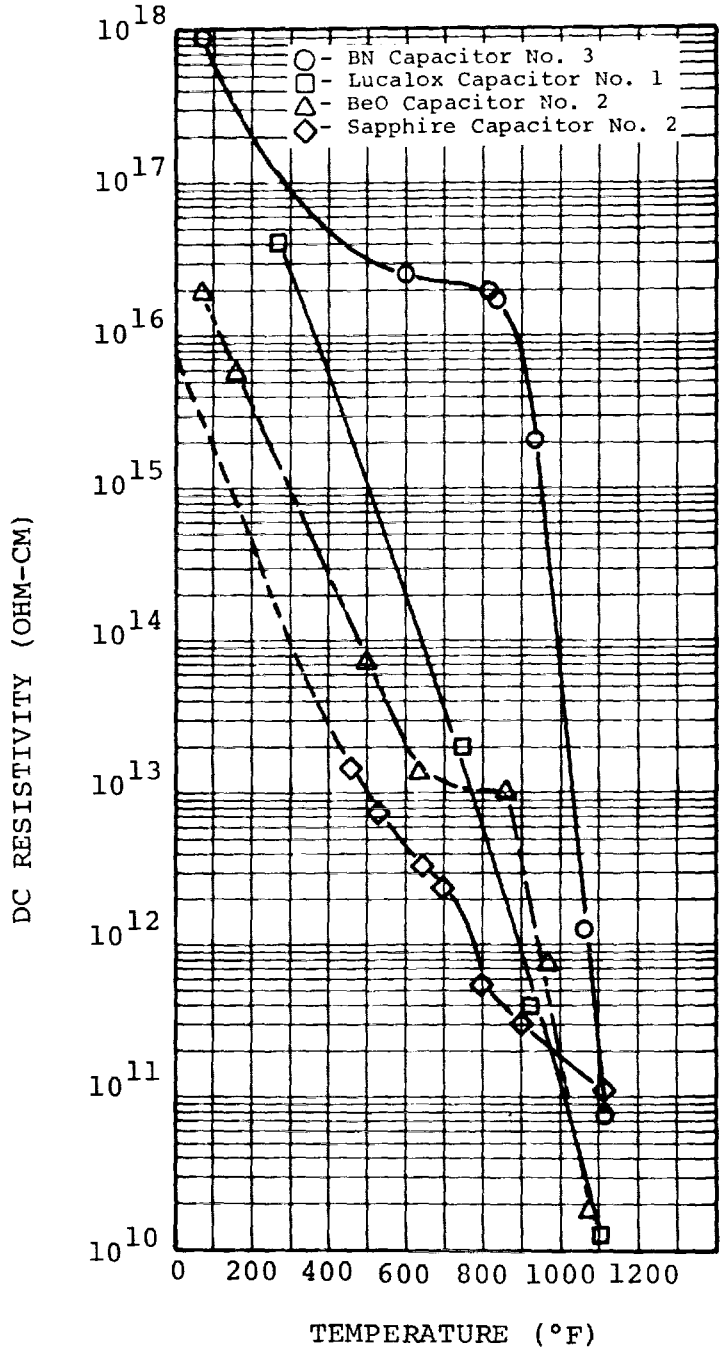


FIGURE 22. DC Resistivity (ohm-cm) Versus Temperature in Vacuum ($1\text{-}4\times10^{-7}$ torr) for Pyrolytic Boron Nitride (PBN Capacitor No. 3), Single Crystal Al_2O_3 (Sapphire Capacitor No. 2), Hot-Pressed BeO (BeO Capacitor No. 2), and Polycrystalline Al_2O_3 (Lucalox Capacitor No. 1)

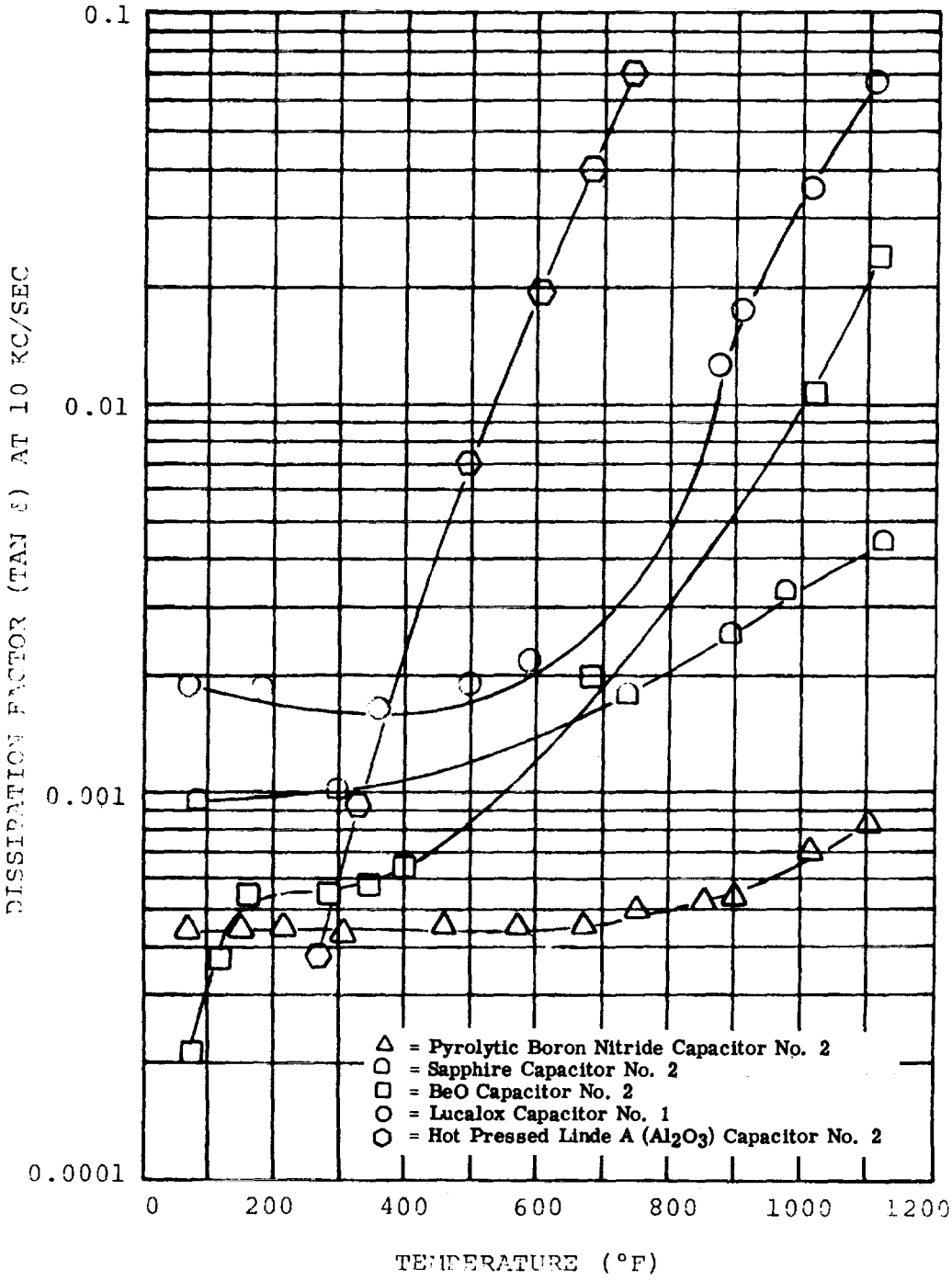


FIGURE 23. Comparison of Dissipation Factor (tan δ) Versus Temperature of Pyrolytic Boron Nitride, Sapphire, Beryllium Oxide, Lucalox, and Hot-Pressed Aluminum Oxide Capacitors (measured in vacuum at 10 kc/sec)

Figure 24 shows the ratio $\frac{\Delta C}{C_{72° F}} \times 100$ as a function of temperature measured at 10 kc/sec for four of the same dielectric materials. A comparison of these data shows that the PBN capacitor has the lowest percentage change in capacitance up to 1100° F. (Maximum change: negative 1.7% versus a positive change of 10 to 14% for the other materials.)

3. DC Breakdown Voltage at 1100° F

Measurement of precise breakdown voltages for capacitors with thin film electrodes was found to present several problems. When an electrical discharge occurs during the test it is usually difficult to determine if the current surge was caused by a surface discharge or a puncture through the bulk of the dielectric. In addition, the power supply relay which limits the current to 10 ma will not trip unless a permanent conducting path is created by the discharge. Since the thin film electrodes volatilize in the area of the discharge (self-healing effect) the current is almost instantaneously interrupted and the relay will not trip. Therefore, a Brush Model RD 2662 Oscillograph was used to record the voltage developed across several of the test capacitors. The first recorded drop in voltage was considered to be the breakdown voltage for that particular capacitor. The d-c power supply used was Model PSP 30-5 manufactured by Research-Cottrell, Inc.

The first test performed at 1100° F in vacuum (1 to 3 x 10^{-7} torr) showed a d-c breakdown voltage for sapphire capacitor No. 1 (3.25 mils thick) of approximately 6000 volts (1840 volts/mil). This value is based on the indicated supply voltage (meter reading) corresponding to the point where the relay tripped the power supply (10 ma). The next test was performed on a one-mil thick pyrolytic boron nitride capacitor at 1100° F (table 6, group 8). The Brush Oscillograph was used on this test to indicate the level of voltage applied to the test specimen. The first indication of a voltage drop occurred at 7000 volts (7000 volts/mil). However, the power supply relay did not trip the power supply until an indicated level of about 10,000 volts was recorded. BeO capacitor No. 2 was tested in a similar manner. The first indication of a voltage drop occurred at 3250 volts (762 volts/mil). The next indication occurred at 5250 volts (1167 volts/mil). The power supply was then manually turned off and the voltage was again increased with the first indication of a voltage drop occurring at 7500 volts (1665 volts/mil).

Examination of the PBN capacitor and BeO capacitor after these tests showed a number of puncture holes directly

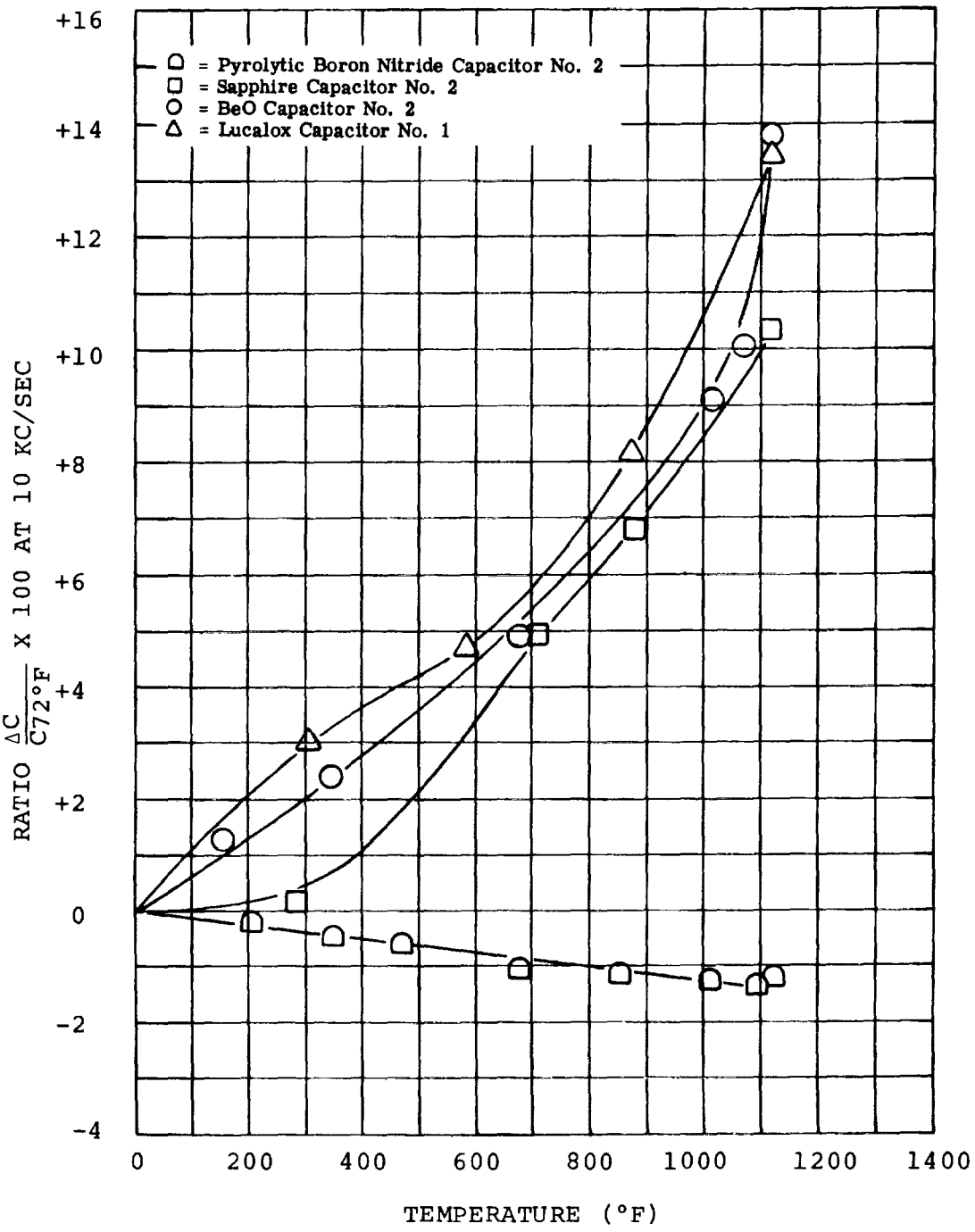


FIGURE 24. Comparison of the Ratio $\frac{\Delta C}{C_{72°F}}$ x 100 Versus Temperature of Pyrolytic Boron Nitride, Sapphire, Beryllium Oxide and Lucalox Capacitor (measured in Vacuum at 10 kc/sec)

through the material and volatilization of the electrodes at these points. The capacitors were still good when contact was made to the remaining portion of the electrodes (from 20 to 30 percent reduction in capacitance).

Summarizing these data for each of the capacitors, the breakdown voltages in vacuum at 1100° F are as follows:

a) Pyrolytic Boron Nitride - 7000 Vd-c/mil

b) Sapphire - 1840 Vd-c/mil

c) Beryllium Oxide - 762 Vd-c/mil

4. Relative Figure of Merit for Dielectric Materials

The data which have been discussed in previous sections for each dielectric material can be combined into a number for comparison purposes. A comparative number can be obtained in a variety of ways; however, the following relationship has been used to generate a so-called "figure of merit" (M).

$$M = \frac{\mu F}{in^3} \times \frac{1}{\tan \delta \ (1100° \ F)} \times \frac{1}{\Delta C/C_{72° \ F}}$$

where

M = Figure of merit

μF = Measured capacitance in microfarads at room temperature (1 kc/sec)

in^3 = Volume (electrode area x thickness) of dielectric material included between electrodes (refer to table 6)

Tan δ = Measured dissipation factor (tan δ) at 1100° F and 1 kc/sec

ΔC = Change in capacitance from room temperature to 1100° F

The value of M will be greater for capacitors that have a thinner dielectric, the lowest losses at 1100° F and show the least change in capacitance over the temperature range from room temperature to 1100° F. Therefore, the figure of merit (M) is an attempt to show the relative merits of each of the dielectric materials in terms of fabricability combined with measured 1100° F electrical data for specific single wafer capacitors.

Figure 25 shows the ratio $\frac{M}{M_{BN}}$ for PBN capacitor No. 2, sapphire capacitor No. 2, BeO capacitor No. 2, and Lucalox capacitor No. 1. Each ratio was determined by using the value of M for pyrolytic boron nitride (PBN capacitor No. 2) in the denominator. It is apparent from figure 22 that pyrolytic boron nitride is a logical first choice for a high-temperature (to 1100° F) capacitor dielectric by a factor of at least 100.

The volume parameter $\mu F/in^3$ used in these calculations does not include a voltage term because a true-working voltage could not be assigned at this point in the program. In fact, a working voltage can not be accurately determined unless extensive life testing were performed for each of the capacitor materials.

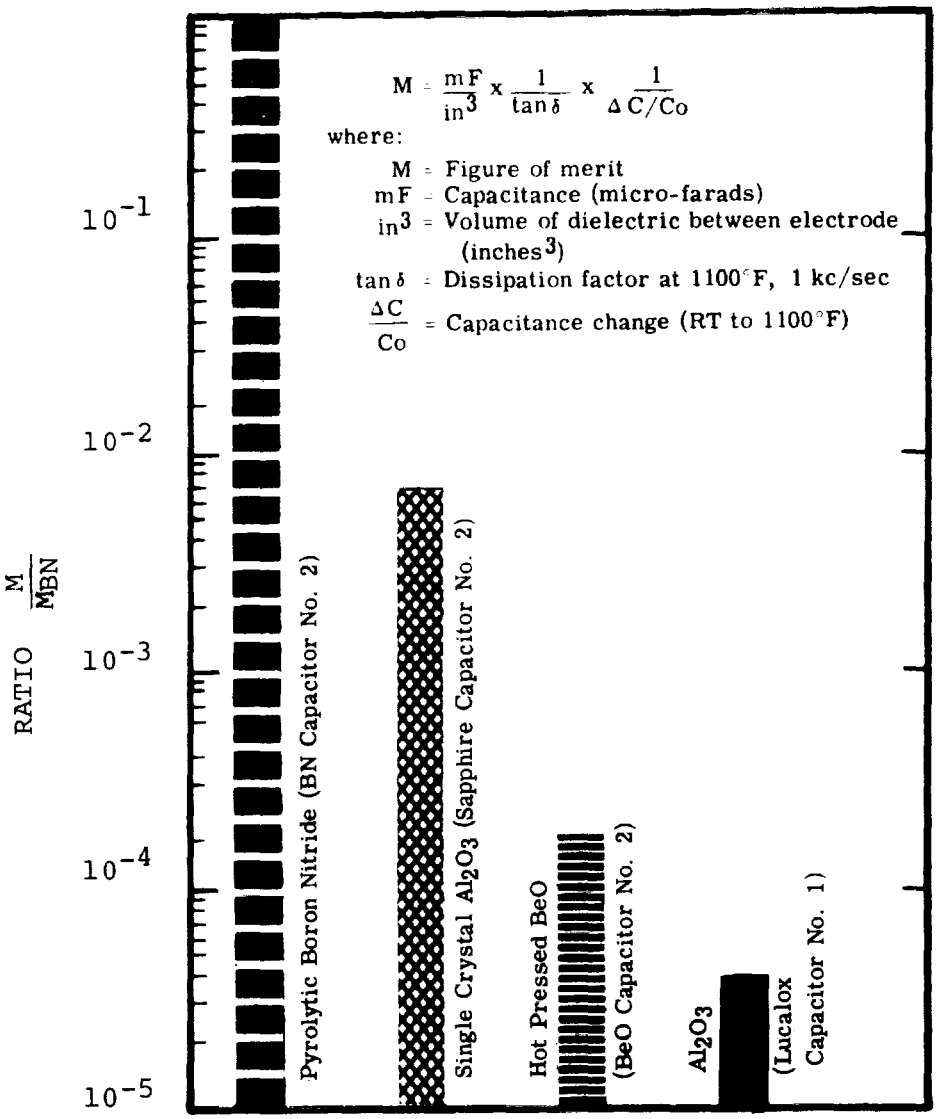


FIGURE 25. Figure of Merit (M) for Four Different Dielectric Materials Expressed as the Ratio $\frac{M}{M_{BN}}$
(M is calculated for 1 kc/sec Electrical Data)

SECTION III

MULTI-LAYER PYROLYTIC BORON NITRIDE CAPACITORS

Practically all fixed capacitors manufactured commercially (other than electrolytic types) are constructed by one of two general methods, stacking or rolling. The method of manufacture is governed primarily by the form and mechanical properties of the particular dielectric material used. For example, mica, glass, vitreous enamel, and ceramic dielectrics are built into high-capacitance units by stacking alternate layers or sheets between metal foil or by applying a metallizing paint or coating directly to each layer. Paper and plastic film dielectrics such as Kraft paper, Mylar or Teflon by virtue of their form and flexibility can be built into a compact unit by rolling two or more continuous sheets between metal foil or each sheet can be directly metallized before rolling.

The stacked approach has been selected to demonstrate the feasibility of an 1100° F capacitor because of the characteristic brittleness of high-temperature dielectric materials. With a satisfactory method of thin film electrode interconnection of individual capacitors, it is possible to obtain very high $\mu F \cdot volt/in^3$ values using thin (1-mil pyrolytic boron nitride) dielectrics. In fact, the $\mu F \cdot volt/in^3$ products of a capacitor capable of operating at 1100° F would be competitive with rolled plastic film capacitors designed for much lower operating temperatures.

The first part of this section contains the results of a group of tests designed to demonstrate the feasibility of interconnecting thin film electrodes in an 1100° F vacuum environment. Included in this analysis is an evaluation of different wafer geometries, wafer surface finishes and electrode thicknesses and materials with a discussion of the relationships between these factors and multi-layer capacitor losses. Methods used to control and measure electrode thicknesses are also discussed.

The section is concluded with a detailed presentation of electrical data obtained for a five layer capacitor and an analysis of the results of a series of endurance tests performed in vacuum at 1100° F.

A. DESIGN FEASIBILITY

1. Interconnection of Electrodes

It is necessary to connect the sputtered electrodes applied to each wafer in a stacked capacitor so that the top electrode of wafer No. 1 is electrically connected to the bottom electrode of wafer No. 2. The bottom and top electrodes of wafers No. 1 and No. 2 respectively, are directly opposite each other and would normally come in contact. This interconnection arrangement is shown in figure 26 for a five-wafer stack. The capacitance of each wafer is in parallel and additive, therefore, in a five wafer stack the total capacitance of the stack will be five times the capacitance of each wafer.

Figure 26 shows the wafers with tabs extending from opposite edges. These tabs are made an integral part of the dielectric and their function is to extend each electrode from one side of a wafer to the other side. When electrodes are applied to the wafers shown in figure 26 and the wafers are stacked one on top of the other, the electrodes on each wafer automatically connect in parallel when the stack is compressed. A 100-layer stack, for example, using one-mil thick wafers would have a compressed thickness only slightly in excess of 0.1-inch since the electrode thickness is negligible (1000 to 4000 angstroms (Å)).

Figure 27 shows how the sputtering masks have been designed to achieve the desired electrode configuration. A tabbed wafer is positioned between the two masks. Proper mask-to-wafer registration is achieved by providing a countersunk depression in one of the masks conforming to the wafer outline. Coincident holes are drilled in the top and bottom masks to insure mask-to-mask registration.

Electrodes are sputtered on both sides of the wafer at the same time. Since the sputtered atoms do not arrive at the substrate wafer from a point source but rather from a planar surface (target), they will deposit around the edges of the tabs. This effect provides electrical continuity from the top and bottom electrodes around to the opposite side of each tab.

The tabbed wafers and masks have been ultrasonically cut into the configurations shown in figure 26. Thin sheets of Corning Glass No. 7059 were used for the masking material. This glass was especially formulated to be used as substrates for thin film resistors and the glass has a very low alkali-ion content.

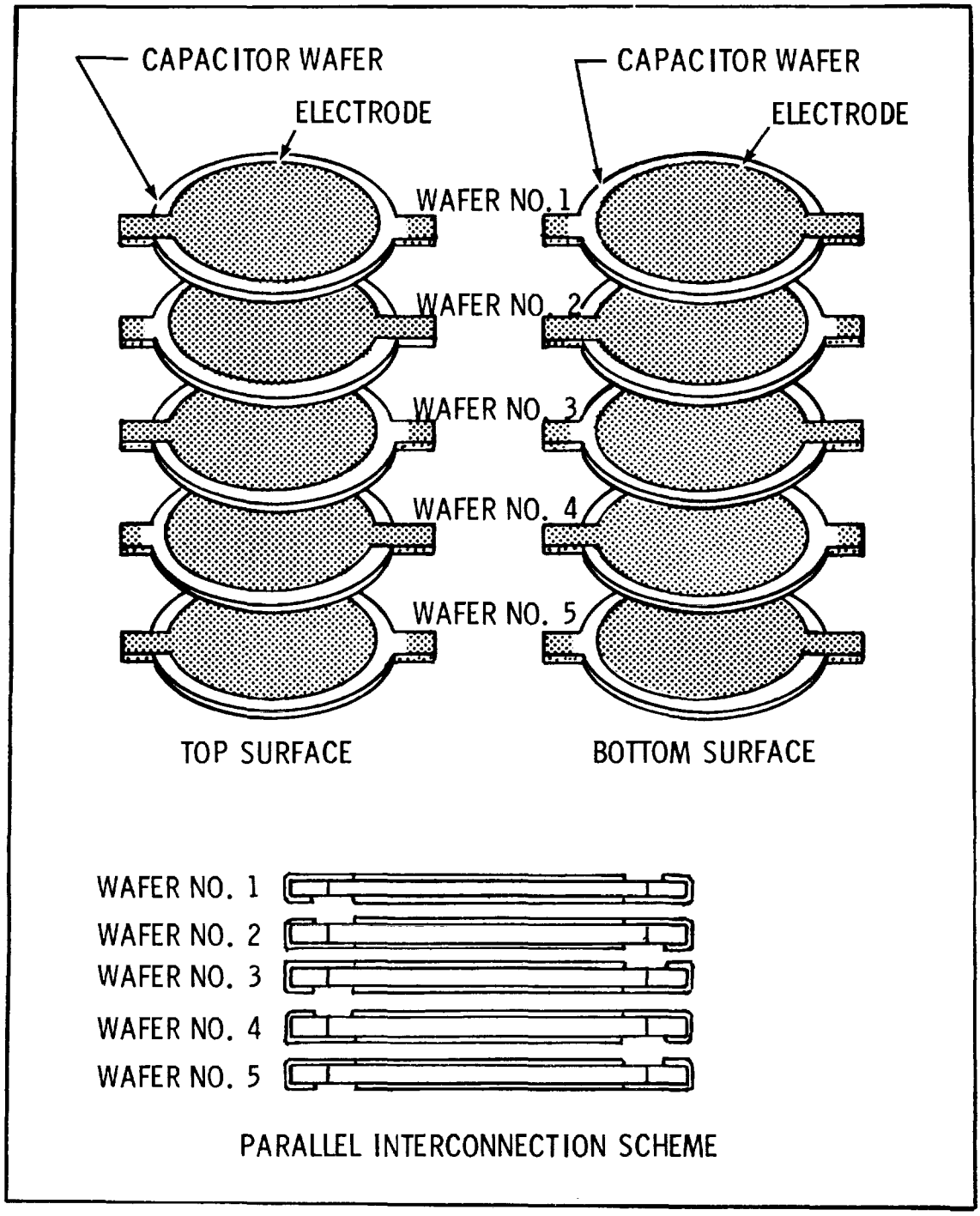


FIGURE 26. A Five-Layer Stacked Capacitor Showing Tabbed Wafers and Electrode Geometries and Electrode Orientation Necessary for Parallel Electrical Interconnection

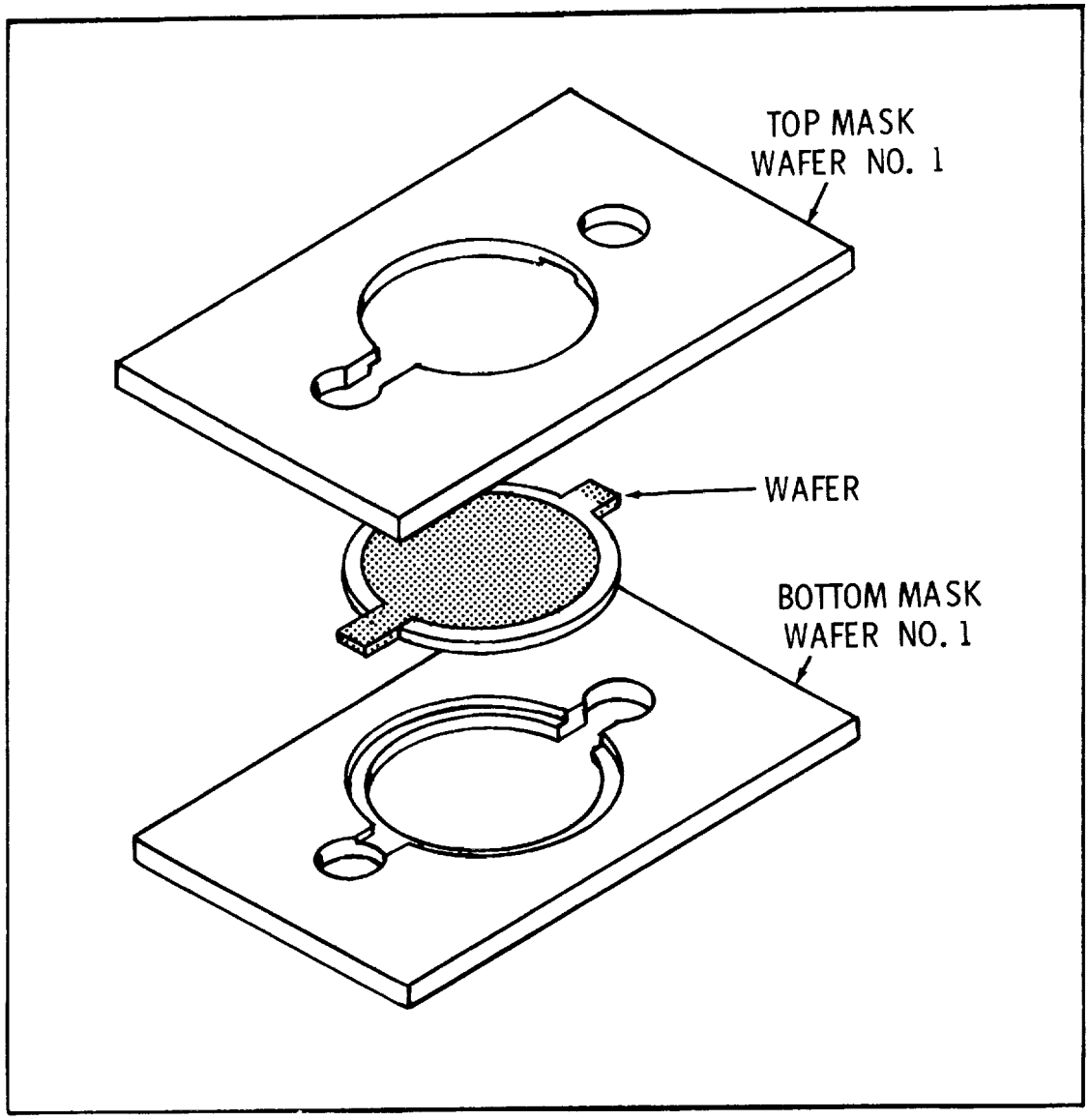


FIGURE 27. A Typical Set of Masks Used for Sputtering Electrodes on Tabbed Wafers

a. TABBED WAFER GEOMETRY

(1) Two-Layer Capacitor

A number of one-inch square by 1- to 0.5-mil-thick wafers of pyrolytic boron nitride were prepared with matte and polished surfaces. Slicing, lapping and polishing and final cleaning methods have been discussed in detail in previous sections.

Tabbed wafers were fabricated by two different methods.

a) Ultrasonic cutting (Sheffield Cavitron, Model 200 B-5) with a "cutting" tool machined into the mirror image or "female" outline of the wafer, and

b) Airabrasive (S.S. White Unit) cutting using a steel mask to cover the wafer outline.

Either of these methods is satisfactory although the "airabrasive" method is more convenient for small quantities. This operation is the final machining step prior to cleaning before deposition of sputtered electrodes.

Two tabbed wafers with sputtered Pt-20% Rh electrodes were prepared primarily to establish the feasibility of the parallel interconnection scheme as outlined previously and illustrated in figure 26.

Table 10 shows the individual capacitance and dissipation factors for the two tabbed wafers with Pt-20% Rh electrodes. In addition, similar data are shown for these two capacitors stacked one on top of the other and interconnected in parallel. All measurements were made via the tab contact points. The arithmetic sum of the individual wafer capacitances is shown in table 10 for comparison with the measured capacitance of the two-layer unit. This value is within 0.01% of the arithmetic sum indicating that a satisfactory interconnection can be achieved using "wrap-around" sputtered electrodes.

One of these tabbed wafer capacitors (tabbed PBN capacitor No. 2) was subsequently heated to 1100° F at 1 to 3×10^{-7} torr for about 1/2 hour. As shown in table 10, there are no significant changes in electrical properties before and after the test when measurements were made via the tab contact points. This test was performed as a preliminary step in evaluating the capability

TABLE 10. Properties of Tabbed Pyrolytic Boron Nitride Capacitors No. 1 and No. 2

	Electrical Data 72°F - Air				Characteristics of Substrate (Boralloy: Pyrolytic Boron Nitride)				
	Capacitance pF		Tan δ		Wafer Thickness (calculated)	Surface Finish	Electrodes	Sputtering Process	
	1 kc sec	10 kc sec	1 kc sec	10 kc sec				Sputter Time & Volts	Cross Reference
Tabbed PBN Capacitor No. 1	507.529	507.052	0.000777	0.000980	0.55 Mils	Polished	Pt-20% Rh	11 min. at 700 volts	Group 6 Table 6
Tabbed PBN Capacitor No. 2	321.549	321.151	0.000998	0.00194	0.86 Mils	As lapped (Matte)	Pt-20% Rh	10 min. at 700 volts	Group 5 Table 6
Arithmetic sum of capacitor No. 1 and No. 2 (capacitance)	829.078	828.203							
Measured value of stacked unit capacitor No. 1 and No. 2	829.183	828.344							
Tabbed PBN Capacitor No. 2 after heating to 1100 F at 2×10^{-7} torr	323.964	323.599	0.000926	0.00141					

of sputtered electrodes to maintain electrical continuity around the tabs after heating to the maximum test temperature (1100° F).

Further inspection of table 10 shows evidence of a possible correlation between wafer surface finish and dissipation factor. For example, tabbed PBN capacitor No. 1 has a polished surface; whereas, tabbed PBN capacitor No. 2 has a matte surface and it can be assumed that both wafers have equal thickness electrodes since the sputtering conditions were almost identical (11 minutes at 700 V for No. 1 and 10 minutes at 700 V for No. 2). Comparing the dissipation factor shown in table 10 for these two capacitors shows that a lower dissipation factor was measured at 1 kc/sec and 10 kc/sec for the capacitor with polished surfaces. This indicates that the increased loss is caused by an equivalent series resistance introduced by the electrodes on capacitor No. 2. The higher series resistance is apparently the result of an increase in the effective resistivity or ohms/square resistance of the thin film electrodes deposited on the capacitor wafer whose surfaces have a higher degree of roughness (matte finish).

(2) Three-Layer Capacitor

Another group of capacitor wafers were prepared with sputtered platinum electrodes (table 6, group 9). Room temperature measurements obtained for a three-layer unit are shown below for three different frequencies.

Capacitance	Dissipation Factor (tanδ)	Frequency
1134.4 pF	0.000520	50 cps
1133.3 pF	0.000605	1 kc/sec
1132.4 pF	0.001140	10 kc/sec

These are three terminal measurements made in a shielded metal box to minimize stray capacitance effects. The fixture used to align the wafers and make external electrical contact to the tab extensions is shown in figure 28. The component parts of the fixture are made from 1 by 1 by 1/8-inch blocks of pyrolytic boron nitride.

The individual capacitors in this unit have "as lapped" or matte surface finishes. The tan δ value for this capacitor is somewhat lower at 1 kc/sec and 10 kc/sec

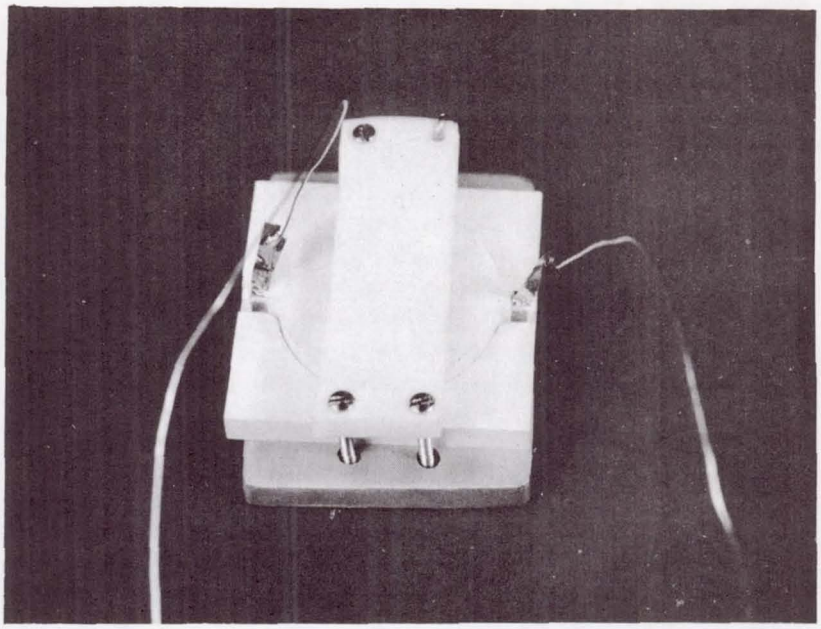


FIGURE 28. Fixture for Making Electrical Measurements on Stacked Tabbed Capacitor Wafers

than the tan δ values for the first two tabbed wafers with Pt-20% Rh electrodes shown in table 10. This is probably due to: a) the thicker electrodes (longer sputtering time) and b) the lower bulk resistivity of platinum versus the platinum-rhodium alloy. Further investigation of these effects are detailed in the next section.

b. RECTANGULAR VERSUS TABBED WAFER GEOMETRY

(1) Discussion of Factors Affecting A-C Losses

The previous section discussed the results of electrical measurements on a stacked three-wafer capacitor consisting of tabbed 0.750-inch diameter wafers (matte surface finish). Although the results were satisfactory, it was believed that lower a-c losses (particularly at frequencies greater than 1 kc/sec) might be obtained with a rectangular wafer geometry because of the increased contact area between interconnecting

electrodes. Figure 29 shows the wafer dimensions, electrode dimensions and the interconnection overlap. A photograph of the actual capacitor wafers together with several tabbed 0.750-inch diameter wafers is shown in figure 30.

For comparison purposes the data obtained for a group of tabbed and rectangular wafer capacitors was compiled into two separate tables (tables 11 and 12 respectively).

Table 11 was prepared to show a complete breakdown of the characteristics of each individual capacitor in a five-stack unit of tabbed capacitors. Electrical data on this unit was obtained from room temperature to 1100° F in vacuum and these results are discussed in another section. However, several important observations can be made with the aid of table 11 and the room temperature electrical data.

For example, the $\mu F/in^3$ value calculated for this unit is 1.74. If it is assumed that the capacitor can be rated at 500 Vd-c, then a $\mu F \cdot volt/in^3$ product of 870 is obtained. This value is better than eight times the minimum value established as a program objective.

Table 11 also shows the calculated average wafer thickness for each wafer. Thicknesses vary from 0.42 mils to 0.81 mils. Figure 31 shows a plot of tan δ versus thickness. For wafers one through four, the relationship is linear with a significant decrease in tan δ with increase in wafer thickness. Tan δ for wafer No. 5 does not lie on the straight line. The value of tan δ for this wafer is abnormally high by comparison and the tan δ versus thickness relationship obtained for the other four wafers could indicate that wafer No. 5 contains thin spots or defects.

One possible explanation of this effect might be associated with higher electrical losses attributed to a mechanically deformed surface layer and the thickness ratio of this layer compared to the overall thickness. For example, the depth of a deformed layer produced by various mechanical surface treatments on brass specimens (ref. 4) varied from about 50 microns to 1.1 micron. Therefore, it is reasonable to expect that the thinner capacitor wafers (0.4 to 0.6 mils or 10 to 15 microns) have a mechanically deformed layer that represents an increasing percentage of the total wafer thickness as total wafer thickness decreases.

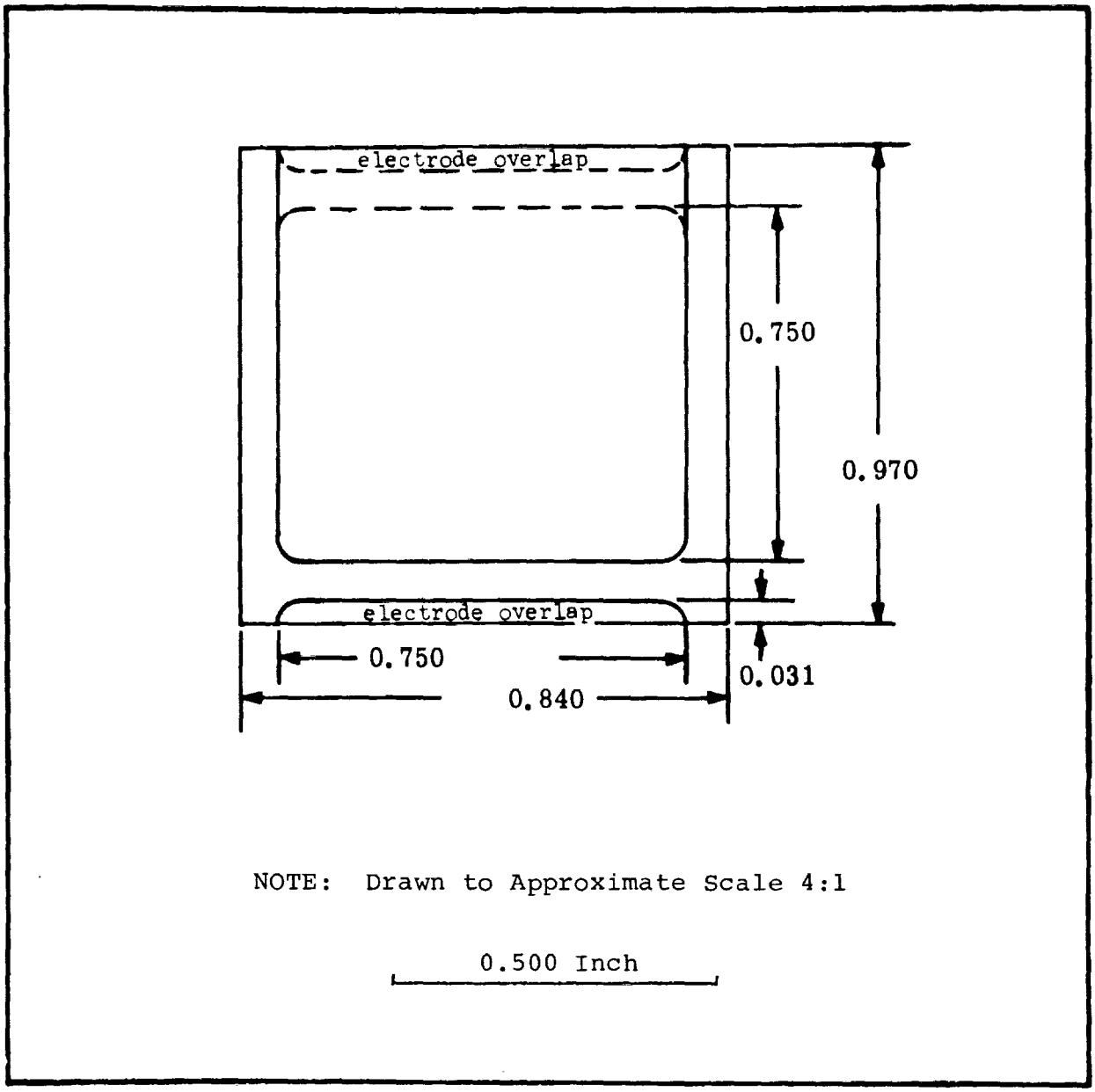


FIGURE 29. Dimensions of Rectangular Capacitor Wafers and Electrodes

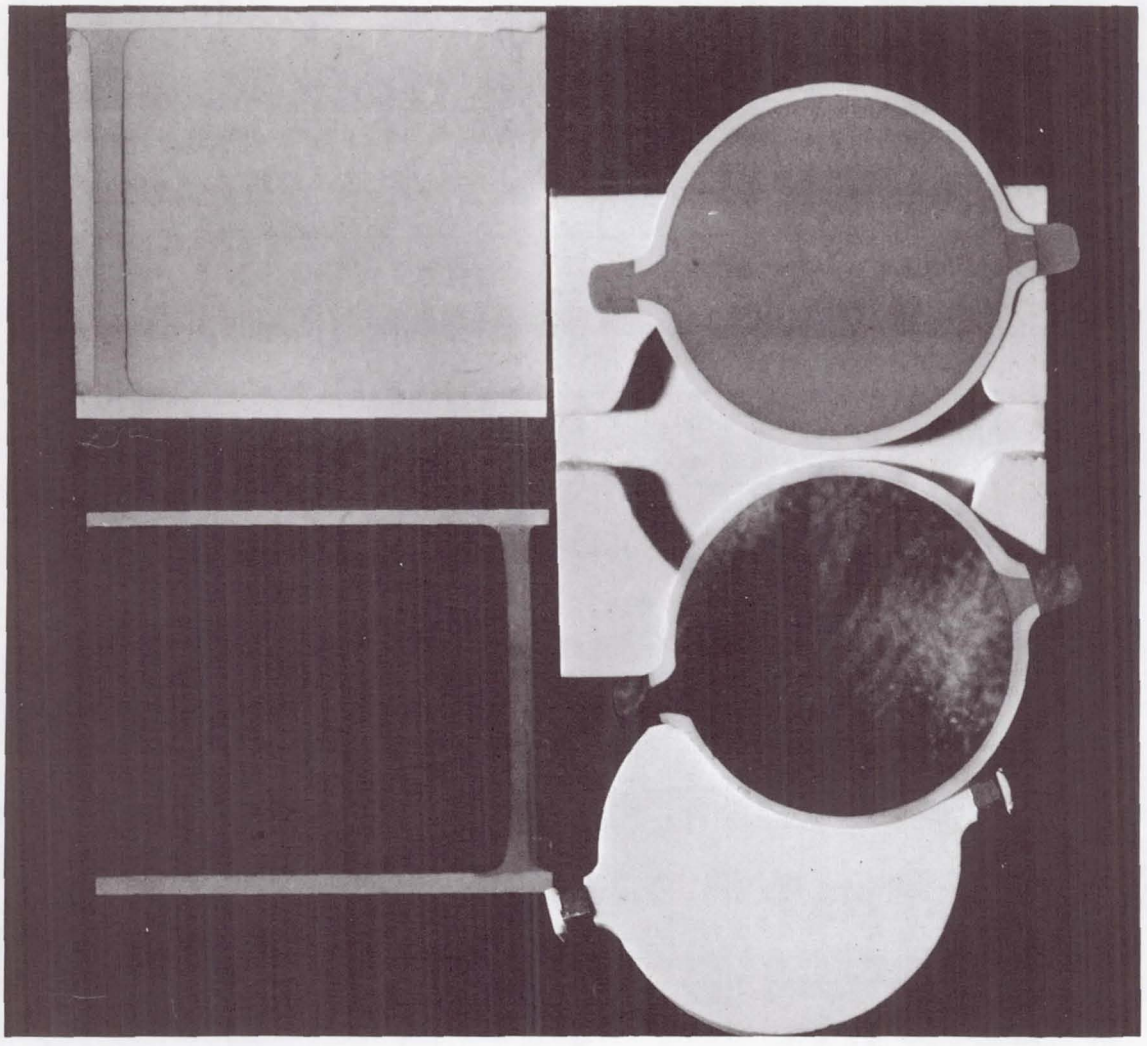


FIGURE 30. Photograph of Rectangular Capacitor Wafers and Tabbed 0.750-Inch Diameter Wafers (approximately 2½X)

TABLE 11. Characteristics of Individual Tabbed Wafers Used in Five-Wafer Multi-Layer Capacitor No. 1 and Calculated Volume Parameter $\frac{\mu F \cdot Volts}{in^3}$

Wafer No. (all polished surface)	Sputtered Electrodes				Capacitance & Tan δ at Room Temp.				Calculated Wafer Thickness $T = \frac{KA}{4.45C}$ (b)	Wafer Area (Including Tabs) (in^2)	Wafer Volume (in^3)	$\frac{\mu F \cdot Volts}{(in^3)}$ (a)
					1 kc/sec		10 kc/sec					
	Material	Sheet Resistivity (ohms/square)	Derived Thickness (ref. tab. 13)	Area (in^2)	(pF)	Tan δ	(pF)	Tan δ				
1	Rh 99.9%	0.2	2500 Å	0.364	343.177	0.000418	342.924	0.00037	0.81 mils (8.1×10^{-4} in)	0.457	3.7×10^{-4}	
2	Rh 99.9%	0.2	2500 Å	0.364	398.50	0.00052	398.034	0.00047	0.72 mils (7.2×10^{-4} in)	0.457	3.3×10^{-4}	
Wafer 1 and 2 Stacked					741.969	0.000488	741.499	0.00052				
3	Pt 99.99%	0.29	3760 Å	0.364	657.277	0.000786	656.627	0.00072	0.42 mils (4.2×10^{-4} in)	0.457	1.9×10^{-4}	
4	Pt 99.99%	0.29	3760 Å	0.364	454.581	0.000605	454.234	0.00054	0.61 mils (6.1×10^{-4} in)	0.457	2.8×10^{-4}	
5	Pt 99.99%	0.29	3760 Å	0.364	566.687	0.00108	565.901	0.00105	0.49 mils (4.9×10^{-4} in)	0.457	2.2×10^{-4}	
Wafers 3, 4, and 5 Stacked	(Measured values)				1680.74	0.000764	1678.98	0.00078				
Total 5 Wafers Stacked	(Measured values)				2434.59	0.000646	2432.42	0.00067	3.05 mils (3.05×10^{-3} in)		1.4×10^{-3}	870

(a) The $\frac{\mu F \cdot Volts}{(in^3)}$ value for the 5 wafer capacitor was calculated using the measured capacitance (2.434×10^{-3} μF), an assumed DC voltage (500V) and the total volume (1.4×10^{-3} in^3).

(b) K (dielectric constant) = 3.4 for PBN, A = electrode area (IN^2), C = measured capacitance (picofarads).

TABLE 12. Rectangular Wafer Capacitors and Electrical Data for Individual Capacitors and Multi-Layer (Stacked) Units

Wafer No.	Surface Finish	Sputtered Electrode Material	Derived Electrode Thickness (Ref. Table 13)	Electrode Area (in^2)	Average Wafer Thickness (Calculated)	Capacitance and Tan δ at Room Temperature				Comments
						1 Kc/sec		10 Kc/sec		
						Capacitance (pF)	Tan δ	Capacitance (pF)	Tan δ	
1	Matte	Rh	3900 Å	0.562	0.88 mils	486.4	0.00075	485.9	0.00075	Wafer flatness is good
2	Matte	Rh	3900 Å	0.562	1.0 mils	432.3	0.00068	431.8	0.00061	Wafer ripped during handling
3	Matte	Rh	3900 Å	0.562	0.94 mils	454.9	0.00093	454.3	0.00089	Wafer flatness is good
Unit No. 1	Measured capacitance and Tan δ of matte wafers No. 1, No. 2, and No. 3 stacked					1377.2	0.0008	1375.7	0.00092	Measurements in room ambient
	Arithmetic sum of capacitors (1 + 2 + 3):					1373.6	--	1372.0	--	
4	Polished	Rh	3200 Å	0.562	0.60 mils	715.3	0.0016	714.2	0.00087	Wafer has tendency to curl
5	Polished	Rh	3200 Å	0.562	0.68 mils	632.2	0.00109	631.4	0.00082	Same
6	Polished	Rh	3200 Å	0.562	0.78 mils	550.8	0.00086	550.3	0.00063	Same
Unit No. 2	Measured capacitance and Tan δ of polished wafers No. 4, No. 5, and No. 6 stacked					1903.9	0.00099	1901.7	0.00076	Measurements in room ambient
	Arithmetic sum of capacitors (4 + 5 + 6):					1898.3	--	1895.9	--	
Unit No. 3	Measured capacitance and Tan δ of polished and matte wafers No. 1, No. 3, No. 4, No. 5, and No. 6 stacked					2889.2	0.00072	2886.3	0.00070	Measurements in vacuum (100 microns)
	Arithmetic sum of capacitors (1 + 3 + 4 + 5 and 6 inclusive)					2839.6	--	2836.1	--	

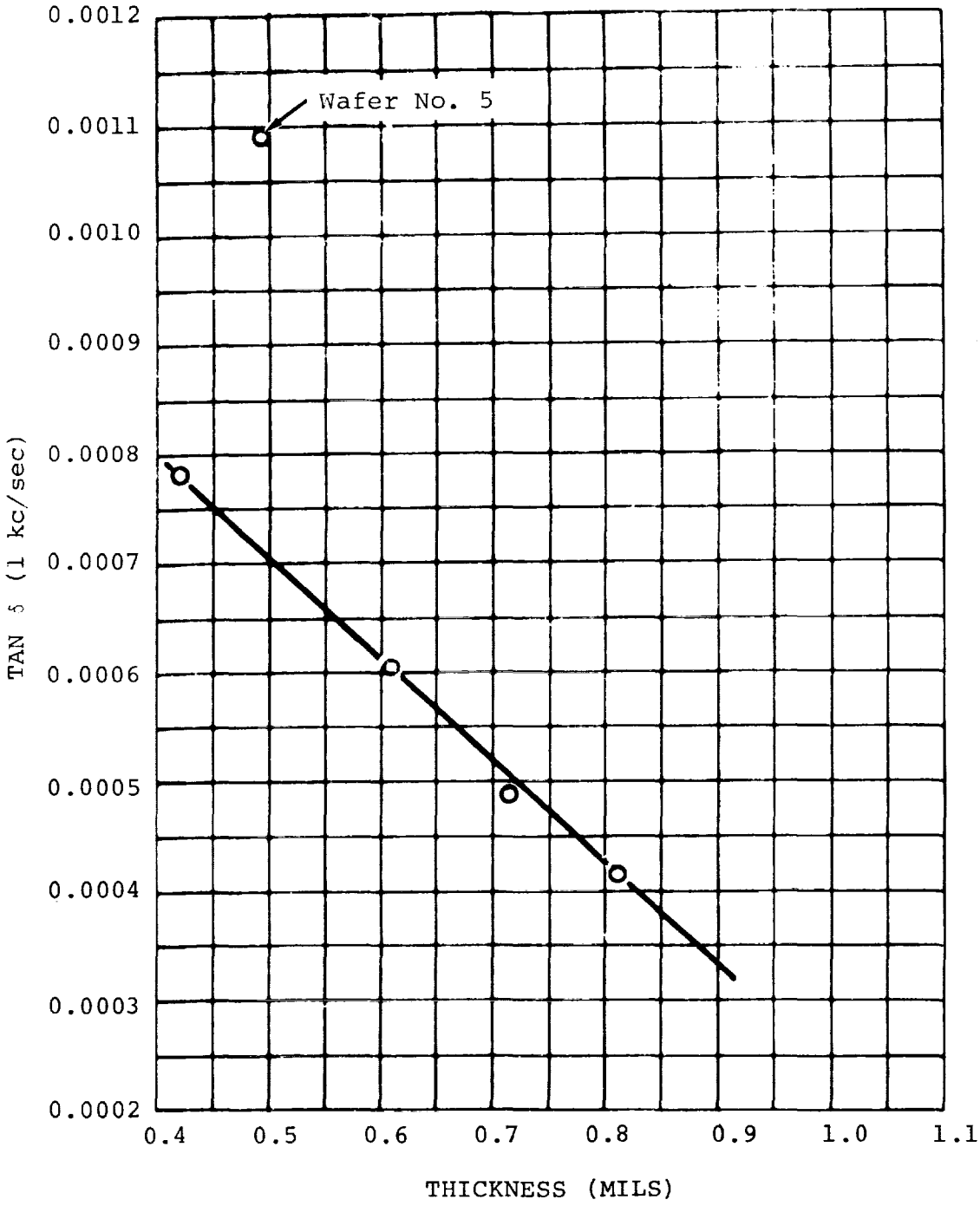


FIGURE 31. Dissipation Factor (tan δ) Versus Thickness for Tabbed Pyrolytic Boron Nitride Wafers That are Used in Five-Wafer Multi-Layer Capacitor No. 1

The data shown in table 12 for the group of rectangular wafers show that there is no significant difference in measured tan δ values of a five-stack rectangular capacitor versus a five-stack tabbed circular capacitor. (Compare data in tables 11 and 12.) In addition, the tan δ values at 1 and 10 kc/sec shown in table 12 for the rectangular capacitors are somewhat higher than the values measured for the tabbed circular capacitors shown in table 11. The reason for this is not clear, although, it may be related to the larger area of the rectangular units and the increased probability that more thin spots in the dielectric are covered by the electrodes.

Under the comments column in table 12, it is noted that the polished wafers with sputtered electrodes have a tendency to curl particularly at the edges where the electrode overlap occurs. The overall flatness of wafers with matte surfaces, however, is much improved.

The data obtained indicates that the surface finish of rectangular wafers might have a greater effect on measured tan δ values at frequencies higher than 1 kc/sec compared to the differences in geometry and interconnection area. For example, table 12 shows tan δ values at 1 and 10 kc/sec for a three-wafer stacked capacitor consisting of all wafers with polished surfaces. In the latter case (unit No. 2, table 12), tan δ decreases from 0.00099 at 1 kc/sec to 0.00076 at 10 kc/sec; whereas, with matte wafers (unit No. 1, table 12) tan δ increases at 10 kc/sec indicating higher contact resistance.

These measurements were made with a 200-gram weight on top of the stack and in room ambient conditions (72° F). Table 12 also shows tan δ values for a five-wafer stack consisting of a mix of matte and polished wafers (wafers Nos. 1, 3, 4, 5 and 6) but measured in vacuum (100 microns) and at higher clamping pressures. In this case tan δ is about the same at 1 kc/sec and 10 kc/sec. The results would indicate that the contact resistance was lowered in vacuum and by the higher clamping pressure.

Because of the problems connected with the rectangular wafers (more difficult to fabricate and generally poorer electrical properties compared to the round tabbed geometry), it was decided to continue all further work with tabbed wafers only.

(2) Thickness Control of Sputtered Electrodes

A series of tests were made on pure platinum and rhodium films sputtered onto 2- by 2-inch and 3- by 3-inch glass squares (Corning 7059) and film thickness was measured by several different methods. The sputtering conditions are shown in table 13 for a total argon pressure of approximately one micron. Measurements were made on these sputtered films as follows:

a) Film resistance was measured by diamond scribing electrically isolated strips with length-to-width ratios of about 15. The strip resistance was measured using a constant current source (battery) and the voltage drop was determined across a known length with a electrometer. The sheet resistivity in ohms/square was calculated from the length-to-width ratio.

b) Film thickness was measured with a multiple beam microinterferometer attachment to a Unitron Series N Metallograph. This device uses a cadmium light filter and generates interference fringes with a separation of $\frac{\lambda}{2}$(λ=6440 Å).

c) The overall film thickness was measured for the platinum film using before and after weight determinations and calculating the thickness from the substrate area and density of platinum.

d) A two-point probe (0.1-inch spacing) connected to an ohmmeter was lightly pressed on the film surfaces and the measured probe resistance was correlated with the sheet resistances determined by a) and b) above. The results obtained were as follows:

Platinum (99.95%)

1) Strip Resistance Measurements - 0.430 ohms/square sheet resistivity equivalent to a 2560 Å-thick film based on a bulk resistivity value of 10.8×10^{-6} ohm-cm at room temperature.

2) Interferometer measurement - 3200 Å

3) Weight determination - 5540 Å

TABLE 13. Sputtering Data Used to Derive Electrode Thickness for Tabbed Wafers (Five-Wafer Multi-Layer Capacitor No. 1)

Substrate	Target Material (Electrode)	Target Size Spacing 1-1 4"	Sputtering Voltage (VDC)	Total Target Area (cm^2)	Target Current (average)	Target mA/cm^2 (average)	Total Sputtering Time (min)	Specific Rate $\left(\frac{mA}{cm^2 \cdot min}\right)$	Measured Film[a] Thickness (Å)	Measured Deposition Rate (Å/min)	Derived Deposition Rate (Å/min)	Derived Film Thickness (Å)
Tabbed No. 3 (Polished)	Pt	Two 3"x3" Sheets	900	116	105mA	0.905	41	0.022	--	--	91.8	3760
Tabbed No. 4 (Polished)	Pt	Two 3"x3" Sheets	900	116	105mA	0.905	41	0.022	--	--	91.8	3760
Tabbed No. 5 (Polished)	Pt	Two 3"x3" Sheets	900	116	105mA	0.905	41	0.022	--	--	91.8	3760
Tabbed No. 1 (Polished)	Rh	One 3"x3" Sheet	900	58	50mA	0.863	25 ea. side	0.0345	--	--	101.1	2500
Tabbed No. 2 (Polished)	Rh	One 3"x3" Sheet	900	58	50mA	0.863	25 ea. side	0.0345	--	--	101.1	2500
STANDARD 3"x3" glass Square-Corning 7059	Rh	One 3"x3" Sheet	900	58	25mA	0.430	60	0.00717	1270	21	--	--
STANDARD 2"x2" glass Square-Corning 7059	Pt	One 3"x3" Sheet	900	58	40mA	0.690	60	0.0115	2890	48	--	--

(a) Measured film thickness is the average of multiple beam interferometer measurement and thickness determined from strip resistance.

(b) Nominal argon pressure - 1_{μ}.

Rhodium (99.9%)

1) Strip resistance measurements - 0.387 ohms/square sheet resistivity equivalent to 1290 Å-thick film based on a bulk resistivity value of 4.98×10^{-6} ohm-cm.

2) Interferometer - 1250 Å

These data show that lower ohms/square values can be obtained with rhodium films that are about one-half as thick as platinum. This is in general agreement with the differences in bulk resistivity. Values (ref. 5) for the bulk resistivity of rhodium and platinum at 930° F (14.6×10^{-6} and 27.9×10^{-6} ohm-cm respectively) show that the resistance of platinum is about two times greater than rhodium. For the same thickness electrodes, therefore, rhodium films should make the least contribution to measured capacitor losses over the temperature range from room temperature to 1100° F.

The variation in the thickness of the platinum film over the entire area of the 2- by 2-inch substrate was estimated by using the two-probe method outlined above. Figure 32 shows a plot of measured probe resistance versus ohms/square values obtained by measuring strip resistances. This curve is not precise but it does give an approximate value of film thickness or sheet resistivity from measured probe resistances. This permits very rapid and simple tests to be made particularly for comparative purposes. On this basis the platinum film thickness varied from approximately 3600 Å to 2700 Å. The maximum thickness was recorded at the lower edge of the substrate. The target used was 3- by 3-inches square and the target to substrate distance was 1-1/4 inches. A larger target area in relation to the substrate area would be one way to minimize thickness variations.

Table 13 shows how the electrode thickness was derived from the sputtering data. The basis for these calculations are the sputtering conditions (sputtering voltage, target area, target current, and sputtering times) recorded during the deposition of rhodium and platinum films on 3- by 3-inch and 2- by 2-inch glass substrates. The thickness of these films measured with an interferometer and calculated from strip resistance measurements was averaged and a deposition rate of 21 Å/min for platinum determined. These values are shown in table 13 together with values for the target current per unit area and time (ma/cm^2-min). Similar deposition rate

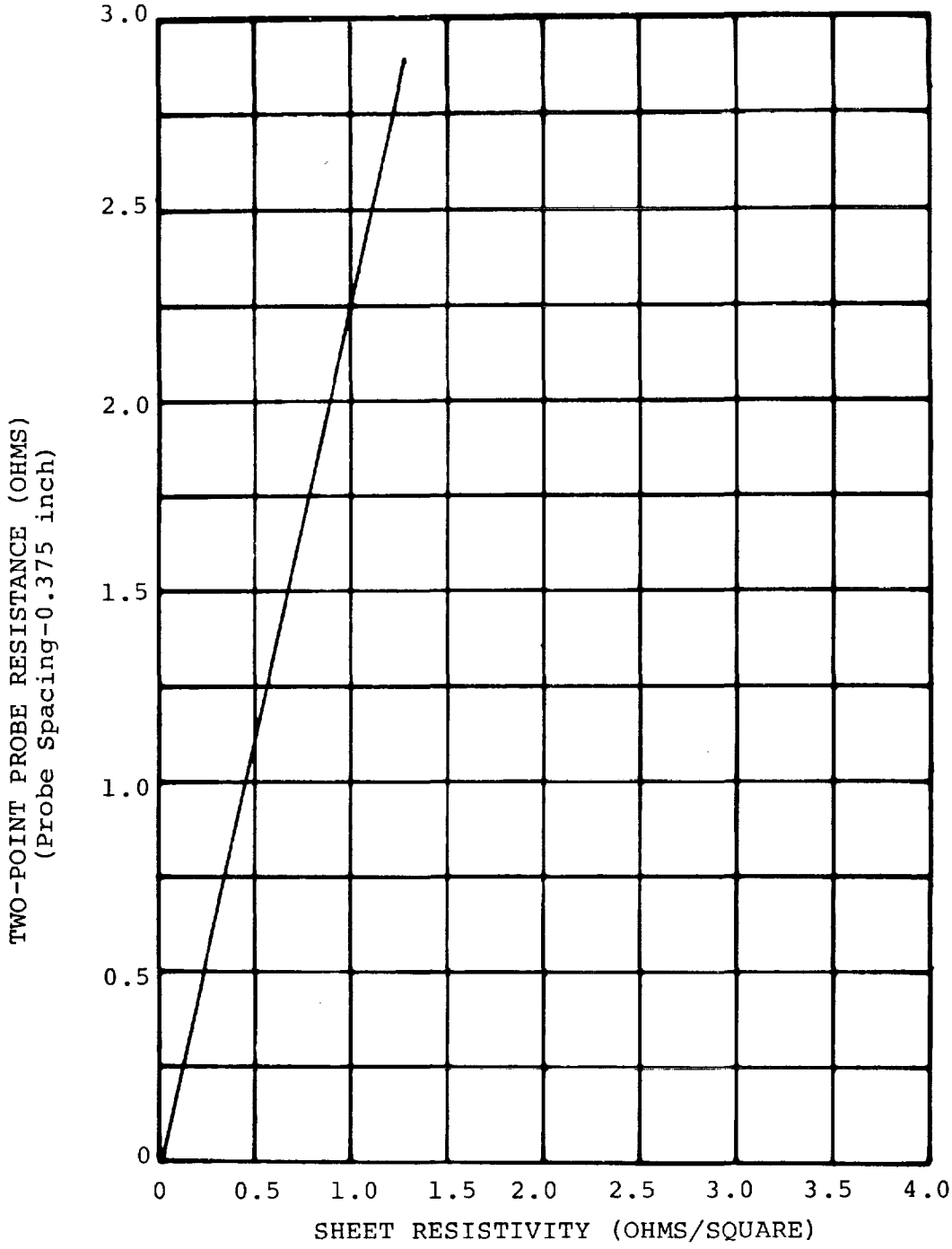


FIGURE 32. Two-Point Probe Resistance Versus Sheet Resistivity

for rhodium was obtained which, when multiplied by the total sputtering time, gives the derived film thickness shown in tables 11 and 12 for tabbed rectangular wafer capacitors.

(3) Electrical Measurements to 1100° F in Vacuum (Five-Layer Capacitor)

The five wafers shown in table 11 were stacked in the pyrolytic boron nitride fixture (figure 27) and capacitance, dissipation factor (tan δ), and d-c resistance was measured in vacuum (~3 x 10^{-7} torr) to 1100° F. Figures 33 and 34 show the complete capacitance and tan δ envelopes versus temperature for seven different frequencies from 50 cps to 50 kc/sec.

Figure 35 shows tan δ versus temperature for one selected frequency (1 kc/sec) during heating and cooling. It is evident that compared to the sapphire, BeO, and Lucalox capacitors discussed previously, very little dielectric after-working or hysteresis occurred.

A number of d-c resistance measurements were made during heating and cooling to and from 1100° F. These data were combined with capacitance and plotted as RC products (megohms x microfarads) versus temperature in figure 36. Also shown in figure 36 are a number of single points quoted by G. Dummer (ref. 6) for Teflon (350° F), mica (670° F), Mylar (300° F), and vitreous enamel (200° F) capacitors. It is clearly shown that the PBN capacitor has several orders of magnitude better RC values over a very wide temperature range.

B. ENDURANCE TESTS AT 1100° F IN VACUUM

1. Nine-Wafer Capacitor

A total of 12 PBN tabbed wafers with polished surfaces and rhodium electrodes (1500 to 2000 Å thickness) were completed for life testing. Wafer thicknesses ranged from 0.5 to 1.0 mil. Nine of these wafers were selected for multi-layer test capacitors after screening at 1000 Vd-c. Evaluation data for each of the nine wafers in this unit is shown in table 14.

The nine-wafer capacitor was placed on life test in a sputter-ion pumped, cold-wall vacuum furnace (R. D. Brew & Co., Inc.,). The test fixture and test equipment used was the same as that described previously. The vacuum furnace was evacuated to the 10^{-8} torr range and capacitance, tan δ, and d-c resistance (at 500 Vd-c) was measured at room temperature. Furnace power was applied, the temperature stabilized

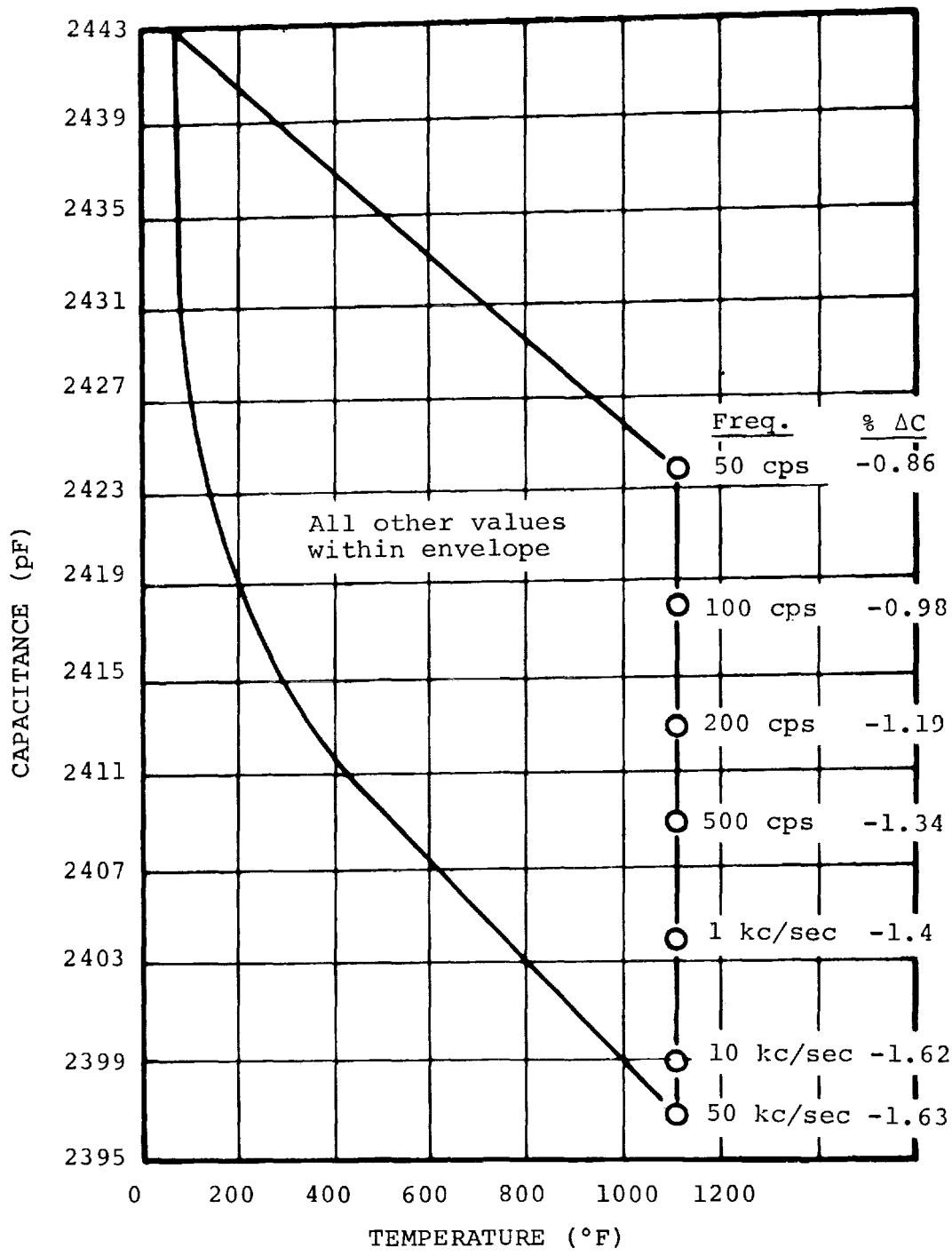


FIGURE 33. Capacitance Versus Temperature Envelope Including Seven Different Frequencies from 50 cps to 50 kc/sec for a Five-Wafer Pyrolytic Boron Nitride Multi-Layer Capacitor No. 1 (Measured in Vacuum at $<3 \times 10^{-7}$ torr)

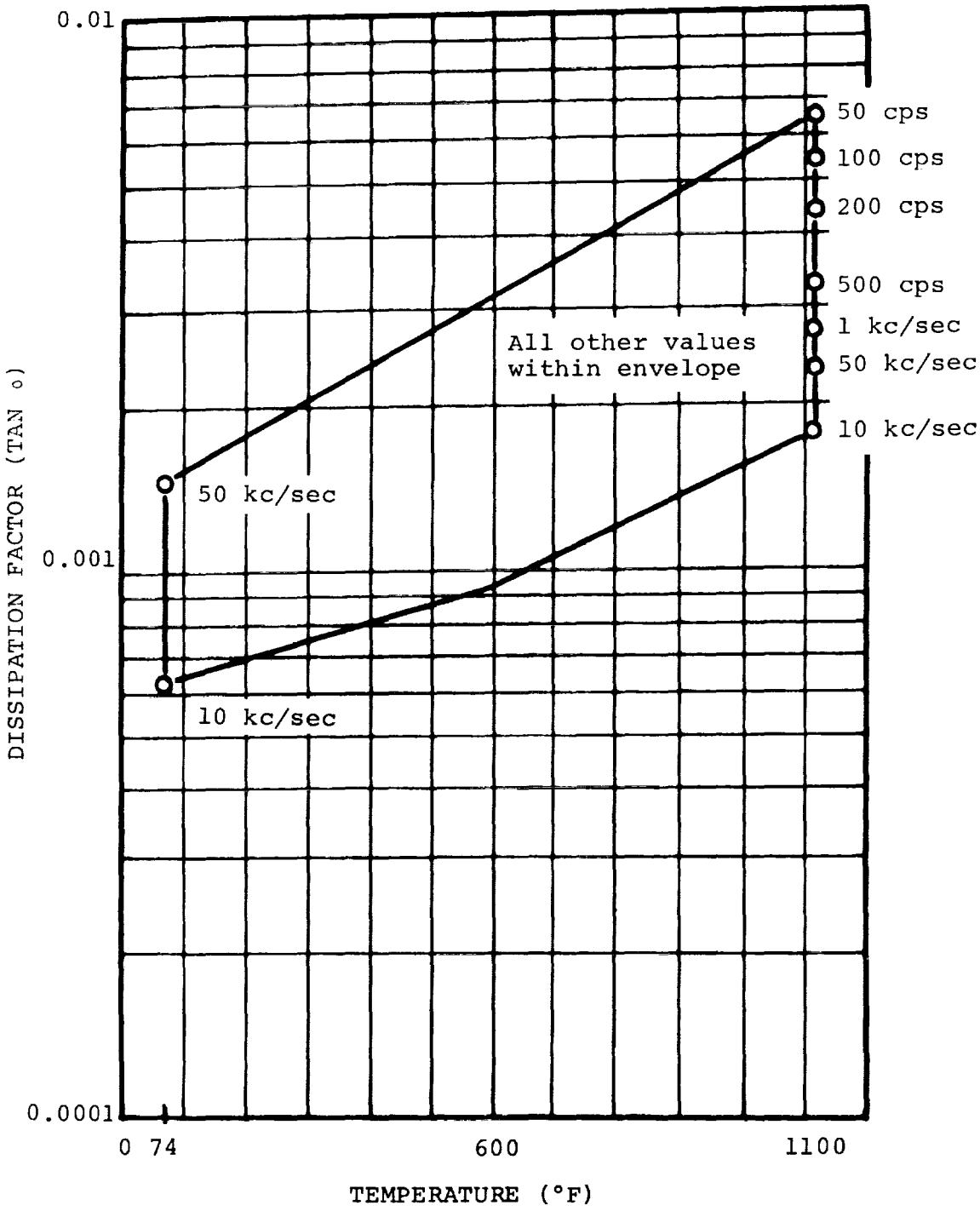


FIGURE 34. Dissipation Factor (tan δ) Versus Temperature Envelope Including Seven Different Frequencies from 50 cps to 50 kc/sec for Five-Wafer Pyrolytic Boron Nitride Multi-Layer Capacitor No. 1 (Measured in Vacuum at $<3 \times 10^{-7}$ torr)

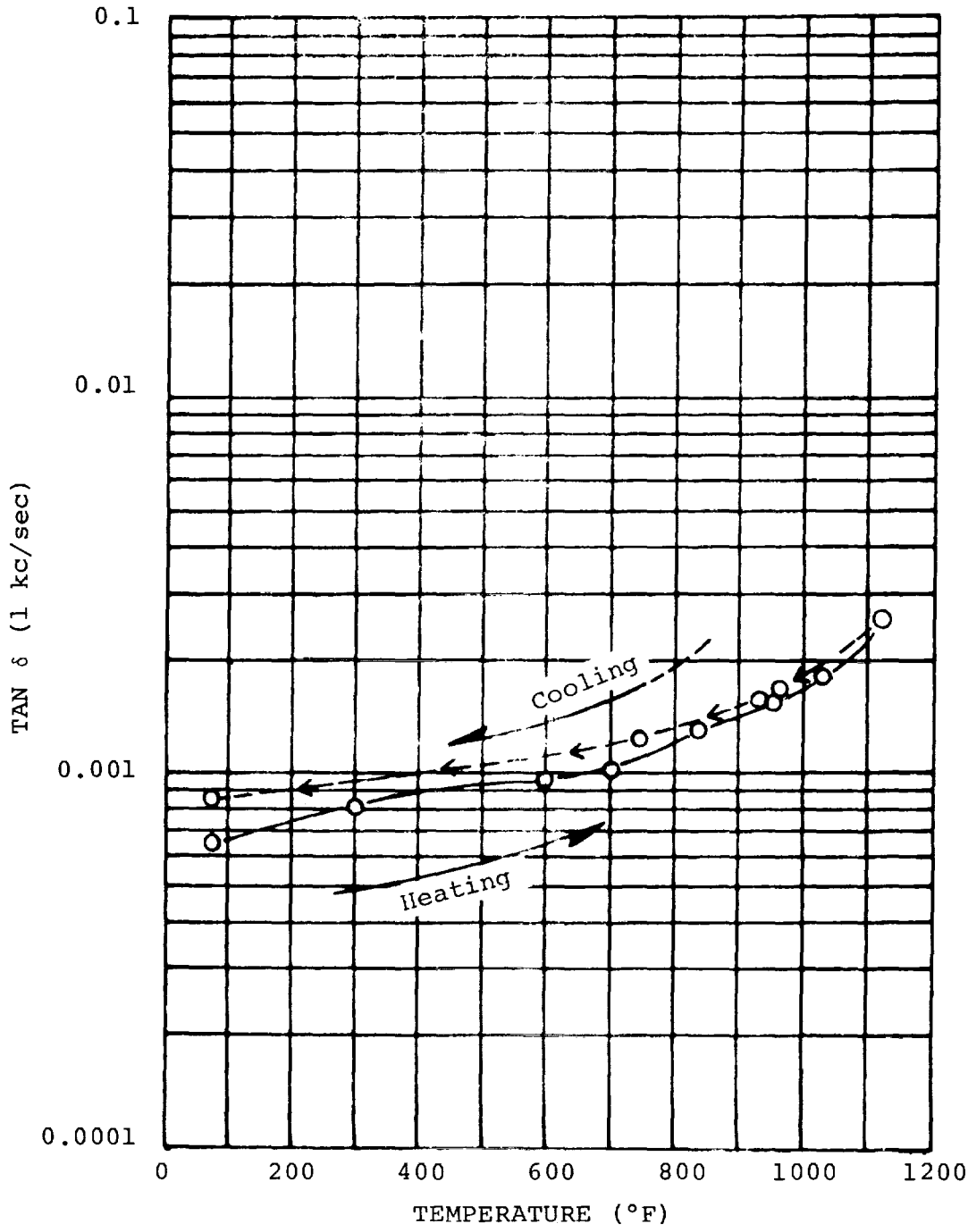


FIGURE 35. Dissipation Factor (tan δ) Versus Temperature Measured During Heating and Cooling to Room Temperature for Five-Wafer Pyrolytic Boron Nitride Multi-Layer Capacitor No. 1

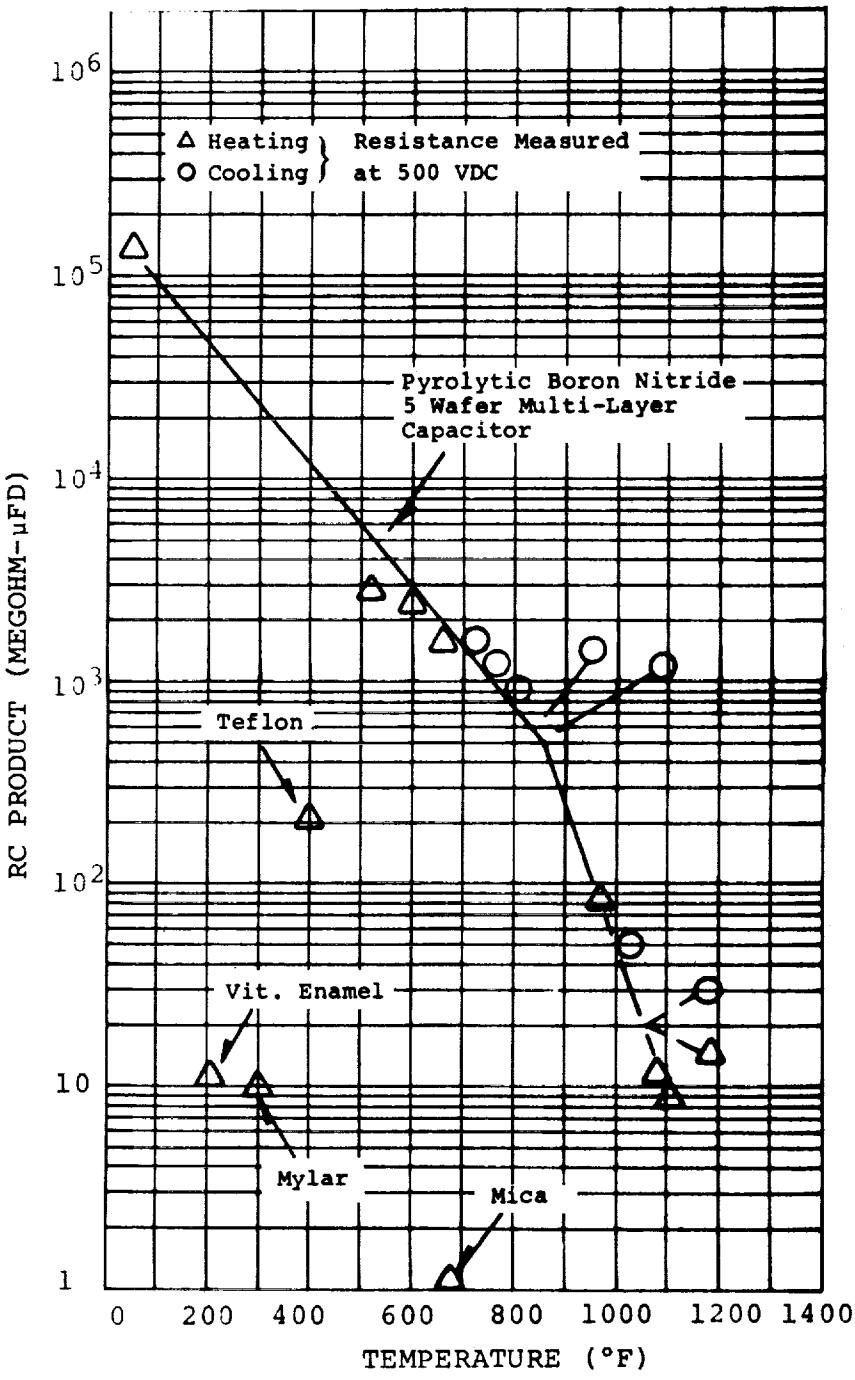


FIGURE 36. RC Product (Megohm x Microfarad) Versus Temperature for Five-Wafer Pyrolytic Boron Nitride Multi-Layer Capacitor No. 1 (Measured at 500 Vdc at Pressures less than 3×10^{-7} torr)

TABLE 14. Evaluation Data for Individual Wafers in the Nine-Wafer Pyrolytic Boron Nitride Capacitor With Sputtered Rhodium Electrodes

Tabbed Wafer No.	Electrode[a] Thickness (rhodium)	Wafer Surface Finish	Calculated Wafer Thickness[b] (mils)	Capacitance (pF) & Tan δ at Room Temperature				1000 V DC Test Applied For One Minute	Voltage Stress at 500 V DC (volts/mil)
				1 kc/sec		10 kc/sec			
				pF	Tan δ	pF	Tan δ		
1	1500-2000Å	Polished	0.94	296.76	0.00067	296.51	0.00049	Pass	532
2	1500-2000Å	Polished	0.91	305.95	0.00095	305.61	0.00068	Pass	550
3	1500-2000Å	Polished	1.0	277.98	0.00059	277.79	0.00041	Pass	500
4	1500-2000Å	Polished	0.71	389.89	0.00028	389.75	0.00024	Pass	704
5	1500-2000Å	Polished	0.50	556.01	0.00082	555.49	0.00079	Pass	1000
6	1500-2000Å	Polished	0.71	390.22	0.00068	389.89	0.00058	Pass	704
7	1500-2000Å	Polished	0.73	381.04	0.00048	380.81	0.00043	Pass	685
8	1500-2000Å	Polished	0.82	340.52	0.00071	340.21	0.00054	Pass	610
9	1500-2000Å	Polished	0.55	504.25	0.00057	503.87	0.00097	Pass	910

(a) Estimated from sputtering data using the relationship (derived): (Refer to Table 13)

$T \approx \frac{j}{k}$; T = electrode thickness (angstroms)
j = average measured target current density (ma/cm^2)
k = experimentally determined constant for different target materials:
Platinum - 2.39×10^4 $ma/cm^2/Å$
Rhodium - 3.38×10^{-4} $ma/cm^2/Å$

(b) From the relationship:

$T = \frac{KA}{4.45C}$; T = thickness (inches)
K = dielectric constant (3.4) - Source: "Boralloy" Data Sheet, "C" direction at 4×10^9 cps
A = electrode area (0.364 in^2)
C = measured capacitance (pF at 1 kc/sec)

at approximately 1100° F, and another set of electrical measurements were made. These data and the data subsequently recorded at various time intervals are shown in table 15.

These data show that after an initial short circuit (estimated at about 19 hours on test) and vaporization of electrode material, a higher tan δ value and lower d-c resistance was obtained (compared to values before the short). It is also believed that six of the wafers became electrically isolated leaving three wafers interconnected. After 66 hours at 500 Vd-c the measured tan δ value shows a decrease but the d-c resistance also decreased; however, just before terminating the test at 162 hours, measurements showed a further decrease in tan δ and an increase in the d-c resistance.

It is indicated from these results that 500 volts per mil is probably a satisfactory stress level for wafers in the one-mil thickness range. Two of the wafers in this unit had thicknesses of about 0.5-mil (refer to table 14) and were, therefore, stressed at about 1000 volts per mil (apparently on excessive stress level for wafers in this thickness range). When the capacitor stack was examined after the test, it was not possible to determine which wafers or wafer caused the initial short circuit because several of the wafers were bonded together via their electrodes. The rhodium electrodes could be peeled from some of the wafers indicating the initial electrode/wafer interfacial bond was lost. The two outer electrodes on the top and bottom wafers in the stack did not show a loss of adherence, presumably because they were not in contact with an electrode of another wafer but with the surfaces of the boron nitride fixture.

2. Five-Wafer Capacitor

Another group of tabbed wafers (changed conductor from rhodium to platinum) were prepared and the following modifications were made based on the results of the nine-wafer unit:

a) Wafer thickness was maintained in the one-mil range to decrease the probability of a short circuit induced by a defect.

b) Wafer surfaces were not polished. Electrodes were sputtered on "as lapped" or matte surfaces. This is intended to increase the effective electrode adherence and minimize the contact area between two electrodes on different wafers.

c) A double thickness of electrode material (platinum) was sputtered on the tab extensions only to

TABLE 15. Life Test Data - Nine-Wafer Pyrolytic Boron Nitride Capacitor With Sputtered Rhodium Electrodes

Elapsed Time at 500 V DC	Furnace Temp. (°F)	Pressure (torr)	Capacitance & Tan δ (Rhodium Electrodes)								DC Resistance [ohms at 500 V DC]	RC Product [megohms x microfarads]
			100 cps		1 kc/sec		10 kc/sec		50 kc/sec			
			pF	Tan δ	pF	Tan δ	pF	Tan δ	pF	Tan δ		
Room Temp.	75	$1x10^{-8}$	3451.3	0.0005	3448.7	0.00046	3447.2	0.00058	3448.8	0.00155	$5x10^{13}$	$1.72x10^{5}$
Start	1112	$2x10^{-8}$	3423.0	0.005	3402.9	0.0035	3389.2	0.0026	3384.5	0.0034	$2.38x10^{9}$	8.1
19 Hours (Approx.) (Short Circuit)	1113				897.66	0.0236	890.11	0.0062			$3.13x10^{9}$	2.3
25 Hours	1112	$2.0x10^{-8}$			898.03	0.0162	890.32	0.0055			$1.25x10^{8}$	0.112
66 Hours	1115	$7.5x10^{-9}$	911.3	0.058	897.03	0.0161	890.04	0.0050			$1.47x10^{7}$	0.013
162 Hours	1114	$4x10^{-9}$	906.8	0.029	896.67	0.0095	889.70	0.0042			$2.0x10^{7}$	0.018

decrease the contact resistance between interconnecting electrodes.

d) Platinum was selected for the electrodes because of its greater ductility and lower Young's Modulus (versus rhodium).

Table 16 shows the thickness of each wafer in the five-wafer unit, capacitance and tan δ at 1 kc/sec and 10 kc/sec, and the voltage stress on each capacitor wafer when connected in parallel with 500 V dc applied.

Table 17 shows tan δ values at several frequencies for the five-wafer stacked unit. The slight increase in tan δ at 10 kc/sec indicates that the double thickness of platinum on the tabs is effective in reducing the contact resistance (effective series resistance) to a value comparable to that obtained with polished wafers and the lower resistivity rhodium electrodes (tables 14 and 15).

a. RESULTS AFTER 259 HOURS AT 500 V DC/MIL

The five-wafer unit was placed on life test at 1100° F using the same conditions, procedures and equipment previously described for the nine-wafer capacitor. Figure 37 shows the change in capacitance as a function of time. The total change was only 1.39 percent for the 259-hour period. The greatest part of this change (1.1%) occurred during the first 65 hours. Table 17 shows the values recorded for tan δ and d-c resistance (shown as an RC product) at indicated furnace temperatures ranging from 1100° to 1117° F.

The variation in furnace temperature was apparently due to changes in line voltage for a pre-set voltage input. This method of control was necessary because of a malfunction in the automatic furnace controller that developed during the early part of the test.

Table 17 shows that tan δ increased and the RC product also increased (decrease in conductivity) over the 259-hour period. Thus, the a-c losses increased but the d-c losses decreased. These effects are discussed in detail in section III.B.2.b.

b. RESULTS AFTER 861 ADDITIONAL HOURS AT 750 AND 1000 V DC/MIL

(1) Change in Capacitance, Tan δ, and DC Resistance

Figures 38 to 43 show a complete presentation of all the electrical data obtained during the extended

TABLE 16. Evaluation Data for Individual Wafers Used in the Five-Wafer Pyrolytic Boron Nitride Capacitor (1120-Hour Life Test)

Tabbed Wafer No.	Electrode[a] Thickness (platinum)	Wafer Surface Finish	Calculated Wafer Thickness[b] (inches)	Capacitance (pF) & Tan δ at Room Temperature				1000 V DC Test Applied For One Minute	Voltage Stress at 500 V DC (volts/mil)
				1 kc/sec		10 kc/sec			
				pF	Tan δ	pF	Tan δ		
1	3500-4000Å	Matte or as lapped	0.00085 (0.85 mils)	326.17	0.00094	325.75	0.00085	Pass	588
2	3500-4000Å	Matte or as lapped	0.0010 (1 mil)	277.86	0.00127	277.39	0.00108	Pass	500
3	3500-4000Å	Matte or as lapped	0.0011 (1.1 mils)	253.54	0.00115	253.14	0.00104	Pass	454
4	3500-4000Å	Matte or as lapped	0.00103 (1.03 mils)	269.19	0.00071	268.93	0.00071	Pass	486
5	3500-4000Å	Matte or as lapped	0.00094 (0.94 mils)	295.01	0.00098	294.61	0.00093	Pass	532

(a) Estimated from sputtering data using the relationship (derived): **(Refer to Table 13)**

$T \approx \frac{j}{k}$; T = electrode thickness (angstroms)
j = average measured target current density (ma/cm^2)
k = experimentally determined constant for different target materials:
Platinum – 2.39×10^4 ma/cm^2/Å
Rhodium – 3.38×10^{-4} ma/cm^2/Å

(b) From the relationship:

$T = \frac{KA}{4.45C}$; T = thickness (inches)
K = dielectric constant (3.4) - Source: "Boralloy" Data Sheet, "C" direction at 4×10^9 cps
A = electrode area (0.364 in^2)
C = measured capacitance (pF at 1 kc/sec)

TABLE 17. Two Hundred and Fifty Hour Life Test Data - Five-Wafer Boron Nitride Capacitor

Elapsed Time at 500 V DC	Furnace Temp. (°F)	Pressure (torr)	Capacitance (pF) & Tanδ										DC Resistance (ohms at 500 V DC)	RC Product (megohms x microfarads)
			200 cps		500 cps		1 kc/sec		10 kc/sec		50 kc/sec			
			pF	Tanδ	pF	Tanδ	pF	Tanδ	pF	Tanδ	pF	Tanδ		
Room Temp.	75	2.6×10^{-7}	1423.66	0.00058	1423.2	0.00055	1422.85	0.00058	1421.75	0.00064			1.66×10^{14}	2.36×10^{5}
Start	1111	4×10^{-7}	(a)	(a)	1382.50	0.0030	1381.39	0.00231	1378.77	0.0012	1377.9	0.0015	1.06×10^{10}	14.7
71 Hours	1104	1.6×10^{-8}											1.25×10^{10}	17.3
89 Hours	1109	1.4×10^{-8}											1.09×10^{10}	15.0
111 Hours	1110	1.4×10^{-8}											1.47×10^{10}	20.3
139 Hours	1114	1.2×10^{-8}	(a)	(a)	1367.1	0.0036	1365.6	0.0028	1362.27	0.0014			0.8×10^{10}	10.6
159 Hours	1117	1.2×10^{-8}											0.7×10^{10}	9.5
189 Hours	1100	1.2×10^{-8}											1.43×10^{10}	19.5
219 Hours	1099	1.2×10^{-8}											1.82×10^{10}	24.8
259 Hours	1100	1.1×10^{-8}	(a)	(a)	1365.2	0.0031	1363.3	0.0024	1360.4	0.0013	1359.6	0.0016	1.77×10^{10}	24.4

(a) A satisfactory null could not be obtained at a test frequency of 200 cps or less at 1100°F

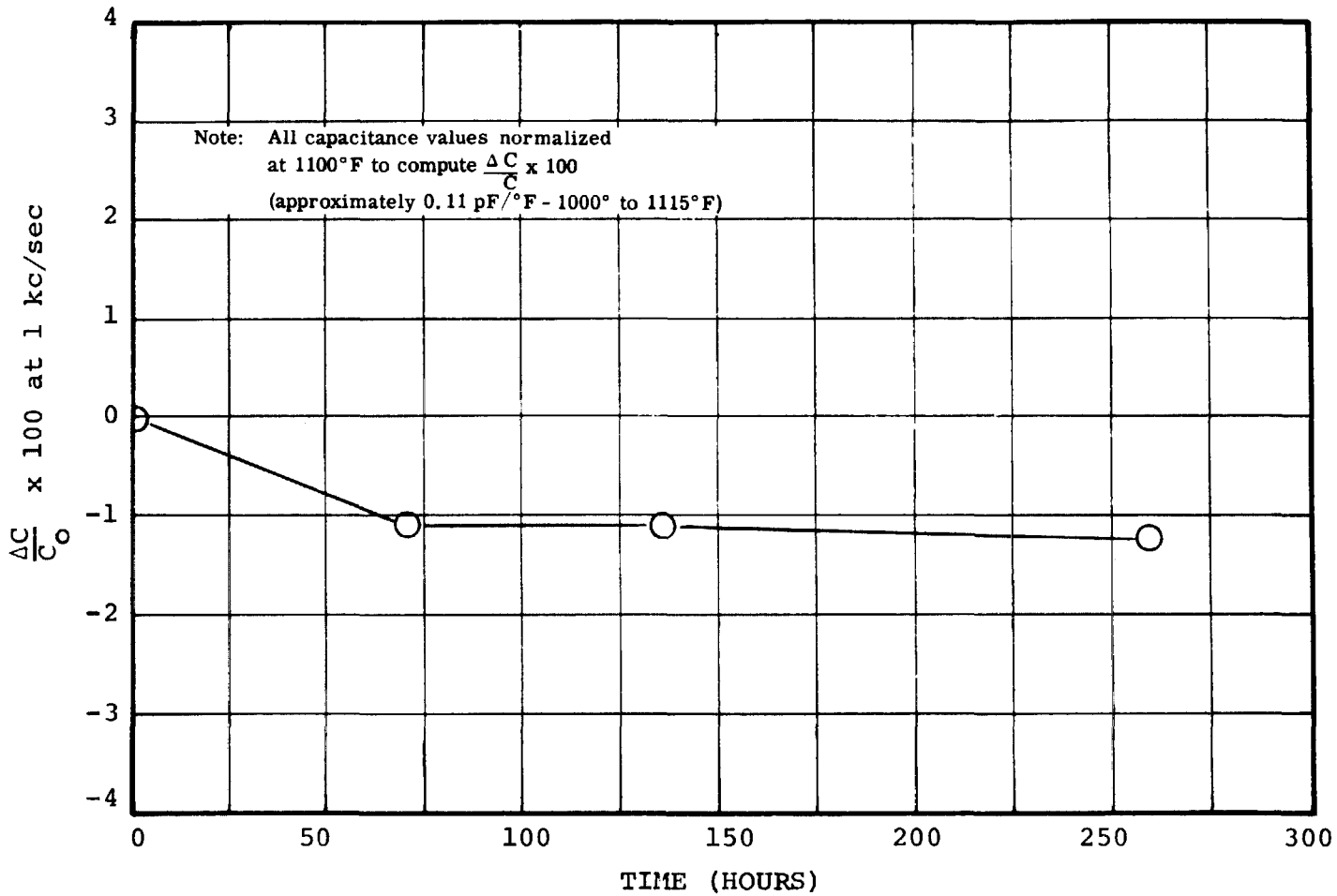


FIGURE 37. Change in Capacitance versus Time at 500 Volts/mil in Vacuum (4×10^{-7} to 1.1×10^{-8} torr) at 1100° F for a Five-Wafer Pyrolytic Boron Nitride Capacitor with Sputtered Platinum Electrodes

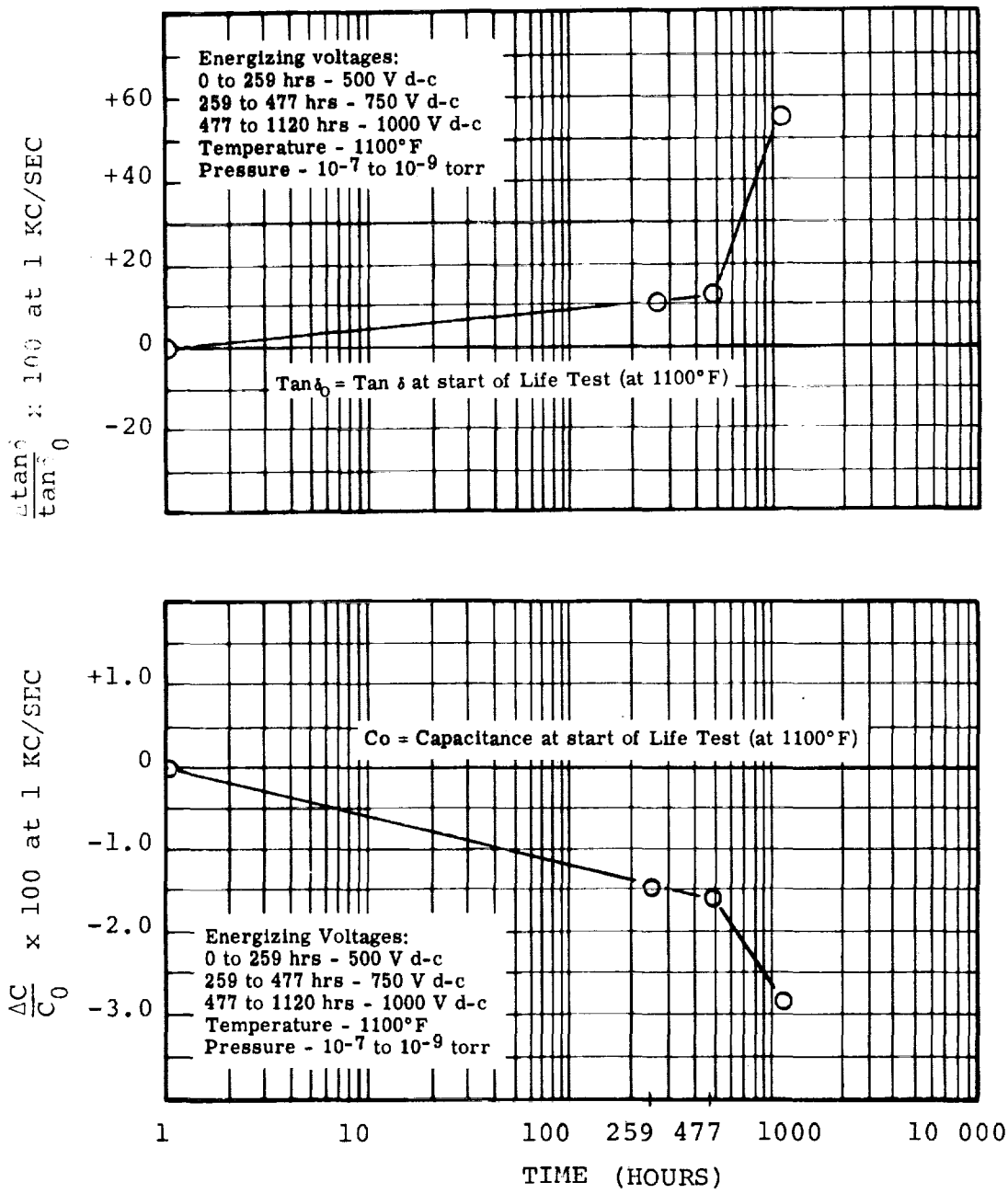


FIGURE 38. Change in the Ratios of $\frac{\Delta \tan \delta}{\tan \delta_0}$ x 100 and $\frac{\Delta C}{C_0}$ x 100 as a Function of Time and Increased DC Energizing Voltages for a Five-Wafer Multi-Layer Pyrolytic Boron Nitride Capacitor with Sputtered Platinum Electrodes in Vacuum at 1100° F

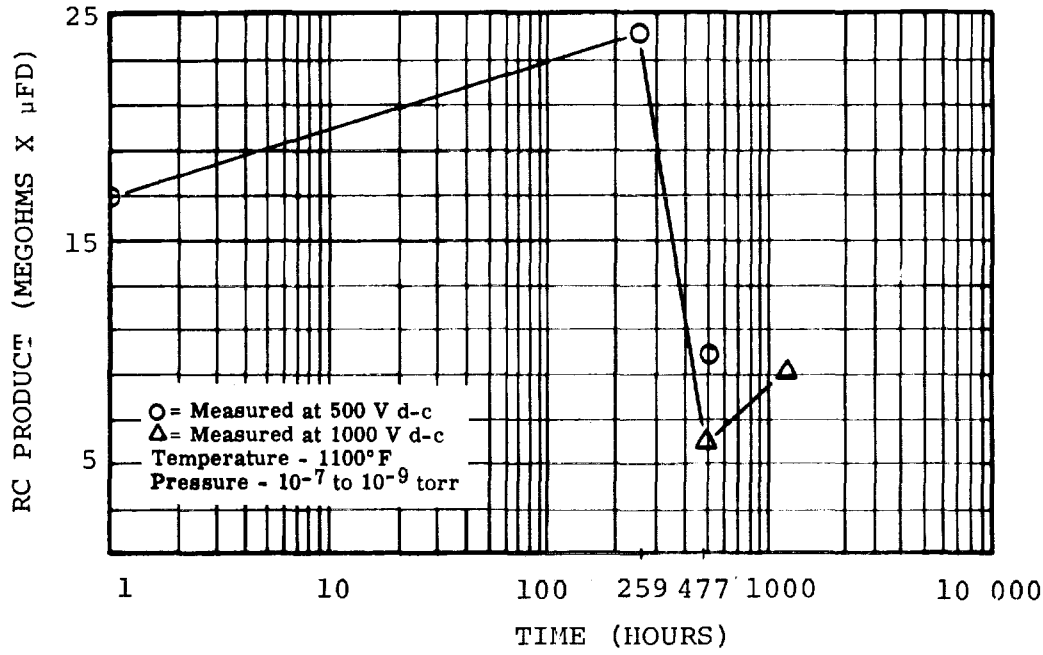


FIGURE 39. Change in RC Product (Megohms x Microfarads) as a Function of Time and Increased DC Energizing Voltages for a Five-Wafer Multi-Layer Pyrolytic Boron Nitride Capacitor with Sputtered Platinum Electrodes in Vacuum at 1100° F

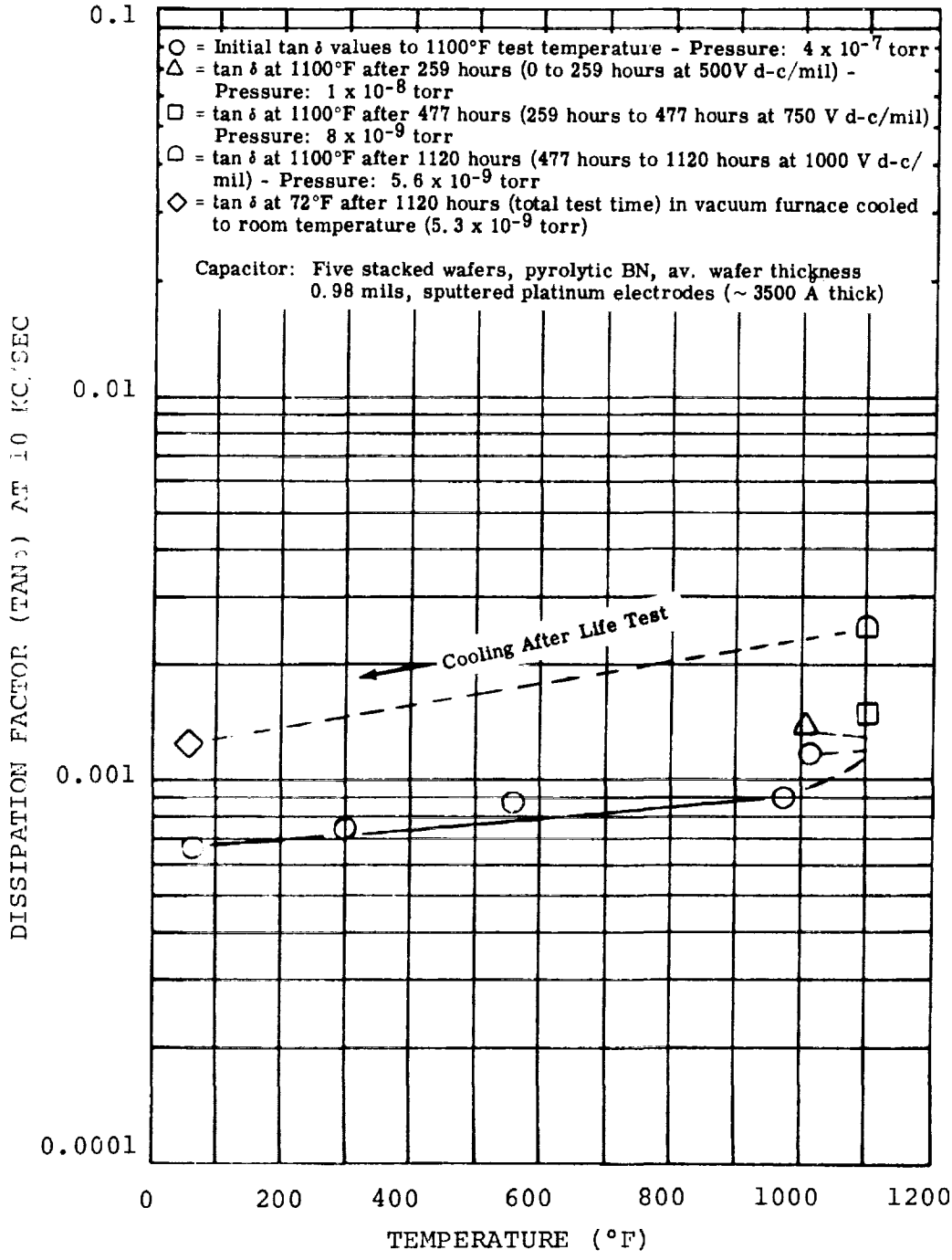


FIGURE 40. Dissipation Factor (tan δ) Versus Temperature and Change in (tan δ) Versus Time and Increased DC Energizing Voltages at Constant Temperature (1100°F) in Vacuum for a Five-Wafer Multi-Layer Pyrolytic Boron Nitride Capacitor with Sputtered Platinum Electrodes

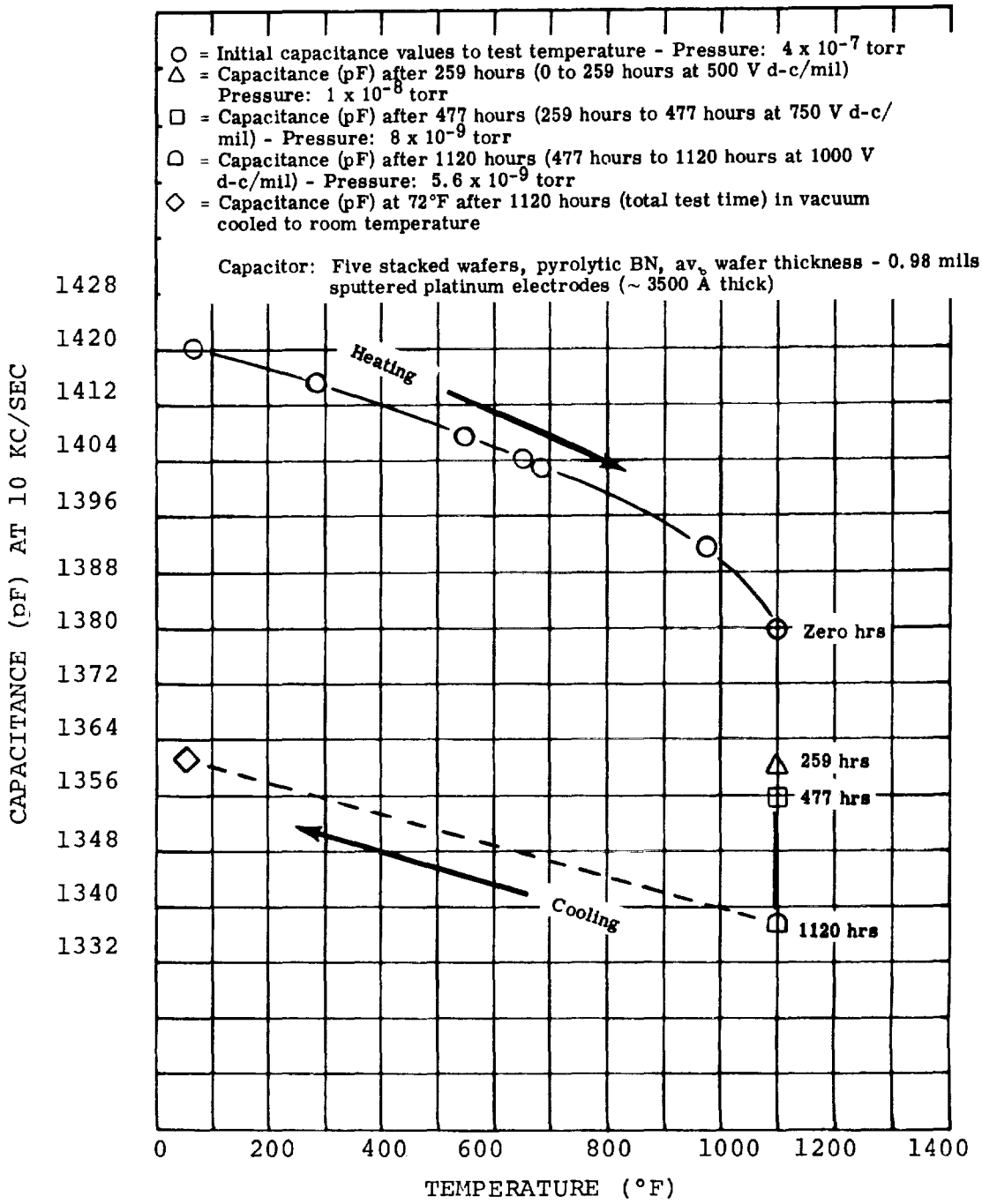


FIGURE 41. Capacitance Versus Temperature and Time at Increased DC Energizing Voltages at Constant Temperature (1100°F) in Vacuum for a Five-Wafer Multi-Layer Pyrolytic Boron Nitride Capacitor with Sputtered Platinum Electrodes

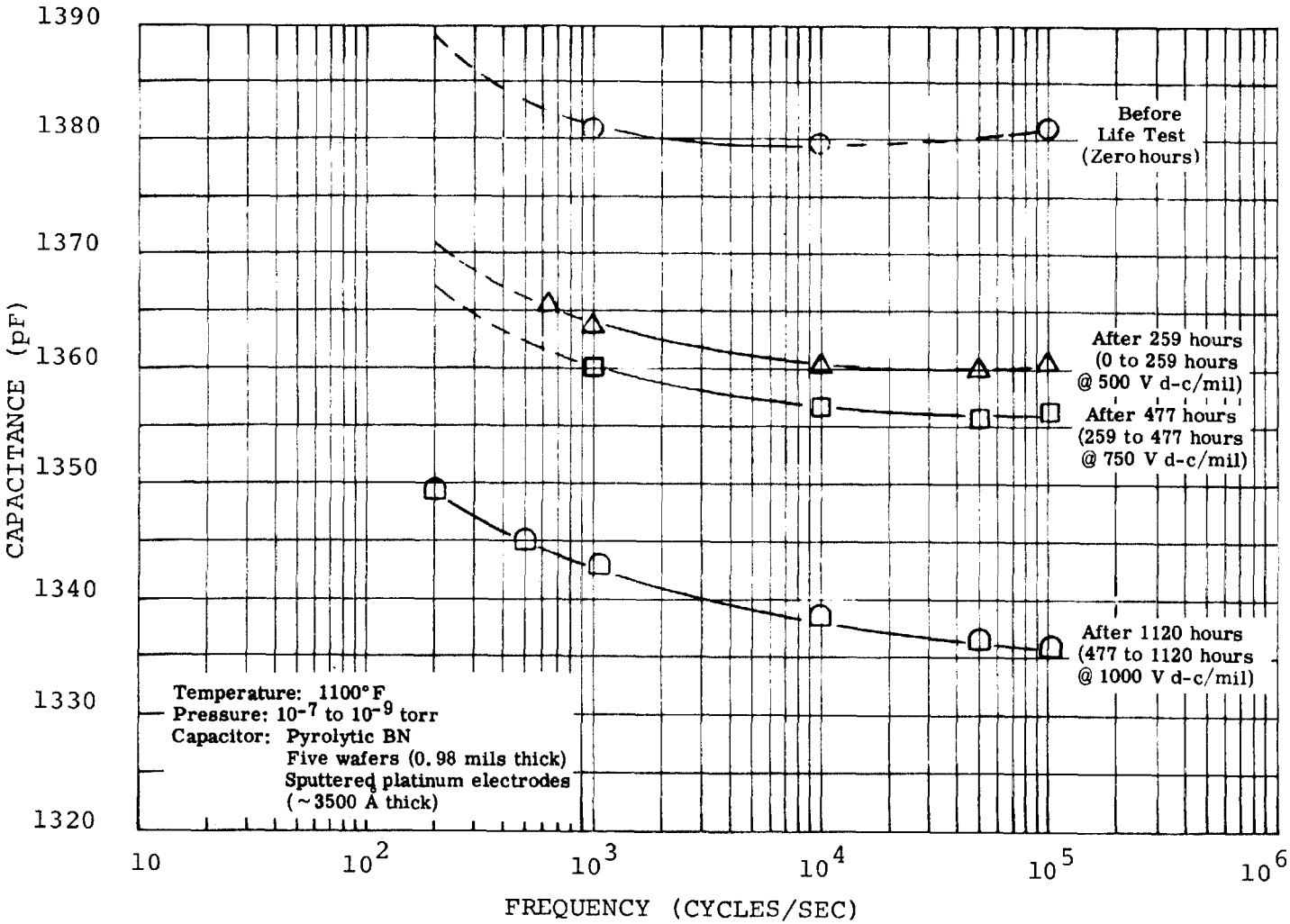


FIGURE 42. Capacitance Versus Frequency at Several Time Intervals with Increasing Energizing Voltages for a 1120-Hour Life Test at 1100°F in Vacuum on a Five-Wafer Multi-Layer Pyrolytic Boron Nitride Capacitor with Sputtered Platinum Electrodes

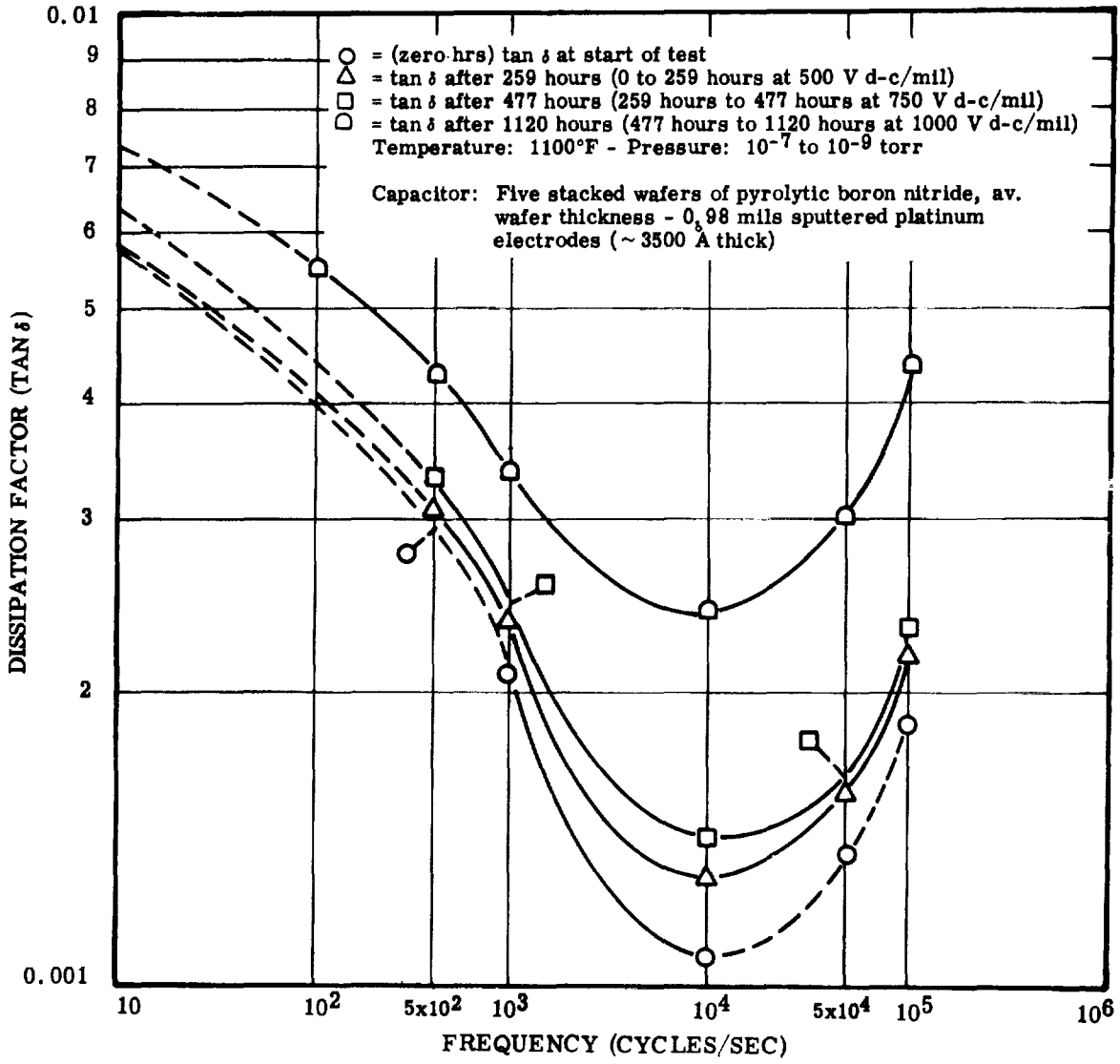


FIGURE 43. Dissipation Factor (tan δ) Versus Frequency at 1100°F in Vacuum at Different Time Intervals and Increased DC Energizing Voltages to 1120 Hours Total Test Time for a Five-Wafer Pyrolytic Boron Nitride Capacitor with Sputtered Platinum Electrodes

life test (to 1120 hours) on the five-wafer multilayer unit. The test was continued beyond the the planned 250-hour test time because of satisfactory performance to 259 hours. In addition, longer test times at increased energizing voltages would help to identify potential problem areas for projected 10,000-hour applications.

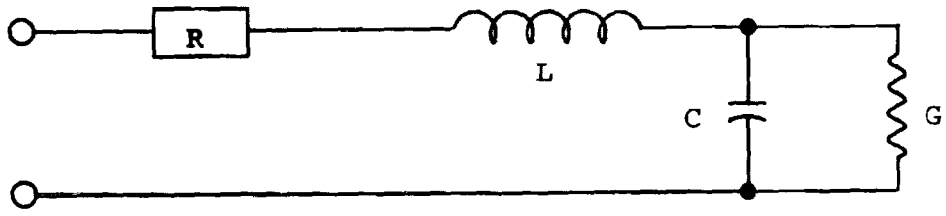
Figure 38 shows the change in tan δ and capacitance as functions of time. In general, it appears that for d-c energizing voltages up to and including 750 volts (750 Vd-c/mil) the rates of change of capacitance and tan δ are essentially constant and relatively small in magnitude. These conditions appear to hold for times up to 477 hours. The d-c voltage was then increased to 1000 volts (1000 Vd-c/mil) for an additional 643 hours. It is evident that tan δ increased and the capacitance decreased at greater rates after 477 hours or for the next 643 hours at 1000 Vd-c.

The change in the RC product (megohms x microfarads) with time and higher energizing voltages is shown in figure 39. An initial increase was observed up to 259 hours. From 259 to 477 hours a decrease occurred, indicating a decrease in insulation resistance or increase in the d-c conductivity. However, from 477 to 1120 hours (at 1000 Vd-c) the RC product again increased. This may be the result of electrode polarization (depletion of charge carriers at the electrodes) or to a decrease in surface conductivity due to evaporation of condensed surface contaminants.

Figures 40 and 41 show tan δ and capacitance as functions of temperature (to 1100° F) and the change in magnitude of these parameters with time at constant temperature (to 1120 hours) at 10 kc/sec. A permanent increase in tan δ and decrease in capacitance is evident after the capacitor was cooled to 72° F.

(2) Capacitance and Tan δ Versus Frequency

Any real capacitor with a solid dielectric deviates from ideal performance (ref. 7) with distributed elements (real and imaginary) represented by the equivalent circuit shown below:



where

R = metallic resistance (leads, supports, electrodes)

L = series inductance of leads, supports and electrodes

C = capacitance between electrodes

G = conductance (dielectric losses of supporting insulators, solid dielectric between capacitor electrodes and d-c leakage conductance)

The measured capacitance increases, therefore, from the zero frequency capacitance, Co, as frequency, f, increases because of series inductance as shown in equation (1).

$$\frac{\Delta C}{C_o} = 2\pi f \; L \; C_o \qquad (1)$$

A tendency for capacitance to decrease with increasing frequency due to space charge polarization produces a negatively sloped curve over part of the frequency range. The sum of these two effects (polarization and series inductance) generally results in a U-shape curve for a capacitance versus frequency relationship.

Similarly, the total dissipation factor (tan δ) varies with frequency in accordance with equation (2).

$$\tan \delta = \frac{G}{2\pi fC} + 2\pi f^{3/2} RC \qquad (2)$$

At sufficiently high frequencies, tan δ will begin to increase as the 3/2 power of the frequency due to the losses represented by the series resistance

(R) in the equivalent circuit. In the lower frequency ranges tan δ decreases with increasing frequency due to conductance losses (G). The sum of these two terms in equation (2) results in a U-shaped curve with a negative slope up to frequencies ranging from 1 kc/sec to 1 mc/sec depending on capacitance values.

Figures 42 and 43 show capacitance and tan δ as functions of frequency at 1100° F in vacuum during several time intervals (after 259, 477 and 1120 hours). The curves shown in figure 42 indicate that most of the capacitance change occurred during the first 259 hours (at 500 Vd-c/mil) and the curves follow the general form of equation (1). Relatively little change occurred during the next 218 hours at 750 Vd-c/mil and the increment of change in capacitance for the next 643 hours at 1000 Vd-c/mil is about the same as the first 477 hours.

The curves for tan δ versus frequency shown in figure 43 appear to follow the form of equation (2) if the conductance term (G) is modified so that tan δ decreases with frequency (in the lower frequency range) as the reciprocal of some fractional power of f.

An IBM 7040 computer program was written to determine resistance (R) and conductance (G) and the functional characteristics from the test data of tan δ (dissipation factor) versus frequency. The program chooses the values of (R) and (G) from equation (2) which give the minimum mismatch to the test data. A least square mathematical critera was used to minimize the mismatch.

The best values of (R) and (G) from equation (2) did not give a good match in the median frequency range (5 kc/sec to 50 kc/sec). The experimental data given in reference 8 for pyrolytic boron nitride indicated that a different power of frequency for the (G) term of equation (2) would result in a better fit between the equation and the test data.

Figure 44 shows the curves determined by the computer program for different values of P (power of f). A (P) value of 0.3 gives the best fit. For each curve, (P) equals a constant and the computer program determines the value of (R) and (G) which gives the best fit to the experimental data.

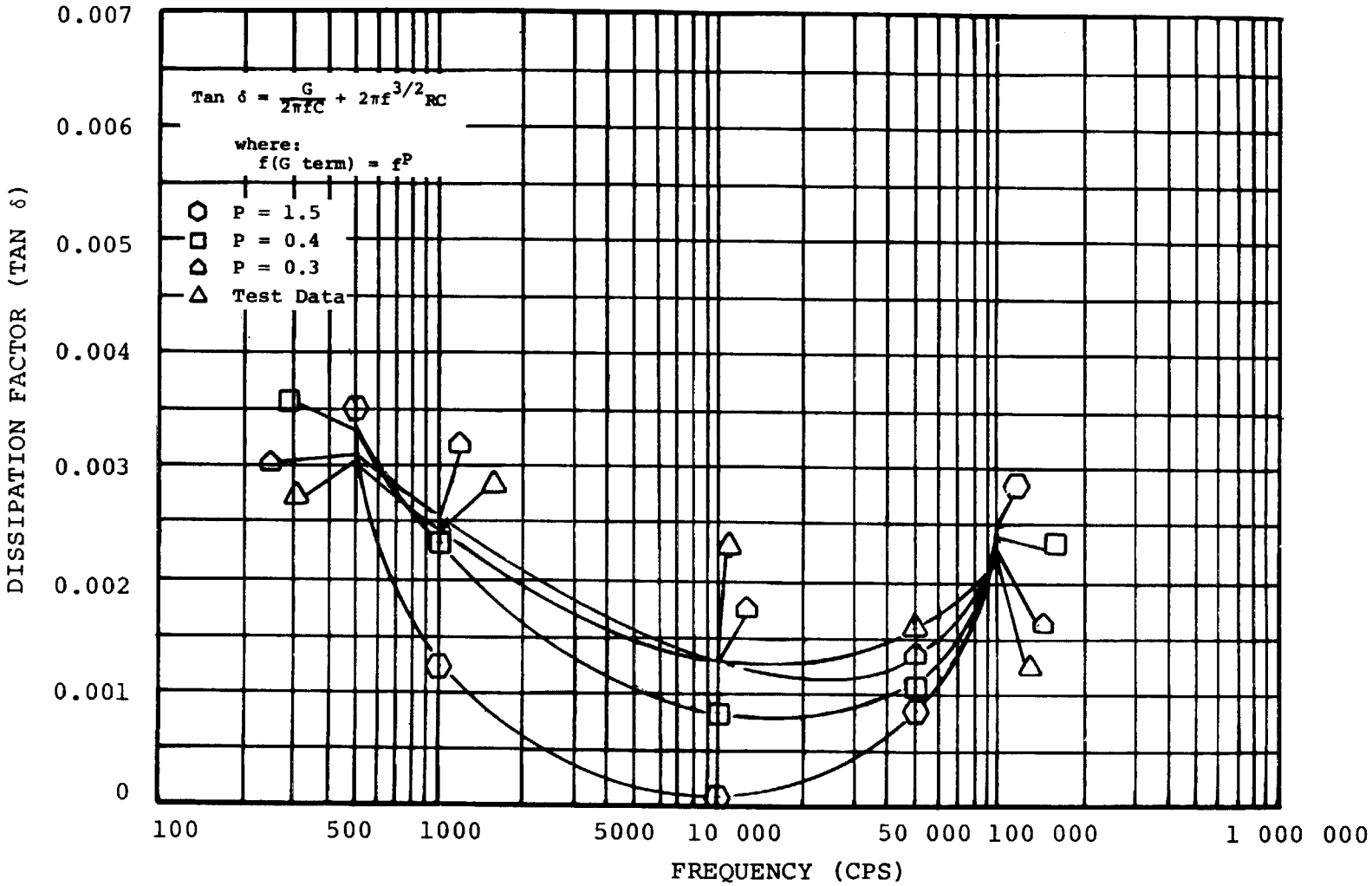


FIGURE 44. Results of a Curve Fitting Computer Program to Find f^P Based on the General Relationship, Tan $\delta = \frac{G}{2\pi fC} + 2\pi f^{3/2}RC$ Using the Experimental Life Test Data (figure 41)

These values of (G) and (R) were computed from the test data (figure 41) for different times up to 1120 hours. Figure 45 shows a comparison of ratios of $\frac{\Delta G}{G_o}$ and $\frac{\Delta R}{R_o}$ x 100 versus time. It appears that the rate of increase in the series resistance (R) does not change significantly until after the 477-hour time interval. This corresponds to the increase in energizing voltage from 750 to 1000 Vd-c/mil. By comparison, the conductance (G) does not show as marked an increase.

These data also indicate that the increase in the capacitor losses for the first 259-hour period are about equally divided between the increase in the series resistance (R) and conductance (G) loss components. From 259 to 477 hours, (G) increases at a faster rate than (R) and becomes the predominant loss component (approximately 80% at 477 hours). However, for the final 643-hour period, the loss components show a reversal. At the completion of the test, only about 45 percent of the total loss can be attributed to the conductance (G) term. Thus, for the overall 1120-hour period, (R) increased 125 percent, whereas (G) increased only 46.5 percent.

(3) Visual Examination

The five-wafer pyrolytic boron nitride capacitor that completed 1120 hours of test time at 1100° F was disassembled and examined. The pyrolytic boron nitride clamping fixture and the two uncoated (less sputtered platinum electrodes) wafers placed at the top and bottom of the five-wafer capacitor stack, showed a slight amount of surface darkening together with several widely dispersed dark spots. Vaporization and condensation of contaminants trapped within the layered structure of the pyrolytic boron nitride fixture may account for some of the darkening effect. In addition, contamination from metallic parts of the test furnace, fixturing and capacitor (electrodes) may be another source of surface discoloration. In general, this effect would account for part of the increase in measured capacitor losses (conductance (G) component) with time due to increased surface conductivities.

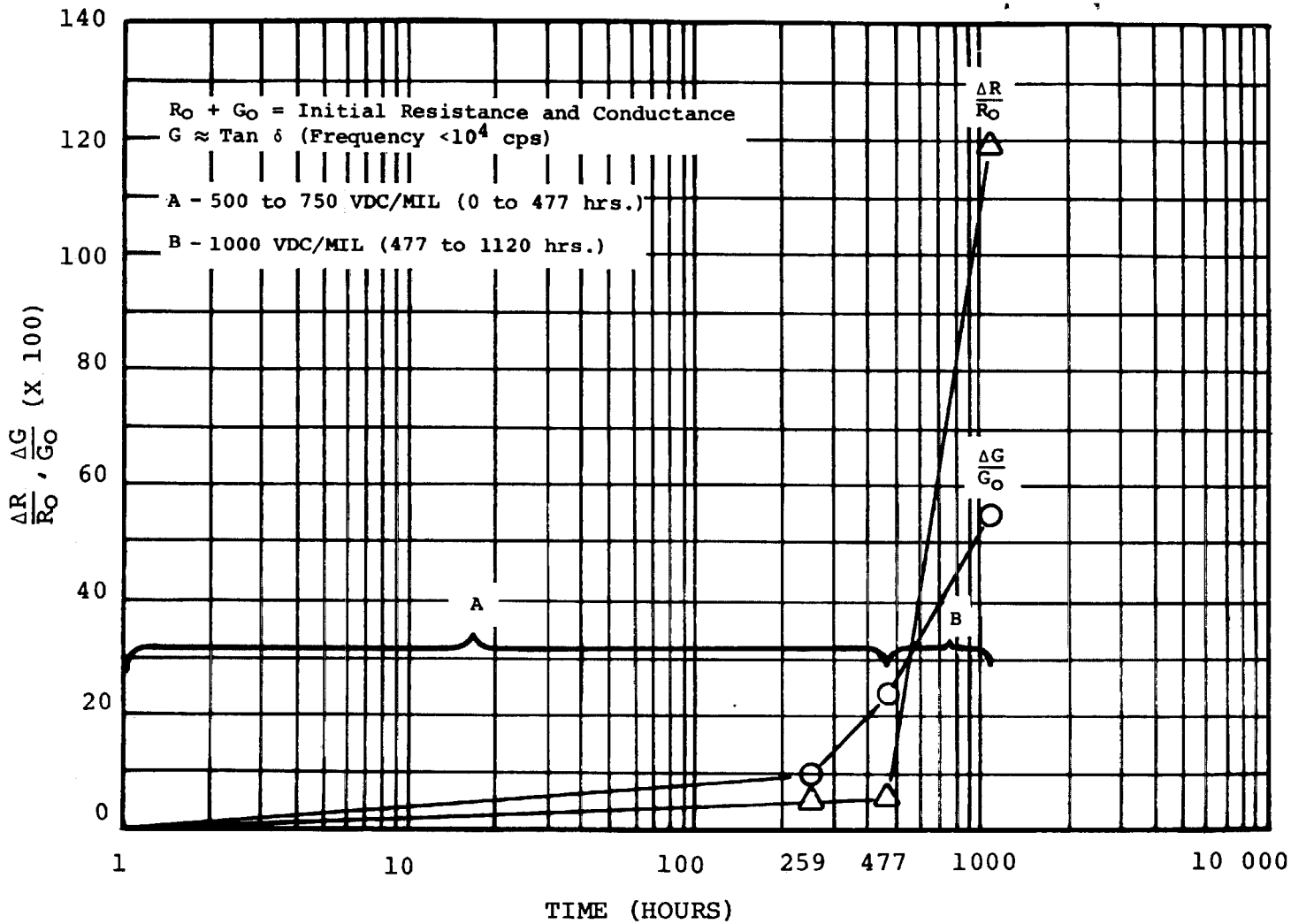


FIGURE 45. Separation of Capacitor Losses (Conductance G and Series Resistance, R) Expressed as the Ratio of $\frac{\Delta G}{G_O}$ x 100 and $\frac{\Delta R}{R_O}$ x 100 Versus Time and Increased DC Energizing Voltages at 1100°F in Vacuum for a Five-Wafer PBN Capacitor

In attempting to separate the individual capacitor wafers in the stack, it was apparent that all of the wafers were bonded together via their electrodes. By carefully inserting a razor blade between two wafers it was found that adjacent electrodes were diffused into a single homogeneous foil. When the wafers were separated, both electrodes adhered to one of the wafers and peeled away from the other. These results indicate that the initial electrode adherence decreases substantially under the combined driving forces of time, temperature, pressure, vacuum, and the lower interface energies associated with metal-to-metal versus metal-to-oxide or nitride contact. The two outer electrodes on the end wafers in the stack did not show a loss of adherence apparently because they were in contact with pyrolytic boron nitride surfaces (high interface energies).

Thus it seems reasonable to conclude that a physical separation or air (vacuum) gap at the wafer electrode interface developed due to a decrease in electrode adherence. The width of this gap apparently increased with time, electrical stress, and temperature fluctuations (furnace power interruptions).

Therefore, the decrease in capacitance and increase in tan δ after 1120 hours can be assigned to a parasitic series capacitance and its associated loss mechanisms produced by the air (vacuum) gap. If, for example, the gap has a width or thickness of 680 Å with a dielectric constant of one (for vacuum), a capacitance of about 30,000 pF would appear in series with one side of a standard capacitor wafer (calculated for an electrode area of 0.364 in^2). If a gap of equal thickness exists at the opposite electrode, another series capacitance is generated of equal magnitude. The effective capacitance is then 15,000 pF and will appear in series with the capacitance attributed to the bulk dielectric (pyrolytic boron nitride).

For example, if the initial measured capacitance is 300 pF, this value will be reduced to about 294 pF (2% decrease is measured capacitance) by the addition of a series capacitor having a value of 15,000 pF. As noted above, the series capacitance can be derived from the appearance of an air gap at the wafer/electrode interface. Therefore, as this gap thickness increases, the series

capacitance decreases and the resulting terminal capacitance will decrease according to the usual relationship for two capacitors connected in series.

To summarize, it appears that the instabilities in electrical properties with time and increasing d-c energizing voltages are primarily caused by electrode interface phenomena and other extrinsic effects not necessarily associated with the bulk of the dielectric. Very satisfactory capacitor performance at 1100° F is indicated for a voltage stress up to 750 Vd-c/mil. At 1000 Vd-c/mil, accelerated degradation of tan δ and capacitance is evident, but with further improvements in capacitor fabrication methods, it appears that the degradation mechanism previously discussed can be minimized significantly.

SECTION IV

CONCLUSIONS AND RECOMMENDATIONS

A. CONCLUSIONS

1) Pyrolytic boron nitride (Boralloy) can be mechanically worked into very thin (0.004- to 0.001-inch) and flexible, pinhole free wafers and sheets from thick blocks of starting material. The harder and more brittle materials (aluminum and beryllium oxides) cannot be mechanically reduced to thickness less than 0.003- to 0.005-inch without experiencing excessive defects.

2) One-mil (0.001-inch) thick pyrolytic boron nitride (PBN) has significantly better electrical properties (tan δ, $\Delta C/C_{72°\ F}$, RC Product and d-c breakdown voltage) at 1100° F than the other candidate materials. These results combined with a higher degree of mechanical workability make this material a logical choice for high-temperature capacitor fabrication.

3) A method of interconnecting sputtered thin film electrodes (platinum, rhodium and platinum-rhodium alloys) deposited on individual PBN wafers has been shown to be a practical and efficient design concept that closely approximates the theoretical maximum capacitance that can be achieved in a given volume. Test results at temperatures up to 1100° F in vacuum on prototype multi-layer capacitors indicate that modular units can be assembled containing 100 or more individual wafers. Unit capacitance values ranging from 0.03 to 0.1 μF could then be achieved.

4) Electrodes and the electrode-substrate interface region have been identified as the most significant variables in the fabrication process to affect capacitor performance. These variables include: electrode resistivity, ductility, modulus of elasticity, thickness, adherence to the substrate, surface roughness of the substrate, and interelectrode diffusion bonding.

5) Successful completion of an 1120-hour life test (PBN multi-layer capacitor) at 1100° F in vacuum under continuous d-c voltages from 500 to 1000 Vd-c/mil has demonstrated overall design and performance feasibility. These results indicate that the program goals (volume parameter, maximum capacitance change, and losses to 1100° F) have been achieved.

B. RECOMMENDATIONS

1) Investigate methods to increase the adherence of thin film electrodes on pyrolytic boron nitride and to reduce or eliminate interelectrode diffusion bonding in a stacked-capacitor configuration. Improved electrical performance of capacitors subjected to shock, vibration and high-electrical stresses at elevated temperatures for extended periods of time is indicated.

2) Study materials and processes necessary to hermetically package pyrolytic boron nitride multi-layer capacitors to obtain maximum volume efficiencies and reliable operating characteristics.

3) Fabricate and evaluate high-capacitance units consisting of 50 or more stacked PBN wafers. Determine operating voltage gradient capabilities under long-term (1000 to 10,000 hours) conditions.

4) Study the feasibility of fabricating high-temperature capacitors using (as deposited) thin-film dielectric materials in the thickness range from 1 to 25 microns.

SECTION V

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APPENDIX A

LAPPING PROCEDURE FOR UNBONDED PYROLYTIC BORON NITRIDE WAFERS DURING FINAL STAGES OF WAFER THICKNESS REDUCTION

The following is a brief description, with photographs, of the lapping process described in detail on pages 19 and 20 of this report.

1) Cleaved or as sliced wafers are wax bonded to a metal holder and lapped to approximately 6 mils. A typical holder with two mounted wafers is shown in figure A-1. Metal shim strips are spot welded to the surface of the holder and act as stops to control the wafer thickness during lapping.

2) Figure A-2 shows the Mazur Lapping/Polishing Machine with a wafer holding fixture about to be placed on the glass lapping plate. The holder and wafers are placed face down onto the lapping plate containing a slurry of abrasive and water. The machine is run at its slowest speed setting and stock is removed from the wafers until they reach the height of the shim stop.

3) Figure A-3 shows a PBN wafer after it has been lapped to about 6 mils. The wafer is not wax bonded to the holder. At least one surface has sufficient flatness at this stage to adhere to the face of the holder by surface tension from a water film (small amount of abrasive slurry). The wafer is lapped to the thickness of the shim stop as outlined in Step 2 and then transferred to another holder with thinner shim stops. This process is repeated until a one-mil wafer is obtained.

Alternate Method

Steps 1, 2, 3 as described above are essentially the same. However, after a wafer thickness of about 2 mils is obtained, the final thickness reduction to 1 mil is done by lapping the wafer between one fixed and one floating glass plate using fine micron alumina abrasive and water. Figure A-4 shows a wafer positioned between the glass lapping plate on the Mazur Machine and a hand held glass plate. The top plate is moved manually in a figure eight motion. The wafer is removed occasionally for thickness measurements until the desired thickness is attained.

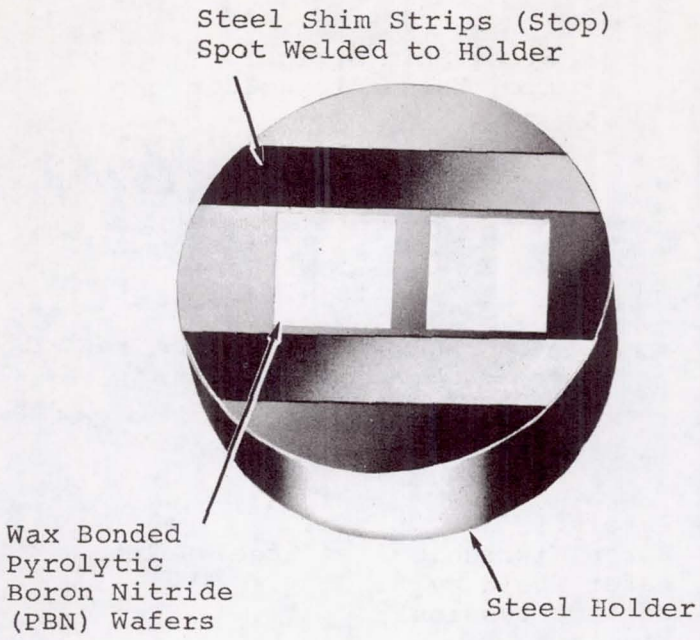

FIGURE A-1. Steel Holder with Wax Bonded Pyrolytic Boron Nitride Wafer

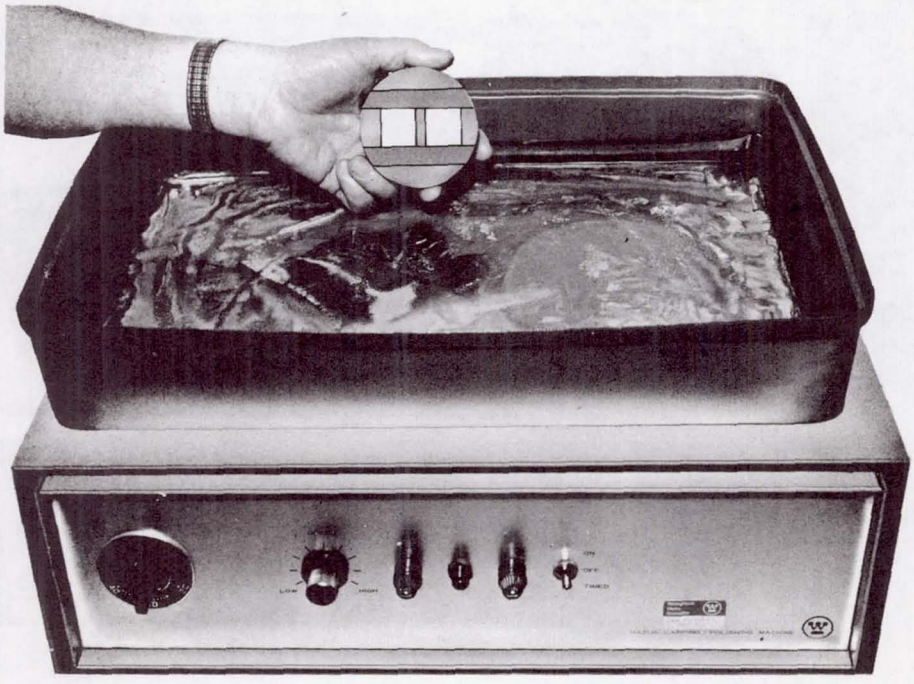

FIGURE A-2. Mazur Lapping/Polishing Machine Showing a Wafer Holding Fixture About to be Placed on Glass Lapping Plate

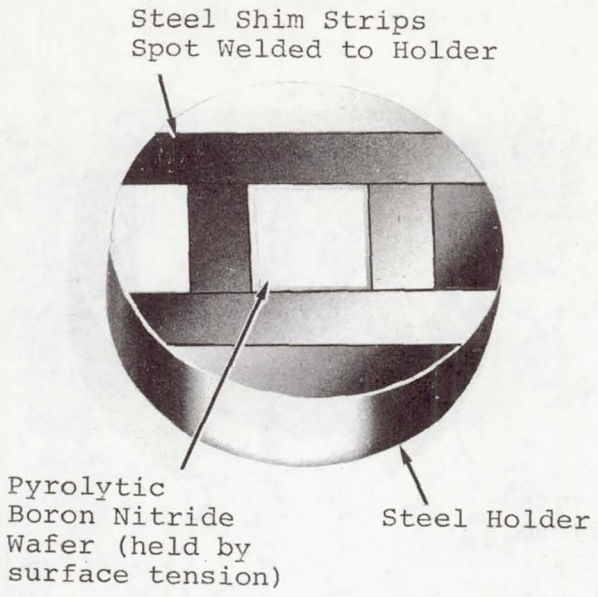

FIGURE A-3. Unbonded Pyrolytic Boron Nitride Wafer and Holder Ready for Lapping to Height of Shim Stops

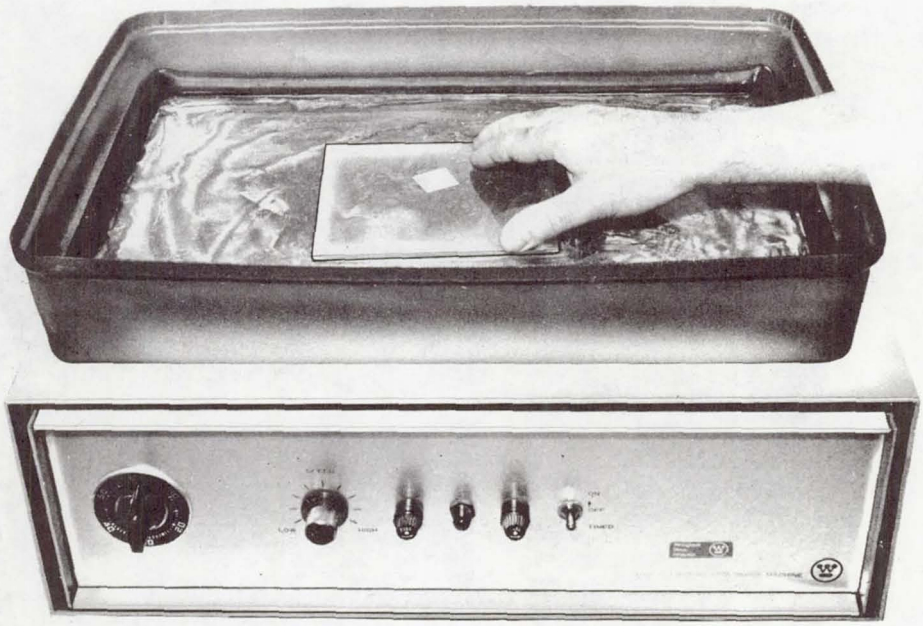

FIGURE A-4. Pyrolytic Boron Nitride Wafer Being Lapped to 1-Mil Thickness by Alternate Method (between two glass plates)