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METALLIZATION SYSTEMS FOR INTEGRATED CIRCUITS

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16. Abstract

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METALLIZATION SYSTEMS FOR INTEGRATED CIRCUITS

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SUMMARY

Metallization-related failure mechanisms have been shown to be a major cause of integrated circuit failures under accelerated stress conditions. The integrated circuit industry is aware of the problem and is attempting to solve it in one of two ways: (1) better understanding of the aluminum system, which is the most widely used metallization material for silicon integrated circuits both as a single level metallization and LSI; or (2) evaluating alternative metal systems.

As integrated circuit structures become more complex, additional processing steps are required to obtain multilevel metallization. Low temperature deposition of dielectrics is essential, and etching through to interconnect the levels of metallization is critical. In addition, smaller geometry and closer spacings are required.

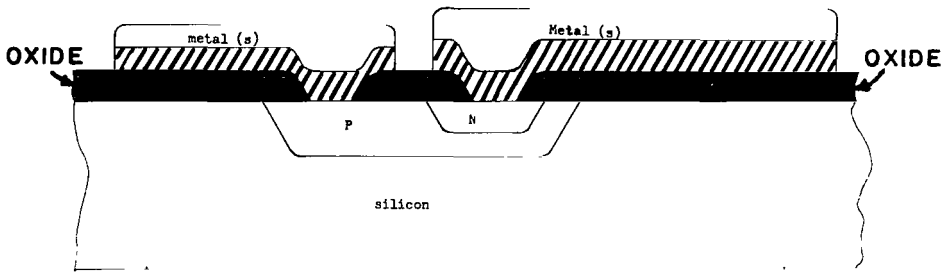
Aluminum metallization offers many advantages, but also has limitations particularly at elevated temperatures and high current densities. As an alternative, multilevel systems of the general form, silicon device-metal-inorganic insulator-metal, are being considered to produce large scale integrated arrays. An attempt will be made in this survey to define the merits and restrictions of metallization systems in current usage and systems under development.

INTRODUCTION

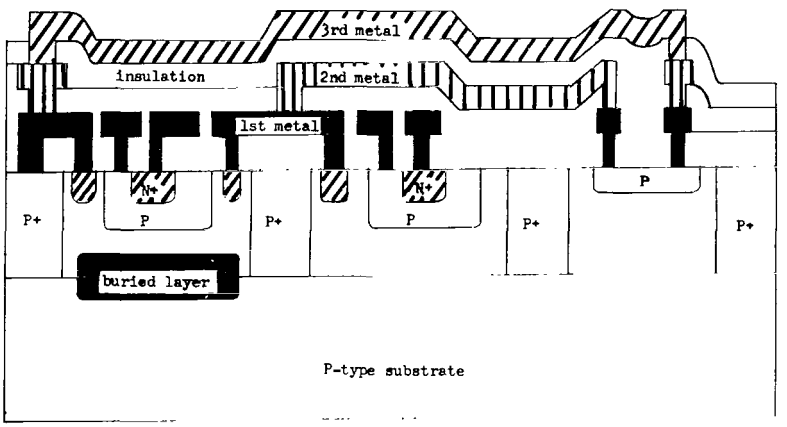
Metallization-related failure mechanisms have been shown to be a major cause of integrated circuit failures under accelerated stress conditions. This survey will concentrate on inherent limitations in material combinations, and methods of detecting these, to provide guide lines for characterization and selection of metallization systems for integrated circuits.

Metallization characterization tests are determined by: (1) properties of metal thin films, (2) metallization requirements, (3) integrated circuit processing, and (4) long term stress.

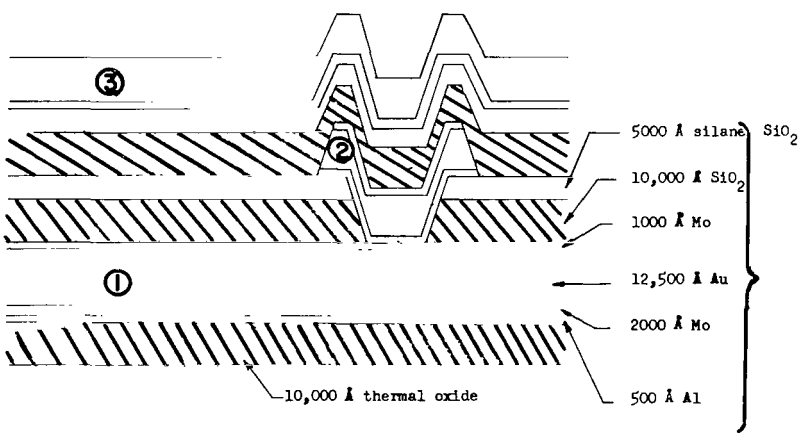
Both single- and multilayer-metallization systems will be discussed as such, and as to their applicability to multilevel integrated circuit fabrication. Figure 1 shows a schematic of single metal, multilayer, and multilevel metallization.



Metallization system on silicon device



Multilayer metallization system



Mo-Au-Mo-SiO_2 multilevel system

Figure 1.- Schematic of single metal, multilayer, and multilevel metallization

The basic requirements of any silicon integrated circuit metallization system are:

1. High conductivity (greater than 10 μ-ohm-cm);

2. Good adhesion to both silicon, dielectrics, and glass;

3. Low ohmic contact resistance to both n-type and p-type silicon;

4. System free from degrading intermetallic compound formation or deleterious silicon reactions during processing or operating life conditions;

5. Amenability to practical production methods of deposition and delineation;

6. Resistance to current-induced metal electromigration;

7. Freedom from surface instabilities induced by the metal(s) and method of deposition;

8. Compatibility with multilevel processing.

The successful production of large scale integration requires a materials and processing capability for forming metal conductor paths interconnecting the various components. In this respect the following factors must be taken into account:

1. Electrical constraints;

2. Chemical needs;

3. Metallurgical requirements;

4. Mechanical requirements to provide reliable operation;

5. The interfaces which must be satisfied by a metallization system.

To consider the electrical requirements, the metallization must be an excellent conductor, since extremely fine lines are required for multilevel, high density, integrated circuits. The thickness of the metal film cannot exceed one-third of the line width. Therefore, for a 2-μ wide conductor line, a 6000-Å thick metal is used, which results in an idealized conductor cross-sectional area of 12×10^{-8} cm^2. The conducting metal must make ohmic contact to both n-type and p-type silicon. In the case of shallow junctions the emitter and base p-n junctions will be within 1 μ (or less) of the surface. This requires that the metal used for contact to the silicon will not penetrate more than 100 Å.

Chemically, the metallization must resist deterioration in oxygen at 500°C to survive the post metallization processing steps. The first layer of metallization must act as a reducing agent for silicon dioxide to reproducibly make ohmic contact through the thin layer that readily forms on silicon. When considering the use of multilevel metallization, it is desirable that the metal does not react sufficiently with the dielectric to form conductive electrical paths between the metal layers at the crossover points. It is therefore necessary that the metal be only a slightly reducing agent and that the temperature at which the reduction takes place be reached rapidly and only once to form the ohmic contact.

From a metallurgical standpoint, one mode of failures that has been noted is a mass transfer of the metal conductor when carrying a high current density at elevated temperatures. For example, the mean-time-to-failure for aluminum film conductors carrying 1.5×10^6 amp/cm^2 at 175°C is about 23 hr. An exchange of momentum between the electrons and activated metal ions causes the metal ions to be transported in the direction of the electron flow. The result is a depletion of metal at the cathode end where a gradient in current density or temperature exists. The effect is cumulative, further increasing the current density resulting in an open circuit. As the geometry of the integrated circuit decreases, current densities exceeding 10^6 amp/cm^2 may exist. Since the self-diffusion coefficient for evaporated films decreases when the films become more ordered, the deposition techniques, which result in well-ordered films whose resistivity approaches that of bulk metal, will also be more stable at high current densities. Refractory metals have low self-diffusion coefficients, which make them attractive for high current density application.

It is also important that metal conductors do not form intermetallics with silicon or with the overlay metal. To minimize these reactions, metals possessing low diffusion coefficients must be used. An equally important consideration is packaging. Both metal components must be sufficiently soft to flow during bonding. Flow by deformation is required to open fresh and, therefore, clean metal surfaces in intimate contact with each other to promote atomic interdiffusion and crystal growth resulting in a weld.

It is desirable for the conductor used in multilayer metallization schemes to utilize a metal which has a coefficient of thermal expansion near to that of silicon. In the application of glass as a protective layer over the conductor, the bulk expansion differential may be sufficient to cause cracking of the dielectric, thus resulting in electrical shorts. The reduction of glass cracking in multilevel metallization requires

that the metal conductor be a reasonable match to the coefficient of expansion of the silicon and the dielectric.

It is very important in the selection of a metallization system to consider the processing steps required in the fabrication of an integrated circuit. These steps are:

1. Deposition of metallization (silicon, containing p-n junctions and dielectrics, heated to 200 to 500°C prior to vacuum deposition and deposition times ranging from 10 to 20 min for each metal layer);

2. Heat treatments (5 to 15 min at 300 to 600°C for good ohmic contacts);

3. Glass deposition (200 to 500°C for 10 to 20 min);

4. Application of solder or eutective bonding material on back of wafer (5 min at 400 to 500°C);

5. Bonding chip to header or package (5 min at 400 to 500°C);

6. Lead bonding (RT to 350°C);

7. Sealing package (5 to 30 min at 200 to 500°C);

8. Operational life stress tests at elevated temperatures (300°C for 1000 or more hours).

One of the most stringent tests is the 300°C storage test with bias voltage applied to the device. Some devices operating at high power result in high current densities and localized temperatures that may exceed 500°C.

EVALUATION OF METALLIZATION SYSTEMS

Single Metal Systems

Aluminum is the predominant metallization system used in the fabrication of silicon integrated circuits for the following reasons:

1. Has a low bulk resistivity of 2.7 μ-ohm-cm (films closely approach this value);

2. Is easily evaporated;

3. For a resistivity of 0.1 ohm per square, films need only be 3000 Å;

4. Has good adherence to silicon and silicon dioxide;

5. Has good ohmic contact to both p-type and n-type silicon;

6. Is easily patterned.

Unfortunately, in certain applications, aluminum does possess undesirable characteristics. For example, aluminum reacts with gold to form various intermetallic compounds which increase contact resistance and can result in open bonds. This reaction takes place rapidly at 450°C and can occur over a period of time at 150°C. Although the interaction of the metals can be eliminated by using ultrasonically bonded aluminum wires, ultrasonic bonding demands precise equipment and process control. Unlike the gold ball bonds, the ultrasonic bond of aluminum wire to aluminum metallization is weaker than the wire itself. The Al-Al bonds usually fail at the heel of the bond where the wire has been deformed by the bonding tool. Figure 2 shows a common potential failure in ultrasonic bonds.

Figure 3 shows another failure mode commonly found in integrated circuits, which appears when aluminum conductors carry current densities in excess of 10^5 amp/cm^2 at temperatures above 100°C. The mode of failure is an open circuit caused by the movement of aluminum ions in the direction of the electron flow. Voids in the metal, resulting from this process, tend to grow in a direction normal to the current flow. The effect is an accumulative one increasing the local current density in the region of the void, thus accelerating the process. This frequently occurs in emitter strips where the strip thickness is reduced as it extends over a step in the glass surface. Aluminum at 500°C will attack the underlying silicon dioxide and migrate through to the silicon in a few hours. Even at temperatures around 300°C, over long periods of time, the aluminum develops high crystalline spots and voids which cause opens in the metallization. An additional concern is a failure mode associated with Al-Si contacts, which results in the growth of etch pits into the silicon at the positive terminals during high current density and temperature stress. It is speculated that the etch pit formations are due to:

1. Solid state dissolution of silicon into aluminum to saturate the aluminum at its operating temperature;

2. Transport of the dissolved silicon away from the interface by momentum exchange between thermal activated

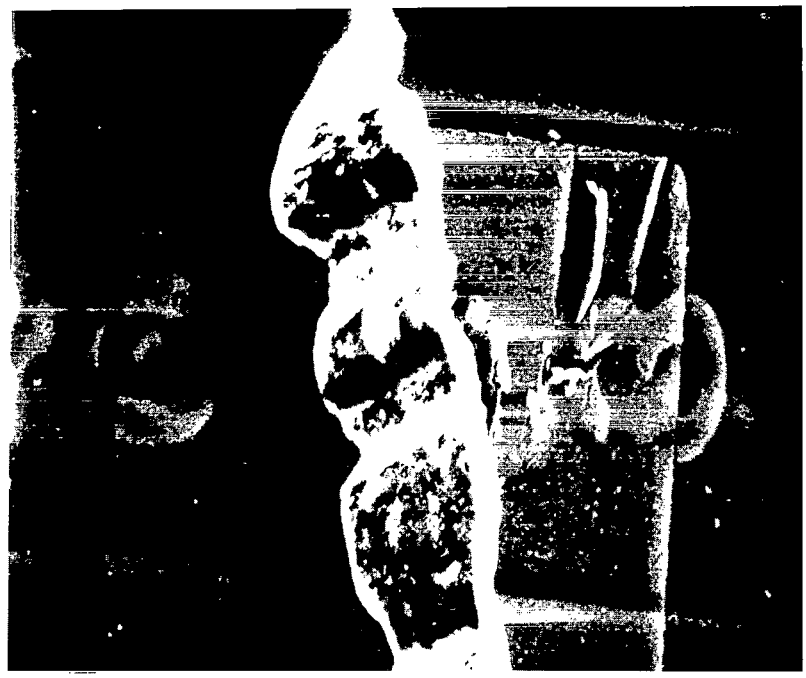
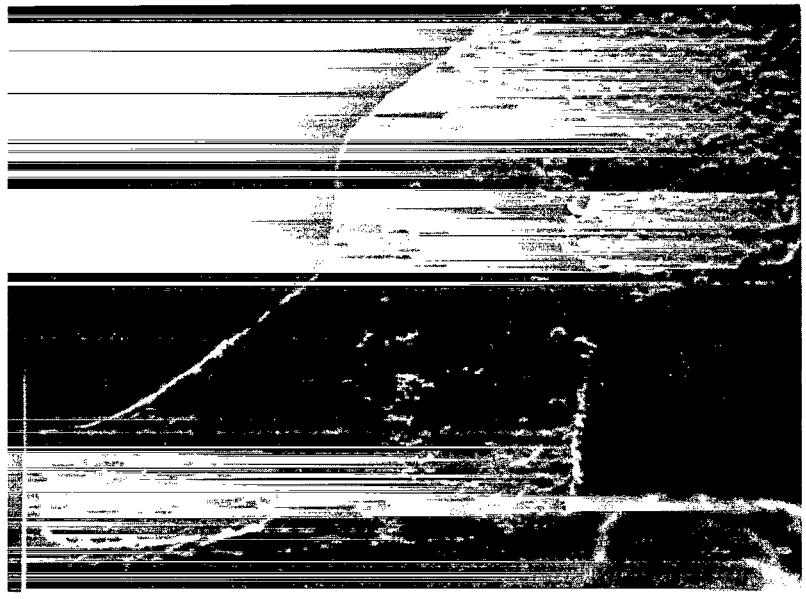


Figure 2.- Potential ultrasonic bond failure



(2400X HORIZONTAL)

Figure 3.- One-mil aluminum strip with void formation due to electromigration

silicon ions and conducting electrons enabling further solid state dissolution of silicon into aluminum.

Because silicon will preferentially enter the aluminum from crystalline dislocation, rather than uniformly over the surface, the process results in the formation of etch pits into the silicon at crystalline dislocations. The process can continue until the junction beneath the Al-Si contact interface is electrically shorted by the growth of an etch pit through the junction.

Other single metal systems present problems in deposition techniques, adherence to silicon dioxide, and high resistance films.

Multilevel Metallization Systems

For the reasons mentioned above, two or more metal layers are considered. A composite-layered metallization system consists of a metal that adheres well to silicon and silicon dioxide and an overlay of a high conductivity metal. In certain cases a third metal may be used to prevent diffusion or interaction between the top and bottom metals. One such system utilizes platinum silicide, which possesses a number of desirable properties for an ohmic contact to both n-type and p-type silicon. The most stable silicon high silicide can be formed by solid-solid reaction far below the melting point of the eutectic. This is an important point (as compared to aluminum metallization processing). Platinum silicide can be formed on atomically clean silicon slightly above 300°C, whereas the melting point of the eutectic is 980°C. Built into the process is a higher degree of cleanliness than exists with other metal systems. Prior to the deposition of platinum, the chemically-cleaned, silicon surface is plasma-etched by backsputtering with argon ions. This produces a plasma over the silicon substrate that is effective in removing traces of residual oxide and contamination which may remain after chemical etching. With extremely small contact areas (0.3 x 0.3-mil windows), the ability to achieve completely cleaned out windows, free of all dielectric and other contamination, is extremely difficult, however, and a high temperature heat treatment of aluminum contacts is employed in order to insure "punching through" the residual dielectric by the aluminum.

The amount of contact resistance and linearity of resistance introduced by a particular metallization process is an important practical problem in the successful fabrication of semiconductor devices. Available data on the contact resistance for n-type and p-type silicon are given in Tables I and II.

One particularly significant application of platinum-silicide ohmic contacts to both n-type and p-type silicon has been

TABLE I.- METAL SILICON CONTACT RESISTANCE IN OHMS, AREA = 10^{-4} cm^2

Si Resistivity, Ω - cm	Metal			and		Metal + PtSi				
	Al	PtSi	Mo	PtSi	Ni	PtSi	Cr	PtSi	Ti	PtSi
n - Type Si										
0.001	0.09	0.02	0.08	0.02	0.02	0.02	0.03	0.03	0.01	0.01
0.01	6 (R)	0.1	5 (R)	0.4	2	0.3	3 (R)	0.2	4	0.2
p - Type Si										
0.002	0.03	0.02	0.06	0.03	0.02	0.02	0.04	0.04	0.01	0.01
0.04	1	0.7	3 (R)	1	4 (R)	2	8 (R)	1	- -	0.9
0.08	- -	- -	- -	- -	45 (R)	4	- -	- -	- -	3
0.5	20	10	80 (R)	10	100 (R)	20	200 (R)	15	- -	15

(R) indicates rectifying contact

TABLE II.- TEMPERATURE STABILITY, CONTACT RESISTANCE (Ω)

Si Resistivity, Ω - cm	Initial Resistivity Ω		After 15 min at 450°C Air Bake		After 15 min at 600°C Forming Gas	
	Al	+ PtSi	Al	+ PtSi	Al	+ PtSi
n - Type Si						
0.001	0.08	0.02	0.08	0.02	4 to 10 (R)	0.02
0.01	4 to 9 (R)	0.1	5 to 20 (R)	0.1	15 to 60 (R)	0.09
p - Type Si						
0.002	0.03	0.03	0.02	0.02	0.01	0.02
0.5	50 to 70 (R)	30	25	30	25	- -

(R) indicates rectifying contact

their incorporation into the design of beam-lead transistors. Prior to a more detailed discussion of beam-lead technology, it should be emphasized that the key contacting areas to active devices are platinum-silicide ohmic contacts. Platinum-silicide ohmic contacts are being used successfully not only on transistor structures but also on insulated gate field transistors utilizing Schottky barrier contacts for source and drain.

A number of refractory metals combined with gold or silver as conducting metals were investigated, and in the cases of Cr-Au, Ti-Au, and V-Au disregarded for reasons of resistance changes due to interdiffusion or intermetallic formation. In all three cases gold alloyed with the underlying silicon through the interface metal. Increasing the thickness of the interface metal delayed the reaction but resulted in a high resistance film. The results of this experimental work are presented in Tables III and IV.

Introducing a barrier metal, such as platinum, between the titanium and gold films prohibits the intermetallic formation mentioned previously. This Ti-Pt-Au combination has been used successfully for several years and is known as beam-lead technology. The critical parameter in the Ti-Pt-Au metal system is the platinum thickness. The platinum must be thick enough to avoid pinholes but thin enough to have a minimum of resistance change at elevated temperature operating conditions. A thickness of 1500 to 2000 Å is a reasonable figure.

Silver has also been used as a barrier between Cr-Au and Ti-Au. The Cr-Ag-Au system is not as thermally stable as Ti-Pt-Au, but is excellent for low temperature operation.

Chromium-Silver-Gold-Metallization

A study has shown that a Cr-Ag-Au metallization system will be more compatible with future transistor structures than aluminum. In the Cr-Ag-Au system the initial layer of chromium is used to provide the necessary metallization adherence to the silicon dioxide, and the outermost layer of gold is employed as a nonoxidizable bonding surface. An intermediate blended layer of Ag-Au is utilized to separate the chromium from the gold, thereby preventing the occurrence of Cr-Au intermetallic solid solutions which can be difficult to etch. The silver and gold, which make up the current carrying portions of this metallization system, have greater atomic masses, greater activation energies for self-diffusion, and higher melting points than aluminum. These factors suggest that this system should have a better high current density capability than does aluminum. It is also noted that chromium and silver do not react with silicon at temperatures below 600°C, thus forming a barrier which

TABLE III.- RESISTANCE OF VARIOUS METALS AFTER AIR BAKES*

Metal / Thickness, Å		Resistance, Ω							
		450°C				650°C			
First Layer	Total Film	Initial Resistance	2 hr	4 hr	Au-Si Alloy	Initial Resistance	2 hr	4 hr	Au-Si Alloy
Al	7000	2.7	2.6	2.7	– –	– –	– –	– –	– –
Cr-Au	2000 6000	5.8	17.4	19.0	100% at 1 hr	– –	– –	– –	– –
Ti-Au	2000 6500	5.4	12	18	100% at 1 hr	– –	– –	– –	– –
V-Au	800 9900	1.7	3.6	3.6	300/400 after 1 hr	1.7	6.6	5.6	100% after 30 min
	1600 6600	3.5	7.1	5.9		3.6	8.3	9.5	
(Ti-Pt)-Au	3000 9000	2.9	4.0	4.3	0/120 after 4 hr	– –	– –	– –	– –
Mo-Au	2100 10,000	3.2	2.5	2.5		2.7	2.3	2.3	12/400 after 4 hr
	2700 7200	3.1	2.8	2.8	1/400 after 4 hr	3.2	2.7	2.8	
W-Au	1400 6600	2.6	2.6	2.5		2.5	2.5	2.4	
	7200	3.4	2.7	2.7	2/400 after 4 hr	3.3	2.7	2.75	6/400 after 4 hr
Ti-Mo-Au	500 1500 5500	5.6	5.7	5.7	– –	5.3	4.8	5.0	– –
W-Au-Ti	300 (Ti)	4.9	3.4	3.2	– –	4.7	2.7	2.6	– –

*1 mil x 50 mil conductors; alloy tests on 20 mil^2 contacts

TABLE IV.- RESISTANCE OF VARIOUS METALS AFTER AIR BAKES*

Metal Thickness, Å		Resistance, Ω							
		450°C				650°C			
First Layer	Total Film	Initial Resistance	2 hr	4 hr	Au-Si Alloy	Initial Resistance	2 hr	4 hr	Au-Si Alloy
Ni-Au									
	6500	2.8	3.3	2.9	5/400 after 1 hr	3.0	open		300/400 at
2700	9500	2.8	7.0	7.0		2.6	10	open	30 min
Co-Au									
	8800	2.4	2.6	2.5	50/400 after 1 hr	2.4	2.4	2.4	– –
	9500	2.5	2.7	2.9		2.5	2.5	2.5	– –
Zr-Au									
1000	6900	2.3	2.5	2.4	100% after 1 hr	2.4	5.1	5.03	– –
2300	7200	3.1	3.0	2.9		3.2	5.4	4.3	– –
Ta-Au									
1600	7200	3.0	3.6	4.2	22/400 after 4 hr	3.1	6.1	5.4	6/400 at 30 min
Nb-Au									
1600	7600	2.5	3.0	3.2	3/500 after 4 hr	2.6	4.3	4.4	100/500 at
1600	5000	5.4	8.9	9.1		5.3	19.0	18.0	1 hr
Hf-Au									
1200	6300	2.8	3.6	3.5	25/400 after 4 hr	3.0	9.8	9.5	– –
	10000	2.4	2.6	2.6		2.4	22.	22	– –

*1 mil x 54 mil conductors; alloy tests on 20 mil^2 contacts

inhibits the dissolution of the silicon substrate. An evaluation was made of the resistance of the contacts of Cr-Ag-Au to silicon using aluminum as a comparison and control. Table V and Figure 4 show the results of these measurements.

These results indicate that Cr-Ag-Au makes a good, low resistance ohmic contact to n-type silicon for doping levels greater than 1×10^{18} atoms/cm^3, whereas aluminum makes high resistance nonohmic contact for doping levels less than 4×10^{18} atoms/cm^3. For doping levels greater than 1×10^{18} atoms/cm^3 in p-type silicon, the Cr-Ag-Au makes as good or slightly better contact than does aluminum. In either case, by the use of an enhancement diffusion the Cr-Ag-Au system can provide better ohmic contact to n-type and p-type silicon than does aluminum.

It should be noted that, for contacts made to p-type silicon, the spreading resistance is the dominant term in the measurements. For n-type silicon, however, the spreading resistance is an appreciable portion of the measured resistance values only for silicon materials of resistivity less than 0.005 ohm-cm.

A study was made of the behavior of the Cr-Ag-Au metallization under high current density loads and elevated temperatures. The experimental procedure used is described as follows. The metallization was deposited onto substrates of 5000-Å SiO_2 on silicon wafers. The metallization consisted of 700 Å of Cr, and 2500 Å of Ag-Au (17 atomic percent Ag) blend. After evaporation, the Cr-Ag-Au film was etched to form a set of four conductor strips, each 54 mils in length and 0.5, 1.0, 1.5, and 2.0 mils in width, respectively. The die was assembled onto TO-5 headers and the metal can sealed under a dry nitrogen ambient. The 2-mil strip was used for the current density experiments, while the 1.5-mil strip served as a control to monitor the resistance change due to temperature alone. The film temperature was determined from the oven temperature plus the temperature rise due to the resistive heating of the film. A thermal impedance of 190°C/W was employed for the TO-5 header.

The results for a typical 2-mil strip aged for 175 hr at a film temperature of 435°C and a current density of 2×10^6 amp/cm^2 are as follows:

initial resistance (at 25°C) = 11.42 Ω

resistance during test (at 435°C) = 16.2 Ω

final resistance (at 25°C) = 12.91 Ω

The current stressed strip showed a 13 percent increase in resistance, while the resistance of the adjacent 1.5-mil control

TABLE V.- CONTACT RESISTANCE OF CHROMIUM-SILVER-GOLD AND ALUMIUM TO SILICON

Silicon Resistivity, Ω - cm	Impurity Concentration, atom/cm^3	Aluminum, Ω - cm^2	Cr-Ag-Au, Ω - cm^2
p-Type Si			
0.001	1.5×10^{20}	1.2×10^{-6}	1.2×10^{-6}
0.002	6.0×10^{19}	— —	4.0×10^{-6}
0.01	1.0×10^{19}	2.3×10^{-5}	3.0×10^{-5}
0.1	6.0×10^{17}	1.1×10^{-4}	1.5×10^{-4}
0.3	9.0×10^{16}	— —	4.8×10^{-4}
1.0	1.5×10^{16}	1.0×10^{-3}	Nonohmic
n-Type Si			
0.001	1.0×10^{20}	1.9×10^{-6}	1.2×10^{-6}
0.007	1.0×10^{19}	— —	8.0×10^{-5}
0.01	5.0×10^{18}	Nonohmic	2.0×10^{-4}
0.03	1.0×10^{17}	Nonohmic	Nonohmic

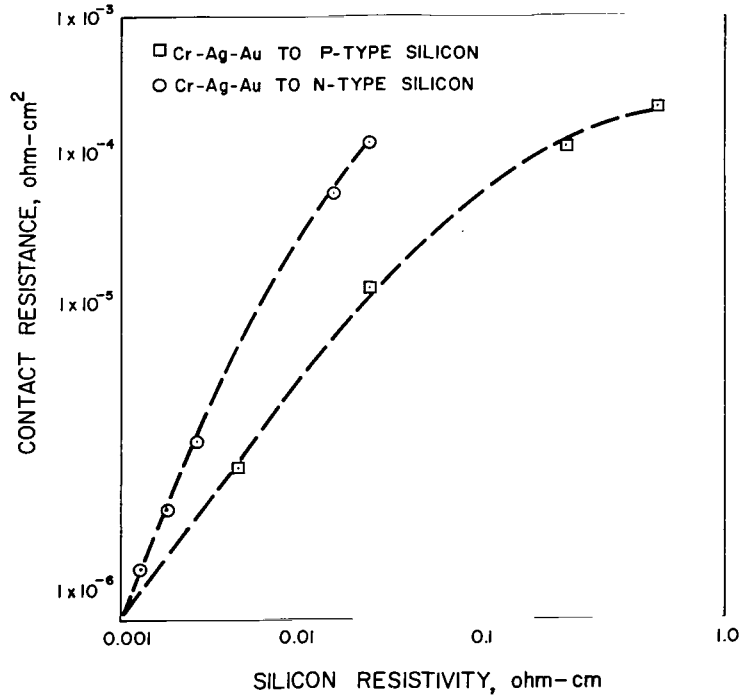


Figure 4.- Contact resistance of chromium - silver - gold vs. silicon resistivity

strip increased 4 percent during the test. There were no open circuit failures of the Cr-Ag-Au metallization when stressed at current densities up to 2×10^6 amp/cm^2 for 500 hr at film temperatures in excess of 400°C. In fact, microscopic examination of the metallization showed no detectable changes in the films due to this aging treatment. It is of interest to note that the mean-time-to-failure for an equivalent aluminum sample is less than 8 hr.

The lessening of the electromigration failure effect is the result of several factors. The activation energies for the self-diffusion of silver (1.93 eV) and gold (1.91 eV) are considerably greater than that for aluminum (1.41 eV), which in itself will reduce the electromigration. In addition, while the blending of the silver and the gold increases the resistivity of the films, the resulting decrease of the electron free path will diminish the electromigration effect in the blended structure with respect to either pure silver or pure gold. In general, the resistivity of the blended Cr-Ag-Au is a factor of two greater than that of the evaporated aluminum. However, the ease with which the Cr-Ag-Au is patterned allows the use of thicker Ag-Au layers in order to decrease the film resistance where that may be a consideration. These factors, coupled with the heavy atomic masses and higher melting temperatures of silver and gold, have resulted in a metallization system which has been shown to be capable of carrying heavy current loads for extended periods of time. This system is thus an attractive one for use in power transistor applications where large currents must be carried at high temperatures.

The Cr-Ag-Au metallization has been used for multilayered metal structures. Two-layered power transistors and three-layered integrated circuits have been fabricated routinely with the above described metallization. No difficulties are encountered in making ohmic contact between the metal layers. Finally, with the glass deposition techniques used for these multilayered structures, there was no observed tendency for the glass to lift away from the Cr-Ag-Au metallization.

Because of the vulnerability of the silver, high temperature exposure of the metallization to an oxidizing ambient increases the film resistivity. The passivation of the metallization with a glass coating results in a factor of ten improvement in the ability of the Cr-Ag-Au to withstand high temperature oxidation. Extended exposure to temperature above 400°C results in the gold diffusing through the silver and chromium, whereby it finally alloys with the silicon.

In summary, the Cr-Ag-Au metallization system, which can be deposited in a conventional evaporator with little increase in

processing complexity, has the desirable characteristics of aluminum metallization. It can be patterned more easily than equivalent thicknesses of aluminum. The Cr-Ag-Au has excellent storage characteristics at 300°C, and has a much longer mean-time-to-failure than does aluminum under high current density, high temperature stress. In addition, measurements show that with the use of an enhancement diffusion the Cr-Ag-Au produces as good or better contact to p-type and n-type silicon than does aluminum. Finally, the absence of significant metallization oxide interaction makes Cr-Ag-Au useful for MOS devices and the ease with which contact is made between layers of this metallization indicates a number of applications for Cr-Ag-Au in multi-layered devices.

Molybdenum-Gold Metallization

The Mo-Au system has been found stable to 450°C, and with adequate molybdenum thickness, alloying of the gold with the silicon is not observed. The Mo-Au metallization is readily patterned and the contact resistance to the silicon is low. It forms stable thermo-compression bonds, and the system is compatible with glassing processes.

Tests of high current density stress have been significant. Circuits have been operated at elevated temperatures with current densities in excess of 10^6 amp/cm^2. Aluminum migration is observed, and at current levels of 10^6 amp/cm^2 and 170°C, lifetimes of the order of 1000 hr are common. In view of the theory that the electromigration is related to the self-diffusion energy of the system, refractory metal, gold metallization systems should show greatly improved high current performance. This has been confirmed in the Cr-Au, Ti-Au, and Mo-Au systems.

Table VI presents measurements of contact resistance of aluminum and refractory metal gold. The results of high current density tests of various metallizations at 175°C and 1 and 2×10^6 amp/cm^2 are shown in Table VII.

BEAM-LEAD TECHNOLOGY

One of the most promising metallization and packaging techniques is known as "beam leads." Beam-lead technology is a process developed to batch-fabricate semiconductor devices and integrated circuits with electro-formed electrodes cantilevered beyond the edge of the silicon. This type of structure simplifies the assembly and interconnection of individual units and integrated circuits, provides its own hermetic seal, and leads to a new class of integrated circuits where isolation is accomplished by etched trenches under the metal interconnections. This structure imposes no electrical penalty on the device, the

TABLE VI.- CONTACT RESISTANCE MEASUREMENTS TO 0.001 ohm-cm p-type SILICON, METALLIZATIONS AT 100 mamp CURRENT LEVEL

Metal	Initial Contact Resistance, Ω	After 15 min at 450°C Air Bake, Ω
Al (evaporated)	0.04 - 0.10	0.021 - 0.022
Cr-Al (evaporated)	0.025 - 0.042	0.019 - 0.026
Cr-Au (evaporated)	0.007 - 0.010 0.023 - 0.026	0.007 - 0.010 0.005 - 0.008
Ti-Au (evaporated)	0.014 - 0.019	0.007 - 0.010
Mo-Au (evaporated)	0.011 - 0.030	0.012 - 0.027
Mo-Au-Mo (evaporated)	0.025 - 0.028	0.026 - 0.028

TABLE VII.- MEAN-TIME-TO-FAILURE AS A FUNCTION OF CURRENT DENSITY FOR VARIOUS METALLIZATIONS

Current Density, 10^6 amp/cm^2	Mean Time to Failure, hr*					
	Al (evaporated)	Al (sputtered)	Mo-Au (evaporated)	Mo-Au (sputtered)	Cr-Au (evaporated)	Ti-Au (evaporated)
1.0	580 (50)	1000 (34)	42,000 (40)	– –	47,000 (20)	58,000 (10)
2.0	28 (57)	– –	32,000 (50)	2400 (22)	2100 (30)	13,800 (10)
2.8	4.0 (10)	– –	– –	– –	– –	– –
3.2	– –	– –	– –	– –	2 (5)	– –
3.7	– –	– –	450 (10)	85 (10)	– –	– –

*Number in parentheses refers to sample size

parasitic capacitance being almost equivalent to a conventional planar device. Basically the process starts with a standard array of planar devices or integrated circuits after the contact holes have been etched through the oxide. Platinum-silicide ohmic contacts are formed in the contact area, and titanium and platinum layers are sputtered onto the silicon. The gold beam leads are electro-formed, using the platinum as a base. The excess platinum outside the gold patterns is removed by r-f discharge etching, and the titanium is etched away. At this point the wafer is turned over and etch-masking patterns are developed in registry over the metallized patterns on the other side. The unmasked areas are etched away, leaving the individual devices with the beam leads extending beyond the edges of the slice. With no additional processing, the previous etching operation may be used to cut isolation trenches in integrated circuits, replacing isolation diffusions or solid dielectric isolation.

The beam-lead structure eliminates the need for chip brazing and external wire bonding. With the beam-lead device facing the substrate, cantilevered leads extending beyond the edges of the chip are readily aligned with matching patterns on the substrate and the beam leads bonded to these patterns. The beam leads are used as the alignment guide — with multiple leads extending beyond the chip where one lead automatically registers the rest, since both the beam-lead array and the substrate pattern are precisely oriented with respect to each other during the photo-lithographic operation. The Au-Au bond is a very reliable metallurgical system; there are no oxide films to hinder the bonding, gold is one of the most ductile metals, thermocompression bonding occurs at low temperature (300°C), and the bond formed is free of attack by oxidation, galvanic corrosion, or other corrosive media.

The application of beam-lead technology to discrete, chip-integrated circuits has been applied to two DCTL with three and four inputs. There are seven, high-frequency silicon transistors (3 leads) and nine, beam-lead, boron-diffused silicon resistors. Several circuits wired as a 3-stage ring oscillator, with a fan-in and fan-out of 1, yield a measured propagation delay of 4.2 nsec. Measurements are made with a collector supply voltage of 5 V, correspondent to an average power per gate of 23 mW. This is equivalent in performance to circuits fabricated with standard chip and lead construction.

Beam-lead transistors have been applied to a tantalum thin-film circuit, a 3-2 input gate DCTL switching circuit. With this structure, it is not necessary to braze the silicon chips to the substrate, subjecting precise resistors to the bonding temperature

required for eutectic brazing. Ultrasonic or split-tip resistance weld may be employed to attach the beam-lead devices to the metallization.

Specific application of beam-lead techniques to monolithic integrated circuits leads to the etching away of the unwanted silicon from under the beam leads, isolation of silicon is attained, and interconnections are made by beam lead. The only capacitative coupling is then through the small, metal electrode overlay (0.105 pf typical). This is many times lower than the stray capacitance incurred with p-n junction isolation monolithic circuits. Ultrahigh speed switching circuits are possible with this technique with no increase in processing complexity. The isolation trenches are automatically formed during the silicon etching.

In the beam-lead process platinum silicide is used as the ohmic contact material. It is one of the most stable compounds of silicon, is corrosion resistant, is a solid phase up to 980°C, has optical reflectivity different from either silicon or platinum, and forms ohmic contact to heavily-doped silicon. To form the compound in contact holes, platinum is sputtered onto the whole slice after the contact holes are opened in the oxide and heated to 700°C, while still in an inert atmosphere. The platinum in the holes will react with the silicon to form Pt_5Si_2, which is a solid phase and will not ball up or creep beyond the edges of the contact holes as a liquid eutectic will. In addition, the silicide is a different color from platinum and can be easily distinguished under a microscope. The next operation is to apply a material that will bond to both the SiO_2 and the Pt_5Si_2 and serve as an electrical connection to the external circuitry. No single element will satisfy all these conditions; however, a composite layered structure consisting of Ti-Pt-Au has been successfully employed. The first layer, titanium, is chosen because of its high oxygen activity, refractory nature, and ability to absorb almost half its weight in reaction products interstitially (commonly known as gettering). Also, it forms a natural oxide which is completely passivating at temperatures up to 400°C. Although other metals such as zirconium and hafnium would probably be adequate, successful prior experience with titanium active metal, semiconductor contact on devices, such as shallow junction solar cells for communication satellites and high frequency silicon transistors, makes titanium a logical choice for the oxide bonding layer.

Gold is chosen as the outer layer because of its extreme resistance to corrosion, ease of bonding, low yield point, high elongation (allows for thermal expansion mismatch with the silicon substrate), and suitability for high resolution electro-forming. However, gold is a metallurgically reactive material and reacts

with titanium chemically at relatively low temperatures to form compounds which have none of the desirable characteristics of the individual metals.

This leads to the use of the metal in the middle layer; platinum is chosen as a filler because of its inertness, ease of bonding the gold outer layer, and the low diffusion coefficient of gold into platinum. The method used to deposit the 0.5-mil thick, gold beam leads is electro-forming, the build-up of material by electroplating in selected areas. This technique has been developed to the point where extremely small geometries are feasible. The use of high resolution KPR dimensions under 0.2 mil is possible. The electrode fingers are etched to a thickness of 0.2 mil, thinner than the 0.5-mil thick, beam leads allowing the close spacing necessary for high frequency operation.

Beam-lead devices have been centrifuged to 135,000 g without failure. Bending tests performed on the leads have yielded twenty 90° bends before breakage. Corrosion testing for periods up to 1000 hr in 360°C steam and 350°C wet NaCl has revealed no physical or electrical degradation of beam leads. In addition, temperature cycling and galvanic corrosion aging have been equally harmless. As a by-product of the metallization procedure Pt-Ti-Pt-Au, there is considerable enhancement of surface stability and junction quality. This is attributed to the use of sputtered titanium, a highly energetic gettermetal particularly for p-n-p transistors which are extremely sensitive to collector channel formation. Forward junction characteristics have been monitored during aging in hot corrosive atmospheres. Typical resistance changes on contact areas of 0.2 x 1.6 mil are under 0.1 ohm after 1000 hr in 350°C air or steam. Obviously no problem has arisen with this metallurgical system since if formed at any of the metal interfaces would yield an increase in contact resistance or would require burning-in. In conclusion, beam leads, as a semiconductor interconnection technique, lend themselves to high frequency, silicon switching transistors and ultrahigh speed integrated circuits. Beam leads have been shown to be rugged; units have survived corrosive atmospheres and 135,000 g centrifuging. This structure imposes no electrical penalty; parasitic capacitance (under 0.05 pf per lead) is equivalent to wire-bonded and brazed-welded assembly. The beam-lead concept is applicable to many other electronic devices as well. In addition, the electro-formed leads are not required to be of constant cross section. They can taper out as they leave the silicon surface for lower inductance, stripline impedance matching, and even better heat conductance. Isolation for integrated circuits is accomplished as a by-product of the structure. Parasitic capacitance has been shown to be negligible and switch-in times are comparable to equivalent chip-and-wire circuitry. This has been achieved with no increase in processing

complexity over discrete devices. The metallizing procedures developed to fabricate beam-lead devices yield an increase in device reliability; contact resistance is maintained at a low value during stringent accelerated aging tests; and passivation of junction and surfaces has been enhanced. In addition, glow discharge etching has been developed, allowing the design of photoresist produced geometries (down to 1 μ) of inert materials such as rhodium and iridium, compatible with normal device processing. Electro-formed gold patterns of high resolution are employed as standard procedure.

Paladium has been substituted for platinum in beam-lead fabrication of devices which could be damaged by sputtering or electron-beam deposition techniques. Paladium silicide has essentially the same chemical and metallurgical properties as platinum silicide and can be evaporated from a high purity tungsten coil. Rhodium is also an alternate for platinum in beam-lead processing.

Gold beam leads have recently been challenged both in this country and abroad. It is said that aluminum beam leads have all the advantages of gold beam leads. Additionally, they are easy to bond ultrasonically. The weld is performed without heating, and there are no reliability problems due to contact of dissimilar metals. Test circuits, comprised of three switching transistors, each welded by three ultrasonic bonds upon a thin film and molded in an epoxy, have been subjected to different treatments with the following results:

1. Thermal fatigue of 23,000 cycles — no failures;

2. Thermal shock from 100°C to -40°C — no failures;

3. Humidity tests at 40°C in an ambient of 90 to 95% relative humidity — no rejects on 40 circuits after 8000 hr;

4. Operating life test at 85°C with switching times in the frequency range of 1 MHz — no failures after 250 hr.

Although comparative cost figures are not available at this time, it is reasonable to assume that aluminum beam leads could be attractive from that standpoint also.

As an overall summary, resistance changes at elevated temperatures, adherence properties, and fabrication difficulties indicate that no one system will meet all metallization requirements. We can divide the systems which most nearly meet these requirements into two groups:

1. Low temperature applications, beam-lead or plastic encapsulation;

2. High temperature and long processing; e.g. LSI, multilayer systems.

The combination that could be useful as a substitute for aluminum in these two groups are:

1. For beam leads and plastics; Ti-Pt-Au, Ti-Pd-Au, Ti-W-Au, Ti-Pt, and Ti-Rh;

2. Multilayer LSI; Ti-Mo-Au, Ti-W,Au, Ti-Pt-Cr, Ti-Ag, or Cr-Ag.

This analysis is taken from the data presented in Table VIII.

TABLE VIII.- SUMMARY OF RESISTANCE CHANGE AND AU-SI ALLOYING

Metals Examined	Increase in Resistance (2 hr at 450°C)	Au-Si Alloying (1 hr at 450°C)
Al	0	— —
Ti-Pt	0	— —
Ti-Rh	0	— —
Ti-Pt-Au	50%	No
Ti-Ag-Au	100%	No
Ti-Mo-Au	0	No
Ti-Ag	5-10%	No
Cr-Ag-Au	100%	No
W-Au	0	— —
Zr-Au	50%	Yes
Nb-Au	100%	No
Ni-Au-	100%	Some
Co-Au	50%	Some
V-Au	100%	Yes
Ta-Au	50%	Some
Cr-Au	100%	Yes
Ti-Au	100%	Yes
Mo-Au	0	No
H_f-Au	50%	Some

It is evident that such composite films are more complex than aluminum to deposit and difficult to pattern; but the versatility of new sputtering techniques in both depositing and patterning present attractive possibilities. Also the excellent

characteristics of refractory noble metal systems with respect to shallow penetration into silicon, excellent resistance to deterioration in adverse environments, and greatly increased current carrying lifetime make their usage most attractive on high frequency, high power devices and large scale integration.

CONCLUSION

In an industry such as integrated circuits, where the technology progresses so rapidly there are probably no two manufacturers who use exactly the same processing to fabricate similar type circuits, the interpretation of reliability data from manufacturer to manufacturer is difficult to attain. In cases where the development of a process has been difficult, and therefore slow, the engineers have designed around this deficiency. This sort of procedure may or may not directly affect reliability; regardless of processing procedures, the specific integrated circuit structure and design can be important factors in determining whether a given metallurgical reaction results in significant degradation of the device characteristics. We have seen from the foregoing discussion that there is one very important conclusion that can be drawn. Most failures observed in presently available integrated circuits at low stress conditions are due to manufacturing defects rather than inherent limitations of the metallurgical systems. If integrated circuits are subjected to stresses far in excess of their ratings, the observed failures will be primarily due to inherent limitations of the materials used. Such inherent failure mechanisms, however, are not necessarily due to mechanisms which are important in terms of reliability of devices under normal usage conditions.

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