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BEAM LEAD TECHNOLOGY

by T. W. Fitzgerald et al.

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PREFACE

This report, based on an extensive and critical literature survey and the personal experience of the writers, has been compiled by the members of the Technical Staff of General Telephone & Electronics Laboratories under the technical direction of Dr. Brian Dale. Mr. John Coulthard was the program manager and Mr. T. Fitzgerald acted as the key person.

In addition to internal reports and documents, the information upon which the report is founded has come from literature searches by our own libraries, the Defense Documentation Center, NASA Scientific and Technical Information Division, and personal visits by several of the authors to companies actively engaged in beam lead work. The authors wish to express their gratitude for the courtesy and cooperation extended them by the personnel of RCA, Sommerville, New Jersey, Bell Telephone Laboratories, Allentown, Pennsylvania, Motorola Semiconductor Products, Inc., Phoenix, Arizona, and Texas Instruments, Dallas, Texas, during these visits.

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SUMMARY

Although the acceptance of the beam lead approach to microcircuit interconnection since its introduction in 1964 has not been as widespread as early predictions would have it, nevertheless there has been considerable effort expended in its application and further development. It is the purpose of this paper to present the present status of the beam lead technology in the areas of Metallization Systems, Surface Passivation, Processing, and Bonding. Additionally, there are sections concerned with the important subject of reliability, and recommendations on the design considerations of the beams themselves.

Much of the subsequent work has been concerned with the practical aspects of the method and, generally, few successful substitutions have been used for the original Titanium-Platinum-Gold metallization in combination with the silicon nitride surface passivation.

A large effort has been expended in the study of bonding beam leads. Many techniques, mostly some form of thermocompression bonding, have been developed for bonding these devices to suitable substrates, and here again gold beams are preferred to those of other metals, including aluminum. The testing of these joints is not entirely satisfactory at this time owing to the lack of a suitable nondestructive test method.

While preliminary data on the reliability aspects are highly encouraging, sufficient information has not been accumulated to accurately establish the hierarchy of values between beam lead and other forms of flip-chip or standard flying wire interconnections. Many of the people actively involved in beam lead work anticipate, perhaps expectedly, that the reliability of beam leaded semiconductor devices with silicon nitride passivation will be at least equal to the best performance previously obtained in any high reliability device and without a hermetic package in the traditional sense.

More recent developments have been concerned with the application of beam leads to surface sensitive devices such as MOS transistors and insulated gate field effect transistors.

INTRODUCTION

While the beam lead approach is but one of several methods of flip-chip technology which have been developed in recent years, it is the purpose of this study to present a critical evaluation of the current developments in the beam lead technology, including device passivation and protection from hostile ambients. Discussed, in turn, are metallization systems and their performance and evaluation, substrates and their qualities as determined by geometry, bonding and thermal properties of beam lead devices, the present status of reliability information, and, finally, a section on the recommended mechanical design considerations for these devices. A complete discussion of the processing used in the preparation of silicon nitride passivated beam lead devices is also included. The final section presents the conclusions drawn from the study and our recommendations as to areas where additional developments are likely to be required.

BEAM LEAD MATERIALS

Metallurgical Systems

Introduction. — Beam lead technology was originally developed by Lepselter et al. (ref. 1) to improve the reliability of conventional wire-bonded silicon planar devices. Since the prime consideration, at that time, was the selection of a metallizing system that would be compatible with silicon planar technology, practically all of the beam leaded devices reported to date are silicon planar devices ranging from simple discrete devices to complex arrays and integrated circuits. There have been, however, several attempts to modify the original beam lead metallurgy to make it compatible with other semiconductor materials. The only successful attempts reported in the literature have been with germanium and gallium aresenide.

The first device to be beam leaded, other than silicon, was a germanium Esaki diode reported by Davis and Gibbons in 1967 (ref. 2). This device had gold-plated beams on sputtered titanium and platinum but used arsenic-tin contacts. A similar device was later reported by Schultz (ref. 3) in 1969 using the identical metallurgy but utilizing a different processing technique.

The first successful attempt to beam lead gallium arsenide was reported by Lynch and Furnanage (ref. 4) in 1967. This device was an electroluminescent array utilizing the conventional beam lead metallurgy but using zinc-gold for P contacts and tin-gold for N contacts.

Since these two devices are the only other semiconductor devices reported in the literature, the rest of this report will concern itself with silicon beam lead technology.

It has been generally accepted throughout the industry that a good beam lead metallurgical system must meet the following conditions:

(1) Resistivity less than 10μ-ohm-cm.

(2) Good adhesion to silicon and dielectrics.

(3) Low contact resistance to P-type and N-type silicon.

(4) Does not form degrading intermetallics between metal layers.

(5) Resists electro-migration.

(6) Resists normal or electrochemical corrosion.

(7) Readily deposited and defined.

(8) Introduces a minimum amount of damage or surface instability while being deposited.

(9) Be compatible with multilevel processing.

(10) Beams must be ductile and easily bonded.

Since the original Lepsetter beam lead metallurgy was reported in 1964, there have been a number of new metallurgical systems reported that claim to be superior because they minimize radiation damage associated with deposition, simplify fabrication, or reduce material and processing costs. While it is true that these systems have desirable characteristics, they generally introduce some other undesirable characteristics which limit their application or decrease their reliability.

Since the properties of a metal demanded by each function vary markedly, it is difficult to find a simple metallurgical system that will satisfy all the requirements. With the exception of the all-aluminum beam lead metallurgy (refs. 5, 6), all other metallurgical systems reported are composed of three or more metals; the contact metal, the bond metal, the diffusion barrier metal, and the beam metal.

The contact metal. — A good contact metal must have high conductivity, low contact resistance, will not degrade at high temperature or high current density, and is easily deposited and defined.

The metals most commonly used for contacts are aluminum, chromium, molybdenum, platinum, palladium, and nickel. Aluminum makes good ohmic contact to P-type silicon and low resistivity N-type as well as performing all of the other functions required. However, as a contact metal, aluminum has some shortcomings, e.g., it dissolves silicon rapidly at high temperatures, which may be augmented by high current densities and it forms rectifying contacts on N-type silicon above 0.1 ohm-cm. Chromium is an excellent contact metal as well as a good bond metal but forms recitfying contacts on P-type silicon over 0.02 ohm-cm. Nickel also makes rectifying contact on high-resistivity P-type silicon and suffers from degrading intermetallic compounds at high temperature. Molybdenum is a good contact material and has good temperature stability but does form rectifying contacts on high-resistivity N- and P-type silicon, above 0.01 ohm-cm. Of all the metals studied, platinum comes the closest to the ideal contact material. It does, however, have one property that limits its use. Due to its very high melting point, it must be evaporated by electron beam or sputtered so that X-rays are present during the deposition which can cause damage to MOS-type devices. Recently, palladium has been suggested (ref. 7) as a replacement for platinum on MOS devices since it can be evaporated from a tungsten filament thus eliminating any possibility of X-ray damage. Since palladium has similar characteristics to platinum and can usually be etched,* it may prove to be a better all-around contact metal than platinum.

*Palladium can be etched in concentrated sulphuric acid at 60°C.

Platinum silicide has been formed at 550°C and at 700°C with no significant change in contact resistance. The higher temperature is necessary where a thin residual SiO_2 layer may exist under the platinum.

The contact resistances of various metals to silicon, with and without platinum silicide, are presented in Table 1. The deposition techniques reported include filament and electron beam evaporation and dc sputtering and were chosen according to the metals being deposited. While specific processing parameters are not given, the results point to the significant reduction in contact resistance resulting from the use of platinum silicide.

The bond metal. — The bond metal must have two basic characteristics. First, it must adhere to metals, silicon, silicon compounds and dielectrics such as oxides, nitrides, or glass. Secondly, it must not react with any material it comes in contact with in a manner that would degrade the metallurgical system either electrically or mechanically. It is important, therefore, that the bond metal does not diffuse rapidly into either the contact metal or the diffusion barrier metal. Although titanium is being used for most beam lead devices without any serious limitation, there are a number of other metals such as chromium, aluminum, zirconium, and hafnium, which could be considered as bond metals because of their adhesive qualities. Aluminum, in fact, has been used by itself to form a complete beam lead system. This system, however, is limited to low current (< 10^5 amps/cm^2) and low temperature (400°C). Since all of these beam metals are very active, they are subject to corrosive undercutting during defining; therefore, they must be deposited in very thin layers.

TABLE 1

METAL SILICON CONTACT RESISTANCE IN OHMS,
AREA = 10^{-4} cm^2

[ref. 8]

Si Resistivity, Ω - cm	Metal and Metal + PtSi									
	Al	PtSi	Mo	PtSi	Ni	PtSi	Cr	PtSi	Ti	PtSi
N-Type Si										
0.001	0.09	0.02	0.08	0.02	0.02	0.02	0.03	0.03	0.01	0.01
0.01	6 (R)	0.1	5 (R)	0.4	2	0.3	3 (R)	0.2	4	0.2
P-Type Si										
0.002	0.03	0.02	0.06	0.03	0.02	0.04	0.04	0.04	0.01	0.01
0.04	1	0.7	3 (R)	1	4 (R)	2	8 (R)	1	--	0.9
0.08	--	--		--	45 (R)	4	--	--	--	3
0.5	20	10	80 (R)	10	100 (R)	20	200 (R)	15	--	15

(R) indicates rectifying contact.

Diffusion barrier metal. — The function of a diffusion barrier is to prevent the formation of degrading intermetallic compounds between the beam metal and the underlying metals. This metal must be relatively inert, form no undesirable compounds with the metals it contacts, and the beam metal must have a low diffusion rate into it. Since this layer must be thick to minimize pinholes and prevent the beam metal from diffusing through, it must be corrosion-resistant to resist attack during processing and environmental testing. Actual interdiffusion rates for many of the metal combinations used in beam lead systems have not been published. The diffusion constant for gold into platinum, 7.8×10^{-11} cm^2/sec at 900°C, is an order of magnitude less than gold into palladium, 1.2×10^{-10} cm^2/sec at 900°C. Palladium, however, has not as yet had the extensive investigation necessary to determine whether any reliability problems due to interdiffusion will arise.

Platinum, palladium, molybdenum, tungsten, nickel, and tungsten-titanium (ref. 9) have all been used successfully in this application. For nonhermetic packages, however, where severe corrosive environments may be encountered platinum is generally selected because of excellent corrosion resistance.

Molybdenum has been used extensively (ref. 10) to fabricate a variety of beam leaded devices. These devices have now been in the commercial market for a number of years with excellent life test data when used in hermetic packages. Molybdenum is also a good diffusion barrier and has the added advantage of being inexpensive and readily defined by chemical etching in the presence of the gold beam, eliminating several costly fabricating steps. Tests have shown molybdenum-gold metallization to be severely corroded in 85°C, 85% R. H. ambients in 48 hours, where platinum-gold metallizations have exceeded 1000 hours in the same atmosphere.

Beam metal. — Since the beam is the contact medium between chip and substrate, special consideration must be given to its compatibility with the substrate metallurgy as well as the chip metallurgy. In general, a beam metal must have the following characteristics:

(1) Good mechanical strength.

(2) Easily deposited in thick layers (> 50,000 Å).

(3) Easily defined by controlled deposition or etching.

(4) High corrosion resistance.

(5) Low yield point.

(6) Coefficient of expansion near to that of silicon or high elongation to overcome mismatch.

(7) High conductivity.

(8) Easily bonded.

Gold, aluminum, nickel (ref. 11), and copper are most often suggested as potential beam metals that could be used in conjunction with a variety of bond and barrier metals. Unfortunately, however, many of these metals systems deteriorate rapidly in corrosive environments which are accelerated if the metals are under electrical bias.

Table 2, compiled by L. Terry (ref. 12), shows the effect of electrical bias on some of these metal systems while submerged in a boiling 1% solution of ammonium hydroxide in deionized water. The vehicles used for testing the metals listed were silicon dice upon which had been patterned parallel "dogbone" conductors to which suitable bonded connections were made. A potential of 10 volts was applied to pairs of the strips while chips were submerged in the electrolyte.

TABLE 2

ELECTROCHEMICAL CORROSION TEST RESULTS

Metal	Type of Failure	Time	Remarks
Al	All contacts open	< 5 min	(–) Terminal somewhat faster
Ti-Pt-Au	Resistance Increase	> 3 hr	Au deplates (+) terminal
Ti-Pt	Slight Resistance Change	> 24 hr	Au wire bond opened
Ti-Rh	Slight Resistance Change	> 24 hr	Au wire bond opened
Cr-Ag-Au	Open (Cr)	< 5 min	Cr from under Ag-Au, even with glass or Si_3N_4 overcoat
Ti-Ag	Large Resistance Increase	< 5 min	Ag corrodes but not removed
Hf-Au	Resistance Increase	> 3 hr	Au deplates (+)
Ti-Ag-Au	Resistance Increase	> 3 hr	Au deplating (+)
Ti-Mo-Au	Open (Mo)	< 5 min	Mo from between Ti and Au
Ti-Au	Resistance Increase	> 3 hr	Au deplates (+)
Mo-Au	Open (Mo)	< 5 min	Mo from under Au, even with glass overcoat
Cr-Au	Open (Cr)	< 5 min	Cr from under Au
W-Au	Resistance Increase	2 - 3 hr	W removed ≅ same rate as Au
Zr-Au	Resistance Increase	> 3 hr	Au deplates (+)
Nb-Au	Resistance Increase	> 3 hr	Au deplates (+)
Ta-Au	Resistance Increase	> 3 hr	Au deplates (+)
Ni-Au	Resistance Increase	> 3 hr	Au deplates (+)
Co-Au	Resistance Increase	> 3 hr	Au deplates (+)
V-Au	Open (V)	< 5 min	V removed (+) from under Au

Although the all-aluminum beam lead system has too many restrictions for general use, it does offer a simple, inexpensive metallurgy for low current applications. A typical all-aluminum system as proposed by C. Mai (ref. 6) consists of a conventional integrated circuit on which a layer of silane glass is deposited and windows are opened over the bonding pads (see Figure 1). This is followed by a multiple source deposition of aluminum until a 5- to 10-micron layer is deposited. The aluminum is then defined and the slice thinned and etched through (see processing section). While these devices did not pass environmental testing, they were able to pass storage and operating life tests at low current density. Failure by electromigration can occur at current densities above 10^5 amps/cm ^{2}.

Platinum and palladium have not been evaluated as beam metals but they have potential in this application for high-reliability devices which are subjected to very severe corrosive environments. The cost would be higher and the bonding would be more difficult but the thermal expansion mismatch would be less and the corrosion resistance would be far superior to any other metal system.

For most applications, however, gold beams are almost the unanimous choice throughout the industry because of the ease of bonding, ease of fabrication, and relatively high corrosion resistance of the gold beam. While gold on titanium and platinum is preferred by most investigators, there have been some recent reports on gold beams on other metal systems such as aluminum (ref. 6) and molybdenum-aluminum (ref. 13).

Generally, these systems have an oxide layer between the beam metal and the underlying metals. This allows beams to be attached to standard chips since a window can be opened over the bonding pads and the beam metal can make contact to the pad through the window and be insulated from the rest of the metallization by the oxide.

Summary. -- The titanium, platinum, gold beam lead metallurgical system has become the industry standard. The all-aluminum system is interesting because of its low cost and simpler processing but is limited to hermetically-sealed packages and low current, low temperature applications. Palladium may be a possible substitute for platinum because it can be evaporated from a filament eliminating any possible X-ray damage.

Substrates

Introduction. -- At the present time, the fabrication of beam-leaded devices has been much better defined that the packaging technology with which they are to be used. A number of packaging schemes have been developed for hybridization of discretely packaged semiconductor devices. These technologies are currently being examined for their ability to accept unpackaged beam-leaded components, and new technologies are being developed with beam leading in mind.

Techniques for providing interconnection patterns compatible with beams and the substrates to form the package are discussed in this section.

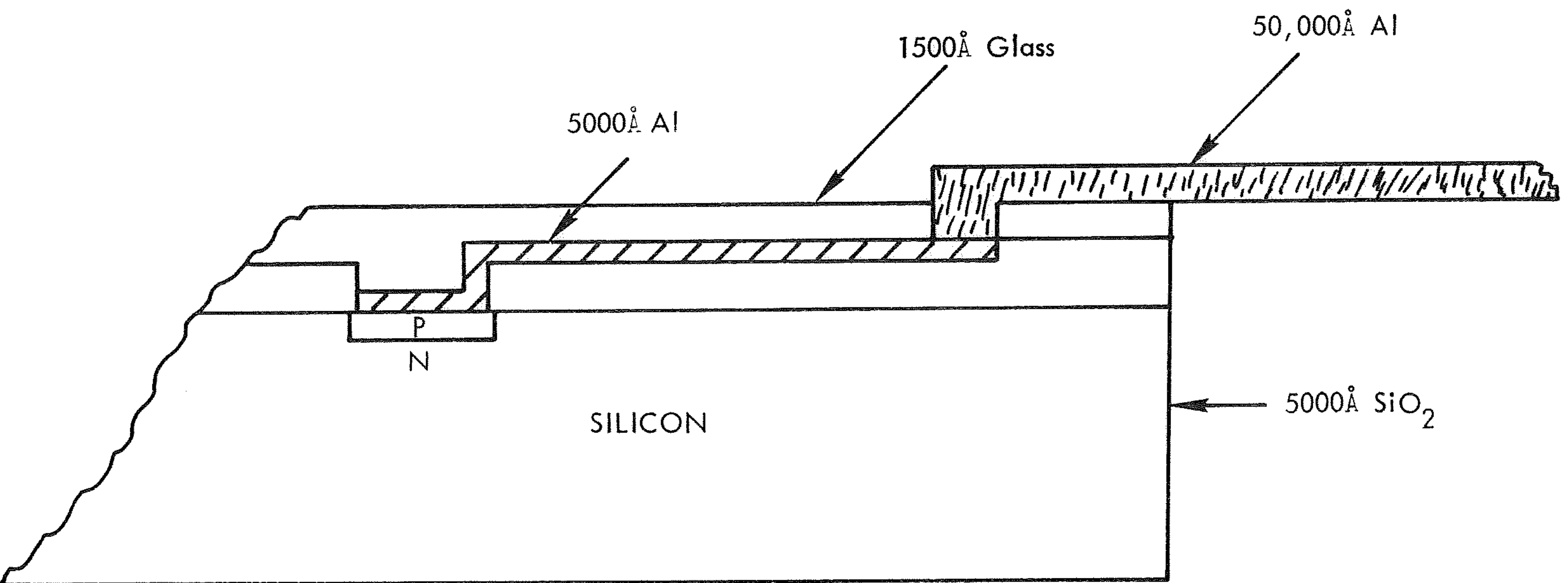


Figure 1. Aluminum Beam Lead System with Separately Deposited Beams

Substrate materials. -- Substrate materials generally fall into two classes for beam leads. Hard substrates, such as ceramics and glasses, are required for high temperature processing, such as screen and fire techniques. Soft substrates, PC boards and other organics, have the advantage of lower costs but lack some of the advantages of the hard substrates. These disadvantages would include poorer thermal conductivity and unsuitability for hermetic sealing. The choice of bonding methods is limited by the inability of this type substrates to withstand bonding temperatures. Some of these substrates, along with their advantages and disadvantages, are discussed below.

Ceramic: Ceramic is probably the most commonly used substrate material for beam-leaded devices. It has the strong advantage of being able to withstand high temperatures and stresses. This property makes all of the beam lead bonding methods practical with ceramic substrates including thermal pulse bonding. It also allows the attachment of heavy external leads and glass hermetic seals. In addition, screen and fire techniques are normally used only on ceramic substrates.

The ceramic most often reported is either 96% alumina (such as Alsimag 664) or 99.5% alumina (such as Alsimag 772). The higher alumina content improves the heat conducting properties. However, the other constituents provide better adhesion for the metals which obtain their adhesive properties on oxides by partial reduction of the oxide. Chromium and titanium are two of these metals.

Surface texture also plays an important role in adhesion. The lower alumina content ceramics are generally supplied with rougher surface finishes (25-μin and greater). The rougher surfaces provide a mechanical factor in metal adhesion. This adhesion becomes important when heavy external metal leads are attached. Glazed alumina provides very poor adhesion for external leads, and other mechanical adhesion aids such as resins are needed with glazed ceramic substrates.

In addition to adhesion, surface finish is critical for thin-film components and metallization. A much thicker thin film (2500 Å) is required for electrical continuity across a 25-μin surface than would be required for a glazed surface (only a few hundred Å). For this reason, selective glazing has been used on ceramic substrates where both thin-film components and adhesive metal films for external leads are required.

Another disadvantage of ceramic substrates is the lack of surface flatness. This is especially true with glazed ceramic. Undulating surfaces lead to variations in line widths, particularly with photoresist defined patterns where the mask does not come in uniform contact over the entire surface. Projection exposure techniques now being developed in the industry may help solve this problem.

The final substrate size is usually formed by sawing with a diamond fritted wheel. Grooved substrates are available which can be broken into predetermined size. However, since the grooving is done in the green state, the accuracy of the pattern dimensions after firing is not easily controlled.

Glass: Glass substrates do not have the problems of surface finish that ceramics do, and are ideally suited for thin-film work and fine geometry interconnections. However, it is difficult to bond external leads to glass and usually a conductive epoxy resin is used for this purpose.

The two glasses most commonly used are Corning 7059 and Corning 0211, the latter primarily because of its low sodium content. It has been reported (ref. 14) that thin glass substrates (15 mil) result in thermal bonds which deteriorate with time, presumably due to stress relief in the glass. Thermal cycling reduces this problem. Thicker substrates (48 mils) do not show this bond weakening phenomenon.

Organic substrates: The printed circuit board is the most widely used of the organic substrates. However, it has several drawbacks as far as beam-leaded devices are concerned. In the first place, the pattern generation techniques most commonly used are too crude to produce the bonding areas for most beam leads. Secondly, the material yields under heat and pressure making thermal bonding techniques impractical. Ultrasonic bonding such as done with ultrasonic wobble tools may be usable, but this has not yet been established.

Other organic substrates, such as Kapton, are rumored to be under development as substrate materials, but have not yet been reported.

Substrate Metallization. -- The vast majority of beam leads are gold and almost all of the substrate metallization systems reported for beam leads incorporate gold as the metal to which the beams are to be bonded. This eliminates any problems with intermetallics that might arise with other metals. In addition, gold interconnections are desirable because of their excellent corrosion resistance.

However, there are annumber of different methods for deposition and definition of these interconnections.

Vacuum deposited systems: Vacuum deposited gold requires another metal to provide adhesion to the substrate. The most widely used of these adhesive metals are titanium, chromium, and nichrome. Besides providing good adhesion, they are easily defined by etching. These layers are kept thin (100 to 500 Å) to reduce lateral corrosion since they are not required for conduction.

The gold itself is either deposited thick (10,000 Å) or, more commonly, deposited thin (500 to 3,000 Å) and electroplated to the desired thickness, usually about 0.5 mil.

Definition is usually accomplished photolithographically by etching.* Direct definition by deposition through metal masks has been reported (ref. 15). However, a limit of five mils on pattern size was observed.

---

*4 KI, 1 I, 4 Deionized Water

The vast majority of literature describes deposition of the gold followed by photoresist masking and etching. However, much finer geometry control can be obtained by vacuum depositing the initial gold and adherent metal and plating up the gold through a photoresist mask. The plated gold acts as a mask for the chemical etching of the excess thin film metals. The technique is similar to the chemical definition of beam leads (p.37).

Thick film conductors: Thick film conductors deposited as inks or pastes are used extensively throughout the industry for hybrid circuits. A large variety of inks are available commercially (ref. 16) including many gold pastes which would be compatible with gold beam leads (ref. 17). Ceramic substrates are used for these materials because of the high (750 to 1000°C) firing temperature required. Definition is obtained by either screening or photolithographic techniques.

Screening is the most commonly used method of defining thick films. However, geometry control limits by this technique are marginal for beam leads, although line widths and spaces of 0.002 to 0.005 inch have been reported in the laboratory (ref. 18). The standards recommended in another section (Dimensional Standardization and Recommentation Section) of this report have been set up to allow for screened substrate metallization providing good control of line widths is present. These fine lines were achieved using 325 mesh screens; finer screens resulted in separation of the components of the ink while coarser meshes gave poorer resolution. Metal masks have also been used to produce fine geometries (ref. 19), but the masks have the disadvantages of being expensive and short-lived.

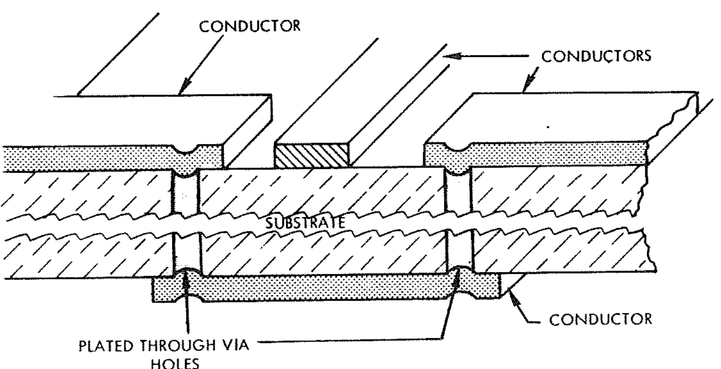
Photolithographic techniques have also been used to obtain finer resolution with thick films (ref. 16). As with etch-defining electroplated gold, this technique is limited by the undercutting obtained on etching thick (0.001 inch) conductors.

In general, the state-of-the-art in thick films limits geometries to 5-mil lines with 5-mil spaces (ref. 20). With this in mind, presently proposed standards call for 10-mil beam spacings. (See Dimensional Standardization and Recommendations Section.)

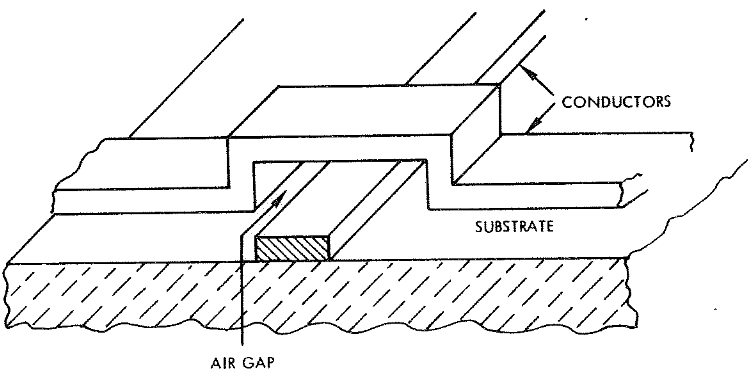
In addition to gold inks, MoMn interconnections have been successfully used with plated gold for conductivity and bonding. A major advantage of this system is that the MoMn can be used in multilayered ceramics for multilevel interconnections.

Decals: Decals are lithographic interconnection patterns on paper or plastic sheets which can be transferred to substrates by either pressure, liquid, or heat transfer processes. A typical metallization system would be moly-manganese with an organic binder. Discontinuities in the patterns which occur during the firing for binder removal step are a major defect mechanism with the decal process (ref. 21).

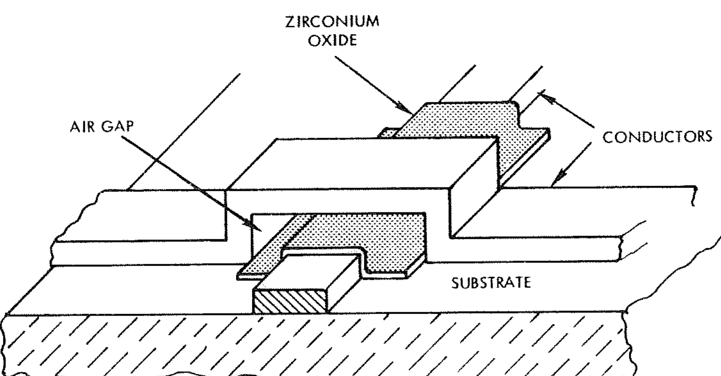
Multilevel interconnections. -- Multilevel interconnections and crossovers are presently being obtained by three techniques: Multilayered substrates, air isolated crossovers, and deposited insulators (See sketch in Figure 2).



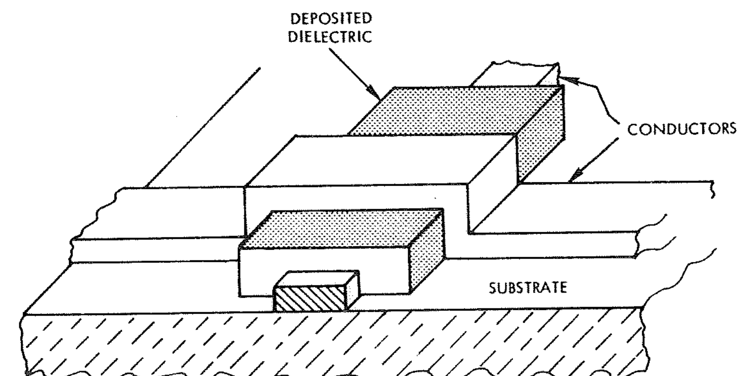
(A) Multilayer Ceramic Isolation



(B) Air Isolated Crossover



(C) Air-Isolated Crossover with Oxide Dielectric



(D) Deposited Dielectric Isolation (Multilevel Metallization)

Figure 2. Interconnection and Isolation Methods

Deposited insulators: Deposited thin-film insulators, such as those used on semiconductors, have not found wide use on substrates. Deposited insulators for crossovers have generally been screened materials. Thick insulators are required to minimize pinholes and capacitive coupling. Photoresist has been used as a binder and definitive media for small geometry insulating pads but this process is still in the experimental stages.

Multilayered ceramic: Multilayered ceramics have been proven as a multilevel interconnection system for beam leads (ref. 22) but are expensive. Screen and fire metallizations along with via-hole plating are used for this technology.

Air isolated crossovers developed at Bell Labs (ref. 23) are not true multilevel interconnections in that all interconnections are on one plane. However, fairly complex metallizations are possible with this technique. The Bell process includes a base gold plated interconnection system, a copper plated spacer, gold pillars plated up through holes etched in the copper, and a gold plated microbridge connecting the pillars. The copper is subsequently etched away to form an air gap.

A similar process (ref. 24) has been developed and uses a gold plated base interconnection pattern, a copper plated spacer, and a second gold plate to thicken the base interconnection and form the bridges.

A thin-film Ti-Zr alloy can be used with the air isolated crossover which, when oxidized, forms a protective insulator over the bottom lead of the crossover in case a bridge is deformed during subsequent processing. The air isolated crossover has the advantage of being capable of much finer geometries than those formed by screening techniques. The process is also being used directly on integrated circuit chips.

Conformal coatings. -- With nitride passivated beam-leaded integrated circuits, hermetic sealing for the sake of preventing chip degradation is unnecessary. However, for many applications where either the die is not nitrided or where protection of external metallization is required, conformal coatings (ref. 25) have been developed both as a sealant and for mechanical protection. More specifically, it is used for reducing thermal resistance as covered elsewhere in this report. A first layer of silicone resin 0.5 to 1.0 mils thick is used as a moisture barrier. This resin is also chosen for its adherence to the die and its ability to penetrate under a face-down mounted die. It must be capable of performing under extended periods at elevated temperatures (1000 hours at 300° C). A second layer of RTV silicone rubber 5 to 10 mils thick is used for mechanical protection not only for the die but also to protect external leads.

Beam-leaded substrates. -- A substrate and interconnection system for mounting conventional chips with connections made by beams formed on the substrate has been developed at Lincoln Laboratory, M.I.T. In this process, holes to accommodate individual die are punched in green ceramic. After firing, the holes are filled with glass to form a continuous surface. The substrate is then metallized and interconnections are formed, including beams extending over the glass. The glass is subsequently

etched away leaving the beams extending over holes. More recently Riston (E.I. Dupont), a photosensitive sheet material has been used to bridge the etched holes in the glass. The beam leads are formed over the Riston, which is later removed either by dissolution or cleaning in a plasma asher. Reliability problems, caused by metal thinning at the step at the bridge edge, can be experienced unless due care is exercised in the preparation and developing of the Riston film. (ref.26).

Individual integrated circuit die are first mounted on molybdenum tabs (for heat sinking) which are then mounted in predetermined locations on a blank ceramic. The beam-leaded ceramic is then joined to the ceramic containing the die with an epoxy so that the beams are aligned with the bonding pads on the die. Bonds are then made either by thermocompression or by ultrasonic techniques.

Both aluminum and gold interconnection systems have been used for beam-leaded substrates. Aluminum has the advantage of compatibility with the aluminum metallization on conventional die. However, the vacuum deposition of adequately thick aluminum beams is a drawback compared to the relative ease of depositing thick gold beams by electroforming. Gold beams can be thermo-compression bonded to standard aluminum chip metallization, but the possibility of Al-Au intermetallic formation exists if high temperature processes, such as cap sealing, take place after the bonds have been formed. The process also lends itself to solder coating beam leads where suitable metal pads have been provided on the device surface to permit reflow soldering to be used as a chip connection technique.

Recently, polyamide films, particularly Dupont's Kapton, have been used instead of ceramics. Multilevel interconnections have been formed by using successive layers of polyamide and connecting layers by bonding beams in windows.

PASSIVATION

Introduction

Passivating dielectric films perform an important function in any planar device structure. This is to protect device junctions which terminate at the surface from ambient moisture and ionic impurities along with maintaining stable device characteristics during field and temperature stress. The following criteria should be met by a passivating film:

(1) High dielectric strength, and high resistivity to allow for stable device performance.

(2) Favorable thermal expansion properties that do not cause high degree of thermal expansion mismatch with semiconductor materials.

(3) Chemical stability, and uniform high density structure which is impervious to contaminants such as ionic impurities, moisture, or organics.

(4) Good interface properties to minimize interface charge instabilities especially in MOS where it governs critical device performance and reliability.

(5) Ease of etching using semiconductor photolithographic processing.

The most universally used dielectric in planar technology is silicon dioxide. It is deposited in the majority of cases thermally by oxidizing the semiconductor silicon material. Although its properties have been optimized by improvements in processing, such as high purity furnace muffles, improved cleaning procedures, and the use of dry oxidizing ambients, it has inherent disadvantages in its lack of resistance to ion migration (1000 Å of SiO_2 penetrated by Na in 20 minutes at 300°C) of alkali metals and permeability by moisture and certain dopant materials. These would include gallium and aluminum.

These facts conflict with the emergence of MIS devices and the need for improved reliability of the dielectric gate, and have caused accelerated investigations of other gate and passivating materials. Silicon nitride, when used as a complement to SiO_2, has been found to remedy many of the shortcomings of the oxide alone. Silicon nitride films have not completely replaced silicon dioxide but are deposited over silicon dioxide and readily complement the interface state properties of silicon dioxide.

Silicon Dioxide Passivation

The fact that silicon dioxide has a high permeability toward impurities is by far the most serious drawback of this universally used dielectric. Due to its porous structure, impurities migrate quite readily through silicon dioxide (ref. 27). Sodium ions (the most common ionic impurity) are highly mobile in silicon dioxide. With the addition of applied fields (10^5 to 10^6 volts/cm) cations will drift in the direction of the field. This field migration of impurities is accelerated greatly by elevated temperatures. The movement of this ionic charge toward the silicon-silicon dioxide interface and the subsequent buildup and termination of an ionic-induced field within the semiconductor material results in degradation of both bipolar and MOS devices.

The presence of cation impurities within the silicon dioxide layers will alter the underlying semiconductor material, depending on the type, in the following ways:

(1) Accumulation - Within an N-type region, electrons will be attracted to the surface due to positive ions in the oxide near the silicon-silicon dioxide interface. This field attraction of majority carrier electrons will cause an excess carrier concentration or "accumulation" at the surface.

(2) Depletion - The same positive ion contaminants in the oxide over a P-type region will repel holes, thus causing a reduction of majority carrier concentration at the surface or an effective lowering or "depletion" at the surface.

Both accumulation and depletion of the semiconductor surfaces alter the carrier concentrations from their bulk values, and hence affect those device parameters which are surface related, e.g., low current gain, reverse leakage current, breakdown voltage, etc. (ref. 28).

(3) Inversion - This effect results from deep depletion of majority carriers (in P-type silicon holes) at the surface. This would be caused by a very high field induced by a large ionic contamination level near the silicon-silicon dioxide interface. With the positive ion concentration, the attraction of the minority carriers to the surface can be high enough to exceed that of the majority carriers (holes). When the concentration of electrons at the surface exceeds that of holes, this surface region changes type. This condition is known as "inversion". This situation will cause the well-known "channeling", or excess current flow, between N-regions previously isolated by a P-region.

In bipolar device structures and integrated circuits, this ionic oxide contamination causes degradation of junction characteristics due to the previously mentioned accumulation, depletion, or inversion effects. Accumulation generally results in lowered breakdown voltage. Inversion, as mentioned, causes increase in leakage current.

Interface charge increases surface recombination velocity which, in turn, lowers transistor gain, especially at low currents.

In MOS transistors, the effect of positive ion contamination can alter the gate threshold voltage (that is, the voltage to induce a channel from source to drain). This can be readily demonstrated in an N-channel enhancement mode device. In order to turn the device on, positive gate bias is applied which attracts minority electrons to the surface until the surface is inverted and a conductive channel is formed. Thus, if positive ionic contamination is present, the positive gate bias will cause these ions to drift toward the silicon-silicon dioxide interface. This ionic charge will attract additional electrons to the silicon surface and terminate this charge at the ionic charge center even after bias is removed. The result of this effect is an unstable threshold voltage which varies with the level of contamination as well as voltage, temperature, and time to which devices were subjected.

Historically, contamination problems in planar devices have been met by first assuming the planar devices would be protected by its own silicon oxide masking. This, combined with protective "glassivation" together with hermetic encapsulation, gave a large measure of reliability improvement. The impetus of MOS technology has developed ultraclean low interface state density silicon oxides. This development has required processing improvements that have proved difficult to maintain, especially in production.

Treating the silicon dioxide surface with P_2O_5 prior to metallization has improved the stability of silicon dioxide. The phosphorus is deposited from a vapor on the silicon dioxide in a diffusion furnace at temperatures from 900°C to 1100°C for times of the order of five minutes. The phospho-silicate glass forms on the device surface as a result of this procedure. It has been established in our laboratories, as well as through the industry, that this treatment will stabilize the silicon dioxide by gettering ionic impurities distributed through the oxide as well as gettering to some degree additional contaminants from the external environment. Depending on the oxide quality and the P_2O_5 treatment (temperature and time), phosphorus can also neutralize sodium ion contamination near the silicon-silicon dioxide interface (ref. 29).

In MOS integrated circuits, uncontaminated SiO_2 is susceptible to external contaminants even with a phosphorous glass coating. Phosphorous glass has limitations on its usefulness because of polarization effects which have been found to be the cause of some device instability in MOST's.

Silicon Nitride Properties

Impetus has been given to the development of silicon nitride processing mainly for two important reasons:

(1) Unlike silicon dioxide, silicon nitride has been found to be a barrier to field-enhanced (10^5V/cm) sodium diffusion even at elevated temperature (400°C).

(2) The highly dense nature of silicon nitride has made it possible to consider eliminating hermetic packaging. This would be replaced with junction sealed hermetic chips. This, of course, will improve the reliability of plastic packaging and increase the use of chips in an unpackaged form.

It also can work as a mask against gallium and aluminum diffusion for which silicon dioxide is not effective (refs. 30, 31) and as a dielectric composite makes feasible development of nonvolatile MOS memory elements (ref. 32).

In addition to silicon nitride's extreme resistance to ionic contaminants, its properties include a high degree of chemical inertness, high temperature strength, extreme hardness, and thermal shock resistance. In fact, silicon nitride does suffer from cracking due in part to its extreme hardness. This cracking does not present any problem unless the thickness of deposit exceeds 2000 Å.

Table 3 presents a comparison of properties of silicon dioxide and silicon nitride. It has been found that thin film deposited silicon nitride has physical, chemical, and electrical properties that vary quite markedly depending on deposition process and conditions. In general, device passivating silicon nitride can be monitored by its etch rate in buffered hydrofluoric acid solution. Details on the process conditions and measurements are to be found in the section on Processing.

Silicon nitride would appear to be a logical replacement for silicon dioxide since it is an improvement over silicon dioxide as both a diffusion mask and as a passive dielectric. Its shortcoming is the instability of the $Si-Si_3N_4$ interface. Such structures exhibit charge instability due to tunneling and trapping at the interface. Hysteresis in surface behavior and the charge instability are eliminated by the use of a silicon dioxide-silicon nitride composite film. Thin layers of thermally grown silicon dioxide covered with a film of silicon nitride eliminates these problems. This composite takes advantage of the excellent diffusion barrier of silicon nitride and the ordered interface properties of clean annealed silicon dioxide (ref. 33). Since silicon nitride does not have as high a dc resistivity as silicon dioxide, this composite system also improves the resistivity over silicon nitride structures alone (ref. 34).

The higher dielectric constant of silicon nitride in a thin silicon dioxide-silicon nitride composite has the beneficial effect of lowering the gate threshold voltage of IGFET structures. In the past, not only the instability of gate threshold voltage but interface problems with other logic elements have limited the growth of MOS devices. The use of silicon nitride with the proper thickness of silicon dioxide (200 Å to 400 Å) results in lower gate threshold voltages compatible with logic levels used with TTL and other bipolar logic circuits. Thus, besides the expected improvement in surface stability inherent in the dense silicon nitride dielectric, MOS technology has received impetus from the improved device performance of $SiO_2-Si_3N_4$ gated MOS structures.

TABLE 3

SUMMARY OF PHYSICAL PROPERTIES

[ref. 35]

	SiO_2 Amorph.	Si_3N_4 Cryst.	Si_3N_4 Amorph.	$Si\text{-}O_xN_y$ Amorph.
Melting Point (°C)	~1600	~1900	--	--
Density g cm^{-3}	2.2	3.4	3.1	--
Index of Refraction	1.46	2.1	2.05	1.60-1.88
Dielectric Constant	3.8-3.9	9.4	7.5	4.77-6.12
Dielectric Strength V cm^{-1}	~5 x 10^6	--	~1 x 10^7	~5 x 10^6
Infrared Absorption Band μm	9.3	10.6	11.5-12.0	9.3-12.0
Energy Gap (e.v.)	8	3.9-4.0	~5.0	--
Thermal Expansion Coeff./°C	5.6 x 10^{-7}	3.0-3.5 x 10^{-6}	--	--
Thermal Conductivity cal cm^{-1} sec^{-1} $°C^{-1}$	0.0032	0.067	--	--
dc Resistivity ohm-cm				
at 25°C	10^{14} - 10^{16}	10^{15}	~10^{14}	
at 250°C	--	--	--	
at 300°C	--	--	--	
at 350°C	--	~10^{13}	~2 x 10^{13}	
Etch Rate in Å/min in 10:1 NH_4:HF	1000	< 0.1	5-10	33-400

[Thermal Expansion Coefficient of Silicon: 3.2x10^{-6}/°C.]

Dielectric Processing

Although the details of the preferred deposition and processing of both the masking silicon dioxide and junction sealing nitride are presented in the Processing section, some general points will be made here.

Silicon nitride, once established as a reproducible process, does not contribute to any instability in a device structure. Potential problem areas in silicon nitride are due to cracking which can occur in pyrolytically-deposited films or blistering which has been found to be due to improper surface preparation prior to deposition. As noted previously, silicon nitride will not contaminate the oxide layer composite which it covers and will only fail as a barrier to impurities when a defect in this film exposes the underlying silicon dioxide.

Silicon dioxide processing. — Silicon nitride, as indicated throughout this section, is best used as a dielectric film overlay. Integrated circuit devices would, in most process film sequences, receive conventional treatment up to and including final diffusion deposition and drive steps.

For bipolar device structures, the quality of the oxide (cleanliness and thickness) is not as critical as it would be in an MOS structure. Here the conventional masking silicon dioxide usually remains and the silicon nitride is deposited over this oxide. In the contact window regions the silicon dioxide is regrown prior to silicon nitride deposition. This allows for the deposition of a more uniform stress-free film and minimizes pitting of the highly phosphorous-doped silicon during the nitride etch.

In general, it has been found that doped oxide layers formed in the diffusion process were not desirable (ref. 36). We have found these doped oxides to cause adherence problems at the nitride-oxide interface and lateral etching difficulties during processing at this same interface.

In MOS structures, a thin, clean, ordered oxide is required under the silicon nitride to eliminate silicon interface instability. Some typical combinations for specific devices are presented in Table 4. Since the device stability is dependent on the quality of the underlying gate oxide, processing of this oxide is critical. In most cases, this oxide is carefully regrown after stripping the gate region. This procedure has been found to be more consistent than to etch back the thicker process diffusion masking oxide prior to silicon nitride growth. Contamination from the etching solution can be trapped in the oxide quite readily (ref. 37). It is best to completely reoxidize the surface after removal of masking oxide (ref. 34). Dry oxygen is preferred for this oxidation since it is easier to control contaminants such as sodium in this ambient.

Silicon nitride deposits. — The most widely used technique of depositing silicon nitride is pyrolytic decomposition followed by synthesis at elevated temperature. The gases, in most cases silane and ammonia, in a carefully controlled ratio, are reacted using a carrier gas (H_2-N_2, etc.) at temperatures from 750° to 900°C. Another reaction

used commonly is the pyrolysis of silicon tetrachloride and ammonia over the same temperature range. The more critical deposition parameters and their effects on the film properties are shown in Table 5.

TABLE 4

SiO_2 - SiN_4 DIELECTRIC COMBINATIONS

	SiO_2	SiN_4
MOS Logic	500 Å	≥ 1000 Å
Bipolar	5000 Å	≥ 1000 Å
Nonvolatile Memories	< 50 Å	≥ 1000 Å

TABLE 5

IMPORTANT SILICON NITRIDE PROCESS PARAMETERS

Parameter		Etch Rate	Film Stress
Temperature of Deposition	↑	↓	↑
Ammonia/Silane Ratio	↑	↓	—
Purity of Reactants	↑	↓	↓
*Total Gas Flow	↑	—	↓
Deposition Rate	↑	↑	↑

*Governs film uniformity.

A deposition temperature range bound on the lower end by growth rate and film density and at the higher end by rediffusion of device structure would be 750° to 900°C. If no difficulties in minimal rediffusion due to device structure occur, the upper temperature level can be raised to 1100°C where crystallites are formed in amorphous films (ref. 37).

Other deposition processes: There are two other deposition techniques which have received attention by the semiconductor industry: rf and dc sputtering, or glow discharge.

(1) Sputtering - The most widely used techniques of sputtering silicon nitride are direct and reactive rf sputtering as well as reactive dc sputtering. Rf reactive sputtering has been found to be superior to dc sputtering because it does not have problems of dissociations, and nonstochemetric deposition (ref. 34). Sputtering must be accomplished without oxygen contamination since it will react more readily than nitrogen to give a silicon oxynitride type film.

Generally, reasonable quality films are deposited by reactive sputtering at a nominal rate of 100 Å/min with a substrate temperature of 200°C. Film density will vary directly with power density and inversely with gas pressure. Unlike pyrolytically-deposited silicon nitride, sputtered films are under compressive stress in the range of $5\text{-}13 \times 10^9$ dynes/cm^2 (ref. 35).

(2) Glow discharge - In glow discharge depositing of silicon nitride, usually an rf technique is used. This glow discharge method has not been as widely studied as the others. The attractiveness of this technique is the low temperature to which the substrate is exposed. The high temperature which is generated within the gaseous discharge initiates the decomposition reaction of the reactant gas mixture. The energy for the reaction is usually supplied to a low pressure gas stream (generally SiH_4 and NH_3) at 10^{-1} torr. This energy is either inductively of capacitively coupled by an rf coil surrounding a quartz reaction tube. Substrate temperatures around 300°C are generally used since higher density films are obtained.

The sputtered or glow discharge deposition of silicon nitride is not generally used in production since high density films are not as consistently obtained as in pyrolsis.

Annealing of passivated devices: Since nitride passivated devices also have an oxide-silicon interface, annealing would be expected to be similar to that used on conventional oxide passivated devices. In most studies, annealing SiO_2 at 300°C to 500°C reduces interface charge particularly that introduced by soft x-rays in electron beam metal evaporation (refs. 38, 39). In order for annealing to be effective with Si_3N_4 - SiO_2 in stabilizing device performance, it has been found that composite contact

windows through the nitride must be opened prior to annealing (refs. 38, 40). This is to allow the forming gas or H_2 to be used most effectively in annealing by permeating the Si-SiO_2 interface to reduce the number of states.

Since most passivating silicon nitride films are deposited at a thickness of 1000 Å to 1500 Å, new techniques of etching have been developed. The three most widely used are:

(1) Use of silicon dioxide in place of photoresist for masking.

(2) Anodic conversion of silicon nitride to silicon dioxide followed by conventional oxide etching.

(3) Sputter etching using photoresist as a mask.

Oxide masking with pyrolitically deposited SiO_2 is the most common method used for selective etching of Si_3N_4. This is accomplished in most cases in the same furnace as the nitride deposition. The etchant used is a mixture of phosphoric acid and water (boiling point about 180°C) which etches silicon nitride much faster than silicon dioxide. Typical etch rates with this solution would be 150 Å/min silicon nitride, 20 Å/min silicon dioxide.

Silicon nitride etched contact windows are very sharp edged and do not have the slope of an oxide window. This causes difficulty with stress and shadowing of deposited metal contacts. Generally, the silicon nitride is deposited over a thin silicon dioxide film in the contact windows. The etching of the oxide is accomplished using the silicon nitride as a mask. This procedure in many cases causes "shelving" (see Figure 3) of the silicon nitride at the oxide interface due to lateral etching of the oxide. This can cause shadowing of the metal deposit, stress, and cracking under thermal cycling.

Reliability and in-process quality control: Potential problem areas in producing a reliable silicon nitride passivated device have been discussed in this section. Process control and quality assurance techniques should be directed toward inspection of the common process difficulties listed below.

(1) Cracking of deposited nitride films due to residual tensile stress at the oxide nitride interface can occur especially during thermal cycling.

(2) Monitor thickness of silicon nitride accurately and do not deposit film at too high a rate ($<$ 150 Å/min) to obtain adequate nitride film adhesion to silicon dioxide. Monitor thermal shock and cycle tests visually on test pieces.

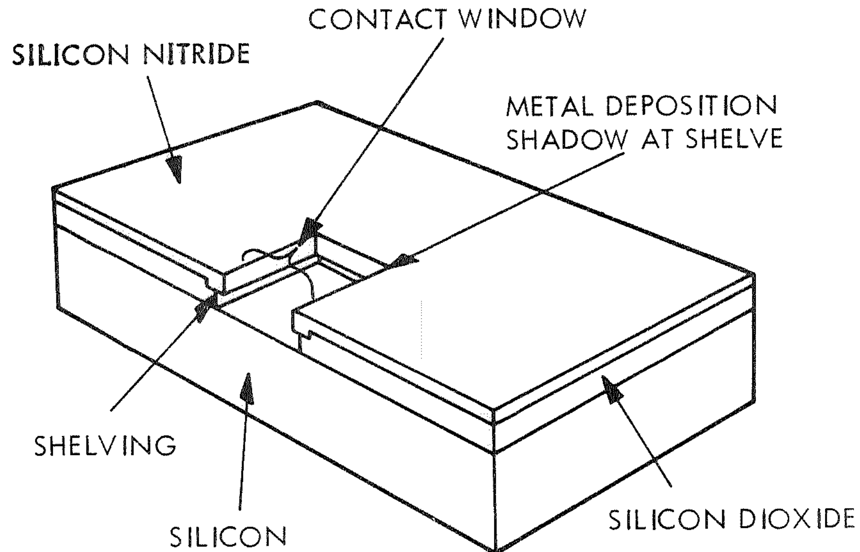


Figure 3. Shelving in Oxide-Nitride Dielectrics

(3) Stability of nitride oxide composite structure is determined primarily by the quality of the oxide since the nitride, when deposited properly, completely seals the device from the outside world.

(4) Oxide quality should be monitored by in-process high temperature bias testing. Shifts in capacitance voltage characteristics of MOS capacitors will be an in-process control of oxide contamination level. Such tests are made on test vehicles immediately after deposition.

The barrier capability of the silicon nitride can be monitored using the same MOS capacitor C-V measurement used on the oxide controls. In this case, films of silicon nitride-silicon dioxide composite can be intentionally contaminated. We have found the etch rate of silicon nitride in buffered HF (25°C) to be a very good measure of film density and quality. Etch rates greater than 25 Å/min are an indication of films which will fail to mask the diffusion of sodium ions and water vapor. A graph of etch versus the density, computed from oxygen content for Si_3N_4 films, is presented in Figure 4.

Completed devices can be evaluated by intentionally contaminating samples with sodium. By reverse bias testing at 300°C using a forming gas ambient, defective junction sealing can be detected readily (ref. 38).

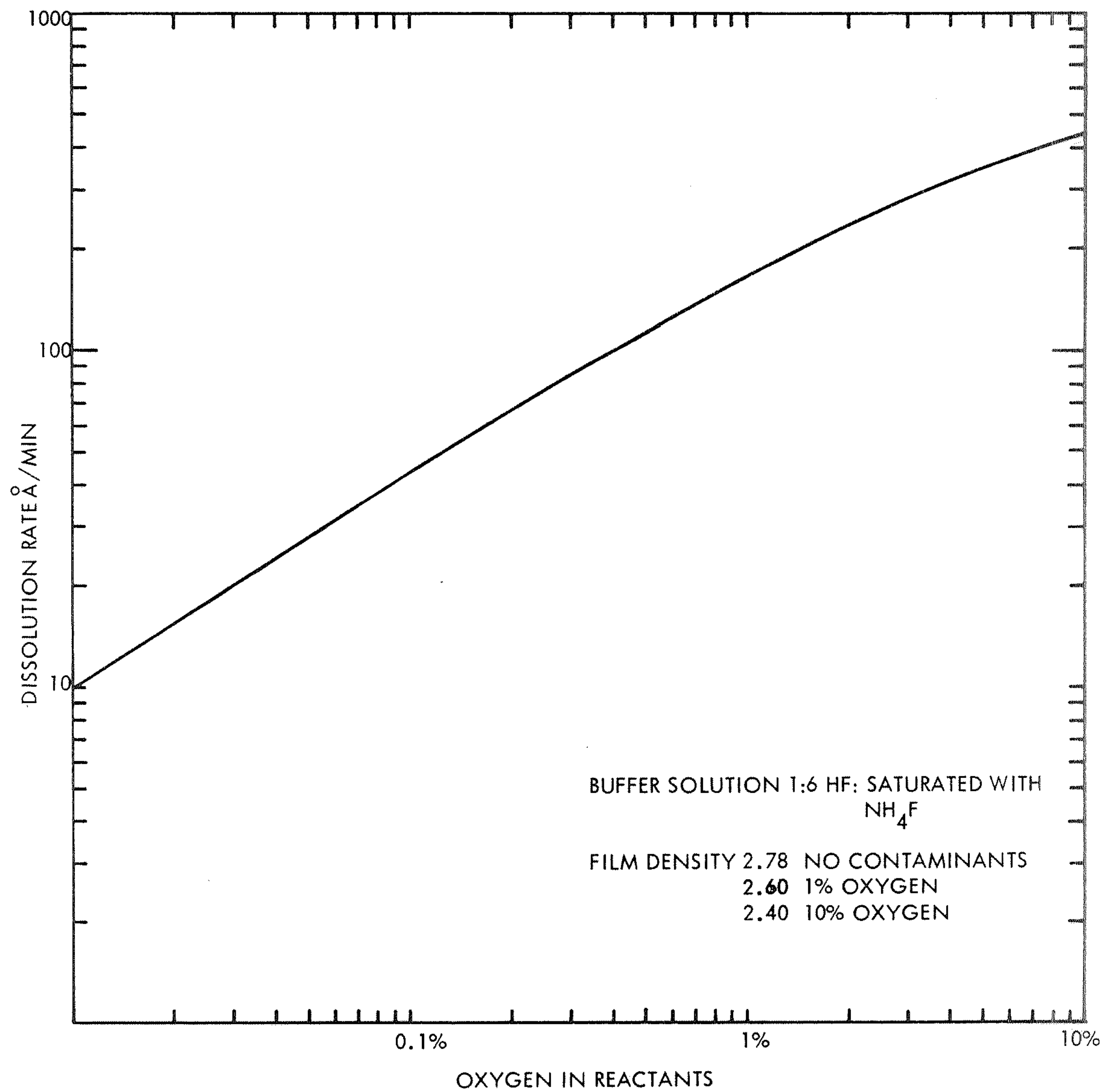


Figure 4. Etch Rates of Silicon Nitride versus Oxygen Content

Radiation resistance: Exposure of oxidized silicon surfaces to ionizing radiation brings about permanent changes in the motion of a positive space charge in the insulation, and an increase in density of fast interface states (ref. 41). Less sensitivity to ionizing radiation has been reported for silicon nitride as a gate dielectric (ref. 42). Stable gate threshold voltages have been obtained with doses of 1×10^{14} e/cm^2 (1.5 mev electrons) for nitride oxide gate dielectrics as compared to 1×10^{11} e/cm^2 for oxide gate dielectrics (ref. 43). Further studies are needed to improve planar device radiation resistance.

Reliability testing: The ultimate reliability of silicon nitride passivated beam lead devices must be verified through life test data.

The intrinsic capability of silicon nitride as a barrier has been well documented in the literature (refs. 27, 38, 39). These studies indicate negligible penetration of sodium into silicon nitride by either thermal diffusion up to temperatures of 600°C or field-enhanced diffusion to 300°C. Many laboratories have monitored silicon nitride-silicon dioxide composites using the MOS C-V measurement technique and have found it to be an extremely effective tool for measuring integrity of the dielectrics (ref. 44).

The life test data of beam lead nitride devices will be treated in the section on Reliability. These data, though limited in scope, indicate nitride-sealed beam lead devices have the potential of hermetic encapsulation in the chip form rather than through conventional packaging. Of course, the metallization system chosen for the beams, intraconnections, and contacts must also be suitable for the rigors of a non-hermetic package.

As indicated previously, some of the reliability of beam lead devices is affected by contacts through the nitride overlay. Nitride contact windows are sharper than oxide windows. Since a composite film is used, the oxide step under the nitride has a lateral etched shelf. This can cause the following:

(1) Discontinuity in metal film contact.

(2) Stress in deposited metal film.

(3) Variation in thickness of deposited metal films (composite metal film used in beam lead).

(4) Alloying at elevated temperature (400°C) due to cracking or shadowing in barrier metal (Pt, Pd).

More studies have to be made especially using a scanning electron microscope as a tool to determine the extent of this problem, and to determine process control improvements needed to minimize the effect in etching this composite film.

Other dielectric films. — The one additional film dielectric that shows promise as both a protective passivating layer and a source of improvement in MIS transistor characteristics is aluminum oxide. This film is used in a composite structure with SiO_2 similar to silicon nitride-silicon dioxide.

The most widely used deposition technique is the synthesis of $AlCl_3$ using both hydrogen and carbon dioxide to hydrolyze $AlCl_3$ to Al_2O_3 (ref. 45). The composite film is processed very much like silicon nitride in that a good quality, clean oxide with low interface density is the initial gate dielectric and the barrier Al_2O_3 is deposited over it. Temperature of deposition is normally 900°C. Al_2O_3 has also been deposited by rf sputtering both on silicon and over SiO_2. Good control of processing and deposition conditions are necessary to produce good quality films (ref. 46).

The Al_2O_3 composite is particularly attractive since it causes a positive shift in threshold voltage due to some polarization at the Al_2O_3 - SiO_2 interface which is not clearly understood at this time (ref. 47). This voltage shift allows for very low threshold device structure.

These alumina layers give good protection against external contamination and, like silicon nitride, the use of Al_2O_3 - SiO_2 composite in practical MOST's is dependent on quality SiO_2 beneath the alumina.

Summary

The efforts within our laboratories and in the literature strongly indicate the following:

(1) Silicon nitride is an effective barrier to ionic contamination and most ambients and is best deposited by pyrolytic deposition.

(2) It is an effective hermetic seal film and, when combined with the proper beam lead metallurgy, gives hermetic seal reliability at the chip level.

(3) It has been found to be completely compatible with beam lead technology and no major failure modes have been introduced by the use of it in combination with beam lead metallurgy.

(4) When used as a composite with silicon dioxide, it improves the reliability and lowers the threshold voltage of IGFET devices.

(5) The only other dielectric that has a good deal of promise at this time is chemically vapor deposited aluminum oxide. This film has some potential advantages in IGFET structures but further investigations are needed.

A thorough review article on the subject of silicon nitride passivation has been used extensively in this section (ref. 35).

PROCESSING

Passivation Processing

Introduction. — Passivation in beam leading consists of a silicon dioxide layer sandwiched between silicon and silicon nitride or, to a lesser extent, aluminum oxide (refs. 48, 49, 50). All agree that the nitride structure produces excellent sealed junction devices. The silicon dioxide under the silicon nitride has the following requirements (ref. 51):

(1) A minimum of interface states.

(2) Few alkali metal ions.

(3) A thickness of > 1000 Å.

Use of the diffusion masking oxide will satisfy these requirements. Properly deposited silicon nitride, 1000 Å thick, has proven to be an effective diffusion barrier to sodium ions.

Preparation for silicon nitride. — Processing for beam leading is considered to start after the completion of conventional IC diffusions. Since high temperature processing is required in beam leading, the diffusion drive time may need tailoring. All photoresist steps used in the process are standard to the industry (ref. 52). When wafers are received after diffusion, they are processed through the photoresist steps to open all contact areas to the silicon. A 5 to 1 buffered hydrofluoric acid* opens the emitter and collector windows. In order to assure that the oxide is completely removed before removing the photoresist, a slice from the lot is tested for continuity in the etched windows. Position probes on the base and resistor adjacent openings, if not conductive, repeat in etch for 15-second intervals until conductive.

Photoresist is removed by placing slices in a commercial stripper, Indust-Ri-Chem Laboratory's J-100, at 140°C for ten minutes and two successive hot trichlorethylene rinses. An acetone dip and deionized water rinse is used. To prevent residues, air drying of wafers is avoided. Drying is accomplished in a specially modified spin dryer where wafers are immediately transferred after final rinse. The use of nitrogen preheated to 150°C allows complete drying in two minutes at 450 rpm, and the reduced speed reduces slice breakage.

RF deposition system. — Silicon nitride is being deposited in an rf reaction chamber; which is the recommended method. Formation of the nitride takes place by reacting ammonia and silicon tetrachloride or silane at elevated

*Buffered HF: 5(600 mℓ H_2O - 400 grams NH_4F)/1(HF) : 900 mℓ/180 mℓ. Assays for chemicals used in preparation of etches are presented in Table 6.

TABLE 6

ETCHING REAGENT ASSAYS

Chemical	Grade	Assay
HNO_3	Reagent, ACS	70.0 - 71.0%
HF	Electronic	49.0 ± 0.25%
HCl	Reagent, ACS	37.0 - 37.8%
Acetic (glacial)	Reagent, ACS	minimum - 99.9%
H_2SO_4	Reagent, ACS	95.5 - 96.5%
H_3PO_4	Reagent, ACS	85.0 - 87.0%
NH_4F	Electronic	40.0 - 41.0%
Absolute methanol (acetone free)	Electronic	99.5% by volume
I (Iodine)	Reagent, ACS	99.8%
KI (Potassium Iodine)	Reagent, ACS	

temperatures (refs. 53, 54, 55, 56, 57). This same system is used to deposit silane glass by reacting oxygen and silane. A typical rf system consists of a 10-kW power supply having a singly wound coil with 15 turns extending 10 inches in length. The reaction takes place in a 2 in. x 3-1/2 in. x 24 in. quartz chamber. A silicon carbide-coated susceptor 1/2 in. x 2-1/2 in. x 8 in. is used to hold the wafers. Because of an interaction between silicon carbide and the ammonia gas, it is desirable to coat the susceptor with several microns of high resistivity silicon. A quartz susceptor holder allows for a 3° tilt. When setting up a system of this type, the number of connections should be kept to a minimum. Stainless steel tubing, of a size adequate to prevent pressure buildup, is recommended. A leak detector is used on all joints except the quartz tube to insure a tight system. The gas input to the quartz chamber should be very large to insure laminar gas flow. Considerable baffling may be needed to obtain uniformity if the input end is not long enough. For consistent results, U.H.P. ammonia and nitrogen should be used. The oxygen is better than 4 - 9's pure. Silane is easier to work with and monitor when obtained in a 10% or less mixture with nitrogen. No refrigeration is needed when using this diluted mixture. Hydrogen has been replaced with nitrogen as the carrier gas, which improves results and considerably reduces the potential hazard. Brooks flowmeters or calibrated leaks are used to regulate gas flows into a common manifold. Automatic valving which heats when in use can cause premature reactions, eventually blocking the valve orifice or changing flow conditions in a calibration leak system. The exhaust gases are directed via flexible stainless steel to a burnoff.

Deposition conditions. — Adherence of the nitride layer to the oxide can be marginal if the oxide surface has been subjected to contamination. Ideally, the nitride should be deposited directly on freshly grown oxide from a high temperature process without intermediate processing. The process calls for an insitu 200 Å silane glass deposit followed by a 1000 Å silicon nitride deposit and a 2000 Å silane glass overlay, all at 900°C. This silane under the nitride provides an excellent interface. Wafers are prepared for deposition by slightly etching the oxide surface in a dilute hydrofluoric acid (10 to 1) for 20 seconds. This removes approximately 100 Å of SiO_2 where most alkali metal ions are located (ref. 58). The etching, deionized water rinse, and spin dry immediately precede the rf deposition. Wafer loading takes place in a laminar flow hood attached to the reaction chamber. With a nitrogen flow rate of 8ℓ/min, the susceptor is positioned into the center of the reaction chamber and purged for five minutes. It has been found that the oxide on some circuits, when subjected to nitrogen at deposition temperatures, becomes pitted. The causes for this are not fully understood; however, this pitting is avoided by purging the chamber for five minutes with 4ℓ/min of oxygen, bringing the susceptor up to temperature in the oxygen ambient and holding it there for five minutes. A slice temperature of 875°C, measured by an optical pyrometer through the quartz chamber, is maintained throughout the run. Nitrogen is metered into the system at 80ℓ/min, the oxygen adjusted to 27 cc/min, and a 1% silane in nitrogen flow adjusted to 270 cc/min. The ratio of oxygen to silane is 10 to 1, yielding a deposition rate for silane glass of 100 Å per minute. After two minutes, the silane and oxygen are stopped and the system flushed with nitrogen for five minutes. Silicon nitride is deposited at a rate of 100 Å/min when the 1% silane flow is adjusted to 270 cc/min, the

ammonia adjusted to 27 cc/min, and the nitrogen flow is at 80ℓ/min. After nitride deposition, allow a five-minute nitrogen flush and reset conditions for a silane glass deposit over the nitride. The deposition conditions are summarized in Table 7.

TABLE 7

DIELECTRIC DEPOSITION PARAMETERS

	N_2	O_2	NH_3	SiH_4	Time	Temp.
Purge	80 L/M				5 min	900°C
First Silane Glass	80 L/M	27 CC/M		2.7 CC/M	2 min	900°C
Purge	80 L/M				2 min	900°C
Silicon Nitride	80 L/M		27 CC/M	2.7 CC/M	10 min	900°C
Purge	80 L/M				3 min	900°C
Second Silane Glass	80 L/M	27 CC/M		2.7 CC/M	20 min	900°C
Purge	80 L/M				15 min	Amb.

Uniformity of deposition is largely dependent on having laminar gas flow and can be controlled by proper baffling at the gas input end. Since 1000 Å of silicon nitride is all that is required and the fact that so little undercutting takes place when etching, a thickness variation of 20% or a range of 900 Å to 1100 Å is acceptable. The first silane glass should be kept thin to facilitate subsequent etching. The second silane glass is used only as an etch mask. Of prime concern is the pinhole density which could effect its masking ability. Low temperature (450°C) silane glass (refs. 59, 60, 61) and pyrolitically-deposited oxide have been used as an effective nitride mask. However, the thickness should be increased to 4000Å due to pinholes in this lower quality glass. It has the advantage of eliminating 25 minutes at an elevated temperature and a disadvantage of adding another piece of equipment and another step to the process. A polished silicon dummy wafer is cleaned with work slices and used as a control. The control is inspected for pinholes and general appearance. Since there are three layers on the silicon, no routine optical measurements can be made. For this reason, on a monthly basis or when gas tanks are replaced, a separate run depositing 4000 Å of silane glass on dummy slices covering the susceptor is made. The glass should look very uniform and nonmilky. When baked for 30 minutes at growth temperature in UHP argon, the

etch rate in "P" etch is 4 to 6 Å/sec. "P" etch is 300 H_2O, 15 HF, and 10 HNO_3 and is used at room temperature. Etch rate is determined by the difference in thickness as measured by an interference technique using a spectrophotometer (ref. 62). Nitride deposited on silicon is measured using the same interference technique. An etch rate of 7 to 10 Å/min is expected using a (6 to 1) H_2O-HF etch. If it exceeds 20 Å/min, the system is cleaned and checked for leaks. Usually an increase in etch rate indicates a leak has developed due most probably to a decrease in film density (ref. 33).

Wafers are masked with photoresist and etched in the contacts and border areas using a dilute (5 to 1) buffered HF etch for 2-1/4 minutes. Wafers are loaded on a teflon carrier for nitride etching. Phosphoric acid, boiling at 182 ± 2°C in a reflux system (ref. 63), is used to etch the silicon nitride with the top silane glass acting as an etch mask. The boiling temperature is adjusted by the addition or evaporation of water. When the system is stabilized, the teflon slice holder is inserted and wafers are etched for 25 minutes. Following etching, wafers are water rinsed and blown dry with N_2. Silicon nitride has an average etch rate of 150 Å/min, but it was found necessary to extend the etch time to assure complete nitride removal. Since no in-process monitor exists, remaining nitride would not be detected until the masking oxide was removed. The result of this over-etching does not affect the devices. The second oxide and the contact areas are etched in (5 to 1) buffered HF. The etch rate is approximately 30 Å/sec. Care must be taken so as not to remove the border oxide which prevents Pt-Si reactions in subsequent processing, yet the windows must be completely oxide-free in order to form silicide.

Metallization Processing

Silicon Contacts. — Cleaning for metallization is very important in order to assure an oxide-free surface on which metal is deposited. A thin oxide or organics will prevent the formation of a uniform contact area. The following procedure has been used which has consistently yielded excellent results. Removal of organics takes place in an oxygen glow discharge (asher) for 30 minutes followed by a two-minute etch (600 H O; 15 HF; 7 HNO_3) immediately preceding vacuum system loading. Others (refs. 49, 64) depend on a sputter etch for precleaning. Sputter cleaning is not preferred since it heats the wafer and can reoxidize the surface if a sufficient amount of oxygen is present, and can redeposit metal from the platen. Various metals have been investigated and evaluated as ohmic contacts to silicon; however, only platinum has, up to now, seen extensive use in beam lead contacts. Electron beam evaporation and dc and rf sputtering of platinum have been investigated. The best results were obtained with rf sputtering. The sputtering system consists of a sputtering electrode for each metal and one backsputtering electrode with four water-cooled platens for slice holding.

After an initial pumpdown to 3×10^{-6} torr, the chamber is backfilled with UHP argon to a slightly higher pressure (25 to 100μ) while pumping against a restriction (e.g., partially opened HV value). This facilitates plasma initiation after which the electrode is presputtered for five minutes with the shutter in place. 500 to 800 Å of platinum is then deposited in six minutes using conditions outlined in Table 8.

TABLE 3

SPUTTERING CONDITIONS

• Source to substrate distance - 1-1/4 inches
• Chamber pressure - 25μ
• Atmosphere - UHP argon
• RF power - 100 watts
• Platen diameter - 7 inches

Formation of platinum silicide takes place at temperatures from 550°C to 700°C. It can be formed inside the vacuum chamber or prefereably in a tube type furnace. Heating in the vacuum system requires jigging which, when heated, adds considerably to the pumping and makes its maintenance requirement quite lengthy. It ties up a system and could cause yield loss if the heaters break down during the cycle. A furnace, on the other hand, is maintained at 640°C and requires very little maintenance. Both $95N_2 - 5H_2$ and argon have been used successfully as the ambient with argon being preferred.

In order to prevent the silicon surface from oxidizing through the thin platinum layer, the wafers are immediately loaded after deposition on to a cool boat in a vertical position parallel to the gas flow. After a five-minute flush, the boat is positioned in the tube outside the furnace end before heating for 20 minutes at 640°C. The boat is cooled at the tube end for 10 minutes. Before heating, the platinum surface is uniformly colored and afterwards is gray in the contact windows. If a change in color is not observed, then silicide was not formed. The excess platinum over the oxide is removed using room temperature aqua-regia which does not attack the silicide. Wafers have been successfully reprocessed through the cycle providing no shallow junction devices are present (< 0.3 microns).

The three major metallization systems in use for beam leaded devices are Ti-Mo-Au, Al-Ti-Mo-Au, and Ti-Pt-Au.

Titanium-molybdenum-gold. — The first system is titanium-molybdenum-gold evaporated by means of an electron beam dual gun, diffusion pumped system capable of co-evaporating molybdenum and gold at a pressure of $< 3 \times 10^{-7}$ torr. Wafers are positioned on an 8-inch diameter rotary substrate holder, having no heating capabilities, 16 inches above the evaporating sources. Evaporations are done in a 24-inch metal bell jar, the surface of which can be heated or cooled with water flowing through brazed-on coils. Walls are heated when the jar is opened to prevent condensation and, during initial pumpdown, to provide outgasing. To increase titanium gettering efficiency and

decrease outgasing during evaporation, the walls are chilled. After obtaining a bell jar pressure of 5×10^{-6} torr, titanium (best available, float zone refined) is evaporated onto the cool bell jar surface, having a shield protect the slices. A rate, determined by a quartz crystal monitor located 16 inches from the source and not shuttered, is adjusted manually to yield 200 Å/min and is maintained for three minutes, at which time the chamber pressure is $< 1 \times 10^{-7}$ torr. The crystal monitor is zeroed and the shutter opened until 500 Å of titnaium is evaporated. Molybdenum should be of ultra-pure quality and deposited immediately following the titanium in order to insure a non-oxidized interface. Because of high resistance and poor adhesion, the molybdenum gold interface has proven to be a weak point unless the gold is codeposited for the last 50 Å or followed by a one-hour bake at 300°C after etching excess metal from between gold beams. Molybdenum is deposited at a rate of 200 Å/min for ten minutes followed by a 1400 Å layer of gold deposited at a rate of 200 Å/min. Measured film resistivities are: Ti = $74 \mu \cdot \Omega \cdot$cm, Mo = 40 to $60 \mu \cdot \Omega \cdot$cm, Au = $4 \mu \cdot \Omega \cdot$cm. The adherence of titanium is greatly affected by the precleaning. If aqua regia is the last step before evaporation, peeling can be seen during the evaporation or if water is allowed to evaporate from the slice surface, peeling takes place. A good pumping system cannot compensate for these poor surfaces. Best results are obtained by an asher treatment for 30 minutes, a two-minute etch in 600 H_2O, 15 HF, 7 HNO_3, D.I. water rinse, and a hot nitrogen spin dry.

Early experiments with this metallurgical system indicated a nonannealable damage to the nitride occurs when high energy methods, such as electron beam evaporation, are used to deposit the metals. The damage produces parameter degradation on MOS devices. C-V measurements on nitride over oxide typically yield flatband voltages of 7V for electron beam evaporated metals versus 0.2V for filament evaporations.

Aluminum-titanium-molybdenum-gold. — A second system uses aluminum interconnects and gold beams (refs. 5, 13, 64, 65). This system has the advantage of accepting wafers from an IC production line following the filament evaporation of 12,000 Å of aluminum. The aluminum is etched in 900 cc H_3PO_4, 30 cc HNO_3 at room temperature for about six minutes using photoresist masking. Wafers are cleaned and heat-treated in a nitrogen furnace at 500°C to 515°C for one hour followed by a 600 H_2O, 15 HF, 7 HNO_3 cleaning for one minute at room temperature for silane glass deposition. A 400°C, 8-inch diameter hot plate having a 6-inch diameter bell jar with uniformly mixed reactant gases is used to deposit the glass. A rate of 250 Å per minute is obtained using 7ℓ/min of nitrogen, 50 cc/min oxygen, and 500 cc/min of 1% silane in nitrogen. Windows are opened in the 4000 Å glass down to the aluminum pad using a 5 to 1 buffered HF for 1-1/2 minutes. For more consistent results, it is best to remove the photoresist and etch for one minute in 600 H_2O, 15 HF, 7 HNO_3 just prior to vacuum system loading. As in the first system, 800 Å of Ti, 2000 Å of Mo, and 1400 Å of Au are electron-beam evaporated to form the basic metallurgy for beam leading. The titanium has excellent adhesion to the aluminum while the molybdenum serves as the barrier metal preventing the formation of gold aluminum intermetallics. The advantages of this system are:

(1) Aluminum contacts have been investigated thoroughly.

(2) It provides the capability to apply the beam lead technology to IC's having standard metallization.

Titanium-platinum-gold. — The third system consists of the Ti-Pt-Au metallurgy (ref. 48). Of the systems used, this one is least affected by surface conditions. Excellent adhesion at all interfaces is commonplace. Initially, the three metal layers were sputtered, but sputtered gold was later eliminated. An rf sputtering system, having a titanium and a platinum cathode located 1-1/4 inches above the target with a shutter in between, is used as the depositing system. Immediately preceding loading, the wafers are cleaned for one minute in 600 H_2O, 15 HF, 7 HNO_3 followed by a D.I. water rinse and a hot nitrogen spin dry. The oil pumped system is as described earlier for platinum. With the shutter in place, a five-minute presputtering is done under a partial argon pressure of 20 microns. This and other sputtering steps in the process, including sputter-etching, are done at an empirically determined rf power level of 100 watts. Presputtering is essential to remove the inevitable residual oxides of titanium present on the cathode. Since titanium is so readily oxidized, trace amounts of oxygen or water vapor in the bell jar must avoided. For this reason, it is important that a good leak-tight system be used. Titanium is sputtered at a rate of 100 Å/min to a total thickness of 900 Å. Platinum is deposited at a rate of 200 Å/min to a thickness of 2000 Å preceded by another five-minute presputtering step. These sputtering rates are empirically determined. This Ti-Pt system has two separate processing procedures. The first one is the etchable procedure (ref. 52) where the platinum, properly masked with photoresist covering the metallization pattern, is etched using a 9 HCL, 1 HNO_3, 10 H_2O etch at 75° to 80°C. This takes 1-1/4 to 1-1/2 minutes and leaves the titanium as the conductive metal for gold plating. The second procedure requires gold plating directly on the Pt surface using the Ti and Pt as the conductive metals for gold plating. Table 9 summarizes the advantages and disadvantages of the two procedures.

TABLE 9

COMPARISON BETWEEN CHEMICAL AND SPUTTERING ETCH DEFINITION SYSTEMS

Chemical Etch	Sputter Etch
Advantages	
• Batch Processing	• Uniform current density during plating • One less photoresist step • No undercutting of PT • Excellent definition
Disadvantages	
• Control of etching uniformly • Photoresist adherence during hot HCL etch • Nonuniform plating	• Limited to small batches in sputter etcher • Shorting between beams

Gold plating. — Gold beams are electroformed in two steps using separate photoresist techniques (ref. 52). A positive type resist, Shiply AZ1350, is used for the interconnecting metal since fine line geometries are needed. In the second plate, where fine geometries are not needed, a negative resist, KTFR, is preferred because of better durability for the longer plating times required. Various types of slice holders are used; however, all strive to prevent plating on the silicon back surface by pressing the wafer against a nonconductive flat surface. Acid type gold baths (refs. 52, 67), having a gold content of 0.7 to 1.5 troy oz per gallon, a density of 14° to 16° baume, and operating at a temperature of 45°C are suitable for plating interconnects and beams. In addition to adhesion, thickness and ductility are the prime concern. Thicknesses are checked optically during the course of plating. A microhardness test (see Bonding Section) after plating is used as a measure of ductility. The ductility is affected by the plating rate and inclusions, both metallic and organic.

Organics are controlled by carbon activation. The gold content, ph, and density are adjusted weekly. Metals which are known to harden gold are maintained at quantities $< 1\%$. Cadmium, for instance, has been found to be a contaminant (ref. 68). Metal parts in contact with the plating solution should be gold-coated with the exception of the platinum-coated titanium electrode. Interconnecting metal is plated to 0.1 mil using 3.5 mA for 40 minutes. Beam buildup requires 3.5 mA for 90 minutes to yield a total thickness of 0.5 mil. A current density of 2 to 3 amps/ft^2 is used. A chip is taken from every fifth processed slice and air-baked for 15 minutes at 350°C and compared with the mother slice for beam discoloration. Grossly contaminated plates are detectable using this technique. Completed wafers are baked for 1.5 hours in a nitrogen atmosphere at 350°C to improve beam adherence.

Definition.

Titanium-platinum-gold (chemical etching technique): Titanium is etched from between the beams using a 9:1:1 (sulfuric, hydrofluoric, water) etch for approximately ten seconds at room temperature. Gold beams are used as the etch mask. Care should be taken so as not to overetch, to avoid beam undercutting and weakening of the beam adhesion. This is the most widely used technique today.

Titanium-platinum-gold (sputter etch technique): Removal of the platinum using gold beams as the mask is accomplished by sputter etching. Sputter etching can also be used as an insitu cleaning prior to metal deposition. Uniform removal from areas having a width of < 0.2 mil are practical without undercutting the larger areas, a drawback in chemical etching. An rf system, as described in the Metallization section, with a sputter etch station is used. Slice holding platens are made of aluminum because its low sputtering efficiency reduces possible redeposition onto the wafer and its ability to uniformly remove heat reduces the generation of hot spots. The platen should be flat so as not to affect the rf field. Initial pumpdown is to the low 10^{-6} torr range.

Either of two procedures can be followed for effective platinum removal. One is to use argon as the ionizing gas; this depends upon knowing fairly accurately the

removal rate. Using empirically determined time, partial pressure, and power, the bombardment can be stopped somewhere in the titanium layer. This requires a thicker titanium layer to insure platinum removal.

The second procedure is to meter in separately oxygen and argon to form a 10% oxygen in argon ionizing gas. This method causes the titanium, when reached, to form a very slowly etching surface oxide which protects the thin titanium below. Larger platinum thickness variations can be tolerated. In both cases, the thickness of gold has to be increased slightly to compensate for removal during etching. Practical sputter etching parameters are a partial pressure of 45 microns and an rf power of 100 watts. Target distance is fixed at 3/4 inch. Sputter etch rates have been determined to be 200 Å per minute for platinum and 90 Å per minute for titanium. The thin oxide on the titanium can be removed by sputter etching in pure argon after pumping the oxygen. In doing this, the less than 400 Å of titanium is free of oxide and is etchable in 20 seconds using concentrated sulfuric acid at 90°C. Sputter etching is being perfected at this time. One of the difficulties with sputter etching is the shorting between beams probably caused by redeposition of platinum along the edge of the nitride.

Titanium-molybdenum-gold: Each metal is removed selectively using chemical etches. Gold is removed at about 200 Å per second using 4:4:1 (potassium iodide: D.I. water-iodine) etch. Molybdenum is etched in 1-1/2 minutes using a 2:2:1 (acetic: phosphoric: nitric) mixture. Titanium is removed in 20 seconds using concentrated sulfuric acid at 90°C.

Summary: Both the chemical etch and sputter etch techniques must be considered on their advantages and disadvantages for the particular devices being processed.

(1) Chemical Etching Advantages

Expensive equipment is not required.

Higher volume.

No induced damage to the nitride.

(2) Chemical Etching Disadvantages

Undercutting problem.

Added photoresist step and its possible problems when masking against aqua regia etch.

(3) Sputter Etching Advantages

Eliminates a photoresist step.

Spacing between interconnects and beams can be realized.

No undercutting problems.

Yields are very high.

(4) Sputter Etching Disadvantages

In MOS devices, induced parameter damage to the device results.

Very expensive equipment if purchased specifically for this step.

Increased processing time.

Limited amount of wafers processed per run.

Platinum shorting problem possibly caused by redeposition.

Slice Thindown

Silicon thickness must be critically controlled when using a nonpreferential etchant. Slight variations in thickness result in overetching areas which can significantly reduce yield. Various type carriers have been used for mounting of wafers. They include Lucalox, Vistal (ref. 52), Sapphire (ref. 53), and glass. All disks must be translucent and have < 0.1 mil thickness variation. Economically, used photolithographic plates can be cut and used as carriers. These disks are lapped using 40.3ℓ D.I. water; 1.75ℓ Ethylene Glycol; 1.75ℓ Rustlick (Rust-Lick, Inc.); 8.75ℓ W5 compound (Micro Abrasives Corp., Westfield, Mass.) for 15 minutes. A pattern of circular depressions is etched into the lapped surface using a 4:1 buffered HF etch for 15 minutes. These depressions allow the bi-wax to hold the wafer more securely. The back surface of the disk is masked during etching. Bi-wax (Biwax Corp., #7050) is used to mount the wafer to the carrier disk at 180°C. It is applied to the preheated lapped surface of the disk and allowed to outgas. To insure the removal of air bubbles, a vacuum jar can be used. A preheated wafer is hand-pressed into the wax using a rubber-tipped metal cylinder. Wax thickness is limited to a maximum of 0.3 mil with no visable bubbles. The silicon surface in contact with filter paper is placed on the rubber-coated bottom plate of the hydraulic press. (See Figure 5.) Upon reaching 150°C, a pressure of 200 lbs is applied for the 10-minute heat and the quick cool cycles. No air bubbles should be visable when inspected. Thinning the silicon down to 2.2 mils ± 0.2 mil can be accomplished by grinding, lapping, etch, or a combination thereof. The finished thin-downed surface should be rough in order that the photoresist hold up for longer etch times. Silicon is removed by using the same lapping compound as described in the disk preparation. Lapping is preferred to etching because of better thickness control.

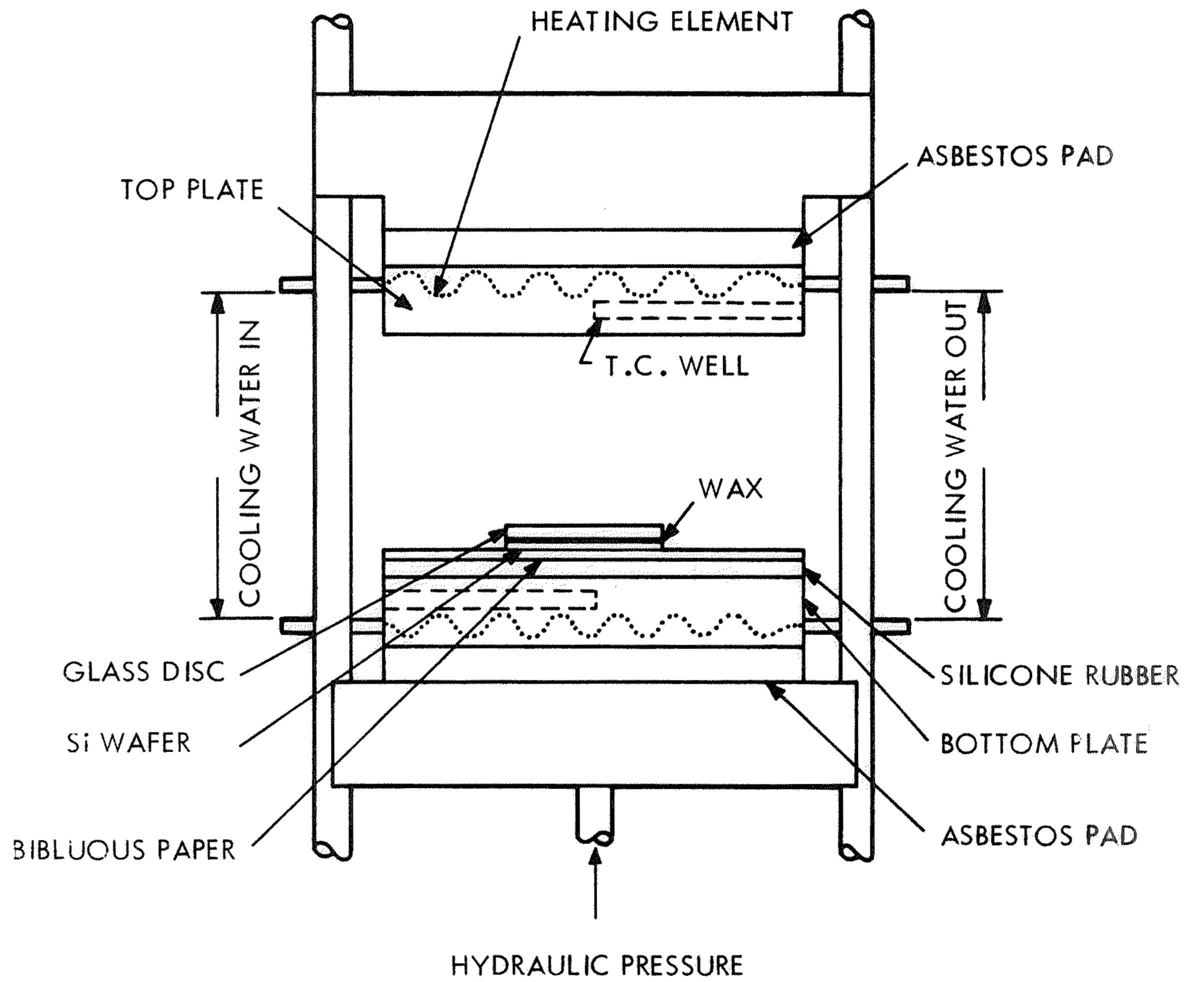


Figure 5. Mounting Device for Wafer Thindown

Silicon Etch-Through

Photoresist is used as an etch mask for die separation (ref. 52). Alignment of the etch-through mask is accomplished by either a dual optics system or an infrared alignment system. The infrared system is affected by surface conditions, and cannot be used to form a metallization pattern on the silicon back side. A dual optics system has none of these drawbacks; however, it does require a prealignment procedure using a test pattern prior to use. Silicon etching for separation can be done using a 5:3:3 mixture (HNO_2:HF:CH_3CO_2H) at room temperature (ref. 52). Reproducable results are obtained using a 5:2:2 (HNO_3:HF:CH_3CO_2H) etch, with a small amount (two drops) of silver nitrate from an eye dropper at -6°C using a rotary etcher. This low temperature is maintained using a refrigerated recirculated mixture of alcohol and water having a specific gravity of 0.95. Silicon has an etch rate of 0.33 mil per minute in this low temperature etch. Slices may be inspected periodically during the etch. Post-baking of the photoresist to obtain good adherence during etching, but allowing removal using a wet air blast, must be controlled. In order to test, silicon dioxide is removed from the back sides of the beams using a buffered HF etch.

Anisotropic etching of silicon (refs. 50, 69, 70) is definitely the preferred process. Use of the preferential etch requires the silicon to be ⟨100⟩ oriented. Increased yield at etch-through, because of better etch control, are the primary reason for going to ⟨100⟩ material. With two-inch wafers being processed through beam leading, yield from the etch-through step can be significantly increased using anisotropic etching, because of reproduceable etching. Thin-down tolerances can be lessened if not eliminated. Finer geometries are obtainable leading to air isolated circuits.

Aluminum System

Two processes have been used to fabricate aluminum beam-leaded devices. The first process (refs. 5, 71) deposits aluminum via tungsten coils to a thickness of 5μ over the entire wafer. The wafers are positioned about 5 cm from the sources and rotated. Precautions are taken to insure a high purity aluminum deposit since impurities in the aluminum can affect the etching conditions. A photolithographic mask is used to define the interconnecting structure and the beams simultaneously. Etching of this thick aluminum limits the closeness of interconnecting metallization, particularly in the contacts. Photoresist adhesion during concentrated phosphoric acid etching can be a problem. Heat treatment of the aluminum contacts (p. 35) follows definition.

With the second method (ref. 6), standard aluminum metallization (6000 Å to 8000 Å) is evaporated, defined, and alloyed with the silicon in the contact areas. A low temperature silane glass is deposited and windows opened through this layer photolithographically over the underlying aluminum in the bonding areas around the periphery of the chip. A heavy evaporation (5μ to 10μ) is used to deposit aluminum over the entire wafer. This deposit provides the metal from which the beams are defined in a final photoresist and etch in phosphoric acid at 55°C.

Standard beam-lead thindown procedures (p. 39) and separation etches are used with both processes.

The second method has the advantages of allowing discretionary application of beam leads following standard IC processing. However, high resistance contacts between the two layers of aluminum may result unless care is taken, similar to that outlined for the Ti-Mo-Au process, to remove contamination or oxide residues in the bonding area windows prior to the second evaporation.

BONDS AND BOND TESTING

Introduction

Since so many of the reliability and, incidentally, cost problems associated with contemporary microcircuit fabrication are to be found in the area of bonded interconnects, it is obvious that any scheme which can reduce both the number of reliable bonds and the complexity of the bonding processes can only result in an improvement in these areas. If, in addition, the method provides the likelihood that the fewer bonds themselves will be more dependable, the advantages to such a technique are even more attractive. The Beam Lead Technology in many ways is just such a system. Here, for the first time, is a system which, among its other advantages, provides the possibility of completely automated handling and bonding systems for complex semiconductor devices. The implications here in terms of consistancy in bonding, reduction of the handling of delicate structures and the relative simplicity of the machinery now available augur well for the reliability of beam lead devices.

Unfortunately, Utopia has not yet arrived. While much work has been done in the bonding of beam leaded devices, their very nature poses some new and unique problems to the chip joining situation.

It will be the intention in this section to discuss the nature of the joining problems, the current efforts in their solution and, where possible, the degree to which the technology is reflecting the promise inherent in Beam Lead.

Since far and away the most commonly used basic technique for joining beam leads is some form of thermo-compression bonding, this method will be briefly discussed first. The restrictions imposed on the system by beam lead, not the least of which is size, and the advantages unique to this approach will be discussed, as will the various adaptations of thermo-compression bonding to beam leaded devices which have been reported.

Other methods of beam bonding have been used and are still under investigation. These, too, will be discussed.

The all-important problem of bond inspection and evaluation, both destructive and non-destructive, which, in the opinion of many, has still not been satisfactorily solved, will be discussed along with its corollary, in-process material and process controls which are slanted toward the ultimate mechanical integrity and bondability of fabricated beam leaded devices.

A comparison of the reliability of the beam lead approach to other methods of automatible bonding systems will be included in the section on reliability.

Thermo-compression Bonding

Thermo-compression bonding has been in use extensively since the late fifties for making electrical connection to semiconductor devices, being originally introduced for the direct bonding of gold wires to active areas of silicon and germanium devices (refs. 72, 73). In more recent years the term has come to mean more — those joints which are effected between two metallic components, such as a fine gauge wire and the metallized surface of a semiconductor or package. Bonds are formed by the diffusion of the components of the joint, under the influence of heat and pressure, across the original interface. As a matter of fact the measure of a good joint is the absence of the original interface where the joint components are of the same metal (ref. 74). When bonds are made with this technique, it is common to achieve joints stronger than the wire. While thermo-compression bonding is a rather straightforward technique, there are some requirements which are necessary to assure reliable bond formation. The most important of these are:

(1) At least one of the members must be ductile at the time of bonding. This prevents elastic deformation which could weaken bonds upon recovery as the pressure is released.

(2) Adequate pressure to promote intimate contact and sufficient thermal energy to cause diffusion to occur in a commercially reasonable time must be supplied.

(3) Clean surfaces in the interface are essential. Those metals with tenacious natural oxides, such as aluminum require special bonding techniques. Thermo-compression bonding of aluminum has for this reason now largely been replaced with ultrasonic joining methods.

In thermo-compression bonding there is no gross melting of the metal in either member (welding) nor is any filler metal used (soldering). One unique advantage to this bonding method is that joints are not limited to the temperature at which they were originally formed. All-aluminum systems, combination aluminum-gold, and, most ideally from the point of view of joint performance, all-gold systems have been used in the manufacture of semiconductor devices.

In practice a wedge has been used to apply pressure to the wire being joined, the amount of force applied being such as to produce the desired deformation which is generally in the range of 20-50%. Because of the notching effect caused by the wedge, the wire itself is weakened if strict control of the bonding parameters is not maintained. Gold ball bonding, the other common thermo-compression method used in wire bonding, geometrically avoids the notching problem and at the same time provides a larger joint area without an increase in wire diameter (ref. 75). Baker and Baker and Jones (ref.76) have advanced the interesting idea that the plastic flow caused by the bonding tool contributes to bond quality. In their view relative metal displacement in the plane of the bond interface produces a cleaning action. The "eyelet bond," which they suggest, is an attempt to maximize metal flow in this plane which, in turn, produces improved interfacial conditions. The sensitivity to bonding force can also be reduced by the choice of heavier, more compliant metallization on substrates or bonding posts (ref. 17).

For a typical thermo-compression bond with gold wire to gold thin films, temperatures in the order of 300°C at the bonding interface are used for a dwell time of 1-5 sec. Pressures of 50 grams are appropriate for 0.001 inch diameter wire, while 250-350 grams are necessary to produce the required deformation in wires 0.004 inch in diameter (refs. 77, 78). Heat is generally supplied via the substrate from a heated clamping device. While the same general conditions are used for gold to aluminum joints, it is necessary to control the pressure and temperature more closely.

Bond evaluation is usually done by 45° pull testing equipment. Bonds are considered good when the break occurs in the bonded wire at a point away from the transition area in the bond at a level equivalent to the ultimate breaking strength of the wire. In the case of one mil diameter gold wire, the ultimate breaking strength is about 6.5 grams.

There are few literature references to specific requirements for the materials used in bonding; however, there is widespread agreement that soft and ductile materials are preferred. Annealing is frequently mentioned in connection with the gold wire. It has been shown (ref. 76) that wire will anneal in the vicinity of the bond under some conditions. (As will be discussed in the section on bonding beam leads, however, it will be shown that this is not necessarily the case with electroplated gold beams.)

Of course, most of the semiconductor bonding operations were done with the aid of manually manipulated machinery, one bond at the time, as indeed were the initial beam lead devices (ref. 79).

This rather brief description of the basic thermo-compression bonding process has been limited to those factors which have been found to have application in the consideration of beam lead bonding using methods based on these ideas. One of the major goads to the development of beam leaded devices was the cost factor which is involved in the manual production of multi-leaded chips. Equally important, moreover, was the inherent variability in such an operator sensitive procedure.

These factors have lead to the development of simultaneous, or at least rapidly sequential, automatic bonding of complex ICs made possible by the beam lead technology which can supply devices with exactly located bonding areas, an obvious prerequisite to automatic handling and bonding systems.

Bonding Methods For Beam Leads

There are a number of approaches to bonding beam leads to substrates based on thermo-compression bonding. These range from manually bonding one lead at a time, similar to gold wire bonds, to the simultaneous joining of as many as thirteen chips, with a total of seventy-six leads, to the same substrate (ref. 80). Machinery has been described which will not only bond beam leads automatically but will also transfer, test and position chips onto substrates (refs. 81, 82). The literature, however, indicates that the presently preferred methods of beam lead bonding lie between these limits, although individual bonding of beams is a popular tool for laboratory work (refs. 83, 84) and GTE Laboratories has developed a tape controlled tool for thermo-compression bonding of beams in opposing pairs, or singly, in any sequence (ref. 85).

The most commonly used thermo-compression -based bonding methods for beam leads at present would include:

(1) Wobble tool

(2) Compliant

(3) Mechanical or electrical thermal pulse

Wobble tool bonding. -- The main additional constraint encountered in multiple-beam-lead bonding arises from the difficulty in providing adequate planarity for the bonding tool. Because of variations in metal thickness, substrate thickness and warpage, not a problem in the thermo-compression bonding of wire or individual beam leads, some form of compliancy between the tool and the bonding surface must be introduced. One such method, termed "Wobble Tool" was developed by Bell Telephone Laboratories and described by J. E. Clark (ref. 86).

With this technique the beams on a chip, which is placed in registration on the appropriate substrate, are bonded sequentially under pressure from a heated tool which wobbles around an axis normal to the back surface of the beams. In the original form of the wobble bonding equipment described by Clark, the wobble action was generated in the work-holding table. Commercial bonding equipment builders have transferred the tilt to the tool, mainly to improve chip handling capabilities (ref. 87). Because only two or three beams are in contact with the bonding surface of the tool at a given point in the cycle, the tool has a tendency to follow irregularities providing more even bonding pressure, especially in depressions. The same action prevents or reduces the deformation of those beam leads which are thicker or higher than other beams on the chip.

Because beams spacings are so small, excessive deformation can cause shorting of adjacent beams as well as weak mechanical connections similar to those experienced when excess pressure is used in the thermo-compression bonding of fine wire. More recent studies (ref. 88) have shown that even on a single chip, variations in the beam thickness of nearly 50% can be accommodated with the wobble tool with no noticeable mechanical weakening.

Beam lead devices are commonly used in multiple arrays on a common substrate containing the necessary interconnecting wiring and often including air-isolated crossovers. It is obviously important that the bonding operation must avoid damage to these delicate structures. With the wobble bonding techniques currently available, the tool can be adjusted such that a crossover as close as 0.006 inch from the end of a beam being bonded can be completely avoided. Such techniques are in use for multichip packages. Since wobble bonding requires no heated work-holding devices for most types of substrate, only the outboard ends of the leads need be heated, and this spares the active device an exposure to temperatures high enough to cause degradation in operating parameters. The addition of ultrasonic energy to the wobble tool may further reduce this factor. Such techniques are currently being investigated in our Laboratories and elsewhere (ref. 86).

A significant drawback in the use of the wobble bonding approach is the limited range of chip sizes which can be handled with a single tool. This would be a particular problem in multi-chip applications where chips of different sizes can be required on the same substrate.

Bonding parameters are also sensitive to the number and sizes of beams on a chip and this too can cause problems in multi-chip work.

Bonding parameters: Aside from mechanical alignment, the essential bonding parameters are time, temperature and pressure. Generally the bonding temperature specified at the bonding interface is 300°C. This, together with the type of substrate, the metallization thicknesses, and tool design will determine the temperature of the tool which is typically in the range of 450-600°C.

Pressure during bonding is set by limiting the deformation as in thermo-compression bonding. The close spacing between beams imposes an additional restriction on the amount of deformation, and the pressure, in order to avoid shorting of adjacent beams. A typical deformation would be of the order of 20-30% in thickness using a tool force of 1.5 to 2.0 pounds.

Two rotations of the wobble tool requiring a total time of 3-4 seconds appears to be standard practice, although one cycle has been found to be sufficient in our laboratory when ultrasonic agitation is added to the bonding tool.

The tools are designed to contact the outboard 50-65% of the beam length. The details on bonding parameters have been abstracted mostly from references 25, 86, 87, and 88 to which the reader is referred.

Compliant bonding. -- Another approach to the problem of planarity in the simultaneous bonding of beam leads uses the equivalent of a soft, conformable tool which can accommodate surface contour irregularities by plastic deformation. Such a technique, called "compliant bonding," has been described by Coucoulas and Cranston of Western Electric (ref. 89).

The compliancy is provided by the insertion of a plastically deformable material between a hard faced bonding tool and the material to be joined. Not only does this material deform to compensate for non-planarity, but it also limits the force which can be applied to protrusions since pressures greater than its elastic limit simply cause it to flow around the protrusion. The use of a compliant medium in the bonding of leads to electronic devices appears to have been particularly successful. Wide ranges in thickness of adjacent lead wires have been successfully accommodated (ref. 89), and the process appears to be relatively independent of the usual thermo-compression bonding parameters once the minimum conditions for plastic flow of the compliant medium have been attained (ref. 80).

The prevalent application of the technique to beam lead bonding calls for the insertion of an aluminum tape, in which a hole a few mils larger than the die has been punched, between the bonding tool and the back side of the beams. When pressure is applied, the 5-10 mil thick tape transmits the force through the underlying beams to the interface with the substrate and causes thermo-compression bonds to occur simultaneously on all bonds under the tape. Since the tape is thicker than the silicon chip, the heated flat-faced tool never comes in contact with the chip. A new tape location must be used for each bonding operation since the metal is permanently deformed in the areas of contact with the beams by plastic flow as the bonds are formed. The operation can be extremely rapid, with good bonds reported in less than two seconds (ref. 89). The fact that the hole in the compliant member must be properly shaped to fit each chip configuration is a drawback to the method. This has been successfully avoided, particularly for the case where chips have beams on only two sides, in a compliant technique developed by H.J. Ramsey of GTE Laboratories. Here a pair of aluminum ribbons whose spacing is easily adjustable is used as the compliant medium. A system of guides maintains these tapes, with the space between them adjusted to the device at hand, between the bonding tool and the backs of the beam leads. Contact between these compliant members and the beam leads is thereby restricted to the outboard ends. The bonding energy from the flat, heated tool is transferred in the same manner as with the perforated tape. As in the case of wobble bonding, the narrow tape limits the action of bonding tool to the extremities of the beams, an advantage in multi-chip work.

Compliant bonding is also admirably suited to laboratory work. Since a heated, flat tool with a smooth vertical motion and capable of delivering a total vertical force of 30-50 pounds is relatively easy to build, the provision of suitably shaped compliant material in alignment with the bonding surfaces is all that is necessary. Substrates, particularly alumina, are generally not flat. For this reason, and because of the large forces involved, the substrate support should be small and centered under the bonding tool if cracking is to be avoided. A small square of 0.005-inch aluminum

shim stock centered under the bonding area has been found to serve the purpose. The amount of deformation can be controlled by the choice of the material and shape of the compliant medium (ref. 89), although 2024 aluminum is recommended for joining gold wires and beam leads to gold metallization patterns. Some restrictions must be placed on the size and surface condition of the compliant medium to prevent the formation of bonds between it and the beam leads or bonding tool. Coucoulas (refs. 80, 89) treats these considerations rather thoroughly. To avoid excessive tool temperatures when bonds are being made to metallized alumina or other thermally conductive substrates, a non-metallic work support is desirable.

In addition to providing compensation for surface irregularities, compliant bonding provides the required control of deformation so necessary with the closely spaced beam leads since material tends to be preferentially extruded toward the chip along the axis of the beams. The reduction of lateral extrusion reduces the tendency for adjacent beams to short. Beam leaded devices with spacings as small as 0.0015 inch have been successfully bonded with this technique (ref. 80). The breaking strength of beam leads bonded in this manner approaches the tensile strength of the beam, and, with the absence of nicking and notching, peel failures generally occur in the beam itself away from the joint (ref. 89).

One of the shortcomings of the compliant bonding technique arises from the problems of compensation for beam hardness. Since a particular compliant material can only develop beam deformation forces up to the yield point, excessively hard beams may not be deformed before the onset of plastic flow in the compliant member. In one lot of beamed chips in these Laboratories, it was necessary to use a nickel compliant layer to produce adequate deformation to form good bonds. Evidently the ductility, or hardness, of the plated materials must be controlled to avoid inadequate deformation.

Mechanical and electrical thermal pulse bonding. -- An aspect common to the methods of bonding beam leads is the idea of supplying a limited but precisely controlled amount of energy to the bonding site. The energy gating can be accomplished mechanically, by controlling the contact time, or electrically, by controlling the amount of energy available. In any case the bonds are formed by the basic thermocompression mechanisms.

Electrical thermal pulse bonding: The electrical thermal pulse method described by Mallery of Bell Laboratories (refs. 83, 84) utilized a tungsten carbide wedge, heated by a current pulse, as the bonding tool. While the method is basically a one-bond-at-a-time technique, it does offer remarkable freedom from the adverse effects of surface contaminants (ref. 83) and a wide tolerance to the pressure and temperature of the bonding tool. Since bonds are made singly, additional topography compensation is not required. These factors make this method ideally suited for laboratory work. The small forces involved and the sharply localized heat source allow this method to be used in bonding beam leaded devices to metallized organic substrates such as Kapton and various printed circuit boards, as well as the more widely used ceramic and glass substrates.

In some applications a loop of resistance wire has been substituted for the heated carbide wedge (ref. 90). Some experience with this technique has been gained in our Laboratory. While successful bonds have been made on the equipment (ref. 85), the drawbacks to the system are numerous. It is difficult to localize the heat at the point of contact between the wire and beam lead. Oxidation and flaking of the refractory wire (usually nichrome) cause the heated area to shift during use, and sliding caused by uncontrolled thermal expansion of the heated wire can damage delicate beam lead structures. In a recently completed study for Rome Air Development Command (ref. 85), a group of beam leads bonded with this technique showed considerably less deformation than normal. It turned out that the beams in this group were harder than usual. From these observations it appears that no significant annealing occurred during the bonding. This may have been due to poor energy coupling with this bonding technique, casting further suspicion on the pulse heated wire approach to beam lead bonding.

Mechanical thermal pulse bonding: This method uses a heated hard-faced ram to supply energy to materials to be bonded. The amount of energy transferred is mainly controlled by the time of contact between ram and the work. It is basically a multi-bond tool and compliancy must be provided. The method has been described by Cushman (refs. 74, 91).

This method, using a suitably shaped tool, gimballed to provide a degree of compliancy, was used for simultaneous bonding of beam leads (refs. 90, 92, 93). Because of difficulties of control of deformation or the larger pressure required (1.5-2 pounds per beam), the method appears to be losing favor to wobble tool and compliant techniques. One advantage, however, that the method shares with wobble bonding lies in the fact that the tool itself can be used as a chip transfer tool with the addition of suitable vacuum porting.

Other bonding methods. -- Eyelet, ultrasonic, parallel-gap, laser, soldering and adhesive bonding methods, though considerably less prevalent, have found application in bonding beam leads. With a few exceptions, most are one-at-a-time bonding methods which can be particularly versatile in laboratory work. Addition utility can be realized by the combination of these methods with tape-controlled positioning equipment such as mentioned earlier. Incidentally, one of the outstanding advantages of the individual bond methods is relief from the necessity of providing specially shaped tools or compliant members to fit each silicon chip, since beam sizes tend to be consistant regardless of the chip dimensions.

Eyelet bonding: Eyelet bonding, which has been demonstrated to provide good bonding in spite of surface cleanliness problems has been used in these Laboratories in the bonding of high reliability beam lead systems for WPAFB (Contract No. F33615-68-C-1632) and in the joining of microwave devices where the maintenance of spatial dimensions is important. Because of the high frequencies involved excessive "Bugging" and beam deformation have proved to be detrimental to the microwave properties of Schottky diodes, PIN devices and capacitor chips. With the eyelet bonds used on these devices, formed with a silicon carbide tool shaped as a hollow cylinder, it was possible to

control the lateral and axial extrusion of the beams and at the same time provide adequate deformation to insure sound bonds. Figure 6 depicts a beam lead eyelet bond. Note the lack of severe lateral deformation. For a beam width of 0.005-inch, a typical eyelet tool would have an outside diameter of 0.004 inch and an inside diameter of 0.0015 inch. Pressures of 350-450 grams would be appropriate. In our practice both substrate and tool are heated; the former to 250°C and the latter to 350°C. The amount of energy coupled to the bond is controlled by the tool temperature and duration of contact, hence eyelet bonding is essentially a mechanical thermal pulse method. The sketch in Figure 7 depicts schematically, the tool shape, the relation of the bonding members and the axial cross section of the completed bond in a beam lead.

Ultrasonic bonding: Both gold and aluminum beam leads have been bonded using ultrasonic techniques. In fact, ultrasonic agitation appears to be the most reliable method with which a reliable aluminum joint can be made. While the method is mainly a single bond system, multiple simultaneous bonds on two sides of a chip have been reported together with a method for providing the still necessary tool-to-bonding surface compliancy (ref. 71). The fact that bonds can be formed at room temperature is also a significant advantage where temperature-sensitive components are involved. The well-known ability of ultrasonic bonding systems to disperse surface contaminants is also an important feature, particularly in the repair of unbonded thermo-compression joints. This spares devices an additional exposure to high temperatures, and is especially attractive considering that surface contaminants may have caused the bonding inhibition originally.

When bonds are made to inorganics, printed circuit boards and other relatively soft substrates, it may be difficult to impart sufficient bonding energy without excessive power levels. The oscillatory displacement of the bonding tip must be carefully controlled with short beam leads to avoid chip damage (ref. 83). Since the bonding tip oscillation occurs more or less unidirectionally, the method is at present limited to single beam joining or multiple beam joining on two sides of a chip. Four sided chips ordinarily require at least two bonding operations. With this limitation in mind, an ultrasonic torsional beam lead bonder is under consideration (ref. 94). In order to bond beams on four sides of a chip simultaneously, a vibration around the vertical axis of the tool is used, in contrast to the more conventional linear oscillation.

Four sided bonding with the addition of ultrasonic agitation to a wobble tool is a subject currently under investigation at these Laboratories. Successful bonds on multileaded chips have been performed at room temperature on this equipment, but sufficient history on this cold ultrasonic method has not been accumulated to permit a thorough evaluation of the process.

The addition of heat to the ultrasonic bonding tool allows the promotion of the necessary deformation and metal flow at reduced ultrasonic energy levels. Coucoulas (ref. 95) has found that increased "liquidity" occurs in the bonding of copper wire at 150-200°C; this prevents strain hardening during bonding, and provides better interfacial contact and crystal structure in the bond areas. Application of such a technique to the bonding of beam leads could result in the more rapid formation of reliable bonds.

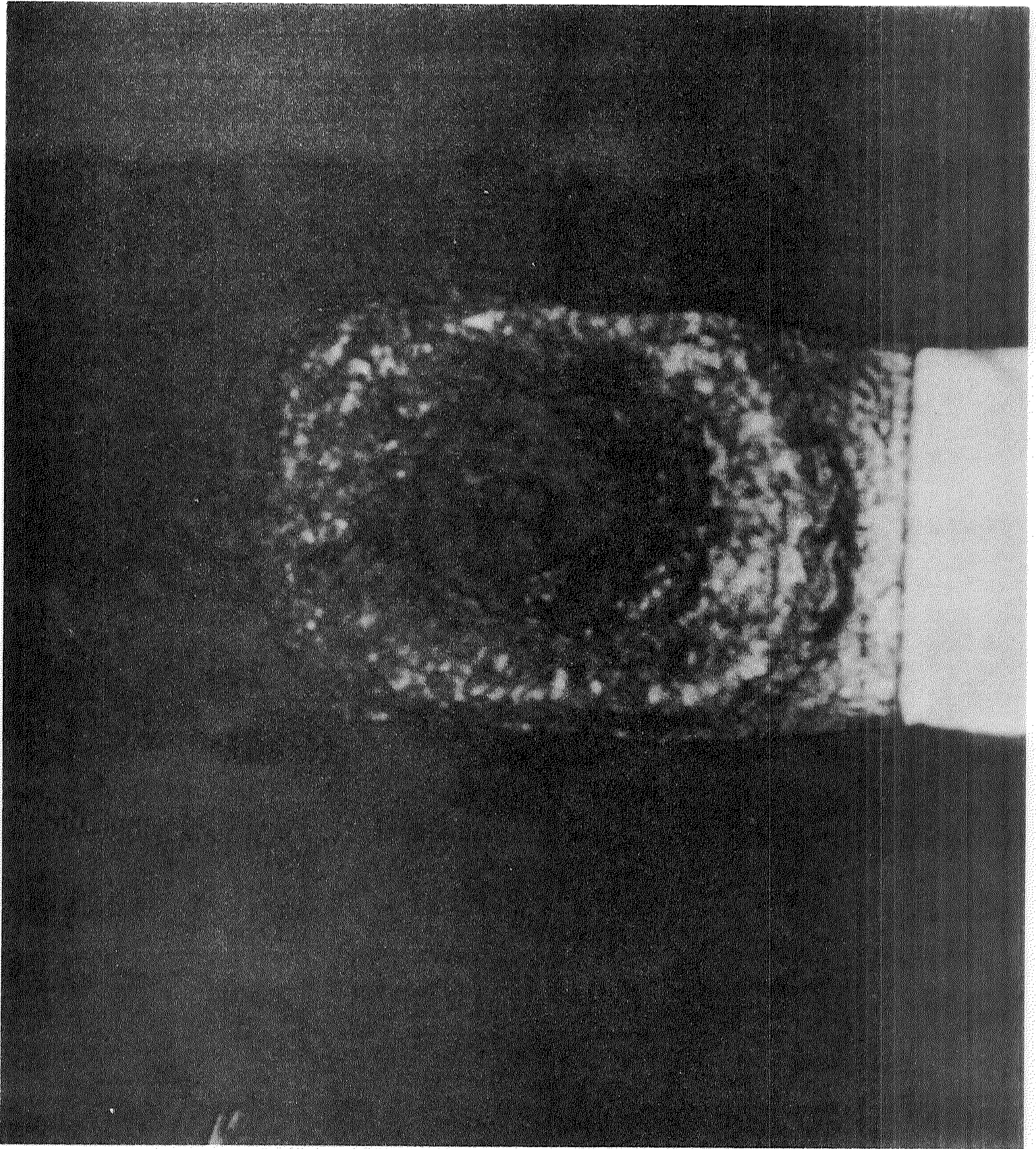


Figure 6. Beam Lead Eyelet Bond

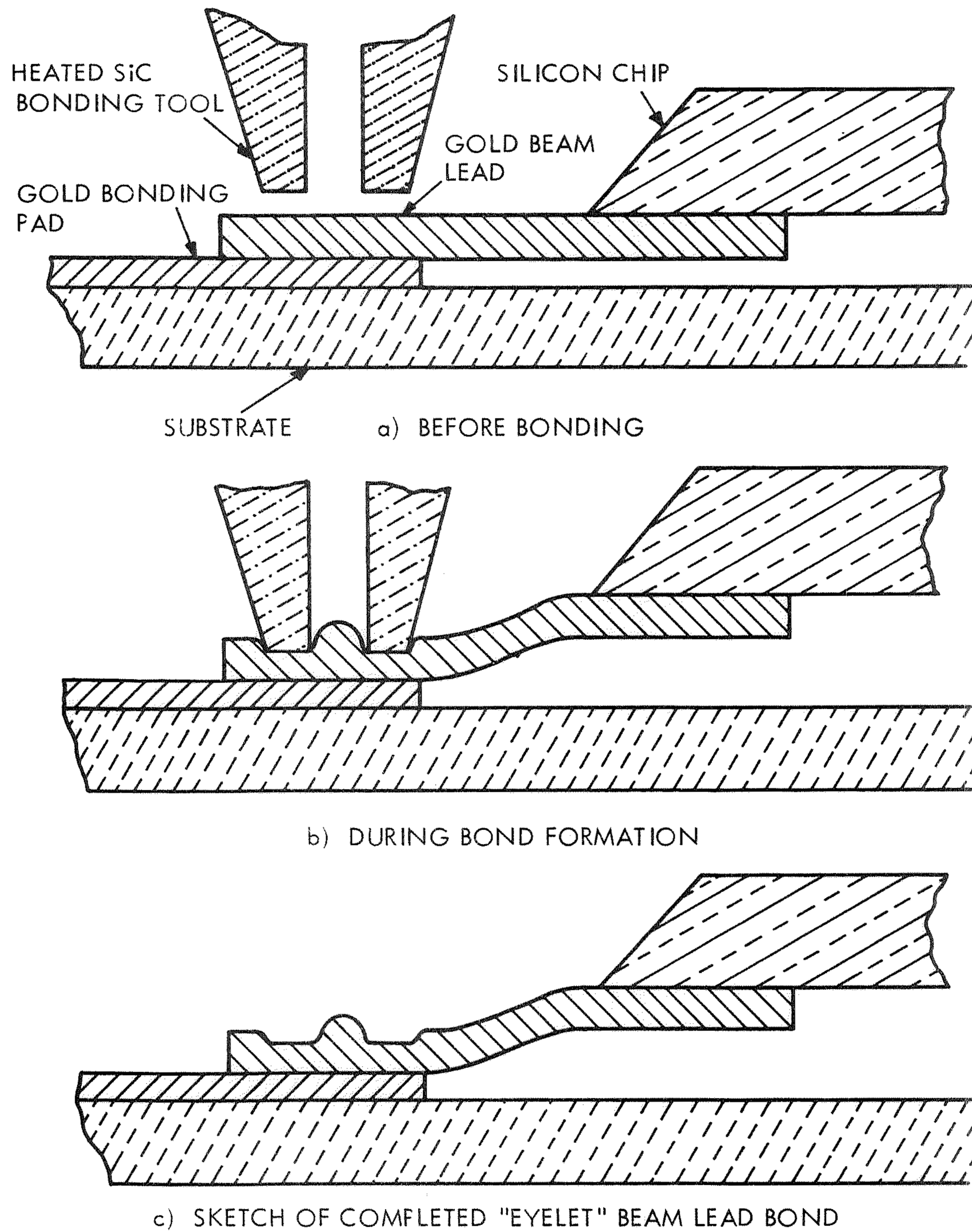


Figure 7. Beam Lead Eyelet Bonding (Not to Scale)

Parallel-gap bonding: In parallel gap bonding, resistive heating in the beam itself, caused by the passage of current through it through a pair of closely spaced electrodes, produces the temperatures necessary for bonding. While the method does have some application in the area of the non-ceramic substrates, it suffers from the varying contact resistance often present on the backs of the beams due to residual SiO_2 or titanium. Maintenance of the tips and the high degree of operator skill required to produce consistant bonds are listed among its drawbacks (ref. 83). As a result, this method does not appear to have widespread use, although parallel gap thermo-compression bonding methods have been used extensively on beam leaded microwave devices (ref. 96). Schematic representation is shown in the sketch (Figure 8).

Soldering and adhesive joining: Soldering and adhesive bonding have both been accomplished internally. Solders with which successful bonds have been made include 95%Pb-5%Sn and the eutectics of gold-silicon and gold-germanium. Gold-tin has been preplated on ceramic substrates and used as a precoated solder in the mounting of beam leaded transistors. Even conductive adhesives, such as silver-filled epoxies, have been used to join beam leads to substrate circuitry. Judging from the available literature, none of these methods are in widespread use.

Laser bonding: Gagliano and Carr (ref. 97) have applied bonding to beam lead devices with some success. Actual fusion of the metals, resulting in strong individual bonds, is accomplished. The technique has the advantage of rapid simultaneous joining of all bonds but is apparently difficult to control. It is a technique which bears further consideration.

Bugging. -- One of the advantages provided by beam lead construction is the potential for mechanical isolation of the silicon device from thermally generated stresses due to differential expansion between chip and substrate. In order to take advantage this feature of the beam lead, care must be taken to preclude the possibility of applying tensile stresses to the beams. In the bonding of beam leads a compressive stress, due to metal flow in the direction of the chip, tends to build up. This is relieved by the tendency of the chip to lift from the surface of the substrate. This "bugging" (ref. 88) causes the beams to bend slightly and reduces shear stresses at the joints and tensile forces in the beams during changing temperature conditions. Excessive bugging, however, can cause peel forces to occur at the chip interface (ref. 25). This is particularly true where an insulating coating has been applied in the space between the bonded chip and the substrate.

The optimum space between chip and substrate depends on the relative thermal coefficients of the silicon and substrate, dimensions of the chip and beams, and the excursion in temperature expected. (Considerable tensile forces can be developed in beams at ordinary temperatures (ref. 98). The most desirable chip-to-substrate spacing seems to be of the order of 0.001 inch.

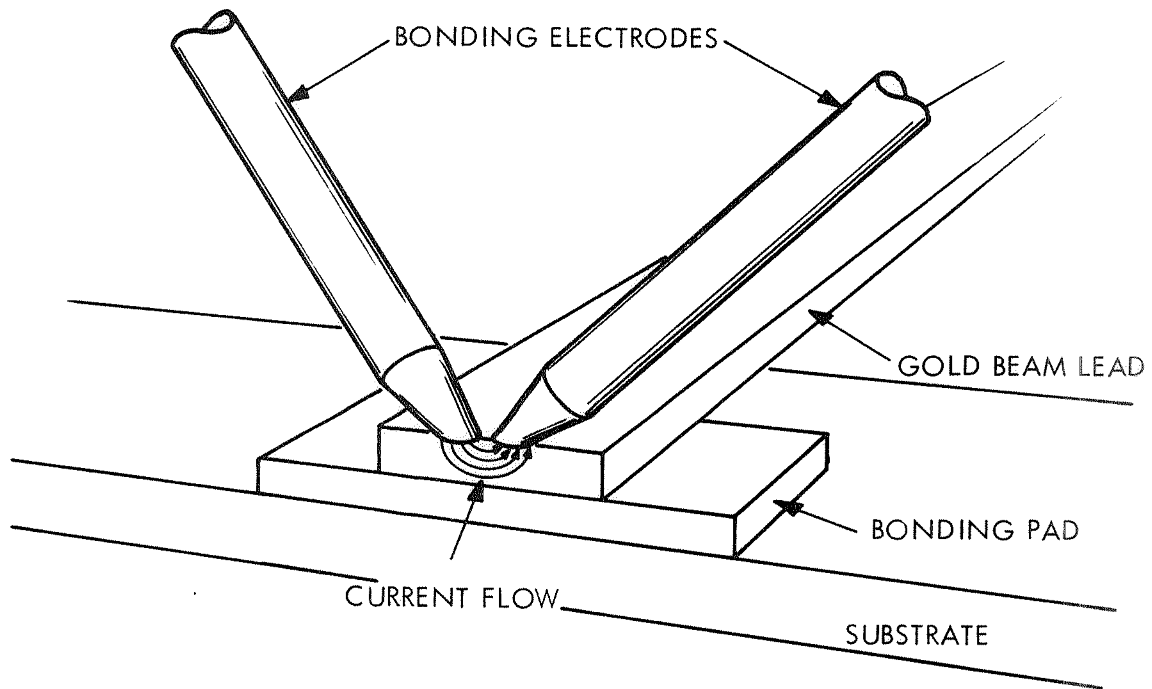


Figure 8. Parallel Gap Bonding on Beam Leads

Bond Testing

While the beam lead structure allows visual inspection of the bonded structure--an important advantage over other flip chip methods--optical inspection alone is not considered entirely adequate for the detection of unbonded or poorly bonded beams (refs. 84, 85). Experience in these Laboratories has shown that in the case where systematic, i.e., process or material related, bonding inhibition does not occur, poorly formed bonds are to be found in isolated cases at random locations. These failures occur at a rate of less than 0.1% in properly controlled bonding operation. While not significant with single chip devices, the cost and reliability of multichip systems, where 100-200 bonds can be present on a single substrate, can be seriously affected.

The types of testing presently employed in beam lead bond testing are those primarily designed to detect systematic flaws in the process or material systems. Samples are adequate for these tests, which are generally destructive and are usually designed to produce at least a quantitative figure of merit, if not recognizable mechanical data. These would include 90° peel (refs. 80, 85), push off (ref. 67) and air blast (ref. 86).

In the peel test the beams are bent up to 90° to the substrate surface, the silicon chip having been mechanically or chemically removed. An instrument, usually built in house, is used to grip the now free end of the bent beam and pull it in a direction normal to the bond surface. The force required to either break the beam or the bond is noted, and this value divided by the width of the bonded area provides a measure of the bond quality. The instrument used in these Laboratories is shown in Figure 9 while Figure 10 depicts the condition of the beam leads as the test is performed. However, the 90° peel test is not a good indicator of overall bond strength since it is not particularly sensitive to the size of the bonded area. This is an important shortcoming with beam leads since misalignment of bonding tools or chips on substrates affects the total bond area and consequently the effective strength of the joint. The peel test, then, must be combined with optical bond area measurements to assure an adequate appraisal of the bond strength in practical beam lead structures. The bond shear test, in which an axial tensile force is applied to the beam lead parallel to the bonding plane, is sensitive both to the quality of the bonding and the area of the joint. In this regard, therefore, it is superior to the peel test. The chief difficulty here lies in the problem of providing adequate jigging for such small structures. Tests such as these are valuable for monitoring production bonding processes on a sample basis, set up of bonding equ ipment and experimental evaluation involving bonding equipment, bonding processes and material properties. The fact that this technique can provide strength distributions resolved into standard stress directions is particularly salutary in laboratory work. With good bonding, 90° peel strengths of the order of 4-6 lbs/in of joint width should be realized on evaporated or plated gold metallized substrates. Shear strengths of a joint with an area of 9×10^{-6} in.^{2} should exceed the breaking strength of a beam of cross section 0.003×0.0005 inch. Other tests in common use, such as the air blast and push-off tests, apply non-specific combinations of peel and shear stresses to all bonds simultaneously. With the air blast test an element of fatigue is introduced. In this test,

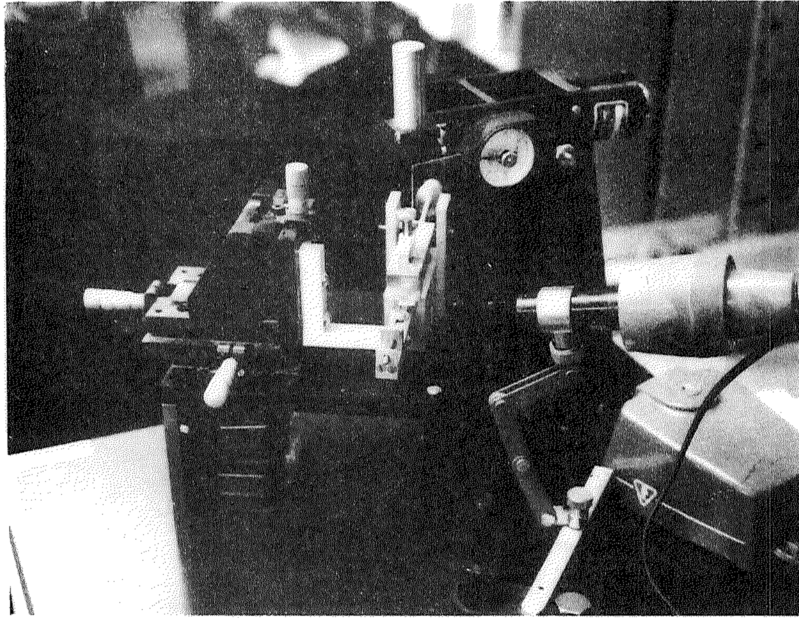


Figure 9. Peel Tester

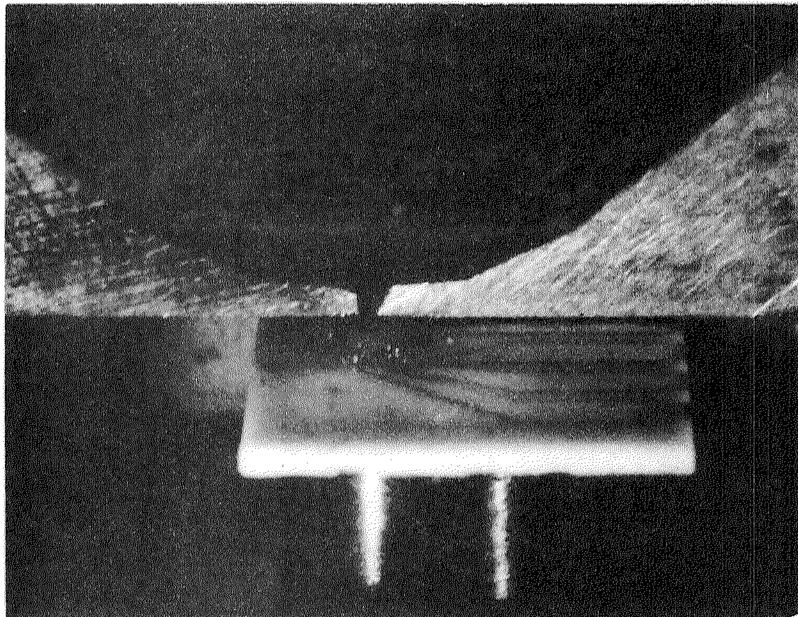


Figure 10. Substrate in Position for Bond Peel Test

jets of compressed air are directed at the bonded device through a system of nozzles. By vertical oscillation of the nozzle arrangement, the entire chip can be caused to alternately lift and fall. The number of cycles which a bonded chip will withstand before the beams fail is used as a measure of the integrity in the beam leads and bonds. The device has been used as a nondestructive screen (ref. 86) and appears to be particularly effective in detecting poorbonding or beam adhesion conditions. The test, when used with simultaneous optical or electrical tests, may also be effective in the detection of randomly poor bonds. There is no evidence in the literature, however, that this is practical; it is particularly questionable where the beams are short and thick, so that their stiffness effectively prevents the vertical motion of the chip which causes the beam stresses required.

As with the air blast test, the "push-off" test applies a stress to all beams on a chip simultaneously. Here the beamed chip is bonded to a special, metallized substrate arranged such that a hole is in position under the bonded chip. Stress is applied to the facedown surface of the chip by the action of a stylus passed through the hole. The force required to separate the chip from the surface of the substrate is measured and used as an indicator of bond quality. Obviously, the criteria for quality must reflect the chip geometry and the number of beams involved. Such a test is used on a sample basis in "Safeguard" as a bonding process control procedure. It is sensitive to the state of the bonding machinery, to the cleanliness of chips or substrate, and likely also to the hardness of the metal members in the bonds. Again, push-off tests are used to detect systematic variations in bond quality. Other tests are concerned more with assuring the mechanical integrity of the chips themselves or the necessary ductility in the beams.

Peel, tensile, buckle (resistance to axial load applied to outboard end of beam) and shear tests can be performed on the beams themselves and have been described in the literature (ref. 79). The prime purpose of such tests is to assure adequate adhesion of the gold beams to the dielectric surface of the chips. Some typical values for these tests would be:

(1) peel - 2-3 grams

(2) buckle - 7-9 grams (room temperature)

(3) shear - 32-38 grams

(4) tensile - 10-12 grams

The important beam ductility can be tested by a beam bending test described by Clark (ref. 68). Here, beams are forced to bend away from the chip surface by means of an anvil, the requirements being that the beams bend before separation from the chip occurs and that no cracks or breaks occur in the bend. Beams which are hard have a tendency to crack or break in the bend or lift entirely from the chip without bending.

Work done in these Laboratories (ref. 82) indicates that the microhardness may serve as an indicator of ductility. The advantage to this non-destructive method is that it provides information on the quality of the plated beams at a time when material rework is still possible. While the exact relation of the microhardness and its causes to bond quality is still under investigation, gold beams with a microhardness less than 70 VHN (5-10 gram load) appear to bond satisfactorily.

An annealing effect appears to be normal on beam lead material after plating. On occasion, however, a lot is recorded on which no softening takes place. This is thought to be connected with impurities in the gold plating bath, probably metallic. The normal behavior of plated beam material is shown in Figure 11.

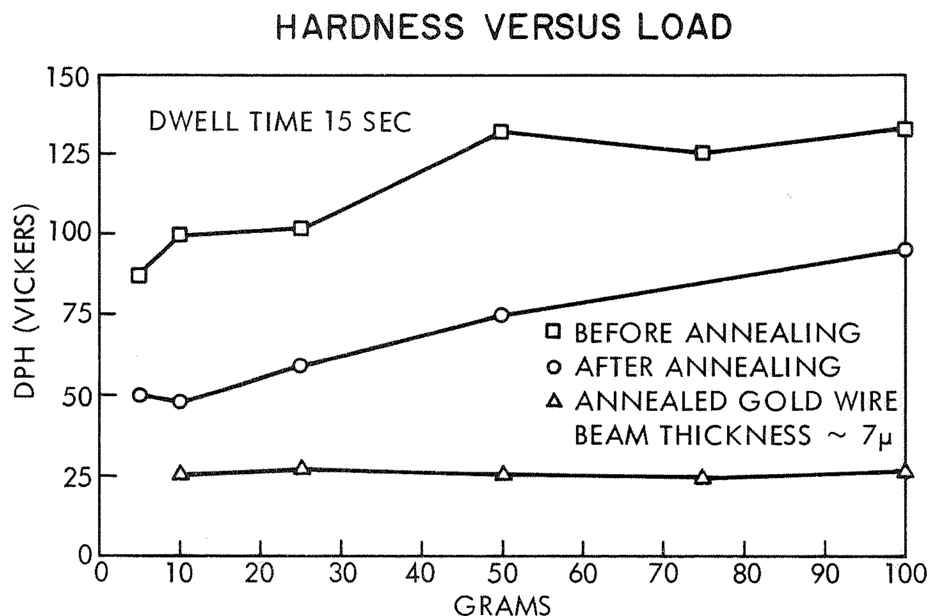


Figure 11. Effect of Annealing on Micro-Hardness of Plated Beam Leads

More recent work (ref. 85) indicates that a decrease in resistivity in the plated metal may accompany the annealing. This offers further possibilities for the timely non-destructive indication of ductility in beam lead fabrication.

While much work has been done in the testing of beam lead bonds, no completely satisfactory method of individually and non-destructively testing bonded beams has been perfected. In spite of the techniques reported in the literature, the most prevalent, if somewhat inelegant, technique used for judging bond quality in the laboratory is to probe each beam with a pointed stick, tweezer point or other suitably shaped stylus. Large-scale testing which can duplicate and quantify this suprisingly sensitive technique has not been developed.

The bonding qualities of the substrates have been treated in the literature (see metallization section). However, other properties of substrates and methods of testing them have not been extensively discussed. This is particularly true with respect to thick film materials. At present, those interested in high reliability devices seem to favor the more easily controlled topography, cleanliness and metal properties of substrates prepared using thin film (evaporation) techniques. It is likely that the random bonding inhibition mentioned earlier can be traced, at least in part to random deficiencies in the substrate materials.

RELIABILITY

The amount of reliability data that has been published or that is available for beam leaded devices is limited. Considerable data are being accumulated by manufacturers for the "Sentinel" program but these data are presently not available for publication.

Interpretation of the available data must be done with the thought that most of the testing was done with the intention of accelerating failure mechanisms which may be inherent in the beam lead process. In most cases the failure rates at accelerated stresses are used to quote a failure rate at another more normal stress level.

Semiconductors, in general, are very reliable and with controlled processes and selective testing, can be made more reliable. The beam leaded and the face bonded devices are shown to have maintained the high level of reliability of semiconductors. Minimizing a major failure mechanism of conventional devices, bonding defects, should result in a more reliable semiconductor product. It is estimated, based on the reduced number of bonds and probably due to improved quality of beam lead bonds, that the degree of improvement should be about an order of magnitude (ref. 99).

The failure rate reported by RADC (ref. 99) for bonds on conventional gold wire devices is 0.00012% per thousand hours and for aluminum wire devices is 0.00006% per thousand hours. RADC estimates that face bond and beam lead devices may improve the reliability by an order of magnitude. IBM (ref. 100) has established, during 10 billion module hours of operation in the 360 computer, a failure rate of 0.003% per thousand hours, and 68% of the failures were due to bonds (0.0002% per thousand hours for their solder bonding with metal balls). More recent data (ref. 101) indicate that the failure rate may be as low as 0.00004% per 1000 hours. Fairchild, employing aluminum bumps to nickel and gold plated moly-manganese, has not had a failure with over a million hours of operation and storage (0.09% per thousand hours). Philco-Ford, employing solder bumps, also has reported zero failures during 1.2 million hours of operation (0.08% per thousand hours). Hughes (ref. 102) has reported that they have achieved an order of magnitude improvement for bonding reliability (0.00001% per thousand hours) employing flip chips.

Beam lead devices are manufactured without any noticeable deterioration of electrical characteristics when compared with conventional semiconductor devices. The beam lead technology is an asset to the electrical characteristics of some devices which are very surface sensitive, such as pnp and MOS, since the beams provide a shielding effect which minimizes surface degradation. "The surface of the oxide becomes equipotential and the effects of charges on the outer surface are nullified, causing no detectable shift in V_F (forward voltage drop), I_R (reverse current), or B_V (breakdown voltage) during 1500 hours at V_R (reverse voltage) = 30V and ambient temperature of 55°C, states J.E. Thomas Jr. and A.Esbitt (ref. 103). The titanium used in most systems enhances surface conditions by providing an interstitial gettering source (ref.104).

High frequency capabilities of beam lead devices are equivalent to non-beam-lead devices. Parasitic capacitances in beam lead devices are typical to those of conventional devices. If the silicon is isolated by selective etching, which is feasible for beam lead devices, it further reduces the capacitance coupling resulting in an improvement for switching speeds.

Thermal resistance values for the beam lead devices are equivalent to those of similar conventional devices when the beam lead devices are back side mounted or when thermally conductive epoxy is applied properly. Thermal resistance of a beam lead device is a function of the width of the beams, source of heat and chip size (ref. 105).

Many choices for metallization of beam leads are available (ref. 106) but data are not available for all the systems. Four systems, for which reliability data on semiconductors was published and are available, are the all aluminum, aluminum gold (GOAL), PtSi-Ti-Mo-Au, and PtSi-Ti-Pt-Au.

Data for the all-aluminum beam lead industry are very limited, but the all-aluminum metallization has been used by the industry for many years and has proven very reliable. The all-aluminum systems main advantages are that there will be no dissimilar metal problems on the chip and fabrication costs will be lowest. The inherent stigma associated with the currently available conventional aluminum devices is still present, particularly aluminum migration and aluminum corrosion, but techniques have been developed and are in use to minimize these problems. The mean-time-to-failure for aluminum film conductors conducting 1×10^6 amperes per square centimeter at 175°C is about 1000 hours (sputtered aluminum) which is the shortest time for the four major metallizations. Thermal shock of aluminum beam leaded switching transistors from 100°C to -40°C was performed without noting any failures. Forty units were subjected to humidity life at 40°C and 90-95% relative humidity without failures to 8000 hours. An operating life test at 85°C and 1 MHz has been performed for 250 hours without failure (ref. 106).

A similar metallization system (GOAL) has been investigated. In this case, however, glass is deposited and then windows are opened remote from the silicon contact regions to the aluminum; Ti-Mo-Au is then used to form the beams and connected through the windows to the aluminum. The GOAL metallization is being used to evaluate

a multi-chip integrated circuit package (ref. 107). Forty-eight units were sequentially submitted to 1-1/4 hours at 450°C, temperature cycling (10 cycles 150°C to -65°C), thermal shock (5 cycles 100°C to 0°C), and moisture resistance without any failures occurring. Forty-eight units were sequentially submitted to 1-1/4 hours at 450°C, shock (1500 G, 1/2 millisecond, five blows in each plane), vibration fatigue (20 G, 32 hours each plane) vibration variable frequency (20G, 100-2000-100 Hz), and constant acceleration (20kG) without a failure. Zero failures occurred after 48,000 unit hours at 200°C. One failure occurred after 48,000 unit hours operating life at 20 MHz.

The PtSi-Ti-Mo-Au metallization systems main advantages are:

(1) The gettering effect of titanium which improves surface stability and the quality of the junctions.

(2) The stability of the metallization resistance to 450°C.

(3) The high mean-time-to-failure of the metallization.

(4) The ability to penetrate into the silicon for ohmic contact.

(5) The resistance to deterioration in adverse environments when Mo, which is susceptible to corrosion at high humidities, is protected.

The empirically determined mean-time-to-failure for Mo-Au metallization conducting 1×10^6 amperes per square centimeter is 42 times greater than that for sputtered aluminum or 42,000 hours at 175°C (ref. 106). Life and design studies have been performed on several thousand bipolar devices. Failure rates, on these unscreened devices, as determined by employing the NASA Microelectronics Device Data Handbook, were classified between "very good and excellent."

The failure rate was 0.02% per thousand hours (MTBF = 5×10^6 hours) at a 60% confidence level which it is estimated, would result in a best failure rate in the range of 0.002-0.0002% per thousand hours (MTBF = 10^8) if the semiconductors had been prescreened. This metallurgical system was compared with the Bell Laboratory metallurgical system as part of an RADC contract (ref. 85) and no significant differences were discovered for mechanical or environmental failure rates although some failure modes were different. The following bond failure rates were determined for tests performed per MIL-STD-883:

(1) Vibration, method 2005A - 0.018%

(2) Mechanical shock, method 2002B - 0.036% (5 pulses, Y_1 plane)

(3) Temperature cycling, method 1010B - 0.006% (5 cycles)

(4) Thermal shock, method 1010F - 0.013% (1 cycle)

Bond peel strengths were similar at about 3.1 g.

The PtSi-Ti-Pt-Au metallization system of Bell Laboratories is the most commonly used by beam lead manufacturers. Its main advantages are the gettering effect of titanium which will improve surface stability and the quality of the junctions, the ability to penetrate into the silicon for ohmic contact, the resistance to deterioration in adverse environments, and it was the first system used to manufacture beam lead devices. Life and design studies have been performed by Bell Telephone Laboratories and reported by D. S. Peck (ref. 108) and M. Eleftherion, F. Schneider and W. Wanesky (ref. 84) and their applications in systems were reported by J. Acosta (ref. 109). The observed failure rate in operation has been found to be less than 0.0015% per thousand hours of which only two failures were reported and neither was positively traced to metallization problems.

It has been reported that beam leaded devices were centrifuged to 200,000 G without any failures (ref. 92). Other accelerated stresses further confirm the reliability of beam leaded devices (ref. 108), e.g.,

(1) 10,000 hours at 250°C - No surface degradation

(2) Storage at 300°C with reverse bias - MTBF = 10,000 hours

(3) 95°C, 90-95% RH - MTBF = 10,000 hours

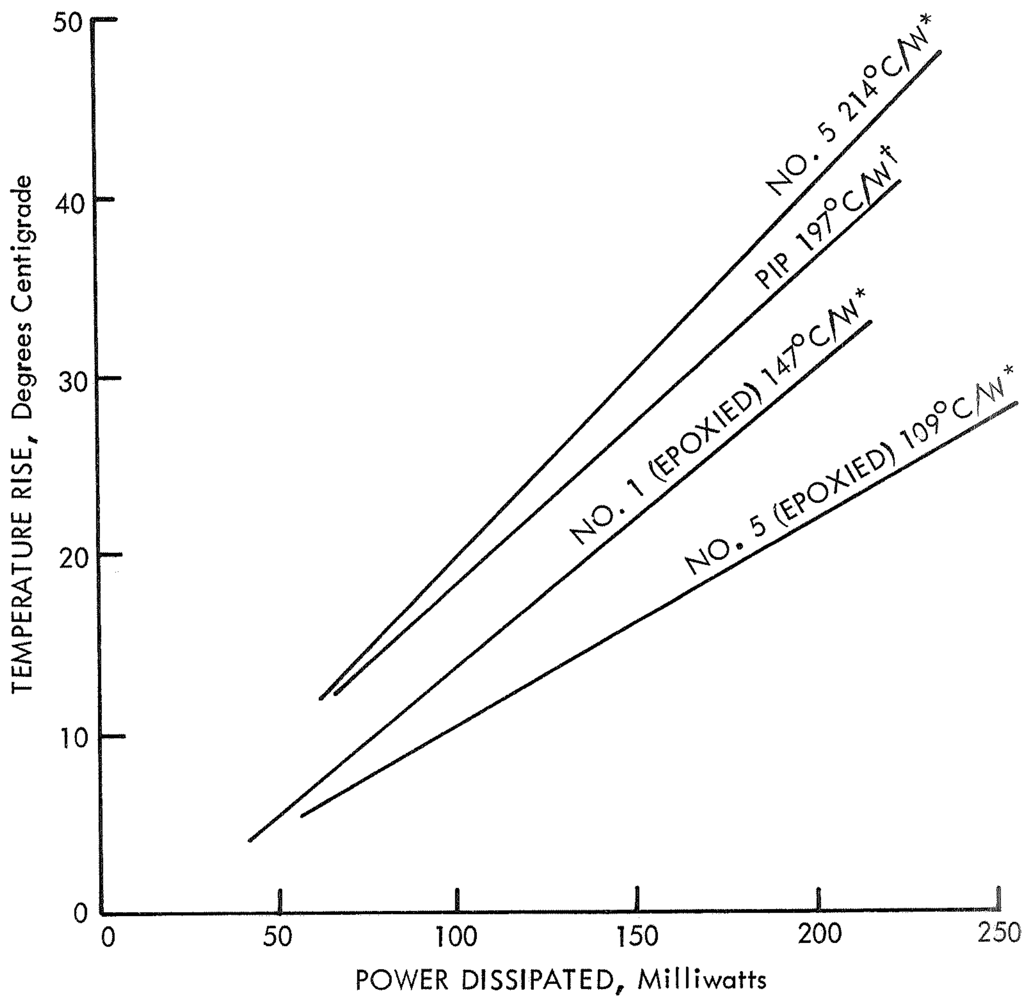
(4) Storage at 300°C - MTBF = 10,000 to 100,000 hours

MECHANICAL DESIGN CONSIDERATIONS

Thermal Resistance

Some criticism has been aimed at the beam lead concept with respect to its capability to dissipate heat. Without some precautions the heat dissipation is not only likely to be inadequate, but may be so limited that the device will not function correctly. In a normally bonded beam lead chip practically all the heat is removed by conduction along the beams to the substrate. This can result in a thermal resistance much higher than that of a conventionally mounted chip. However, there are several fabrication techniques which may result in chips with thermal resistances as much as 30% lower than the conventional unit.

Several papers (refs. 25, 105, 110) have examined the thermal resistance of a beam lead chip with respect to various geometrical specifications and in particular with the use of epoxy or similar conducting coatings. GTE Laboratories has been able to obtain in some cases greater reductions in thermal resistance (Figure 12) than those quoted in these papers by selection of the epoxy, minimizing the separation between the chip



*Beam lead units on a ceramic substrate
†Conventional unit in a PIP package

Figure 12. Thermal Characteristic, SG140, Clocked Quad Gate

and the substrate and filling the remaining gap with a homogeneous layer of epoxy. The latter is best accomplished by placing the coated device into a vacuum chamber. The thermal resistance can be further reduced by backside mounting the chip, as is done in conventional assembly, and then bonding the beam down to the substrate (ref. 88). This has been done at our Laboratories using 0.002 inch thick chips and 0.006 inch long beams without any significant problems. It should be noted, however, that unless steps are taken to remove the refractory metals from the back surface of the beam, the bond will no longer be gold-to-gold. This is covered in the standardization recommendations, although no specification for a longer beam for face-up bonding is noted. Whether or not this is a necessity has yet to be established.

An additional rather novel idea for removing heat from the beam lead chip has been suggested by Naylor (ref. 98). This involves the use of a heat spreader. A technique such as this is of course relatively expensive, but it does indicate ways in which the high thermal resistance of a basic beam lead chip can be reduced.

Proper design considerations of the basic chip can reduce thermal resistance as shown by Naylor (ref. 98). The thickness of the chip, the number of beams, and the placement and area of the major heat generating components are important. Naylor has shown that over a given range the thermal resistance can be reduced by a factor of three by increasing the radius of the heat source by a factor of three. He also shows that thinning the chip below 0.005 inch begins to increase the thermal resistance significantly. This, however, depends on how heat is being removed from the back surface. If some form of heat sink exists on the back of the chip the reverse relation may result.

Hardwick (ref. 105) has shown that the number and dimensions of the beams can significantly affect thermal resistance. Below eight leads the change is important, beyond that the change becomes quite small. However, even these data have to be qualified by the size of the chip and the position and size of the heat source. The width and thickness of the beams over the range considered practical for other reasons does not significantly affect thermal resistance, except where the latter is very high (over 200°C/watt).

No actual values of thermal resistance have been quoted here except as shown in Figure 12. It is clear from the above discussion that a vast number of conditions can affect the thermal resistance, in addition to device type and the method of packaging. To specify a value would be meaningless without complete documentation of the specific case under consideration.

Dimensional Standardization and Recommendations

It is desirable for several reasons to attempt to standardize as far as possible the dimensional structure of the beam lead chip. The three major reasons are:

(1) To have a regular chip size, beam width and spacing and beam length in order that the number and form of metallization

patterns on the substrate can be minimized and also that direct replacement of units from different sources is possible.

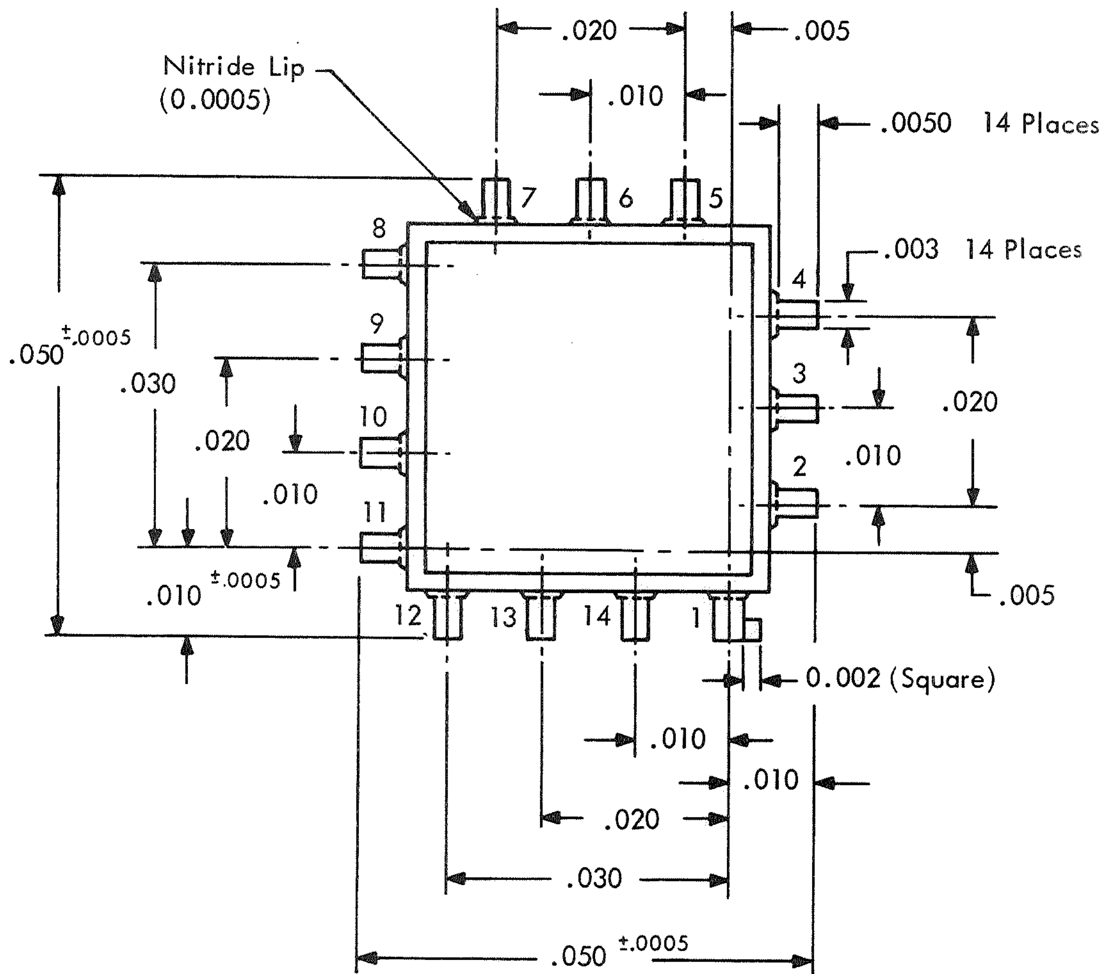
(2) To define geometrical specifications such that a degree of chip quality can be guaranteed and that, chip to chip, a given set of handling and assembly procedures will be compatible. Examples of these items are beam thickness and beam anchor area to the chip.

(3) To detail both mechanical and geometrical conditions in order to optimize both thermal and electrical resistances. Included in this area might be standards aimed at making the beams equally bondable, since differences in the type of metal used and even the hardness of the same metals may necessitate the use of different bonding techniques from chip to chip.

Chip outline. -- Several attempts have been made already in the industry to standardize the outline of beam lead chips. Obviously, it is impossible to have one configuration for all devices, and therefore all the attempts have revolved around a formula or pattern to take into account the size of chips and the number of beams. The EIA approach initially involved the use of a formula to determine outline standards; GTE Laboratories, as part of their effort on a Multichip Contract for WPAFB, developed a set of standards that went further toward defining a recommended outline (ref. 107). More recently Texas Instruments established a series of outlines for beam lead chips based on the number of beams. In our view, with minor modification, this is the best set of standards to date. An example of a typical outline is shown in Figure 13, the beam dimensions and spacings are the same on all chip sizes. It is recommended that the chips be within 0.005 of being square, that beams extend outward on all four sides and that the number of beams on each side differ by no more than one. The basic specifications on chip outline are contained in Table 10.

Other geometry factors. -- Other factors which are presented in items (2) and (3) above, and which are included in Table 10 and Figure 14, cover details of the configuration of the beam area over the chip and the passivation film overlap. The latter is used to prevent electrical shorting to the silicon substrate as a result of misalignment or over-etching in the processing operations. The specifications covering the anchor area of the beam on the chip are aimed at obtaining a sufficient strength of attachment of the beam to the chip. It is assumed that the interface bonds between the various metal layers used, between the initial metal layer and the passivation layer and between the passivation layer and the silicon are satisfactory. These latter conditions are determined by in-process quality control tests.

Other standards activity. -- Other standards activity is currently being considered by S.A.E. Committee G-8, on Electronic Interconnection Techniques and Packaging. This group, composed of members from various semiconductor manufacturers, is in the initial stages of preparing working and inspection standards for the bonding of beam leaded devices. Their work has only started, but it is of interest to be aware of such activity.



ALL DIMENSIONS IN INCHES TOLERANCE 0.0001 INCHES EXCEPT WHERE NOTED (NOT CUMULATIVE)

Wafer Thickness 0.002   0.005 ±0.0005

Beam Thickness 0.0005 ±0.0002

Chip – Silicon with Oxide-Nitride Surface Layers

Beams – Gold

Figure 13. Suggested Geometrical Outline for a 14 Lead Beam-Lead Chip

TABLE 10

A LIST OF SPECIFIC RECOMMENDATIONS IS OUTLINED BELOW:

	RECOMMENDATION	REASON
1.	All chips should have a corner beam having a distinctive shape indicating the No. 1 or A lead, or on the side on which this lead is situated if it is not a corner beam.	Ensures the correct alignment of chip when face down and easy identification of specific leads.
2.	Center to center spacing of adjacent beams on the same chip should be 10 mils or a multiple of 10 mils.	Minimum separation presently easily achievable with interdigitation and adequate beam spacing on both the chip and substrate (including thick film).
3.	Exposed beam length from edge of excess passivation film 5 mils ± 0.5 mil.	Adequate length for bonding while minimizing the use of silicon "real estate."
4.	Projection of excess passivation beyond the silicon edge should be 0.5 to 1.0 mil.	Protects against beam shorting to silicon as it passes over the chip edge.
5.	Width of beam should be ideally 3 mils, although beams as narrow as 2 mils and as wide as 4 mils have been used successfully.	Adequate width for bonding and heat removal while allowing recommended beam spacing.
6.	Beam on one side of chip should be exactly opposite a space on the opposite side of the chip.	Allows for interdigitation of beams on adjacent chips.
7.	Design thickness of beam should be 0.5 mil ± 0.2 mil.	Adequate minimum for bonding and removal of heat, while allowing some flexibility.
8.	Beam anchor width on chip should be a minimum of 5 mils commencing at the excess passivation edge and continuing back on the chip. *	This item*, as well as the next two, have been found to greatly increase the reliability of the bond between the beam and the chip. Any significant reduction in the dimensions below that recommended can result in a degradation of the beam peel or pull strength even if the interface bond strength is normal. Increasing the dimensions does not significantly increase the peel or pull strength because the failure then appears elsewhere.
9.	Beam anchor depth from the edge of the silicon should be a minimum of 2.5 mils.	
10.	Beam anchor area should be at least 10^{-5} in.^{2}, in the event that one of the above conditions cannot quite be met.	

*The larger anchor areas reduce the detrimental effects of undercutting of the adhesive metal layers and enables a larger peel strength to be obtained.

TABLE 10 (Continued)

	Requirement	Reason
11.	Exposed beam area to be metallurgically identical on top and bottom faces of the beams.	This facilitates bonding either face-up or face-down. The former being used to decrease thermal and/or electrical resistance.
12.	Chip thickness should be either 2 mils or 5 mils (not 2 to 5 mils).	A large difference in chip thickness presents problems in automating handling and requires a different process mask. However, manufacturing methods may require either a thick or thin chip.
13.	Minimum distance of a beam from a corner of the chip should be 1.0 mil.	To avoid the weakening of a beam by its "falling off" at a corner as a result of misalignment or over-etching of the silicon.
14.	If the beam configuration results in an odd number of beams on one side of the chip and an even number on the opposite side, the middle beam on the odd numbered side should lie on the center line of the chip. If there are an equal number of beams on opposite sides of the chip, the beams nearest to the center line on each side of the chip should be equally spaced from the center line (i.e., one quarter of the beam spacing).	This is required to standardize the beam locations with respect to the silicon edge and also allows the relatively simple design of a master substrate layout that can receive many chip sizes. Specifically, it locates the "X" axis beams with the "Y" axis beams.
15.	Chips should have a type code which can be read while the chip is face down.	Since the beam lead chip is generally face down, this greatly simplifies identification. With a ⟨100⟩ crystal orientation etching a code into the backside of the chip during the separation etch is very straightforward.

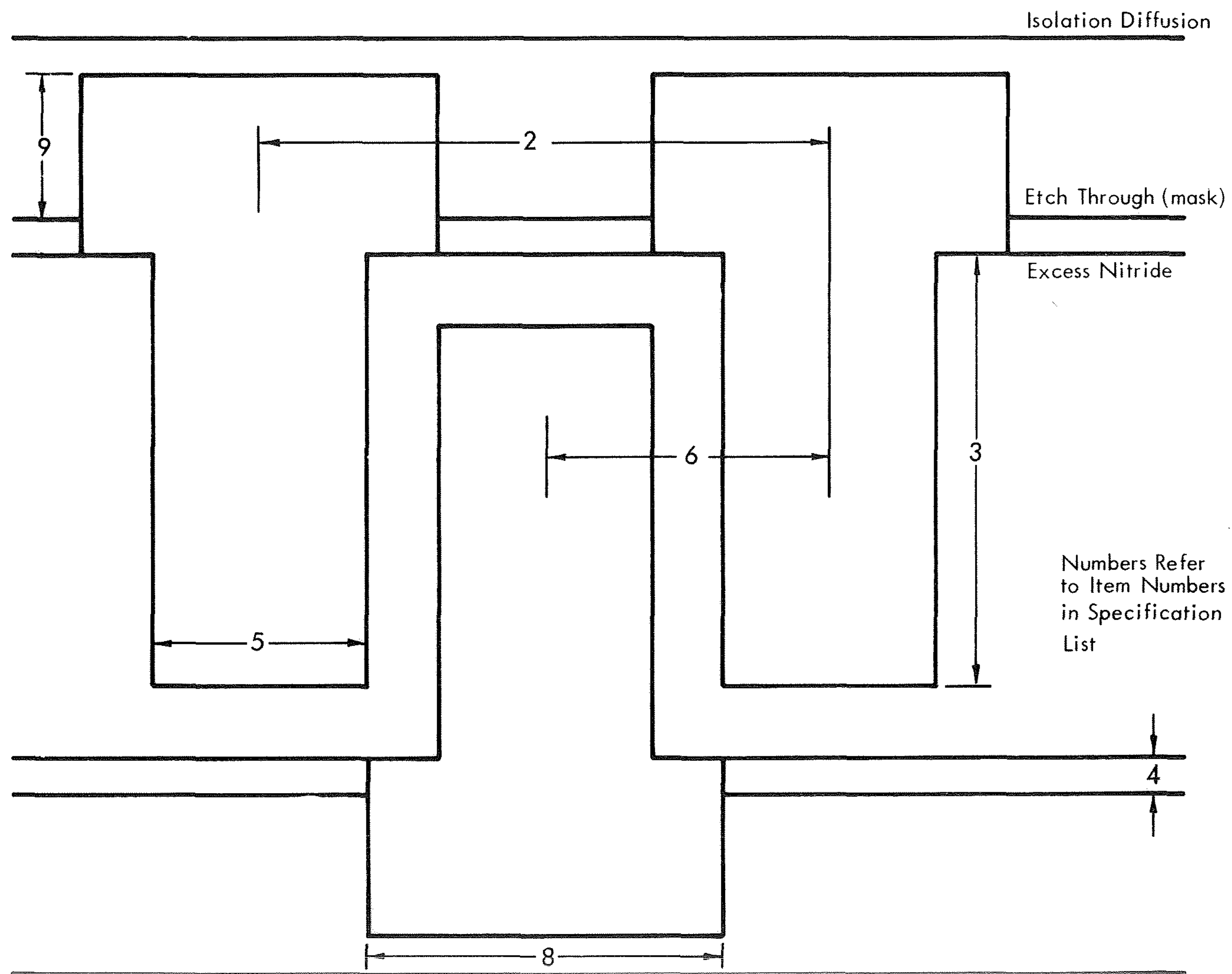


Figure 14. Proposed Geometrical Layout for Beam Lead Devices Showing Anchor Design and Interdigitation Tolerances

SUMMARY AND CONCLUSIONS

Introduction

The recommendations here presented will point out those areas in which advancements have been made to insure a reproducible technology and an improvement in integrated circuit reliability. In some cases several processes or materials have been studied extensively and little difference can be seen to establish more than an arbitrary choice. This section is also presented to establish those areas where the state of the art can be advanced by further development efforts.

Passivation

In the important reliability area of junction surface passivation the following is recommended:

(1) Use of silicon nitride over conventional silicon dioxide diffusion masked integrated circuit structures.

(2) Use of silicon nitride over clean oxide is recommended in beam lead MOS circuits.

(3) Best quality silicon nitride obtained by synthesis of silane and ammonia or silicon tetrachloride and ammonia at temperatures of 750-900°C.

Metallurgy

The ultimate reliability of the beam lead system is dependent on the materials and processes used in depositing the metallurgy for the contact and interconnects required. The major recommendations are presented in the following subsections.

Ohmic contacts. --

(1) Platinum with the formation of an intermetallic silicide (Pt_2Si_5) is a low resistance contact to silicon. It is a direct replacement for the aluminum ohmic contact and does not suffer from spike alloying and electron migration at high current densities as does aluminum.

(2) Aluminum contacts can be used where the addition of beam leads to standard IC chips is desired. In these cases the deposition of a glass layer over the aluminum is necessary.

<u>Bonding and barrier metallurgy</u>. -- The important criteria for the interface metals is to obtain good adherence to silicon nitride or silicon dioxide, and to act as a conductive layer-diffusion barrier for the plated beam material. Except in the case of aluminum beam leads, the above criteria are best satisfied by the use of two metals: (1) A reactive one for beam adherence, and (2) a barrier metal to act also as a conductive metal for plating. The recommendations on these materials are as follows:

(1) Titanium is a reactive metal which has good adhesion to dielectrics such as silicon nitride, silicon dioxide or alumina. It has been used extensively for beam adherence and shows no major reliability problems. As is the case for any reactive metal, corrosion and lateral etching difficulties can occur. This has been minimized by use of a thin layer of titanium (<1000 Å).

(2) Of the studied materials that can be used as the beam lead barrier metal, platinum and palladium have the properties of corrosion resistance, low diffusivity to gold, and high conductivity with ease of plating.

(3) Molybdenum has proved to be an effective barrier material and is recommended for those applications where it can be protected from moist ambients by hermetic packaging.

<u>Beam metal.</u> -- A gold-based system would be the recommended metallurgy used for the beam metal. Since the beam metal is relatively thick, it is in most instances electroplated. Aluminum is the only single metal conductor that combines low contact resistance, adhesion to silicon or dielectrics, and good conduction properties. A gold-base metallization system has increased reliability specifically in corrosion resistance, high current carrying capability, reliability, and ease of bonding. It is for these reasons the gold plated beam interconnect system is recommended for high reliability over aluminum.

Substrates

(1) Of the wide variety of materials that can be used for chip mounting substrates, the high alumina ceramics have the best combination of properties for high reliability bonding of chips. Ceramic substrates have temperature stability over a wide temperature range, and can easily be processed with conductor patterns by use of screen and fired decal mounting or by evaporation and photoresist techniques. The ceramic materials also have thermal conductance advantages over glasses or organic substrates.

(2) Conductor materials for substrate fabrication should have properties similar to the beams themselves. Since the beams are gold-based

materials, the substrate metallization in most cases will also be gold based. The conductor, gold, will have an adhesive metal such as titanium deposited initially, and for increased reliability, especially when exposed to wet ambients and high temperatures for long periods, a barrier metal such as palladium should also be used.

Processes

(1) All metals can be deposited by sputtering or electron beam evaporation. We have found sputtering to be a preferred technique since more reproducible adhesion of metal is obtained. In the case of palladium it can be conventionally evaporated, minimizing interface state problems in low threshold MOS devices.

(2) Metal definition is accomplished by either sputter etching or chemical etching. Sputter etching produces better definition, while chemical etching is somewhat less complex with little set up of capital equipment.

(3) Gold-beam plating is best processed using a pure (24 K) bath, and it is our recommendation that it is an acid bath. Procedures to minimize organic and heavy metal build up, which reduce ductility of beams and cause bonding and handling failures, are essential.

Bonding

Since bonding is made between a gold plated beam and a gold conductive pad on its mating substrate, any number of techniques would appear to assure high yield and reliable bonding. The most widely used technique is thermo-compression bonding at temperatures of 250-350°C using a wobble tool or a force tool with a compliant media. Consequently, either of these thermo-compression techniques is recommended based on the considerations outlined below.

(1) Of the techniques used in bonding, thermo-compression wobble tool bonding has had the widest acceptance and development effort. It has proven to be a reliable technique of bonding. This technique has some shortcomings in that deformation of beams cannot be tightly controlled and in some cases this causes excessive bugging. This deformation puts restraints on the spacing of leads in chip layout of complex circuits such as MOS LSI.

(2) Compliant bonding has advantages over wobble bonding in that it reduces lateral deformation of the beams and intimately contacts beam to substrate conductors even when there are differences in

height. This technique suffers from the more complex set up and alignment of compliant film (usually aluminum) along with the usual chips and tool alignment to the substrate. Any microbridge system where crossovers are formed close to bonding pads could not be used with compliant bonding due to the large area needed for the compliant material.

Major Future Development Areas

(1) Development work should be pursued to improve handling assembly and packaging of devices. In order for beam lead chips to be more reliably mounted, the techniques of (1) chip transfer, (2) bonding, and (3) package fabrication have to be refined and made more automated and thus more reliable. Although a great deal of work has been accomplished in beam lead technology as regards device fabrication, extensive use of beam leads in the future will depend directly on handling, bonding and packaging in a reliable automated process.

(2) Although most of the beam lead studies pursued to date use titanium as the adhesive metal, further work should be pursued to compare titanium reliability with other metals (such as hafnium, chromium, etc.) to insure an optimized beam lead metallurgical reliability.

(3) Although accelerated life studies indicate an improved reliability of beam lead devices over conventional devices, the available data is not sufficient to be conclusive. Further studies should be carried out to establish the ultimate reliability of these systems. These systems (e.g., Ti-Pt-Au, Ti-Pd-Au, Ti-Mo-Au) are potentially susceptible to interdiffusion problems not present in a single metal interconnect system.

(4) Continued studies should be carried out to improve both bipolar and MOS device radiation resistance. This is particularly true for beam lead devices since the metallurgical differences from conventional aluminum metal circuits may further complicate the attempts to improve reliability when exposed to a variety of radiation levels and types.

(5) Palladium shows promise as a substitute for platinum as both a contact and barrier metal. It is particularly attractive for IGFET's since it can be evaporated using a conventionally heated coil or boat. It is recommended that further development be carried on to establish failure modes in operating life by substituting palladium for platinum in beam lead circuits.

(6) Further development efforts be continued in the use of aluminum oxide over silicon dioxide. This system is particularly suited to low threshold voltage IGFETs and is also an effective barrier to diffusion of impurities such as sodium, potasium and copper.

(7) Study further and improve the chemical interface properties of silicon nitride, silicon dioxide to minimize metal deposition shadowing and metal removal shorting at the silicon nitride silicon oxide steps.

(8) The compliant bonding technique is one in which further development in tool design with simplification of alignment will advance the state of the art -- especially when more complex chips are used. It also minimizes the constraints on the substrate topography. Further studies using ultrasonic wobble tool bonding will advance the state of the art in aluminum lead bonding and also give insight concerning its effect on conventional gold-based beam lead bonding. Gold beam thermo-compression bonding is highly reliable but does suffer from low ($<1\%$) bond failure due to gold hardness or contamination of surfaces. Ultrasonic bonding has not been studied sufficiently to establish whether it can improve the bonding reliability over thermo-compression techniques.

(9) In the matter of bond testing, no completely satisfactory non-destructive test method exists for establishing the strength of beam lead bonds. Such a test when, and if, combined with the idea of prestressing beam lead joints would be a welcome asset in improving bond reliability and reducing inspection costs in high reliability work.

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