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A DIGITALLY CONTROLLED VERY HIGH FREQUENCY SYNTHESIZER

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16. Abstract

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SUMMARY

A digitally controlled frequency synthesizer, which can replace the multicrystal local oscillator in a general aviation navigation receiver, is described. The development of this synthesizer resulted from an effort to find less expensive and more reliable methods for generating local oscillator frequencies than is currently available by using the multicrystal technique. The synthesizer employs a phase-locked loop in which the output of a VCO (voltage-controlled oscillator) is digitally divided and phase locked to a stable reference frequency. A new technique is used to accomplish the dividing. Because it is digital, the synthesizer lends itself readily to computer control. A breadboard model of the synthesizer is described.

INTRODUCTION

Frequency synthesizers are used to generate a large number of discrete frequencies from which one may be selected for use. Such a device finds wide use as a laboratory signal source and in the frequency selection function of communications equipment. This paper describes a digitally controlled frequency synthesizer, which is to be used as the local oscillator in a general aviation communications and navigation (COM/NAV) receiver. The general aviation COM/NAV receiver in this instance refers to that class of equipment used by the private pilot who normally flies a single-engine aircraft. Interest in this area of avionics arises out of a growing need to reduce the cost of avionic equipment, and thereby promote widespread use of navigation aids and other services available through radio communications.

The frequencies of interest include the VOR (very high frequency omnirange) navigation band ranging from 108 MHz to 118 MHz and the aircraft communications band from 118 MHz to 136 MHz. The channel spacing is 100 kHz and 50 kHz, respectively, with the possibility of this spacing being reduced to 50 kHz and 25 kHz in the future. Current methods for generating the necessary local oscillator frequencies have generally consisted of using as many as 30 to 40 crystals in a "crystal saver" technique. (See ref. 1.)

There are two basic approaches possible in a single-crystal synthesizer. One approach combines the harmonics of a reference oscillator by mixing and filtering

(refs. 2 and 3), and the other is the phase-locked loop technique (refs. 3 and 4). Synthesizers of the former type generally require extensive filtering to minimize the spurious sidebands on the output. The phase-locked loop technique was chosen for development because of its potential advantages which include: a spectrally pure output which requires no filtering; implementation with digital integrated circuits; ease of programing due to the use of digital circuits; and the possible use of microelectronic mass production techniques to reduce cost. In this approach, the frequency of a VCO (voltage-controlled oscillator) is divided digitally and phase locked to a reference oscillator. Varying the divider in integer steps causes the VCO to change in steps of the reference frequency, and thereby causes the receiver in which it is incorporated to change channels.

SYMBOLS

C_1, C_2	capacitance of capacitors C_1 and C_2, respectively
D_1, D_2, D_3	voltage-variable capacitors
F_1, F_2	flip-flops
F_o	selected channel frequency and output of voltage-controlled oscillator
F_R	reference frequency
F(s)	filter transfer function
G(s)	equation for forward loop gain
H(s)	equation for feedback loop gain
j	complex variable
K_p	gain of phase detector, volts/radian
K_v	gain of voltage-controlled oscillator, (radians/sec)/volt
N	integer which divides frequency F_o
Q_1, Q_2	outputs of flip-flop F_1 and F_2, respectively

R	reset input of flip-flop F_1
R_1, R_2	resistances
S	set input of flip-flop F_1
s	Laplace transform
T	trigger input of flip-flop F_2
T_1	transistor
V	supply voltage
V_{error}	phase-locked loop error voltage
W,X,Y,Z	integers
$\phi_E(s)$	phase angle of error signal
$\phi_R(s)$	phase angle of reference signal
$\phi_o(s)$	phase angle of voltage-controlled oscillator signal
ω	frequency, radians/sec
ω_o	low-pass filter cutoff frequency, radians/sec

SYNTHESIZER OPERATION AND DESCRIPTION

The frequency synthesizer described herein was developed for use as the local oscillator in the navigation part of a receiver. The VOR navigation band extends from 108 MHz to 118 MHz, and the receiver has a 10 MHz I.F. (intermediate frequency). Therefore, the synthesizer is designed to range from 98 MHz to 108 MHz with 50-kHz channel spacing. This range means the receiver will have a 200-channel capability, although only 100 channels are currently required. The 50-kHz channel spacing will permit the receiver to accommodate future expansion of the VOR facilities.

THEORY OF OPERATION

A simplified block diagram of the frequency synthesizer is shown in figure 1. The output signal from the VCO with frequency F_o (the desired channel frequency) is fed

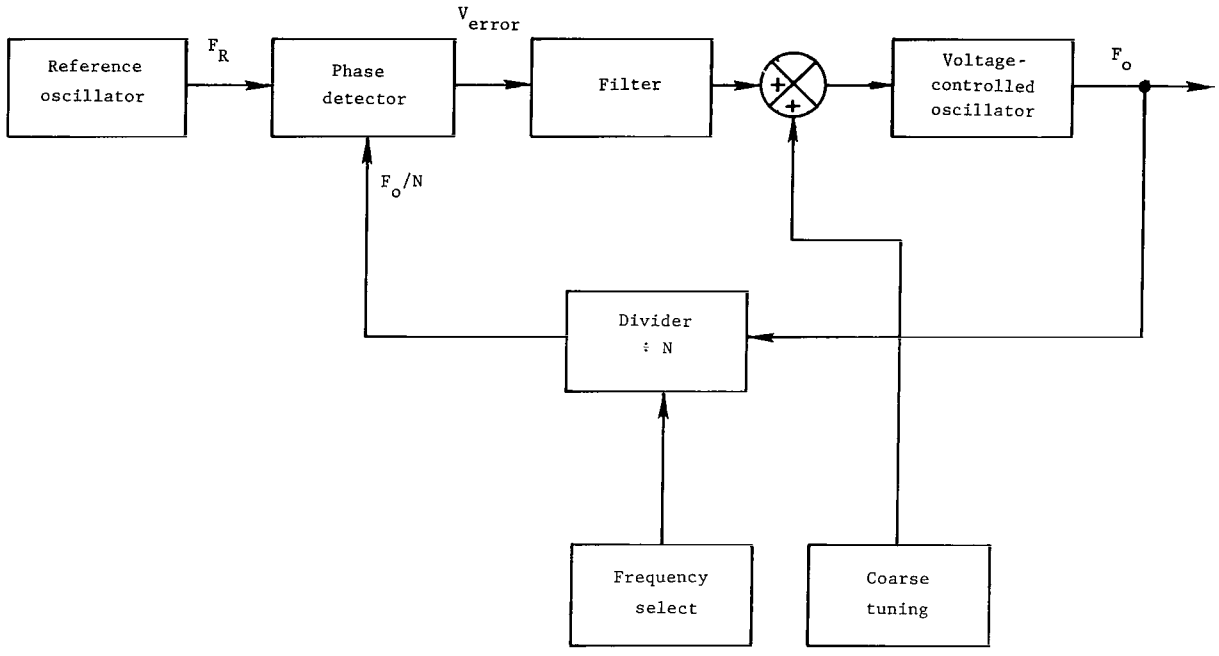

Figure 1.- Block diagram of digital synthesizer.

into a variable-digital divider which divides F_o by an integer N. The integer N is determined by the selected F_o and has a value such that when the desired F_o is attained, $F_o/N = F_R$, where F_R is the reference frequency. The phase detector compares the divider output with the reference frequency to determine whether this relationship exists. If F_R and F_o/N are not equal, an error signal is generated. Since phase is the quantity being compared, a frequency difference produces a phase error signal which varies at a rate equal to the frequency error. This signal causes the VCO to sweep until its output reaches a frequency such that $F_o/N = F_R$. The loop then acquires phase lock. A steady-state phase error sufficient to maintain $F_o/N = F_R$ exists in the loop. If F_o/N attempts to change frequency, the phase detector senses a phase change and its output varies in a direction to maintain lock. While in the phase-locked condition, the VCO output frequency is always a multiple of the reference frequency. A unit change in N causes the output frequency to change by an amount F_R.

The filter on the output of the phase detector removes the ripple which is present at the reference frequency. The filter restricts the capture or pull-in capability of the loop. The pull-in range is the maximum frequency error which can exist and still

permit the loop to achieve lock. This maximum frequency error is generally less than the hold-in range, which is the maximum range over which the loop will remain in lock once lock is achieved. The pull-in range is determined primarily by the pass band of the filter. If the frequency error falls very far outside this pass band, the sweep voltage from the phase detector is attenuated and is insufficient to drive the VCO to lock. Therefore, a coarse-tuning network is provided for tuning the VCO to within the pull-in range of the loop.

VARIABLE-DIGITAL DIVIDER TECHNIQUE

The significant feature in the implementation of this phase-locked loop synthesizer is the technique employed in the variable divider. The variable divider is designed to accept directly the VCO signal with frequency F_O, which ranges from 98 MHz to 108 MHz. It divides these frequencies by a number N such that the divider output at phase lock is the reference frequency, 50 kHz, that is, $F_O/N = 50$ kHz. Therefore, $N = F_O/50$ kHz and ranges from 1960 to 2160 in integer steps for the given range of F_O. For example, if $F_O = 98.55$ MHz, $N = \frac{98.55 \times 10^6}{50 \times 10^3} = 1971$.

Operating at the high input frequencies represented by F_O, a conventional divider, which counts up to the selected number of pulses N and then is reset to 0, would not be able to achieve the reset operation in the 9 to 10 nanoseconds available between input pulses unless subnanosecond logic is used. In order to circumvent this requirement, a unique design for the variable divider was conceived in which the first stage is permitted to free run while the first-stage reset operation is accomplished with additional control circuitry operating at slower speeds. Subsequent stages are designed with reset as in a conventional divider since these stages operate at a fraction of the divider input frequency and thus do not have to be reset in a few nanoseconds.

The variable divider must be capable of counting at least 2160 pulses. For reasons which will become clear later, the divider was designed with four stages; the first is a divide-by-twenty, the next two are divide-by-tens, and the last is a divide-by-two. A block diagram of the divider is shown in figure 2. With this design, the count in the fourth stage has a weight of 2000 (that is, the count in this stage is incremented by one each time a total of 2000 pulses are received), the count in the third stage has a weight of 200, the second stage a weight of 20, and the first stage a weight of 1. The desired number of pulses to be counted is controlled as indicated in the diagram by the numbers selected for W, X, Y, and Z on an input device such as BCD (binary coded decimal) thumbwheel switches. The maximum range of each number is shown in figure 2. In general, the total number of pulses counted is $N = 2000W + 200X + 20Y + Z$. The divider

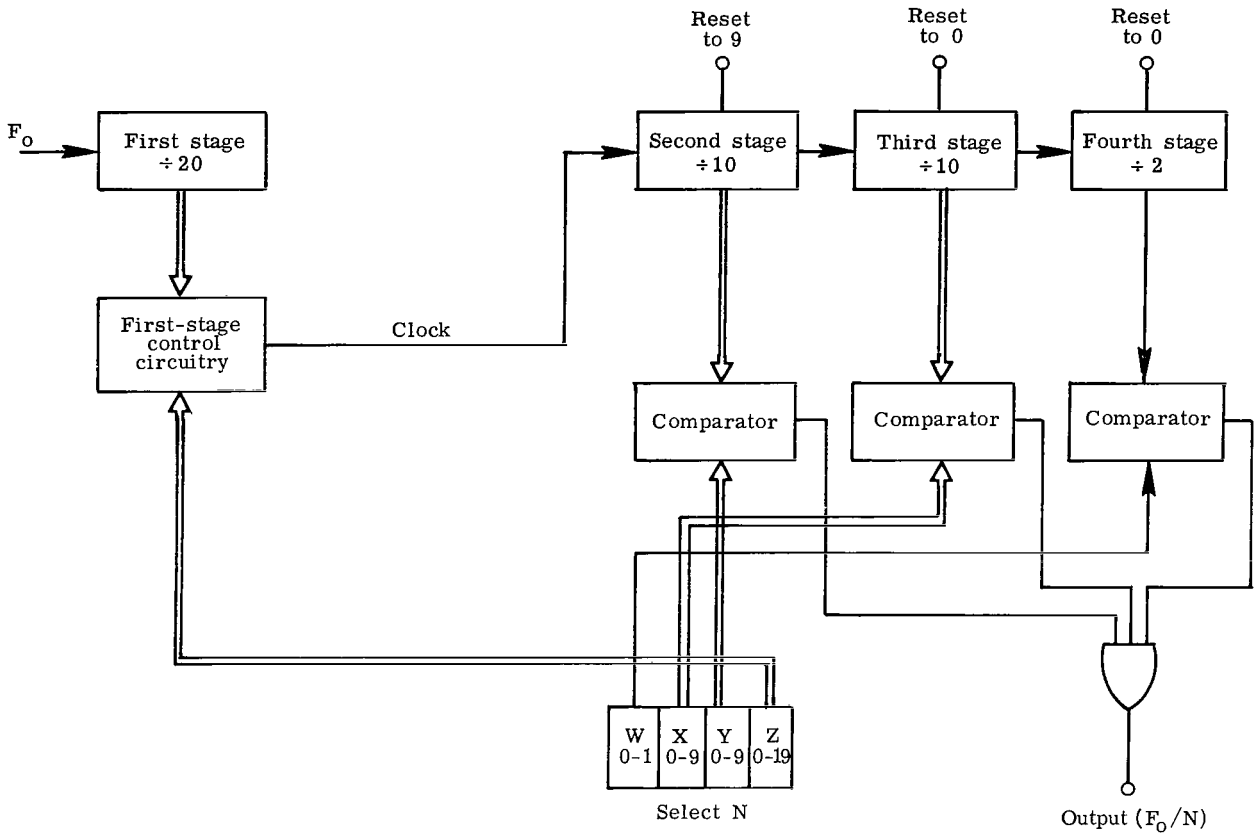

Figure 2.- Block diagram of variable divider.

output is generated as soon as the last three stages reach a count which coincides with the numbers selected for W, X, and Y.

The inclusion of Z pulses in the total count is accomplished with the aid of the first-stage control circuitry. The expression for N can be rewritten as $N = 2000W + 200X + 20(Y + 1) - (20 - Z)$. In this form, the two basic operations which take place are indicated. First, near the beginning of each count cycle, the clock pulse to the second stage is controlled to occur once for every 19 input pulses until $20 - Z$ of these clock pulses have reached that stage. The rest of the time the clock pulses occur once for every 20 input pulses. The result is that $20 - Z$ fewer pulses are input than should be to satisfy the count in the last three stages. Second, the second stage is forced to count $Y + 1$ pulses, and thereby causes 20 extra pulses to be input. Thus the count is reduced by $20 - Z$ in one operation and increased by 20 in the other operation with the result that a net increase of Z pulses occurs.

The implementation of this procedure required to count Z pulses consists of the following. The reduction of $20 - Z$ in the number of pulses counted is achieved through the first-stage control circuitry. A block diagram of the latter is shown in figure 3.

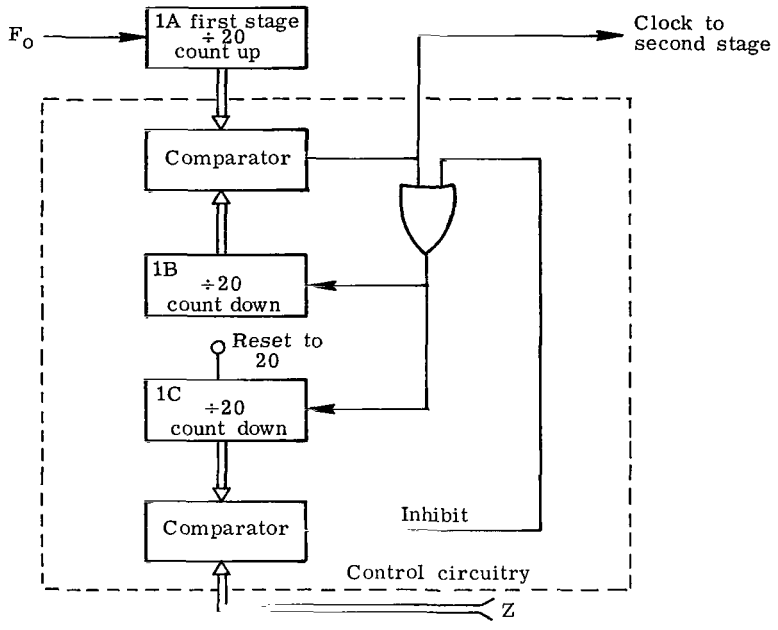

Figure 3.- First-stage control circuitry logic.

The VCO signal drives 1A, the first stage, which continually cycles from 0 to 19. The count in 1A is compared through a set of gates with the count in 1B, another divide-by-twenty counter which is designed to count down. Whenever the counts in 1A and 1B are identical, the comparator generates a clock pulse to the second stage. Initially, 20 input pulses are counted and the second stage receives a pulse. 1B receives the same clock pulse and shifts down one count. Only 19 input pulses are then required before 1A and 1B agree again. Each time 1B is decremented the next pulse to stage 2 will arrive after only 19 input pulses. Divider 1C, which is also designed to count down from 20, keeps track of the number of times this condition occurs. When 1C counts down to Z, the number selected for the first stage (that is, when 20 - Z clock pulses have reached the second stage), then an inhibit signal is generated to prevent 1B from being clocked. After the next clock pulse to the second stage, 20 input pulses are required before 1A and 1B agree. As long as 1B remains at the same count, the clock pulse to stage 2 continues to occur after 20 input pulses. The inhibit signal remains until the last three stages reach their selected count and an output is produced. At this time, the inhibit is removed and 1C is reset to 20. At the same time, stage 2 is reset to 9 rather than to 0, and thereby requires the second stage to count one more clock pulse and thus increases the selected Y by one. The last two stages are reset to 0, and a new count cycle begins.

The particular configuration of the divider was selected because it resulted in a one-to-one correspondence between the desired VCO output frequency and the required

value of N. For example, if the desired output frequency F_O is 105.75 MHz then $N = \frac{F_O}{F_R} = \frac{105.75 \times 10^6}{50 \times 10^3} = 2115$. N can be written equivalently as 2000(1) + 200(0) + 20(5) + 15. The correct value of N results when W = 1, X = 0, Y = 5, and Z = 15 (15/20 = 0.75). Thus the proper value of N is automatically selected if the whole number of MHz of F_O is set into the W, X, and Y inputs shown in figure 2 and if the desired fraction of a MHz is selected and then encoded into the proper number ranging from 0 to 19 for the Z input.

Because of the high input frequency from the VCO, the divider was constructed with nonsaturating emitter-coupled logic. This logic has propagation delays and rise times from 2 to 5 nanoseconds, depending on the logic function. Therefore, much care was exercised in the layout and wiring of the boards.

VOLTAGE-CONTROLLED OSCILLATOR

The voltage-controlled oscillator (VCO) shown in figure 4 is a grounded-base configuration with feedback provided through a voltage-variable capacitor D_3 from

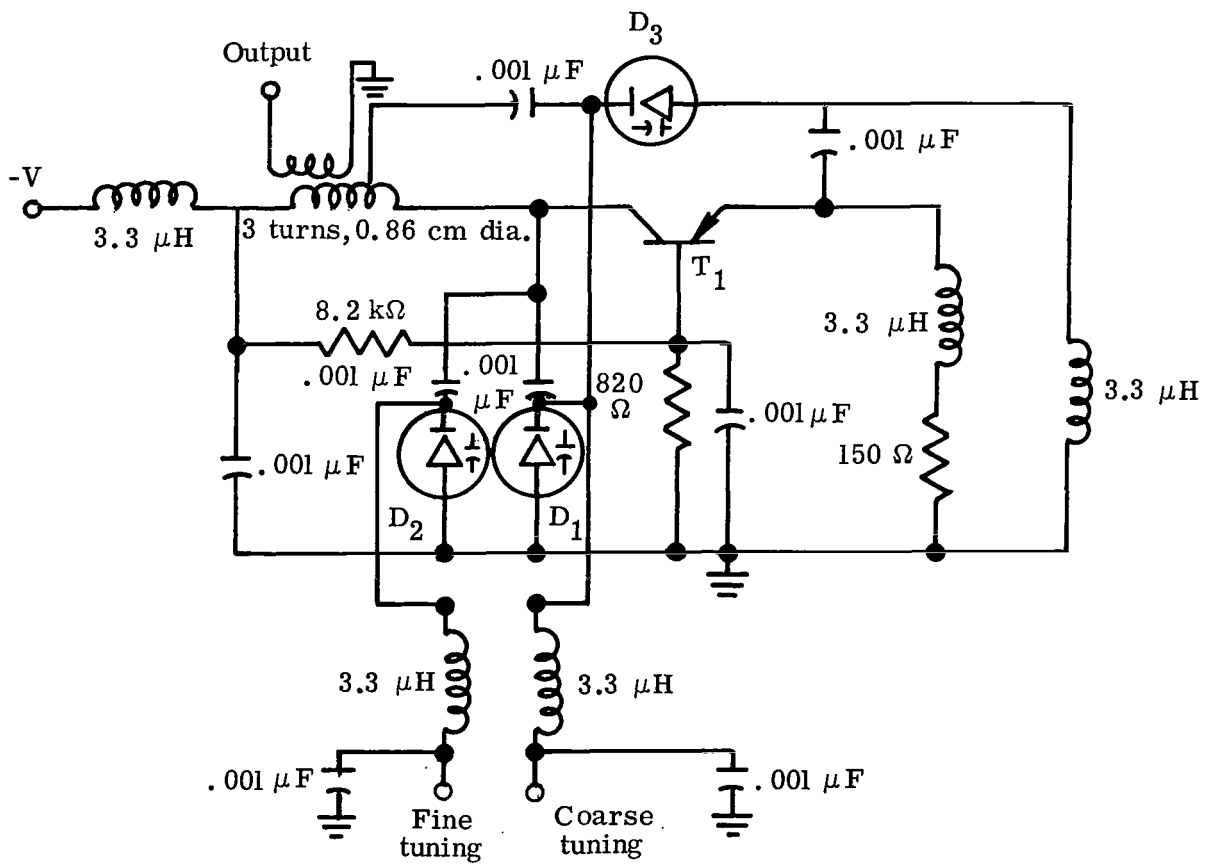

Figure 4.- Voltage-controlled oscillator.

collector to emitter. D_3 is variable in order to prevent overdriving T_1 as the frequency is varied. Two voltage-variable capacitors (D_1 and D_2) connected in parallel determine the capacitance of the parallel-tuned tank circuit. The capacitance, and hence frequency of the oscillator is varied by either of two control voltages. Capacitor D_1 is tuned by a coarse-tuning voltage which will bring the VCO to within approximately 1 MHz of the desired frequency. The other capacitor D_2 is controlled by the fine tuning voltage from the phase detector which locks the VCO to a multiple of the reference signal. The output from the VCO which ranges from 98 MHz to 108 MHz feeds a buffer amplifier between the VCO and mixer in the receiver. The VCO provides approximately a 1-volt peak-to-peak signal to the variable divider and has a short-term stability of 2 ppm.

DIGITAL PHASE DETECTOR

Phase comparison between the reference signal and divider output takes place in a set-reset flip-flop shown in figure 5. The signal from the divider F_o/N is fed to the

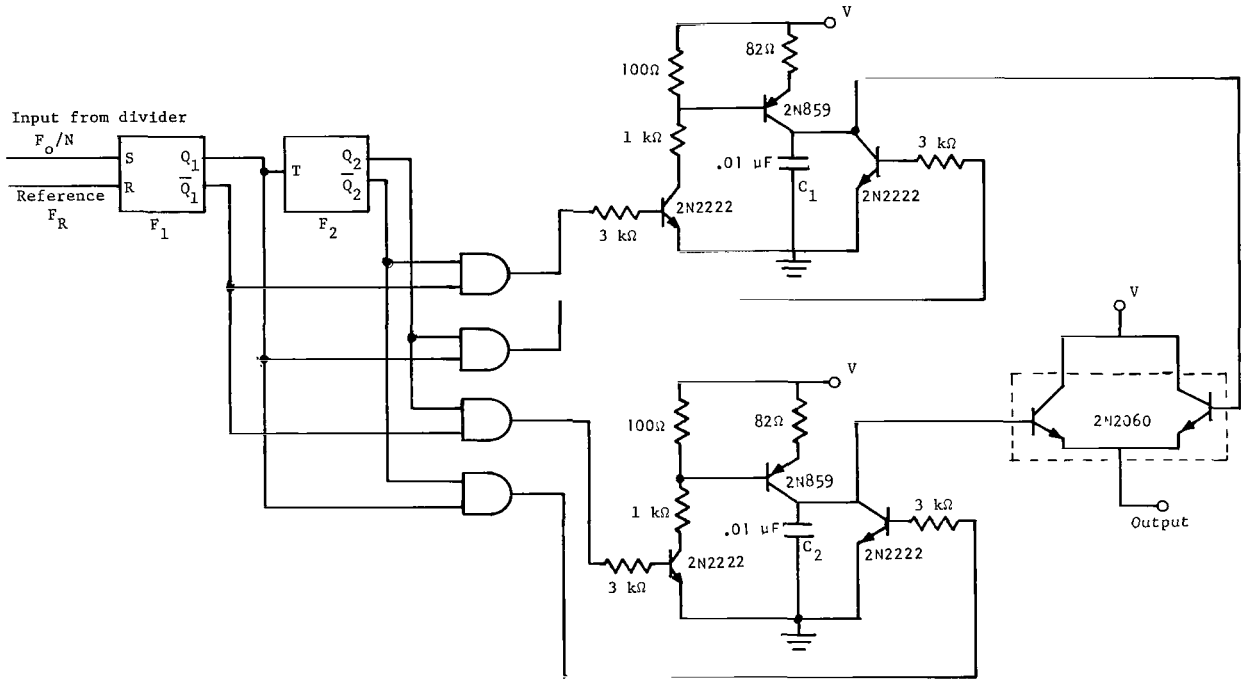

Figure 5.- Phase detector.

set input, and the reference signal F_R triggers the reset input. The output of the flip-flop is a pulse whose width is proportional to the phase difference between its two inputs. The average value of this pulse will yield a dc voltage proportional to phase difference and thus will provide a control voltage to drive the VCO. A simple first-order low-pass

filter on the output of the flip-flop would yield the dc voltage; however, a very narrow bandwidth filter is required to reduce the 50-kHz ripple on the control voltage to a few microvolts. Excessive ripple on the control voltage frequency modulates the VCO and produces 50-kHz sidebands on the VCO output. These sidebands need to be attenuated at least 60 dB below the desired output.

A sample and hold type of circuit is used to reduce the amount of ripple on the phase detector output and thus the amount of filtering needed. The details are shown in figure 5. In this circuit, two capacitors alternately charge and hold a voltage which is proportional to the pulse width of the output of the set-reset flip-flop. The output from the two capacitors is combined through two diodes connected back to back to obtain a dc control voltage. Four pulses in sequence are needed to effect the charging and discharging of the two capacitors. In order to obtain four pulses, the PDM (pulse duration modulation) output of the set-reset flip-flop is used to toggle a second flip-flop and the four states of the two flip-flops are then decoded with AND gates. The outputs of the gates are used to turn on transistors which alternately charge and discharge capacitors C_1 and C_2, depending on the state of the flip-flops. The operational sequence may be better understood by observing the timing diagram in figure 6. This diagram

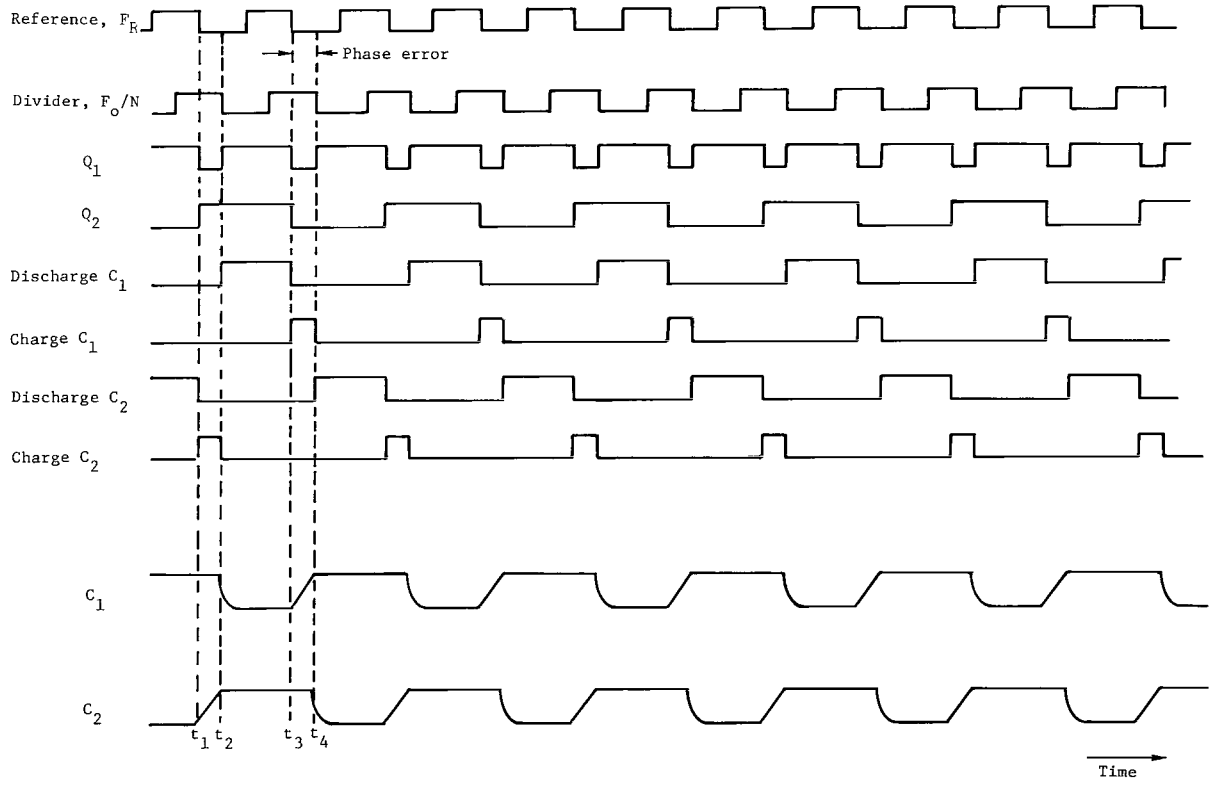

Figure 6.- Phase detector timing diagram.

shows the pulses appearing on the flip-flops and the gates for a given phase error between the divider and reference signals. It also shows the sequence in which C_1 and C_2 are charged and discharged. Times t_1 to t_4 constitute one complete charge-discharge cycle. The capacitors charge for a period of time directly proportional to the phase error. Because of capacitor leakage, there is still a 50-kHz ripple on the output of the phase detector. Also, any mismatch between the two circuits which are used to charge and discharge the capacitors contributes a 25-kHz component to the ripple voltage. Thus, a filter is needed to attenuate these two signals further.

FILTER

With no filter on the output of the phase detector, the VCO output exhibits sidebands at 25 kHz and 50 kHz which are only 20 dB and 15 dB down, respectively. To reduce these sidebands to 60 dB or more, an active notch filter at each of those frequencies was first attempted, but the selection of component values proved to be too critical for practical use. A low-pass, second-order Butterworth filter was considered. With a cutoff frequency of 2.5 kHz, this arrangement would give approximately 40-dB attenuation at 25 kHz and 52-dB attenuation at 50 kHz. An analysis was undertaken to determine whether the feedback system would be unstable with this second-order filter. The transfer function for the phase-locked loop was determined and from it an expression for the open-loop gain function and open-loop phase shift was obtained. This expression is discussed in more detail in the appendix. A computer program was written to calculate the open-loop gain and phase response with frequency. A plot of each is shown in figure 7. Bode's criterion for feedback systems states that a system should be stable if the open-loop gain falls below unity gain before the open-loop phase shift reaches -180°. Observe in figure 7 that the gain is 6.1 dB below the 0-dB crossover when the phase shift reaches -180°. This gain margin should be sufficient to guarantee a stable system. These calculations were performed for the worst case value of N, 1960, which is the smallest value and yields the largest gain.

The second-order filter was implemented by using an active filter configuration since this type of filter requires only resistors, capacitors, and an operational amplifier. The filter is shown in figure 8. The amplifier connected to the output of the filter is used for inverting the signal and for isolation. With this filter, the sidebands at 50 kHz were found to be only 55 dB down. Therefore, a resistance capacitance (RC) network with a cutoff frequency of 25 kHz was added to the output of the second amplifier. This network provided 6 dB more attenuation at 50 kHz and reduced all sidebands on the VCO output to greater than 60 dB. With a cutoff frequency of 25 kHz, the additional stage of filtering does not contribute a sufficient amount of additional phase shift to alter the gain margin significantly.

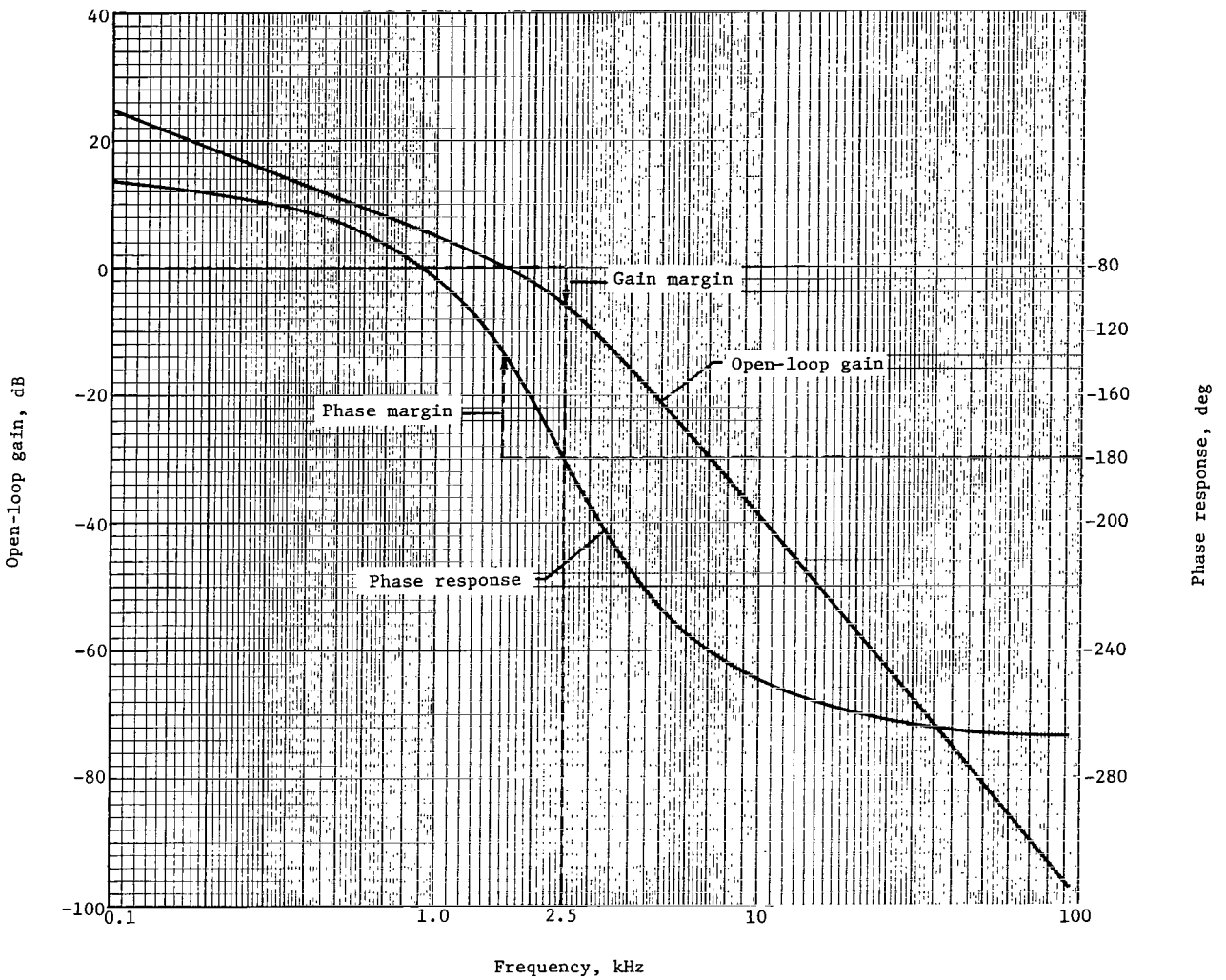

Figure 7.- Gain and phase response.

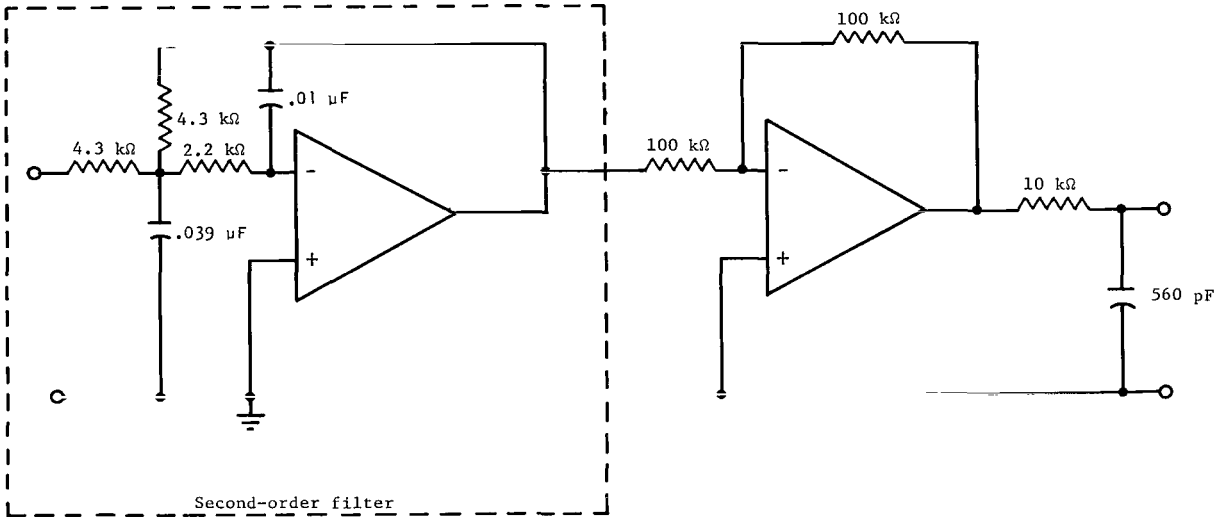

Figure 8.- Filter.

COARSE-TUNING NETWORK

Before the filter was added, the loop pulled into lock over about a 20-MHz range (measured with respect to the VCO frequency). This pull-in range was maintained even with step changes in phase error. The hold-in and pull-in range were the same. With the addition of the filtering, the pull-in range was reduced to approximately 2.4 MHz. This value corresponds to a frequency error between the reference signal and divider output of about 1.2 kHz. This figure is reasonable to expect since the filter starts rolling off at 1.0 kHz, and it is the primary factor limiting the pull-in range.

The coarse-tuning network compensates for the reduced pull-in range by providing a voltage which will tune the VCO to within ±1 MHz of the desired frequency. The phase detector then provides the fine tuning voltage and is capable of providing sufficient voltage variation to enable the loop to obtain lock over a 2-MHz range. The coarse-tuning network is activated by the frequency selection controls. It consists of a weighted resistor configuration and provides step increases in the control voltage to the VCO as the selected frequency is increased.

REFERENCE OSCILLATOR

The long-term stability of the frequency synthesizer depends on the stability of the reference oscillator. The crystal oscillator, shown in figure 9, supplies a stability of

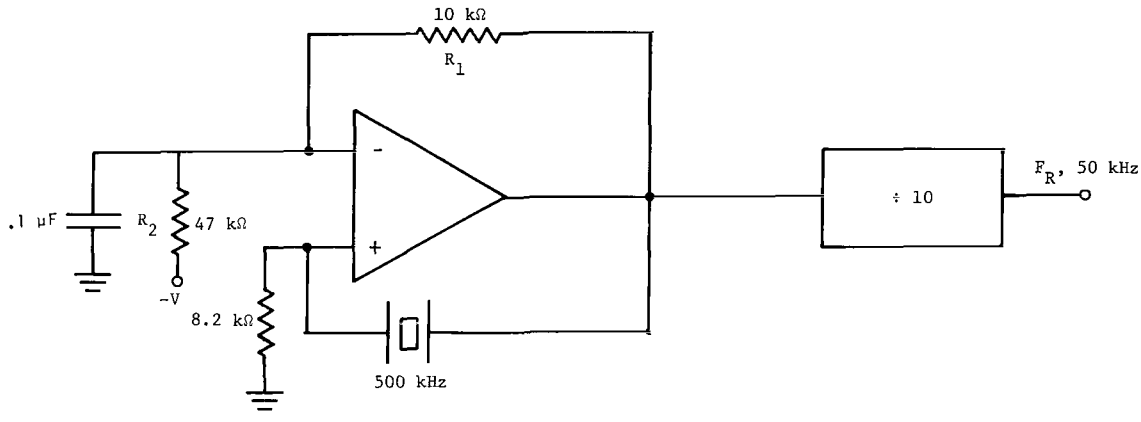

Figure 9.- Crystal reference oscillator.

0.005 percent. A high-speed differential voltage comparator is used with a 500-kHz crystal which is connected from the output to the noninverting input. This comparator provides positive feedback, and hence, oscillation. R_1 and R_2 are chosen to bias the dc operating point of the amplifier in the linear region of the output dynamic range of the comparator. The output of the comparator is compatible with transistor-transistor logic and is used to drive a decade divider directly. The divider reduces the reference oscillator frequency to the desired 50 kHz.

SYNTHESIZER PERFORMANCE

The digitally controlled frequency synthesizer operates from 98 MHz to 108 MHz in 50-kHz increments. Figure 10 shows a photograph of the output signal of the synthesizer. The spurious sidebands are greater than 60 dB below the output signal. The spectrum of the output is shown in the photograph of figure 11. The hold-in range for the phase-locked loop is about 4.7 MHz and the pull-in range is about 2.4 MHz. Frequency stability is 0.005 percent. Frequency selection is accomplished with thumbwheel switches. Channel switching time is on the order of 15 to 40 milliseconds. The speed with which the channels may be selected is limited by the thumbwheel switches and varies with the digit selected. If switching is accomplished electronically, such as by computer command, the worst case channel switching time (10-MHz change) is 15 milliseconds. The total power consumption is 10 watts. The performance of the synthesizer at room temperature is satisfactory. The performance over the full temperature range is currently being investigated.

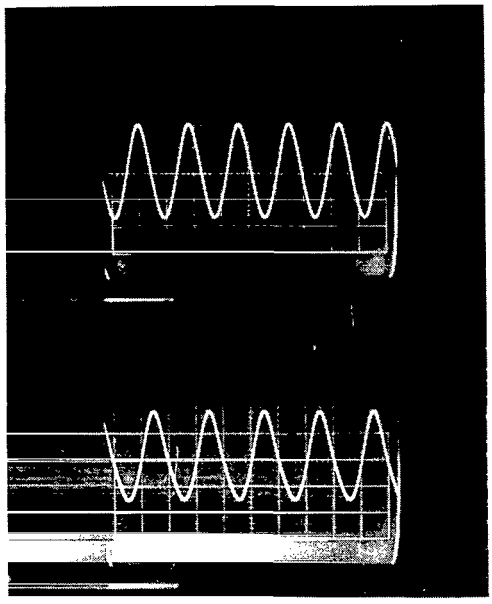

Figure 10.- Voltage-controlled oscillator output. Top, 108 MHz; bottom, 98 MHz; vertical scale, 0.5 V/div.; horizontal scale, 5 ns/div.

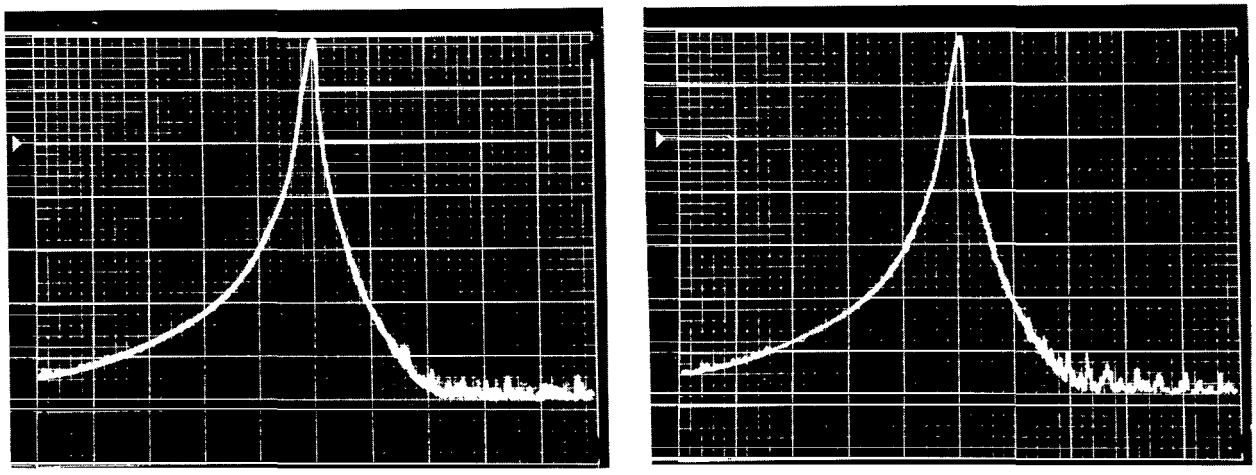

Figure 11.- Voltage-controlled oscillator output spectrum. Left-hand side, 98 MHz; right-hand side, 108 MHz; vertical scale, 10 dB/large div.; horizontal scale, 30 kHz/large div.

MODIFICATIONS FOR EXPANSION OF THE SYNTHESIZER

As noted, this frequency synthesizer was designed specifically for the navigation band, and it includes channel spacing of 50 kHz to handle future VOR system expansion. A similar design applies for the local oscillator in the communications section of the receiver. The primary modification required is to change the VCO frequency range to cover 108 MHz to 126 MHz. If 25-kHz channel spacing is desired in order to handle the future expansion of the communications band, a few additional modifications of the design as presented are required. The reference frequency must be reduced by a factor of two, and this reduction can be accomplished with the addition of a flip-flop. Likewise, the divider will require an additional flip-flop. For ease in relating the desired frequency to the required value of N, the flip-flop should be added to the first stage, making the latter a divide-by-forty, rather than a divide-by-twenty. Reducing channel spacing to 25 kHz will also produce stronger sidebands at 25 kHz and add some at 12.5 kHz; as a result, a reduction in the low-pass filter bandwidth is required. With the consequent reduction in loop bandwidth, the pull-in range will be decreased and heavier dependence will be placed on the coarse-tuning network. The latter may possibly be improved sufficiently by providing step changes in voltage for smaller increments in frequency.

CONCLUDING REMARKS

A digitally controlled frequency synthesizer for the very high frequency (VHF) navigation band was constructed by using the phase-locked loop technique. The same design can be readily modified for the communications band and for narrower channel spacing. A unique technique for performing the divider reset operation without actually resetting the first stage was developed to overcome the high-speed logic requirements of a conventional divider. This technique can be applied in even higher frequency synthesizers where the divider speed requirements exceed the state-of-the-art logic. The digital synthesizer, because of the techniques employed, can take advantage of the mass production techniques of medium-scale and large-scale integration which are a potential source of cost reduction and increased reliability.

Langley Research Center,
National Aeronautics and Space Administration,
Langley Station, Hampton, Va., June 25, 1971.

APPENDIX

STABILITY ANALYSIS WITH A SECOND-ORDER FILTER

The phase-locked loop may be analyzed as a simple feedback system with phase as the variable of interest. Figure 12 shows a mathematical model of the feedback system.

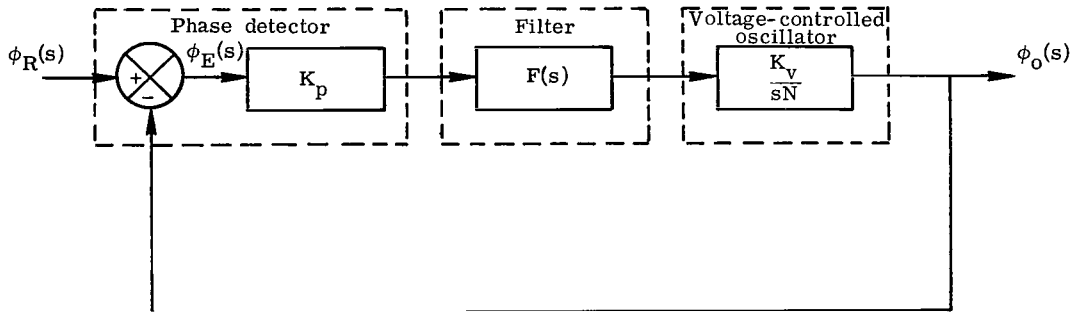

Figure 12.- Mathematical model.

The input is $\phi_R(s)$, the phase angle of the reference signal, and the output is $\phi_o(s)$, the phase angle of the VCO signal. The phase detector can be approximated by a summer with a gain of K_p volts/radian. The loop filter has a transfer function $F(s)$ and the VCO can be represented by a gain function K_v (radians/sec)/volt and an integrator which integrates frequency to phase. Since the divider divides the VCO frequency, $1/N$ is included in the forward loop as part of the VCO gain.

The transfer function of the closed loop is given by

$$\frac{\phi_o(s)}{\phi_R(s)} = \frac{G(s)}{1 + G(s)\,H(s)} \tag{A1}$$

where

$$G(s) = \frac{K_p K_v F(s)}{sN}$$

$$H(s) = 1$$

Feedback theory states that whenever $G(s)\,H(s) = -1$, the transfer function in equation (A1) has poles in the right-hand half-plane and the system is unstable. This relationship is equivalent to the Bode criteria which says that the system should be stable if the open-loop gain function $H(j\omega)\,G(j\omega)$ falls below unity gain before the

open-loop phase shift reaches -180^{o}. In order to apply the latter criteria in examining the system's stability, a plot of open-loop gain and open-loop phase is necessary.

From equation (A1) the magnitude $\left|H(j\omega)\ G(j\omega)\right|$ is given by

$$\left|H(j\omega)\ G(j\omega)\right| = \left|\frac{K_p K_v F(j\omega)}{j\omega N}\right|$$

A second-order Butterworth filter was used in this analysis; therefore,

$$\left|F(j\omega)\right| = \frac{1}{\sqrt{1 + \left(\frac{\omega}{\omega_o}\right)^4}}$$

and

$$\left|H(j\omega)\ G(j\omega)\right| = \frac{K_p K_v}{\omega N} \frac{1}{\sqrt{1 + \left(\frac{\omega}{\omega_o}\right)^4}} \tag{A2}$$

where

$K_p = \frac{\pi}{6}$ volts/radian

$K_v = 2\pi(1.8 \times 10^6)$ (radians/sec)/volt

$\omega_o = 2\pi(2.5 \times 10^3)$ radians/sec

$N = 1960$

The phase angle of $H(j\omega)\ G(j\omega)$ is given by

$$\angle H(j\omega)\ G(j\omega) = -\frac{\pi}{2} + \angle F(j\omega)$$

$$= -\frac{\pi}{2} - \arctan \frac{\sqrt{2}\,\omega_o \omega}{\omega_o^2 - \omega^2} \tag{A3}$$

From equations (A2) and (A3), the gain and phase response curves of figure 7 were obtained. The phase and gain margins are shown on the plots and indicate that the system is stable if a second-order filter with a cutoff at 2.5 kHz is used.

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