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**DEVELOPMENT OF HIGH TEMPERATURE
GALLIUM PHOSPHIDE RECTIFIERS**

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Prepared by
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16. Abstract Large area high performance, GaP rectifiers have been fabricated by means of Zn diffusion into vapor phase epitaxial GaP. Devices with an active area of 10^{-2} cm² typically exhibit forward voltages of <3 volts for a bias current of 1 ampere and have reverse breakdown voltages of >300 volts for temperatures from 27^o C to 400^o C. Typical device reverse saturation current at a reverse bias of 150 volts is less than 1×10^{-9} amp at 27^o C and less than 50×10^{-6} amp at 400^o C.					
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TABLE OF CONTENTS

	Page
SUMMARY	1
INTRODUCTION	1
MATERIAL GROWTH AND CHARACTERIZATION	5
Vapor Phase Epitaxial Growth Technique	5
Tabulation of Epitaxial Layers Grown for the Program	6
Material Characterization	8
Hall Effect Measurements	8
Photoluminescence	12
Spectroscopic and Absorption Analyses	12
DEVICE FABRICATION	17
Junction Formation	17
Processing and Contacting	17
Packaging	19
DEVICE EVALUATION	22
Techniques and Instrumentation	22
Current-Voltage Characteristics	22
Capacitance-Voltage Characteristics	24
Diode Response Time Measurements	24
Results of Device Evaluation	26
Current-Voltage Characteristics	26
Temperature Dependence of Reverse Current	26
Effect of Thermal Cycling and Heat Treatment on	
Current-Voltage Characteristics	32
Temperature Dependence of Rectifier Forward	
Bias Current-Voltage Characteristics	35
Rectifier Reverse Breakdown Voltage vs. N_D	39
Capacitance Measurements	42
Diode Response Times	44
SUGGESTED FUTURE PROGRAMS	46

LIST OF FIGURES

	Page
1. Avalanche breakdown voltage versus impurity concentration for one-sided abrupt junctions in GaP.	2
2. Depletion layer width at breakdown for one-sided abrupt junctions in GaP.	4
3. Hall constant, R , versus reciprocal temperature, $1/T$, for nitrogen doped and nitrogen free GaP.	10
4. Hall mobility versus temperature for nitrogen doped and nitrogen free GaP.	13
5. Photoluminescence spectrum obtained with undoped VPE GaP ($T=4.2^\circ\text{K}$).	14
6. Photoluminescence spectrum obtained with nitrogen doped VPE GaP ($T=77^\circ\text{K}$).	15
7. Junction reverse breakdown voltage measured at (A) 10 mA/cm^2 and (B) 100 mA/cm^2 versus temperature for a device fabricated with an 80% Au-20% In alloy.	18
8. Junction reverse breakdown voltage measured at (A) 10 mA/cm^2 and (B) 100 mA/cm^2 versus temperature for a device fabricated with an 88% Au - 12% Ge alloy.	20
9. Schematic illustration of standard GaP high temperature rectifier structure.	21
10. Test equipment and circuitry used for measurement of device current-voltage-temperature characteristics in (a) forward bias and (b) reverse bias.	23
11. Test circuitry for radiative decay time constant measurements.	25
12. Rectifier current-voltage characteristics measured at 27 and 400°C .	27
13. Rectifier reverse current versus reciprocal temperature measured at a bias of -150 volts.	29
14. Header leakage current versus reciprocal temperature measured at a bias of -150 volts for headers with (a) glass insulation and (b) ceramic insulation.	30

	Page
15. Rectifier reverse current, curve (a), versus reciprocal temperature for a standard rectifier fabricated on a header using ceramic insulation. Header leakage current shown in curve (b).	31
16. Rectifier forward voltage measured at 1.0 ampere forward current at 27 and 400°C during the required three temperature cycles. Devices exhibit expected temperature dependence.	33
17. Rectifier forward voltage measured at 1.0 ampere forward current at 27 and 400°C during the required three temperature cycles. Devices exhibit anomalous temperature dependence.	34
18. Rectifier forward voltage measured at a constant low forward current versus temperature for a nitrogen doped (NARV1-29-1) and nitrogen free (GP4-80-1) sample. The GaP band gap energy, $E_g(T)$, in electron volts, is also shown.	37
19. Rectifier forward bias current-voltage characteristics at temperatures of 24, 150 and 400°C.	38
20. Logarithm of rectifier current versus voltage at 25 and 400°C.	40
21. Reverse breakdown voltage versus carrier concentration for lightly doped GaP rectifiers.	41
22. [Rectifier capacitance] ⁻² versus voltage obtained with a standard GaP high temperature rectifier.	43
23. Capacitance versus carrier concentration for high purity GaP high temperature rectifiers.	45

LIST OF TABLES

	Page
I	Tabulation of Wafers Grown for the Program. 7
II	Electrical Property Data for GaP. 9
III	Trace Impurities in Undoped VPE GaP by Emission Spectroscopy. 16
IV	GaP Rectifier (25°C) Radiative Decay Time Constants. 46
V	Device Characteristics for Sample Rectifiers Supplied to NASA. 48

SUMMARY

The objective of this program was to develop a high temperature GaP rectifier with a current carrying capacity of 1 ampere with a forward voltage drop of < 4 volts and a reverse breakdown voltage of > 150 volts at a leakage current of < 0.1 ma at room temperature and < 5.0 ma at 400°C. The program involved the evaluation of different GaP epitaxial growth procedures and device fabrication techniques.

All of the device requirements of the program have been surpassed. Rectifiers have routinely been fabricated with forward voltages of < 3.0 volts and reverse breakdown voltages of > 250 volts (> 400 volts for the best devices) with leakage currents of < 0.01 μ A at room temperature and < 0.5 ma at 400°C.

A variety of GaP epitaxial growth parameters have been investigated including substrate carrier concentration, impurity type, epitaxial layer thickness, carrier concentration and the effect of nitrogen doping. As a result of this work a GaP material specification has been developed which will routinely yield high performance devices.

Device fabrication and packaging techniques have been developed which allow device operation to temperatures in excess of 400°C. These techniques include the formation of a suitable p/n junction, high temperature ohmic contacts, and a stress relief pad which matches the linear coefficient of thermal expansion of GaP.

This work represents a major step forward in GaP material and device technology and makes the fabrication of GaP active components, such as transistors and monolithic light emitting arrays with memory, realistic possibilities for the future.

INTRODUCTION

High temperature rectifier design considerations can be broken into three general areas; epitaxial layer carrier concentration and geometry, junction formation, and contacting and encapsulation.

In order for a GaP rectifier to exhibit a reverse breakdown voltage in excess of 150 volts the net carrier concentration in the vicinity of the p-n junction must be less than $10^{16}/\text{cm}^3$ as can be seen in Figure 1. The solid line in Figure 1 has been calculated for an abrupt junction by Sze and Gibbons.

In order to minimize the device series resistance, and hence the forward voltage drop, it is necessary that the lightly doped region of the device

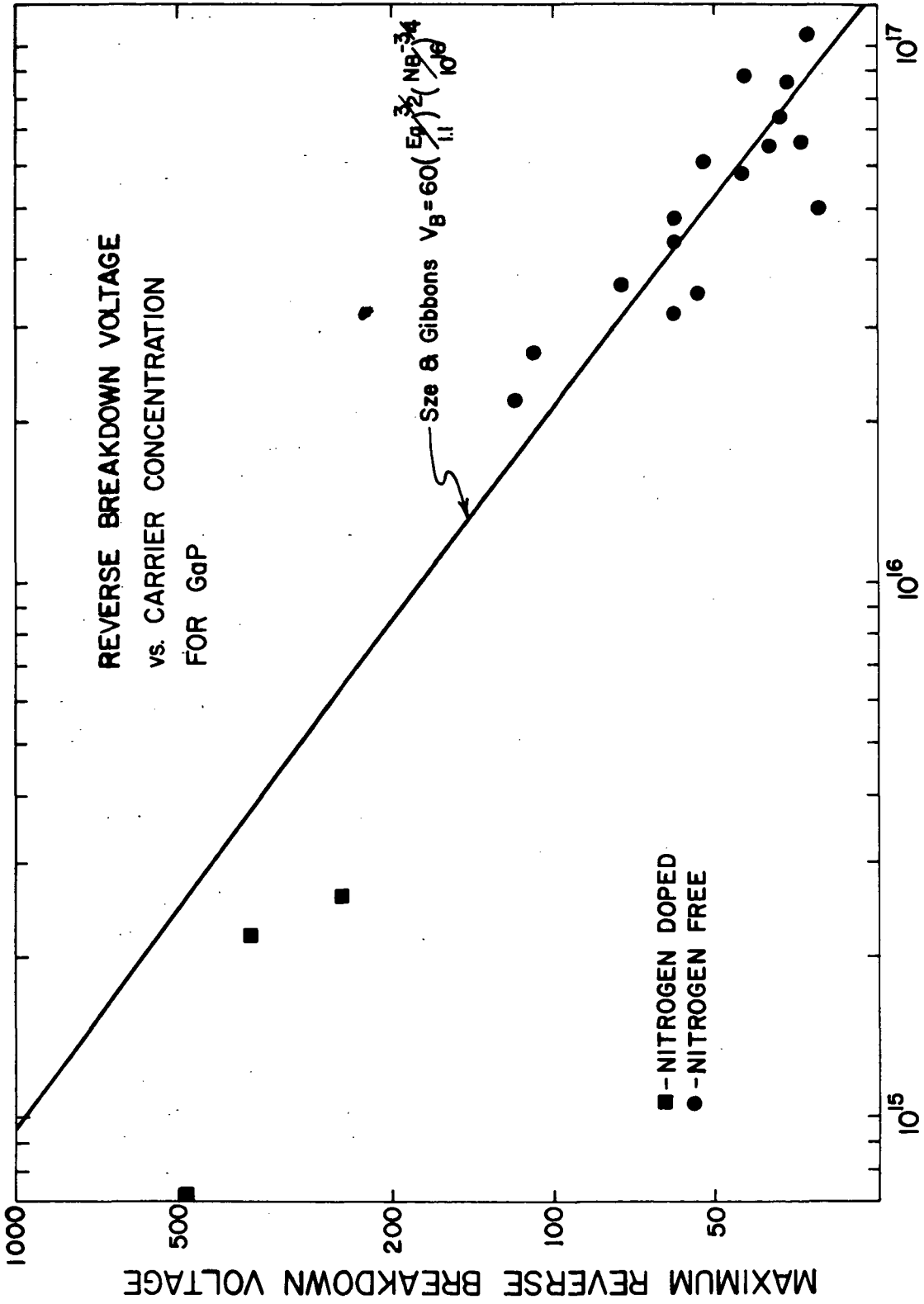


Figure 1. Avalanche Breakdown Voltage versus Impurity Concentration for One-Sided Abrupt Junctions in GaP

structure have the minimum possible thickness. The minimum thickness is determined by the depth of the p-n junction and the width of the depletion region at maximum reverse bias. The width of the depletion region increases with increasing bias voltage as shown in Figure 2. If the depletion region extends into the n⁺ region, premature breakdown will occur due to punch-through. For a reverse breakdown voltage of 150 volts the depletion layer width is $\approx 4 \mu\text{m}$ and corresponds to a carrier concentration of $\approx 10^{16}/\text{cm}^3$ as discussed above. Thus if we assume a junction depth of 5 - 7 μm , the minimum layer thickness required would be $\approx 10 \mu\text{m}$. However, as will be discussed below, it was found that epitaxial layers with carrier concentrations of $\approx 10^{15}/\text{cm}^3$ and reverse breakdown voltages of ≈ 400 volts could be achieved. A breakdown of 400 volts corresponds to a depletion layer thickness of $\approx 20 \mu\text{m}$. Thus the thickness of the lightly doped epitaxial layers is chosen to be 25-30 μm .

The lightly doped epitaxial layers are grown on substrates with high net carrier concentration in order to minimize the device series resistance. The maximum carrier concentration in GaP substrates is limited to $\approx 10^{18}/\text{cm}^3$ based on solubility considerations. The advantages which can be gained by using an n/n⁺ structure instead of having a carrier concentration of $\approx 10^{16}/\text{cm}^3$ throughout the device can be readily calculated. For ease in device fabrication, a minimum total die thickness of 150 μm is desirable. Thus a typical device structure consists of a 25 μm thick n region with $n < 10^{16}/\text{cm}^3$ and a 125 μm thick n⁺ substrate with a carrier concentration of $\approx 10^{18}/\text{cm}^3$. The series resistance represented by an n-type layer doped $\approx 10^{18}/\text{cm}^3$ with an associated room temperature mobility of $\approx 100 \text{ cm}^2/\text{V-sec}$, a thickness of ≈ 125 microns and an active area of $\approx 1 \times 10^{-2} \text{ cm}^2$ is $\approx 0.08 \Omega$. In contrast, the series resistance represented by a uniformly doped device with a doping level of $\approx 10^{16}$ and associated mobility of $\approx 180 \text{ cm}^2/\text{V-sec}$ would be $\approx 4.4 \Omega$. Thus the n/n⁺ structure yields a reduction in forward voltage at 1 ampere forward current of more than four volts as compared with the uniformly doped structure. Because of the reduction in forward voltage and heat dissipation the composite two layer structure also allows for a higher device current density and subsequently, a reduction in required device size for a given current rating.

The device area should be reduced as much as possible consistent with maintaining a forward voltage drop, at the operating current of 1 ampere, which is safely below the specified 4 volt maximum. By minimizing the device area the yield of devices with a maximum breakdown voltage is increased since the probability of encountering defects increases with the area. A device area of 10^{-2} cm^2 has been found to be suitable. This results in a current density of 1.00 A/cm² at 1 ampere which is similar to the current densities employed in high power silicon devices.

The p-n junction fabrication technique must yield a planar junction, since spikes in the diffusion profile will give rise to regions of increased field,

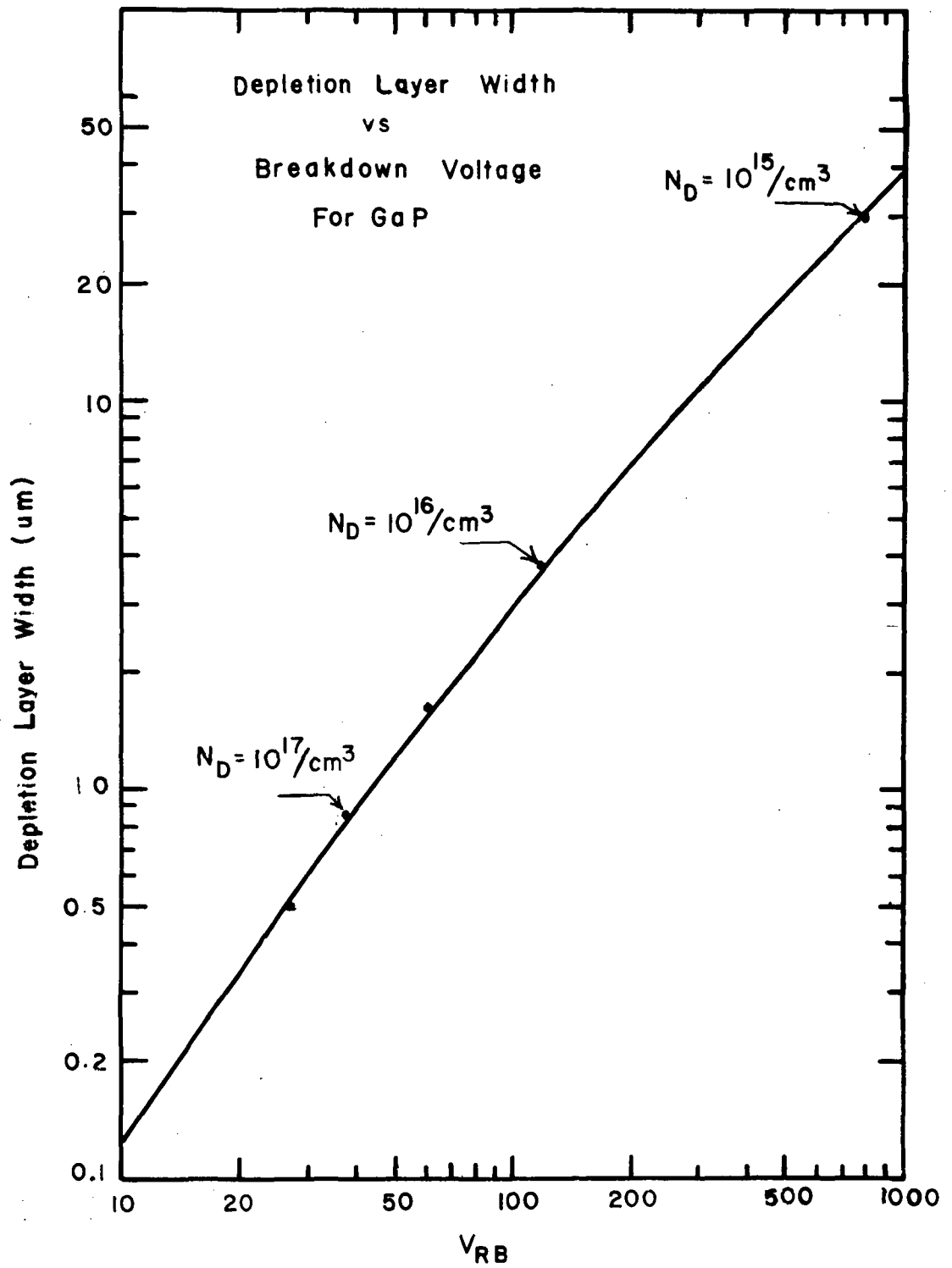


Figure 2. Depletion Layer Width at Breakdown for One-Sided Abrupt Junctions in GaP

and consequently, premature breakdown. Further, the p-n junction must be relatively abrupt since a broadly graded junction would increase the device dynamic resistance, resulting in larger forward voltage drops. Finally the p⁺ region of the crystal should have a sufficiently high surface concentration so that low impedance ohmic contacts can be readily formed.

The ohmic contacts which are made to the p-type regions of the device must have the lowest possible resistance so that current can be passed through the device with a minimum of joule heating. It is rather difficult to form ohmic contacts on GaP, particularly on lightly doped n-type GaP that are truly low resistance. Utilization of the n/n⁺ structure discussed above has the additional advantage that it is not necessary to contact lightly doped n-type material. In fact for carrier densities greater than $\approx 5 \times 10^{17}/\text{cm}^3$, abrupt junction (e. g., metal-semiconductor junctions) current-voltage characteristics are dominated by the tunneling mechanism and thus the ohmic contacting problem is vastly simplified. In addition to providing an ohmic contact, the metallization on the p-type side of the chip must have a sheet conductivity high enough to minimize spreading resistance and current crowding adjacent to the wire bonds on the crystal.

The metalized chip must be attached to a stress relief pad in order to minimize crystal strain during thermal cycling. The stress relief pad must have a linear coefficient of thermal expansion which closely matches that of the GaP crystal, and further the stress relief pad must have the maximum possible thermal conductivity in order to efficiently remove heat from the device.

The contacted device must be mounted in a package which will withstand thermal cycling to temperatures in excess of 400°C. The device package must provide a heat sink such that heat is transmitted away from the junction region as efficiently as possible and must also provide a capability for the required hermetic seal.

MATERIAL GROWTH AND CHARACTERIZATION

Vapor Phase Epitaxial Growth Technique

Material used in the fabrication of these devices was prepared by the VPE growth of thin ($\approx 30 \mu\text{m}$), high resistivity layers on low resistivity liquid encapsulated Czochralski (LEC) substrates. The growth was carried out in an open tube system using PH₃ with HCl transport of Ga. Both PH₃, as a 5% mixture in H₂, and HCl were ultra high purity grade obtained from Precision Gas Products, Inc. The other reagents were AIAG 99.9999%

Ga and H₂ purified by Pd diffusion. HCl at 3 ml/min. (STP) diluted with 50 ml/min. of H₂ was passed over Ga at close to 780°C to form GaCl vapor which then is mixed with the main H₂ stream of 450 ml/min. including 10 ml/min. of 5% PH₃ in H₂ mixture. From the mixing zone at 930°C, the combined reactant gas stream was passed over the horizontally supported substrates located at 800°C to 850°C in a temperature gradient of 10°C/cm. Epitaxial layers were grown at a rate of ≈ 10 microns/hr. Routinely, the epitaxial layer thickness was in the range of from 25 to 35 μm and uniform to within ± 1 μm for a given wafer.

The epitaxial layers were doped with nitrogen, an isoelectronic impurity, to a concentration of ≈ 10¹⁹ cm⁻³, and were otherwise not intentionally doped. Studies, carried out by Monsanto Company prior to the initiation of this program, demonstrated that, under the growth conditions employed here, the incorporation of nitrogen reduces the effective donor concentration in the epitaxial layers as evidenced by increased junction reverse breakdown voltage and decreased junction zero bias capacitance.

Nitrogen doped epitaxial layers grown for this program have exhibited carrier densities as low as 3 x 10¹⁴/cm³, determined by Au-GaP Schottky barrier C-V analysis. Epitaxial layers grown in the same reactors, but without nitrogen doping, have background carrier concentrations of ≈ 10¹⁶/cm³. The mechanism by which nitrogen doping reduces carrier concentration is discussed later in this report.

Substrates for this work were obtained from bulk single crystal GaP ingots pulled by the LEC method at the Monsanto Commercial Products Company, St. Peters, Missouri facility. Sawed wafers, oriented about 5° off the (100) were mechanically polished and cleaned, and then, just prior to use, chemically etched in fresh, warm HCl:HNO₃:H₂O solution. The substrates were doped with either S or Te. Substrates with a variety of carrier concentrations were employed in order to determine the effect of the substrate carrier concentration on the properties of the epitaxial layer.

Tabulation of Epitaxial Layers Grown for the Program

A tabulation of the wafers grown during this program is shown in Table I. The epitaxial layer thickness of each wafer grown was measured by cleaving the crystal and staining the cleaved surface with an etch. The thickness of the grown layer was then measured with a 500x optical microscope. The room temperature net carrier concentrations were determined by Hall measurements on test layers, grown on Cr doped, insulating substrates, which were placed in the growth zone adjacent to the wafers. The nitrogen concentration was determined by optical absorption measurements as described later.

Table I
Tabulation of Wafers Grown for the Program

Sample	Substrate Doping	Layer Thick.	$T_{300^\circ\text{K}}$	Nitrogen Conc. $\times 10^{19}/\text{cm}^3$	$V_f(20\text{A}/\text{cm}^2)$	$\text{VRB}(\text{max}/\text{min})$ (Area 10^{-3}cm^2)	$\text{VRB}(\text{ave})$ (Area 10^{-3}cm^2)	Yield for 10^{-2}cm^2 Devices
NARV1-29-1	1×10^{18} S	($\approx 23\mu$)	1.7×10^{15}		2.31	525/176	343	12/17
NARV1-29-2	1×10^{18} S	($\approx 8\mu$)	5.6×10^{14}	14	2.16	315/155	232	
NARV1-30-1	1×10^{18} S	19.5	2.4×10^{15}		2.80	420/100	295	
NARV1-30-2	1×10^{18} S	14.2	7.5×10^{14}		2.08	140/70	106	
NARV1-56-1	8×10^{17} S	19.5	4.7×10^{15}		--	--	--	
NARV1-56-2	8×10^{17} S	19.5	1.4×10^{15}		2.19	350/150	271	6/10
NARV1-59-1	6×10^{18} Te	44	2.1×10^{15}		3.64	260/120	198	
NARV1-59-2	1×10^{18} Te	33.5	6×10^{14}		3.25	150/98	130	
NARV1-61-1	8×10^{17} S	31.6	hi P	14	insulating	--	--	
NARV1-61-2	8×10^{17} S	31.2	hi P		insulating	--	--	
NARV1-62-2	8×10^{17} S	86.1	4.3×10^{16}		2.27	25/15	20	
NARV1-65-1	8×10^{17} S	27.0	4×10^{15}	2.7	2.39	390/150	266	7/9
NARV1-65-3	6×10^{18} Te	24.8	1.3×10^{15}	6.3	2.35	250/110	147	0/2
NARV1-66-1	8×10^{17} S	24.6	4.7×10^{15}	0.33	2.26	350/150	255	5/12
NARV1-66-3	6×10^{18} Te	32.6	1.7×10^{15}	0.52	2.23	250/120	175	
NARV1-67-1	2×10^{17} S	29.6	--	3.1	3.03	450/100	166	
NARV1-67-3	2×10^{17} S	31.2	hi P	6.5	insulating	--	--	
NARV1-69-1	2×10^{17} S	23.4	1.5×10^{15}		2.18	375/210	295	6/7
NARV1-69-2	2×10^{17} S	27.3	1.5×10^{15}		2.51	475/150	319	10/12
NARV1-70-1	2×10^{17} S	27.7	2.5×10^{15}		2.42	375/140	253	7/10
NARV1-70-2	2×10^{17} S	37.4	2.5×10^{15}		2.12	390/150	190	8/14
NARV1-71-2	8×10^{17} S	27.3	1.6×10^{15}		3.88	350/100	236	4/10

The device properties of the epitaxial layers are also shown in Table I. The device data presented in this table (i. e., forward voltage, V_F and maximum, minimum, and average reverse breakdown voltages, V_{RB}) were measured on batches of small 12.5 mil x 12.5 mil. (10^{-3} cm²) material evaluation diodes. A minimum of fifteen of these small area devices were fabricated from each wafer. The fabrication and evaluation of a large number of small devices (which are easier and less expensive to fabricate) gives a determination of the properties of the epitaxial structure which is more accurate, from a statistical point of view, than would the fabrication of smaller numbers of large samples.

Also shown in Table I is the fabrication yield obtained for the fabrication of full-size (10^{-2} cm²) rectifiers. The ratio shown in Table I is the number of devices which were fabricated that met the required specifications divided by the total number of full-size devices fabricated from the wafer. It can be seen that for most of the wafers, with suitable properties, the device yield was 50% or higher.

Material Characterization

Hall Effect Measurements

The analysis of the temperature dependence of the Hall coefficient can result in values for the donor and acceptor concentration, N_D and N_A respectively, and for the activation energy E_A , of the majority impurity involved. In addition the temperature dependence of the Hall mobility yields information about the scattering centers present. For this reason the temperature dependence of the Hall coefficient and resistivity were measured for several samples.

For the particular reactor used to grow these samples, the addition of nitrogen dopant lowers the carrier concentration considerably. This can be seen in the data in Table II and the temperature dependence of Hall coefficient in Figure 3 for samples G24-8-2 and RVI-39-4. The analyses show an increase in N_A and a decrease in N_D when N is added, and the activation energy for the N doped sample is roughly twice that for the undoped sample. Since the accuracy in determination of E_A from the data is on the order of 10% or better, this difference in E_A is significant and will be considered further.

Photoluminescence (PL) measurements indicate that the residual donor impurities in undoped GaP are either S, Si or both. The upper limit for the activation energy which occurs at lowest concentrations is 0.082eV for Si, ^(2,3) and 0.102eV for S. ^(2,4) This is consistent with the observations on

Table II

Electrical Property Data For GaP

Sample ^a	Dopant	N_{300} ($\times 10^{-15} \text{cm}^{-3}$)	μ_{300} (cm^2/Vsec)	N_{77} ($\times 10^{-13} \text{cm}^{-3}$)	μ_{77} (cm^2/Vsec)	ND ($\times 10^{-15} \text{cm}^{-3}$)	NA ($\times 10^{-15} \text{cm}^{-3}$)	EA (eV)
G24-8-2	none	5.48	183	8.81	2680	6.9	0.48	0.081
RV1-39-4 ^c	N	0.08	97	--	--	3.1	3.0	0.155
RV1-42-1	N, Te	6.09	87	--	--	(29.0) ^d	(25.0) ^d	0.106
NARV1-62-3	N, Te	40.1	151	6.07	498	59.0	1.1	0.090

- a) All samples grown in same reactor, on $\langle 100 \rangle$ oriented substrate
- b) N concentration determined by optical absorption
- c) Substrate removed so that substrate conductivity will not interfere with measurement
- d) These numbers are not trustworthy due to nature of data on this sample

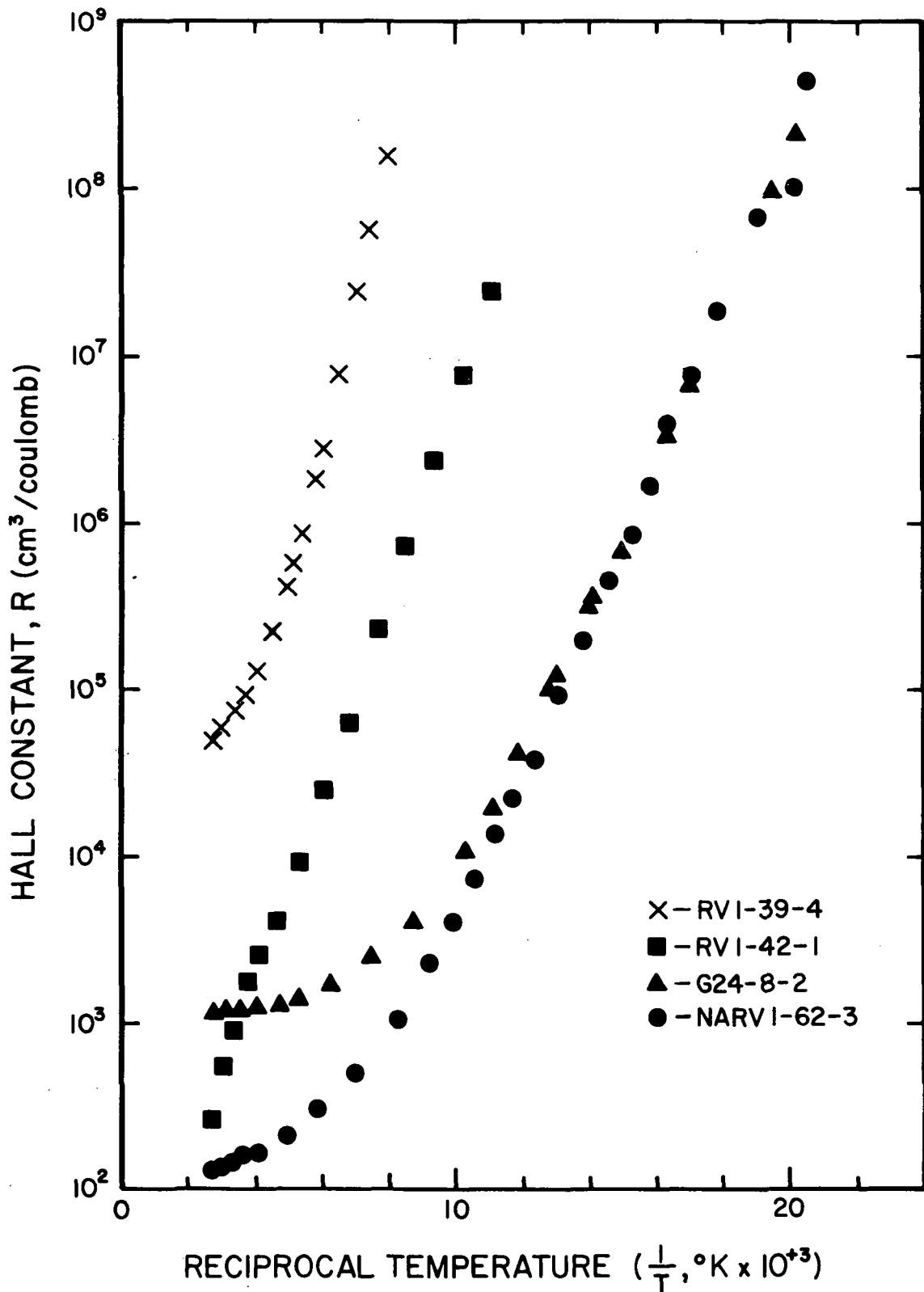


Figure 3. Hall-Constant, R, versus Reciprocal Temperature, $1/T$, for Nitrogen Doped and Nitrogen Free GaP

the undoped sample, since the observed E_A is often smaller than the maximum values just mentioned.

In the case of the N doped sample, a single donor with $E_A \approx 0.15$ eV is predominating. The identity of this level is not known, but various activation energies from 0.2 - 0.55 eV have been observed for GaP which are likely to involve oxygen.⁽³⁾ These are not distinct activation energies, but seem to vary continuously from sample to sample with the variation related to the room temperature carrier concentration. Although the values found here do not exactly fit this published⁽³⁾ relationship, it seems likely that a similar explanation may apply. Other candidates for levels in this region from PL measurements are a Ga-vacancy oxygen complex⁽⁵⁾ at ≈ 0.16 eV and an "unknown donor x"⁽⁵⁾ at 0.153eV.

The question as to whether the N, in some manner eliminates the shallow donor or merely provides compensation can be considered as follows. If simple compensation occurred, one would expect N_A for the nitrogen doped samples to be considerably larger than N_D for the undoped samples. This is not the case for either RV1-39-4 or NARV1-62-3. Thus the addition of nitrogen seems to significantly reduce the shallow donor concentration. The question as to whether the deep donor is added along with the nitrogen or merely "uncovered" by the reduction of the shallow donor concentration can not be answered from this data.

A possible explanation for the reduction of shallow donor by the addition of N could be the competition of the nitrogen with any group VI donor like S for the phosphorus site. This would imply that such a reduction would not take place if the residual donor were Si, which occupies the Ga site. Unfortunately there is not sufficient evidence available at the present to be able to prove or disprove this theory.

Since the lowered carrier concentration of the nitrogen samples limits the range of the Hall and resistivity data available, the question of the reliability of the N_D and N_A estimates arises. Two runs were made in which Te as well as N was added in order to provide information on this point. Sample NARV1-62-3 provides a large range of good data for this purpose as is seen in Figure 3. The E_A for this sample agrees very well with published values^(7,8) for Te as would be expected. Since N_A is roughly the same as that determined for G24-8-2, and RV1-39-4, we can feel fairly confident of these numbers. In addition it seems reasonable to conclude that neither the N nor the Te doping is adding significant compensation to the samples.

The Hall data for RV1-42-1 shows that this sample contains considerably more deep impurity from some unknown source than any of the other 3 samples. The N_A , N_D and E_A results for this sample were obtained using

only the data for $1000/T > 4$, so that N_A and N_D in particular are not too reliable. The high temperature Hall data indicates that a donor level with $E_A \geq 0.14\text{eV}$ is predominant at room temperatures and above.

The mobility data for these samples is presented in Figure 4. This shows quite clearly that the presence of N decreases the mobility, particularly at low temperatures, even though it does not add to the carrier concentration. The amount of the reduction does not appear to be simply related to the N concentration for these three samples. If one eliminates RV1-42-1 from consideration, however, the mobility due to the presence of nitrogen, μ_N , at 150°K (calculated from $(\mu_{\text{meas.}})^{-1} = (\mu_{\text{lattice}})^{-1} + (\mu_N)^{-1}$) is 4 to 8 times that predicted theoretically.⁽⁹⁾ The theoretical curve for μ_N shown in Figure 4 is based on a nitrogen concentration of $10^{19}/\text{cm}^3$. Considering the possible error of 2 to 4 times in the nitrogen concentration calibration (unpublished data from E. C. Lightowers)*, the agreement could be within a factor of 2. The temperature dependence of μ_N (see Figure 4) is not the same as that observed, but this could be due to the presence of some ionized impurity scattering (μ_I shown in Figure 4). The theoretical curve for μ_I shown in Figure 4 corresponds to an ionized impurity concentration of $10^{17}/\text{cm}^3$.

Photoluminescence

Measurements of photoluminescence at 4.2°K and 77°K have been carried out on numerous samples of GaP. Undoped samples show lines related to the presence of Si, S and N (see Figure 5), with either of the former predominating. The extrinsic spectra which is attributed to the presence of Si impurities matches the published data⁽¹¹⁾ very closely. The spectra also indicate that N is present only in very low concentrations. The presence of Cl is also indicated by a wide band at $\approx 7200\text{\AA}$ in undoped material.⁽¹²⁾ The PL of GaP is well enough known and sensitive enough that if any of the other usual (Group II, IV and VI, except O_2) dopants were present in significant amounts, they would have been detected.

In the case of the nitrogen doped crystal, only nitrogen and nitrogen pair lines⁽¹³⁾ are observed. These are efficient enough to allow photoluminescence spectra to be readily measured at 77°K as shown in Figure 6.

Spectroscopic and Absorption Analyses

Nitrogen concentrations in the nitrogen doped epitaxial layers were measured by an optical absorption method.⁽¹⁴⁾ Typical values for these layers, as listed in Table I, lie in the $10^{19}\text{atoms}/\text{cm}^3$ range. The nitrogen concentrations appear to depend strongly on layer thickness, deposition

*The equation in Ref. 10 may give N concentrations 2 to 4 times too high. Comparison of optical absorption and mass spectroscopy done here on 3 samples indicates that the factor may be closer to 4.

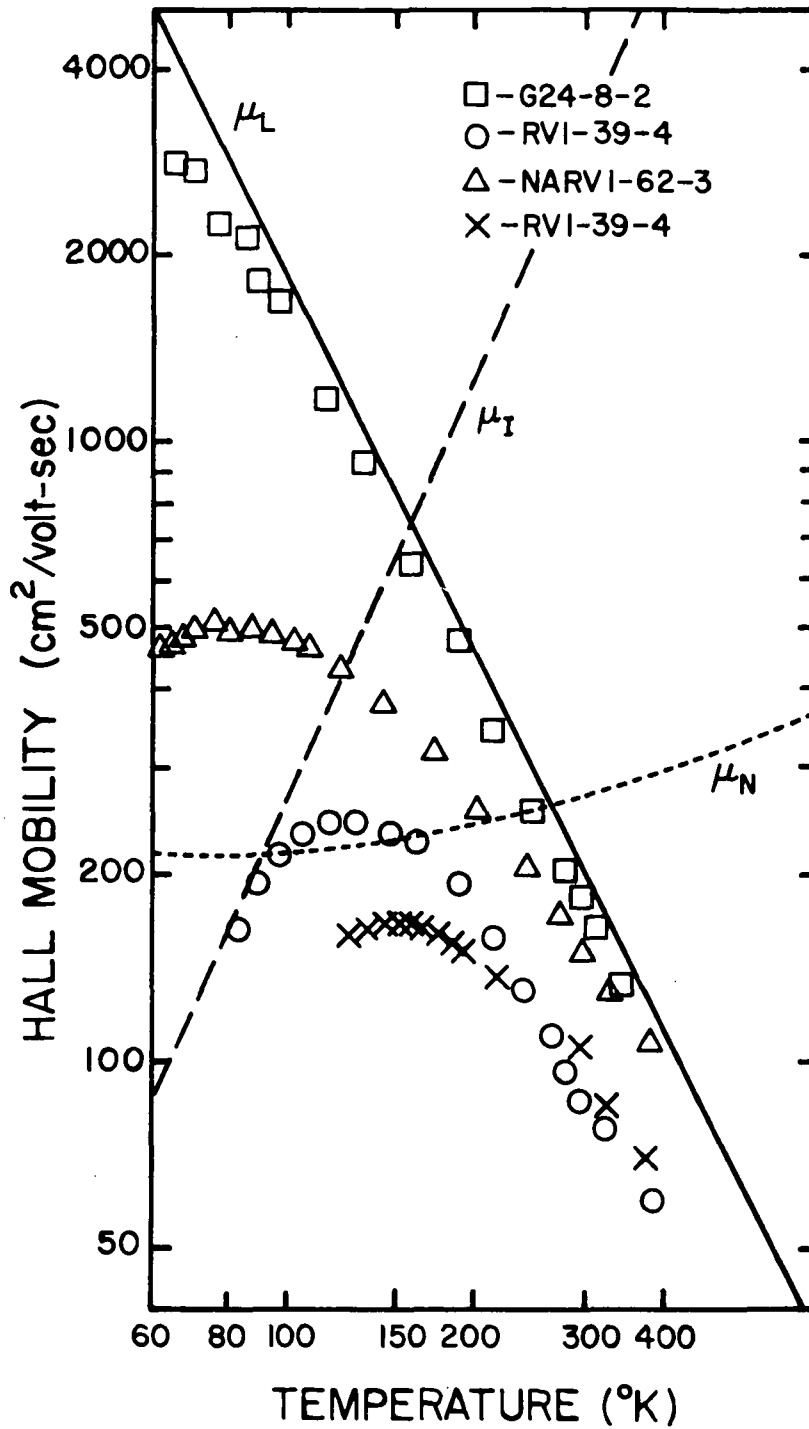


Figure 4. Hall Mobility versus Temperature for Nitrogen Doped and Nitrogen Free GaP

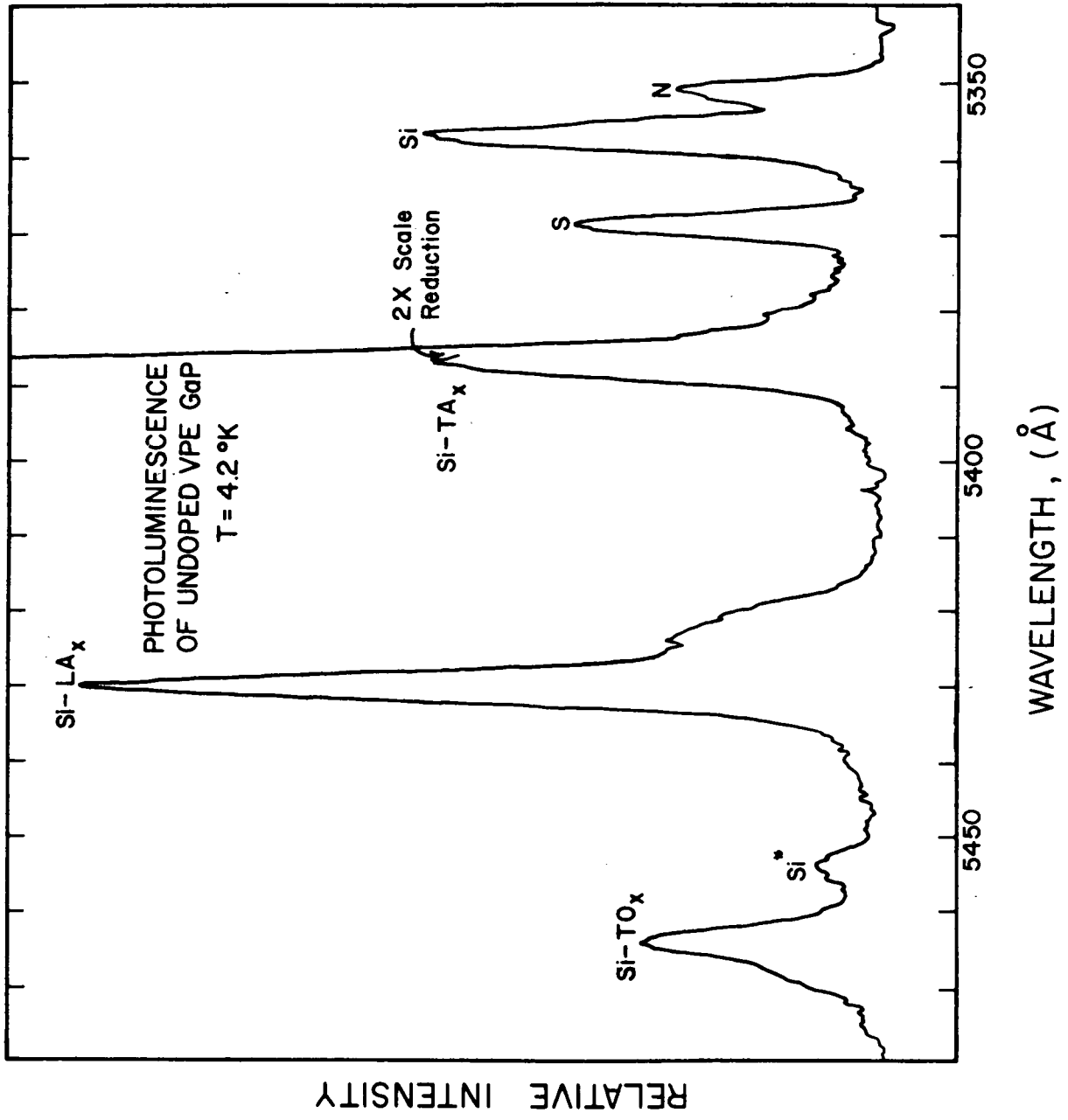


Figure 5. Photoluminescence Spectrum Obtained with Undoped VPE GaP (T=4.2 °K)

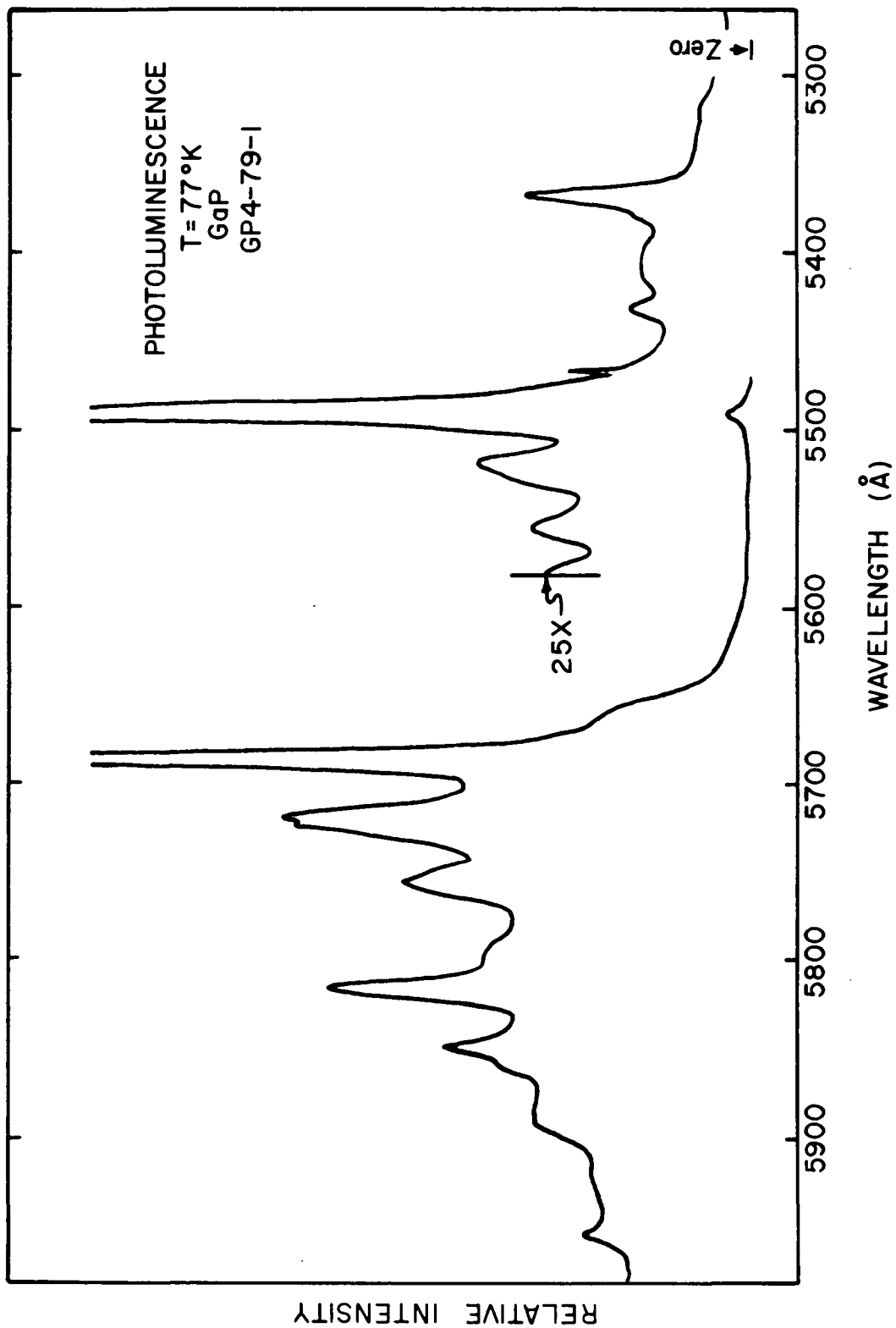


Figure 6. Photoluminescence Spectrum Obtained with Nitrogen Doped VPE GaP (T = 77°K)

temperature, and other unknown factors, to produce a wide scatter in concentration for a given ammonia flow rate. The non-reproducible rate of catalytic decomposition of ammonia undoubtedly plays a role in the run to run variation.

The thin epitaxial layers grown for this study do not provide enough material for quantitative emission spectrographic analysis. Therefore chemical analysis for trace background impurities has been performed on thick, non-intentionally doped layers from which the substrate could be removed. Typical analyses, shown in Table III, demonstrate the very low background contamination in these samples. For example the Si concentrations, corresponding to 1.5×10^{15} and 1.2×10^{15} atoms/cm³, and Cu, $1.4 - 2.1 \times 10^{14}$ atoms/cm³ all well below the donor and acceptor concentrations determined by electrical measurements. Difficulty in growing such thick N doped layers precluded a similar analysis for N doped material.

Table III

Trace Impurities in Undoped VPE GaP by Emission Spectroscopy

Element \ Sample	Concentration	(ppb w/w)
	GP4 -91-1	GP4 -91-2
Si	17	14
Mg	<1	2.5
Al	135	250
Cu	3.5	5.3
Ca	200	300
Ag	---	---
Fe	---	---

DEVICE FABRICATION

Junction Formation

Junctions were formed in the thin epitaxial layer by a closed ampoule Zn diffusion using either a ZnAs_2 or a metallic Zn source. The standard diffusion cycle used during the majority of this program was a 90 minute diffusion at 800°C , using an 8 mg. charge of ZnAs_2 in a 10 cc ampoule. The junction depth was in the range from 5 - 10 μm , typically 6 μm .

Processing and Contacting

Diffused wafers were lapped and polished on the substrate side to a final thickness of $\approx 150 \mu\text{m}$. A thin film of Au-Ge eutectic alloy was vacuum evaporated on the substrate side to improve the n-type side ohmic contact. A thin film of Al was then evaporated onto the p-type side to reduce spreading resistance in the p-type layer. The wafers were then diamond scribed and cleaved into 0.040" x 0.040" chips (10^{-2}cm^2).

The n-type side of the chips were alloyed to stress relief pads using 88% Au - 12% Ge eutectic preforms. Since the Au-Ge eutectic alloy has a melting temperature of 365°C , it was initially thought that these preforms would be unsuitable for this program. However, it was found that during die attachment, the preform metal alloys with the GaP crystal and the Au on the stress relief pad and shifts in composition to an alloy which is stable at the maximum device operating temperature (400°C).

Although the Au-Ge bond has proven to be stable throughout the required temperature range, it is believed to remain soft enough to allow additional stress relief for the crystal during thermal cycling. A number of higher temperature alloys were evaluated and found to be too hard for variable temperature applications. An example of device degradation which is believed to be due to an overly hard alloy bond, is shown in Figure 7. In this case, a chip with an active area of 10^{-3}cm^2 was alloyed to a stress relief pad with an 80% Au-20% In alloy which in turn was alloyed to a TO-46 header. Although the device initially had a reverse voltage capability of $\approx 525\text{V}$ at 25°C , it failed badly at high temperature. Although not shown in Figure 7, the device recovered to its original I-V characteristics when cooled to room temperature.

The stress relief pads used in this work had a composition of 99.5% W and 0.5% Ni and dimensions of 0.150" dia. x 0.015" thick. Stress relief pads

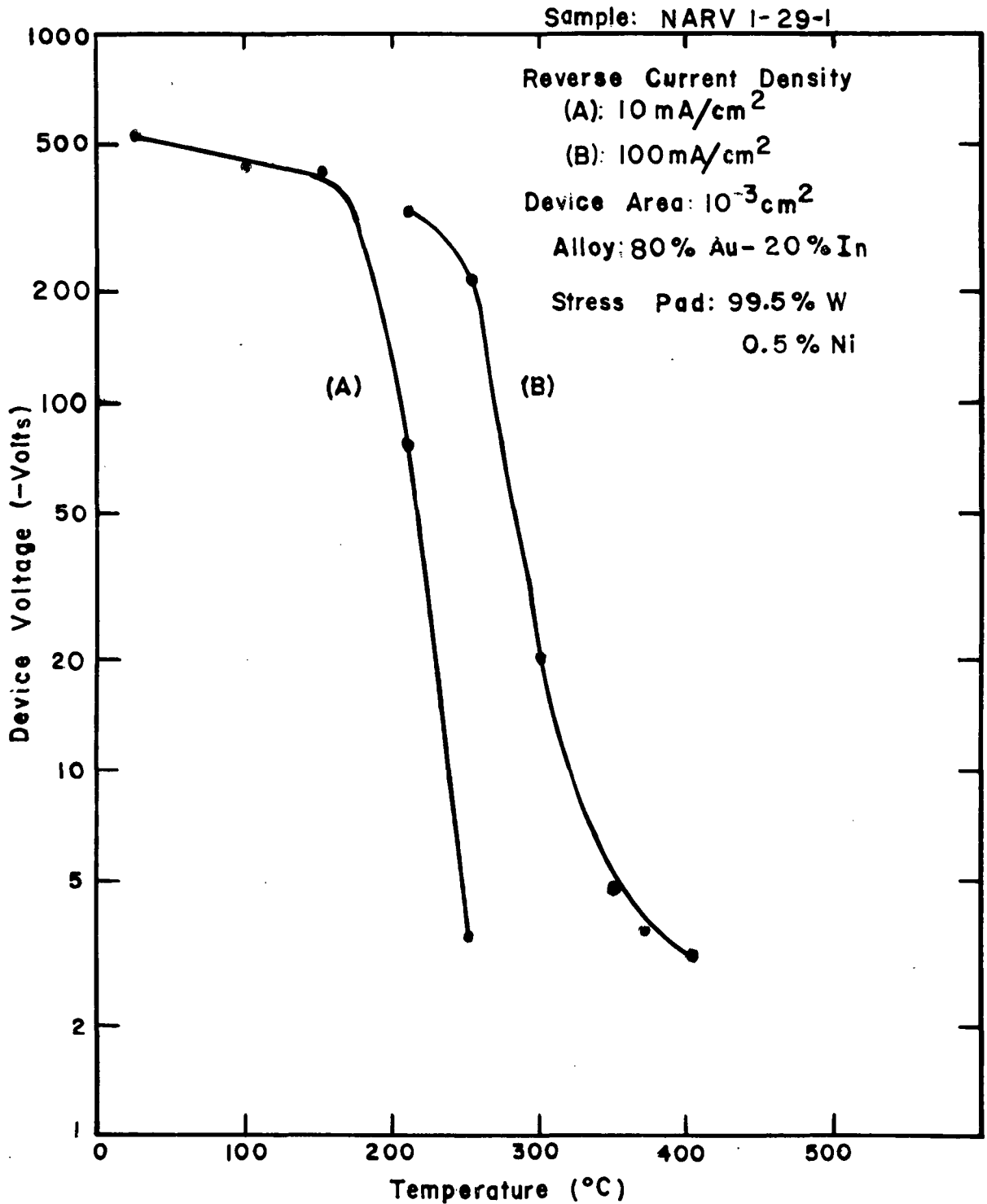


Figure 7. Junction Reverse Breakdown Voltage Measured at (A) 10 mA/cm² and (B) 100 mA/cm² versus Temperature for a Device Fabricated with an 80% Au-20% In Alloy

(grade CW 363) were obtained from Stackpole Carbon Company. To improve wetting of the Au-Ge alloy on the W-Ni stress relief pad, a thin film of Ni followed by a thin film of Au was plated onto the pad by electroless plating.

The GaP chip-stress relief pad subassembly was then attached to a Au plated Kovar TO-5 header with an 88% Au-12% Ge preform in a pure H₂ atmosphere at a temperature of from 450 to 500°C. The resulting alloy bonds have been demonstrated to be stable at high temperatures with successful device operation in excess of 500°C.

The 99.5% W - 0.5% Ni stress relief pads have a coefficient of expansion of $6.9 \times 10^{-6} \text{ }^\circ\text{K}^{-1}$ which very closely matches that of GaP. The thermal conductivity of the stress pad is $\approx 0.35 \text{ cal sec}^{-1} \text{ cm}^{-1} \text{ }^\circ\text{C}^{-1}$ which is appreciably lower than that of Cu but is sufficiently high for most applications.

During the initial stages of this program devices were fabricated without stress pads in order to determine whether or not stress pads were, in fact, essential for the high temperature device operation required in this program. The results of one experiment in which a device was alloyed directly to a TO-46 header with a Au-Ge eutectic alloy are shown in Figure 8. As can be seen, the device initially suffered severe degradation with temperature until the alloy began to soften and relieve the stress which had developed in the crystal. The results strongly implied that crystal strain was responsible for the degradation of performance at high temperature.

Devices which have been fabricated using Au-Ge preforms and W-Ni stress pads have proved highly reliable under repeated temperature cycling to 400°C as discussed later in this report.

Packaging

After the chip is bonded to the stress pad the subassembly is mounted on a standard Kovar TO-5 header. Contact to the p-type side of the chip is accomplished with four ultrasonic bonds using 0.003" Al wire. A standard Ni TO-5 can is then welded to the header, in a dry nitrogen atmosphere, in order to form the hermetic seal. A schematic diagram of a completed rectifier structure is shown in Figure 9.

Although the TO-5 package was satisfactory for this program, since it was inexpensive, easy to use, and withstood high temperature cycling, it is not regarded as a suitable package for general power device applications. A stud mounting package with ceramic insulation would provide improved heat removal from the device and, in addition, would give rise to lower leakage currents at high operating temperatures. (As will be discussed later in this

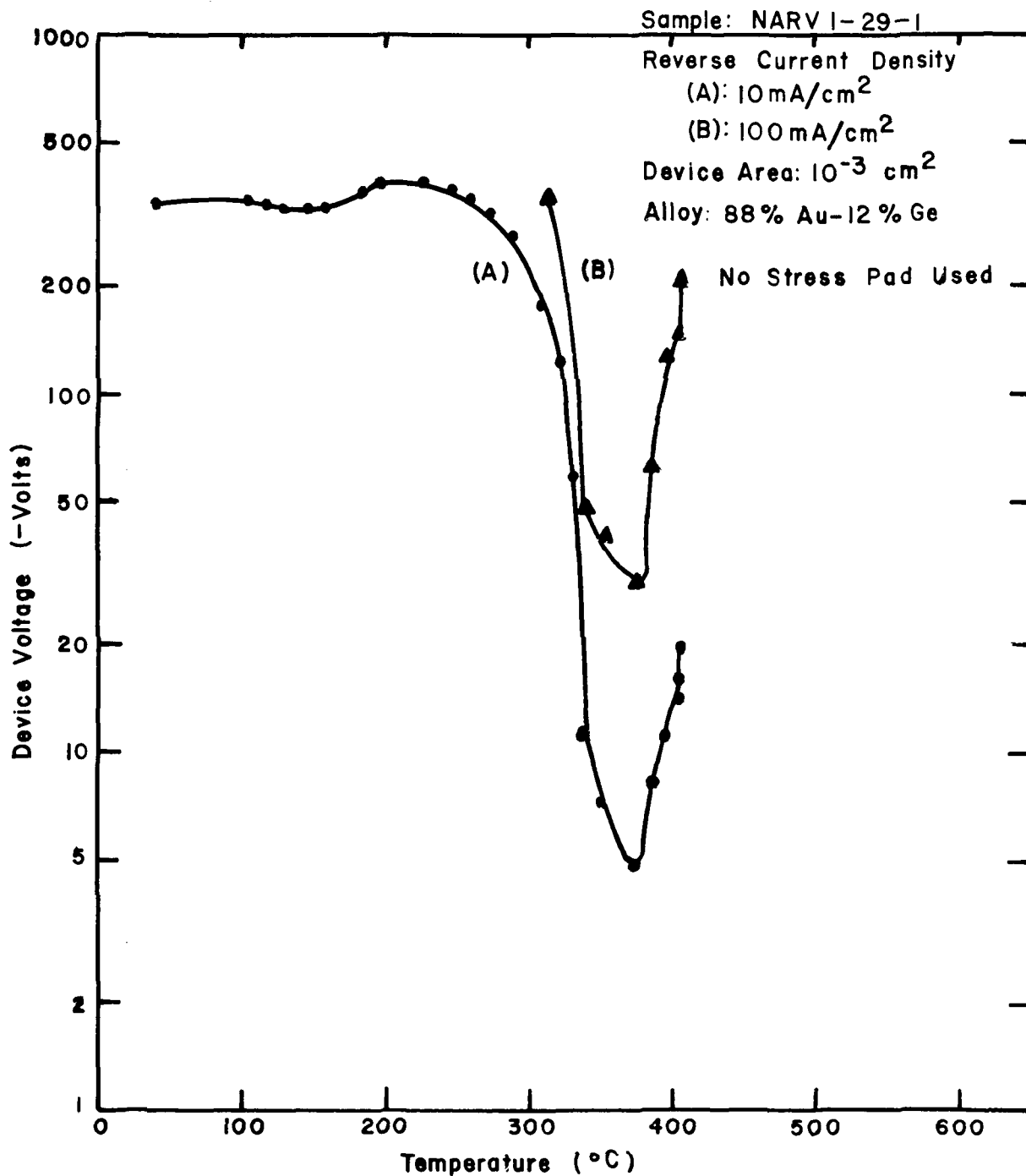


Figure 8. Junction Reverse Breakdown Voltage Measured at (A) 10 mA/cm² and (B) 100 mA/cm² versus Temperature for a Device Fabricated with an 88% Au-12% Ge Alloy

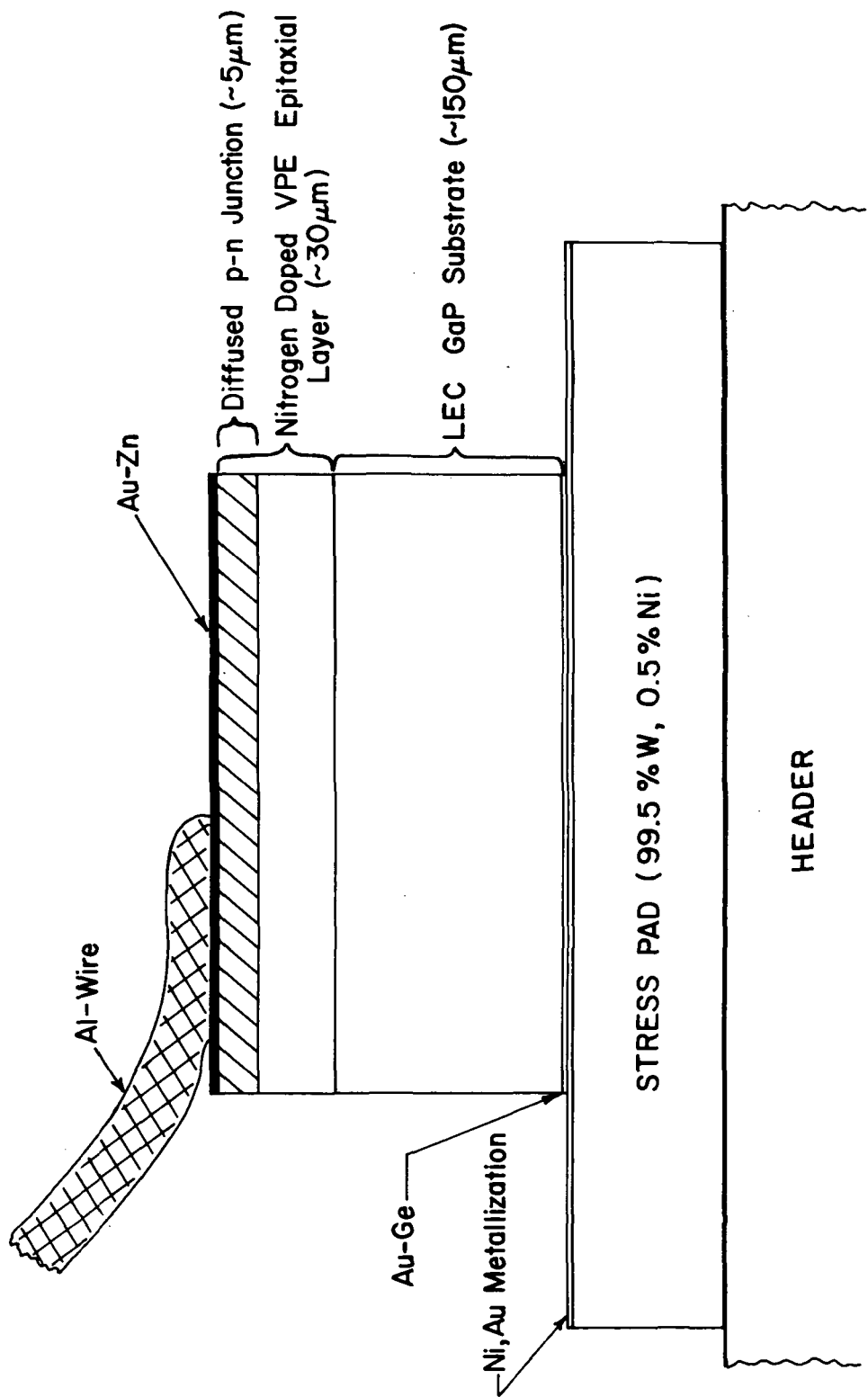


Figure 9. Schematic Illustration of Standard GaP High Temperature Rectifier Structure

report much of the leakage current observed in the devices studied here was due to leakage through the glass insulation of the header and not through p-n junction.) Unfortunately the only available stud mounted ceramic packages, which were compatible with existing bonding equipment, were found to crack when subjected to repeated thermal cycling. Consequently, the TO-5 package was chosen as a satisfactory, if not ideal, package for this program.

DEVICE EVALUATION

Techniques and Instrumentation

Current-Voltage Characteristics

The rectifier terminal characteristics of greatest importance in this work are the device current-voltage characteristics in the temperature range extending from room temperature to 400°C. I-V characteristics were routinely measured with a Tektronix model 575 transistor curve tracer. The calibration of this instrument is traceable to the National Bureau of Standards.

The high temperature operation of the rectifiers was evaluated by placing the devices in an instrumented Thermolyne Corp. model 1400 controlled temperature furnace. The device temperature was monitored with a chromel-alumel thermocouple and a Leeds and Northrup model 8686 potentiometer.

For precision determination of current-voltage characteristics, the instrumentation and circuitry shown in Figure 10 was used. The circuit shown in Figure 10a was used to determine the device forward voltage for forward currents ranging from zero to 1.0 ampere. For this measurement, the digital voltmeter (hp 3460-A) was connected directly across the device terminals for maximum accuracy. Since the voltmeter input impedance is $10^7 \Omega$, negligible errors in current measurements occur in this circuit for device currents greater than 10^{-5} amperes.

The circuit shown in Figure 10b was used to accurately measure reverse bias leakage currents. Since the room temperature reverse bias resistance of full size rectifiers measured at a bias of -150 volts was routinely $\approx 10^{10}$ to $10^{11} \Omega$, it was essential to place the ammeter (Keithley 610R electrometer) between the device under test and the voltmeter. Further-

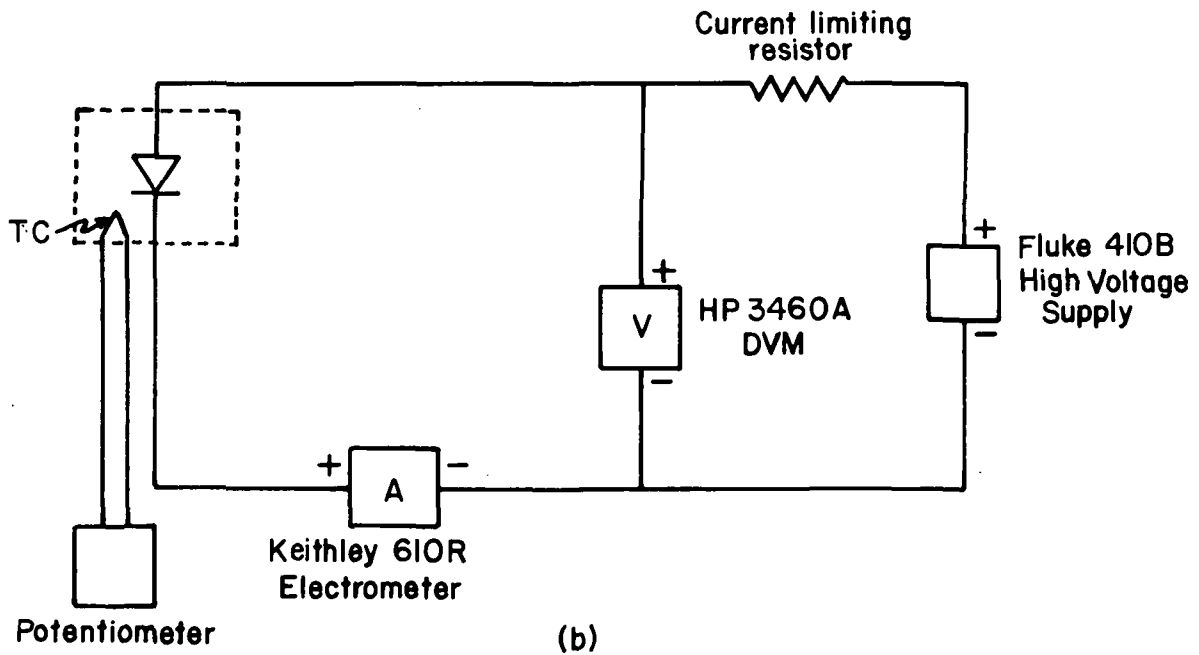
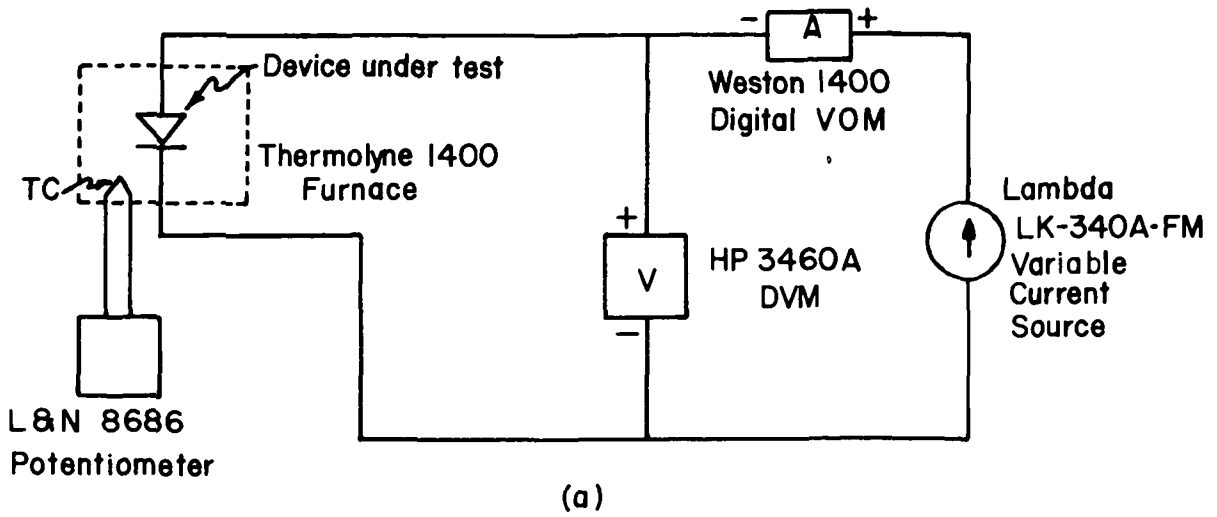


Figure 10. Test Equipment and Circuitry Used for Measurement of Device Current-Voltage-Temperature Characteristics in (a) Forward Bias and (b) Reverse Bias

more, since the voltage drop across the ammeter is less than 10^{-3} volts, the errors incurred in measurement of the reverse bias (for bias values of ≈ 150 volts) were negligible.

Capacitance-Voltage Characteristics

Capacitance and capacitance-voltage measurements were routinely made using a Boonton Electric Corporation model 75A-54 (1MHZ) capacitance bridge. The C-V measurements as presented on pages 42-44 were used to determine the gradation of the diffused junctions and the impurity profiles of the epitaxial layers.

Diode Response Time Measurements

Since the switching speed obtained in the standard diode reverse recovery time measurement is a function of both the initial diode forward current and pulsed reverse current, the maximum diode turn-off times were determined by measuring the radiative decay time constants of pulsed diodes.

Rectifier electroluminescent radiative decay time constants were determined by detecting pulsed diode emission with an apertured RCA C70042K photomultiplier (rise-time $t_r < 2$ nsec) and displaying the detected signal with a Tektronix model 567 digital readout oscilloscope fitted with sampling amplifier ($t_r < 0.35$ nsec) and trigger modules. The exponential radiative decay time constants were determined directly with the oscilloscope digital unit by measuring the time required for the optical pulse to decay from 73% to 27% of its peak value. Diode excitation was supplied by a Spencer-Kennedy Labs model 503A charged line pulser ($t_r < 0.5$ nsec). The experimental arrangement for decay time constant measurements is shown in Figure 11. Our present capability allows for measurement of radiative decay time constants of ≈ 2 nsec or greater.

All voltmeters and ammeters used in this work were calibrated against Eppley Laboratory, Inc. standard cell No. 835347 with a Leeds and Northrup model K-3 potentiometer and General Radio Company standard resistors.

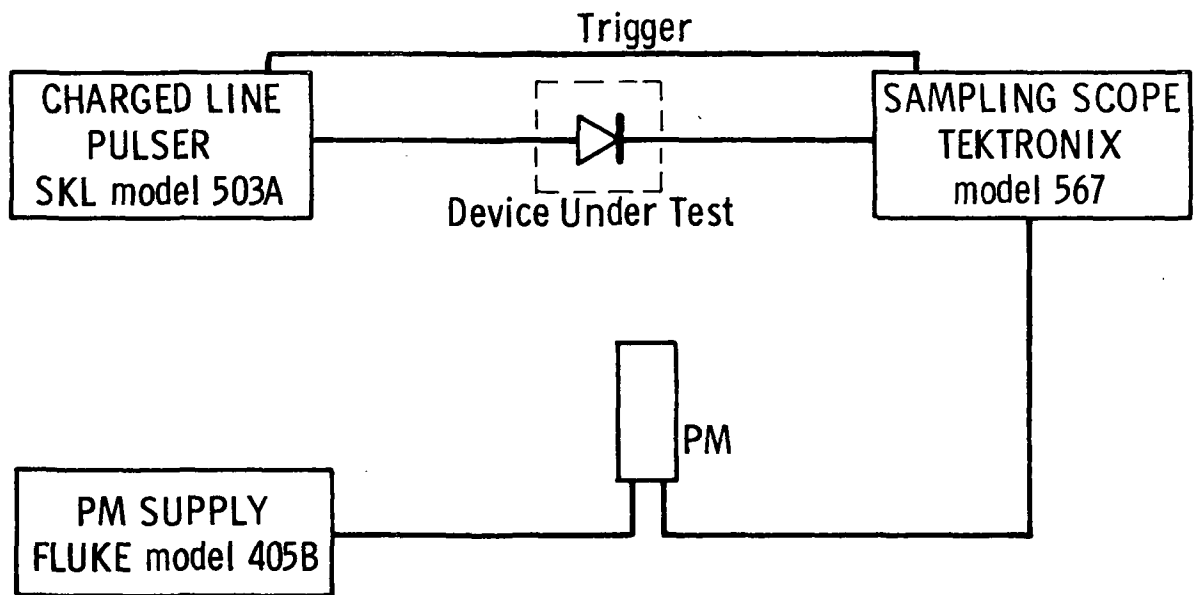


Figure 11. Test Circuitry for Radiative Decay Time Constant Measurements

Results of Device Evaluation

Current-Voltage Characteristics

The room-temperature and 400°C current-voltage characteristics of one of the rectifiers fabricated and tested for this program are shown in Figure 12a and 12b respectively. As seen in Figure 12a, $T = 27^\circ\text{C}$, this device has a forward voltage of 2.6 volts at a forward current of 1.0 amperes with a dynamic resistance at this bias condition of 0.77Ω . In reverse bias, the device exhibits negligible reverse current for voltages in excess of -250 volts. In fact, this particular device exhibited a reverse current of only 6×10^{-9} amperes at a bias of -150 volts.

At a temperature of 400°C, as shown in Figure 12b, the device offers a slightly lower forward voltage of 2.5 volts at a forward current of 1.0 amperes. The dynamic resistance at this bias condition is 1.5Ω or approximately double that which was observed at room temperature. This increase in series resistance is considered to be caused primarily by a reduction in mobility of majority carriers in the n and p regions due to increased phonon scattering.

In the reverse bias condition, leakage current is now noticeable but still at quite an acceptable level of ≈ 0.1 mA at -150 volts bias and ≈ 0.5 mA at -250 volts bias, well within the 5.0 mA at -150 volt bias specification. This particular device was assembled on a header which used a ceramic insulation which yielded a considerable reduction in total device leakage current at high temperatures. This issue will be treated more fully in the next section.

Temperature Dependence of Reverse Current

Since it had been determined that rectifier reverse breakdown voltage was controlled primarily by point defects and not by bulk avalanche (see pages 39-42) and that operation of these devices into reverse breakdown often caused catastrophic failure, it became necessary to monitor the reverse current at a reverse bias of 150 volts as a function of temperature rather than monitoring the reverse breakdown voltage at a given reverse current as a function of temperature. The results of the measurement of reverse leakage current at -150 volts bias as a function of temperature during two thermal cycles from 27 to 400°C for a standard full size rectifier are shown in Figure 13 as a plot of the logarithm of reverse current versus reciprocal temperature. As seen in Figure 13, the plot is linear over at least three decades of current. By fitting the curve to the

NARVI-69-1

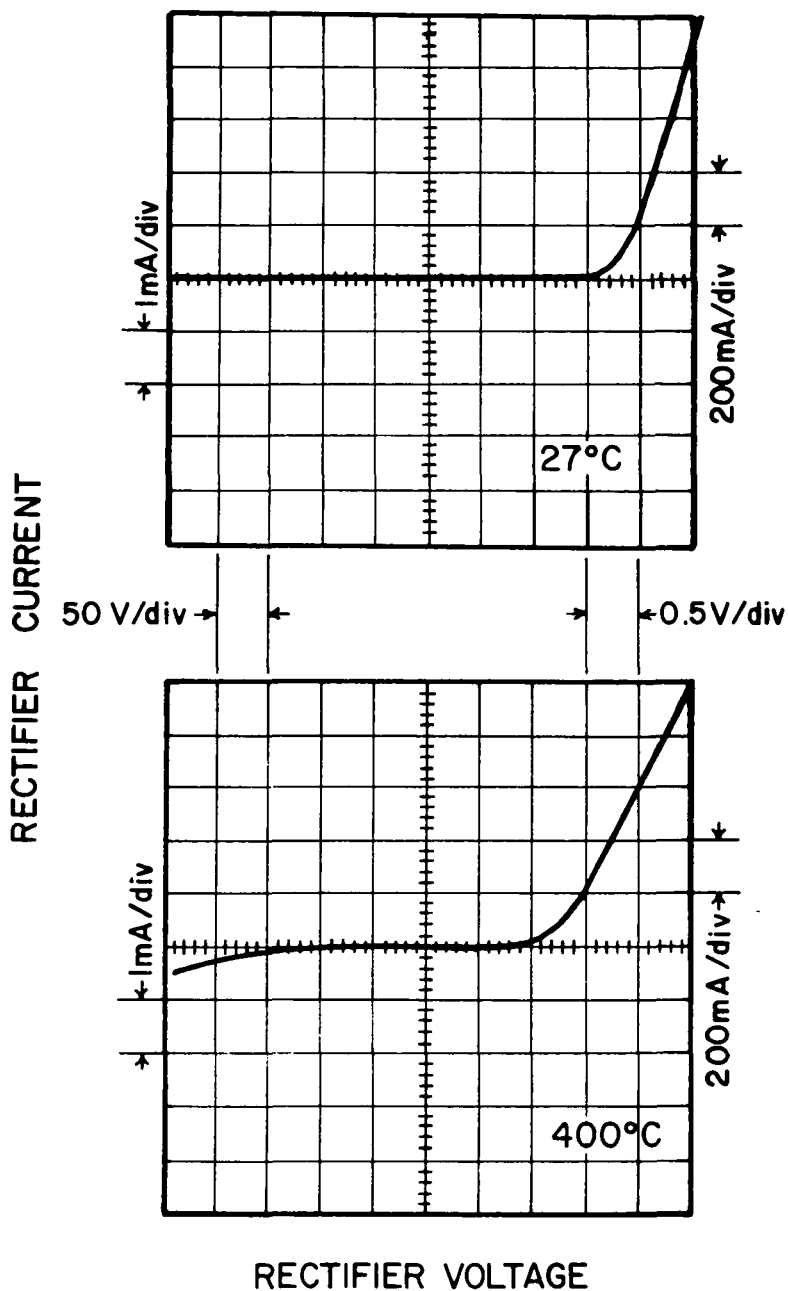


Figure 12. Rectifier Current-Voltage Characteristics Measured at 27 and 400°C

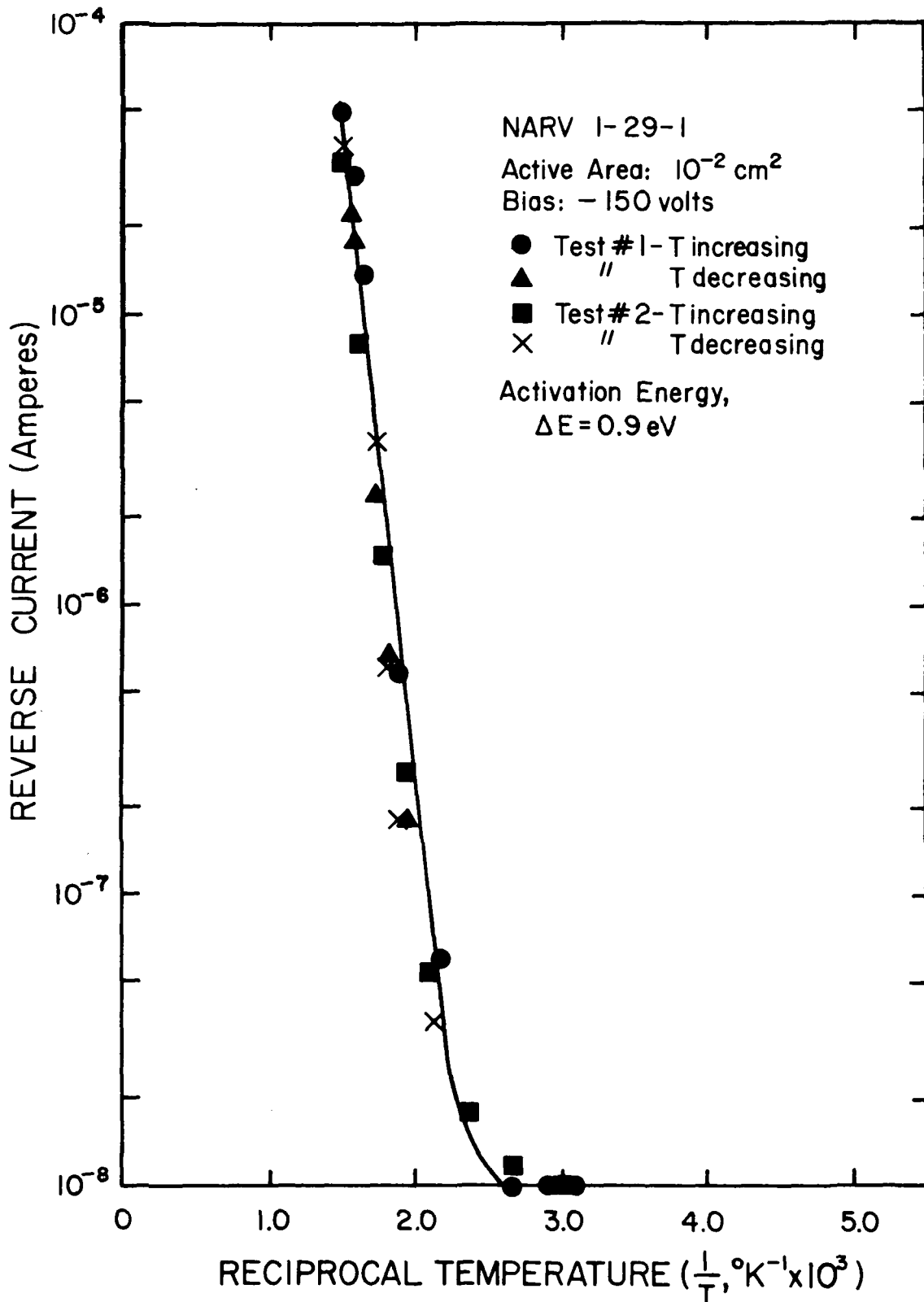


Figure 13. Rectifier Reverse Current versus Reciprocal Temperature Measured at a Bias of -150 Volts

relationship $I_R = I_0 \exp(-\Delta E/kT)$ where I_R is the reverse current, I_0 is a constant, ΔE is the thermal activation energy for reverse current, k is the Boltzmann constant, and T is the absolute temperature, an activation energy for reverse current of $\Delta E \approx 0.9\text{eV}$ is obtained.

Since the minimum activation energy of reverse current due to thermal generation of carriers via traps in the junction depletion regions is one half the bandgap, E_g , for a trap state at the center of the bandgap, the observed leakage current could not be attributed to semiconductor bulk or p-n junction processes.

Tests were then conducted to determine if any of the instrumentation of high temperature wiring was responsible for the observed anomalous behavior. These tests proved to be negative. Subsequently the standard TO-5 headers used in this work were tested. The results are shown in Figure 14a. It was found that the glass insulation used in isolating the header leads from the header base was responsible for a major portion of the leakage current observed at high temperature for standard devices. Furthermore, the insulator leakage current had an activation energy, ΔE , of 0.925 eV and exhibited the exponential current dependence for over 4 decades of current.

Subsequently, other headers were examined and it was found that although a stud mounting TO-5 type header having a ceramic insulator exhibited leakage currents approximately 2 orders of magnitude lower than the standard TO-5 header, the leakage current (see Figure 14b) still obeyed the exponential dependence and exhibited an activation energy of 0.925eV, identical to that observed for glass insulators.

In order to obtain a more accurate determination of actual junction leakage current, rectifiers were fabricated in stud mounting TO-5 type headers which used ceramic insulation. The results of the reverse current measurements are shown in Figure 15a. Also plotted in 15b is the leakage of the same header after the Al bonds were removed from the chip. As can be seen in Figure 15, the header, in this case, accounts for only $\approx 1\%$ of the total leakage current as compared with $\approx 50\%$ for devices fabricated on standard TO-5 headers. Although the observed activation energy for the device represented in Figure 15a is somewhat greater at 0.95eV, it is still less than $E_g/2$ and is not entirely understood. Device surface leakage, for example, may be responsible in part for the excess reverse current. The surface current component of device leakage should be related to the device edge length rather than junction area. Experimental evidence supporting this hypothesis however has not as yet been obtained.

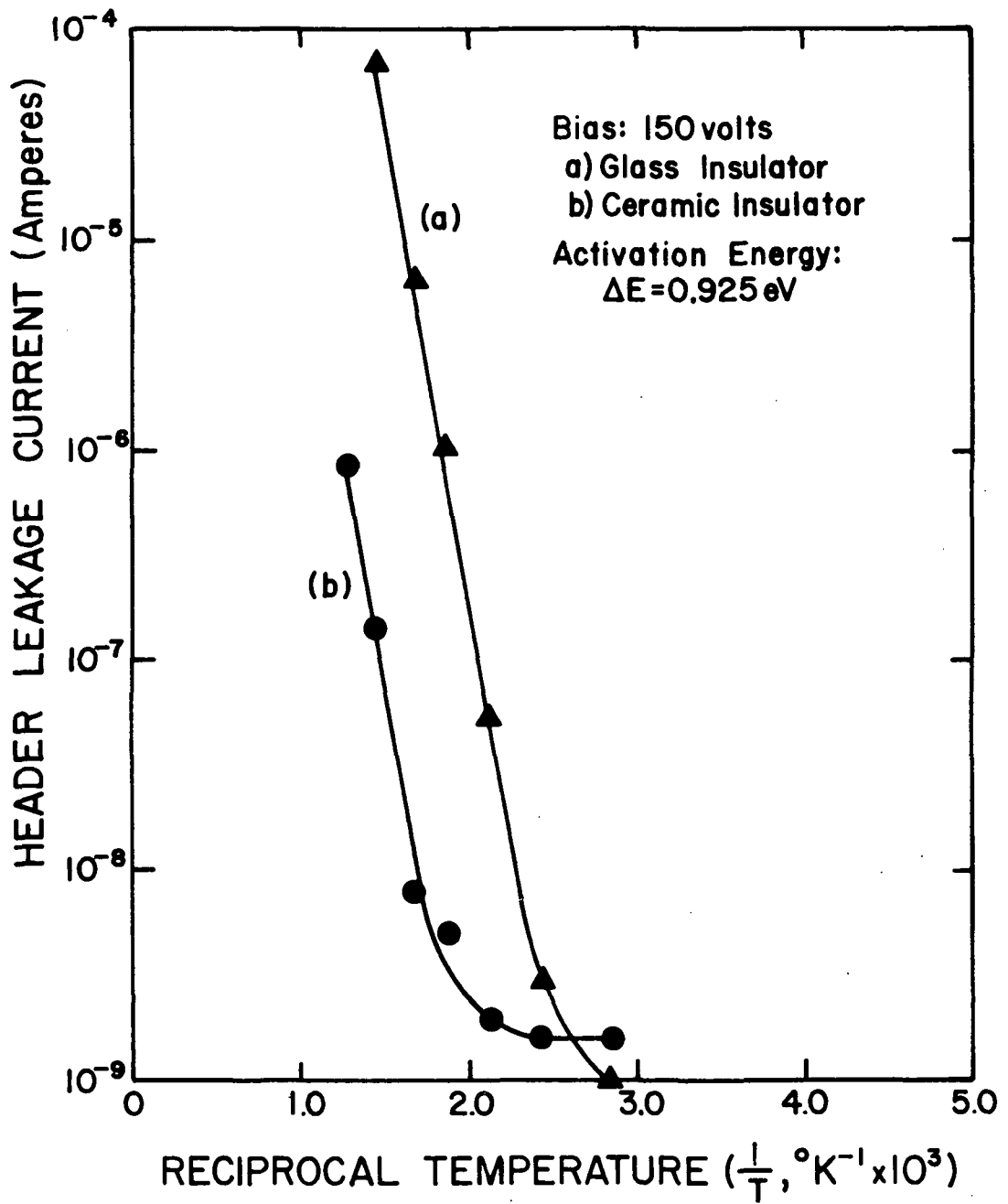


Figure 14. Header Leakage Current versus Reciprocal Temperature Measured at a Bias of -150 Volts for Headers with (a) Glass Insulation and (b) Ceramic Insulation

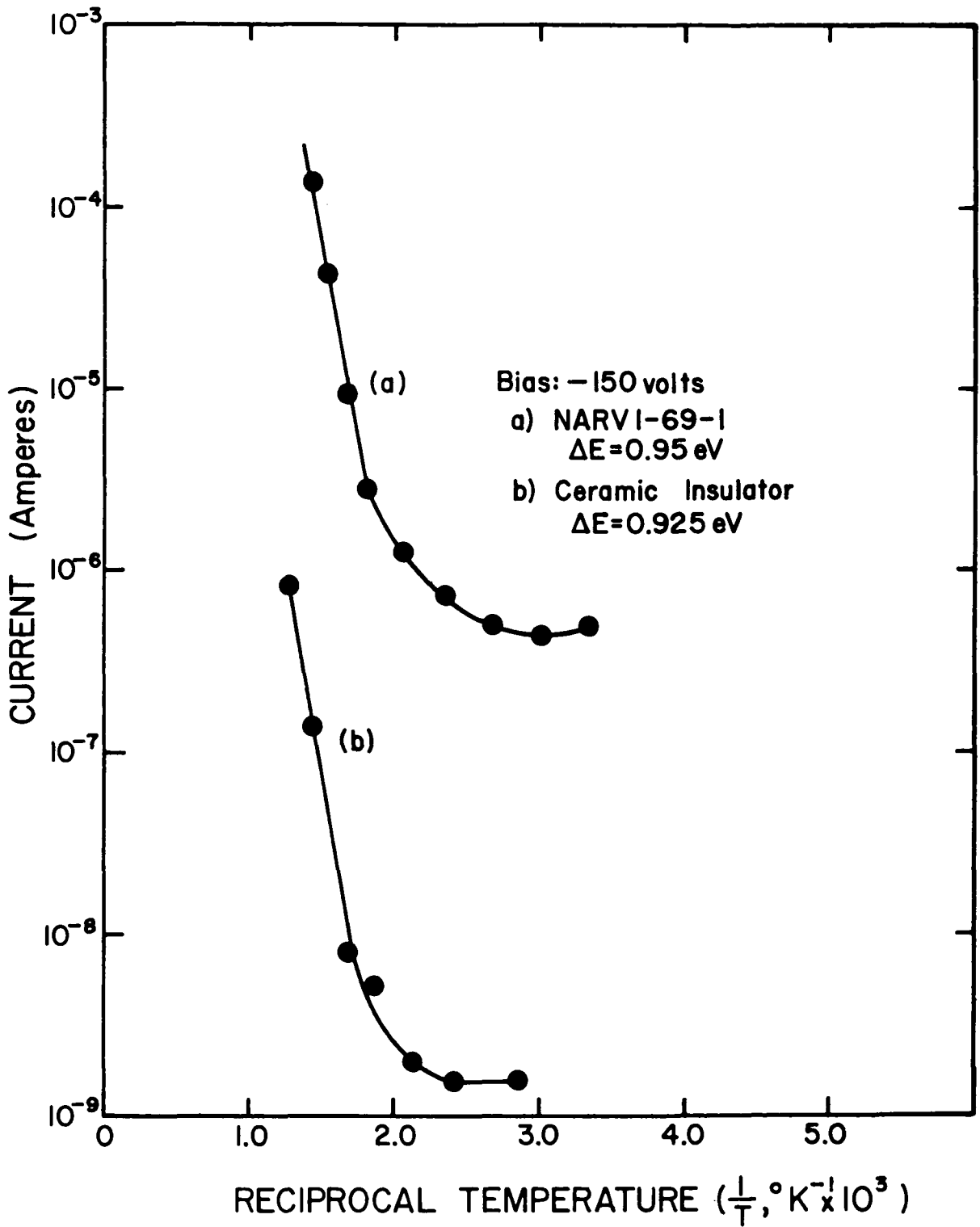


Figure 15. Rectifier Reverse Current, Curve (a), versus Reciprocal Temperature for a Standard Rectifier Fabricated on a Header Using Ceramic Insulation. Header Leakage Current Shown in Curve (b).

Effect of Thermal Cycling and Heat Treatment on Current-Voltage Characteristics

The variation of rectifier forward voltage at a current of 1.0 ampere at room temperature and 400°C during the required three thermal cycles for various samples is shown in Figures 16 and 17. Routinely, rectifier parameters were measured at room temperature prior to installation in the controlled temperature furnace. After installation, parameters were remeasured to insure proper installation. The furnace was then brought to equilibrium at 400°C and held there for 1 hour. At the end of the one hour interval, the furnace was allowed to cool to room temperature. Rectifier parameters were measured both at the beginning and at the end of the one hour, 400°C, heat treatment in order to determine if any changes in device performance occurred during the high temperature portion of the cycle. As can be seen in Figure 16, some increases in forward voltage did occur during the first and second 400°C heat treatment. This increase is apparently due to initial degradation of one or both of the device ohmic contacts. However, in most cases, the increase was small and did not cause the devices to exceed the program specification. Furthermore, stability in the forward voltage parameter at 400°C was usually achieved by the end of the first heat treatment.

In most cases, an increase in temperature resulted in a reduction in forward voltage at 1.0 ampere forward current as shown in Figure 16. Some of the devices tested, however, exhibited an increase in forward voltage with temperature as can be seen in Figure 17. The excessive increase in forward voltage of device No. 3 in Figure 17 is considered to be due to degradation of the ohmic contacts since during the final cycle, no additional changes were observed. Samples No. 1 and No. 2 exhibited more stable variations of forward voltage which were opposite in nature to those shown in Figure 16. It must be kept in mind that at a forward current of 1.0 ampere, the device forward voltage is a function of both the bandgap energy and the bulk resistivity of the n and p regions. Results presented in pages 35-39 confirm the fact that the device forward voltage at low currents behaves properly with respect to the bandgap energy as a function of temperature. Therefore it is quite likely that the variation in the difference between the room temperature and 400°C values of forward voltage at 1.0 ampere are due primarily to the temperature dependence of bulk resistivity for the various wafers.

It is interesting to note that there is a close correlation between the variations in forward voltage with temperature and the respective wafers used. For example, devices made from wafers NARV1-69-1 and NARV1-69-2 (separate wafers grown during the same run) show a definite similarity which is distinguishable from the behavior of devices made from wafers NARV1-70-1 and NARV1-70-2.

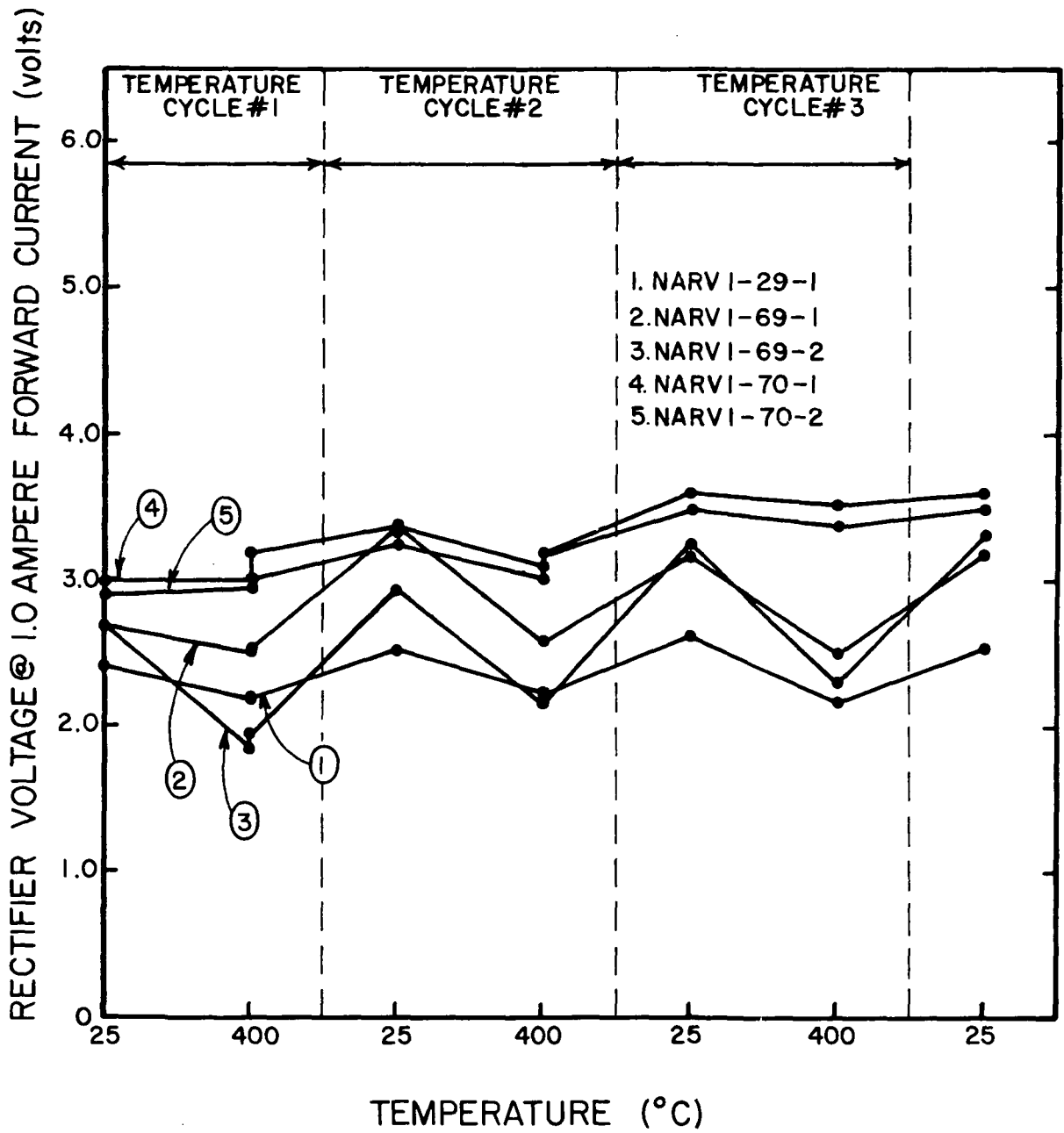


Figure 16. Rectifier Forward Voltage Measured at 1.0 Ampere Forward Current at 27 and 400°C During the Required Three Temperature Cycles. Devices Exhibit Expected Temperature Dependence.

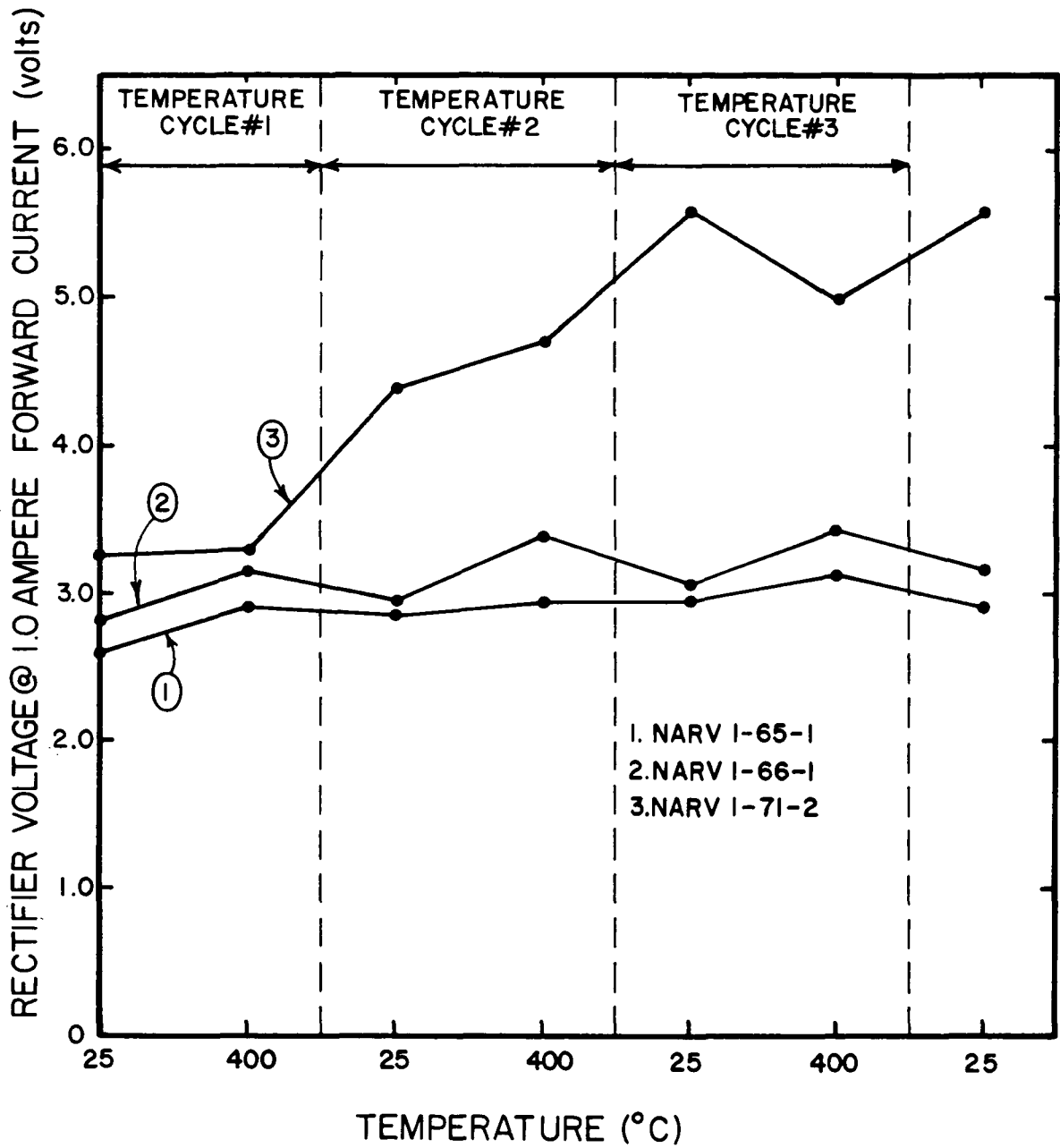


Figure 17. Rectifier Forward Voltage Measured at 1.0 Ampere Forward Current at 27 and 400°C During the Required Three Temperature Cycles. Devices Exhibit Anomalous Temperature Dependence.

The variation in the reverse saturation current with temperature for successive thermal cycles was negligible as seen in Figure 13. This is due primarily to the fact that for large values of reverse bias and low values of device current, small changes in the contact resistivities and bulk resistances caused by changes in carrier mobility cause negligible changes in the total device voltage.

Temperature Dependence of Rectifier Forward Bias Current-Voltage Characteristics

In order to separate the effects of decreasing bandgap energy and increasing bulk resistivity with increasing temperature on device forward bias current-voltage characteristics, it was necessary to monitor the device forward voltage at low currents as a function of temperature in addition to the high current values presented in the previous section.

The current-voltage-temperature dependence of an ideal diode is given by the well known Shockley equation (see, for example, Ref. 15)

$$J = J_s [\exp (qV/kT) - 1]$$

where

$$J_s = \frac{qD_p P_{n0}}{L_p} + \frac{qD_n N_{p0}}{L_n}$$

which reduces to

$$J = \frac{qD_p P_{n0}}{L_p} [\exp (qV/kT) - 1]$$

for p⁺/n abrupt junctions which is the case at hand. Since

$$L \equiv \sqrt{D_p \tau_p}$$

and for most cases

$$D_p / \tau_p \propto T^\gamma,$$

where γ is a constant, J_s can be expressed as

$$J_s \approx \frac{qD_p P_{n0}}{L_p} \approx \frac{D_p n_i^2}{\tau_p N_D}$$

$$\sim [T^3 \exp (-E_g/kT)] T^{\gamma/2} = T^{(3 + \gamma/2)} \exp (-E_g/kT).$$

Since the $T^{(3 + \gamma/2)}$ term is insignificant in comparison to the exponential term, the forward current J , will increase approximately as

$$\exp [- (E_g - qV) / kT].$$

Thus for a constant value of current, the forward voltage, V , should be related to temperature T and $E_g(T)$ by the simple expression

$$V = E_g/q - \frac{kT}{q} \times (\text{const.})$$

The bandgap of GaP may be determined from the empirical equation

$$\frac{E_g}{q} = 2.338 - 6.2 \times 10^{-4} T^2 / (T + 460). \quad (16)$$

Therefore,

$$V = 2.338 - 6.2 \times 10^{-4} T^2 / (T + 460) - T \times (\text{const.}).$$

The comparison between the above equation and experimental results for a nitrogen doped (NARV1-29-2) and a non-nitrogen doped sample (GP4-30-1) are shown in Figure 18. The data representing sample NARV1-29-1 were taken on a standard 10^{-2}cm^2 rectifier at a forward current of $20 \mu\text{A}$. The data representing the non-nitrogen doped sample GP4-80-1 were taken on a 10^{-3}cm^2 device assembled in a manner similar to standard high temperature devices and operated at a forward current of $10 \mu\text{A}$. As can be seen, satisfactory agreement of theory and experiment was obtained for both samples indicating that at low currents, these devices are properly behaved and void of the anomalous forward bias behavior at increased temperatures as was experienced in earlier work.⁽¹⁷⁾ The small amount of scatter which is evident is considered to be due to experimental error in determination of junction temperature.

A somewhat more graphic illustration of the temperature dependence of the entire forward bias current-voltage characteristic is shown in Figure 19. In order to compare the device performance at low, medium, and high currents, multiple exposures of the device I-V trace at each temperature were made at current sensitivities of a) $10 \mu\text{A}$, b) 1mA , and c) 100mA/div . As might be anticipated, the shift to lower voltage of the (a)-trace with increasing temperature is consistent with the data shown in Figure 18. The (b)-trace exhibits a similarity in behavior with temperature to that of the (a)-trace but also shows some reduction in slope due to increasing bulk resistivity. The variation in the (c)-trace is dominated by the doubling in bulk resistivity as evidenced by the factor of two decrease in slope when going from 27 to 400°C . Thus, based on the data presented in Figures 18 and 19, it is safe to conclude that the forward bias characteristics of these devices behave properly with temperature and that the variation in device voltage at maximum current with temperature is dominated by the temperature variation of the device bulk resistivity.

In order to identify the predominant mechanism responsible for forward current in these devices, the logarithm of forward current was plotted

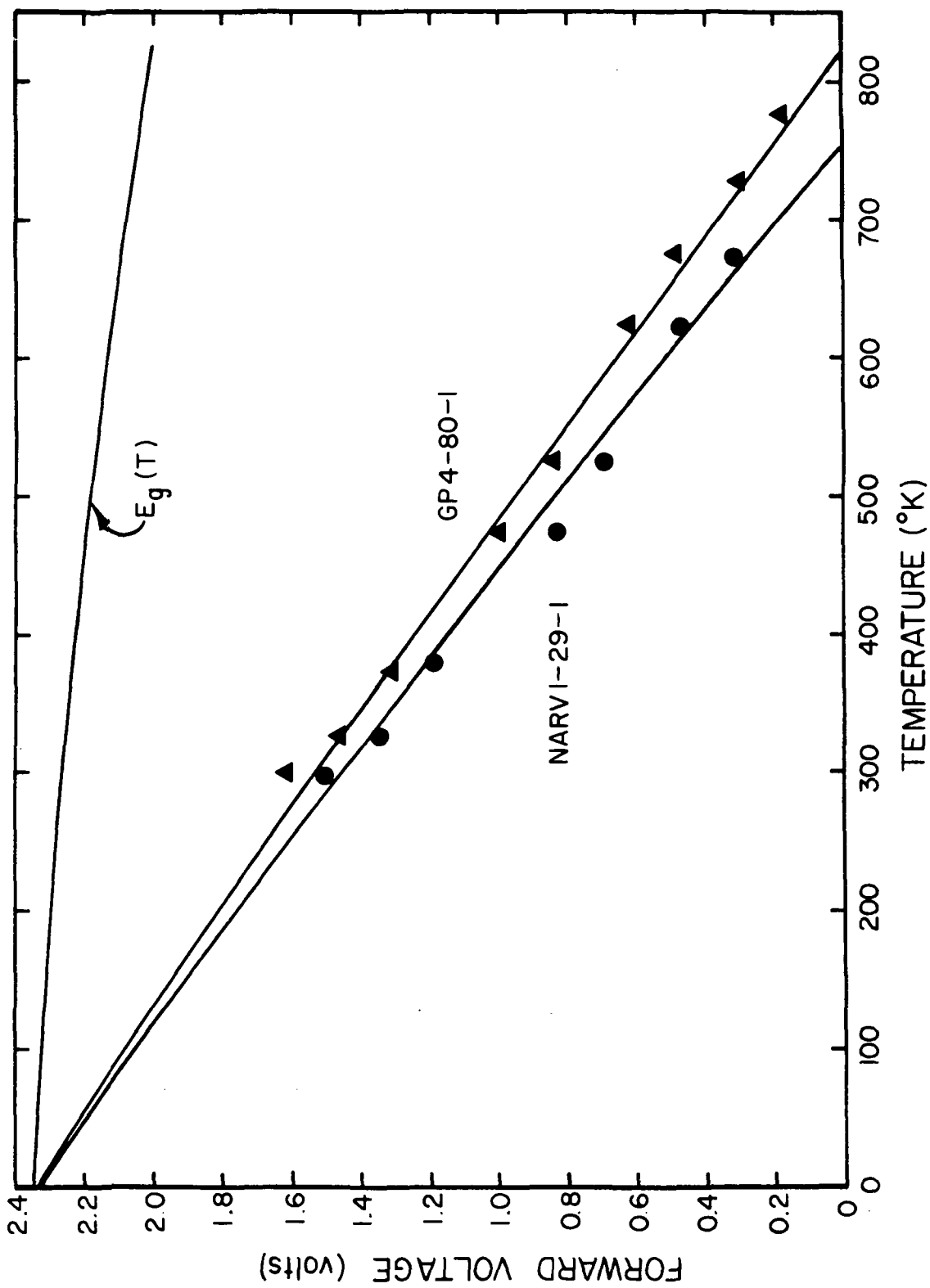


Figure 18. Rectifier Forward Voltage Measured at a Constant Low Forward Current versus Temperature for a Nitrogen Doped (NARV1-29-1) and Nitrogen Free (GP4-80-1) Sample. The GaP Band Gap Energy, $E_g(T)$, in Electron Volts, is also Shown.

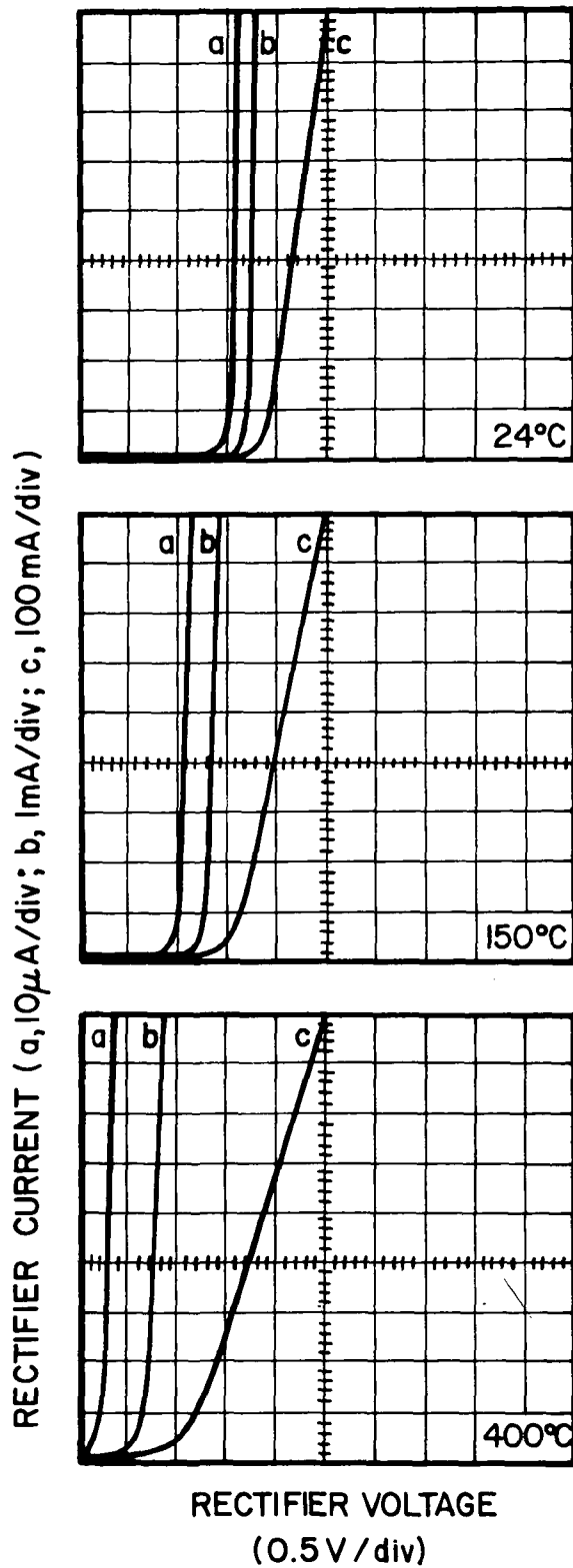


Figure 19. Rectifier Forward Bias Current-Voltage Characteristics at Temperatures of 24, 150 and 400°C

versus voltage for currents ranging from 10^{-9} to 1.0 amperes as shown in Figure 20. In general the forward current follows the empirical expression

$$J_1 = \approx \exp (gV/nkT)^{(15)}$$

where $n = 2$ when space charge recombination dominates and $n = 1$ when diffusion current dominates. As seen in Figure 20, the plot of data representing sample NARV1-29-1, at room temperature, exhibits distinct regions where the two mechanisms act independently. That is, for currents in the range of from 10^{-9} to 10^{-4} amperes, junction current occurs primarily by space charge recombination. For currents in the range of from 10^{-4} to 10^{-2} amperes, current transport proceeds mainly via diffusion. Above 10^{-2} amperes, high injection effects and device series resistance cause the curve to become grossly nonlinear. Rectifiers fabricated from wafer NARV1-69-1 exhibit I-V characteristics and current transport mechanisms for various currents which agree well with those obtained for wafer NARV1-29-2 except for considerable excess current observed for current values less than 5×10^{-7} amperes. The mechanism responsible for this excess current has not been identified.

At 400°C , current transport proceeds via a combination of diffusion and space charge recombination currents resulting in a value of n between 1 and 2 for currents in the range of from $\approx 5 \times 10^{-7}$ to 10^{-2} amperes.

Rectifier Reverse Breakdown Voltage vs. N_D

The reverse breakdown voltage, V_{RB} , as a function of carrier concentration is shown in Figure 21. The solid circles show the average breakdown observed for a sample, and the vertical line indicates the range of breakdown voltages observed. The data shown in Figure 21 were taken on samples which had an area of 10^{-3} cm^2 , and not full size 10^{-2} cm^2 rectifier devices. A minimum of 15 devices are fabricated for each wafer (data point) shown.

It can be seen that there is a great deal of scatter in the data for these devices, and that V_{RB} does not change appreciably as a function of carrier concentration. For all but two samples V_{RB} remains well below the theoretical curve calculated by Sze and Gibbons.⁽¹⁾ The behavior of these lightly doped samples can be contrasted with the more heavily doped samples shown in Figure 2. For samples with $N_D > 10^{16}/\text{cm}^2$ the reverse breakdown voltage generally follows, and often exceeds, the Sze and Gibbons curve. These data confirm that fact that the reverse breakdown voltage in the devices studied here is determined by breakdown at localized point defects within the crystal. This breakdown can be visually observed under a microscope when the devices are biased into avalanche.

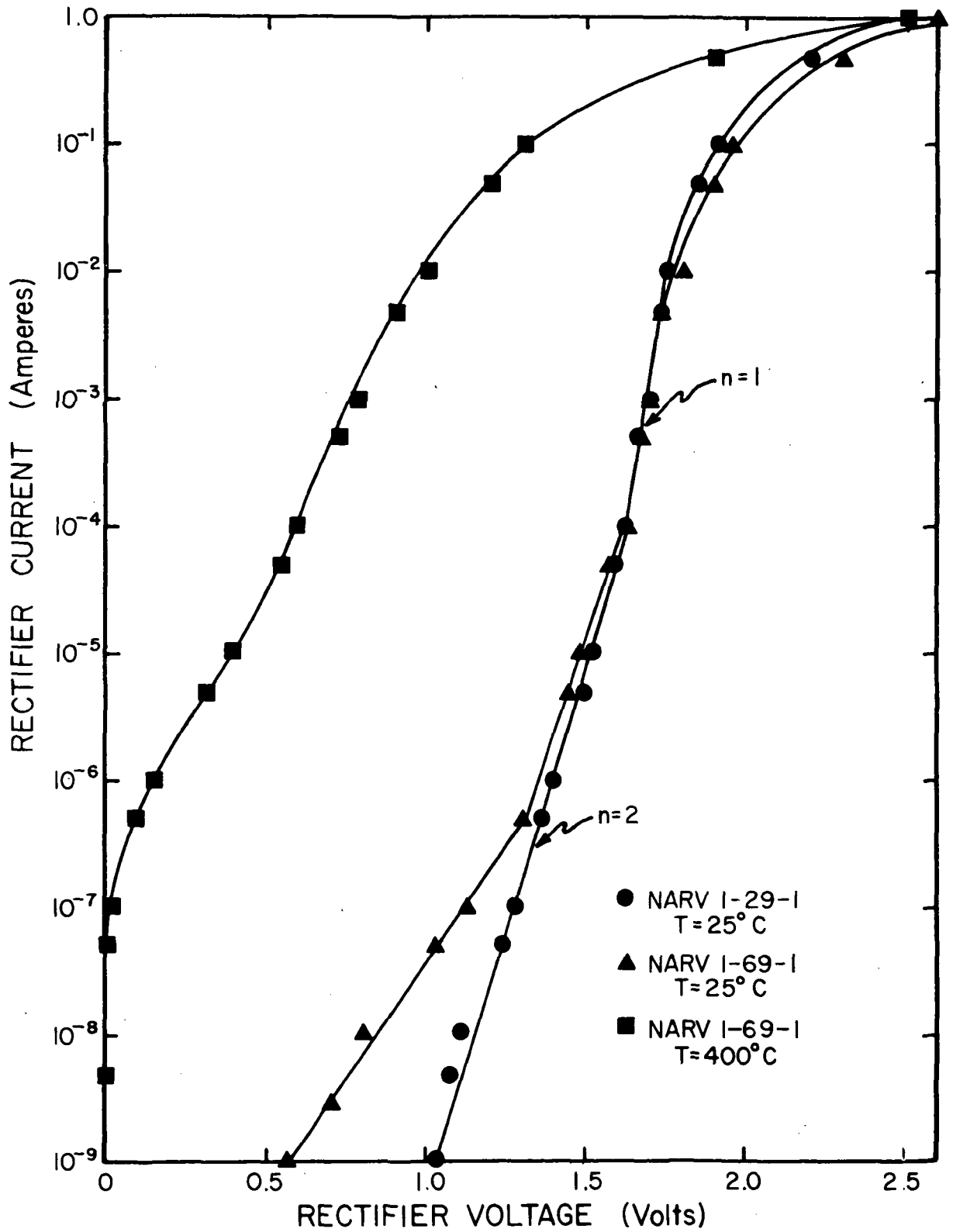


Figure 20. Logarithm of Rectifier Current versus Voltage at 25 and 400°C

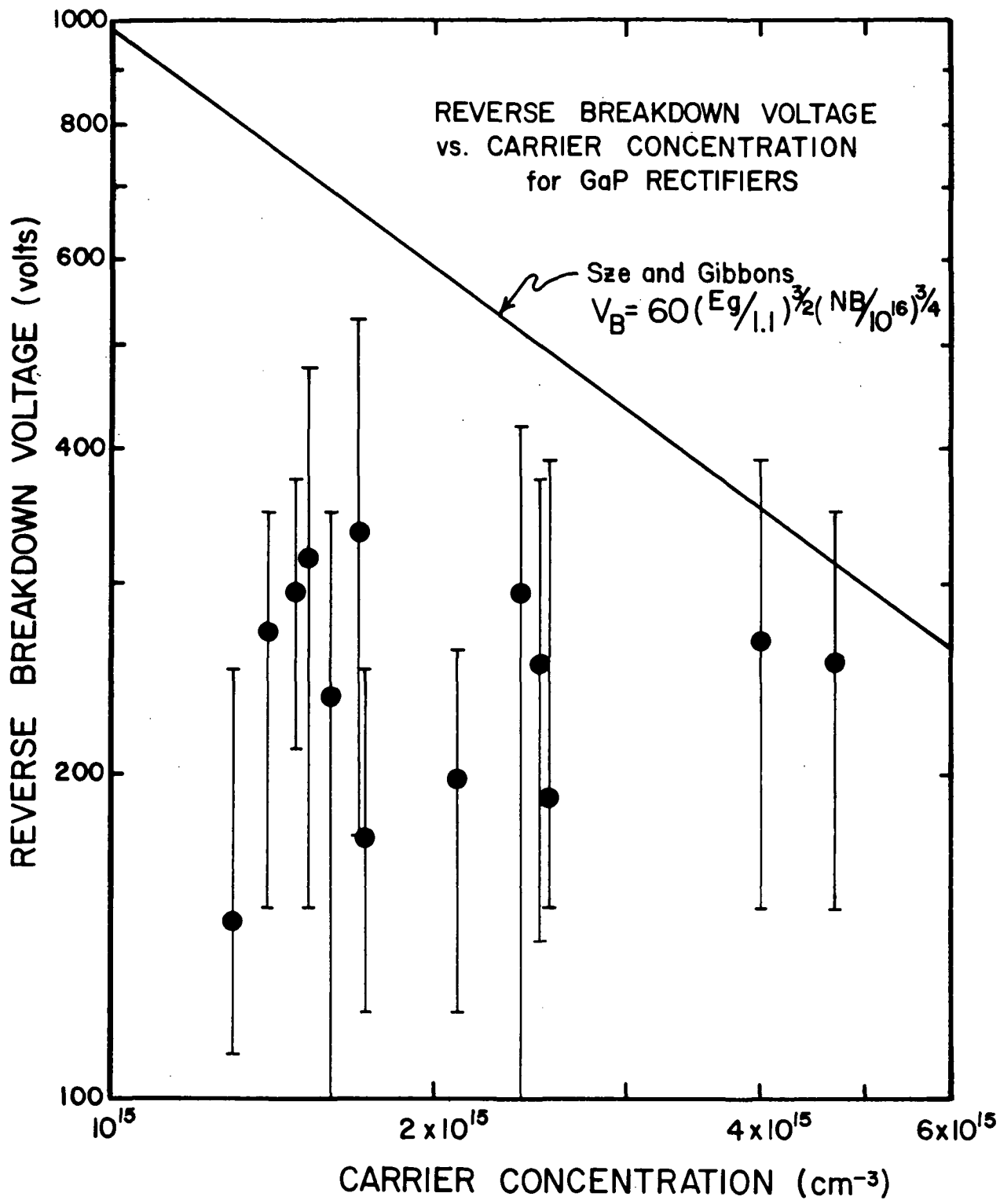


Figure 21. Reverse Breakdown Voltage versus Carrier Concentration for Lightly Doped GaP Rectifiers

The nature of the point defect is, in many cases, related to the substrate. The three samples (NARV1-59-1, 1-65-3 and 1-66-3) with the lowest maximum breakdown voltages shown in Figure 21 (all three have maximum breakdowns of ≈ 250 volts) were grown on substrates taken from the same boule. The boule was Te doped and, on the end of the boule from which the substrates for these samples were taken, had a very high carrier concentration $6 \times 10^{18}/\text{cm}^3$ which might be expected to lead to structural disorder. However, a sample grown from the other end of the boule, NARV1-59-2, which was doped to only $1 \times 10^{18}/\text{cm}^3$ also had a very low breakdown (150 volts maximum). This sample is not shown in Figure 21 since the carrier concentration in the epitaxial layer is only $6 \times 10^{14}/\text{cm}^3$. These data suggest that the whole GaP boule yields poor results. Since this boule was Te doped these data suggest that Te doping might be less suitable than S doping for use as substrates for high voltage devices. However, since this was the only Te doped boule used during the course of this program, these results should under no circumstances be regarded as conclusive. The inferior performance of this boule may also have been related to structural defects or to some other unintentional impurity.

Capacitance Measurements

Capacitance and capacitance-voltage measurements were performed on finished rectifiers in order to obtain information concerning the carrier concentration and the Zn diffusion profile in the epitaxial layer in the region of the p-n junction. The capacitance voltage measurements indicated that the diffusion cycle used yielded abrupt junctions. The value of n in the standard expression

$$C = C_0 \left[\frac{V_0}{V_0 + V_a} \right]^{1/n}$$

(where C_0 is the capacitance at zero bias, V_0 is the built in voltage, and V_a is the externally applied voltage) was typically 2.0 with a built in voltage, V_0 , of ≈ 2 volts which is indicative of an abrupt junction.

A plot of $1/C^2$ versus voltage for a typical rectifier is shown in Figure 22. As seen in the figure, the data result in an essentially linear dependence between $1/C^2$ and V with a horizontal axis intercept of 2.0 volts, the built in voltage. Since the carrier density, N_D , is related to device capacitance and voltage by the standard expression

$$N_D = \frac{-2 \Delta V}{q \epsilon A^2 \Delta (1/C^2)} \quad (15)$$

the carrier density in the epitaxial layer of wafer NARV1-69-1 can be determined from the data in Figure 22 to be $N = 2 \times 10^{15} \text{ cm}^{-3}$. The depletion region width of the device represented in Figure 22 at a reverse

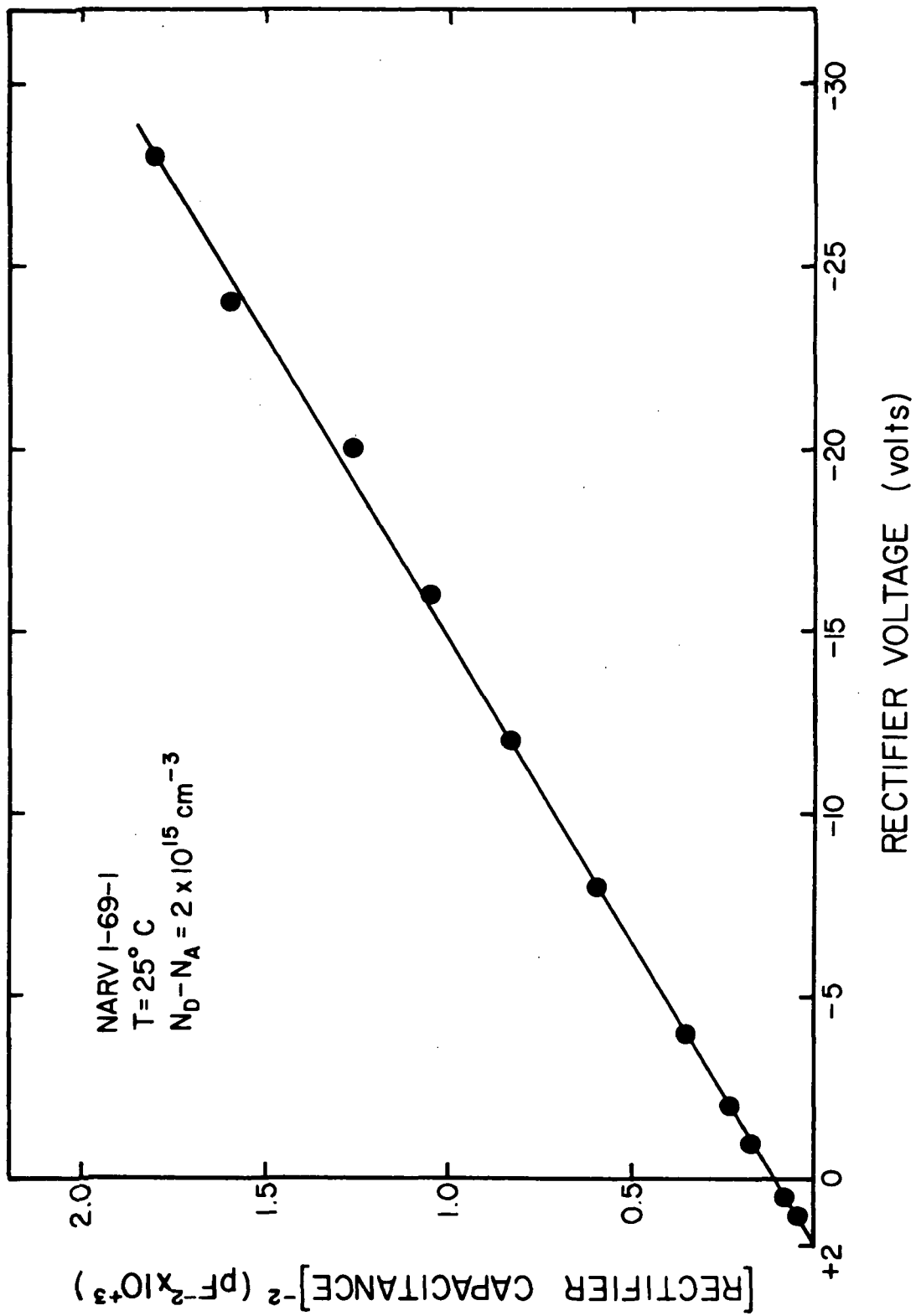


Figure 22. [Rectifier Capacitance]⁻² versus Voltage Obtained with a Standard GaP High Temperature Rectifier

bias of 30 volts is $\approx 4 \mu\text{m}$ as determined by the expression

$$X_D = \frac{\epsilon A}{C} .$$

Thus since the junction depth in these devices is ≈ 5.0 to $5.5 \mu\text{m}$, the impurity profile exhibits good uniformity in the region from ≈ 5 to $10 \mu\text{m}$ below the surface of the epitaxial layer.

The zero bias junction capacitance of the rectifiers fabricated in this program was typically in the range of from 70 to 100 pF which is consistent with a donor concentration of from ≈ 1 to $2.5 \times 10^{15} \text{cm}^{-3}$ for an abrupt junction device.

The capacitance per unit area as a function of carrier concentration is shown in Figure 23. The solid line in Figure 23 is the theoretical curve for an abrupt junction at zero bias, obtained using the equation

$$C/A \approx \left[\frac{e\epsilon N_D}{2V_0} \right]^{1/2}$$

where e is the electronic charge, ϵ is the dielectric constant, N_D is the carrier concentration and V_0 is the built in voltage. Using $\epsilon = 11.1$ and $V_0 = 2.0$ as obtained from Figure 21 we find that $C/A = [N_D/2.54 \times 10^{13}]^{1/2}$

It is apparent in Figure 23 that, although the capacitance values are in rough agreement with the theoretical curve, there is a great deal of scatter in the data. This scatter may be due in part to inaccuracies in the determination of carrier concentrations. As described earlier in this report, the carrier concentrations are measured on test samples which are placed adjacent to the actual wafer in the epitaxial reactor. Since relatively small research scale reactors were used for this work there is some variation in carrier concentration expected from sample to sample which in part accounts for the observed scatter.

Diode Response Times

As mentioned previously in pages 24-25, rectifier switching speeds were characterized by measuring the device radiative decay time constant, T_R . Actual maximum recovery times may be determined by multiplying T_R by a factor of 2.2. For exponential processes, the 10 - 90% switching time is directly related to the exponential time constant by the factor of 2.2. It should be noted that the radiative decay time constant is measured during a period of zero device terminal current. If for example a reversing current pulse is applied during the measurement period, the measured value of T_R decreases due to the removal of excess injected carriers across the junction.

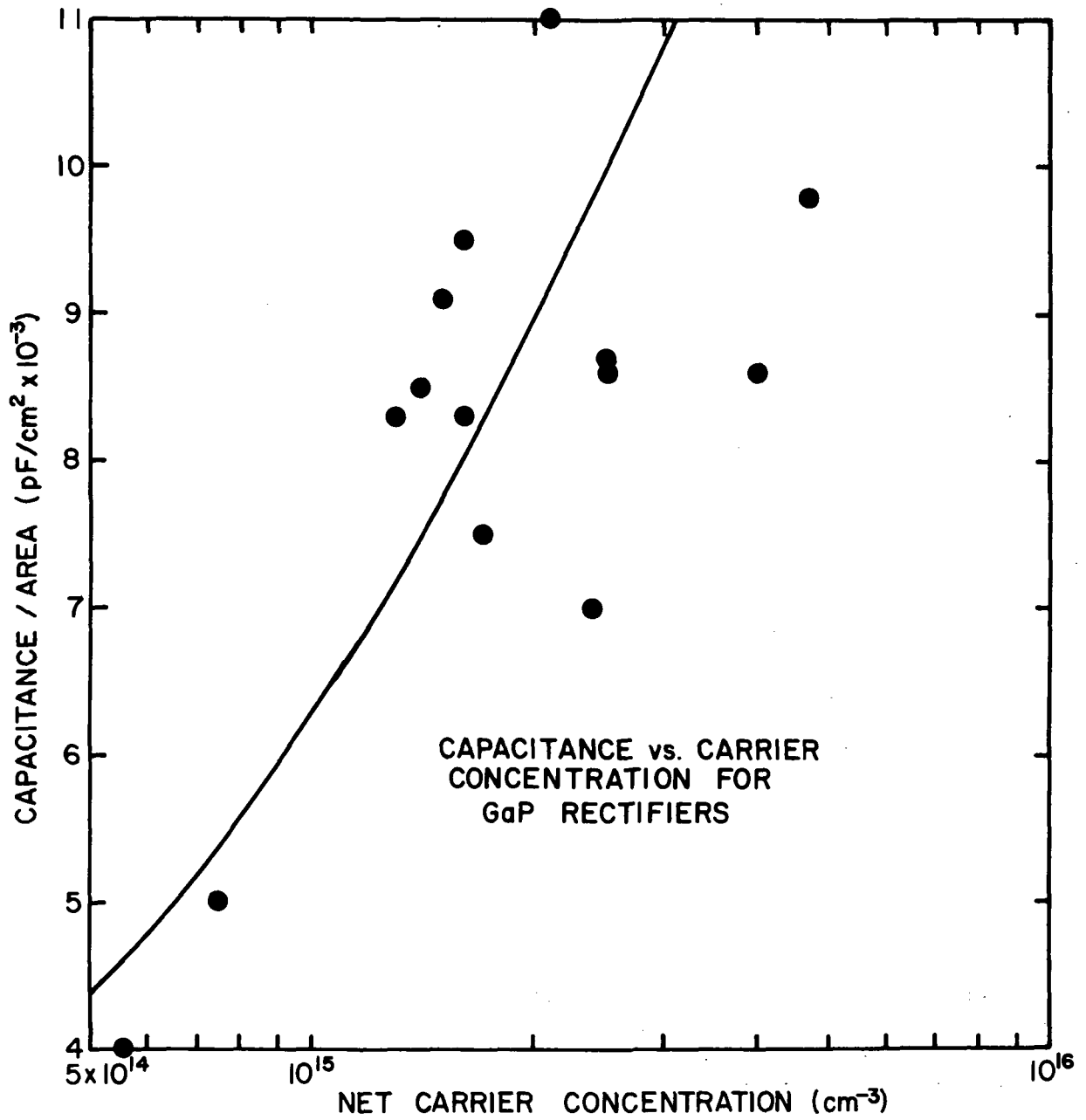


Figure 23. Capacitance versus Carrier Concentration for High Purity GaP High Temperature Rectifiers

The results of these measurements are presented in Table IV. As can be seen, the majority of the value of T_R are in the range of from 70 to 100 nsec which are typical for nitrogen doped GaP.

Table IV
GaP Rectifier
Radiative Decay Time Constant

Sample	Radiative Decay Time Constant (n sec)
NARV1-65-1	99
NARV1-66-1	76.5
NARV1-69-1	103
NARV1-69-2	96.5
NARV1-70-1	74.8
NARV1-70-2	96.0
NARV1-71-2	37.7

SUGGESTED FUTURE PROGRAMS

During this program a great deal of progress has been made toward the development of high temperature GaP devices. However, there remain several problems areas which should be investigated if reliable and reproducible GaP high-temperature devices are to become a reality.

Foremost among these problem areas is the improvement in the quality and reproducibility of the GaP material. Although the full size device yield for many of the wafers was in excess of 50%, the wafers still had a relatively high number of point defects. This is evidenced by the fact that, in the vast majority of the devices studied, the breakdown occurred at point defects rather than by uniform avalanche multiplication. In order to obtain

larger area rectifiers with higher breakdown voltages it will be necessary to determine the nature of the point defects and reduce their concentration.

In order to obtain rectifiers with reproducible reverse breakdown voltages it will be necessary to accurately control the background carrier concentration for net concentrations of $10^{15}/\text{cm}^3$. This will become possible only when the mechanism by which nitrogen reduces the carrier concentration is fully understood, or when the carrier concentration can be controlled in the $10^{15}/\text{cm}^3$ range without the addition of nitrogen. Over the past few years there has been a steady improvement in the quality of the starting materials and substrates which has contributed to the growth of improved epitaxial layers. This must continue if the full capability of GaP is to be realized.

The initiation of a program to develop a high power GaP rectifier, for example, a 10 Amp rectifier with a device area of $\approx 0.1 \text{ cm}^2$ and a reverse breakdown voltage of 400 volts would spur the development of improved GaP epitaxial films and carry GaP technology a major step forward.

A second program which would further hasten the evolution of GaP technology, is the development of GaP active devices such as transistors and controlled rectifiers. Within the past few months GaP p-n-p-n switches and controlled rectifiers have been fabricated in the Monsanto Company laboratories and operated to temperatures in excess of 500°C . Thus the feasibility of such devices has been demonstrated although a great deal of work remains before devices can be reproducibly fabricated to a given set of specifications.

If current programs, for the development of large area high power rectifiers and low power active devices, were carried out, the fabrication of high temperature GaP integrated circuitry could become a reality in the near future.

SAMPLES SUPPLIED TO NASA

At the conclusion of this program ten hermetically sealed rectifiers were supplied to NASA. Prior to delivery, these devices had been fully tested including three temperature cycles from room temperature to 400°C , with a total time of at least three hours at 400°C .

The final room temperature and 400°C device specifications are tabulated in Table V. The reverse breakdown voltages for these devices are not shown, but in all cases the breakdown is well in excess of the required

150 volts and may be greater than 400 volts. The reverse breakdown voltage was not measured on these devices because in many cases devices were destroyed when biased into avalanche.

Table V

Device Characteristics for Sample Rectifiers Supplied to NASA

<u>Diode No.</u>	<u>Wafer No.</u>	<u>V_f at 1 amp (25°C)</u>	<u>I_R at -150V (25°C)</u>	<u>V_f at 1 amp (400°C)</u>	<u>I_R at -150 V (400°C)</u>
1	NARV 1-66-1	3.35	< 1 μ A	3.5	150 μ A
2	1-66-1	3.75	< 1 μ A	3.6	250 μ A
3	1-66-1	3.9	< 1 μ A	3.9	110 μ A
4	1-65-1	3.35	< 1 μ A	2.5	220 μ A
5	1-65-1	3.0	< 1 μ A	3.2	270 μ A
6	1-65-1	3.6	< 1 μ A	2.75	74 μ A
7	1-29-1	2.8	< 1 μ A	2.2	56 μ A
8	1-29-1	2.75	< 1 μ A	2.2	32 μ A
9	1-29-1	2.8	< 1 μ A	2.0	28 μ A
10	1-29-1	2.75	< 1 μ A	2.4	64 μ A

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