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NPC 275-1

NASA Parts Publication NPC 275-1
August 1966 Edition

OCT 17 1966

(NASA-NPC-275-1) MICROELECTRONIC DEVICE DATA HANDBOOK (Arinc Research Corp., Annapolis, Md.) Aug. 1966 327 p
N72-73275
Unclas
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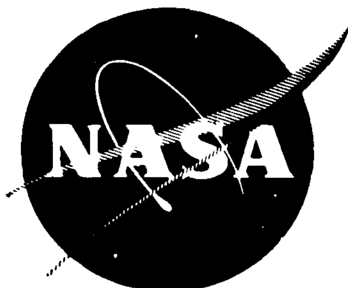
MICROELECTRONIC DEVICE DATA HANDBOOK



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NASA Parts Publication
NPC 275-1

MICROELECTRONIC DEVICE DATA HANDBOOK

August 1966

National Aeronautics and Space Administration

ARINC RESEARCH CORPORATION
a subsidiary of Aeronautical Radio Corporation
2551 Riva Road
Annapolis, Maryland 21401

Publication 514-01-1-655

FOREWORD

This is the second edition of the Microelectronic Device Data Handbook, prepared under National Aeronautics and Space Administration Contract NASW 1250. It supersedes the first edition, NASA Parts Publication NPC 275-1, published in March 1964.

The first six chapters of this handbook contain general information on reliability, manufacturing processes, packaging, specifications, design, and testing. The last chapter presents detailed data on manufacturers and on the performance characteristics of integrated circuits available from stock.

Acknowledgement is made of the excellent cooperation of microelectronic-device manufacturers, who responded generously to all requests for information.

A number of publishers kindly permitted the use of their published material in this handbook. Certain sections of Chapter Two are taken almost entirely from previously published papers and articles, as follows:

Section 2.1.10, "Linear Amplifier Checklist," is from D. C. Bailey, "Converting Amplifiers to Integrated Circuit Format," EEE, February 1964, Mactier Publishing Corporation, New York.

Table 2-5, "Blackbox Checklist," is from D. C. Bailey, "Blackboxing Your Linear Integrated Circuit," Electronic Design, 22 June 1964, Hayden Publishing Company, Inc., New York, New York.

Section 2.1.11.6, "Digital Circuit," is from L. B. Valdes, "Case History: Integrating a NOR Circuit," Electronic Design, 2 March 1964, Hayden Publishing Company, Inc., New York, New York.

Sections 2.2.5, "Drain Current," 2.2.6, "Pinch-off," and 2.2.13, "Switching Times," are from C. T. Sah, "Characteristics of the Metal-Oxide Semiconductor Transistors," Transactions of the IEEE, July 1964, Institute of Electrical and Electronics Engineers, New York, New York.

Section 2.2.10, "Equivalent Circuit of the MOS," is from D. M. Griswold, "Understanding and Using the MOSFET," Electronics, 4 October 1964, McGraw-Hill, Inc., New York, New York.

Section 2.2.15, "MOS Digital Circuits," is from R. D. Lohman, "Application of MOS FET's in Microelectronics," Semiconductor Products and Solid State Technology, March 1966, Cowan Publishing Corporation, Port Washington, New York.

The Defense Systems Division, UNIVAC Division of Sperry Rand Corporation provided all of the photographs and much of the text of Chapter Six.

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INTRODUCTION

ONE

This handbook is intended as a quick-reference document for use by NASA design engineers, technicians, and parts specialists, and by NASA's contractors. The text material in the handbook is addressed to those with little or no experience in microelectronics. It is intended to provide general guidance for employing the technology. Solutions to the specific problems of equipment design engineers must be considered in the context of the cost, schedule, environmental, and other constraints of a particular application and are therefore beyond the scope of this handbook. The handbook does provide general information that will be of substantial assistance in the solution of specific problems.

The balance of this introduction is a summary of the microelectronics technology; its purpose is to provide the general reader, particularly management personnel, with a capsule sketch of the problems, advantages, and limitations of the technology.

1.1 Physical Description of Microelectronic Devices

The physical characteristics of microelectronic devices are striking, but it must be kept in mind that equipments utilizing them cannot yet take full advantage of these characteristics. For example, a typical integrated circuit comprising four transistors, six diodes, and ten resistors can be produced in a silicon chip with a volume of 0.00007 cubic inch. However, present device packaging techniques will increase the volume to at least 0.001 cubic inch, exclusive of leads. Assembling the integrated circuit into an equipment requires

further volume, so that the system may average 0.01 cubic inch per package. This is still quite small, of course, in comparison with a conventional transistorized circuit of approximately 1/2-cubic-inch.

The volume of thin-film and multichip circuits is usually greater than that of the integrated circuit. The multichip circuits are usually put into a modified TO-5 transistor case with a volume of approximately 0.016 cubic inch, excluding leads. Typical thin-film circuits range from this same volume upward to about 0.1 cubic inch, the larger volumes usually being used for the more difficult linear circuitry. The microelectronic circuits, then, occupy a volume 1/5 to 1/50 that of conventional circuits when assembled into equipments.

The weight of the smallest integrated-circuit package in general use is approximately 0.1 gram (0.00022 pounds). Again, the assembled equipment averages a much higher weight -- an estimated 1 gram per unit -- than is obtained by adding the weights of the integrated-circuit packages. As with volume, the weight of multichip and thin-film microcircuits is greater than that of the integrated circuit, and microelectronic circuits weigh 1/5 to 1/50 as much as conventional circuits when connected into equipments.

The estimates given above are quite rough and are valid only for comparisons at the circuit level. A given equipment's volume or weight may be changed drastically or only slightly with microelectronics conversion, depending mainly on the weight and volume of the parts that are not converted. Further, there is a strong trend to increase the functional complexity of the integrated circuit; increased complexity can often be achieved without materially increasing overall package weight or volume. The present practical limit to integrated-circuit complexity is approximately 100 elements per substrate. This amounts to a threefold increase over the past three years. Newer substrates can be placed in the same package used for the less complex earlier substrates. Additional increases in integrated-circuit packaging efficiency can be expected.

A brief discussion of integrated-circuit power consumption is appropriate here. It is often mistakenly believed that an integrated circuit consumes much less power than an equivalent conventional circuit. While microelectronic equipments are often designed to consume considerably less power than the conventional version, this reduction cannot be attributed to an inherent power efficiency in the individual microelectronic circuits. Any power-speed combination available today in a microelectronic circuit can also be achieved with conventional components. The sharp reductions in power that often accompany conversion of an equipment to microelectronic form are due to changes in design: Many conventional equipments were designed without severe power restrictions; thus there is considerable room for reduction.

There is a reduction in lead lengths and mechanical joints in the integrated circuit, and a corresponding reduction in power loss. This power difference is negligible in most cases at present, but as the power levels continue to decrease, it will become more significant. If "nanowatt" circuits become available, the microelectronic circuit will indeed be significantly more efficient than conventional circuitry.

1.2 Performance Characteristics

The integrated-circuit technology has concentrated on digital circuitry because such circuitry does not require passive elements with tight tolerances and broad ranges of values in integrated-circuit form, and because there is usually a high degree of repetition of the same circuit in each digital equipment. All digital functions required in modern systems are currently available in integrated-circuit form.

More than 1300 items are available off-the-shelf from inventory, although many of these circuits overlap in function. This is not to say, however, that such circuits are interchangeable; most of the major manufacturers have developed their own compatible circuit family to provide most of the required digital functions. Mixing items from different families is generally not feasible; thus, in working from the standard inventory, a designer must initially choose the logic scheme and characteristics that best suit his needs and then design his system around a single family of circuits.

Special requirements, not covered by the stock packages, can be met by custom-connecting (metalizing) the elements of standard matrix wafers, which are maintained in inventory for this purpose by some manufacturers. To fill even more exacting needs, fully custom circuits can be made by all manufacturers.

Although the monolithic structures are especially appropriate for digital circuitry, some multichip, hybrid, and mixed-monolithic* circuits are used -- generally for the extremes of the operating frequency range.

More than 80% of the off-the-shelf monolithic gate circuits operate in the 2-50-mW range, with the lower-power circuits having longer propagation delay times. Propagation delays for 85% of the stock digital circuits are below 50 nsec, a number of them being less than 5 nsec.

The appropriateness of digital circuitry for the integrated circuit resulted in its receiving almost the full attention of manufacturers for a number of years. While an unsatisfied demand for digital circuits continued, other applications were neglected. Recently, however, the early pioneering nature of the

---

* An integrated circuit with passive elements deposited on top of the passivation layer.

digital market, with the rush to establish positions therein, has leveled off somewhat, allowing effort to be directed into other areas -- notably linear circuits.

Factors that inhibit the penetration of integrated circuitry into the linear-circuit field* include the following:

(1) Low repetition of types in a given equipment

(2) Fewer opportunities to standardize

(3) Size of equipment (there is only a minor opportunity to reduce size because of constraints of front ends, power stages, and power supplies)

(4) Low manufacturing volume, difficult process control

(5) Poor reliability

(6) Meager reliability data

(7) Very high cost

However, significant progress has been made in the application of microelectronics to analog functions.

Factors similar to those which led to the adoption of the digital functions for initial integrated-circuit development resulted in appearance of the differential amplifier as the first major linear function in integrated-circuit form. The reliance of this function on proportionate differences between circuit elements, rather than on absolute values, recommended it for integrated-circuit development. Adjacent regional elements on a silicon wafer exhibit inherent close proportionate tolerances and track exceptionally well with temperature variations. Approximately one-half of all off-the-shelf linear circuits are differential amplifiers, with 3-db bandwidths as high as 40 MHz. Westinghouse reports a gain of 1000 for a 48-KHz differential amplifier, while a gain of 50 is average for various manufacturers' circuits listed for operating frequencies in the megacycle range.

Circuits for performing other linear functions are now becoming available slowly -- some as integrated circuits, some as hybrid blocks. Operational amplifiers, video amplifiers, rf-if amplifiers, pre-amplifiers, servo amplifiers, and a number of miscellaneous and general-purpose amplifiers have been introduced. Bandwidth capabilities run up to 70 MHz, voltage gain figures range from less than 10 to 500, and power gains go as high as 51 db. Servo amplifiers are available from Norden with signal-power outputs of 8 watts.

* Dr. Robert E. Samuelson, Proceedings of the NSIA/AFSC Conference, "Applications of Microelectronic Technology", December 8-9, 1965, Washington, D. C.

The offerings in the linear functions, however, are by no means as complete as those in the digital area. Approximately 100 circuits are available as stock items, as against the 1300 for digital packages. This proportion is heavily out of balance with the potential utilization in the two areas -- partly, of course, because of the later start made on linear functions. However, it must be borne in mind that one of the factors that made the digital system so attractive to manufacturers of integrated circuits was its unitized design based on the repetitious use of a few basic circuit forms. An equivalent advantageous design situation does not exist to any such degree in the linear market, so that there is a constraint against the establishment of a stock inventory and a tendency to rely more on the custom approach.

One method of increasing the degree of repetition of circuits is to employ multifunction circuitry, which involves the use of a single integrated-circuit chip to perform different electronic functions, the specific function required being selected by proper lead arrangement. Although multifunction circuits have been used in digital circuitry (a multiple gate chip that by proper lead arrangements can be made to perform the flip-flop function, for example), little effort has been made to develop multifunction circuits that can be used in linear or both digital and linear applications. Clearly, the degree of repetition of circuits within an equipment is increased if multifunction circuits are available. Significant logistic economies are also possible with such circuitry available. Work now being conducted by the Naval Applied Science Laboratory is expected to result in widespread use of multifunction circuit-design concepts.

The concerted effort now being made to design linear circuits in integrated-circuit form, and the developments in technology to improve element isolation and tolerances, should eventually result in an extensive linear capability.

1.3 Reliability

For military and space applications, the single most important characteristic of the integrated circuit is its extremely high reliability potential. The early prediction of some manufacturers that the reliability of the integrated circuit would approach that of a single transistor produced by the same basic processes appears to be quite accurate.

To verify the soundness of the prediction, it is worthwhile to examine the factors that determine the reliability of silicon planar transistors. A given group of transistors contains two separate populations, one comprising items with serious defects and the other comprising items with minor defects. The items with minor defects have, for all practical purposes, an infinite life; their reliability approaches unity. The items with serious defects have a very short life; their reliability, for practical purposes, is zero. Fortunately,

most serious defects can be detected with visual, environmental, and operating tests. The average reliability of a group of transistors, then, is determined by the frequency and types of defects that have been introduced during manufacture and the adequacy of testing performed to reject defective units.

The integrated circuit is manufactured of the same materials and virtually the same processes as those used for certain transistors. Excluding electrical connections, the integrated circuit is as vulnerable as the transistor to the introduction of defects. The integrated circuit requires more leads than a single transistor, and these additional leads increase the probability of introducing a defect during the lead-attachment operation. Therefore, the reliability of the integrated circuit can only approach that of a transistor -- the exact reliability being determined by how many defects are introduced during the bonding operation and how well these defects can be detected.* If defects are rarely introduced during bonding or can be detected and rejected, the integrated circuit's reliability can come quite close to that of the transistor. This appears to be the present case for some manufacturers' products, since at least one large sample of integrated circuits has exhibited a failure rate of less than 0.0018% per thousand hours with 90% confidence;** this figure is competitive with published figures for silicon planar transistors.

This discussion does not consider crystalline defects, which would be expected to occur more frequently in the large circuit crystals than in the small crystals of single transistors. While these defects will influence the manufacturers' yield, they will have little or no effect on reliability because basically they influence only the electrical performance and do not vary with time.

The integrated circuit, then, is no more reliable than its most unreliable elements. However, excluding interconnections, all the elements in an integrated circuit combined have the same susceptibility to the introduction of defects as a single transistor manufactured with the same processes, and the total reliability of the resultant products is determined by the ability to detect and remove the defective items. The available information on integrated-circuit reliability indicates that most defective items are being detected and rejected by the manufacturers.

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* This discussion assumes that all defects that can be detected in a single transistor can also be detected in an integrated circuit.

**"The Application of Failure Analysis in Procuring and Screening of Integrated Circuits", by L.D. Hanley, et. al., MIT Instrumentation Laboratory, October 1965.

Integrated-circuit reliability data are summarized in Section 6.4. As might be expected, these data show a wide range in failure rates (almost three orders of magnitude) for different samples and different operating conditions.

These data also show that as the accumulated hours increase, the estimated failure rates decrease, with minor exceptions. This trend supports (but does not prove) one of the points mentioned earlier: The integrated circuit has no inherent wear-out mechanism, and once the damaged and poorly made devices have failed, the remaining devices in the sample will continue to operate indefinitely. Naturally, as more and more test time is accumulated on the sample without additional failures, the estimated failure rate decreases.

The assumption ordinarily used for reliability prediction -- that a constant failure rate greater than zero applies -- should not be used for semiconductor devices unless a crude estimate is desired (a crude estimate is frequently all that is required). The failure rates of semiconductor devices normally decrease rapidly with time for the first few hundred hours and become constant only when the rate approaches zero. The term mean time between failures (MTBF) therefore has little meaning for semiconductor devices or equipments comprising these devices. The time rate of change of the fractional defective devices in a given group of devices would be much more meaningful as a measure of the reliability of the group.

For equipments, times to first, second, third, (etc.) failures would also be a more meaningful measure of reliability than MTBF since they would indicate how rapidly the device failure rate, and therefore the equipment failure rate, is decreasing. Since the large majority of defective semiconductor devices are identified during environmental tests or in the first few hundred hours of operation, proper screening at the device level will reduce the failure rate to an extremely low level, approaching zero. The time to first failure of an equipment that uses only these devices, then, will be extremely long (approaching infinity) provided the devices are not damaged during assembly into the equipment and are not subjected to excessive stresses while operating in the equipment. Equipment testing, then, could logically be reduced to the determination of whether any devices have been improperly assembled or whether any devices are being overstressed. There is no time base for this testing; the time it takes to determine the existence of damaged or overstressed devices may be very short or very long, and this time is not a direct factor in determining the equipment's reliability.

It is emphasized that even highly reliable semiconductor devices may exhibit slight changes in their performance characteristics at any time. This slight instability may be negligible in many cases but can result in equipment malfunctions if not taken into account during equipment design. In other words, an equipment can be so poorly designed that even using highly reliable devices that have not been damaged or overstressed will not prevent frequent malfunction. Therefore,

a careful design analysis should be performed to determine the effects of device-parameter tolerances and variations on the equipment performance. As the frequency of failures due to severe degradation of device characteristics decreases, such an analysis becomes increasingly important for the improvement of system reliability.

The design analysis ordinarily used for electronic circuits or equipments, the "worst case" analysis, has serious drawbacks. While this analysis is easily performed, it is adequate only where the analysis shows that there are no problems and thus no action needed. Where the worst-case analysis shows that malfunctions can occur and some action may be required, the approach is weak because it gives no indication of the probability of a malfunction. A great deal of effort is often expended in redesigning a circuit or equipment so that it can tolerate the worst-case combination when the probability of the worst case's actually occurring is so remote that no redesign effort is justified. Conversely, engineers often incorrectly assume that the probability of the worst case is too small for concern. A design-analysis method that includes probabilities of occurrences of various combinations of events is needed.

The required design analysis technique must utilize the probability distributions of the various device characteristics involved. Several such techniques for analyzing individual circuits on high-speed computers have been developed in the past few years. However, these techniques have not been widely accepted or used, mainly because of the difficulties in programming specific circuits for analysis. These techniques are being rapidly improved, and a limited amount of work is being done to expand their capability to include large combinations of circuit functions. An easily applied technique that will provide the necessary probability information even for large systems is expected to become available in the next few years.

After a comprehensive design analysis has been performed and corrective action taken where necessary, the resulting equipments must be tested for improperly assembled devices and excessive device stresses. This is a large-scale undertaking but not an impossible one. The major difficulty arises from the fact that, ideally, each and every device should be investigated. The first step is to break down the improper-assembly and overstress categories into subcategories.

Improper assembly includes incorrect wiring, damaged devices, and devices that have not been properly mounted for thermal and mechanical protection. Incorrect wiring can usually be located quickly with functional tests at the module or equipment level. The use of redundancy is a complicating factor, but this is not a new problem.

Damaged devices are not so easily detected -- except those which are so severely damaged that they also exhibit themselves immediately in a functional or environmental test. However, the time to failure of any damaged device is completely unpredictable and cannot be determined before the failure occurs. A time-based acceptance plan to detect these failures is of little practical value since the number of failures that occur in any given time interval has no known relationship to the number that will occur in any other time interval.

The improper-mounting problems can be a result of poor design or poor assembly and are often detected during environmental tests such as shock, vibration, and temperature cycling. These mounting problems include improper heat-sinking, poor interconnections (cold-solder joints, etc.), mounts that allow excessive movement of parts under shock or vibration, excessive lead lengths that can cause shorts, and careless workmanship that leaves solder, weld splash, and foreign material in the equipment. Here, again, time-based operational testing is unlikely to provide much useful information. The only improper mount that might reasonably be expected to show up under extended operational testing is improper heat-sinking, and this should be detected during the testing for overstress conditions.

The problem of detecting thermally or electrically overstressed devices is a difficult one. Thermal overstress, in this discussion, is assumed to be electrically generated but at voltage levels that do not cause instantaneous breakdowns.

With the exception of transients, the design analyses mentioned earlier will reveal excessive power and voltage conditions for a given device and heat-sink combination. Unfortunately, voltage transients, both internally and externally generated, constitute one of the most serious problems in semiconductor equipments now in use. The problem of transient elimination and protection must be given serious attention in both equipment design and testing or the reliability potential of microelectronics may be seriously diluted.

Testing for excessive thermal stresses in equipments has been quite crude, consisting mainly of attaching thermocouples at various points in the equipment for measuring temperature. Recent advances in infrared scanning techniques give rise to the hope that an economical method for rapidly measuring the temperature of large arrays of miniature devices may become available in the near future. The infrared technique is expected at least to indicate whether any device package in a planar array of devices is abnormally hot.

The value of time-based testing for detecting excessive electrical or thermal stresses is essentially the same as the value of accelerated testing, with the additional complication that the exact extent of the overstress is not known. Historically, accelerated testing of electronic devices by means of excessive stresses has failed even when the exact degree of stress was known. There is little reason to expect time-based reliability testing at the equipment level to

have any value insofar as excessive electrical or thermal stresses are concerned. This does not mean that failures due to overstress will not occur during extended operational life-testing at the equipment level. The reverse is true, but the occurrence of such failures tells nothing about the probability of re-occurrence without additional information.

It appears, then, that the reliability of microelectronic equipments cannot be accurately determined with time-based reliability acceptance test plans such as the AGREE method. Emphasis must be shifted to procurement of high-reliability devices, careful design verification, production quality control, and environmental testing. These can be summarized as design verification and testing for damaged or overstressed devices.

What reliability improvement at the equipment level can be expected with microelectronics? For only that portion of the equipment which utilizes the integrated circuit, the reliability can approach unity. The reliability can also approach zero, depending on how carefully the equipment is designed and produced. Several of the reliability data samples shown in Section 6.4, are from systems, indicating that some very-high-reliability systems are currently being produced.

As was the case for weight and volume, the reliability of a given equipment may be controlled by non-microelectronic items. This is particularly true of those equipments which must provide large amounts of output power. Comparisons between microelectronic and conventional weight and volume on a functional-circuit basis were made earlier in this chapter. These are admittedly gross but still more accurate than reliability comparisons. Essentially, the very high reliability potential of an integrated circuit can be realized or degraded to zero depending on the care with which it is procured, handled, and applied. Equipment producers' quality control and design techniques are now capable of yielding complex microelectronic equipments with mean-times-between-failures of thousands of hours.

1.4 Cost

As shown in Figure 1-1, the price of the integrated circuit has been steadily decreasing for some time and now is competitive with that of conventional circuitry -- in the sense that the integrated circuit can be procured for no more than is required to procure, assemble, and test a group of conventional components that will perform the same electronic function. The current prices of the integrated circuit are still far higher than the potential prices based on circuit functions provided.

Most of the cost of an integrated circuit is incurred in the packaging of the crystal. This packaging cost remains essentially constant for a considerable range of circuit complexity. The cost per circuit function is expected to drop well below that of conventional circuitry in the next few years as the capability for increasing complexity (with constant yield) improves.

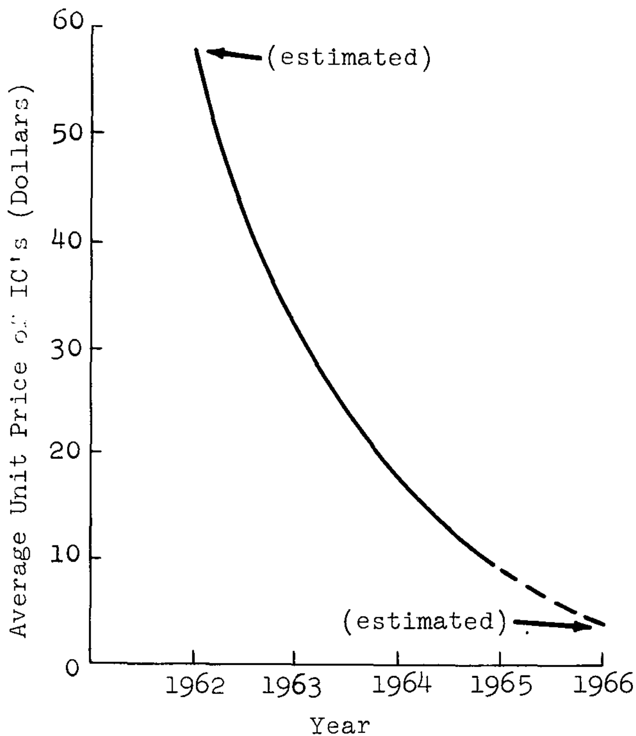

FIGURE 1-1

AVERAGE UNIT PRICES OF INTEGRATED CIRCUITS vs. TIME

Savings resulting from the widespread use of microelectronics will begin at the device-procurement stage but will be far more significant after the equipments are placed in operation. Both maintenance and logistics costs can be drastically reduced even without standardizing circuit performance characteristics. These reduced costs for maintenance and logistics result directly from the increased reliability.

With fewer failures occurring in equipments, the number of maintenance actions required is obviously reduced. The maintenance costs are reduced correspondingly provided the maintainability remains constant. Actually, the maintainability can be increased with microelectronics as the cost per circuit function decreases because the throw-away complexity level can be raised without a corresponding increase in throw-away cost.

For logistic support, the very high reliability of microelectronics makes new and more economical approaches possible. One of these approaches, logistic self-support,* is based on the assumption that sufficient spares can be carried with the equipment to support maintenance throughout the expected life of the equipment at a lower cost than that of supplying spares through currently used logistics channels. This approach eliminates the cost of the paperwork necessary to enter and maintain an item in logistics channels; it also reduces the actual number of spares required to support the equipment.

1.5 Current Physical Limitations

It was pointed out earlier that the cost per function decreases and the reliability increases when more and more functions are included in the integrated-circuit chip. The obvious conclusion, then, is to put a complete system in the

*For a detailed discussion of this approach see "Factors Affecting the Early Exploitation of Integrated Circuitry", Interim Technical Documentary Report ASD-TRD-7-998-4, Volume 4, 1 July 1963.

chip and reap maximum benefits in terms of reliability and cost (weight and volume would also be minimized). Unfortunately, current technology does not permit this. There are severe limitations on the functional capability as well as physical limitations on the complexity achievable with current integrated-circuit technology.

One of the major limitations on complexity is the single-level intraconnection** technique now in use. The inability to make crossovers in the conductor pattern not only limits the total complexity achievable but also places severe restrictions on element layout which adversely affect the functional capability. The precise limit on complexity imposed by single-level intraconnections is not known but appears to be the equivalent of approximately ten simple gates. At any rate, complex circuits now available are approaching the limit, and a technique for at least double-level intraconnections is required for further increases in complexity. It is hoped that a multi-level technique will be developed to remove intraconnections as a practical limit on complexity.

Another physical problem is the electrical isolation of elements in the chip. The generally used p-n-junction method of isolation restricts the frequency capabilities of integrated circuits. The restriction becomes more severe as elements are crowded closer together, and it eventually limits the element density for useful frequencies.

Some experts have stated that a flexible, computer-controlled intraconnection technique that would permit the connection of only good elements into complex circuits is necessary for achieving practical yields for extremely complex circuits. While such a technique would no doubt be useful, the actual effect on yield is not as predictable as one might think. For example, if most of the defective elements are concentrated in certain areas on the slice (as is frequently the case), yield will be approximately the same whether a fixed or flexible intraconnection technique is used. (It is assumed that several circuits are possible from the slice; if only one or two circuits are possible, yield might vary significantly.) Also, the constraints imposed by the technique used for separating the slice into individual chips (dicing) must be considered.

The approach of testing all elements and connecting only acceptable ones into circuits is, in effect, an application of the standby-redundancy concept. Through the application of active-redundancy concepts, both the yield and long-term reliability of circuits could be increased and the current fixed-mask technique could be employed for intraconnections.

**Intraconnections are defined as the connections between the elements in a single chip, e.g., the aluminum conductor pattern alloyed into the chip surface.

While the flexible-intraconnection technique's utility for increasing yield is not certain, its value for implementing custom large-scale digital functions is unquestioned. Many system designers feel that there is little use for standard digital functions above the complexity of multiple gates. The lack of replications of large-scale digital functions makes the manufacture of such items unattractive at the present time. A flexible intraconnection technique would permit large-scale functions to be economically produced on a custom, small-volume scale.

1.6 Future Microelectronic Developments

A common reaction to the first encounter with an integrated circuit (properly magnified) is "the whole production process must be completely automated". This is not the case, however; a major portion of integrated-circuit manufacturing is performed by highly skilled personnel.

If the manufacturing steps are broken into two major groupings, those involving the complete wafer and those involving separate chips, it is seen that the first group relies heavily on automation and the second group relies heavily on human labor.

The major role of people in the wafer-processing steps is in the operation of automatic equipments, loading and unloading these equipments, and transporting groups of wafers from place to place. Little increase in automation is expected in this area.

Manufacturing steps that involve device assembly offer promise for automation (device testing is already highly automated in most production plants). The chip-mounting and lead-attachment steps are particularly inviting for automation since they are almost completely dependent on human skill, with the accompanying cost and reliability penalties. Further, errors at these points are very difficult to detect (there is no practical technique available for the nondestructive testing of minute connections and joints). The "flip-chip" technique, in which the chip is turned face downward and the metalized contact areas are joined to similar areas preformed on a substrate, or some variation of it, may provide the solution to the mounting and lead-attachment problems.

In addition to manufacturing steps, major areas of concern in the automation of integrated-circuit production are the production tooling (particularly the diffusion and intraconnection masks) and circuit design.

The electronic design of current integrated circuits is much more constrained by the topological layout of the circuit elements than are conventional circuits. The coupling problems are more severe (because of the p-n junction method of isolation), and only a single level of intraconnections is utilized. As the circuits become more complex, the number of variables that must be considered becomes

enormous. Considerable effort has therefore been expended on development of computer techniques to assist the designer in handling these variables. These efforts are expected to yield valuable results in the next few years.

The utility of a flexible intraconnection technique was mentioned earlier. According to E. A. Sack*, the use of a machine-controlled light beam or electron beam to create a tailored intraconnect pattern appears to offer great flexibility. It requires little extrapolation of present technology to envision a machine that scans the integrated-circuit wafer to identify functional gates**; accepts instructions for the interconnection of these gates into a given digital function; decides on an optimum topology against criteria of speed, minimum area, etc.;† and delineates the interconnection pattern on the wafer. Parts of this machine are now under development in a number of laboratories, and the ultimate employment of such apparatus in one form or another seems to be only a matter of time.

Similar computer-controlled apparatus could be used in the diffusion-masking steps to reduce the time necessary for development of new and custom circuits. Extension of this apparatus to include the selection of diffusion variables and element layout and, finally, to control the actual diffusion processes is not beyond the realm of current technology.

Computers are expected to play a major role in future integrated circuitry, aside from their obvious role as major consumers of these circuits. The use of computers in extensive design analysis of electronic circuits has become more and more common in the last few years. Variations of these analysis techniques are frequently used to "optimize" designs, at least from the viewpoint of performance and, occasionally, reliability. These techniques will be increasingly applied to integrated circuits and -- if performance and reliability variables are included, along with manufacturing yield (and thereby initial circuit cost) -- will permit optimal designs to be achieved economically.

1.7 Summary

This chapter has painted a bright picture for the future of microelectronics. Microelectronic circuits, particuarly integrated circuits, appear to be superior to equivalent conventional circuits in several respects. However, a note of caution is in order. Early in its life the transistor was acclaimed as the solution to virtually all problems then plaguing electronic systems. Most of these problems still exist.

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*Microelectronics and Large Systems, Spartan Books, 1965.

**T. E. Everhart, O. C. Wells, and R. K. Matta, "Evaluation of Passivated Integrated Circuits Using the Scanning Electron Microscope." J. Electrochem. Soc. Vol. 3, No. 8, (August 1964), pp. 929-936.

†I. M. Mackintosh, "Programmed Interconnections - A Release from Tyranny," Proc. IEEE, Vol. 52, No. 12 (December 1964).

As was the case with the transistor, the integrated circuit is a long step forward in reliability potential. However, the potential of the transistor has not been fully exploited, and carelessness in the procurement or application of the integrated circuit can result in the same deficiency. Reliable devices, whether piece parts or complex circuits, do not guarantee reliable equipments or systems.

The major aspects of microelectronics are summarized as follows:

(1) On a functional-circuit basis, microelectronic circuits can be assembled into equipments at 1/5 to 1/50 the volume and weight of transistorized conventional circuits.

(2) The performance capability of microelectronics is still limited, and a given equipment or system may therefore remain essentially unchanged in size, reliability, etc., if converted to microelectronics.

(3) The constant-failure-rate assumption normally made for reliability calculations is incorrect for microelectronic devices. The failure rate for these devices decreases rapidly with time, becoming asymptotic to zero.

(4) A failure rate of 0.0018% per 1000 hours with 90% confidence has been confirmed for one large sample of digital integrated circuits.

(5) Equipment-reliability acceptance-test procedures based on extended operational life-testing are impractical for high-reliability micro-electronic equipments.

(6) The cost of digital integrated circuits is competitive with that of conventional component circuits and can be expected to drop well below conventional-circuit cost as the complexity within a single package increases.

(7) The total cost of microelectronic equipments can be well below conventional equipments provided a large portion of the reliability potential is achieved. These cost savings will accrue from reduced maintenance and logistic costs; testing, production, or design costs may also be lower on specific equipments.

(8) The design freedom of equipment designers has been increased by microelectronics, and many new approaches to performing electronic functions will be developed.

(9) The small size and weight, high reliability, and low cost per function of integrated circuits provide the means for practical implementation of redundancy concepts.

BASIC PROCESSES AND DESIGN CONSIDERATIONS

TWO

2.1 Bipolar Transistor Devices

Some of the basic processes and techniques that are important in integrated-circuit fabrication are discussed in this chapter to provide the reader a basic understanding of how these factors constrain circuit design. Section 2.1 is a discussion of integrated circuits that use bipolar transistor devices. Section 2.2 covers metal-oxide-semiconductor (MOS) field-effect devices.

2.1.1 Preparation of Semiconductor Materials

The rapid advances in semiconductor-device technology over the past fifteen years would not have been possible except for the impressive progress made in the purification and preparation of semiconductor materials. Near-perfect crystals of virtually absolute purity are needed if consistent, high-quality devices are to be made. The impurity level must be controlled to less than one impurity atom per million -- at times, to less than one atom per billion. This level is not detectable chemically or spectroscopically. Its measurement depends entirely on electrical conductivity. The expression for conductivity is:

$$\sigma = q(\mu_p P + \mu_n N) \qquad (2\text{-}1)$$

where

μ_p = mobility of holes

μ_n = mobility of electrons

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p = number of holes per cubic centimeter

n = number of electrons per cubic centimeter

q = electron charge at or near room temperature

For an intrinsic semiconductor n or p can be assumed equal to the donor or acceptor impurity density, respectively. When n is very much greater than p, the semiconductor is n type (electrons are the majority carriers); also, generally, n is much greater than n_i (the intrinsic free-electron density), so that n_i can be ignored when the concentration of donor impurity is being determined.

2.1.2 Measuring Conductivity

The heated-probe check is a convenient method for determining the polarity of the charge carrier, that is, to determine whether the semiconductor wafer is n-type or p-type. A galvanometer is connected to the semiconductor wafer by means of two probes that are conveniently placed on the wafer. One of the probes is at room temperature, and the other probe is attached to a heated soldering iron, as shown in Figure 2-1. With the hot probe connected to the negative side of the galvanometer, the needle of the galvanometer registers a negative reading for the n-type material and a positive reading for the p-type material.

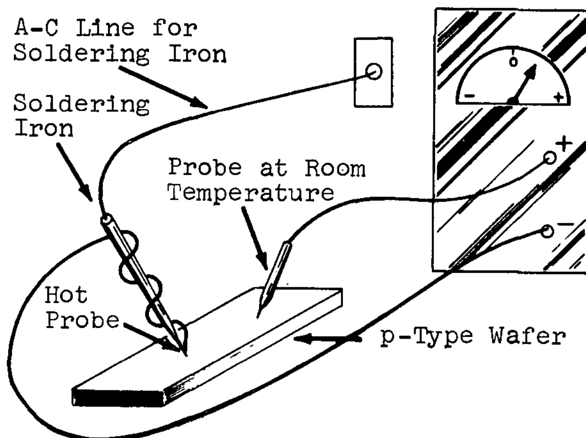

FIGURE 2-1
THE HEATED-PROBE CHECK

The heated-probe check can be set up with a microammeter instead of a galvanometer. When current is indicated on the microammeter with the hot probe connected to the negative terminal of the meter, the wafer is p-type. When the hot probe is connected to the positive side of the microammeter and current is indicated on the meter, the sample is n-type. These indications occur because the majority carriers diffuse in the direction of the negative temperature gradient. The majority carriers are electrons in the n-type material and holes in the p-type material. In an n-type semiconductor, the majority-carrier electrons diffuse away from the hot probe; thus they cause it to become positive with respect to the colder probe.

A commonly used technique for measuring conductivity is the 4-point probe technique shown in Figure 2-2. Four equally spaced probes are aligned on the semiconductor wafer. For the arrangement illustrated the resistivity is given by

$$\rho = \frac{V}{I} 2\pi S F\left(\frac{W}{S}\right) \qquad (2\text{-}2)$$

where $F\left(\frac{W}{S}\right)$ is a geometrical correction factor that corrects for alteration of current-flow lines through the sample for special boundary conditions such as a finite sample thickness W.

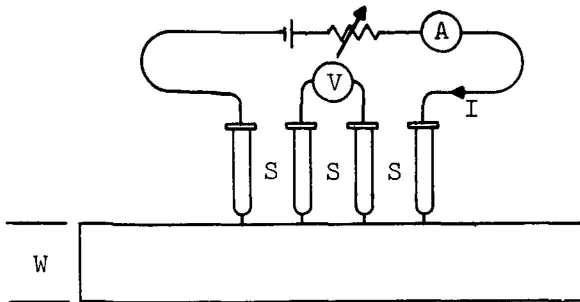

FIGURE 2-2
ARRANGEMENT FOR FOUR-POINT PROBE MEASUREMENT

Another method for measuring conductivity type and carrier concentration employs the Hall effect. When a sample piece of semiconductor is placed in a magnetic field and a current is made to flow perpendicular to the field, a voltage is produced across the sample along an axis perpendicular to both the magnetic field and the direction of current flow, as shown in Figure 2-3. The magnitude and direction of this voltage can be used to determine the concentration and sign of the current carriers in the semiconductor sample. For a sample of width, W, the Hall voltage is given by

$$V = 10^{-8} \frac{RIH}{W} \qquad (2\text{-}3)$$

where V is in volts, I in amperes, H in Gauss, and W in centimeters, and R is the Hall constant given by

$$R \approx \frac{3}{8} \qquad (2\text{-}4)$$

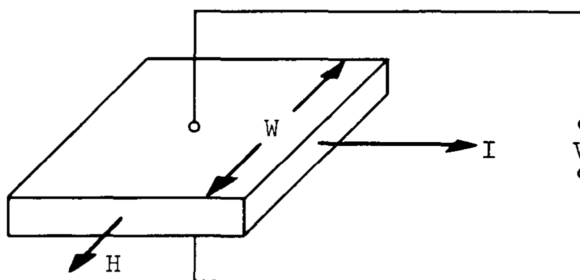

FIGURE 2-3
HALL EFFECT

The expression for sheet resistivity is developed as follows:

The resistance of the conductor illustrated in Figure 2-4 is

$$R = \rho \frac{\ell}{tw} \text{ ohms} \qquad (2\text{-}5)$$

where

ρ = resistivity of the diffused conductor

ℓ = length of the diffused conductor

t = thickness of the diffused conductor

w = width of the diffused conductor

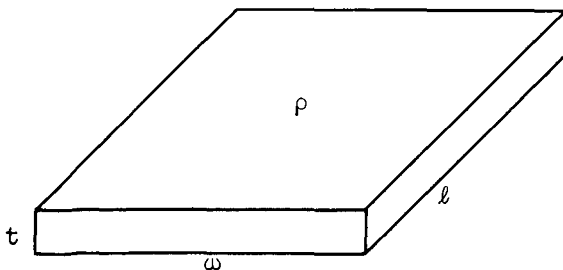

FIGURE 2-4
PARAMETERS FOR DETERMINING SHEET RESISTIVITY

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The sheet resistivity is defined as

$$\rho_s = \rho/_t \qquad (2\text{-}6)$$

This is valid when the depth of the conductor is small (a few microns) and it is relatively constant, as is the case for most diffused resistors. Substituting ρ_s for $\rho/_t$ in the above equation for resistance gives

$$R = \rho_s \frac{\ell}{W} \qquad (2\text{-}7)$$

or

$$R = \rho_s K \qquad (2\text{-}8)$$

where

$K = \ell/W$

The term K is referred to as the length-to-width ratio and is important in specifying resistor values. If ρ_s is known, the resistance of any resistor is determined simply by specifying the ℓ/W ratio.

As an example, consider a system which requires a 5K-ohm resistor using a sheet resistivity of 50 ohms/sq.

Since R and ρ_s are given, it is only necessary to solve for K:

$$K = \ell/_W = R/_{\rho_s} = \frac{5K}{50} = \frac{500\not{0}}{5\not{0}} = 100 \qquad (2\text{-}9)$$

The resistance is determined by $\ell/W = 100$. There are an infinite number of solutions, and the actual choice of dimensions will depend on other factors such as required surface area for power dissipation, or distributed capacitance.

2.1.3 Alloying

In an npn transistor, three regions alternate in the conductivity type. In an alloy transistor the starting material is p-type, and an n-conductivity layer has to be realized on either side of the wafer, as shown in Figure 2-5.

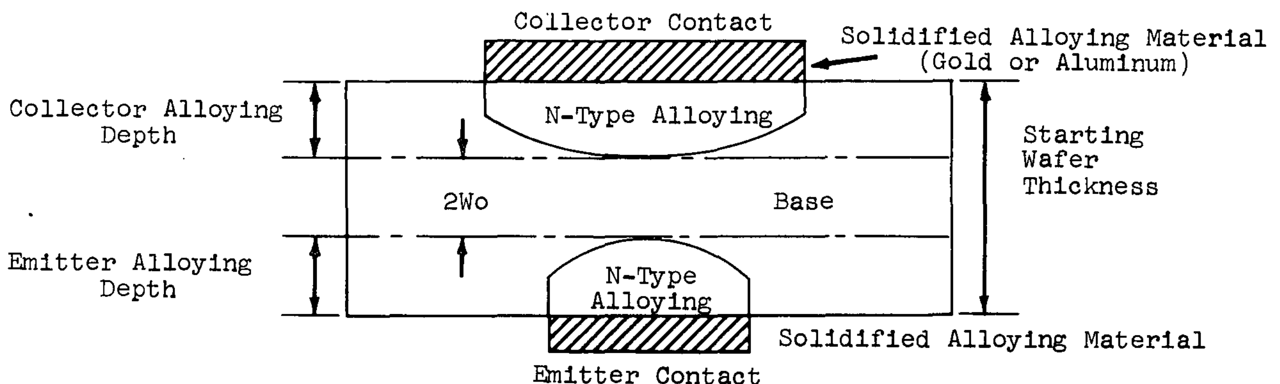

FIGURE 2-5
ALLOY TRANSISTOR

These regions are formed by placing spheres or discs of doping material on opposite sides of a prepared wafer, and heating to allow the dope to melt and dissolve part-way into the wafer. As the molten alloy is carefully cooled, dissolved germanium recrystallizes at the liquid-solid interface of the wafer, which acts as a single-crystal seed. The temperatures at which these processes are carried out vary from 700° to 900°C depending on the alloying material used.

Attempts to reduce the dimensions of alloy transistors for high-frequency applications led to the introduction of electrochemical etching and plating techniques, which made possible the development of interface-barrier transistors. In this device, very close emitter-collector spacings are possible. It is necessary to start with a thin wafer of semiconductor and then etch it still further by subjecting it to two coaxial jets of etching solution. When the thickness of the central web has been reduced to about 0.2 mil, metal contacts are electroplated into the same points, with the same jets being used as electrolyte vehicles.

2.1.4 Diffusion

By diffusing donor and acceptor impurities into semiconductor materials, it is possible to fabricate p-n junction devices that have superior electrical characteristics. The diffusion process has many distinct advantages over other fabrication processes, particularly if silicon is the material used. It is the basic process and in most cases the only process in which superior transistor characteristics can be realized. Junction depths and impurity concentration of the layers can be controlled more precisely than in alloyed structures. An important consequence of the diffusion is the realization of an accelerating or drift field in the base of a transistor. The mathematical relationships for impurity concentration are developed below.

Fick's law of diffusion can be written as

$$\frac{\delta C}{\delta t} = \frac{\delta}{\delta x}\left(D \frac{\delta C}{\delta x}\right) = D \frac{\delta^2 C}{\delta x^2} \tag{2-10}$$

(which is a form of Fourier's law of heat conduction)

where

D = the diffusion constant

x = space coordinate (referenced to crystal surface)

t = time in seconds

c = Impurity concentration density atoms/cm^3

Equation 2-10 can be written as

$$D \frac{\delta^2 C}{\delta x^2} = \frac{\delta C}{\delta t} \tag{2-11}$$

This expression is easily solved by the Laplace transform method:

$$L\left[D\frac{\delta^2 C}{\delta x^2}\right] = L\left[\frac{\delta C}{\delta t}\right] \quad (2\text{-}12)$$

Let

$$L\,[C] = F(S) \quad (2\text{-}13)$$

Then

$$D\frac{\delta^2 F(S)}{\delta x^2} = SF(S) \quad (2\text{-}14)$$

The solution for Equation 2-14 can be written as

$$F(S) = C_1\, e^{\sqrt{S/D}\,x} + C_Z\, e^{(-\sqrt{S/D}\,x)} \quad (2\text{-}15)$$

To evaluate C_1 and C_2 , suppose F(s) is an infinitesimaly small number; then

$$\Sigma = C_1\, e^{\infty} + C_2\Delta \quad (2\text{-}16)$$

where Δ is also a small number. In order for Equation 2-16 to be true, it is necessary that

$$C_1 = 0 \quad (2\text{-}17)$$

Thus

$$F(S) = C_2\, e^{(-\sqrt{S/D}\,x)} \quad (2\text{-}18)$$

For the boundary conditions $C_2 = C_o$ at x = 0 for all t,

$$C_2 = \frac{C_o}{S} \quad (2\text{-}19)$$

Therefore

$$F(S) = \frac{C_o}{S}\, e^{(-\sqrt{S/D}\,x)} \quad (2\text{-}20)$$

The inverse Ĺ transform of Equation 2-20 is given as a complementary error or an error function as shown in Equation 2-21:

$$C = C_o\,\mathrm{erfc}\left(\frac{x}{2\sqrt{Dt}}\right) = C_o\left[1 - \mathrm{erf}\,\frac{x}{2\sqrt{Dt}}\right] \quad (2\text{-}21)$$

The concentration with respect to time and distance follows this error function; it is plotted in Figure 2-6. In the derivation of Equation 2-21, it was assumed that there was an infinite source of impurity available throughout the diffusion period. For a limited number of impurity atoms the following expression is obtained:

$$C = \frac{\overline{C}_o}{\sqrt{\pi Dt}}\, e^{(-\,x^2/4Dt)} \quad (2\text{-}22)$$

where $\overline{C}_o$ is the number of impurity atoms placed on the surface.

After the introduction of the diffusion techniques into semiconductor fabrication it was possible to achieve base widths, with high accuracy, of less than 1 micron, which improves considerably the transport factor and the α cut-off frequency. Other means of improving the high-frequency response would be to reduce the collector-base junction area, as has been done with mesa transistors. A typical mesa transistor is shown in Figure 2-7.

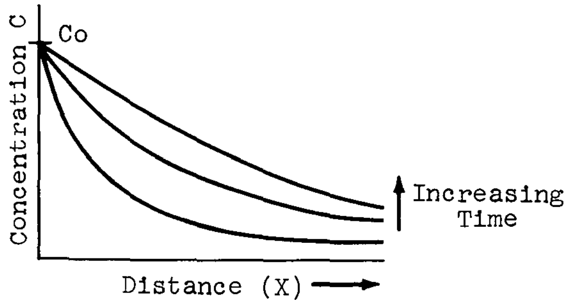

FIGURE 2-6
IMPURITY CONCENTRATION VS DISTANCE

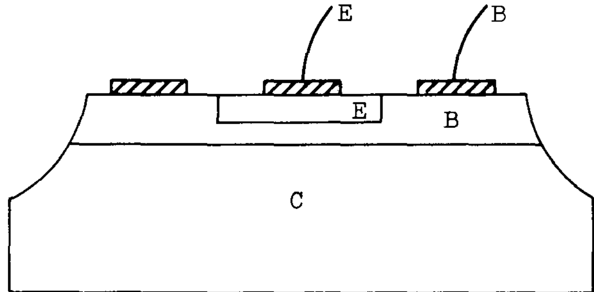

FIGURE 2-7
MESA TRANSISTOR

The defect of such a structure is apparent. The collector-base junction is exposed to the surrounding atmosphere, and surface effects at this point are severe. To minimize surface effects on junctions, the planar diffused structure was introduced by Fairchild. A typical planar structure is shown in Figure 2-8.

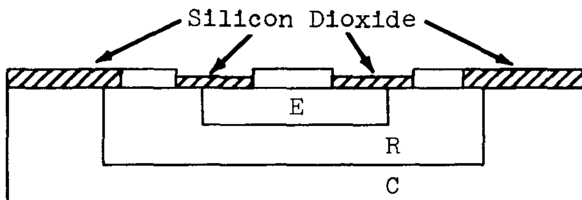

FIGURE 2-8
PLANAR STRUCTURE

The planar process permits the passivation of the surface by an oxide layer at an early fabrication stage. The silicon-oxide coating is grown on the surface before any junctions are diffused. This greatly improves the parameters that are particularly sensitive to surface conditions. These parameters are the reverse leakage currents, breakdown voltages, noise figure, and low current β. Planar structures also made it possible to solve many problems in the realization of integrated structures, in which several elements are built simultaneously on the same piece of semiconductor.

To show how the planar process is used to fabricate devices for microcircuits, the steps taken in building a planar-diffused transistor are described here. This process is common to all bulk-type microcircuits.

The steps used in the fabrication of an npn planar-diffused transistor are shown in Figure 2-9. The starting material is n-type silicon (A). The entire surface of the n-type silicon wafer receives a thermally grown oxide layer. A window is chemically opened through the oxide layer (B). A p-type diffiusion is then performed to construct the base region of the transistor (C). The wafer with the window is placed in a diffusion furnace, with an impurity such as boron, for a few hours at about 1300°C. The junction formed in (C) is formed under the original oxide layer and never sees the ambient environment of the diffusion furnace. A new oxide layer is formed during the diffusion.

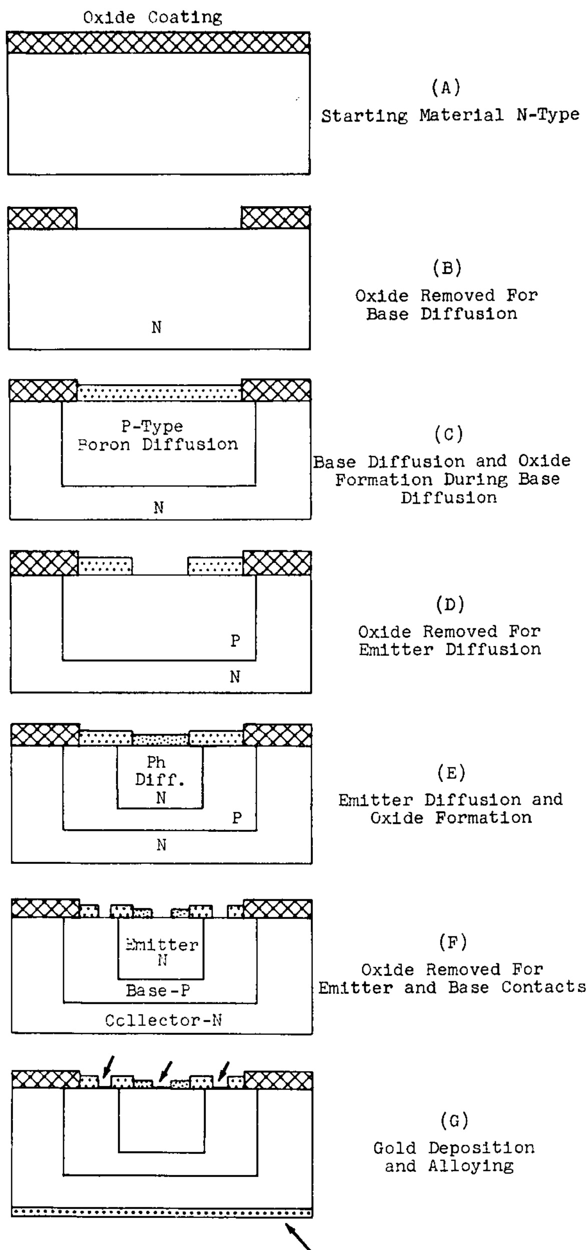

FIGURE 2-9

FABRICATION STEPS

A window is now opened through the new oxide layer (D). This window is much smaller than the previous window used for the base diffusion. The n-type emitter diffusion is carried out in the same manner as the base diffusion except that now an n-type dopant such as phorphorous is used (E). During the diffusion, the oxide layer is regrown across the window.

Through precision masking techniques, very small windows are opened in both the base and emitter regions (F). These windows are about 0.005 inch in diameter for many transistors. Aluminum is then deposited into these windows to form the ohmic contacts to the transistor (G). The lead wires may now be attached. The collector connection is frequently made by soldering the substrate directly to the header. It should be noted that the p-n junctions (throughout the fabrication process and on the finished device) have always been beneath the oxide layer. The oxide layer protects or passivates the p-n junctions from outside effects

that can cause degradation of the device.

Thus, in addition to furnishing the masking during diffusion, the planar oxide layer or coating is also a means of protecting or passivating the p-n junction. Planar devices are used in bulk-type semiconductor microcircuits instead of mesa devices. As was shown in Figure 2-7, the p-n junctions on mesa-type devices are exposed.

2.1.5 Oxide Masking

The opening of windows in the silicon dioxide layer forms a stencil-like structure through which diffusion and alloying can be carried out. This stencil-like structure or oxide mask is made by the following process (usually referred to as the planar process):

(1) The clean silicon wafer is placed in a furnace, where the oxide layer is grown.

(2) The oxide layer is coated with a photosensitive acid-resistant film such as Kodak KPR.

(3) The KPR film is stabilized with infrared light for about thirty minutes.

(4) A positive (the areas where diffusions are desired are black areas on a transparent film) of the configuration desired is placed over the wafer with the KPR film.

(5) Ultraviolet light is used to illuminate the KPR film through the positive. Areas of the KPR film exposed to the ultraviolet light are hardened and are impervious to acid etches; areas not exposed are removed by developing.

(6) The KPR is developed so that it is removed where not exposed. The result is an acid-resistant film stencil.

(7) The wafer is then placed in hydrofluoric acid, which removes the silicon dioxide where there is no KPR film.

(8) A window is thus opened through the oxide, forming a mask for diffusion and alloying.

2.1.6 Precision Evaporation

The extreme thinness of the diffused layer created obstacles, which required a search for new methods to make alloyed electrical contacts to the layer without puncturing or otherwise destroying it. Another problem required a solution just as urgently as that of the thin base layer. For high-frequency performance these alloyed regions have to be as close together as possible -- without electrically shorting. This problem was solved by a vacuum-evaporation technique. The evaporation

technique allows the controlled deposition of thin layers of materials. It is also a method for depositing highly reactive materials, such as aluminum, that are difficult to work with in air. Further, it allows greater cleanliness in technique and hence gives a more intimate contact between the layer and the surface upon which it has been cooled. In addition, the fact that the evaporation beams travel in straight lines permits the use of precisely dimensioned masks to create similarly precise evaporated patterns. An alloying operation follows the evaporation of the gold antimony or aluminum stripe.

2.1.7 Epitaxial Techniques

Epitaxy is a means of growing a very thin (3-25μ), uniformerly doped monocrystalline region on a relatively low-resistivity semiconductor substrate. The epitaxial process involves the decomposition of $SiCl_4$ with hydrogen at approximately 1200°C; the silicon that is freed is deposited on the basic silicon substrate. The deposition is perfectly oriented; the result is a layer of monocrystalline silicon with a uniform doping level at all depths. Subsequent diffusions are more predictable because of this uniform doping. The combination of planar diffusion techniques with epitaxial structures gives improved transistor characteristics. A typical planar-epitaxial transistor is shown in Figure 2-10.

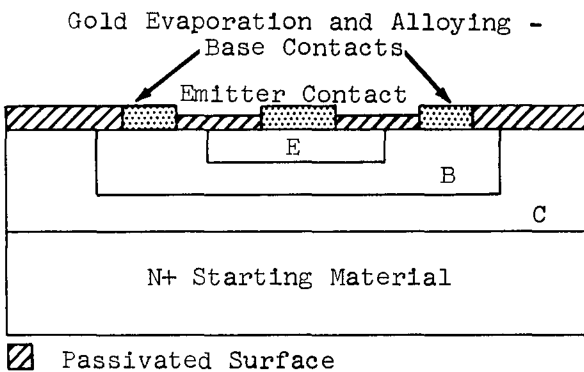

FIGURE 2-10
PLANAR-EPITAXIAL TRANSISTOR

As Figure 2-10 implies, there are several advantages of incorporating an epitaxial layer on the collector substrate. The epitaxial layer has comparatively higher resistivity than the starting material, so that base-collector junction capacitance is low. The series-collector bulk resistance remains low since the epitaxial layer is thin and the substrate is lightly doped. Thus the saturation resistance is low, which permits higher current flow for a given dissipation, and shorter collector-saturation time. Also, the collector-base breakdown is high because of the high resistivity of the epitaxial layer.

In one process, a mixture of hydrogen and silicon tetrachloride flows through a quartz tube into the reaction zone of the furnace. The flow path may be vertical or horizontal. Consider the horizontal case, shown in Figure 2-11. Energy is delivered to the reaction zone by external r-f coils that couple to a graphite "susceptor". The wafers lie on top of a quartz sleeve, which encases the susceptor, and they are thus protected from possible contamination by impurities from the graphite.

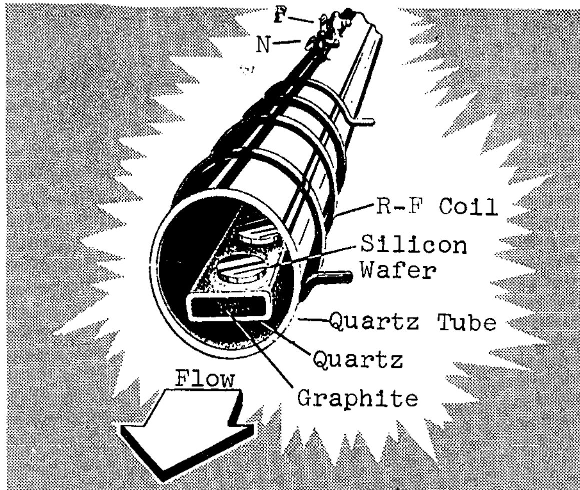

FIGURE 2-11

REACTION ZONE OF EPITAXIAL FURNACE

In the overall reaction that proceeds in the vicinity of the heated silicon wafers, hydrogen reduces silicon tetrachloride to form pure silicon and hydrogen chloride gas. Silicon evolved in the reaction is deposited on the silicon wafer and has a strong tendency to continue the crystallographic pattern embodied in the wafer. This continuation of structure is "epitaxy". While this picture of the process is imperfect with respect to detailed mechanisms, it is reasonable to assume that to maintain the crystal pattern a silicon atom on the growing surface must be given sufficient time to migrate to the proper crystallographic site or to leave the surface before it is trapped by other atoms in a wrong position. This qualitative picture is supported by the observation that disordered growth occurs if the growth rate is pushed above a certain value at a given temperature. Raising the temperature raises the tolerable growth rate. Since the rate of the deposition process can be controlled, and since it can be stopped at any time by shutting off the reactants, the thickness of the epitaxial layer can be controlled to within a few tenths of a micron.

It is also possible to adjust impurity doping precisely. Again, a number of methods can be used. An impurity compound can be mixed in a small quantity with the silicon tetrachloride; this mixture can then be reduced in the reaction zone, and the impurity atoms will be included in the resultant crystal. Alternatively, separate vessels can be provided for the main silicon tetrachloride supply, for a p-doped supply, and for an n-doped supply, giving separate n and p ports, as suggested in Figure 2-11. As in the main supply, a carrier gas can be sent through the doped vessels. Also, diffusion can be employed as the delivery mechanism. In the latter, it is possible to control vapor pressure by adjusting temperature. Still another approach employs gaseous impurity compounds diluted in a carrier gas.

2.1.8 Isolation

The isolation between components on a monolithic substrate is usually accomplished by reverse-biased p-n junctions. Associated with the p-n junction is a capacitance and the normal leakage currents (see Figure 2-12). Therefore, complete isolation is not accomplished, and the effect is less-than-optimum performance.

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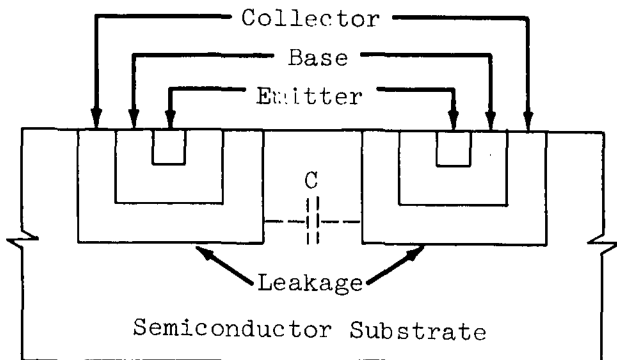

FIGURE 2-12
CAPACITANCE AND LEAKAGE IN P-N JUNCTION ISOLATION

As indicated in Figure 2-12, there is capacitive coupling between the collectors of the two transistors because of the capacitance associated with the junctions. At normal doping levels, the value is about 0.1 pf/sq.mil at 0.5 volts of reverse bias. In addition, the leakage current is a function of temperature and may be appreciable at high temperatures. It would be best to isolate the devices from each other by a dielectric and obtain isolation more closely related to discrete components. A number of techniques have been developed to accomplish this. Some manufacturers are also developing methods for growing single-crystal silicon on an insulating substrate.

A number of monolithic isolation techniques* are currently in use. One of the earliest** to be developed is illustrated in Figure 2-13. The starting material is an n-type silicon substrate with a heavily doped epitaxial layer, as shown in (A).

Grooves are etched in the substrate according to some predetermined layout. These grooves are several mils deep. An oxide is either grown or vapor-deposited over the entire surface of the substrate. This oxide is SiO_2 and will perform the isolation function (B). Polycrystalline silicon is epitaxially deposited over the oxide (C). The single-crystal substrate is lapped to a point where single-crystal islands are isolated from one another by the oxide and imbedded in polycrystalline silicon (D). The sole purpose of the polycrystalline silicon is to hold the single-crystal islands together. These islands can now be doped and the devices fabricated.

One difficulty with this technique is the degree of control required in the lapping operation. The thickness of the n region is important in device fabrication, and the necessary lapping tolerance is in the order of 1 to 2 microns.

A number of techniques have been proposed for overcoming this difficulty†. One is illustrated in Figure 2-14. In this method a highly doped, uniform single-crystal substrate, as illustrated in (A), is processed in exactly the same

* J. W. Lathrop, "The Status of Monolithic and Thin Film Circuits", Electronic Industries, June 1965, p. 38.

** D. McWilliams, C. Fa, G. Larchian, and O. Maxwell, Jr., "A New Dielectric Isolation Technique for High Quality Silicon Integrated Circuits," Symposium Electro-Chemical Society, III, 153c July 1964.

† N. Schwartz, "Reactive Sputtering", Tenth National Vacuum Symposium, American Vacuum Society, p. 325 (1963) MacMillan, New York.

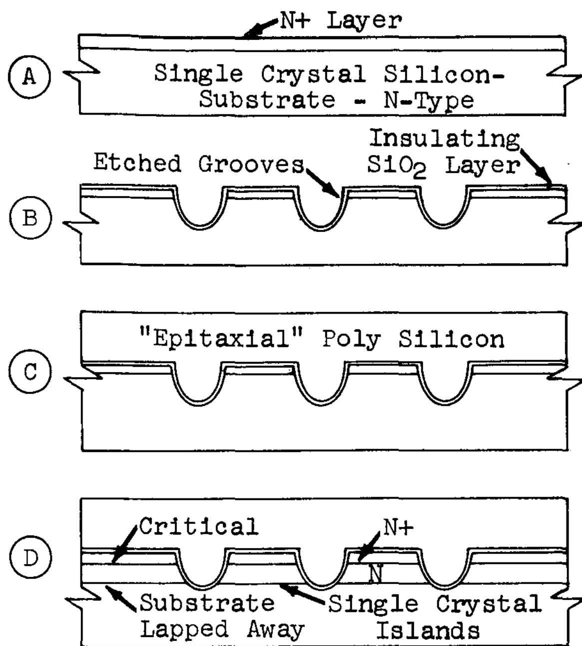

FIGURE 2-13

DIELECTRIC ISOLATION (I)

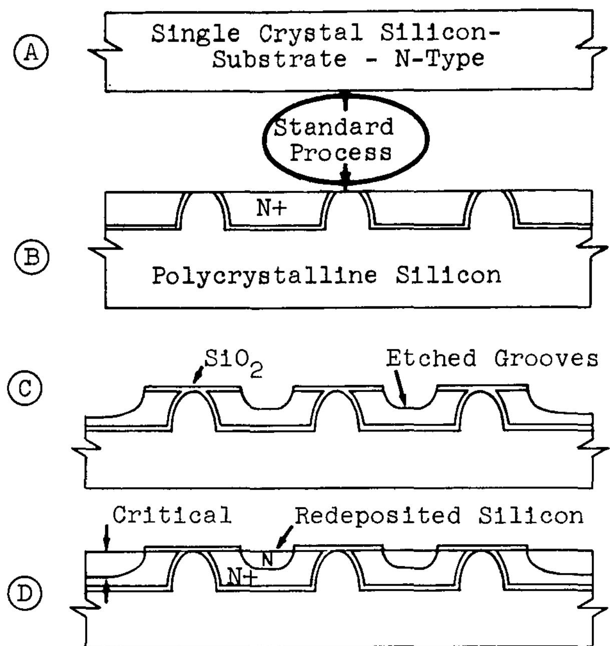

FIGURE 2-14

DIELECTRIC ISOLATION (III)

way as in Figure 2-13 to yield isolated islands of low-resistivity material (B). By use of a SiO_2 film for selective masking, regions within these islands can be vapor-etched (C) and lower resistivity silicon redeposited, as in (D). The critical distance is now controlled by the etch and deposit processes of epitaxial deposition, which are superior to mechanical lapping.

Another method* is shown in Figure 2-15. The critical distance is controlled during the initial step of epitaxially depositing an n-film on an n+ substrate,

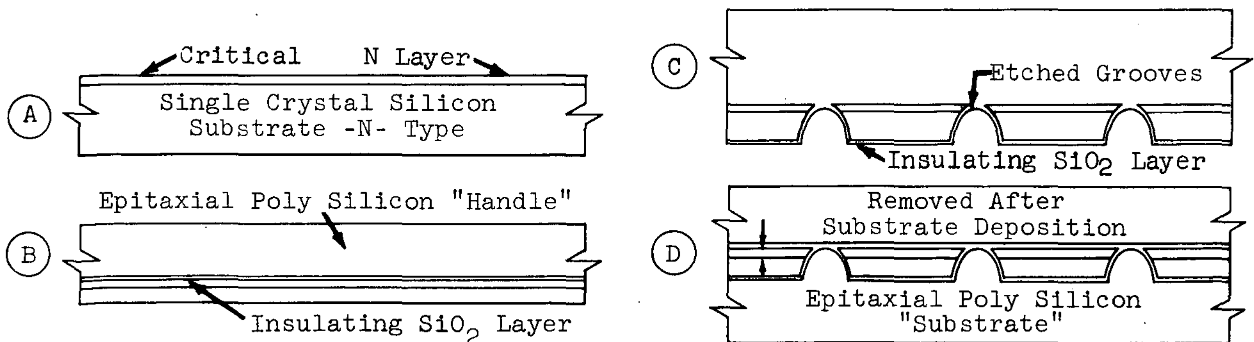

FIGURE 2-15

DIELECTRIC ISOLATION (II)

* G.L. Schnable and A.F. McKelvey, "A Technique for Preparing Oxide-Isolated Silicon Wafers for Microcircuits", Electron Devices Meeting, Washington, D.C., October 1964.

as shown in (A). Next, an insulating SiO_2 layer is deposited over the n-layer, and polycrystalline material over this. The only purpose of this polycrystalline layer is to serve as a "handle" during operations and allow the substrate to be thinned to a few mils, as shown in (B), without breakage. Grooves are then etched in this thinned single-crystal material, creating mesas over which an oxide can be grown as in (C). Finally, an epitaxial polycrystalline "substrate" is deposited over thin oxide and the "handle" material removed to leave isolated regions with a common flat surface, as shown in (D).

The processes of Figures 2-14 and 2-15 minimize the lapping control for dielectric isolation, but at the expense of additional processing. The p-type, as well as n-type, material can be processed and both types of islands can be formed on the same slice.

The result of these methods is isolated islands of semiconductor material into which impurities can be diffused to form active and passive components.

A circuit fabrication procedure* combining oxide isolation with other techniques -- which include localized epitaxial growth, localized etching and backfilling, and localized gold doping -- is described below. The process steps are illustrated in Figure 2-16.

(1) An epitaxial substrate wafer is prepared by conventional processing techniques with an n+ layer on one surface. The starting resistivity is chosen to be that required for one or more of the finished circuit elements.

(2) Depressions are etched into the back of this wafer in locations corresponding to regions where the required conductivity type and impurity density will be different from those of the region selected in (1).

(3) Each depression is filled with epitaxial silicon that has the impurity density and type required for additional devices.

(4) Grooves are etched into the silicon around each of the desired regions from the back side of the wafer.

(5) In a two-step process, metal and oxide layers are deposited.

(6) Polycrystalline silicon is then grown over the entire back side of the wafer to a thickness approximating that of the original wafer.

(7) The top surface of the wafer is then lapped or etched down to expose each of the desired isolated regions.

(8) The wafer is then processed conventionally to form each of the desired devices.

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* C.G. Thornton, "The Application of New Metallurgical Technique to Silicon Integrated Circuits," presented at Electronic Devices Meeting, Washington, D.C., 1964.

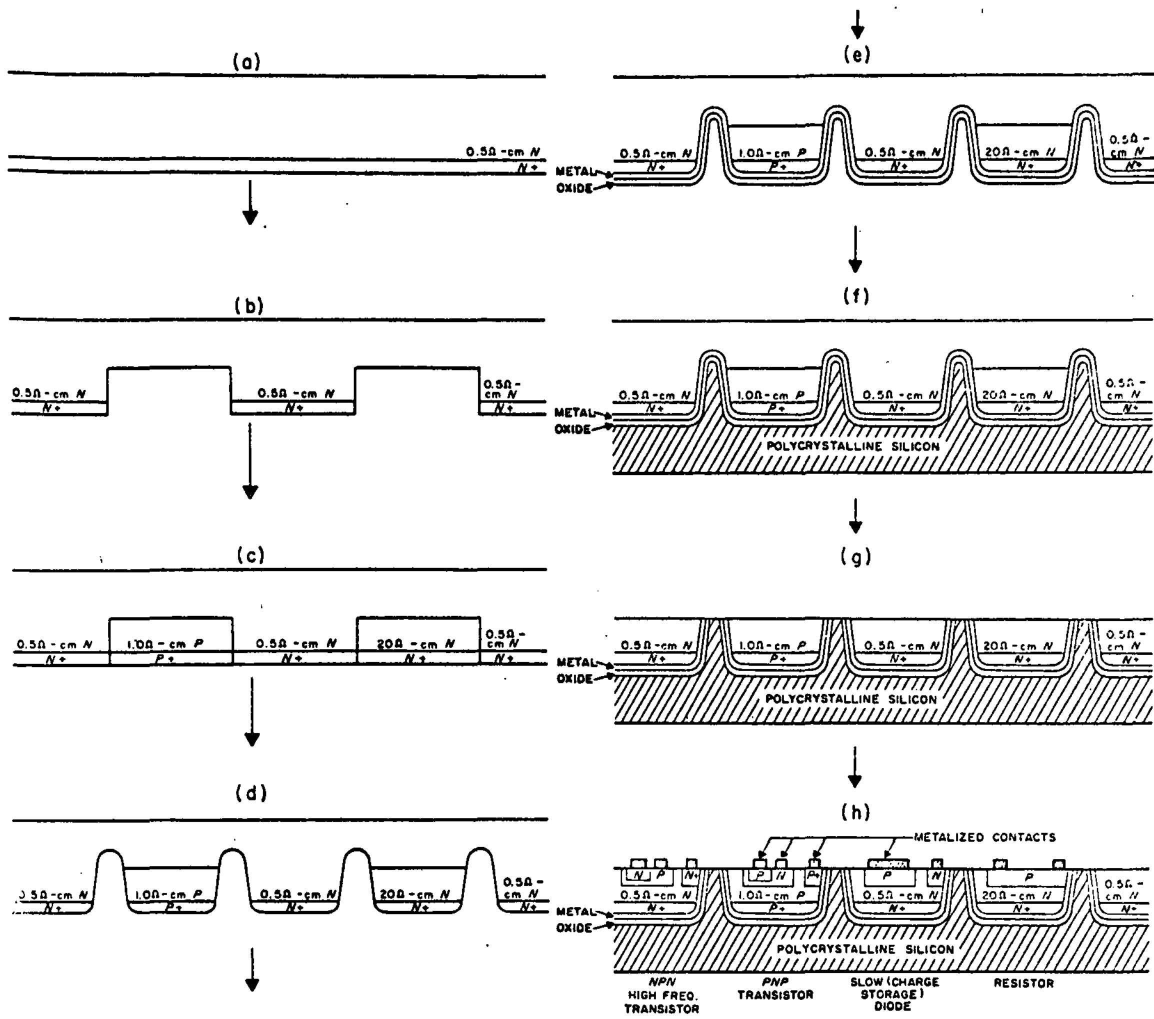

FIGURE 2-16

FLOW CHART FOR OPTIMIZED MICROCIRCUIT PROCESS

Prior to final metalization, gold is deposited through openings in the oxide in those regions where it is desired to reduce lifetime. A short heat treatment (approximately 1000°C for 15 minutes) is sufficient to distribute the gold throughout the desired regions.

The capacitance associated with oxide isolation is in the range of 0.02 pf/sq. mil per micron of oxide thickness. Thus a 5-micron-thick oxide reduces the capacitance coupling by a factor of 25 below that of p-n junctions that have a slight reverse bias.

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2.1.9 Specifying the Circuit

The design engineer can follow one of two approaches in microelectronic circuit design. In one approach he will keep current with and be experienced in the state of the art of monolithic circuit fabrication. He will then be in a position to give the circuit manufacturer detailed specifications on all components required to fabricate his circuit. The other approach is to provide the manufacturer with complete "black box" terminal specifications to which the final circuit must be manufactured and guaranteed.

Basic to both of these approaches is an understanding of the limits or boundary conditions that put constraints on the circuit design. One such constraint involves the fabrication technology itself. What types of devices can be fabricated on the same substrate? Table 2-1 is a monolithic compatibility chart which illustrates the possible combinations of devices on a single chip. It should be understood that the more complicated the circuit the more costly it will be to fabricate.

TABLE 2-1

MONOLITHIC COMPATIBILITY CHART

Devices	Signal		MOS-FET	Junction FET	Power Transistor	Matched Pairs*	Signal Diodes	Complementary
	NPN	PNP						
Signal NPN	-	Y	Y	Y	N	Y	Y	Y
Signal PNP	Y	-	Y	Y	N	Y	Y	Y
MOS-FET	Y	Y	-	Y	N	D	Y	D
Junction FET	Y	Y	Y	-	N	D	Y	N
Power Transistor	N	N	N	N	-	Y	Y	N
Signal Diodes	Y	Y	Y	Y	Y	Y	-	Y

Y - Yes
N - No
D - Difficult

*Useful matching is achievable for most devices; close matching of gain is difficult with any of the devices.

Microcircuits are fabricated in a variety of ways. Monolithic, hybrid, thin film, and thick film are some of the approaches. Generally, only monolithic silicon integrated circuits and some variation or hybrid of the monolithic form are considered here. The sheet resistance of monolithic circuits is limited to that associated with the base and emitter diffusions. This is necessary from a fabrication standpoint. The passive components are formed at the same time the transistor base or emitter is fabricated.

The hybrid offers a wider variation in sheet resistance than is possible with diffusion only. Thin film resistors are available for use with monolithic circuits in a wide range of sheet resistances. Diffused resistors above 300-400 ohms per square are not recommended for close tolerances, because of the change in value with the temperature associated with lead-bonding operations. Ranges of resistor values are given in Table 2-2.

TABLE 2-2

TYPICAL RESISTOR DATA FOR MONOLITHIC INTEGRATED CIRCUITS

Type	Range Ω	Ohms/Sq	TC PPM/°C
Diffused (Base)	100-30K	200	1500
Diffused (Emitter)	10-1K	2.5	100
Thin Film (Nichrome)	20-50K	40-400	100
MOS	4.5K at 10mA	--	500

Capacitors are either silicon-oxide (nonpolar with relatively high Q at high frequencies) for bypass and high-frequency tuning or junction type (low Q due to effective series resistance of the top contact) for bypass and voltage tuning. Typical characteristics are given in Table 2-3.

TABLE 2-3

TYPICAL CAPACITANCE DATA

Type	Range	Pf/Mil^2	Breakdown Voltage
SiO_2	2-200 pf	0.25	50V
Junction	2-500 pf	$\approx \frac{0.3}{\sqrt{V_R}}$	10V
MOS	2-200 pf	0.2	50V

The yield and, therefore, the cost of a circuit is more dependent on the area the circuit requires than on the number of components. In this respect it is wise to keep the circuit area to a minimum consistent with other requirements, such as component value and power requirements.

Area efficiency is a key factor with regard to capacitance. Large capacitors (500 to 10,000 pf) become progressively more expensive because of the area requirement. Values above 10,000 pf are not practical.

Though state-of-the-art monolithic transistors impose certain constraints, geometry nevertheless can be varied, and many combinations of transistor characteristics are possible. Typical characteristics of monolithic transistors are given in Table 2-4.

TABLE 2-4

MONOLITHIC TRANSISTOR CHARACTERISTICS

Characteristics	Emitter Dimensions In Mils			
	1x1-1/2	3x3	2x10	2x20
BV_{CBO}	← 35 Volts →			
BV_{CEO}	← 15 Volts →			
BV_{EBO}	← 7 Volts →			
$h_{FE/IC}$	40/100μA	40/1mA	40/2.5mA	25/2.5mA
$h_{FE/IC}$	80/5mA	60/10mA	50/50mA	50/50mA
ft (mc)	550	220	--	--
Collector-Base C (pf) at 6V	2	7	10	16.3
Emitter-Base C (pf) at 6V	2	5	10	16
Collector-Substrate C (pf) at 6V	4	10.5	10	17
R_{CS} (ohms)	70	120	35	27

Another constraint is imposed upon the designer by the fact that the inductance function per se is not available in the monolithic technology. If inductance is required, it is necessary to synthesize or design around it.*

2.1.10 Linear Amplifier Checklist**

The nine-point checklist given below is a handy guide for developing a conventional set of performance specifications for a final integrated circuit.

(1) Establish circuit specifications (specify black-box functions, establish environmental conditions and restrictions imposed on the design). A black-box specification† is illustrated in Table 2-5. It provides the guide for fabricating the circuit. The more complete and realistic the specification, the simpler it is to begin fabrication. For the design engineer who is not going to fabricate the circuit, this specification is all that is required providing he has not violated the constraints imposed by the technology.

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* V. Uzunoglu, "Six Possible Routes to Noninductive Tuned Circuitry", Electronics, 15 November 1965, p. 114.

** D.C. Bailey, "Converting Amplifiers to Integrated Circuit Format", EEE, February 1964, p. 70

† D. C. Bailey, "Black-Boxing Your Linear Integrated Circuit", Electronic Design, 22 June 1964, p. 74

TABLE 2-5

BLACK-BOX CHECKLIST

Environmental
- Operating-temperature range
- Storage-temperature range

Gain Specifications
- Frequency
- Source impedance
- Load impedance
- Power supply tolerance
- Open loop or gain setting
- Voltage gain, V_o/V_{in}
- Transconductance, $\Delta I_o/\Delta V_{in}$
- Current Gain, I_o/I_n
- Transresistance, $\Delta V_{in}/\Delta I_o$
- Gain stability (gain vs temperature)
- Gain linearity (gain vs signal level)

Bandwidth
- Source impedance
- Load impedance
- Power supply tolerance
- 3, 6, or 0 db points
- Open or closed loop (if closed loop, what gain)
- Frequency response
- Gain-bandwidth product
- f_t
- Cutoff frequencies
- Gain margin
- Phase margin
- Slope of gain vs frequency characteristics

Stability
- Temperature range
- Input-output conditions (capacitances and resistances)
- Expected life
- Maximum equivalent input drift (Voltage and/or current)
- DC stability
- AC stability
- Phase margin with maximum feedback
- Maximum output capacitance

Noise
- Frequency and bandwidth
- Source Resistance
- Noise figure (or equivalent input noise voltage)

Maximum Output (dc)
- Power supply voltage
- Load impedance
- Minimum linear output voltage
- Minimum linear output current
- Maximum output impedance

Input (dc)
- Minimum input impedance
- Differential mode
- Common mode
- Maximum common-mode voltage
- Minimum common-mode rejection ratio (specify frequency and common-mode voltage swing)

Dynamic Range (ac)
- Power supply voltage
- Load impedance
- Source impedance
- Maximum input before clipping
- Minimum unclipped output
- Dynamic range of input signal
- Minimum power output

Power Supply
- Output voltages
- Tolerances
- Ripple and noise
- Impedance vs. frequency
- Output power

Package
- Form factor (TO-5, flatpack)
- Environmental requirements
- Salt spray
- Leakage
- Linear acceleration
- Shock

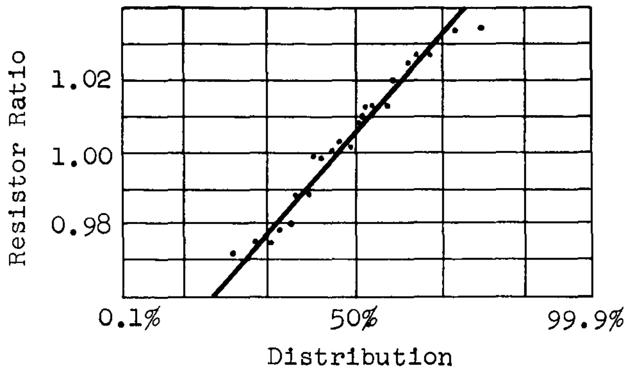

FIGURE 2-17

DISTRIBUTION OF RESISTOR RATIOS ON A MONOLITHIC STRUCTURE (SHEET RESISTANCE: 200 Ω/sq.)

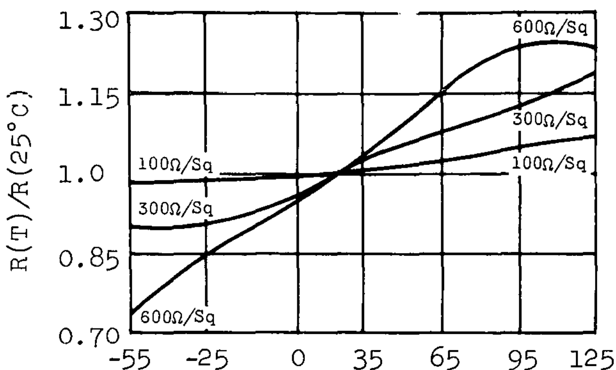

FIGURE 2-18

PERCENTAGE CHANGE OF RESISTANCE WITH TEMPERATURE FOR DIFFUSED RESISTORS WITH THREE VALUES OF SHEET RESISTANCE

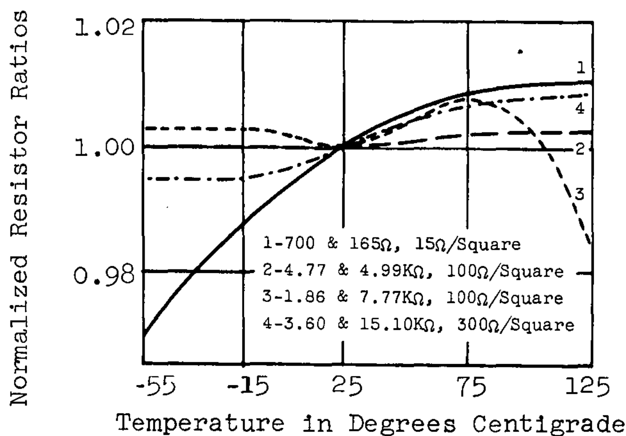

FIGURE 2-19

TRACKING ERROR OF DIFFUSED-RESISTOR RATIO FOR THREE DIFFERENT SHEET RESISTANCES (3 SEPARATE TAPPED CHIPS)

(2) Synthesize circuit configurations within the boundaries fixed by integrated-circuit technology. The active devices that can be used are found in Table 2-1. If inductance is required, a method must be determined to realize this function. Will an all-monolithic form be used or will hybrid techniques be required to give optimum performance?

(3) Establish an analysis method that utilizes measurable quantities in the final integrated circuit.

(4) Perform d-c analysis of the circuit. After the circuit has been synthesized, it must be analyzed from the standpoint of d-c stability. Much of this can be done by statistical methods, since the data on integrated-circuit elements are generally available in that form. The component values and their tolerances must be specified.

Figures 2-17, 2-18, and 2-19 are useful for d-c analysis. Resistor tolerances are normally wide and expensive to control or adjust to close values. However, resistance ratios are easily controlled and, if proper design is used, are frequently more important than the absolute values.

Integrated circuits have distributed parameters and parasitics associated with them. If possible, these characteristics should be employed as useful circuit elements.

(5) Breadboard the circuit, using discrete components. The circuit performance is compared with the

black-box specifications for performance. If the required performance levels are not achieved, the circuit can be modified or a different circuit approach can be synthesized. In some cases it may be necessary to repeat these steps several times to achieve the desired results.

(6) Draw a mask layout and compute the parasitics. These include resistance and capacitance interconnection parasitics, isolation parasitics, and substrate resistance. The calculated parasitic elements are inserted into the original breadboard in the form of discrete-equivalent lumped resistors and capacitors. Again circuit performance is measured and compared with blackbox specifications.

(7) Breadboard the circuit with integrated components. Compare the results with the black-box specifications. At this point it should be possible to determine if the specifications can be met with this particular design, although modifications may still be necessary before optimum results are achieved.

(8) Submit mask drawing for mask preparation. Include pin connections, lands, and spacing.

(9) Fabricate sample circuits and determine if they meet the required black-box specifications. Now the design can be optimized for the black-box specifications. Sometimes it becomes necessary to go through several process runs to achieve the desired distribution of electrical properties that best meet the original specifications.

2.1.11 Applications

Circuit analysis plays a major role in the design approach outlined above. The applications to follow use two techniques that have been found satisfactory. For d-c amplifiers a technique developed by Middlebrook* is used, and for high-frequency circuits a method proposed by Linvill** (which characterizes the integrated circuit as a black box with admittance parameters) is used.

Optimum analysis techniques have yet to be developed. The small-signal "nonlinear model" is more accurate at high frequencies because the two-pole alpha is included. Below a megacycle, capacitive parasitics can usually be neglected since small-geometry transistors will be used and since the passive parasitics present a negligible impedance at these frequencies. Resistive parasitics such

* R.D. Middlebrook, Differential Amplifiers, John Wiley and Sons, Inc., New York and London, 1963.

** J. G. Linvill and J. F. Gibbons, Transistors and Active Circuits, McGraw-Hill Book Co., Inc., New York, N.Y., 1961.

as the series collector resistance cannot be neglected. At low frequencies, series collector resistance can be lumped into the normal T-equivalent or small-signal nonlinear model.

2.1.11.1 D-C Amplifiers

An ideal d-c amplifier would have zero output with zero input; provide constant gain regardless of time, temperature, and input-level variations; provide an output that is a magnified replica of the input; and have an infinite bandwidth. To approach the ideal the following are needed: low noise figure, low equivalent-input offset voltage and drift, good linearity and dynamic range, gain stability with variations in temperature, and wide bandwidth.

Little information is available on integrated-circuit-type transistors, but indications are that noise figures are slightly greater than those of discrete types made by the diffusion process. With temperature variations, the noise figure becomes masked by internal d-c drift of the transistor.

Silicon diffused transistors exhibit a temperature coefficient of base-to-emitter voltage of about 2.3 mV/°C. In a single-transistor (unilateral) input stage, this coefficient is multiplied by the entire amplifier gain; thus to use such an amplifier for d-c amplification, temperature would have to be held constant, or it would be necessary to calibrate the amplifier with temperature. A better circuit configuration is the differential amplifier (Figure 2-20). Through canceling of the drift of one transistor with an equal and opposite drift of another, d-c drift can be reduced by several orders of magnitude.

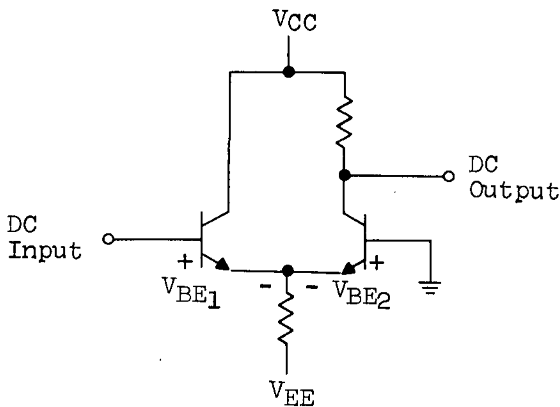

FIGURE 2-20
DIFFERENTIAL AMPLIFIER

A differential amplifier used as an input stage for a d-c amplifier helps reduce d-c drift. For a unilateral d-c amplifier, the performance of the discrete version and that of the integrated version are both subject to the d-c drift problem.

2.1.11.2 A-C Amplifiers

A well-known limitation of present integrated-circuit technology is its inability to produce inductors or large capacitors. Thus direct coupling should be used where possible. The following ground rules are recommended:

(1) Use a differential input stage.

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(2) Design for as much d-c gain as can be tolerated with the specified amount of drift in the first stage.

(3) If gain is insufficient, add a second d-c amplifier stage, using an external coupling capacitor.

(4) Use overall feedback for gain stability.

(5) Obtain high impedance (FET's will provide this if it cannot be achieved otherwise) to permit the use of smaller coupling capacitors.

Figure 2-21 illustrates the application of these principles. The differential amplifier permits a gain of about 100 with sufficiently low drift to maintain a reasonable dynamic range. With the FET stage, a large external resistor is needed, but the small capacitor required can be integrated.

High a-c gain and good d-c stability are obtained in the circuit of Figure 2-22. Here a large amount of d-c feedback provides d-c stability, and a small amount of a-c feedback results in high a-c gain. The amount of a-c feedback is controlled by external capacitor C_1 and resistor R_1 (if R_1 is zero, a-c gain is maximized).

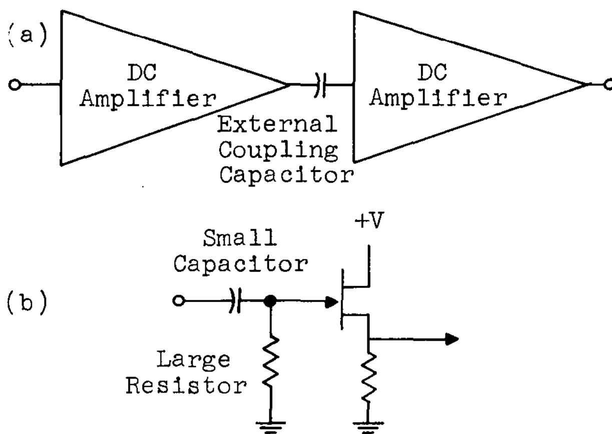

FIGURE 2-21
A-C AMPLIFIER TECHNIQUES

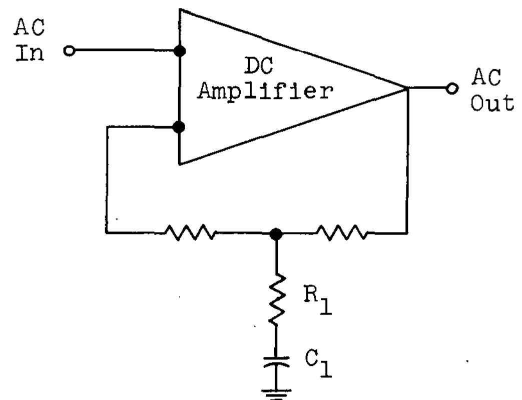

FIGURE 2-22
HIGH A-C GAIN, D-C STABLE CIRCUIT

2.1.11.3 Signal-Processing Circuits

A major goal in the servo-control field is the elimination of transformers. The integrated choppers, demodulators, and quadrature rejection circuits illustrated in this section should be examined with that in mind.

The two major factors in the design of choppers are offset current and voltage, and drift. (Offset causes an output in the absence of an input, and drift produces a change in output with time and temperature.) The inverter transistor connection reduces both offset and drift.

Figure 2-23 shows how even lower offsets can be achieved. Here the drift is determined by tracking of the transistor characteristics with temperature and time, and by the difference in junction temperature between the two units. Cancellation of offset is achieved by equal and opposite offset of another device. The integrated version has an obvious advantage over the discrete version since the transistors will be matched and and operating with small differences in temperature.

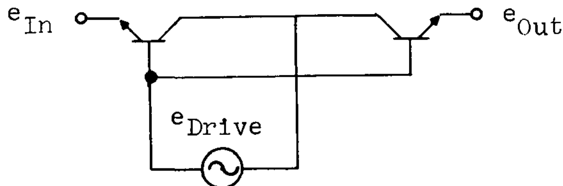

FIGURE 2-23
BASIC CHOPPER CIRCUIT

Offsets and drifts of standard integrated circuit pairs (Figure 2-24) in the inverted chopper connection average 50 µV offset and 1 µV/°C drift. Figure 2-24(a) shows two transistors diffused into a single die; and Figure 2-24(a) shows two emitters diffused into a single collector-base junction area, which provide even tighter control of drift and offset. Double-emitter devices have been reported to have offsets under 20 µV and drifts less than 0.2 µV/°C.

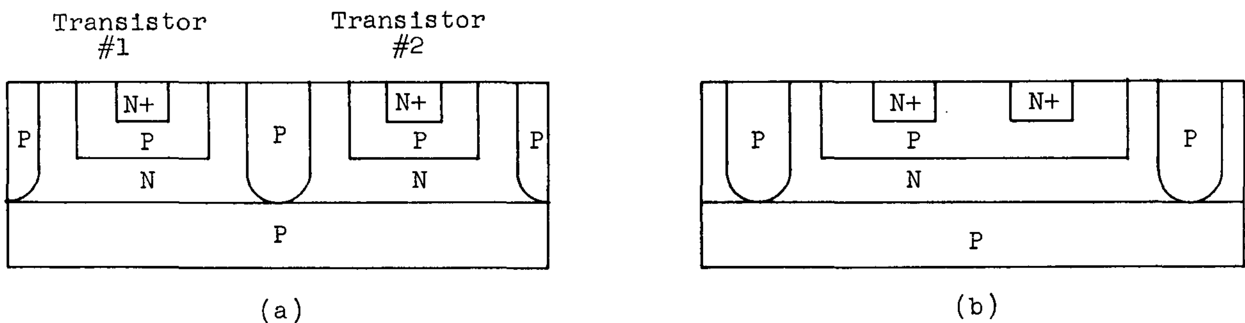

FIGURE 2-24
STANDARD CHOPPER CONFIGURATIONS

2.1.11.4 Demodulators

Although demodulators vary widely in configuration, only diode-quad types are discussed here.

In discrete diode-quad bilateral switches, the usual procedure is to select diodes in quads or pairs to achieve low offsets. Offsets from 10 mv down to 1 mv (with successively poorer yields) are typical. In integrated circuits, two diodes

can be diffused side by side into the same silicon substrate. An n-on-p diffused pair can be connected to a p-on-n pair to form a bridge (Figure 2-25). The p-on-n

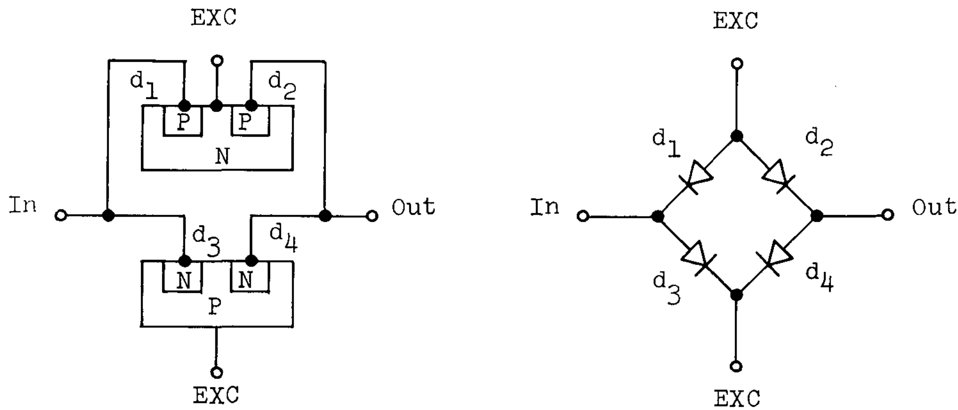

FIGURE 2-25
DIODE-QUAD SWITCH CONSTRUCTION

pair should match and track, as should the n-on-p pair. Figure 2-26 shows a diode quad in a demodulator. Quadrature rejection is accomplished by controlling the conduction angle. The d-c output is the average value of the in-phase sine wave. At that time the quadrature signal is passing through zero. The output will be zero for quadrature signals and nearly equal to the peak magnitude for in-phase (o°) signals. A paralleled R and C is used to achieve a peak-conducting circuit.

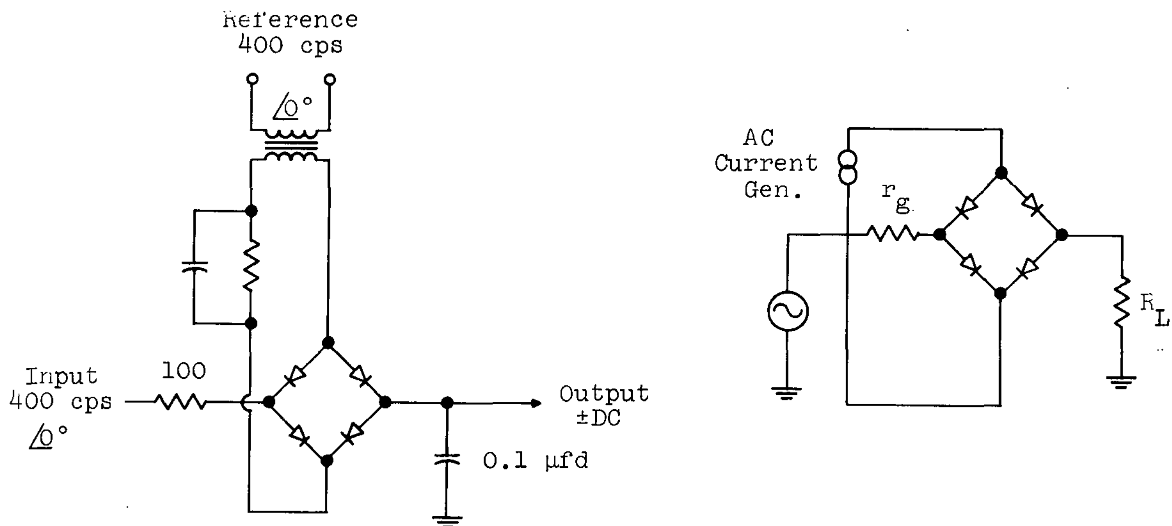

FIGURE 2-26
DIODE-QUAD DEMODULATOR AND EQUIVALENT CIRCUIT

A transformerless version of the demodulator is shown in Figure 2-27. In this version, the isolation property of the transformer is approached by use of the high output-impedance of the common-base connection. When Q_1 and Q_2 are cut off, the impedance is essentially infinite. When Q_1 and Q_2 conduct, the drive

nodes of the bridge are connected to the current generators with the output impedance of Q_1 and Q_2 across them (it is above 500 KΩ at low frequencies).

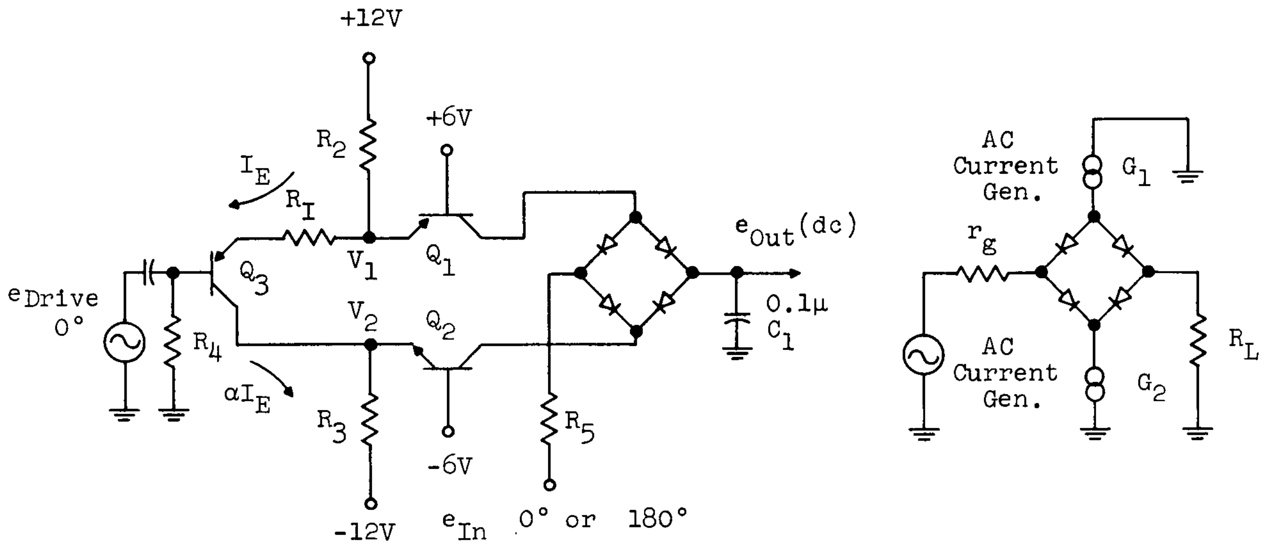

FIGURE 2-27

TRANSFORMERLESS VERSION OF DEMODULATOR SHOWN IN FIGURE 2-26

The demodulator functions of the transformer and transformerless circuits are essentially the same. In the transformerless version, the bridge conducts for 30 to 50 degrees about the peaks of the cycle, causing C_1 to charge up to the average value of the peaks of the input signal through R_5. When the drive circuit cuts off, C_1 holds the charge until the next half cycle. The output is a bipolar d-c voltage, corresponding to the zero and 180-degree input signals. Another transformerless demodulator is shown in Figure 2-28.

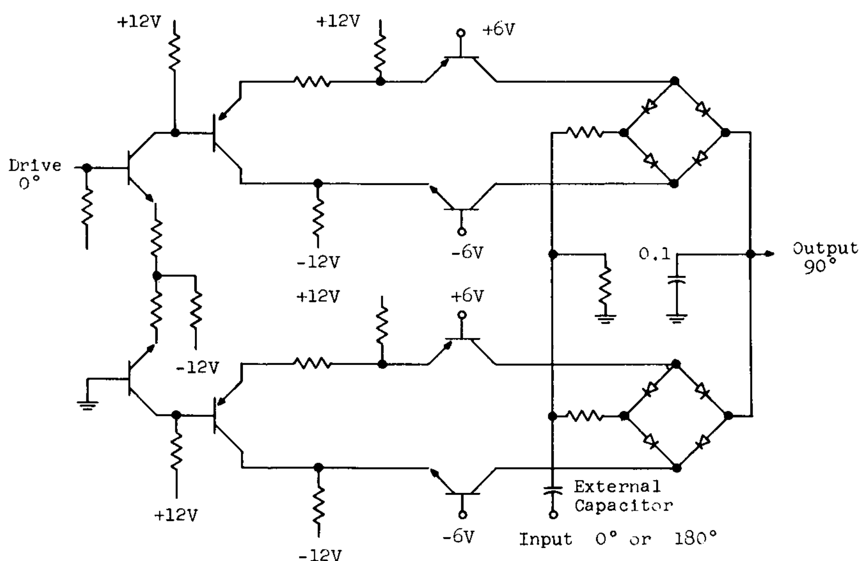

FIGURE 2-28

TRANSFORMERLESS QUADRATURE REJECTION DEMODULATOR

2.1.11.5 Communication Circuits

R-f and i-f amplifiers, mixers, oscillators, and multipliers with good performances over a wide range of frequencies can be designed and fabricated in integrated-circuit form. Monolithic integrated circuits can often match the performance of discrete versions up to about 10 MHz. Above this, parasitics begin to play a significant role.

For monolithic r-f circuits, it is recommended that impedances be kept low or that resistive isolation techniques be used. Vhf and uhf circuits are not yet practical in monolithic form. At these frequencies it is often desirable to separate the individual circuit elements on a high-frequency dielectric (e.g., ceramic), as in hybrid circuits.

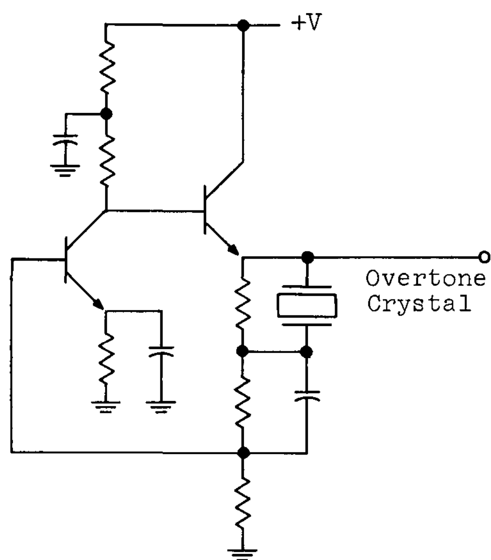

FIGURE 2-29
OVERTONE CRYSTAL OSCILLATOR

Again, it is desirable to eliminate chokes and transformers. Figure 2-29 shows an overtone crystal oscillator without inductors. It can provide a frequency stability better than 0.005% from 0°C to 50°C. Naturally, the crystal is not included in this monolithic integrated circuit.

2.1.11.6 Digital Circuit

While design of digital circuits is similar to that of analog circuits, there are differences in the particulars of the design. Some of the more important digital characteristic are as follows:

(1) Fan-in, (2) Fan-out, (3) Noise immunity (4) Propagation delay, and (5) Best logic type for a particular application. Design factors that must be considered before determining the desired diffusion profiles and mask layout include the following: (1) Reliability, (2) Fan-out, (3) Temperature range, (4) Switching speed, (5) Noise immunity, (6) Power dissipation, and (7) Production yield. Often a design that is best for one parameter acts to degrade another; for example, high switching speeds are not compatible with large fan-out and low power.

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In setting the specifications for the circuit it is necessary to determine the following:

(1) The type of transistor required, which includes setting the diffusion profiles and determining the geometrical layout

(2) The center values of the resistor

(3) The tolerance on transistor and resistor parameters

To determine these values it is necessary to state the basic black-box objectives of the digital circuit.

The following example* will serve to illustrate some of the important design considerations for digital circuits. The electrical equivalent circuit for this example is illustrated in Figure 2-30. It is a three-input, modified direct-coupled transistor-logic (DCTLO NOR gate. Logic 0 is approximately +0.2V, and logic 1, +0.8V. A pulse at inputs 1, 3, or 5, or any combination of them, will drive one or more of the transistors into saturation and produce a 0 at output pin 7.

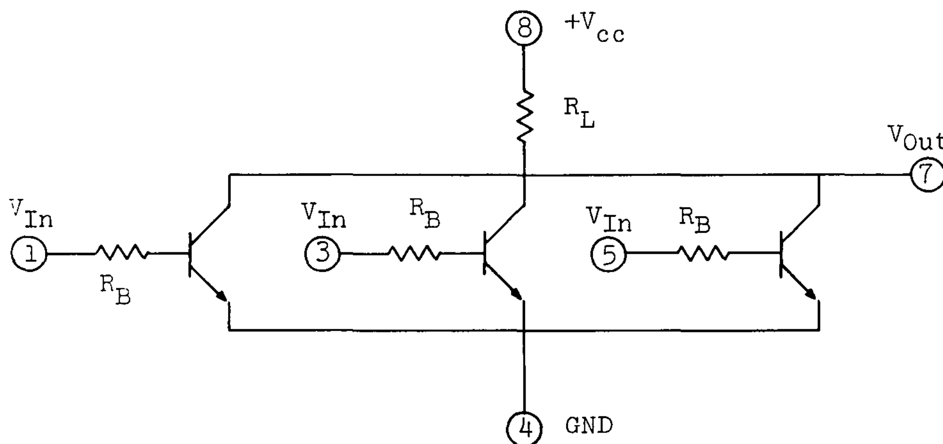

FIGURE 2-30
MODIFIED DCTL NOR GATE

External Black-Box Parameters		Internal "Device" Parameters	
Fan-in	= 3	Load Resistance R_L	≈ 600 ohms
Fan-out	≥ 5	Base Resistance R_B	≈ 400 ohms
Power Dissipation	≤ 15mW	Saturation Resistance	≈ 40 ohms
Operating Voltage	≈ 3 V	Current Gain h_{FE}	> 20
Noise Immunity	≥ 0.3V	h_{FE} Peak at Ic	≈ 5mA
Maximum Supply Voltage	≤ 10V	Frequency Cutoff f_T	≈ 500 MHz
Propagation Delay	≤ 25 nsec	Saturation Voltage V_{BE}	≈ 0.7V
Operating Temperature Range	-55 to +125C	Saturation Voltage V_{CE}	< 0.25V
		Base Sheet Resistance P_S	≈ 100 ohm/sq

*L. B. Valdes, "Case History: Integrating a NOR Circuit" Electronic Design 2 March 1964.

The noise-immunity objective requires that when a transistor is locked in saturation, a 0.3 V signal superimposed on the output voltage will not turn on the transistor in the next circuit system (assuming that one NOR gate drives another). Ideally, the integrated circuit should be designed with V_{CE} sat as low as possible.

A minimum value of load resistance, R_L, can be obtained from the power-dissipation requirements; 15 mW at 3 V gives a maximum current consumption of 5 mA.

Thus

$$R_L \text{ min} \approx \frac{3.0 - V_{ce\ sat}}{0.005} \approx 530 \text{ ohms} \tag{2-23}$$

If diffusion control limits the load resistance to ± 15%, the center value of R_L is set at 620 ohms. An upper value is approximately 720 ohms.

This calculation also tells us that in a typical case a transistor in saturation is at I_c = 5 mA. For maximum fan-out it would be desirable to have the transistor in saturation with the base current I_B as small as possible. Thus a transistor with a large value of h_{FE} is wanted. The curve of h_{FE} vs. I_c should also peak at I_c = 5 mA. From switching-speed considerations (maximum propagation delay of 25 nsec) it is also known that a fast transistor will be needed, one with an f_T of at least 500 MH_z.

Choosing the proper value of R_B is somewhat more complicated. If R_B is small, the transistors will draw too much base current from the previous stage. This not only limits the fan-out of each gate, but may lead to "current-hogging", which can be illustrated with the aid of Figure 2-31. Current available from Gate A is limited to a maximum value given as:

$$I_{avail} = \frac{V_{cc} - V_{in}}{R_L} \tag{2-24}$$

This gate drives five others, which have slightly different input characteristics. Gate B1 has the lowest $V_{BE\ sat}$ of the group, and B5 has the highest. Thus it may happen that Gates B1 through B4 draw so much I_B that virtually all the available current is directed into these four gates and there is not enough left to turn on Gate B5; the first four gates have "hogged" the available current.

Most silicon transistors are in saturation at I_C/I_B = 10 or $I_B \approx 0.5$ mA. At this point, $V_{BE\ sat} \approx 0.7$ v, and it is evident that too much series voltage drop cannot be added across R_B. If this series voltage drop is arbitrarily

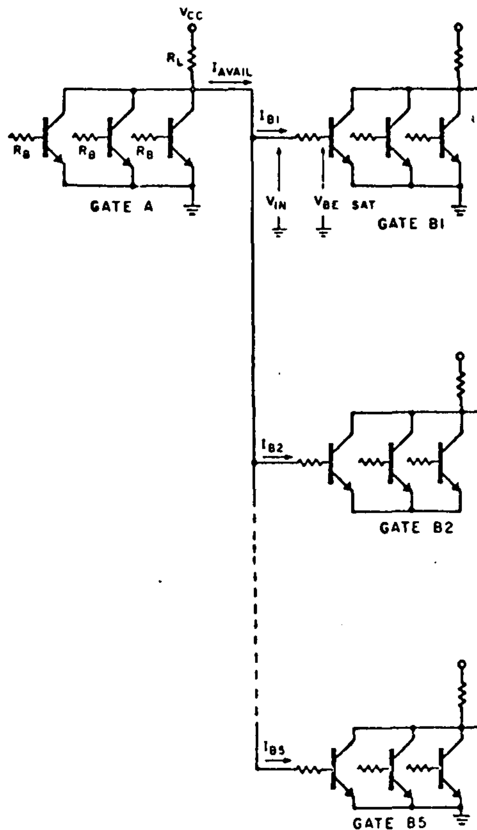

FIGURE 2-31

REPRESENTATION OF NOR GATE A DRIVING FIVE LOADS (GATES B1 TO B5)

chosen as 0.2 V, the result is R_B = 400 ohms. Figure 2-32 illustrates what happens if two transistors are paralleled, one with V_{BE} sat = 0.7 V and the other with $V_{BE\ sat}$ = 0.8 V. The input current is only 0.25 mA to the second transistor, but it remains in saturation as long as h_{FE} is greater than 20.

The actual selection of R_B = 400 ohms was made after a "worst-case" analysis of the circuit. It is obviously not sufficient to consider the various requirements independently. It is necessary to examine what happens when all component parts of the integrated circuit are at their worst possible values, and to consider the variation of these parameters with temperature. In addition, the transient characteristics of the device must be examined, together with all the parasitic terms that are an integral part of every integrated circuit.

The desired electrical characteristics can be satisfied with a transistor having the geometrical layout of Figure 2-33. This unit has a base width of 0.8 μ and enough gold doping to produce a storage time of 20 nsec. It has been designed to minimize transverse voltage drop in the collector region and obtain a saturation resistance of less than 40 ohms.

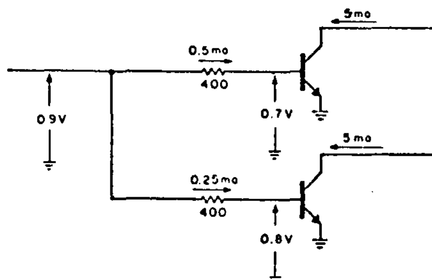

FIGURE 2-32

EFFECT OF DIFFERENT $V_{BE_{sat}}$ VALUES ON NOR GATE CIRCUITS DRIVEN IN PARALLEL

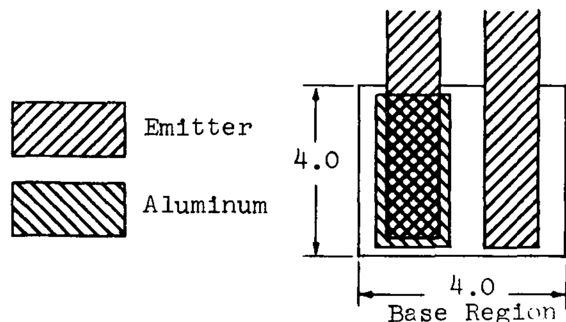

FIGURE 2-33

TOP VIEW OF EMITTER AND BASE REGION OF TRANSISTOR USED IN AN INTEGRATED CIRCUIT

A heavily doped n+ region has been diffused around three-fourths of the base region, reducing the possibility of channeling..

The load resistor R_L and input base resistors R_B are produced by use of the same p-type diffusions as for the base of the transistor. As explained earlier, their values are adjusted by controlling the ratio of length ℓ to width w of the resistor pattern and using the equation

$$R = \rho_s \frac{\ell}{w} \tag{2-25}$$

where the sheet resistivity, ρ_s, is of the order of 100 ohm/square.

The fact that the resistors are at a more positive potential in the circuit than the transistors requires that they be placed in separately isolated n-type regions. Figure 2-34 is a cross-section of the circuit, showing one transistor and one resistor.

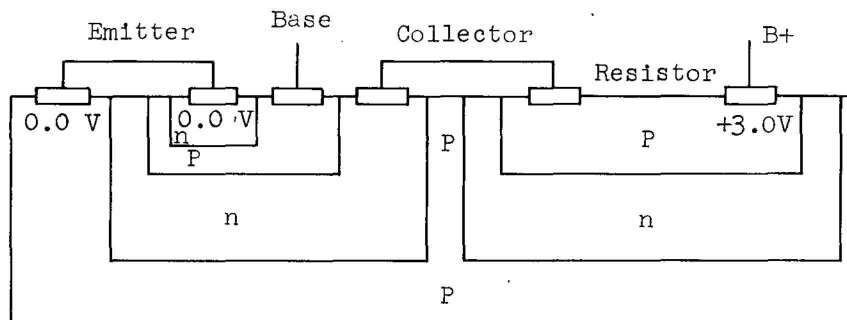

FIGURE 2-34

CROSS-SECTIONAL VIEW OF AN INTEGRATED CIRCUIT
SHOWING ONLY ONE TRANSISTOR AND THE LOAD RESISTOR

The measured characteristics of two devices constructed from the foregoing information are given in Table 2-6. Two saturation voltage tests were performed: one with 0.825 V applied to the input, and a second with 1.5 V. The output voltage, V_o (for the light saturation condition), illustrates the ability of the transistor to turn on at a prescribed signal level.

The hard-saturation voltage condition provides a measure of the ability of the circuit to handle a large input signal. It is also used to ascertain that there are no parasitic elements limiting the operating of the device. For example, there may be a parasitic clamping diode between the input

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terminal and the substrate, which would tend to lift the output voltage as the input voltage is increased.

The output current is measured with 0.55 V applied to all three transistors. This is a "worst-case" condition. It should be noted that if one of the transistors turns on too soon (at V_{BE} = 0.55), the current through R_L will be diverted through such a transistor rather than going through the output terminal and into the next circuit. Early turn-on of a transistor is also characterized by the value of I_{CEX}.

The fan-out of the NOR gate is theoretically the ratio of the minimum output current divided by the maximum input base current -- in this case, 2.9/0.37 = 8.

TABLE 2-6

MEASURED PARAMETER VALUES FOR NOR CIRCUIT

Parameter	Value	Unit
Base Input Current I_B (0.825 V applied to input)	370	μa max
Output Voltage V_O (0.825 V applied to input)	300	mv max
Saturation Voltage V_B (1.5 V applied to input)	250	mv max
Output Current I_O (output at 0.825 V)	2.9	ma min
Threshold Current I_{CEX} (input at 0.55 V, output at 1 V)	200	μa max

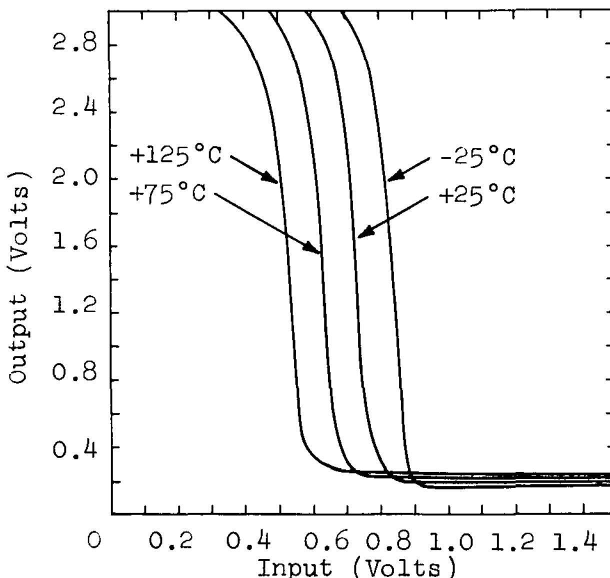

FIGURE 2-35
OUTPUT VOLTAGE VS INPUT VOLTAGE

Figure 2-35 shows the output voltage vs input voltage of a typical gate. These curves can be used to determine the noise immunity of the gate. Take the highest temperature (+125C curve), or worst-case, condition. The gate turns on at approximately V_{BE} = 0.55 V. If V_{CE} sat < 0.25V, the required 0.3-V noise immunity is achieved at maximum operating temperature.

The temperature variations of some of the other significant gate parameters are illustrated in Figures 2-36 through 2-38. The propagation delay is defined in the test circuit illustrated in Figure 2-39; it is the average of the turn-off time t_1 and the turn-on time t_2. Both of these are measured at the 50% point in the input waveform A and the output waveform B.

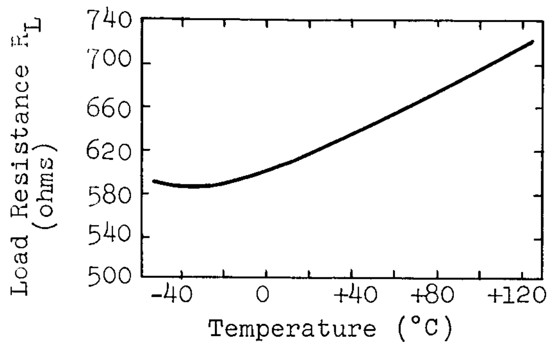

FIGURE 2-36

EFFECT OF TEMPERATURE
ON THE LOAD RESISTANCE R_i

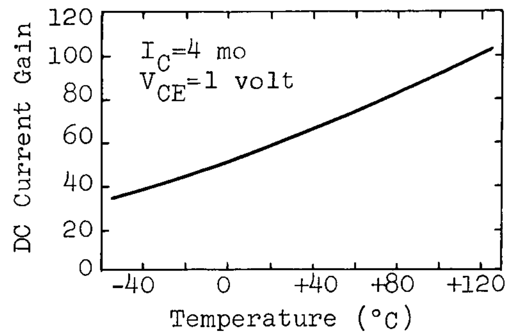

FIGURE 2-37

EFFECT OF TEMPERATURE ON
THE CURRENT GAIN OF AN
INTEGRATED CIRCUIT TRANSISTOR

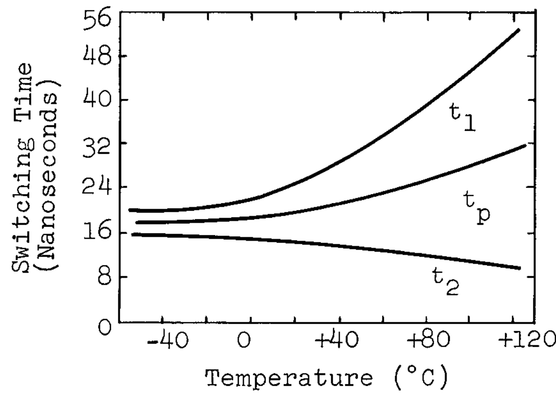

FIGURE 2-38

SWITCHING TIMES t_1 AND t_2 AND
PROPAGATION DELAY t_p

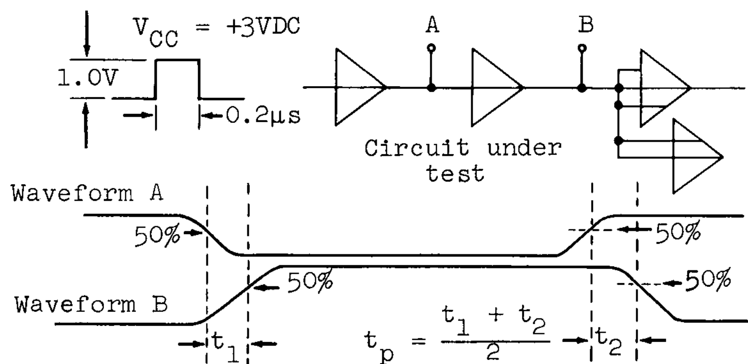

FIGURE 2-39

CIRCUIT USED FOR THE MEASUREMENT OF
PROPAGATION DELAY t_p

2.2 MOS Field-Effect Devices

The metal-oxide-semiconductor (MOS) field-effect transistor (FET) uses an electric field applied through an insulated gate electrode to modulate the conductance of a channel layer in the semiconductor under the gate electrode. The channel consists of a lightly doped region contained between two highly doped regions called the "source" and "drain". The conductuance of the channel is dependent upon the intensity of the field and hence the voltage applied to the gate electrode. Most MOS transistors now available are fabricated on a silicon substrate. The insulating oxide is silicon-dioxide. (Some results of using silicon-nitride as the insulator have been published.) The MOS has high input resistance (>10^{15} ohms), and at high frequencies the input impedance becomes highly capacitive. Unlike the junction transistor, which is a current-controlled device, the MOS is voltage- or charge-controlled.

There are two basic types of MOS devices: enhancement and depletion. Each of these types can be fabricated so that either electrons or holes are the majority carriers. Thus four distinct types of MOS transistors exist. These are listed in Table 2-7, with associated bias-voltage requirements.

TABLE 2-7

CHARACTERISTICS OF FOUR BASIC TYPES OF MOS DEVICES

MOS Type	Symbol	Gate-to-Source Voltage to Cutoff	Incremental Gate-to-Source Voltage to Increase Conduction	Normal Drain-to-Source Voltage	Normal Substrate-to-Source Voltage
N-Channel Depletion	G, D, SS, S	Negative	Positive	Positive	Zero or Negative
N-Channel Enhancement	G, D, SS, S	Zero	Positive	Positive	Zero or Negative
P-Channel Depletion	G, D, SS, S	Positive	Negative	Negative	Zero or Positive
P-Channel Enhancement	G, D, SS, S	Zero	Negative	Negative	Zero or Positive

G - Gate S - Source D - Drain SS - Substrate

2.2.1 N-Channel Enhancement MOS

The majority carriers are electrons in the N-channel enhancement transistor. A positive voltage (with respect to the source) applied at the gate induces a positive potential in the oxide at the oxide-semiconductor surface. This in turn attracts electrons to the semiconductor surface, and these carriers form the transistor's induced channel. An enhancement-type transistor structure is shown in Figure 2-40.

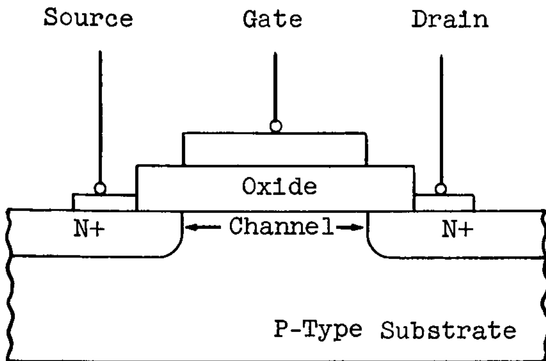

FIGURE 2-40

N-CHANNEL ENHANCEMENT MOS

At zero gate voltage there is only a very small current flow ($\approx 10^{-9}$ amps) between source and drain. Since there is no gate voltage, there are no free carriers in the space between the two N+ regions. The current that does flow is that of the reverse-biased junction formed by the P-type substrate and the N+ drain region.

When a positive voltage is applied to the gate electrode, minority carriers (electrons) are attracted from the P-region to the surface to form the channel. The surface has an excess of holes (empty valence states) since it is originally P-type, and as the electrons are drawn to the surface of the P-region underneath the oxide, these empty states are filled. Therefore, a gate voltage is reached at which there are just enough electrons to fill the empty valence states. At this value of gate voltage the channel is intrinsic. For further increases in gate voltage the channel becomes N-type. When this happens, the surface is referred to as "inverted." Figure 2-41 is an illustration of the drain current as a function of drain voltage for an enhancement field-effect transistor. Because of the nature of surface states, surfaces change easily from P-type to N-type, which makes it quite difficult to fabricate the enhancement FET; they have a tendency to become depletion-type devices. The surface resistivity must be kept low to prevent the channel from forming when there is no gate bias.

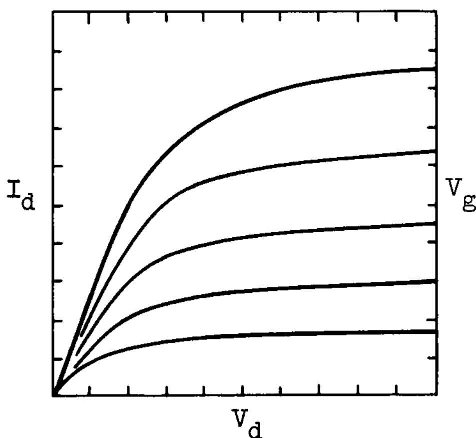

FIGURE 2-41

DRAIN CURRENT VS DRAIN VOLTAGE
Vertical: 1mA per division
Horizontal: 2V per division

2.2.2 P-Channel Enhancement MOS

The P-channel enhancement MOS utilizes holes as the majority carriers. The substrate is N-type, and the induced channel

is P-type. The drain and source regions are P+, and the drain-to-source voltage is negative. The channel is induced by application of a negative gate-to-source bias. The drain current as a function of drain and gate voltage is similar to that shown in Figure 2-41 except that all the voltages are reversed.

The metalized gate electrode shown in Figure 2-40 covers the entire channel region. It is characteristic of the enhancement-type transistor that the gate electrode overlaps both source and drain N+ regions. This is necessary to prevent a high resistance from appearing in series with the source and drain, since no carriers would be attracted into that part of the channel not included in the gate electric field.

This geometry, however, results in a large capacitance from gate to drain and gate to source. The exact value depends on the degree of overlap and the thickness of the oxide. The thicker the oxide the smaller the capacitance value; yet, for sensitivity, the oxide must be thin enough to provide high gate fields for reasonably small gate voltages. To meet these opposite demands, the oxide is usually made thin over the channel and thick over the N+ regions (P+ regions for P-channel devices), as shown in Figure 2-42. Also illustrated is the effect of gate voltage on carriers for both P- and N-types.

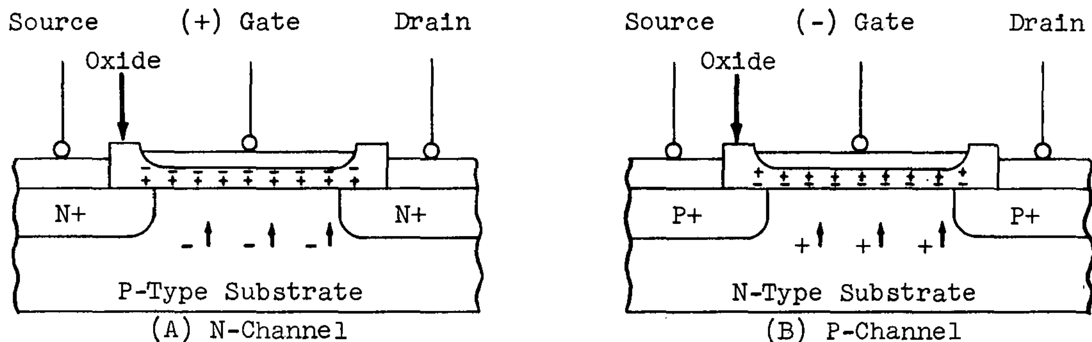

FIGURE 2-42

OXIDE THICKNESS AND CHARGE ON ENHANCEMENT MOS TRANSISTOR

2.2.3 N-Channel Depletion MOS

The depletion-type MOS is illustrated in Figure 2-43. The channel for this device is formed at the time when the oxide is fabricated on the surface. The degree of doping for the channel depends on the saturation current desired at zero gate voltage. The current that flows with zero gate voltage is higher in the depletion-type device since the channel exists at all voltages. The drain

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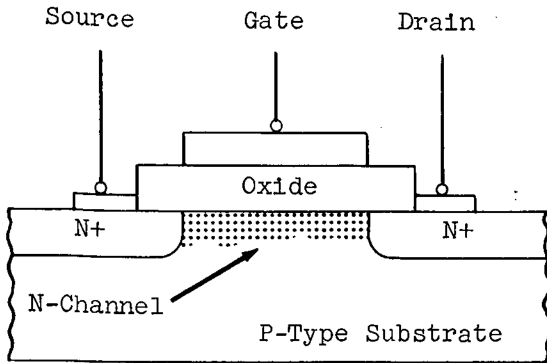

FIGURE 2-43

DEPLETION-TYPE MOS

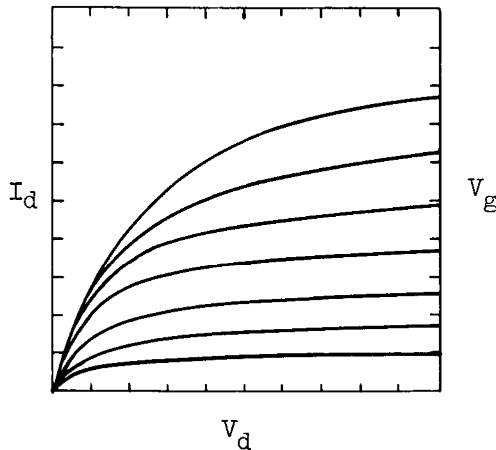

FIGURE 2-44

DRAIN CURRENT VS DRAIN VOLTAGE
Vertical: 2mA per division
Horizontal: 5V per division

current as a function of drain voltage is illustrated in Figure 2-44 for an N-channel depletion MOS transistor.

This device operates for negative as well as positive bias on the gate. It is unique in its applications and can be considered as operating either in the depletion mode or in the enhancement mode.

Operation in the depletion mode requires a negative gate-to-source bias. As the gate bias is made more negative, the channel is depleted of electrons because of the electric field induced in the oxide. The field at the oxide-semiconductor interface is positive and repels the electrons from the surface. The result is a decrease in current as a result of the decreasing conductance of the channel.

2.2.4 <u>P-Channel Depletion MOS</u>

The geometry for the P-channel is the same as that of the N-channel depletion MOS. The majority carriers, however, are holes. This device has all the characteristics of the N-channel except that all voltages are reversed.

The channel is not as highly doped as the drain and source regions. Because of the relatively high free-carrier concentration in the channel, it is not necessary that the gate electrode overlap the drain. This is referred to as "gate off-set". A small series resistance will be induced in the channel at the drain when the transistor is operated in the enhancement mode. The only effect this has on device operation is to increase the drain voltage at which current saturation occurs. The gate electrode does overlap the source. If it did not, the series resistance associated with the source would introduce degenerative feedback, which would have deleterious effects on device gain. The gate off-set significantly reduces the gate-to-drain feedback capacitance.

The two basic MOS structures are illustrated in Figure 2-45. These basic structures were first proposed by D. Kahng and M. M. Atalla.*

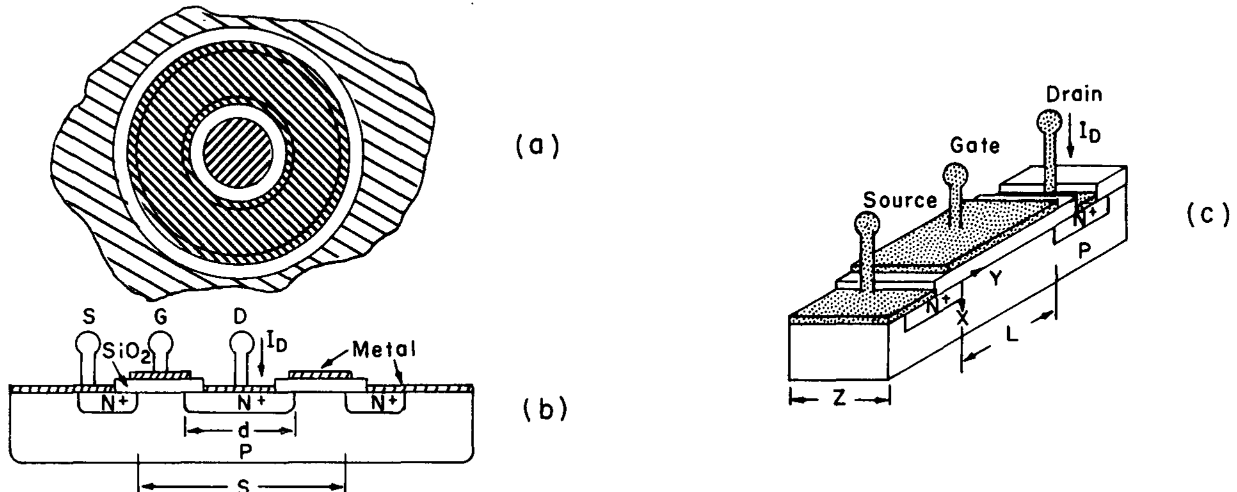

FIGURE 2-45

GEOMETRY OF N-CHANNEL MOS TRANSISTORS. (a) TOP VIEW.
(b) CROSS-SECTIONAL VIEW. (c) THE LINEAR STRUCTURE.

The N+ regions of the structure shown in Figure 2-45 are obtained by high-temperature diffusion of phosphorus impurity into the P-type silicon substrate by the use of oxide masking techniques.** The N+ region used as the source can be internally connected to the P-type substrate when the source electrode is fabricated. If it is not, the device is a four-terminal device, with the substrate acting as the fourth terminal. The other N+ region is the drain and is usually employed as the output terminal. The source acts as the common terminal for the input and output.

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*U.S. Patent No. 3102230, "Electrical Field Controlled Semiconductor Devices", filed 31 May 1960 and issued on 27 August 1963 to D. Hahng; and U. S. Patent No. 3056888, "Semiconductor Triode", filed 17 August 1960 and issued on 2 October 1962 to M. M. Atalla. Some of the materials covered in these two patents were presented at the IRE-AIEE Solid State Device Research Cong., Pittsburgh, Pa.; June 1960 by these authors in "Silicon-Silicon Dioxide Field Induced Surface Devices".

**For a comprehensive review of the silicon planar technology developments see G. E. Moore, "Semiconductor Integrated Circuits," Chapter 5 of the "Principle of Microelectronic Engineering", E. Keonjian, Ed., McGraw-Hill Book Co., Inc. New York, New York, 1962.

The input lead, called the gate, is evaporated over the oxide. In this particular structure the oxide is silicon dioxide. However, work is currently being done with silicon nitride as the insulator. The SiO_2 layer is a determining factor of device characteristics and stability.

The oxide insulator can be grown thermally at high temperature or anodically at room temperature. Oxide thickness of the order of 1000 Å is generally used. Thick oxide reduces the transconductance, gain, and speed of the device for a given d-c operating point; and very thin oxide makes the reproducibility of the device difficult.* The metal gate electrode and the metal electrodes that form the ohmic contacts to the source and drain regions are made by evaporation and photoresist techniques. Metals such as aluminum, silver, and gold are used.

The linear structure illustrated in Figure 2-45c is well suited for integrated circuit work. It is easy to interconnect the devices, and there is a natural isolation between devices on the same substrate.

2.2.5 Drain Current

The equation for drain current is derived by Sah* as:

$$I_D = \frac{\bar{\mu}_n C_o}{L^2} \left[(V_G - V_T) \; V_D - \frac{V_D^2}{2} \right] \tag{2-26}$$

where

I_D = drain current

V_G = gate-to-source voltage

V_D = drain-to-source voltage

V_T = the turn-on voltage if it is positive or turn-off voltage if it is negative

C_o = the total capacitance of the oxide layer under the gate

L = the channel length as indicated in Figure 2-45c

$\bar{\mu}_n$ = average surface mobility of electrons in the channel

Equation 2-26 is based on a simplified model of the channel and is valid only for gradual channels; it ceases to be a good approximation in the region of the channel where it is pinched-off or nearly pinched off.

*C. T. Sah "Characteristics of the Metal-Oxide-Semiconductor Transistors" IEEE Trans. ED, July 1964 p. 324-345.

If V_T in equation 2-26 is positive and V_G is zero, the current will be negative. This cannot be the case in practice. What is indicated here is that V_G must be larger than V_T in order to have current flow in the channel; thus we are dealing with an enhancement transistor. This is easily seen in Figure 2-46, which illustrates the transfer characteristic of an enhancement MOS transistor.

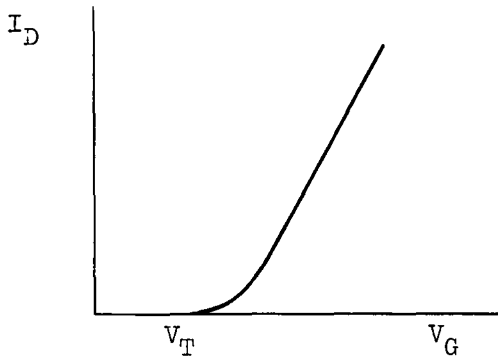


FIGURE 2-46

TRANSFER CHARACTERISTIC OF ENHANCEMENT MOS TRANSISTOR

From Figure 2-46 it can be seen that current does not flow until some value of gate voltage (V_T) is applied between gate and source. This is the voltage required to invert the channel discussed in Section 2.2.1. Current will not flow in the channel until the gate voltage exceeds the transistor turn-on voltage. The determining factor in the magnitude of V_T is the oxide thickness. For thin oxides, V_T is lower than for thicker oxides.

If V_T is negative, Equation 1 indicates a current at zero gate voltage. This is the case for the depletion-type transistors. The transfer characteristic for an N-channel depletion transistor is illustrated in Figure 2-47.

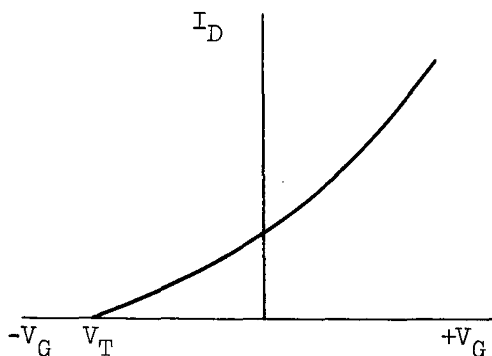


FIGURE 2-47

TRANSFER CHARACTERISTIC FOR DEPLETION MOS TRANSISTOR

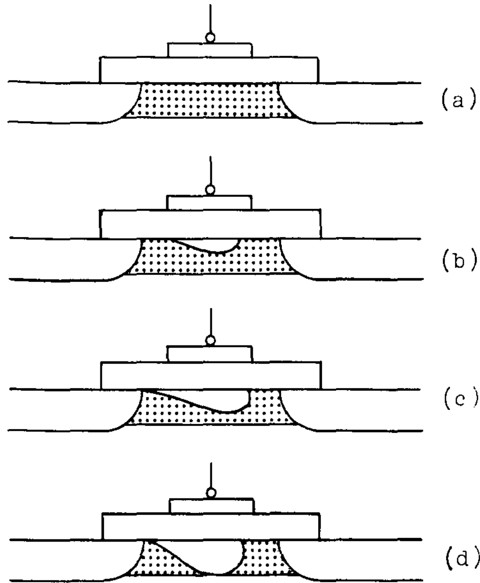
Note that for $V_G = 0$ in Figure 2-47, there is substantial drain current. In this case V_T is the voltage required to turn off the drain current.

2.2.6 Pinch-off

Equation 2-26 indicates a linear current-voltage relationship for the MOS. This is true only in the ohmic region of the V_D - I_D characteristic. As the drain voltage is increased beyond some value (assuming constant V_G), drain-current saturation takes place. At this point, the channel is in "pinch-off." This is the pentode region of the V_D - I_D characteristic.

The gradual pinch-off of the channel of an N-type depletion MOS is illustrated

in Figure 2-48. Assume that the gate electrode is shorted to the source ($V_G = 0$). For zero applied drain voltage the channel is unconstricted, as is shown in Figure 2-48a. As the drain voltage is increased from zero in a positive direction, current begins to flow in the channel. This is point (b) on the curve of Figure 2-48e.



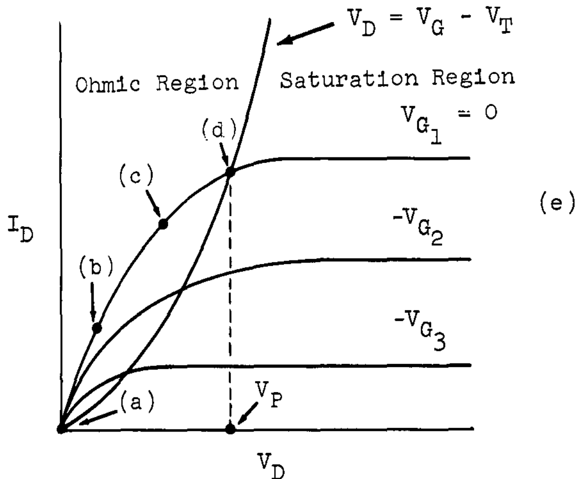


FIGURE 2-48

PINCH-OFF FOR DEPLETION MOS TRANSISTOR

The applied voltage is dropped across the channel, and the effect is to reverse-bias the gate electrode relative to the channel. Since the channel resistance is distributed, the voltage is distributed along the channel and the most negative area is that closest to the drain. The result is an induced depletion region in the channel, with the greatest depletion occurring closest to the drain, as is indicated in Figure 2-48b.

As the drain voltage is increased to correspond to point (c) on the curve of Figure 2-48c, the depletion region is further enlarged. At point (d) the drain voltage equals the pinch-off voltage, and drain current saturation takes place. At this point it is assumed that the depletion region extends across the channel. There is only a slight increase in drain current for further increases in drain voltage.

From Figure 2-48e it can be seen that the drain current can be divided into two segments: that which appears in the ohmic region and that which appears in the saturation region. These regions are divided by the locus of points determined by

$$V_D = V_G - V_T$$

For values of $V_G - V_T < V_D$ Equation 2-26 is valid. However, in the saturation region, where $V_G - V_T \geq V_D$, this equation is no longer valid; the gradual-channel approximation fails. This condition corresponds approximately to the condition of maximum drain current from Equation 2-26 and can be obtained from it as follows:

If we set $$\left(\frac{\delta I_D}{\delta V_D}\right)_{V_G} = 0$$ and use Equation 2-26, (2-27)

the pinch-off condition is

$$V_D = V_{DS} = V_G - V_T \tag{2-28}$$

where V_{DS} is the drain voltage at saturation.

The drain current at the pinch-off condition is given by

$$I_{DS} = \frac{\mu_n C_0}{2L^2}\left(V_G - V_T\right)^2 = \frac{\bar{\mu}_n C_0}{2L^2} V_{DS}^2 \tag{2-29}$$

If the drain voltage is further increased beyond the pinch-off voltage given by Equation 2-28, the pinch-off region lengthens into the channel. Most of the additional voltage applied to the drain beyond the pinch-off voltage appears across the length of the pinch-off region and causes little increase in the drain current.

In the saturation region the channel is said to be pinched off. Yet a constant current is being conducted from source to drain. In this region space-charge-dominated currents* are generated in the drain area. This type of current flow differs from ohmic current flow since the channel drift field now controls the distribution of mobile charge as well as the charge velocity. It is analogous in this sense to space-charge current flow in conventional vacuum tubes, where the plate-to-cathode field gradient determines the space charge.

2.2.7 Determining V_T

A rapid experimental determination of the threshold voltage V_T can be obtained from two terminal characteristics. The gate electrode is connected directly to the drain for the enhancement-mode N-channel device which has $V_T > 0$ and no built-in channel. For the depletion-mode N-channel device a battery $V_{GG} > |V_T|$ (positive side tied to the drain) is used that has a sufficiently high voltage to pinch off the built-in channel.

*G.T. Wright, Proceedings of the IEEE, Volume 51, p. 1642, 1963.

In these connections, the device is in the saturation region since $V_D = V_G + V_{GG} > V_{DS} = V_G - V_T$. Thus the two-terminal drain current can be obtained from Equation 2-29 by the use of Equation 2-28:

$$I_{DS} = (\bar{\mu}_n C_o / 2L^2) \cdot (V_D - V_{GG} - V_T)^2, \qquad (2\text{-}30)$$

which shows that the onset of the drain current corresponds to a drain voltage of $(V_T + V_{GG})$. For devices of the enhancement type, the turn-off voltage V_T can be determined readily from a display of this characteristic without the use of a gate battery since $V_T > 0$. For the depletion type, $V_T < 0$; and a gate battery of $V_{GG} > |V_T|$ must be used to determine the turn-on voltage V_T. This slight additional complication comes from the fact that an N-channel MOS transistor, which has a P-type substrate, cannot be biased with a large negative drain voltage, since then the drain junction would be forward-biased and the large forward-drain junction current would mask off the pinch-off point.

2.2.8 Determining the g_d and g_m

The low-frequency values of g_d, the drain conductance below saturation, can be determined from Equation 2-31.

$$g_d = \left(\frac{\delta I_D}{\delta V_D}\right)_{V_G} = \frac{\bar{\mu}_n C_o}{L^2} (V_G - V_T - V_D), \qquad (2\text{-}31)$$

Thus g_d decreases linearly with drain voltage and becomes zero at saturation, where $V_D = V_{DS} = V_G - V_T$.

The transconductance (g_m) is

$$g_m = \left(\frac{I_D}{V_G}\right) V_D = \frac{\bar{\mu}_n C_o}{L^2} V_D \qquad (2\text{-}32)$$

and its maximum, which occurs at saturation, is given by

$$g_{ms} = \frac{\bar{\mu}_n C_o}{L^2} V_{DS} = \frac{\bar{\mu}_n C_o}{L^2} \left(V_G - V_T\right) \qquad (2\text{-}33)$$

Since $(V_G - V_T) = V_{DS}$ in the saturation region, one can use Equation 2-29, substitute into Equation 2-32, and rearrange such that

$$g_{ms} = \sqrt{\frac{2 I_{DS} \bar{\mu}_n C_o}{L^2}} \qquad (2\text{-}34)$$

The value of transconductance in Equation 2-34 is also approximately the value of transductance when the device is operated beyond the saturation voltage.

2.2.9 Frequency Limitations of an MOS Device

The upper frequency limit of an MOS device depends on τ, the transit time of a carrier from source to drain. The transit time is a function of device channel length (L), the surface mobility (μ), and the applied voltage from drain to source. The equation for transit time is

$$\tau = \frac{L^2}{\mu V_{DS}} \tag{2-35}$$

The intrinsic gain-bandwidth product for the MOS is

$$GBW = \frac{g_m}{2\pi C_c} \tag{2-36}$$

where g_m is the device transconductance and C_c is the active gate-to-channel capacitance (in saturation $C_c = 2/3\ C_o$). The gain-bandwidth product is directly related to the carrier transit time as

$$GBW = \frac{1}{2\pi\tau} \tag{2-37}$$

In actual practice the upper frequency limit may be substantially lower than $1/2\pi\tau$. For a 10-micron channel, the upper frequency limit will be several hundred megacycles per second.

2.2.10 Equivalent Circuit of the MOS

An equivalent circuit of the MOS is illustrated in Figure 2-49.* The equivalent circuit is composed of six resistors, five capacitors, a constant-current source, and two diodes.

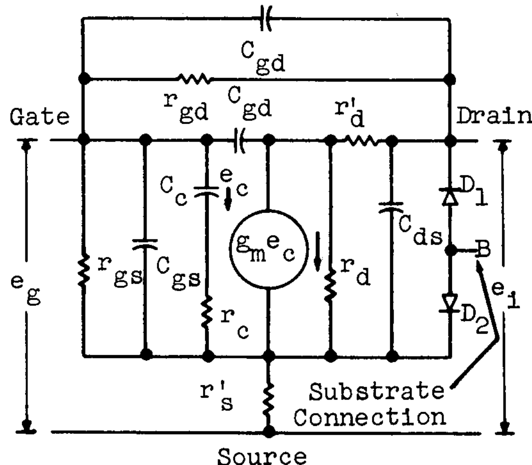


FIGURE 2-49

EQUIVALENT CIRCUIT FOR MOS FET OPERATING IN THE PINCH-OFF REGION

Resistance r_{gs} represents the leakage from gate to source, and r_{gd} is the leakage from gate to drain. These values are very high, typically about 10^{15} ohms.

The series network formed by C_c and r_c is a lumped approximation of the distributed network of the active channel. The capacitance C_c is the sum of the small capacitors distributed over the active channel area; it is expressed as

$$C_c = \frac{\partial Q_c}{\partial V_g} \tag{2-38}$$

where Q_c is the total channel charge. C_c is usually a function of the applied

*D. M. Griswold, "Understanding and Using the MOSFET", Electronics, December 14, 1964, p 66.

gate and drain voltage. In saturation, this simplifies to:

$$C_c = \frac{2}{3} A_c C_{ox} \tag{2-39}$$

where A_c is the gate area overlying the active channel and C_{ox} is the oxide capacitance per unit area. Typically, oxide thickness T_{ox} = 1000 angstroms, so that $C_{ox} = 10^{-8}$ Farads/Cm^2.

The capacitance C_c charges and discharges through the channel resistance r_c. The channel resistance, in turn, is composed of innumerable series and parallel resistors between the source, or drain, and the points in the channel where the individual channel-to-gate capacitances take effect. The high-frequency performance of the MOS is strongly dependent on the r_c C_c time constant.

When the MOS is operated in the saturation region, it appears as a constant current source. For this reason the active portion of the circuit is depicted as a constant current source with a value of $g_m e_c$. The low frequency value of g_m can be obtained from the V_D - I_D characteristic as

$$g_m = \left.\frac{\Delta I_D}{\Delta E_g}\right|_{V_D} \tag{2-40}$$

Resistance r_d in parallel with the current generator, $g_m e_c$, represents the dynamic output resistance of the transistor. It can be determined by the slope of the output characteristics as

$$r_d = \left.\frac{\Delta V_D}{\Delta I_D}\right|_{V_{sG}} \tag{2-41}$$

In the pinch-off region, r_d is several orders of magnitude larger than any parasitic resistances. The parasitic resistances appear in series with the source and at the drain.

Resistances r_d' and r_s' represent those portions of the source-to-drain channel which are not controlled by the transistor's gate. These parasitic resistances are mostly caused by the metal-to-semiconductor contact of the source and drain regions. However, when the gate electrode is offset from the drain (depletion-mode transistor), that portion of the channel resistance not under the gate electrode is included in r_d'.

The only effect of r_d' is to shift the value of the external drain voltage required to obtain drain current saturation. However, r_s' appears as a common element to the input and output circuit and therefore induces degenerative feedback. It lowers the external terminal transconductance, g_m, which is expressed as

$$g_m = \frac{g_{mo}}{1 + r_s' \, g_{mo}} \tag{2-42}$$

where g_{mo} is the internal transconductance. To keep r'_s as small as possible, the gate electrode always overlaps the N+ source contact.

Capacitances C_{gd}, C_{ds}, and C_{gs} are the physical case and interlead capacitances between gate and drain, gate and source, and drain and source. Capacitances C_{gd} and C_{gs} also include any capacitances that are not dependent on voltage, such as that contributed by the physical overlap of the insulated gate over the source or drain. C_{gd} is reduced significantly when gate off-set is used for depletion-mode devices. Capacitance C_{ds} includes the capacitances of D_1 and D_2.

Capacitance C'_{gd} represents the intrinsic gate-to-drain capacitance, which decreases as the channel voltage approaches the pinch-off region. This capacitor is quite significant since it determines the degree to which drain-current saturation is achieved.

Diode D_1 represents the junction formed between the N+ drain region and the semiconductor substrate; D_2 is the junction formed between the N+ source region and the substrate. D_1 and D_2 are back-to-back diodes in parallel with the channel. At high frequencies the diodes contribute an equivalent series RC network that affects the output admittance.

2.2.11 Amplifier Circuits

There are three basic single-stage circuit configurations in which the MOS is used. Each has its advantages in a particular application.

2.2.11.1 Common-Source

The common-source configuration is illustrated in Figure 2-50a. The signal is applied between gate and source. This circuit has a high input impedance and a medium-to-high output impedance. The circuit provides a voltage gain greater than unity, which is given by

$$A = -\frac{g_m r_d R_L}{r_d + R_L} \qquad (2\text{-}43)$$

where g_m is the transconductance, r_d is the drain resistance, R_L is the effective load resistance, and the minus sign indicates the phase reversal from input to output. If an unbypassed resistance is introduced between the source and ground as shown in Figure 2-50a, degenerative feedback is induced in the circuit. The common-source voltage gain A' with an unbypassed source source resistor is

$$A' = \frac{g_m\ r_d\ R_L}{r_d + (g_m\ r_d + 1)\ R_s + R_L} \qquad (2\text{-}44)$$

where R_s is the unbypassed source resistance. The output impedance, Z_o, is increased by the unbypassed resistor:

$$Z_o = r_d + (g_m\ r_d + 1)\ R_s \qquad (2\text{-}45)$$

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2.2.11.2 Common-drain Circuit

This circuit arrangement, illustrated in Figure 2-50b is sometimes referred to as a "source follower." The input impedance is very high, but the output impedance is low. There is no phase reversal between input and output. The distortion is low, and the voltage gain is less than unity.

This circuit finds application where an impedance transformation from high to low is required and where low input capacitance is desirable. The input is injected between gate and drain, and the output is taken between source and drain. This circuit provides 100% degenerative feedback. Its gain is given by

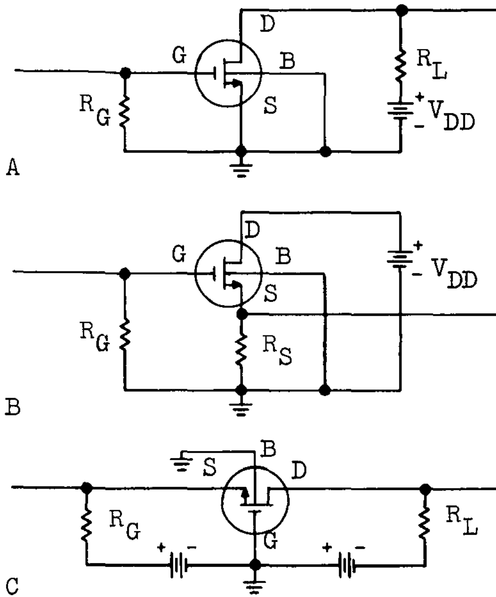
$$A' = \frac{R_S}{\left(\frac{\mu + 1}{\mu}\right) R_s + \frac{1}{gm}} \qquad (2\text{-}46)$$

Since the amplification factor, μ, is usually much greater than unity, this reduces to

$$A' \approx \frac{1}{1 + \frac{+1}{g_m R_S}} \qquad (2\text{-}47)$$

The input resistance is R_G when R_G is connected to ground. If R_G is returned to the source contact of the MOS, the input resistance R_i is given by

$$R_i = \frac{R_G}{(1 - A')} \qquad (2\text{-}48)$$



B=Bulk Gate
D=Drain
G=Control Gate
S=Source

R_G=Gate Resistor
R_S=Source Resistor

FIGURE 2-50

THE THREE BASIC AMPLIFIER CONFIGURATIONS FOR A FET;
(A) COMMON-SOURCE OPERATION
(B) SOURCE-FOLLOWER OPERATION
(C) COMMON-GATE-OPERATION

If the load is resistive, the input capacitance of the source follower is reduced by the negative feedback:

$$C_i = C_{gd} + (1 - A')C_{gs} \qquad (2\text{-}49)$$

The output resistance is given by

$$R_o = \frac{r_d\ R_s}{(g_m\ r_d + 1)\ R_s + r_d} \qquad (2\text{-}50)$$

Since $\mu = g_m\ r_d$ and is usually much greater than unity,

$$R_o \approx \frac{1}{g_m + G_s} \qquad (2\text{-}51)$$

where

$$G_s = \frac{1}{R_s}$$

2.2.11.3 Common-Gate Circuit

The common-gate circuit (Figure 2-50a) is used to transform from a low to a high impedance. The input impedance of this configuration has approximately the same value as the output impedance of the source-follower circuit. The gain is given by:

$$A = \frac{(g_m\ r_d + 1)\ R_L}{(g_m\ r_d + 1)\ R_G + r_d + R_L} \qquad (2\text{-}52)$$

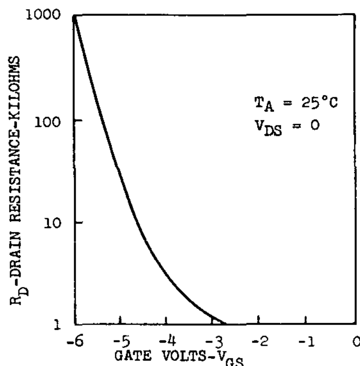


FIGURE 2-51

DRAIN RESISTANCE CHARACTERISTICS

2.2.12 Variable Resistor

The MOS can be used as a variable resistor or voltage-controlled attenuator. A variation in gate voltage causes the drain-to-source resistance to vary. Within a certain range of gate voltage this resistance change is linear. Figure 2-51 is an illustration of the variation of drain resistance with gate voltage. For high negative voltage the characteristic is linear and the range is from 5K to 1M ohm.

2.2.13 Switching Times

For switching applications, such as the inverter circuit shown in Figure 2-52, the switching times consist of both the time constant of charging and discharging the channel and the time constant associated with load resistance, R_L, and capacitance, C'_d. This capacitance, C'_d, consists of the drain-junction capacitance and the stray capacitance of the device header and package and associated circuit wiring. During the turn-on transient, the time constant for charging the channel dominates over $R_LC'_d$, while during the turn-off transient, $R_LC'_d$ dominates.

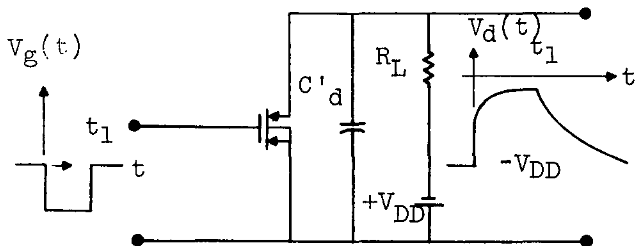


FIGURE 2-52

SWITCHING TRANSIENTS IN A P-CHANNEL MOS TRANSISTOR INVERTER CIRCUIT

Consider the turn-on transient as illustrated in Figure 2-52 for a P-channel device without a built-in channel. The device is initially in the off state, with a negative drain voltage, V_{DD}, and zero gate voltage. At t = 0, a negative gate voltage is applied which is sufficient to induce a hole channel and cause holes to flow down the drain from the source and discharge the capacitance C'_d, which is initially charged up to a charge of $-V_{DD}$. If the time constant, $R_LC'_d$, is large compared with the time constant of the channel, the discharge time of C'_d is essentially the time constant of the channel since during this time the

*C. T. Sah, op. cit.

build-up of charge on C'_d by the load current flowing through R_L from the V_{DD} battery is negligible. The channel time constant is an intrinsic property of a given device and depends on the device geometry and material properties.

This time constant is the transit time of the electrons across an N-type channel for the case of constant electron mobility and is the same as Equation 2-35:

$$\tau = \frac{L^2}{\mu V_{DS}} \tag{2-53}$$

From this equation it is seen that the channel time constant decreases slightly as the drain voltage is increased beyond V_{DS}. If the value of $V_{DS} = \dfrac{2L\mu I_{DS}}{\mu\ C_c}$ (where C_c is the total effective gate capacitance, which equals 2/3 C_o in saturation) is substituted into Equation 2-53 the following expression for the channel time constant is obtained:

$$\tau = \frac{L^2 C_c}{2\mu\ I_{DS}} = \frac{C_c V_{DS}}{I_{DS}} \tag{2-54}$$

A numerical example will illustrate the contributions from various sources on the switching time of the turn-on transient. For a P-channel MOS transistor switch, the following numerical values are typical: channel length, L, 10 microns; channel width, Z, 250 microns; bulk resistivity, 10 ohm-cm corresponding to a donor impurity concentration of 4×10^{14} atoms/cm^3; average surface mobility of holes, 100 cm^2/v-sec; oxide thickness, X_o, 1000Å. The total gate capacitance (C_o) is given as

$$C_o = \frac{K_o\ \epsilon_o\ Z\ L}{X_o}$$

where

K_o = dielectric constant of the oxide (≈ 4.0)

ϵ_o = permissitivity of free space (8.85×10^{-14} farad/cm)

$$C_o = \frac{[4.0\ (8.85)\ 10^{-14}\ (250)\ 10^{-4}\ (10)\ 10^{-4}]}{1000 \times 10^{-8}}$$

$$= 0.885 \times 10^{-12} \text{ farads}$$

$$= 0.885 \text{ pf}$$

In the saturation region the effective gate-to-channel capacitance is

$$C_o = 2/3\ C_o$$

Therefore, C_c = 0.590 pf.

Assuming that the device is switched on by a gate voltage to a steady-state drain current in the saturation region of $I_D = I_{DS}$ = 10 ma, then the saturation drain voltage can be calculated from Equation 2-29 as

$$V_{DS} = \sqrt{\frac{2L^2 \, I_{DS}}{\mu_p \, C_o}} = \sqrt{\frac{2 10^{-6}(10^{-2})}{(10^2)(0.885)10^{-12}}}$$

$$V_{DS} = 15$$

and

$$\tau = \frac{C_c \, V_{DS}}{I_{DS}} = \frac{0.590 \times 10^{-12} \times 15}{10^{-2}}$$

$$= 885 \times 10^{-12} \text{sec.}$$

This is the value of the electron transit time or the charging and discharging time of the channel for the given conditions. The gain-bandwidth product for such a device is

$$GBW = \frac{1}{2\pi\tau}$$

$$= \frac{1}{(6.28)(885)10^{-12}}$$

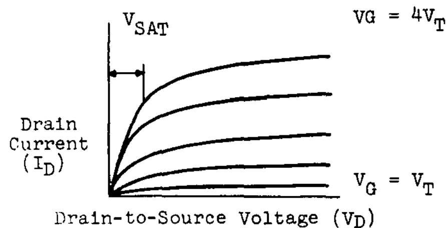
$$GBW = 180 \text{ Mc}$$

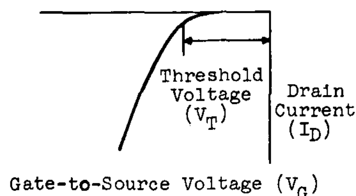
Let us compare the channel time constant with $R_L \, C'_d$. Assume R_L = 1000 ohms. The capacitance associated with the drain-to-substrate is about 0.1 pf in a typical device. The drain lead capacitance through the header is about 0.5 pf for a TO-5 package. Other stray capacitance associated with the circuit wiring may be as high as 3 pf. Assuming 3 pf, it can be determined that $R_L \, C'_d = 3000 \times 10^{-12}$ sec, which is considerably greater than the channel time constant of 885×10^{-12} sec. The turn-on time constant is determined by the transit time.

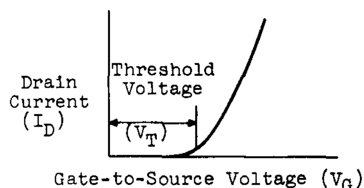
However, the relative importance of the circuit and channel time constants is reversed during the turn-off transient. The drain-voltage transient decreases toward $-V_{DD}$ (see Figure 2-52) more slowly since the capacitance C'_d must be charged up to $-V_{DD}$ through R_L. Thus the turn-off time constant is approximately $R_L C'_d = 3000 \times 10^{-12}$ sec. If the circuit time constant is comparable to the transit time, the total switch-off time constant would then be given approximately by the sum of these two time constants. The total switching time (turn-on plus turn-off) is limited by the circuit rather than the device.

2.2.14 Switching Applications

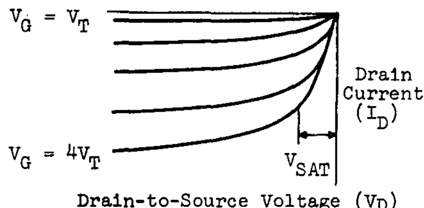
The enhancement-type transistor is well suited for digital circuit applications because direct-coupled signal inversion is possible with no need for level shifting between stages. Characteristics of the devices that are important in this application are illustrated in Figure 2-53, which displays the output and transfer characteristics of both N-type and P-type enhancement-mode MOS transistors. Of particular importance is the fact that the saturation voltage ($V_{D \, Sat}$) is less than the threshold voltage (V_T); this characteristic of MOS devices enables the circuit designer to construct extremely simple direct-coupled logic circuits.







Transfer and output characteristics for a typical p-channel enhancement-type MOS device.



Transfer and output characteristics for a typical p-channel enhancement-type MOS device.

FIGURE 2-53

MOS DIGITAL CIRCUIT*

2.2.15 MOS Digital Circuits*

The potential advantages of MOS devices in integrated digital arrays can be realized only if proper consideration is given to circuit choice. Although many circuit configurations are possible, only one or two take advantage of the unique properties of MOS devices to achieve a high figure of merit of functional complexity per unit at high yield. Before logic and storage circuits are discussed, four possible MOS inverter circuits will be considered. Each will be evaluated for application in an integrated circuit, not as a circuit constructed from discrete components.

To simplify the discussion and to use only positive voltages, it is assumed that all the examples shown for single-channel MOS circuits use N-channel devices. If all voltages are reversed, the same results can be achieved with P-channel devices. In fact, P-channel arrays, because of their somewhat simpler processing, are more common than N-channel arrays at present.

Figure 2-54 shows an inverter that uses an MOS inverting transistor and a resistor. In integrated form, this circuit is a very poor choice. For small MOS structures, a high value of resistance is required (greater than 10,000 ohms). If the resistor is formed by the source and drain diffusion, it occupies too large an area. If a separate diffusion is used, or if the resistor is formed as a thin film over the oxide, the processing is increased in complexity. In either case, the figure of merit for the circuit is reduced.

*R. D. Lohman, "Applications of MOS FET's in Microelectronics", SCP and Solid State Technology, March 1966.

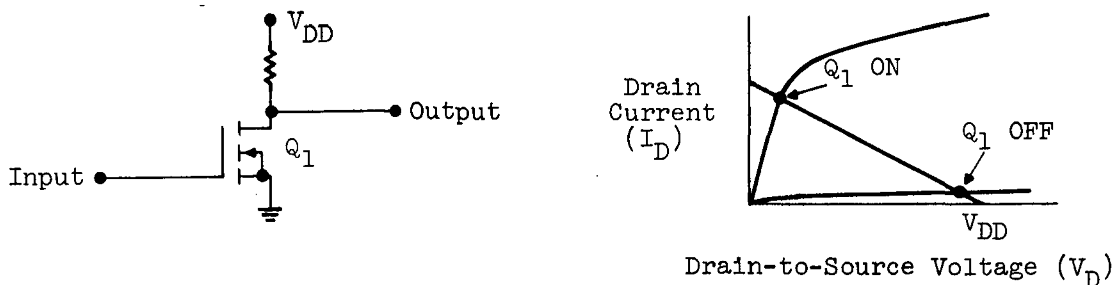


FIGURE 2-54

INVERTER USING MOS TRANSISTOR AND A RESISTOR
WITH TYPICAL LOAD LINE

Figure 2-55 shows an inverter that uses a depletion-type MOS transistor as a load for an enhancement-type MOS inverter. (A depletion-type MOS transistor is one that conducts appreciable current with zero bias between gate and source.)

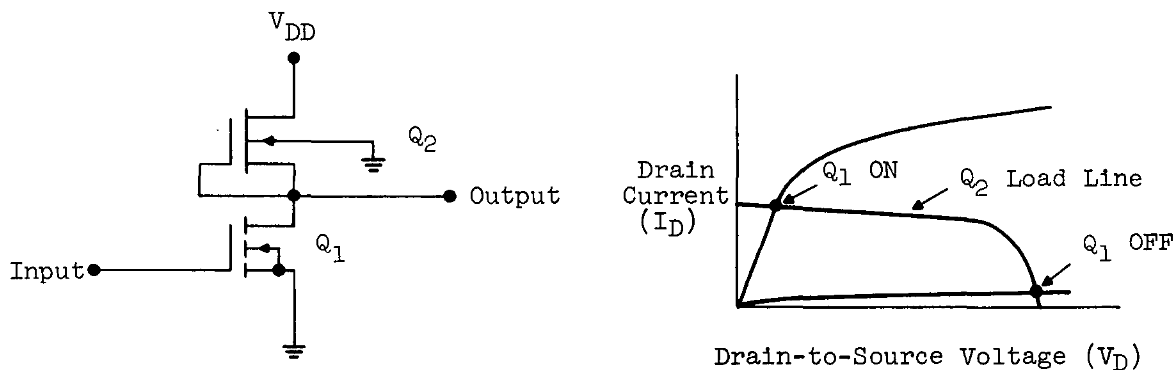


FIGURE 2-55

INVERTER USING DEPLETION-TYPE MOS TRANSISTOR AS LOAD
FOR ENHANCEMENT-TYPE MOS INVERTER, AND TYPICAL LOAD LINE

This circuit has a number of advantages. First, its area is potentially very small because it consists only of MOS devices. Second, the shape of the load line that results is capable of improved speed as compared with an ohmic resistor. From a processing standpoint, however, it suffers from the disadvantage that two types of MOS devices, with different threshold voltages, are required. The resulting processing complexities tend to lower its figure of merit drastically.

Figure 2-56 shows an inverter that uses an enhancement-type MOS transistor connected as a source follower to serve as a load for the inverting MOS transistor. Although this circuit is a poor choice from a discrete-component point of view, it possesses a very high figure of merit considered in the light of digital integrated arrays. First, it uses the absolute minimum area because, to operate at

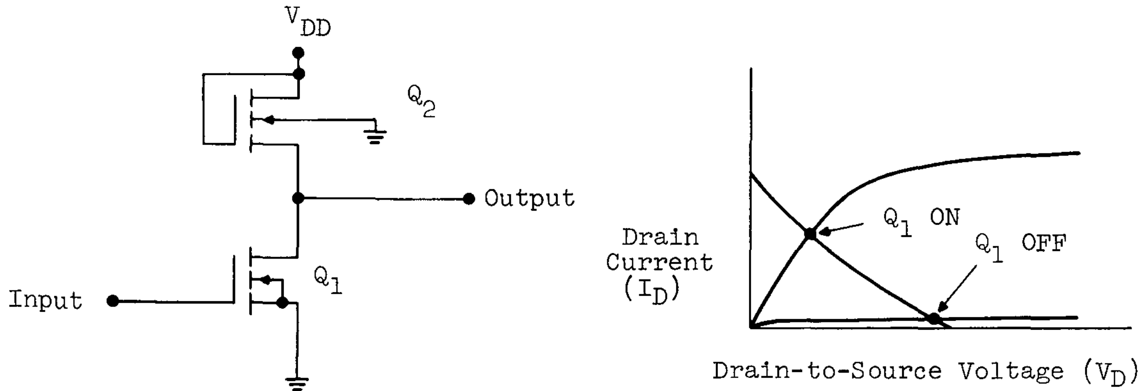


FIGURE 2-56

INVERTER USING ENHANCEMENT-TYPE MOS TRANSISTOR
CONNECTED AS SOURCE FOLLOWER AS LOAD FOR INVERTING
MOS TRANSISTOR, AND TYPICAL LOAD LINE

all, the load MOS device must be smaller than the inverting MOS device. Second, the processing required to fabricate the circuit is also minimum because the load MOS device is made by the same process as that used for the inverter MOS device. The operation of the circuit depends on the control of the ratio of the transconductance of the two devices. Although the absolute value of the transconductance depends on a number of factors, including the oxide thickness under the gate, the ratio is determined by the geometries of the two devices. When accurate masks are used, therefore, the ratio can be held constant even with variations in processing.

The final inverter circuit to be considered is shown in Figure 2-57. It consists of a pair of complementary MOS devices connected in series, with the

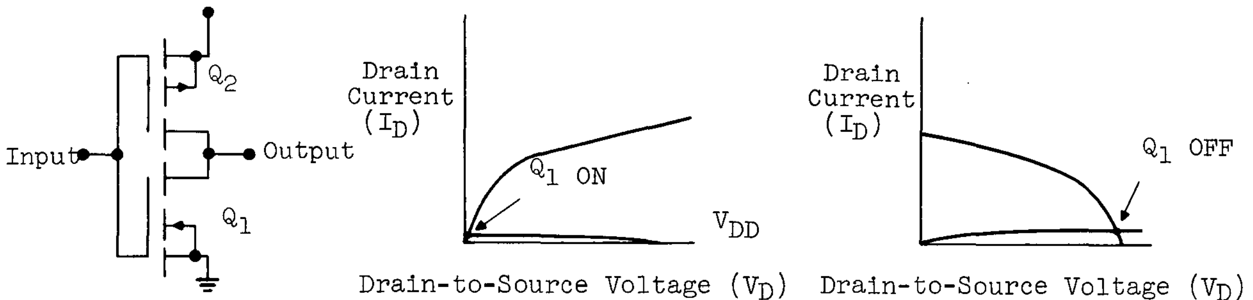


FIGURE 2-57

INVERTER AND LOAD LINES
(USING COMPLEMENTARY MOS DEVICES)

gates connected to each other and driven by the input signal. When the input signal is zero, the P-channel device is on and the N-channel device is off. The reverse is true when the input signal is positive. Each device, when on, is required to supply a direct current equal to only the leakage current of the other device. During a transistion of the input signal, however, capacitive loads

are charged through the low output impedance of one or the other of the two devices. Thus, although it requires very low standby power, the circuit is inherently fast. The load lines in Figure 2-57 indicate the very low standby power. The figure of merit for the circuit is not as high as for the source-follower circuit shown in Figure 2-56, because slightly more area is required and the processing is considerably more involved. Despite these disadvantages, arrays of complementary MOS circuits are beginning to find applications where either very low standby power or high speed is important enough to compensate for the reduced figure of merit.

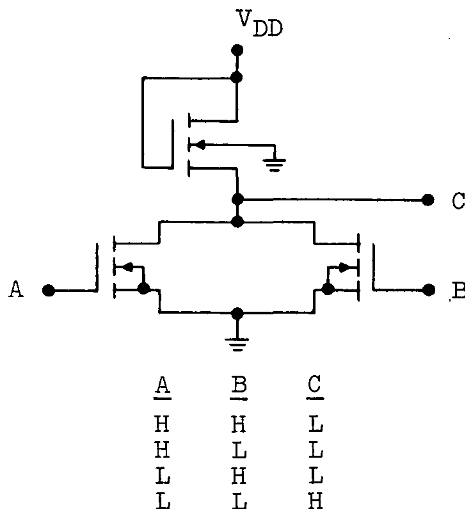
The total power dissipated, neglecting the standby power, in a complementary MOS circuit during switching is given by

$$P = C_L \, V_{DD}^2 \tag{2-55}$$

where C_L is the total output capacitance and V_{DD} is the supply voltage.

2.2.16 Single-Channel Arrays

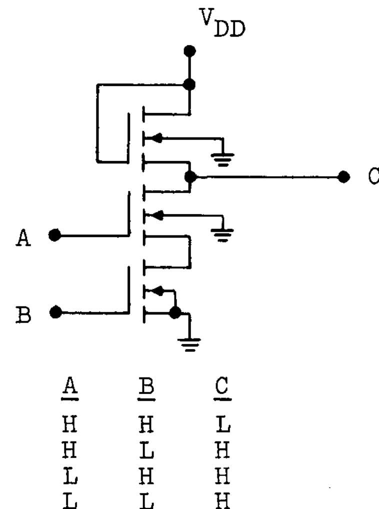
The basic circuit shown in Figure 2-57 can be developed into a wide variety of digital circuit arrays. Parallel connection of the inverter transistor forms a NOR gate, as shown in Figure 2-58. Figure 2-59 shows how a NAND gate can be



A	B	C
H	H	L
H	L	L
L	H	L
L	L	H

FIGURE 2-58

NOR GATE USING PARALLEL CONNECTION OF MOS TRANSISTORS



A	B	C
H	H	L
H	L	H
L	H	H
L	L	H

FIGURE 2-59

NAND GATE USING SERIES CONNECTION OF MOS TRANSISTORS

formed by series connection of the inverting transistors. When the NAND gate of Figure 2-59 is used in conjunction with the NOR gate of Figure 2-58, the resulting configuration offers a high degree of logic flexibility. However, the series connection suffers from the disadvantage that the inverter transistors must be twice as large as their parallel counterparts to maintain the same control of logic levels.

2.2.17 MOS Noise

In the MOS transistor, three mechanisms give rise to gate noise and thus input noise in an amplifier.* The main source of noise at high frequencies** is thermal noise due to random fluctuations in the free-carrier concentration in the channel. Noise figures comparable to low-noise vacuum tubes are obtained at frequencies above 50 Mc.

The low-frequency noise spectrum,† which may extend up to tens of megacycles per second in some devices, is controlled by the fluctuations in the number of electrons occupying surface traps; it resembles an f^{-n} distribution. The value of n is generally between 1 and 2, and the spectrum extends down to very low frequencies. Shot noise is produced by fluctuations of the individual charges as they drift and diffuse toward the surface. Leakage noise is associated with the small flow of current through the oxide.

*A. G. Jordan and N. A. Jordan, "Theory of Noise in Metal Oxide Semiconductor Devices", Transactions of IEEE ED, March 1965, p. 148

**A. Van der Ziel, Proceedings of IRE, Vol. 50, p. 1808, "Thermal Noise In Field-Effect Transistors", 1962

†A. G. Jordan and N. A. Jordan, "Noise in MOS Devices", Solid-State Devices Research Conference, Boulder, Colorado, 1964; and

C. T. Sah, "Theory and Experiments on the 1/f Surface Noise of MOS Insulated-Gate Field-Effect Transistors", Solid-State Devices Research Conference, Boulder, Colorado, 1964

PACKAGING AND INTERCONNECTIONS

THREE

3.1 General Requirements of IC Package

One of the major considerations in applying integrated circuits to a particular system is selecting the proper IC package. In this regard, certain factors merit special attention by both the manufacturer and the user.

The device* manufacturer has primary responsibility for the reliability of the IC package, whether he fabricates the package or purchases it. The device manufacturer, then, must consider such characteristics as mechanical integrity, hermetic seal, lead stresses, etc.

The user of the device, of course, is concerned also with package reliability; he also investigates characteristics such as space efficiency and design flexibility.

General requirements of an IC package fall under the following headings:

- Mechanical integrity
- Electrical requirements
- Hermetic seal
- Thermal transfer
- Space efficiency
- Design flexibility
- Special requirements
- Low cost

These requirements are discussed briefly in the following paragraphs.

---

*"Device" is defined as the integrated circuit plus its package.

3.1.1 Mechanical Integrity

During fabrication and operation, the IC package must withstand exposure to certain levels of shock, acceleration, vibration, soldering or welding heat, temperature cycling, thermal shock, moisture, and lead stresses. MIL-STD-202 tests are designed to ensure that the package will withstand the stresses encountered in device assembly (installing the chip into the package and performing the final seal), system fabrication (mounting and attaching the package to the mother board), and system operation.

3.1.2 Electrical Requirements

Electrical requirements of the IC package include the following:

(1) The number of leads must be sufficient to accomodate a fairly complex circuit chip. Unused leads can be used for package tie-down (extra strength), or may be clipped off.

(2) The package must avoid excessive distributed capacity and inductance.

(3) In many applications, the package must be capable of providing electrical shielding.

3.1.3 Hermetic Seal

Another fundamental requirement of an IC package is that its internal environment remain constant; variations in this environment can cause failure mechanisms to be generated within the device. Although an exact correlation between leakage rate and device life is extremely difficult to establish, packages with a leakage rate of less than 10^{-8} cubic centimeters per second have proven to be reliable from a hermetic standpoint. This rate, usually measured by a helium leak detector, is equivalent to the leakage of one cubic centimeter of air in ten years, at a pressure differential of one atmosphere.

3.1.4 Thermal Transfer

The operating temperature of an integrated circuit is a major factor affecting its reliability. Of the three methods of heat transfer [conduction, convection, and radiation (see Figure 3-1)], conduction can generally transfer the most heat; thus the IC package should be constructed of materials that have high thermal conductivity.

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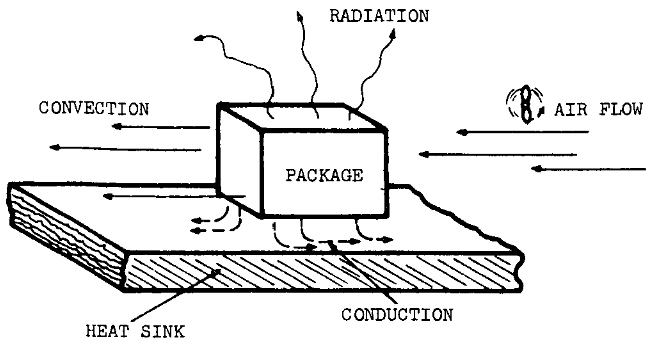

FIGURE 3-1

HEAT-TRANSFER MODES OF IC PACKAGE

3.1.5 Package Space Efficiency

For maximum utilization of space, the package should conform closely to the shape of its contents. Standardized packages are often unable to meet this criterion, but the "poor fit" can offset by increasing the circuit functions (i.e., more or larger chips).

3.1.6 Design Flexibility

The device user requires that the IC package have certain features which facilitate handling and assembly. These features, collectively called "flexibility", include the following:

(1) The package must be easily handled during device manufacturing, testing, shipping, and fabrication into a particular equipment. Handling difficulties encountered during any of these phases will result in an increase in equipment costs and generally a decrease in reliability.

(2) The package must be amenable to various mounting techniques (planar, stacked, on edge, etc.); to the standard interconnection methods (flow-soldering, dip soldering, welding, or thermocompression bonding; and to various means of heat dissipation.

(3) The package should have high-density potential. Integrated circuits play a major role in microminiature systems, where high-density packaging is mandatory.

3.1.7 Special Requirements

The package should be resistant to corrosion or other physical change due to external reactive agents (electrical fields, moisture, etc.). In some cases, the package may also have to be immune to light radiation because of the type of circuit enclosed. For example, Texas Instruments produces an Optoelectronic Pulse Amplifier (SNX 1304) which requires an opaque case to protect a light-sensitive diode.

For electrical shielding, the package may have to be made of metal, with one of its leads electrically connected to the case for grounding purposes.

3.1.8 Package Costs

Naturally, the cost of the package should be as low as possible. For many devices, however, the cost of the package is greater than that of the silicon circuit die.

3.2 Available Package Types

The two most widely used IC packages are the modified TO-5 transistor package and the flat pack. These two packages are discussed in this section.

3.2.1 Modified TO-5 Package

Modified TO-5 assembly methods are extensions of the techniques applied in the production of standard transistor packages. Since the modified TO-5 package typically has 10 leads, compared with the 3 or 4 of the standard transistor package, the pin-circle diameter of the former is slightly larger (0.230 inch vs. 0.200 inch). An exploded view of the modified TO-5 package is shown in Figure 3-2. The materials used in the header are Kovar (a nickel-iron alloy) for the leads and eyelet, and type-7052 glass for the preform. The can may be made of German silver, Kovar, or nickel. Kovar and 7052 glass are usually used since they have similar coefficients of thermal expansion (see Figure 3-3) and provide a matched seal.

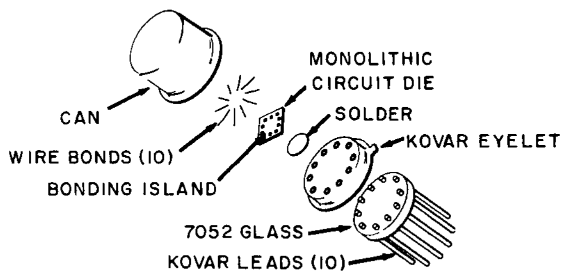

FIGURE 3-2

EXPLODED VIEW OF TO-5 PACKAGE

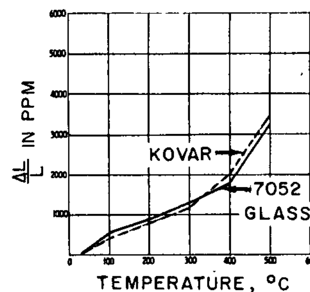

FIGURE 3-3

THERMAL EXPANSION CURVES

The Kovar leads are enclosed in the glass preform and assembled to the eyelet. The glass, leads, and eyelet are sealed by fusion in an oven at 1000°C. After this sealing process, the entire assembly -- called the "header" -- is cleaned, and the leads are clipped off to obtain the desired post height. The header is then plated with 0.0001 inch of gold cyanide. The monolithic die (dice) is bonded to the header by (1) inserting a gold-silicon preform between the die and the header; (2) placing a weight on top of the assembly, and (3) heating the entire header stage to approximately 395°C. The gold-silicon eutectic is reached as a result of the heat and pressure, and the die, preform, and header are fused together. The circuit is then wirebonded to the posts and baked in an inert atmosphere at 200° to 300°C for approximately 30 minutes.

In the case of hybrid circuits utilizing a ceramic disc, the pattern on the disc corresponding to the location of the disc is metalized with molymanganese. The substrate is then gold-plated, with the gold adhering only to the metalized area. The disc is affixed to the header by brazing, the dice are bonded to the metalized pads of the ceramic with a germanium-gold eutectic, and the dice are interconnected and wire-bonded to the posts.

After the circuit is checked electrically on the header, the can is welded to the flange of the eyelet. The welding is done in a controlled atmosphere to ensure stability of the circuit under operating conditions.

3.2.1.1 TO-5 Thermal Characteristics

Figure 3-4 is a cutaway view of the modified TO-5 package, with heat-flow paths indicated. Most of the heat is conducted from the chip to the header assembly. The header assembly then conducts the heat radially to the lip and sides of the package, where it is transferred to the atmosphere by convection and radiation.

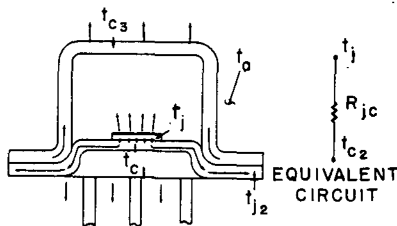

FIGURE 3-4

THERMAL PATHS IN TO-5 PACKAGE

The heat-dissipating capability of the modified TO-5 package can be improved by either of two methods. A metal container (with or without fins) can be fitted over the top of the package to increase its surface area, or forced air cooling may be used.

The most significant thermal parameters in IC packages are the junction-to-case and junction-to-ambient thermal resistances (θ_{JC} and θ_{JA}, respectively). Values of these parameters vary among manufacturers but are typically 80°C/W for θ_{JC} and 180°C/W for θ_{JA}. The θ_{JC} of a hybrid circuit mounted in the TO-5 package is approximately 10% higher than in standard circuits because of the ceramic disc between the chips and the header assembly.

3.2.1.2 TO-5 Space Efficiency

The space efficiency of an IC device utilizing the TO-5 package is generally poor, since the circuit usually occupies only a small fraction of the package height (see Figure 3-3). One means of reducing the void space is to apply hybrid techniques to silicon monolithic circuits. Each silicon circuit is mounted on a ceramic wafer having a diameter approximately that of the TO-5 chip mounting area. The ceramic discs are then stacked in layers to a height sufficient to fill the package (0.180 inch). The individual monolithic circuits are interconnected with fine gold wires and terminated at the external leads. This method of increasing space efficiency requires elaborate fabrication equipment and is quite costly.

The space efficiency problems associated with the TO-5 have led to the development of a low-profile variation of this package. The newer design, known as the modified TO-47, is illustrated in Figure 3-5, with the TO-5 shown for comparison. In spite of its greater inherent space efficiency, the TO-47 has not approached the level of usage of the TO-5, because of the TO-47's higher cost and lower power-dissipation capability.

Also detrimental to the space efficiency of the TO-5 is the inefficient utilization of lateral area. The IC die is always square or rectangular, since it is impractical to perform die separation in a manner that yields circular dice. These cornered dice do not conform closely to the circular mounting area on the TO-5 header (see Figure 3-6).

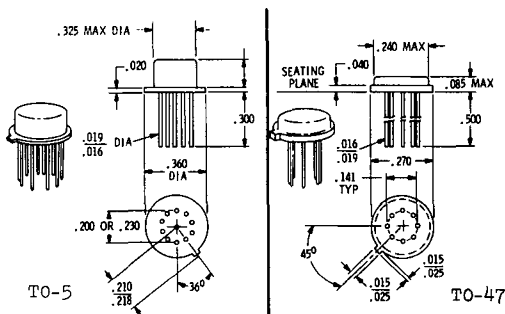

FIGURE 3-5

MODIFIED TO-5 AND TO-47 DESIGNS

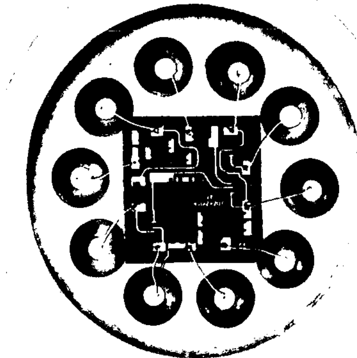

FIGURE 3-6

IC DIE IN MODIFIED TO-5 PACKAGE

3.2.1.3 TO-5 Design Flexibility

As mentioned earlier, the IC package should have features that facilitate handling and assembly. The modified TO-5 has become a standard package; thus most semiconductor and electronic-system manufacturers have the equipment for handling it efficiently. Also, the fixtures used in manufacturing, testing, shipping, and installing the package are available from a variety of vendors at reasonable prices.

Another design-flexibility requirement is that the package be amenable to various mounting techniques. The TO-5 package can be either plugged into the board or embedded in the board, as illustrated in Figure 3-7. The former method is preferred. In either method, the interconnection pattern required for the package leads creates an area that must be avoided by other printed conductors

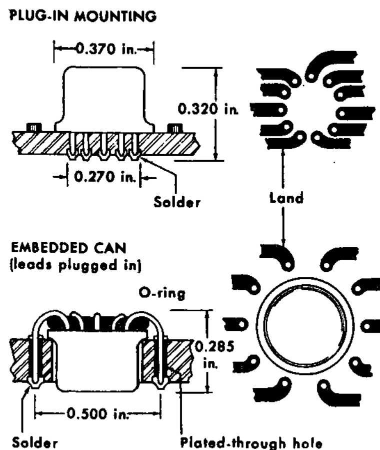

FIGURE 3-7

TWO METHODS OF MOUNTING
TO-5 PACKAGE ON BOARD

on both sides of the board. The surface (plug-in) method yields insufficient clearance between the islands to route additional circuitry. In the other mounting method (embedding), there is sufficient area between the islands (because of the increased diameter of the interconnection pattern) for additional conductors; however, the 0.325-inch hole required to accept the package poses a restriction. Thus the interconnection pattern problem and the fact that only two mounting methods are obtainable restricts the design flexibility of the modified TO-5 package.

Generally, the TO-5 package is secured to the mounting area by a solder-dip or reflow process. Welding techniques such as parallel gap, axial, and electron-beam are seldom used for the TO-5 package because of the cylindrical geometry of the individual leads and the overall package.

The modified TO-5 package has a low-density potential relative to the flat package. The effective area of the TO-5 package is 0.160 square inch, and its volume is 0.042 cubic inch. As a result, its theoretical density potential (with surface mounting) is approximately 24 circuits per cubic inch, or 40,000 per cubic foot. Additional items such as interconnecting and heat-dissipating devices will reduce the density even more. With mounting boards that have conductors on both sides and sufficient adjacent area for heat transfer, a maximum of two TO-5 10-lead packages per square inch is obtainable. With multi-layer boards (to be discussed later), the density can be increased to approximately 7.5 packages per square inch.

3.2.1.4 TO-5 Package Costs

The modified TO-5 package is inexpensive compared with the flat package. A typical cost is 10 to 12 cents per package in quantities of 10,000 or more. Since the TO-5 package has been in existence for at least five years, the present price probably will not decrease significantly.

Several manufacturers have produced packages similar to the TO-5, but of an epoxy material. These packages can be produced for less than 5 cents each in large quantities. However, some epoxy materials have a tendency to absorb water and have a large thermal-expansion coefficient, so that the hermetic seal may be less reliable than that of the TO-5. For this reason, the epoxy package has thus far found its greatest use in commercial applications.

3.2.2 Flat Pack

Many types of IC flat packages are being produced, in various sizes and materials. These packages are available in square, rectangular, oval, and circular configurations with 10 to 60 external leads. The package can be made of metal, ceramic, epoxy, glass, or combinations thereof. Only the ceramic flat pack will be discussed, since it is representative of all flat packs with respect to general package requirements.

Construction of the ceramic flat pack is illustrated in Figure 3-8. The Kovar leads, which are attached within a frame, are inserted into the castellations of the ceramic mounting base. A 7052 glass substance is applied to the castellated area, and the assembly is placed in a furnace operating at 1000°C. The 7052 glass is fused to the ceramic base and Kovar leads, creating a hermetic seal. (The castellations in the mounting base provide additional strength to the body-to-lead seal.)

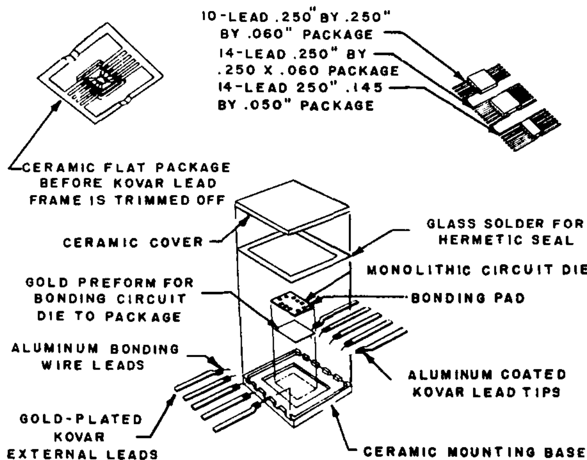

FIGURE 3-8

EXPLODED VIEW OF CERAMIC FLAT PACK

After the leads are sealed to the mounting base, a rectangular area on the inside bottom of the base is treated with molymanganese. This metalization provides a surface suitable for bonding the IC chip to the base. The lead frame is then cut away from the secured leads, and these leads and the metalized area in the bottom of the package are gold plated. The die is then attached via gold-silicon eutectic bonding.

The die bonding is followed by bonding gold or aluminum wires between the bonding islands on the IC die and the inner portions of the package leads.

Following the wire bonding, a glass-solder preformed frame is placed on top of the mounting base. One surface of the ceramic cover is coated with Pyroceram* glass, and the cover is placed on top of the mounting base. The entire assembly is placed in an oven at 450°C, causing the glass solder and Pyroceram to fuse and seal the cover to the mounting base.

*Trademark of Corning Glass Company.

3.2.2.1 Flat-Pack New Fabrication Technique

Considerable effort is being devoted to eliminating the fine wires connecting the circuit to the Kovar leads. The omission of these wires would materially reduce the cost of integrated circuits by eliminating the bonding labor. This design improvement would enhance reliability by precluding a potential cause of circuit failure.

A promising fabrication technique is the face-down (flip-chip) mounting method, in which conductive patterns are evaporated inside the package before the die is attached. These patterns connect the external leads to appropriately located pedestals on the interior surface of the package. The location of these pedestals corresponds to the bonding pads on an integrated circuit die. The die is then inverted over the pedestals, which are brazed to the circuit bonding pads (see Figure 3-9). This technique requires precise registration of the circuit die pads and pedestals, and must be further developed before it can be applied to production devices.

3.2.2.2 Flat-Pack Thermal Characteristics

Figure 3-10 is a cutaway view of the flat pack, with the heat flow indicated by arrows. Heat generated by the silicon die is radiated into the interior and conducted into the mounting base. The heat quickly reaches the package outer surface because of the close contact of the die with the package and the

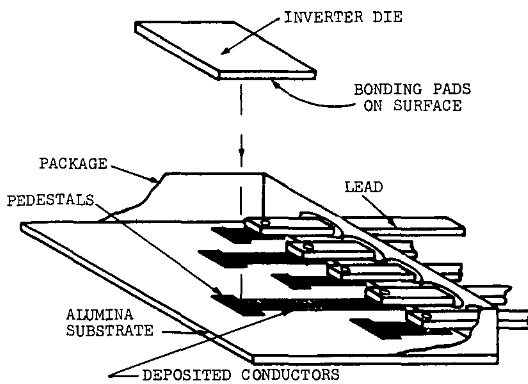

FIGURE 3-9

FLIP-CHIP TECHNIQUE

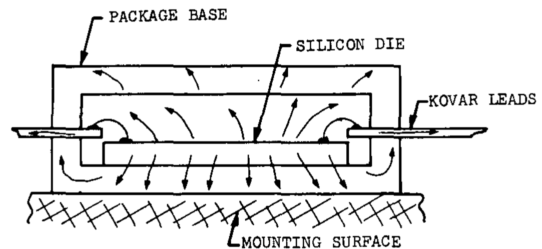

FIGURE 3-10

CUTAWAY VIEW OF FLAT PACK, SHOWING HEAT-FLOW PATHS

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high thermal conductivity of the package material (alumina). The flat pack has a lower θ_{JC} than the TO-5 package, with a typical value of 40°C/W (vs. 80°C/W for the TO-5). However, its θ_{JA} is higher than that of the TO-5 package (typically 250°C/W vs. 180°C/W) because of its relatively small surface area.

The low θ_{JC} of the flat pack allows efficient removal of heat from the pack by conduction to the heat sink through a thin strip of metal placed under the pack. For this reason, heat transfer by conduction is commonly used today in high-density packaging. It is discussed in detail in Section 3.3.3.

3.2.2.3 Flat-Pack Space Efficiency

The internal volume of the flat pack can be utilized efficiently for integrated circuits. The rectangular flat pack conforms closely to the rectangular or square silicon IC die (see Figure 3-11). The external leads are brought into the pack through the walls, leaving the base area unobstructed and available for large dice. The thin package helps to minimize the internal unused space. The silicon circuit often consumes 80% of the available mounting space inside the flat pack.

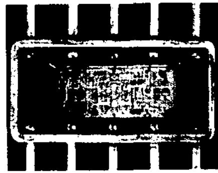


FIGURE 3-11

SPACE EFFICIENCY OF FLAT PACKAGE

3.2.2.4 Flat-Pack Design Flexibility

Holding the flat pack secure for fabrication, testing, shipping, and installation constitutes a major problem. The package is very small (1/8 × 1/4 × 1/16 inch), and its leads are quite delicate (measuring 0.004 × 0.012 inch). Fixtures used in retaining the flat package are discussed in detail in Chapter 4.

Design flexibility is greatly enhanced if alternative means can be employed for mounting the package to a surface. The flat pack can be mounted in several ways: surface, stacked, or on-edge, with the first of these generally preferred.

One interconnection pattern for the flat pack is shown in Figure 3-12. The package leads are attached directly to the printed conductor and additional printed circuitry is routed underneath the package. An insulating substrate is placed between the printed conductors and the package during assembly, and an epoxy is applied to secure the package in place. Naturally, the insulating

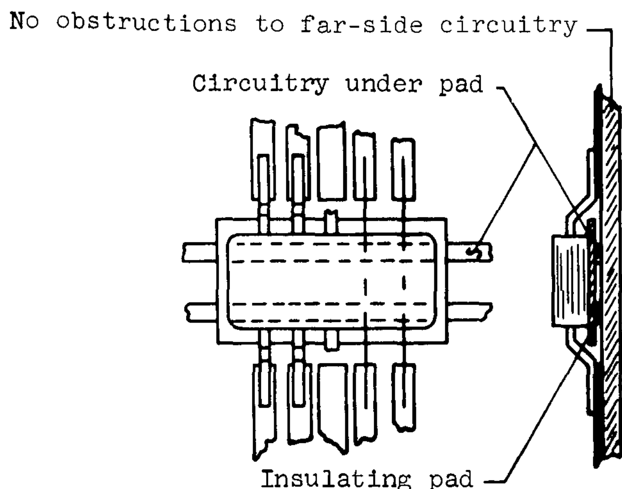


FIGURE 3-12

INTERCONNECTION PATTERN FOR FLAT PACKAGE

pad causes an increase in thermal resistance (by about 5°C/W) between the package and the mounting area.

Another feature of this type of mounting is the absence of obstructions to printed circuitry on the opposite side of the mounting board. In many designs, flat packs are mounted on both sides of the board, directly opposite each other. The package leads are attached to the printed conductors by soldering or welding. The most promising technique for lead tie-down appears to be welding.

The flat pack has high-density potential because of its small size, unique interconnection pattern, and adaptability to microminiature heat-dissipating techniques. The effective area of an 1/8 × 1/4 × 1/16 flat pack is 0.0875 square inches, and its volume is 0.00031 cubic inches.

The theoretical density potential of the pack is 324 per cubic inch. Taking interconnections and heat conductors into consideration, only 2.5 packages per square inch are practical on mother boards with circuitry on both sides. The use of multilayer boards increases this to nine packs per square inch.

3.2.2.5 Flat-Pack Costs

The flat pack is relatively expensive compared with the modified TO-5. Since the package material may be ceramic, metal, glass, epoxy, or a combination of these materials, it is difficult to quote "typical" prices for the flat pack. An approximation would be 60 cents apiece (excluding epoxy) when purchased in large quantities. The price of the flat pack is declining rapidly, and this trend should continue for the next several years. Some package manufacturers predict that the flat pack will be less expensive than the modified TO-5 within the next two years.

3.2.3 Comparison of TO-5 and Flat Packages

In Table 3-1 the TO-5 and the flat pack are compared according to their compliance with the general requirements for IC packaging.

TABLE 3-1

COMPARISON OF TO-5 AND FLAT PACK

Modified TO-5	Flat Pack
Mechanical	
(1) Has been in production for many years.	(1) Fabrication processes are not yet standard.
(2) Fabrication methods are well established.	(2) Package cost is 60-65 cents in large quantities.
(3) Production yield is high and price is low (10-12 cents in quantities of 10,000).	(3) Many engineers are unfamiliar with its advantages and disadvantages.
(4) Is an industry standard, with well-known capabilities and limitations.	(4) Available reliability data are limited.
Electrical	
(1) Cannot be used for complex circuit chips because of 12-lead maximum.	(1) Are available with as many as 60 leads.
(2) Shielding and circuit isolation are efficient.	(2) Isolation between conductors is effective.
	(3) Intra-circuit shielding is not good.
Hermetic Seal	
(1) Has a reliable hermetic seal.	(1) Stitch welding and glass-to-metal sealing need improved fabrication techniques.
Thermal Transfer	
(1) Has a high θ_{JC} and low θ_{JA}.	(1) Has a low θ_{JC} and a high θ_{JA}.
(2) Available heat sinks are too large to permit high-density packaging.	(2) Heat transfer by conduction is applicable to microminiature heat-sinking technique (deposited metal pads on module boards).
Package Space Efficiency	
(1) Contains wasted space, except when hybrid circuits (stacked wafers) are used.	(1) Chips usually fill most of available space.
Package Flexibility	
(1) Standard fixtures permit easy handling.	(1) Is difficult to handle in fabrication, testing, and installation.
(2) Number of mounting methods are limited.	(2) Can be mounted in a variety of ways.
(3) Low-density potential does not permit optimum use of space.	(3) Has a high-density potential.
Package Costs	
(1) Is inexpensive and readily available.	(1) Is expensive.

3.2.4 Standardization

Many types of package are available for use with integrated circuits, but such packages are difficult to standardize because of the rapid advance of the technology. The modified TO-5 and the 1/8 × 1/4-inch flat pack are now used in larger quantities than any of the other package types. Their popularity is probably due to the large quantity of available test data on these packages. The current trend in military systems is toward the flat pack, whereas the trend in commercial systems favors the modified TO-5 or the dual in-line package.

The Electronic Industries Association (EIA) has approved eight flat-pack designs of the 10- and 14-lead variety on four basic configurations (see Table 3-2). Therefore, it appears that some standardization of packages is possible, though new types will continue to enter the market for some time to come.

TABLE 3-2

EIA-APPROVED FLAT PACKAGES (0.035-INCH THICKNESS)

Designation	Package Dimensions (inches)		No. of Leads	Designation	Package Dimensions (inches)		No. of Leads
TO-84	0.250	0.125	14	TO-88	0.330-0.350	0.240-0.260	14
TO-85	0.250	0.160-0.185	14	TO-89	0.250	0.125	10
TO-86	0.250	0.250	14	TO-90	0.250	0.160-0.185	10
TO-87	0.375	0.250	14	TO-91	0.250	0.250	10

3.3 Interconnection Techniques For Integrated Electronics

New generations of electronic systems will require increasingly dense and complex interconnections, and the trend toward higher operating frequencies will necessitate extremely careful design, even of single conductors. Conductor width, spacing, dielectric material, etc., are electrically critical and in many cases directly influence signal propagation, noise figure, pulse shape, and other electrical parameters of the system. Therefore, it is mandatory that designers of systems and circuits become thoroughly familar with the new interconnection techniques. This section discusses the three most used techniques: conventional printed wiring boards (single- and double-sided), welded-wire planes, and multi-layer printed wiring boards.

3.3.1 Conventional Printed Wiring Boards

The conventional printed wiring board consists of a glass-epoxy insulating base on which a copper interconnection pattern is etched (see Figure 3-13). The photolithographic etching process, which leaves a copper pattern approximately 0.003 inches thick, is described in MIL-STD-275A.

3.3.2 Welded-Wire Planes and Assemblies

Welded-wire planes are two layers of wire or metal ribbon (usually nickel) positioned at right angles to each other and separated by a thin plastic film. The layers are welded together through prepunched holes in the plastic film. Where external connections are required, the metal ribbons are welded to connect pins. An assembly is then encapsulated in a hard epoxy. The completed unit is shown in Figure 3-14.

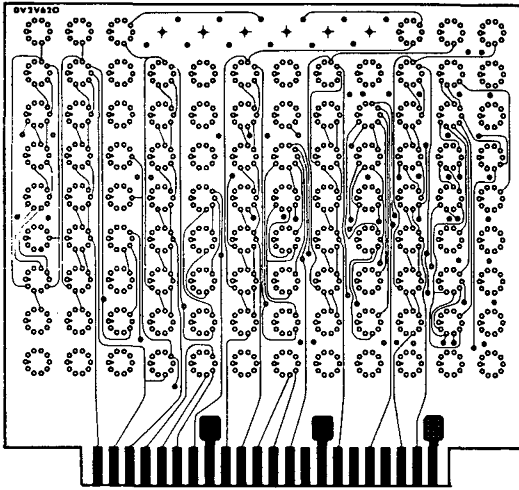
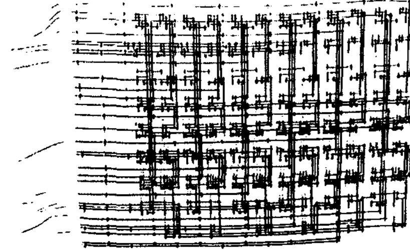


FIGURE 3-13

PRINTED WIRING BOARD



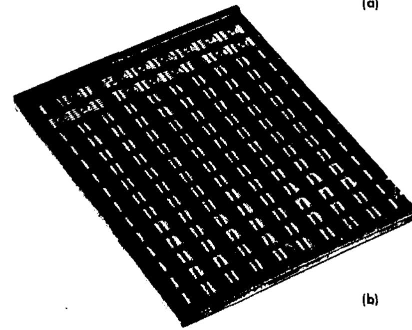


FIGURE 3-14

WELDED WIRE ASSEMBLY

Welded wiring permits 400 or more connections per square inch. Welded-wire networks must be encapsulated, since they would otherwise offer little or no support to attached components; therefore, they weigh more than an equivalent multilayer printed-wiring card. One plane is approximately 0.007 inches thick.

Because of difficulties in mass-production techniques, a multilayer, encapsulated welded-wire matrix costs approximately 25% more than an equivalent multilayer printed wiring card. The welded connection is probably more reliable than a multilayer plated-through hole, but information to support such a conclusion is lacking at this time.

3.3.3 Multilayer Printed Wiring Boards

Multilayer printed wiring is emerging as the solution to interconnection problems associated with high-density packaging. Consequently, the balance of this discussion will be concerned with this particular technique. Multilayer

boards are used: (1) to save weight and space in interconnecting circuit modules; (2) to eliminate costly, complicated wiring harnesses; (3) to provide shielding of a large number of conductors; (4) to provide uniformity in conductor characteristic impedances in high-speed switching systems; and (5) to provide greater wiring density on boards.

Figure 3-15 illustrates the various individual boards that are mated to form the multilayer unit. Although all multilayer boards are constructed in a similar manner, the methods vary for interconnecting the circuitry from layer to layer. Three proven methods are discussed.

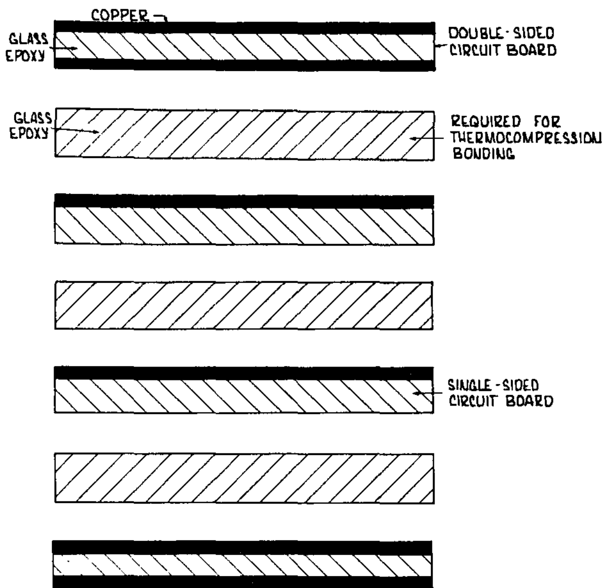


FIGURE 3-15

MULTILAYER BOARD CONSTRUCTION

3.3.3.1 Clearanch-Hole Method

In the clearance-hole process, a hole is drilled into the copper island (terminating end) of the appropriate conductor on the top layer, providing access to a conductor on the second layer (Figure 3-16, hole A). The clearance hole is filled with solder, and the desired connection is completed. Usually the hole is extended through the entire assembly at the connection sites. This small hole is necessary for a solder-flow process normally used with this interconnection method.

To interconnect conductors located several layers below the top, a stepped-down hole process is employed (Figure 3-16, hole B). Before assembly, a clearance hole is provided down to the first layer to be interconnected (in Figure 3-16, through layers 1 and 2 to layer 3). The first layer to be interconnected (3) is predrilled with a smaller hole than that of layers 1 and 2, and succeeding layers to be connected have progressively smaller clearance holes. After assembly,

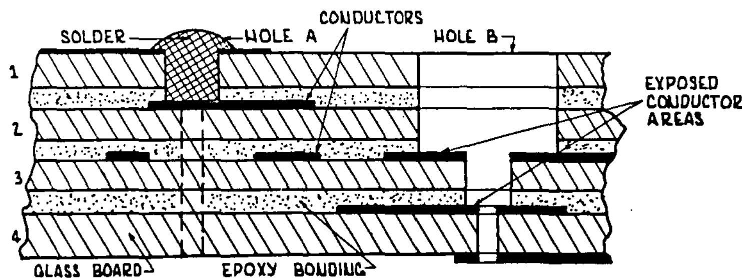


FIGURE 3-16

CLEARANCE-HOLE INTERCONNECTION TECHNIQUE

the conductors to be interconnected have a portion of their island areas exposed. The stepped-down hole is then filled with solder, completing the connection. Obviously, the larger the number of interconnections required at one point, the larger must be the diameter of the clearance hole on the top layer. Large clearance holes on the top layer result in less space for components and therefore reduce packaging density.

3.3.3.2 Plated-Through-Hole Method

The plated-through-hole method of interconnecting conductors is illustrated in Figure 3-17. The first step is to assemble, temporarily, all the layers into their final configuration. Holes corresponding to required connections are drilled through the entire assembly, and the unit is then disassembled. The internal walls of those holes to be interconnected are plated with metal (0.001 inches thick), which, in effect, transfers the conductor on the board surface into the hole itself (the process is identical to that used for standard printed-wiring boards). The boards are then reassembled and permanently fixed into their final configuration, and all the holes are plated through with metal.

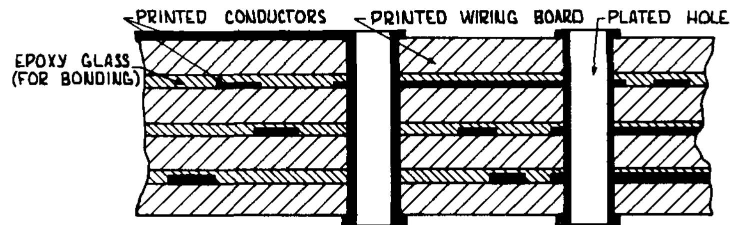


FIGURE 3-17

PLATED-THROUGH TECHNIQUE

3.3.3.3 Layer-Build-Up Method

In the layer build-up method, conductors and insulation layers are alternately deposited on a backing material (see Figure 3-18). This method yields all-copper

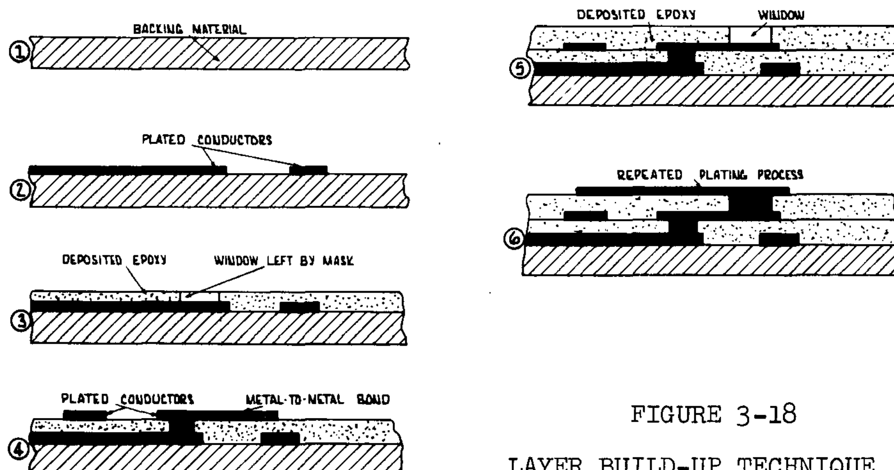


FIGURE 3-18

LAYER BUILD-UP TECHNIQUE

interconnections between layers, and therefore is more reliable than the other two techniques.

3.3.3.4 Comparison of Methods

Each interconnection technique has its advantages and limitations, as discussed below.

(1) Cost -- For small quantities the clearance-hole method is the cheapest, since it requires a minimum of equipment and engineering capability. However, the cost of applying this method goes up drastically for larger quantities -- even though fabrication is simple, the operations are quite time-consuming. The plated-through hole method is usually moderate in cost for both small and large quantities. Built-up layers are generally more expensive than the other two types, regardless of the quantities involved. However, various interconnection designs can have an effect on the multilayer-board price. For example, in the built-up layers, interlayer connections are made without bringing the connections to the surface (as is necessary in the other two methods), allowing greater flexibility in wiring layout. Thus fewer layers are needed for the complete board, and a price lower than that for the plated-through hole method may result.

(2) Density -- The build-up method yields the highest packaging density, since its internal interconnections do not require corresponding holes in other layers. The clearance-hole technique offers the lowest packaging density of the three methods because of the oversized holes required.

(3) Reliability -- As previously mentioned, the built-up layers form the most reliable interconnections, because of their solid-copper makeup. The clearance-hole method is the next most reliable, and the plated-through technique the least reliable. In the latter case, uniform metalization has proven difficult to achieve.

(4) Maintainability -- In general, interconnections made by the clearance-hole method are the least difficult to rework. Plated-through connections are second, and bult-up layers third in this category. In the built-up layers, it is usually difficult -- if not impossible -- to rework any of the internal connections.

Table 3-3 summarizes the advantages and limitations of the three interconnection techniques.

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TABLE 3-3 COMPARISON OF MULTILAYER-BOARD INTERCONNECTION TECHNIQUES (Relative Rating, Where 1 = Highest)				
Technique	Cost*	Density	Reliability	Ease of Repair
Clearance Hole	3	3	2	1
Plated-Through Hole	2	2	3	2
Built-Up Layers	1	1	1	3
* Small quantities.				

3.3.4 Package Tie-Down Techniques

For connecting modules or components to multilayer boards, the conventional method is to solder their leads or pins into the holes of the boards. Recently, other means of component attachment have been tried successfully. These new methods include resistance welding of component leads to tabs, pins, or eyelets protruding over the surface of the board; and parallel-gap welding to tabs made of nickel, Kovar, special foils, or plain copper on the board surface (see Figure 3-19). For soldering, the common hand, dip, and wave processes have been supplemented with techniques such as resistance microsoldering, controlled-heat-zone soldering, and hot-air soldering. The search for an ideal component-attachment method is still going on, and such exotic techniques as the focused electron beam (see Figure 3-19) and diffusion bonding are under investigation.

3.3.5 Multilayer Board Fabrication

A six-bit parallel adder, containing integrated circuits mounted in the modified TO-5 package will be used to illustrate the multilayer assembly process. A diagram of the interconnections required for each IC is shown in Figure 3-20. Figure 3-21 illustrates the probe-side and component-side signal layers of the

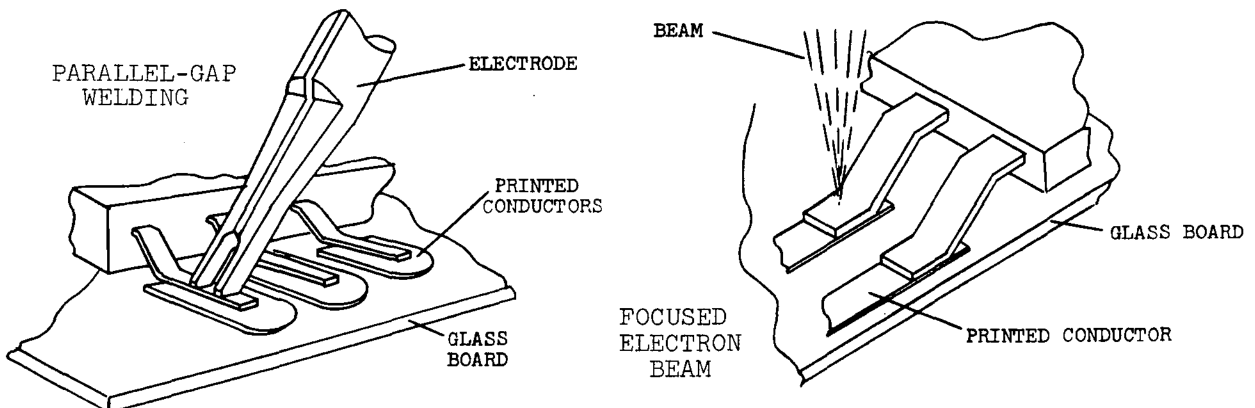


FIGURE 3-19

NEW WELDING TECHNIQUES

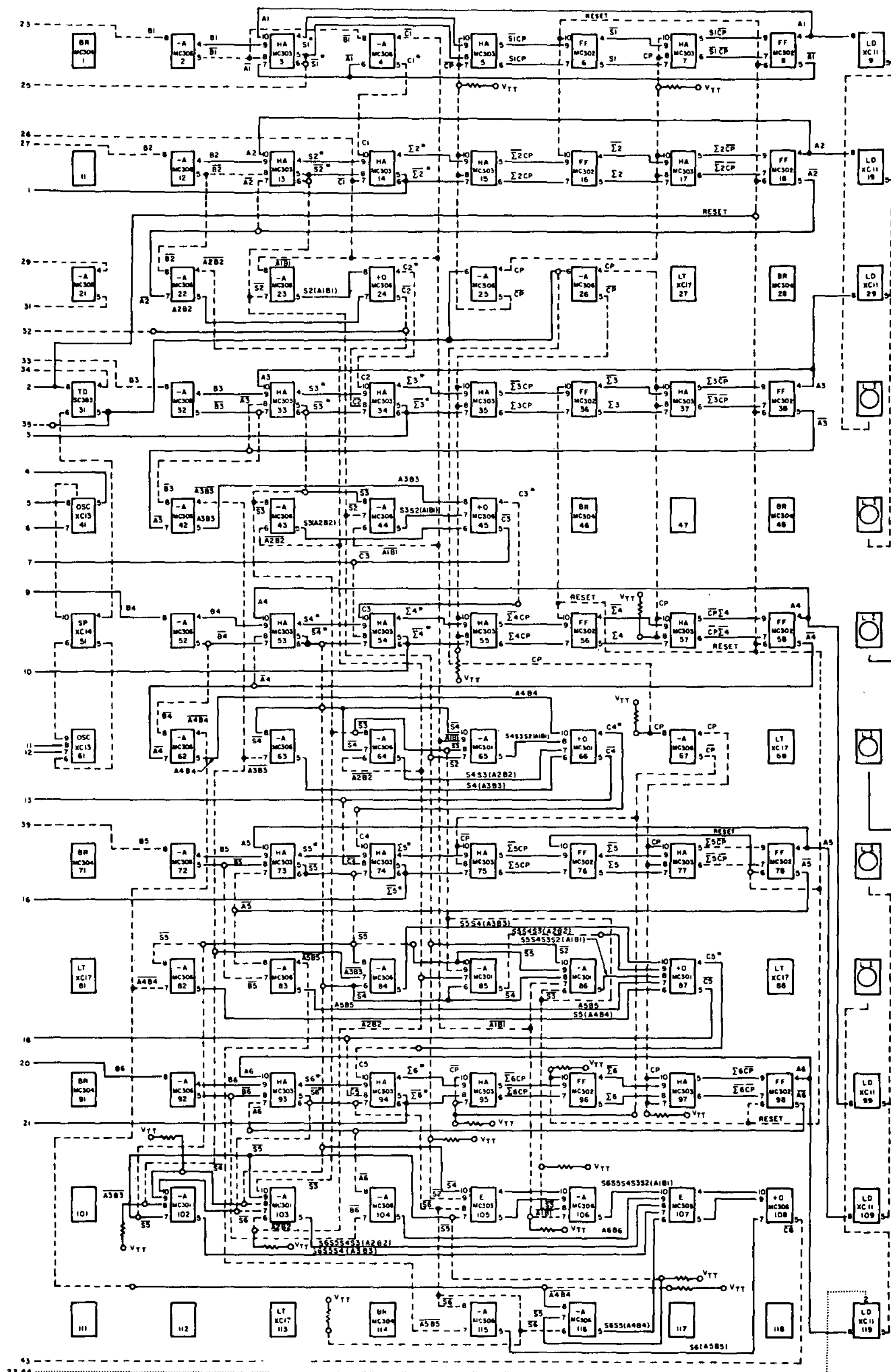
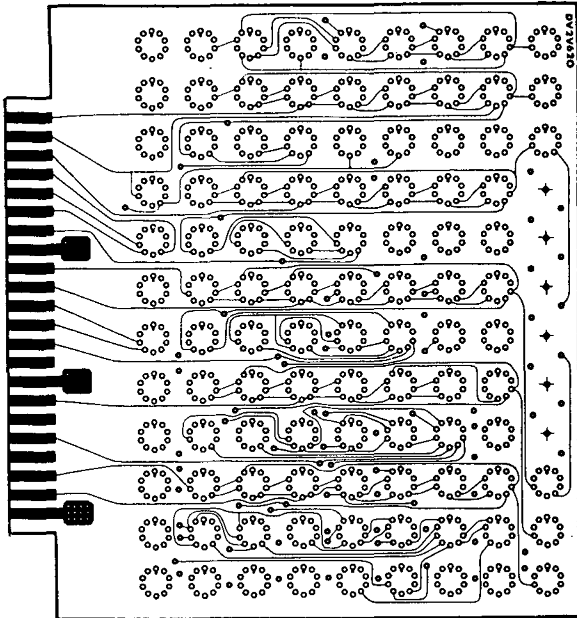
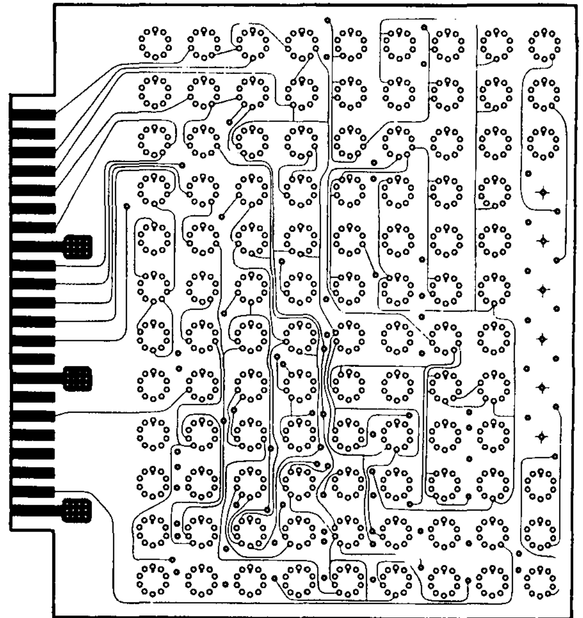


FIGURE 3-20

INTERCONNECTIONS FOR 6-BIT PARALLEL ADDER



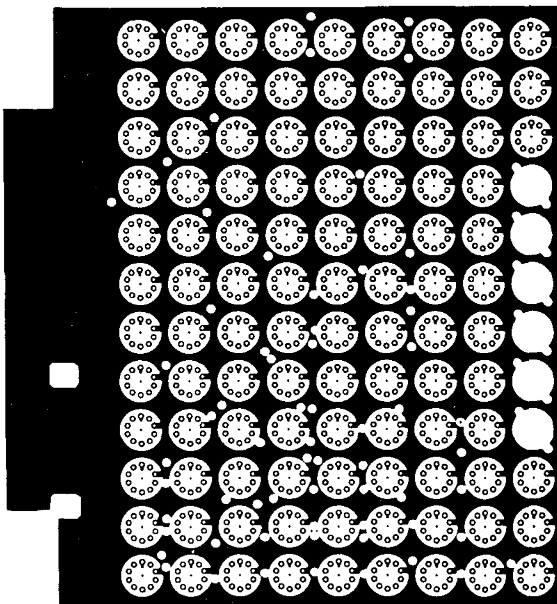
Probe-Side Signal Layer



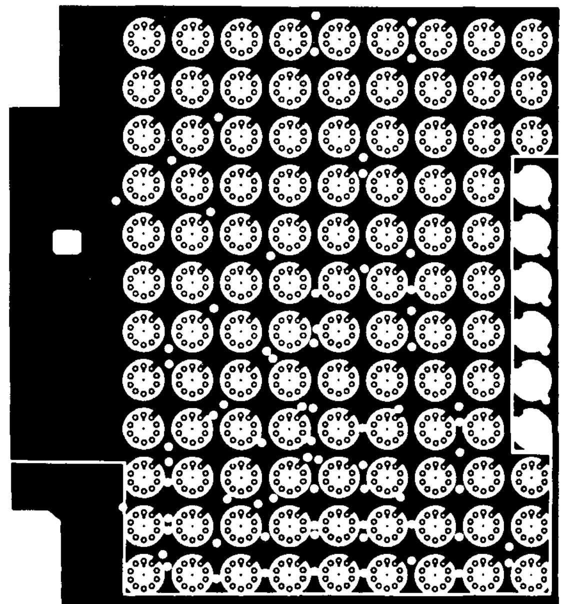
Component-Side Signal Layer

FIGURE 3-21

PROBE-SIDE AND COMPONENT-SIDE SIGNAL LAYERS



V_{CC} VOLTAGE DISTRIBUTION LAYER. PLANE NO. 4



V_{EE} VOLTAGE DISTRIBUTION LAYER. PLANE NO. 2

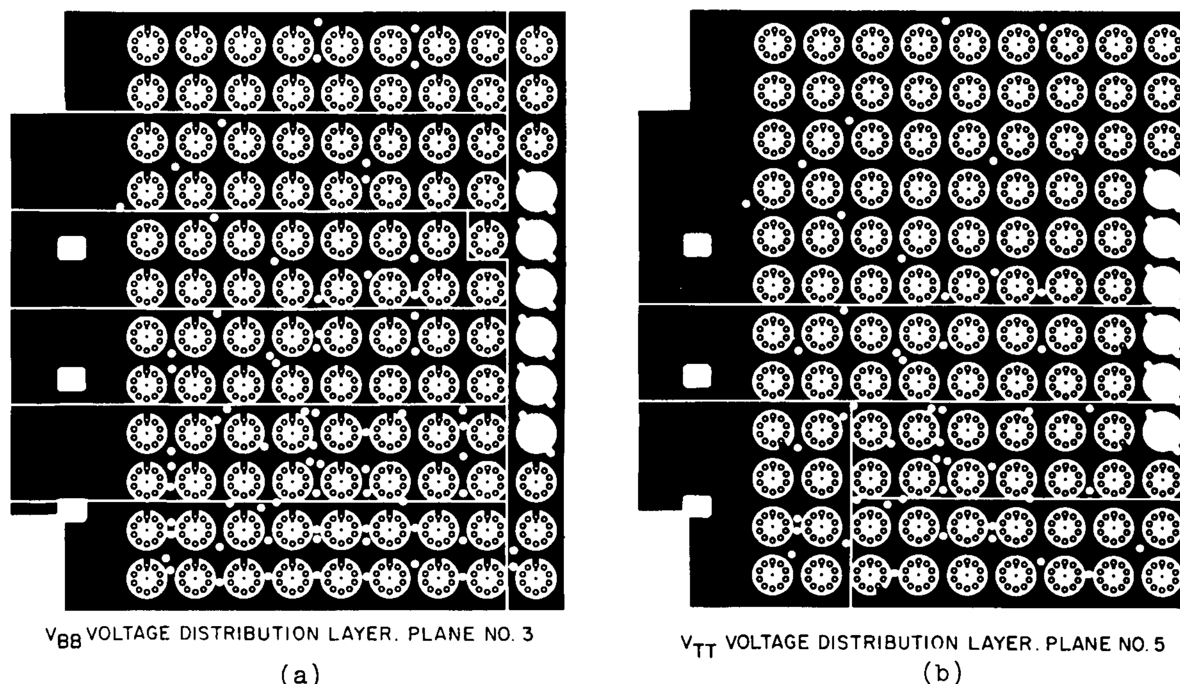
FIGURE 3-22

VOLTAGE DISTRIBUTION LAYERS

multilayer board. Sandwiched between these two signal planes are four voltage planes that distribute voltages to the appropriate pins. Examination of the pin layouts on the individual circuits will show that bias-voltage inputs are well standardized for the various pins (e.g., V_{CC} is distributed through pin 3 on the gates, flip-flops, etc.). This standardization of pin breakouts lends itself to the multilayer technique shown in Figure 3-22. The smaller openings in these patterns are holes which allow the TO-5 leads to go through unshorted. The dark areas on the boards are copper. Note that on each of the voltage-distribution boards one particular pin is shorted to the copper area.

Figure 3-23A shows the bias-voltage plane that distributes the V_{BB} voltage to the logic unit. This distribution is accomplished by connecting pin 1 (output) of the bias drive unit to pin 1 (bias input) of all logic units. The V_{BB} plane is subdivided into seven smaller planes, with one bias driver supplying the necessary voltage for each plane.

Figure 3-23B is the termination-voltage plane, which distributes the V_{TT} voltage generated by the line drivers to the terminating resistor of long signal lines through pin 5. The V_{TT} plane is subdivided into five smaller planes, with one line driver supplying the voltage for each plane.



V_{BB} VOLTAGE DISTRIBUTION LAYER. PLANE NO. 3
(a)

V_{TT} VOLTAGE DISTRIBUTION LAYER. PLANE NO. 5
(b)

FIGURE 3-23

VOLTAGE DISTRIBUTION LAYERS

Figure 3-24 is a cross section of the multilayer board, with the various layers identified according to function and material. The bonding of these

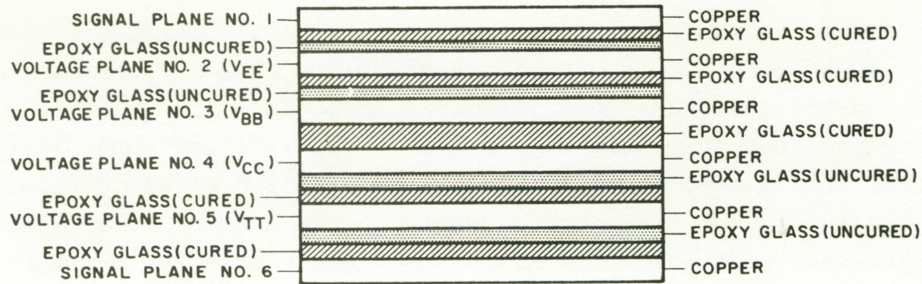


FIGURE 3-24

CROSS-SECTION OF BONDED MULTILAYER BOARD

boards requires accurate registration and a thermocompression technique. The completed multilayer board is shown in Figure 3-25.

3.3.6 Density

The maximum density of TO-5 packages is about two per square inch on two-sided boards and about 7.5 per square inch on multilayers. The corresponding densities for the smaller flat packs are roughly 2.5 and 9 packs per square inch. An increase in the number of components on a multilayer board -- with the same component density maintained -- requires an increase in the number of layers as well as the surface area. The additional layers are needed to provide the capacity for the added interconnections. For example, to connect 25 flat packs, three to four layers are usually sufficient (1 × 3-inch board); to interconnect 50 to 60 flat packs, between five and six layers might be required (2×4-inch board); to interconnect 450 flat packs, 12 layers might be required (6×9-inch board). However, an increase from 5 to 10 layers will increase the cost of multilayer boards (made by the plated-through-hole method) by only 30% to 40%. This explains the tendency toward the production of larger boards.

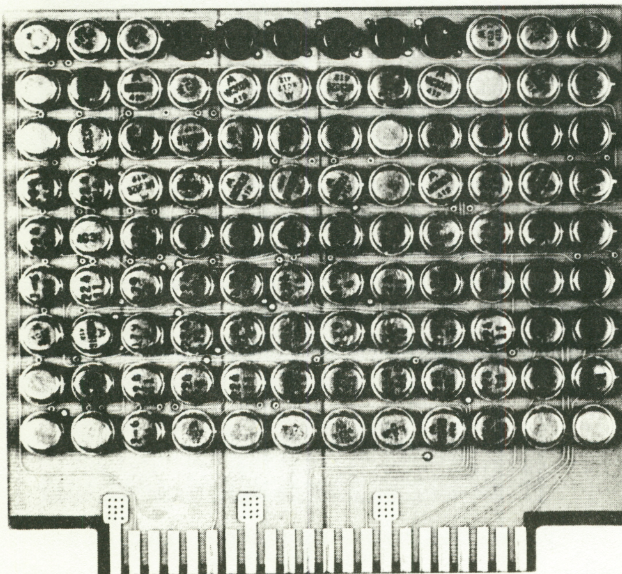
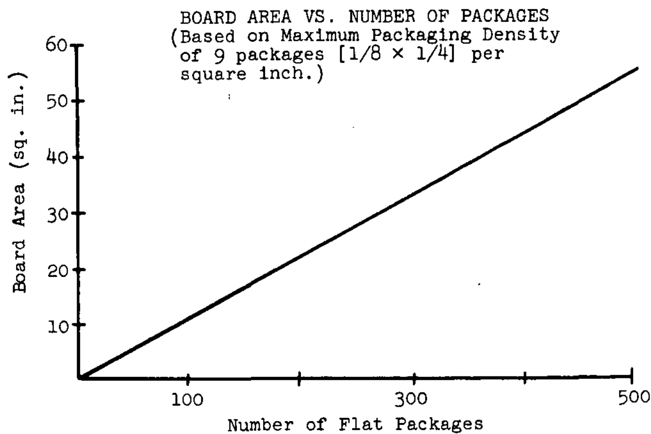


FIGURE 3-25

SIX-BIT PARALLEL ADDER

Figures 3-26a and 3-26b show the required number of layers and required board areas as a function of the number of flat packages.



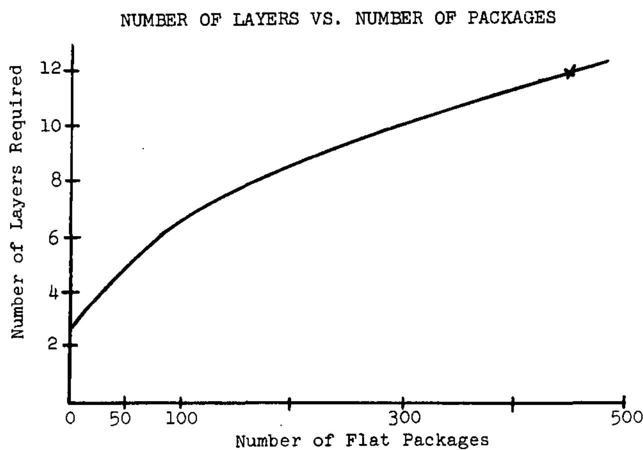


FIGURE 3-26

REQUIRED BOARD AREA AND NUMBER OF LAYERS
AS FUNCTIONS OF NUMBER OF FLAT PACKAGES

3.3.7 Heat Distribution

Equalizing the distribution and removal of heat in systems utilizing integrated circuits is a major design consideration. A typical heat-sink arrangement for multilayer boards is shown in Figure 3-27. The heat-sink layer is usually about 0.006 inches of copper, added (quite inexpensively) during the normal plating stage of manufacturing. A method for removing heat from closely assembled TO-5 packages is shown in Figure 3-28.

3.3.8 Electrical Characteristics Associated with Multilayer Boards

The current-carrying capacity of conductors is usually more than adequate for milliwatt circuitry interconnected by multilayer boards. The ohmic resistance is not a highly important factor, except in cases where conductive paths are

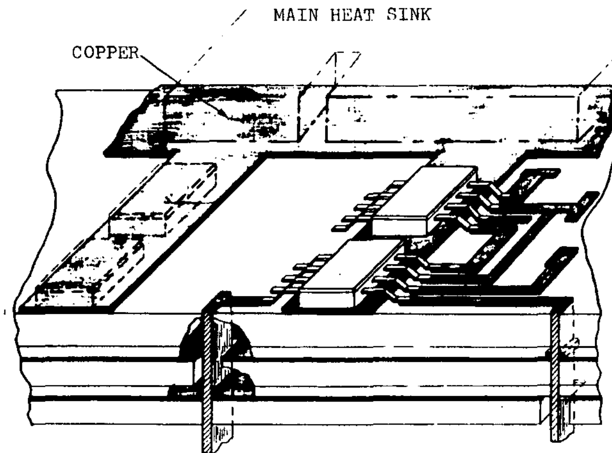


FIGURE 3-27

TYPICAL HEAT-SINK ARRANGEMENT
FOR MULTILAYER BOARDS

very long. For an approximate calculation of conductor resistance, the following values can be used:

Foil Thickness	Ohms Per Foot Length Per Mil Width of Conductor
1-ounce copper	6
2-ounce copper (standard)	3
3-ounce copper	2

Thus a 2-ounce copper conductor 0.01 inches wide has an approximate resistance of 0.3 ohms per foot; the same conductor 0.020 inches wide has a resistance of 0.15 ohms per foot.

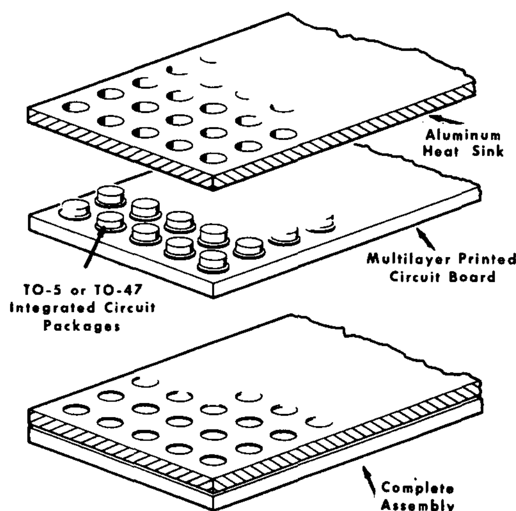


FIGURE 3-28

METHOD FOR REMOVING HEAT FROM
CLOSELY ASSEMBLED TO-5 PACKAGES

A more important electrical aspect of multilayer boards is the distributive capacitance between conductors. This capacitance is quite small between two conductors in the same layer, but is sufficiently large between conductors located directly opposite each other on adjacent layers that it must be accounted for in high-frequency designs. The general capacitor equiation can be used to obtain an approximate value of distributive capacitance (C):

$$C = \frac{K\epsilon_o A}{d}$$

where K = dielectric constant; ϵ_o = permittivity of free space (3.6×10^{-3} pf/inch); A = conductor area; and d = distance between conductors.

This equation gives values approximating, but below, the values obtained by actual measurement. Therefore, the calculated values should not be used in a worst-case analysis. A typical application of the equation is shown below; the data are taken from Table 3-4.

Conductor width = 0.030 inch
Conductor length = 10 inches
Distance between conductors = 0.076 inch
Dielectric constant (K) = 5.4

$$C = \frac{K\epsilon_o A}{d} = \frac{(5.4)(3.6 \times 10^{-3}\text{pf/inch})(3 \times 10^{-2}\text{inch})(10\text{ inch})}{7.6 \times 10^{-2}\text{ inch}} = 0.77\text{ pf.}$$

TABLE 3-4

TYPICAL DIMENSIONS (IN INCHES) OF MULTILAYER BOARD MATERIALS

Item	Dimension
Thickness of copper conductors	0.003 to 0.005
Width of copper conductors	0.020 to 0.030
Thickness of copper heat sink	0.006 to 0.008
Thickness of glass epoxy board (for conductor support)	0.016 to 0.062
Thickness of glass epoxy board (for bonding purposes)	0.060 to 0.100
(Dielectric constant for glass epoxy: 4.8 to 5.4)	

The capacitive coupling between conductors can be minimized by (1) increasing the insulation thickness between layers, (2) narrowing the conductor width and increasing the distance between conductors, and (3) routing circuitry on one layer at right angles to the circuitry on the other layer. In the case of circuits located over the shield or ground plane, the entire length of a conductor is capacitively coupled to that plane, for which allowance must be made in the design.

The calculation of characteristic impedance for microstrip and strip lines in multilayer boards for high-frequency application is a complex procedure and will not be covered here.

3.3.9 Ground Planes and Shielding

Solid copper planes, with clearance holes etched out in areas where no contact is desired, can be placed anywhere within the multilayer board. These planes serve to minimize interference, or cross-talk, between various critical circuits and to shield the circuits within the board from external interference.

3.3.10 Board Design Considerations

Of interest to system designers is the relationship between design requirements and cost of multilayer boards. The overall board size and number of layers do not affect price to any great extent; the density of terminal points or holes and the corresponding density of interconnections are the main variables controlling cost. The approximate dividing line between the cheaper and costlier versions of multilayer boards is the hole-center separation distance of 0.100 inches. Multilayer boards with hole centers spaced 0.100 inches or more apart have room for at least one conductor between the terminals. This makes possible the placement of 0.020-inch conductors on 0.020-inch spacing, and allows registration and hole-location tolerances of at least ±0.005 inches, all of which are well within the state of the art of printed-circuit manufacturing. The production of such boards with good yields does not present any great difficulty. For boards with hole spaces of less than 0.100 inches, all parameters and tolerances must be decreased proportionally. When the design requires 0.010-inch conductors and spacing, and tolerances of ±0.001 inch on layer thicknesses or ±0.003 inch on hole location and layer registration, the price increases rapidly.

To reduce manufacturing costs, a common practice is to process many small boards on a large panel and separate them in the last steps of the manufacturing cycle. If the tolerances are wide, large panels with small individual circuits can be processed without difficulty. Manufacturing costs increase when close terminal-area spacing and tight tolerances are demanded. Panel size must be reduced to ensure accuracy of registration and hole location, so that only a few multiple circuits can be processed simultaneously on the panel. The difference in cost between wide- and narrow-tolerance circuits can be 80% or more.

3.3.11 Device Mounting Considerations

The following are some general rules for mounting components to multilayer boards:

(1) If some discrete components are included in the design, these heavy components should be located near the secured edge of the board to minimize shock and vibration effects.

(2) In high-density packaging all components will normally require heat sinks.

(3) The IC's with the highest dissipation should be mounted on their heat sinks at points nearest the connection to the main heat sink, since such points are the coolest.

(4) Whenever possible, the IC's with the greatest number of interconnections should be located close to each other. This will reduce the complexity of the interconnecting circuitry.

3.3.12 Multilayer Board Costs

It is impossible to give a valid, general price figure for multilayer boards, since they vary greatly in their particulars. Some generalizations are possible for multilayer boards interconnecting IC packages, since in such boards the variations in design are limited. As a rough estimate, these boards can be purchased in large quantities (say 100 boards of a type) for $2.50 to $3.00 per integrated circuit. Continuing improvements in manufacturing processes are expected to reduce the price per IC to $1 eventually. Such prices are quite reasonable for the functions the boards must perform and are in line with projected cost reductions in IC packages themselves.

3.3.13 Delivery Time

From the date artwork for a multilayer board in quantity is approved, the minimum delivery time is about four weeks. To produce and check out the artwork may take three or four weeks, giving a minimum delivery cycle of seven weeks. The user frequently prepares the artwork himself.

As with other equipments, there is no assurance that the multilayer board will operate as specified until the first unit is assembled and tested. Hand-wired breadboards do not exactly reproduce the conditions of the completed multilayer boards, since the parameters of conductors in multilayer boards are quite different from those of wires on breadboards. However, after the prototype-development stage has been completed, system production can be achieved within four to five weeks. Thereafter it is only a matter of scheduling to keep the flow of multilayer boards at the required level.

3.3.14 Conclusion

In their five years of existence, multilayer boards have proven to be efficient, reliable, and economical in large electronic systems. The sharply increasing activity in this field reflects the important role multilayer circuits have assumed in electronics packaging.

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TESTING

F O U R

4.1 Quality Assurance Tests

Quality-assurance tests of the type performed on transistors and diodes can usually be applied to integrated circuits as well. Figure 4-1 shows the sequence of events in a typical test program; it indicates the tests that might be conducted and the various organizations involved. The extent to which these tests are employed depends on the criticality of the device application. Devices intended for noncritical use (industrial equipment, radio, television) usually receive minimum testing before being installed. The manufacturer might, for example, perform only a partial electrical test, and the customer's incoming inspection might consist of only a part count and a visual check for damage. However, a device earmarked for a high-reliability system is generally subjected to extensive testing. The manufacturer is likely to perform mechanical, electrical, and hermetic-seal tests on these parts, along with a reliability study to verify the failure rate and screening tests to detect potential failures. The customer's incoming inspection for high-reliability devices includes both visual and electrical checkout. In many cases the customer's component-engineering group subjects a sample of the devices to tests identical to those performed by the manufacturer. The two sets of data (manufacturer's and customer's) are then compared to verify device reliability.

Devices destined for today's military equipments are generally subjected to the more rigorous program described for high-reliability systems.

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As shown in Figure 4-1, design groups are also involved in performing both static and dynamic (actual circuit) evaluations. The manufacturer supplies device samples directly to the design and component-engineering groups, usually carefully selecting and testing the devices beforehand, if not otherwise directed. When working with such samples, the test engineer must bear in mind that they are seldom randomly selected items.

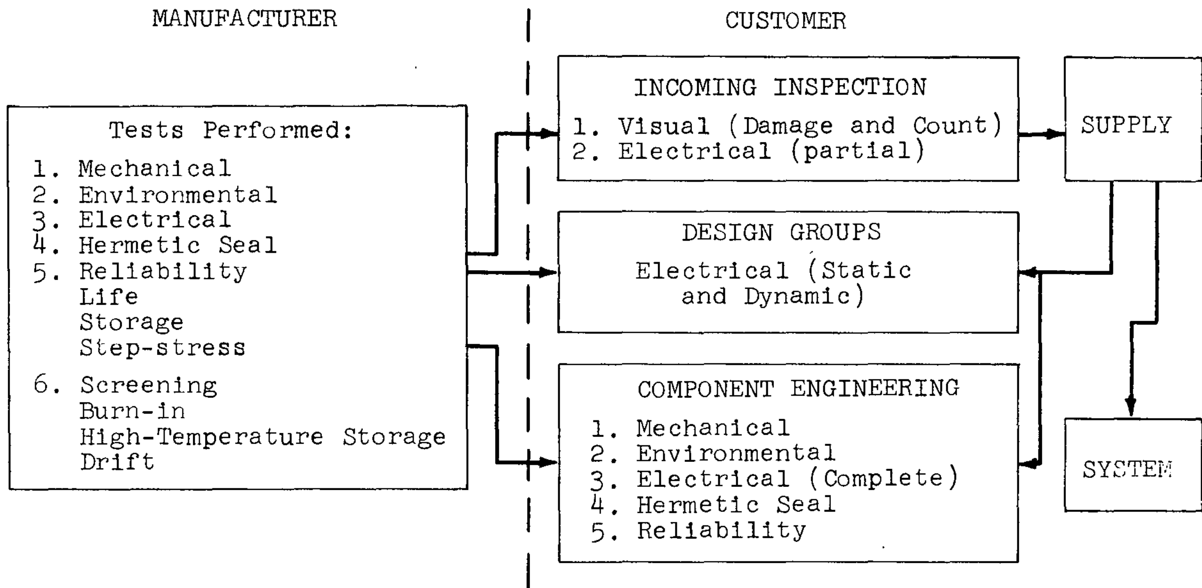

FIGURE 4-1

SEQUENCE OF EVENTS IN TYPICAL TEST PROGRAM

Figure 4-2 indicates some of the problems associated with routing integrated circuits through a test program. For incoming inspection, new test fixtures and procedures are needed for handling the IC packages. Additionally, since IC's cannot always be tested on a go/no-go basis, many tests are quite complex; as a consequence, test personnel must be retrained. Supply groups may encounter difficulties in handling and stocking IC's, since new device carriers are required and stocking procedures must be modified. The small size of IC's poses problems when they are being assembled into equipments or systems. The circuit designer may have trouble interpreting parameters and adhering to design limitations since many IC's have parameters and response characteristics unfamiliar to him. The component engineer may also be faced with the problems of interpreting parameters and dealing with new test equipments, in addition to generating IC specifications and performing failure analyses.

This section concerns various tests, equipments, and fixtures required for evaluating integrated circuits.

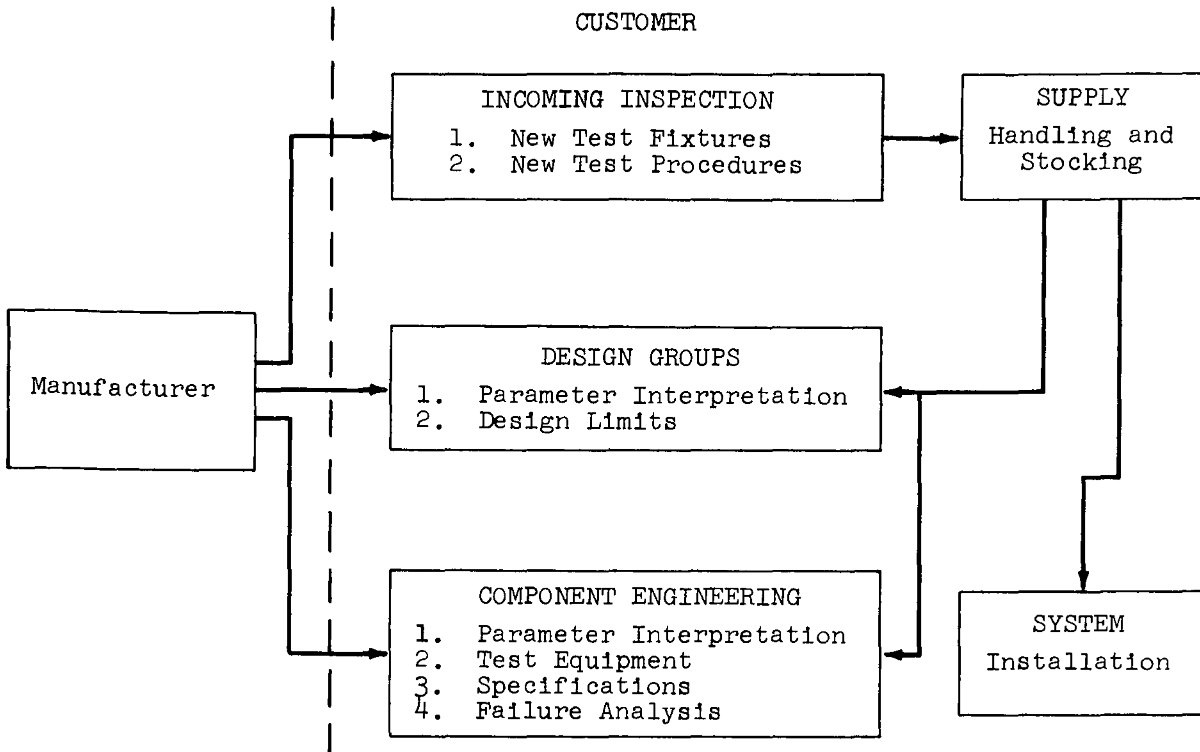

FIGURE 4-2
PROBLEMS ENCOUNTERED IN INTEGRATED-CIRCUIT TEST PROGRAM

4.1.1 Mechanical and Environmental Tests

The mechanical and environmental tests outlined in MIL-STD-202 have been used in the semiconductor industry for a number of years. Included are such tests as shock, vibration, temperature cycling, thermal shock, and moisture resistance. Minor modifications of stress levels are required to adapt the tests to integrated circuits.

4.1.2 Hermetic Seal Tests

The hermetic seal of an IC package can be checked by the gross-leak and fine-leak tests normally used on transistors.

4.1.2.1 Gross-Leak Tests

The most common method of detecting gross leaks in the IC package is the bubble test, in which the package is immersed in a liquid (e.g., silicon oil or alcohol), usually at an elevated temperature; if the seal is defective, bubbles will escape from the package.

Another method of gross-leak detection is the detergent bomb test. The device is placed in a water-detergent solution under pressure; if any gross leaks exist, the detergent enters the package, and a subsequent electrical test will

detect its presence by indicating a change in the reverse current of the device. The detergent bomb test is not recommended for IC's, for the following reasons:

(1) The surface passivation of the chip may prevent the detergent within the package from being detected by parameter measurement.

(2) It is not always possible to measure in an integrated circuit a parameter that is highly sensitive to surface conditions such as I_{CBO}.

A good leak detection for the ceramic flat package is the die-penetration test. The package is immersed briefly in a dye solution under pressure, after which the exterior is washed free of the solution. Visual examination reveals cracks or holes where the dye is trapped.

4.1.2.2 Fine-Leak Detection

Tests for detecting fine leaks utilize a tracer gas. The most common test of this type utilizes the helium-leak detector, which is basically a mass spectrometer set to maximum sensitivity for helium. The package under test is immersed for a short time in helium under pressure. The package is transferred to an evacuation chamber, where an inert gas, such as nitrogen, washes the external surfaces to remove any adsorbed helium. The chamber is evacuated to approximately 10^{-6} mm Hg, and a valve connecting the evacuated chamber to the mass spectrometer is opened. Helium forced into the package through leaks during the pressure cycle now leaks out of the package into the spectrometer vacuum chamber, where it is detected and measured.

The radioactive-tracer technique is similar to the helium test, except that it uses a radioactive medium (such as radioactive krypton). The package is immersed in the radioactive medium under pressure; when it is removed, its exterior is washed free of the medium. It is then placed in a radiation detector: the radiation count is a measure of the amount of radioactive material that has leaked in.

Each leak-test technique has its advantages and limitations. The helium leak test is nondestructive in that any helium remaining inside a package has no effect on the device. The opposite may be true for the dye and radioactive medium, either of which could have an adverse effect on the device even though the amount of dye or gas entering the package is acceptable from the standpoint of leakage. A disadvantage of the helium leak test is that leaks may be overlooked if they are large enough to permit rapid evacuation of all of the helium in the package during the evacuation period. Thus an additional gross-leak detection is usually required.

4.1.3 Electrical Tests

Electrical quality-assurance tests for integrated circuits are similar to those for transistors and diodes. The most common is static burn-in, in which certain d-c bias voltages and currents are applied to the circuit for specified

times and temperatures. After termination of the burn-in period, the general parameters are measured to determine if the device passed the specification limits. In the dynamic burn-in test, a signal voltage superimposed on the specified d-c bias simulates the operational stresses to be encountered by the circuit. The dynamic burn-in test is effective in screening out potential failures, but is also costly.

The electrical burn-in test is one of the best quality-assurance measures available. The time intervals range from 25 to 1000 hours, depending on the device.

4.1.4 Drift (Delta) Test

In the delta or drift test, parameters such as drain currents, gain characteristics, and triggering levels are measured before and after burn-in. A comparison of the two sets of values indicates parameter drift (the specification will state a maximum drift limit.) The main advantage of the drift test is that it indicates those units which may be within specification limits after burn-in but are likely to exhibit drift beyond specification limits at a later date. The drift measurements provide valuable design information, but they are expensive and time-consuming.

4.1.5 High-Temperature Back-Bias Test

In the high-temperature back-bias test, reverse potentials are applied to various semiconductor junctions at elevated temperatures, and changes in leakage currents and breakdown voltages are observed. This test also detects channeling effects in semiconductors. It is not usually performed on digital and small-signal analog integrated circuits.

4.1.6 High-Temperature Stabilization Test

In the high-temperature stabilization test, the unpowered device is heated to a specified temperature for a specified time. This test serves to stabilize the surface states (reduce leakage currents) in the silicon die, detect poor wire and die bonds, and stress the final seal of the package.

4.2 Testing IC Electrical Characteristics

For evaluating the electrical characteristics of the IC, the "specified point" and "black box" test methods can be employed.

4.2.1 Specified-Point Testing

Specified-point testing involves checking the electrical characteristics of the IC between its external leads, or between each lead and the substrate. The responses can be analyzed to determine the IC's ability to perform its various

electrical functions. This technique is always used in IC failure analysis. The test fixture consists of a switching arrangement (Figure 4-3) that places various combinations of the collector, base, and emitter terminals of a curve tracer between the external leads of the IC under test.

An example of specified-point testing is shown in the functional schematic of Figure 4-4. The circuit is a fully integrated power amplifier (Darlington

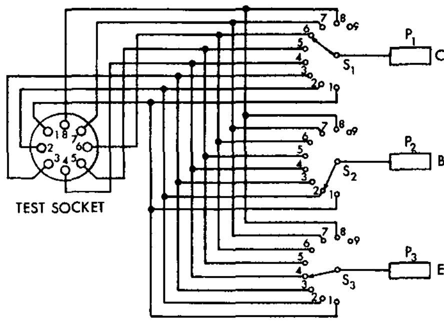

FIGURE 4-3

INTEGRATED-CIRCUIT TEST FIXTURE

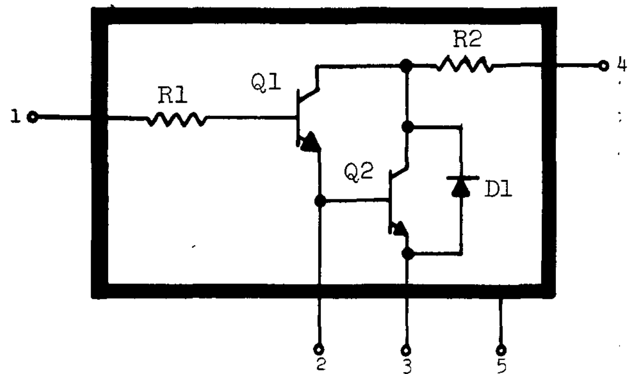

FIGURE 4-4

FUNCTIONAL SCHEMATIC OF POWER AMPLIFIER

configuration) containing two resistors, two transistors, and one diode. Examination of the circuit schematic reveals that both transistors (Q_1 and Q_2) are accessible. This situation would normally indicate that accurate measurements could be made of such parameters as current gain, breakdown and saturation voltages, and leakage currents. However, fully integrated circuits have associated d-c parasitics which often cause parameter variations. Suppose, for example, that a measurement of the current gain of Q_1 is desired. The collector, base, and emitter terminals of the curve tracer (common NPN) are applied to IC leads 4, 1, and 2, respectively. The resultant display on the curve tracer is a combination of Q_1 current-gain characteristics, the leakage currents of the parasitic transistors, and the collector-base leakage of Q_2 (see Figure 4-5). Though these leakage currents are usually small, they can become a problem in power-circuit measurements.

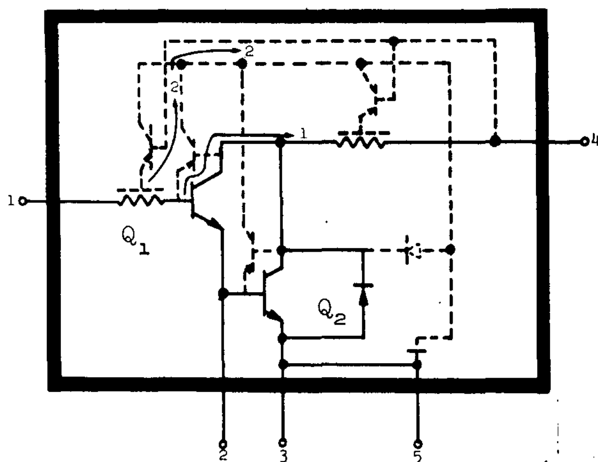

FIGURE 4-5

DC EQUIVALENT SCHEMATIC OF POWER AMPLIFIER

Another test that could be performed by the specified-point technique is the measurement of the collector-to-base breakdown voltage (V_{CB}) of Q_1. This test is performed by switching the collector and emitter terminals of the curve tracer (common NPN) to IC leads 4 and 1, respectively. The display on the curve tracer shows V_{CB} plus all other parasitic junction characteristics. If during this test a breakdown occurs in the Q_1 junction, resistors R1 and R2 provide current limiting for leakage path 1. However, there is no current limiter in the parasitic-junction leakage path 2.

If the engineer knows the equivalent circuit of an IC (including parasitics), he can apply the specified-point test method for an effective d-c analysis of simple circuits. For complex circuits, however, this task becomes difficult, if not impossible, because of the large number of d-c parasitics involved. As mentioned earlier, specified-point testing is generally reserved for IC failure analysis.

4.2.2 Black-Box Testing

In fully integrated circuits, individual components tend to disappear into the physical structure. It is not always possible or practical to check circuit performance by the specified-point method. In the black-box technique, the IC is connected to all supply and bias voltages required for operation, and a signal voltage is applied to the input. Output voltage as a function of input voltage is shown on an oscilloscope, and the output waveform is analyzed. The circuit is specified only by its functional characteristics -- input, output, and transfer. Herein lies the advantage of black-box characterization: no testing is required of individual components (resistors, transistors, diodes), only of those operational characteristics which lie within a prescribed band of values.

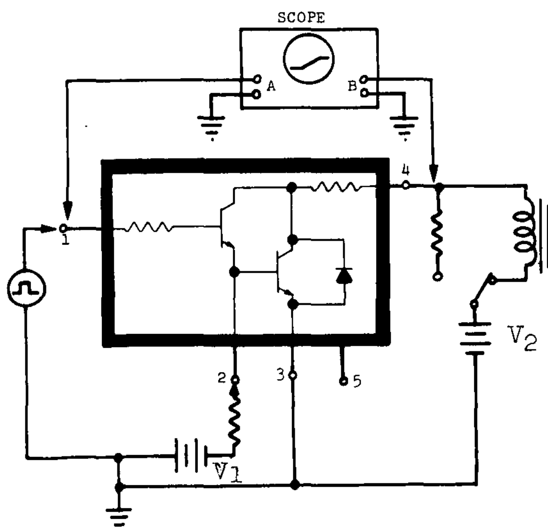

FIGURE 4-6

BLACK-BOX TESTING OF POWER AMPLIFIER

Figure 4-6 illustrate the black-box technique as applied to a power amplifier. Bias voltages (V_1 and V_2) are applied to the IC, and the device is loaded inductively to simulate actual circuit conditions. The input is driven by a square-wave generator, and the input-output response is monitored by a two-channel oscilloscope. Using this test technique, one can determine values for such parameters as dynamic impedance, minimum/maximum operating levels, drain currents, and transient responses. In effect, all necessary operational characteristics of this IC can be determined without a detailed investigation of the package contents (as was necessary with the specified-point technique).

The black-box technique can also be applied to digital integrated circuits. One important measurement in digital IC's is output voltage versus input voltage. Figure 4-7 shows a typical test set-up for this measurement, the digital device being a TTL logic gate. Note that the output of this circuit is leveled. Output loading is necessary for circuits that do not have unilateral characteristics, or whose output resistance is comparable to input resistance over part of the operating range (In the case of the TTL, both output voltage and current are dependent on a load state.) Although this test can be performed on an ordinary oscilloscope with direct input to the horizontal plates, an oscilloscope with a horizontal-amplification capability (Tektronix type 536 or equivalent) will permit more accurate measurements.

To measure the inverse-voltage transfer characteristics, the test leads shown in Figure 4-7 are reconnected, with the second-stage input voltage going to the Y-deflection terminals of the oscilloscope and the second-stage output going to the X-deflection terminals of the scope and to the variable-voltage source. In addition, bias voltages must be provided at the input of the first stage to provide one-input and zero-input logic levels. Two waveforms can be obtained in this manner -- one for an input "one" condition, and one for an input "zero" condition.

Figure 4-8 shows a standard test arrangement for determining input current versus input voltage (using the same TTL as discussed previously). As in the case of the output-voltage versus input-voltage characteristic, a horizontal drive amplification is required. In the present case, however, the vertical deflection must be proportional to the voltage drop across the current-sensing resistor (R). This measurement must be performed with caution on gate circuits with high input impedances, since the current-sensing resistors have high values; thus, the input impedance of the oscilloscope can cause current-shunting effects that tend to make the input impedance of the circuit under test appear lower than it actually is. As in the previous example, a load stage is required to test the circuit under appropriate system conditions.

Figure 4-9 shows the test circuit for evaluating output current versus output voltage. As in the case of the inverse characteristic, curves are obtained for the "one" and the "zero" input conditions. A differential input to the oscilloscope is required to sense the current through resistor R.

Probably the most difficult black-box measurement is the current-transfer characteristic, since R2 (see Figure 4-10) must be large enough to measure current accurately, but not so large as to have an appreciable effect on gate operation.

Other combinations of input and output voltages and currents can also be measured by the foregoing technique. These techniques apply not only to logic gates, but also to flip-flops, Schmitt triggers, and other direct-coupled circuits (Figure 4-11).

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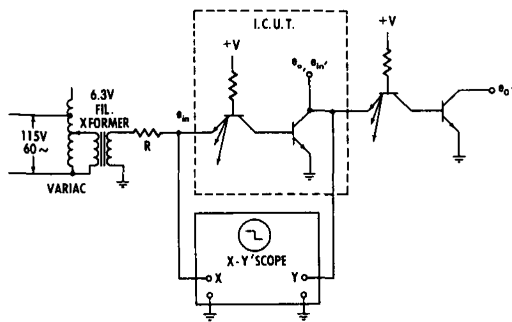


FIGURE 4-7

TEST SETUP FOR MEASUREMENT OF
e_{OUT} VS e_{IN} CHARACTERISTICS (T^2L)

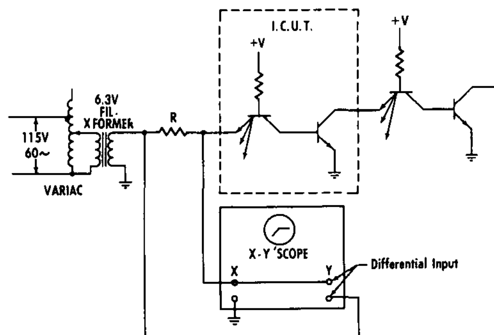


FIGURE 4-8

TEST SETUP FOR MEASUREMENT OF
i_{IN} VS e_{IN} CHARACTERISTICS (T^2L)

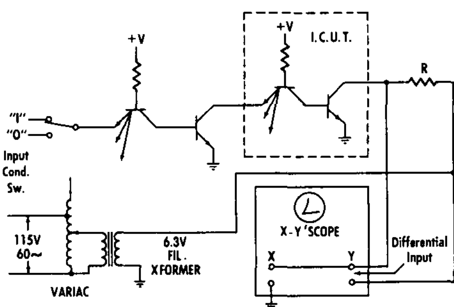


FIGURE 4-9

TEST SETUP FOR MEASUREMENT OF
i_{OUT} VS e_{OUT} CHARACTERISTICS (T^2L)

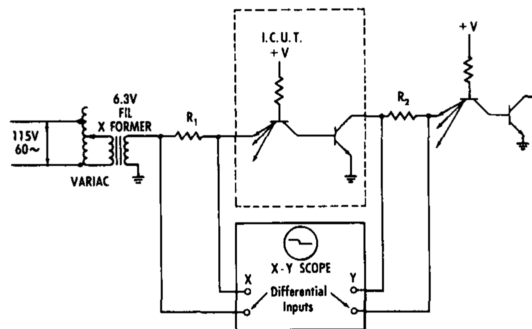


FIGURE 4-10

TEST SETUP FOR MEASUREMENT OF
i_{OUT} VS i_{IN} CHARACTERISTICS (T^2L)

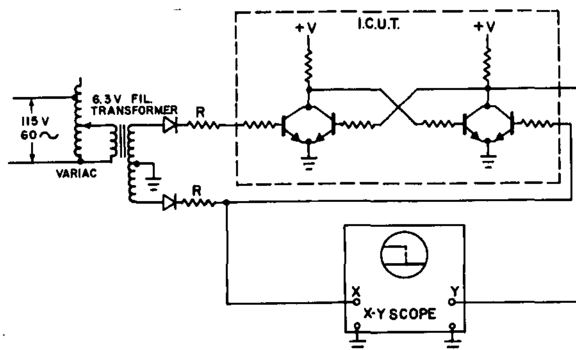
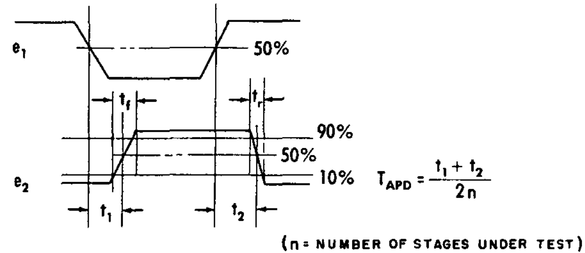


FIGURE 4-11

TEST SETUP FOR MEASUREMENT OF
e_{OUT} VS e_{IN} TRANSFER CHARACTERISTICS
OF AN R-S FLIP-FLOP (RTL)

The switching or transient response of the IC device can be evaluated by a variety of methods. Figure 4-12 shows an arrangement for measuring average propagation-delay time. This arrangement allows a large number of samples to be



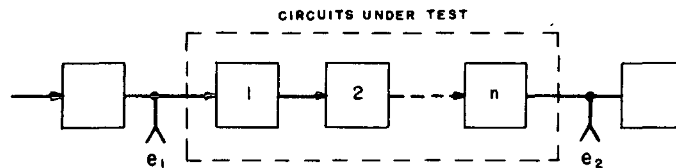


FIGURE 4-12

CIRCUIT FOR MEASURING PROPAGATION-DELAY TIME

checked simultaneously, but this practice has one drawback: the devices could collectively meet the specification requirement although some might be fast and some slow. Therefore, it is usually preferable to test units individually for propagation-delay time. The driving and loading gates can be of either IC or discrete-component form.

4.3 Problems Associated with Testing Integrated Circuits

The most common problem in testing IC's is the variation in normal device operation because of test-fixture capacitance and inductance. All fixtures should be constructed on ground planes with fully bypassed power supplies and minimal lead lengths.

For IC's, all high-frequency measurements (such as roll-off characteristics) are difficult and time-consuming. Oscilloscopes with fast response times are needed to check roll-off distortion during the voltage swing tests.

Other problems associated with IC testing are as follows:

(1) A small impedance mismatch between the driving source and input of the circuit may cause an excessive amount of ringing and greatly distort the driving waveform.

(2) The sequence of application of power supplies is important; if one bias supply is connected before another in some IC's, an internal junction may be forward-biased and excessive current flow may destroy the device.

(3) In many linear circuits, slight variations in bias supplies drastically affect the circuit output. Bypassing is necessary on all power supplies.

(4) Many circuits are required to have good tracking ability with respect to temperature and drift. The test fixtures used for these temperature tests necessarily have long leads, which makes the measurement of transient response extremely difficult.

(5) Noise is always a problem, and discrimination and rejection circuits may be needed.

(6) It is difficult to limit the number of tests to be performed on an analog circuit and still be confident of its performance. Tests such as phase shift, pulse-width modulation, and frequency response are time-consuming but frequently necessary.

The tests for evaluating IC's are quite similar to those for testing discrete-device circuitry at the module level. IC testing differs in that a designer cannot always probe certain portions of the circuit to determine why the output or input functions changed during a test.

4.4 Standard Tests

IC specifications, both commercial and in-house, contain a certain amount of standardization with respect to test circuits. It is feasible at this time to create a general test specification for integrated circuits. Several of the larger manufacturers have generated their own basic product-control specifications. These basic specifications contain definitions of the static and dynamic parameters, test methods, and test fixtures. Standardization efforts have been directed more toward digital circuits than analog circuits.

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4.5 Test Fixtures

A number of companies are producing fixtures for securing and testing TO-5 and flat packages. Unfortunately, many of these fixtures have serious shortcomings. In some, the IC must be welded or soldered into the holder area, and unsoldered or cut upon removal. In others, the IC is clamped in place with inadequate contact pressure, such that test results can be compromised. Some fixtures are not polarized for proper IC insertion. Some do not allow sufficient exposure of IC surfaces for identification markings. Many fixtures cannot be grouped or stacked readily for storage.

Figure 4-13 shows test sockets produced by Barnes Corporation for use with the modified TO-5 package. The major difference between these sockets and those designed for the standard TO-5 is the number of terminals. Some of the sockets are especially designed for ease of insertion, and can accept lead lengths of 0.5 to 1.5 inches. The sockets are polarized and are available with 6, 8, or 10 leads.

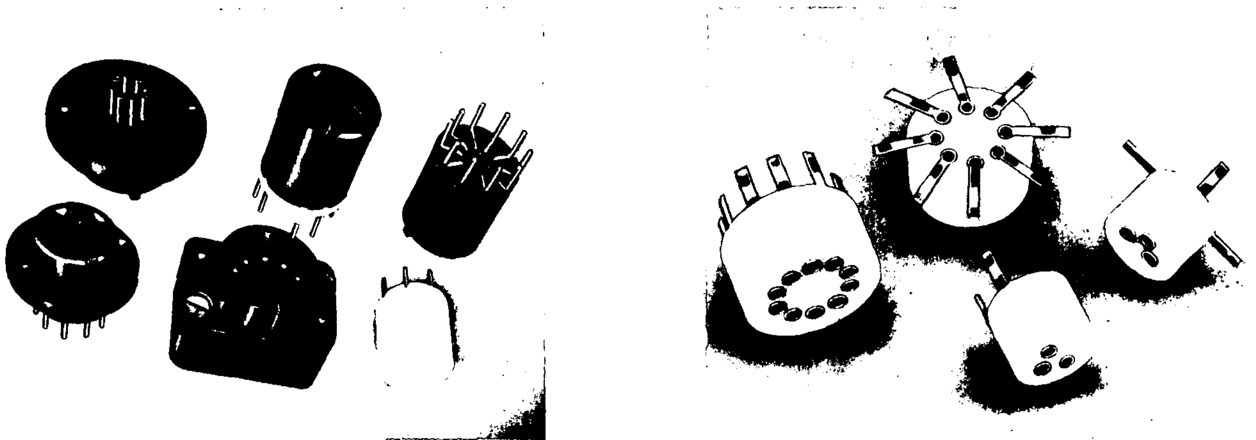


FIGURE 4-13
BARNES CORP. TEST SOCKETS FOR TO-5 PACKAGE

A carrier manufactured by Walkirt Company for the flat-pack configuration is illustrated in Figure 4-14. This carrier accepts a 1/4 × 1/4 or 1/8 × 1/4 flat pack, and converts the IC pin configuration into an arrangement for plugging into a printed-circuit board (0.050 × 0.100 centers). The IC must be soldered into this fixture. The unit price of the Walkirt carrier is about $1.50 in quantities of 1000.

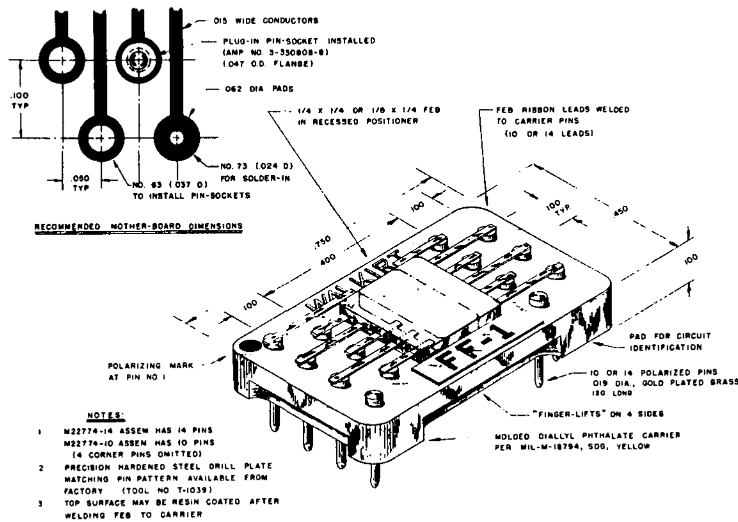


FIGURE 4-14

WALKIRT CO. CARRIER FOR FLAT PACKAGE

Figure 4-15 shows a test board manufactured by Modular Electronics. In this test fixture, the depression of two buttons raises spring-type fingers. The IC is placed under these fingers, the buttons are released, and the package is held in place by the spring-loaded fingers. This fixture accepts the 1/8 × 1/4 flat pack with 10 or 14 leads. The test board accepts standard printed-circuit card connectors. One shortcoming of this fixture is the difficulty of aligning the IC leads directly beneath the spring fingers; the resulting poor contact can lessen the accuracy of test measurements. Sylvania produces a similar carrier which requires that the leads be welded or soldered in place. The unit price of the Modular Electronics fixture is about $3 in quantities of 1000.

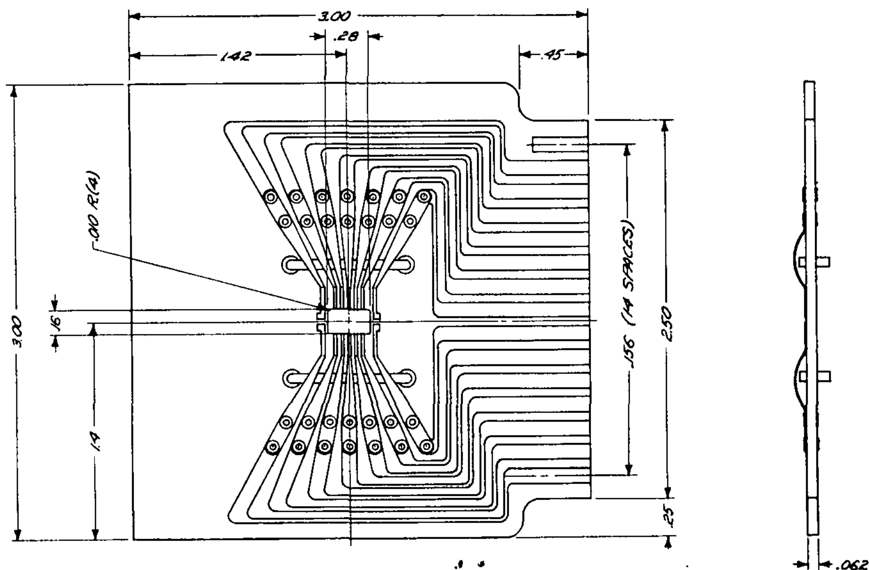


FIGURE 4-15

MODULAR ELECTRONICS CO. TEST BOARD

Several variations of the "flip-top carrier" are available; one produced by the Barnes Corporation is shown in Figure 4-16. The flip-top carrier has the following advantages:

(1) Device leads are positioned automatically by the fixture cavities.

(2) Uniform and adequate pressure is exerted on all leads.

(3) A variety of package configurations, with 10 to 14 leads, can be accepted.

(4) The enclosure can be used for shipping as well as testing, since the fixture completely surrounds the integrated circuit.

(5) The terminals are large enough that wires can be soldered directly to them.

The fixture has terminals that accept the Barnes RD-24 socket. The price of the fixture is about $4 in quantities of 100.

The Westinghouse Auto-Pak carrier consists of a test socket, cover, base, and retainer clip, as shown in Figure 4-17. An IC device can be tested in this carrier and then shipped to the customer. The recipient can perform the same tests, utilizing the carrier with a test socket. The carriers cost 15 cents apiece in quantities of 5,000, and can be returned to the vendor for partial credit after the IC's are removed. The test socket and retainer clip are produced by Barnes Corporation and must be purchased separately.

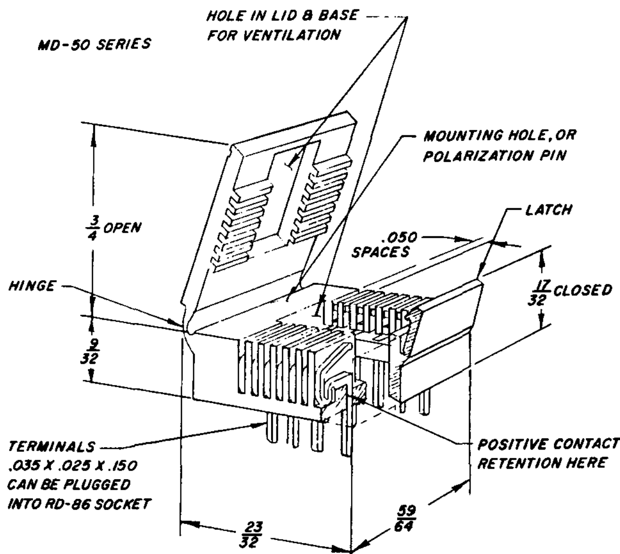
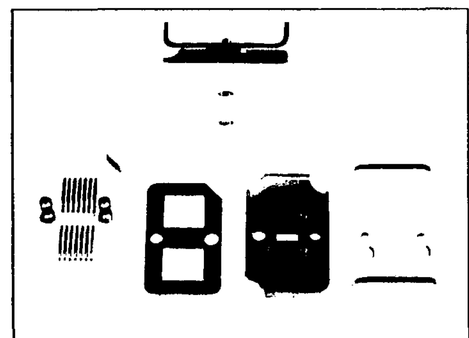


FIGURE 4-16

BARNES CORP. FLIP-TOP CARRIER



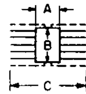
Shown at top is assembly of AUTO-PAK carrier in APS-2 test socket. Below are detail parts (left to right) test socket body, carrier cover, carrier base, and retainer clip.

FIGURE 4-17

WESTINGHOUSE AUTO-PAK CARRIER

An IC test socket produced by Augat Corporation is shown in Figure 4-18. The socket assembly has a double-sided printed-circuit board for use with a standard double-row printed-circuit connector. Two or more units can be installed side-by-side in one double-row connector. The price of this unit is $2.45 in quantities of 1 to 99 (with connector, an additional $2.05).

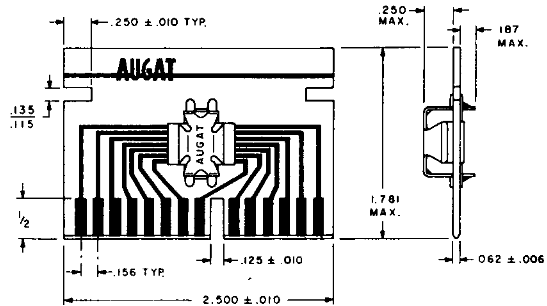
The 8104 SERIES is similar to the 8075 series illustrated on page 6, incorporating a polarization notch and two extractor notches.



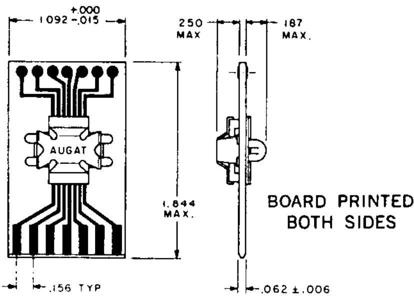
PART NUMBERS

With Connector	Without Connector	A	B	C
8104-1G3	8104-1G1	1/8 .180 Max. 1/4	1/4 1/4 1/4	.500 Min. 1.000 Max.

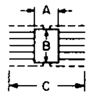
CAN BE FURNISHED FOR OTHER FLAT PACK SIZES



MATERIALS see below



Part no.	A	B	C
8075-39G1	1/8 .180 Max. 1/4	1/4 1/4 1/4	.500 Min. 1.000 Max.



CAN BE FURNISHED FOR OTHER FLAT PACK SIZES

Designed for space-saving applications, this assembly features a double-sided printed circuit board for use with a standard double row printed circuit connector. Two or more units can be installed side by side in one double row connector (example – two units can be plugged into a fifteen contact double row connector)

MATERIALS

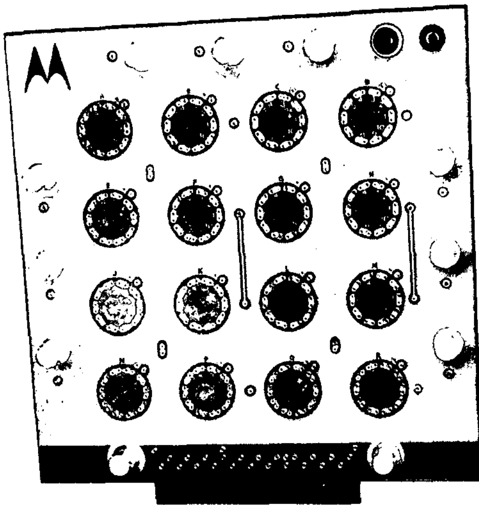
PRINTED CIRCUIT BOARD — 1/16 thick glass epoxy, NEMA grade G-11, copper circuitry, gold over nickel plated

LEAD SEPARATOR — Diallyl phthalate

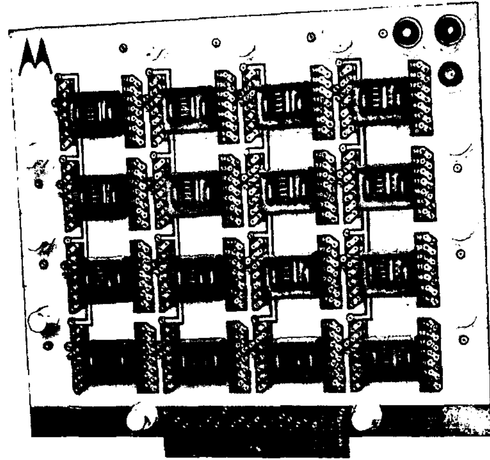
COVER — Spring temper stainless steel
Insulating pressure pad — Silicone rubber

FIGURE 4-18
AUGAT CORP. IC TEST SOCKET

Several types of multiple-unit test boards are available for testing and bread-boarding integrated circuits. Figure 4-19 shows an IC interconnection patchboard (Motorola) which can be used with either the TO-5 or flat pack. Patch cords form the interconnections. A 22-pin edge connector and 9-pin BNC connector are supplied for input-output connections. The boards cost about $200 each in quantities of 25 or more.



XC63

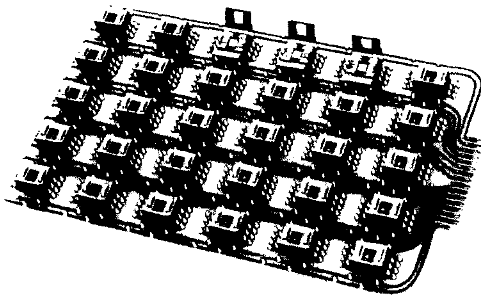


XC72

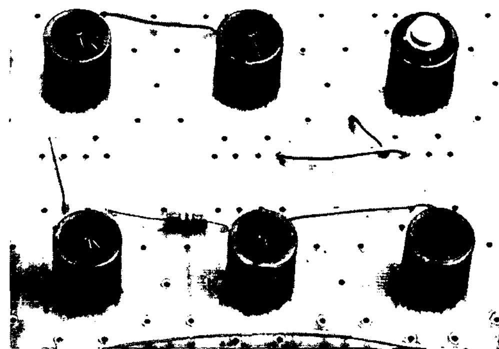
FIGURE 4-19

MOTOROLA IC INTERCONNECTION PATCHBOARD

Barnes Corporation produces test boards for both the TO-5 and flat pack, and with either point-to-point or printed wiring; two types are shown in Figure 4-20.



030-001 BOARD



TYPICAL TO-5 BOARD ARRANGEMENT WITH PLUG IN JUMPERS.

FIGURE 4-20

BARNES CORP. TEST BOARDS FOR IC PACKAGES

The Augat printed-wiring board accepts 50 sockets for flat packs and is equipped with bussing strips for common power and ground connections to the flat packs (see Figure 4-21). This unit costs about $190 in quantities of 10 to 24.

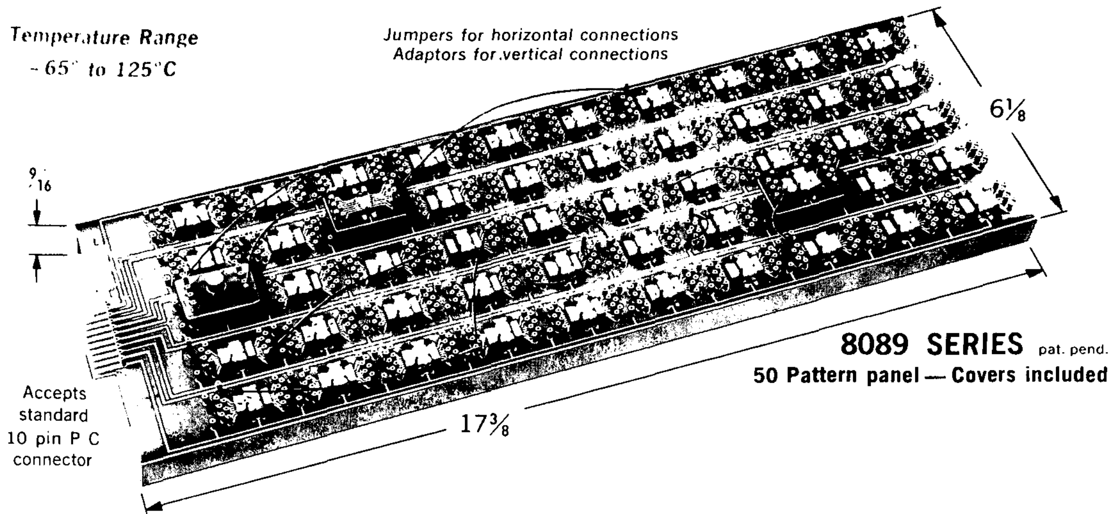


FIGURE 4-21

AUGAT CORP. PRINTED-WIRING BOARD FOR FLAT PACKS

As with test sockets, there is a large selection of test boards.

One of the problems associated with test sockets and fixtures is that IC manufacturers are continually producing new packages, while the socket manufacturers are still trying to make effective low-cost holders for the packages that are already standardized.

4.6 Test Equipment

There are three general types of IC test equipment: engineering, quality assurance, and production control.

Engineering test equipments serve to analyze and evaluate IC's in small quantities. The equipment must be adaptable electrically and mechanically to a variety of circuits and must be easily reprogrammed.

Quality-assurance test equipments are employed by the customer to verify the quality of purchased items. These equipments do not require eleborate programming capabilities, since the few tests they perform are usually of a go/no-go nature. However, quality assurance equipment must offer good repeatability, accuracy, and stability with respect to parameter values.

The manufacturer's production-control test equipment is usually intricate and expensive, since it must perform complex test programs rapidly and accurately. With this equipment, the IC's are automatically transferred from storage racks to test sockets, where 15 to 30 tests are performed on a single device in less than 25 seconds.

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Many IC users are building their own test equipment. In doing so they must consider the following:

(1) Whether the device to be tested is digital or linear. Where both types of devices are to be tested, complex equipment may be required.

(2) Whether the device must be exposed to unusual environments (high temperature, shock) while under electrical test. This requirement could necessitate sophisticated fixtures and testing techniques.

(3) The sequence of testing. An inappropriate test sequence could have an adverse effect on time, cost, yields, and failure information.

(4) The method of measuring transient response. The requirements for fast switching speeds may necessitate several fixture cards rather than a single universal fixture.

A simple test jig for IC evaluation may consist of nothing more than an adapter assembly (for switching IC leads) in conjunction with a curve tracer. The curve tracer cannot perform all of the specified d-c tests listed in the average data sheet, but can quickly check the performance of several IC elements. This procedure represents a simple way of measuring such parameters as the collector node resistance, series base resistance, threshold voltage, current gain, and saturation voltage.

If the user decides to build his own IC test equipment, he should remember that its usefulness is largely determined by the simplicity of its basic design. A complex fixturing scheme built into the tester may be self-defeating. While it may afford a variety of fixturing arrangements, the interaction among them might result in a test of both the fixturing environment and the device under test, rather than of the device alone.

A typical IC test unit for large-quantity evaluations includes several variable power supplies, a pulse generator, a sampling oscilloscope, and various voltmeters, all mounted in a single console. A switching arrangement is included so that the instruments can be connected to any combination of leads on the IC test socket. Before buying commercial test consoles, designers should investigate existing equipment, since these equipments can sometimes be converted for IC testing.

The major characteristics of a few of the currently available commercial test equipments are described below as representative of the general capabilities of microelectronic test apparatus.

Integrated Circuit Breadboard, Engineering Electronics Corporation, Santa Ana, California. This unit contains a signal generator, a power supply, and a development panel that accepts 24 integrated circuits. Its primary use is as a

design tool in the development of circuit functions. However, if a number of circuits of a given type are to be tested, it can be so connected that all critical parameters will be exercised. The circuits are then plugged into the appropriate connector on the development panel. The states of the input and output signals can be monitored by the indicator lights for rapid go/no-go testing. The unit can be used as a design tool, training device, and mobile test unit all in one. The price is approximately $1800 (not including IC test samples).

Series "400" Integrated Circuit Test Set, Fairchild Instrumentation Division of Fairchild Camera and Instrument Corporation, Mountain View, California. Portable and manually operated, this test set measures d-c parameters of integrated microcircuits. It is designed to serve as a standard bench instrument for engineers who have a continuing need for making accurate measurements on small numbers of devices. The flexible programming allows the selection of any desired configuration of connections and forcing functions, and rapid alterations and accurate repeatability of particular programs. The Series 400 consists of five precise, programmable voltage supplies; a variable-range current-measuring circuit; a 10 × 15 pin-board programming matrix; additional front-panel controls for extremely versatile programming; test jacks for optional connection of external devices to various points in the test circuit; and a test socket with adapters for axial-lead, flat-pack, and PC card-mounted devices. The instrument will operate with an accurate digital voltmeter for readout. The Series 400 tester costs approximately $5000.

Integrated Circuit Analyzer, Model IC101, Optimized Services, Inc., Pleasantville, New York. This analyzer provides a rapid means for evaluating, testing, and analyzing IC's. It features four programmable power supplies, a self-contained voltmeter, and a unique slide-switch assembly for connecting any or all IC leads to any of the four supplies. The IC101 costs approximately $1600.

SCAT 24, Continental Device Corporation, Hawthorne, California. This unit tests all electrical parameters for each circuit lead. It will test leakage and drain currents, gain, modulation, transient times, and forward and reverse voltage drops. It also employs such subroutines as self testing, register testing of noise sensitivity, and time-drift characterization. Visual displays on the SCAT-24 include (1) device number, (2) test-sequence number, (3) a four- to five-digit display of test results, and (4) a range multiplier of the results. This instrument can take measurements at frequencies and rise times in the range of 10-100 gigacycles. Its price is approximately $45,000.

Series "4000M" Integrated Circuit Test System, Fairchild Instrumentation, Division of Fairchild Camera and Instrument Corporation, Mountain View, California. The Fairchild 4000M IC test system is a direct-readout type with optional go/no-go data-logging capabilities. This equipment is generally used in production testing, reliability study programs, and manufacturing process control.

Model 659B, Texas Instruments, Inc., Dallas, Texas. This instrument is suitable for testing large quantities of devices. Some of its capabilities are static and dynamic testing; rapid programming; sequenced applications of d-c bias; high resolution for dynamic tests; and automatic addition, subtraction, or averaging of test results.

SPECIFICATIONS AND PROCUREMENT

FIVE

5.1 Introduction

Since the primary purpose of a specification is to inform the supplier of the end-use needs of the purchaser, it may consist of nothing more than a simple description of the product. Depending on the nature of the product and its application, such a specification may be entirely adequate.

On the other hand, a specification may be a complex document that requires the manufacturer to spend substantial sums to qualify as a supplier; it may contain detailed descriptions of every known characteristic of the desired item, making the cost of verification alone many times the cost of the manufacturing operation. There are few such specifications; however, many military and aerospace specifications -- particularly those for semiconductor devices -- approach such complexity.

In addition to informing the supplier of the purchaser's needs (which will be referred to herein as performance characteristics), the more comprehensive specifications set forth requirements that the manufacturer must meet before his product will be accepted by the purchaser. These additional requirements generally consist of procedures for qualification, acceptance testing, and preparation for

shipment. The basic functions with which most specifications for military and aerospace electronic devices are concerned are as follows:

(1) Performance characteristics

- (a) Electrical parameters
- (b) Environmental stress levels
- (c) Reliability
- (d) Physical dimensions and form factor

(2) Assurance-test procedures

- (a) Sample plan
- (b) Test sequence
- (c) End points

(3) Qualification procedures

- (a) Management and administrative requirements
- (b) Process requirements
- (c) Product test requirements

5.2 Performance Characteristics

Performance characteristics and their numerical tolerances are generally determined by the application for which the device is intended. If the application is not reflected in the specification, the procured devices may fail to function properly over at least a portion of the desired operational range. Specified performance characteristics must also be compatible with limitations of the associated manufacturing technology and not imply a requirement to advance the state of the art.

5.2.1 Electrical Parameters

The manner in which electrical parameters are specified for integrated circuits (IC) is essentially identical to that of discrete semiconductors. However, while it is possible to specify all of the electrical parameters considered in the design of the discrete component, this is not generally feasible with integrated circuits, because many IC parameters are inaccessible to measurement. The designer is usually restricted to specifying only those IC parameters involving the input and output terminals of the device and the power supplied in terms of voltage and current.

It is possible for an integrated circuit to be manufactured in such a manner that, even with the terminal parameters well within the specific limits, one or more of the "buried parameters" is either unstable or far removed from its design value, causing the device to fail early. If measurement were possible, the device would be rejected. The only known protection against such a possibility that can be incorporated in an integrated-circuit specification is the "test group" concept.

During preparation of the wafer masks, selected areas on the wafer can be reserved wherein active and passive devices are fabricated with open terminals. The assumption is that elements incorporated in adjacent circuits will possess similar electrical parameters. Those elements within the test groups are accessible to measurement, and their electrical parameters can be specified in a manner identical to that for discrete devices.

There are exceptions to the rule of specifying performance characteristics in accordance with the device application. Some electrical parameters of semiconductor devices can indicate device quality or stability. Although the exact numerical range depends on the device and technology involved, there is generally a range of values for device parameters outside of which the quality or stability of the device becomes suspect. For example, the silicon planar-passivated transistor commonly incorporated into integrated circuits typically exhibits extremely low leakage currents, usually orders of magnitude lower than required by most applications. If such a device exhibits leakage merely approaching the maximum allowable for many applications, it is likely to be an early failure. Although such a device could be rejected because of other requirements given in the specification, the best opportunity for rejection is lost if this parameter is specified according to the requirements imposed by its application. Thus electrical parameters should be limited to the numerical range commonly associated with quality and stability irrespective of application requirements.

5.2.2 Reliability

The reliability levels inherently associated with the silicon monolithic circuit are so high that reliability measurement becomes impractical because of the great number of operating hours required for assessment.

System manufacturers sometimes specify failure rates that the device vendors must demonstrate. If a component is assigned a relatively high failure rate, this requirement may not be a problem. However, many of the failure rates included in high-reliability specifications are extremely low (0.01% to 0.001% per thousand hours). The implications of specifying low failure rates for IC's are pointed out in the following example.

An integrated-circuit specification issued by a major military contractor calls for a failure rate of 0.002% per 1000 hours at a 60% confidence level when the device is subjected to a defined operating-life test. Demonstration of this failure rate at the desired confidence level would require about 5 million device-hours with no failures, or 10 million device-hours with one failure. Even with a relatively large number of devices (say 500) available for testing, one or two years of continuous testing would be needed -- depending, respectively, on whether no failures or one failure occurred -- to assure this level of reliability. The

situation is complicated by the fact that the device is only one of possibly 10 or 20 IC's in a particular system and that several vendors would be attempting to qualify on each device. It can also be seen that as the confidence level is increased, the problem is even further complicated. It is thus impractical to require the demonstration of extremely low failure rates in IC specifications.

Currently, there is no direct quantitative method available for verifying the reliability levels that IC devices can achieve, other than time-consuming and expensive life testing. Many individuals in the field of quality and reliability assurance, when confronted with high-reliability requirements, have therefore turned their attention from failure rates to failure mechanisms. The assumption is that those devices which are free of known failure mechanisms will possess reliability levels equal to or close to state-of-the-art capability.

Since extensive research has been performed in the development of semiconductor devices, virtually all of the failure mechanisms that can be associated with monolithic silicon circuits have been identified. The existence of most of these failure mechanisms can be diagnosed through either visual examination or brief electrical and environmental testing. Failure mechanisms that cannot be so diagnosed but are known to occur can be eliminated or reduced by the specifying of appropriate processes, procedures, and controls.

One of the more important procedural aspects is the requirement for a thorough failure-analysis program: briefly, a detailed diagnosis of failures that occur during processing or under use conditions. Appropriate administrative machinery is required to ensure that information regarding processing inadequacies is acted on in the shortest possible time. However, when basic changes in processing are considered, a careful, and often time-consuming, evaluation is mandatory to ensure that other failure mechanisms are not introduced into the product as a result of process changes.

5.2.3 Environmental Requirements

Environmental characteristics specified for IC devices should reflect the conditions to which the devices will be exposed under use conditions. Additionally, however, all environmental conditions that are related to known failure mechanisms of the devices should be specified regardless of whether the devices will encounter such conditions in use.

The environmental requirements specified for integral circuits are generally the same as those specified for transistors. Applicable tests are described in MIL-STD-750, Test Methods for Semiconductor Devices. It may be noted that these test methods differ from those which military electronic systems are required to undergo. While including all the types of mechanical and environmental stresses required for systems, they are particularly adapted to such low-mass devices as

integrated circuits. Frequently, system manufacturers will specify mechanical and environmental tests for integrated circuits on the basis of the test requirements of their completed systems. It is not particularly desirable to perform these types of tests on integrated circuits, because they will not sufficiently accelerate the potential failure modes.

5.3 Assurance Testing

It should be generally assumed that devices procured to a specification will possess only those characteristics which are verified by the test requirements of the document. This assumption is seldom precisely correct, but it is always advisable because it will usually prevent inadequate devices from finding their way into systems -- whether their inadequacy is due to failure to comply with specifications or to misapplication of the device by the system designer.

In a very real sense, the test requirements alone define the device. The manner in which they are specified is of vital importance, particularly for military and space applications.

5.3.1 Sample Plan

In any plan by which the characteristics of a large population are assured by the testing of a sample, there is a risk of not obtaining an accurate picture of the characteristics of the total poulation. The smaller the absolute size of the sample, and the smaller the sample is in relation to the total population, the greater the risk. The sample test results may give an accurate, pessimistic, or optimistic picture of the true characteristics of the total population. Thus the plan must be selected to give as accurate a picture of the total population as cost and time limitations permit.

The accuracy with which the sample test results reflect the characteristics of the total population is known as the confidence level. For example, if the results of a sample test are being used to state a reliability level for an entire lot, then the maximum assured failure rate increases as the confidence level with which it is assured increases. Thus any statement of failure rate must include information as to whether it is a measured failure rate or a maximum failure rate; if it is a maximum failure rate, then the associated confidence level must also be stated.

Two basic sampling plans, the AQL and the LTPD plans, are used in the semiconductor industry today. The AQL (Acceptance Quality Level) procedure has been in use for a number of years. Under it, an inspection level and an AQL are specified. For each lot size, the inspection level specified determines the number of samples required. The number of samples to be tested increases as the lot size increases, but the ratio of sample size to lot size decreases for larger lots.

MIL-STD-105, "Sampling Procedures and Tables for Inspection by Attributes", specifies the sample size for any inspection level and lot size and stipulates the number of failures permitted for any AQL. The AQL value is roughly the maximum average percent defective permitted if 95% of lot submissions are to be accepted.

The AQL system is known as a "producer's risk" plan because the producer's risk is specified but the consumer's is not. The manufacturer has approximately a 5% chance of having a lot rejected if the percent of defective devices is less than the specified AQL. The lots accepted, however, could have a considerably higher percentage of defectives than the AQL indicates. This method of quality assurance is especially unsatisfactory if the sample size is small.

The LTPD (Lot Tolerance Percent Defective) method of quality assurance has gained increased acceptance in recent years. Under this procedure, assurance is given that only infrequently (generally 10% of the time) will lots with a poorer quality than that specified be passed. Since under this plan the consumer is protected against receiving poor quality 90% of the time, the LTPD system is a "consumer risk" plan; that is, the risk of the consumer is specified.

The relationship between AQL and LTPD is illustrated by Figure 5-1. This curve is the Operating Characteristic (OC) for an AQL of 4.0% at sample-sizes of 15 and 150. An operating characteristic is a measure of the ability of an acceptance plan to distinguish between acceptable and reject lots. The ideal operating characteristic is a vertical line intersecting the abscissa at the desired quality level. This ideal operating characteristic can be achieved only by 100% inspection. At less than 100% inspection, the operating characteristic is a measure of the degree to which the results of the sample test assure the quality of the total lot. For smaller sample sizes, the effectiveness of the AQL procedure is quite poor. In Figure 5-1, for a 4.0% AQL, a sample size of 150 will permit one lot out of 10 with 11% defectives to pass, while a sample size of 15 will permit a lot with 25% defectives to pass 10% of the time.

Under the LTPD procedure, the lower end of the operating characteristic is controlled so that no more than one in 10 lots can pass if the specified LTPD is exceeded. The LTPD's that can be assured by sample sizes of 15 and 150 are 25% and 11%, respectively.

Under the LTPD plan, sample size is independent of lot size. MIL-S-19500 lists sample sizes and number of defectives permitted for various LTPD's. The percent defective permitted in a sample size required to assure a specified LTPD increases as the sample size increases. Under a pure LTPD plan, the percent defective permitted in the sample approaches the actual specified LTPD as the sample size approaches 100% inspection.

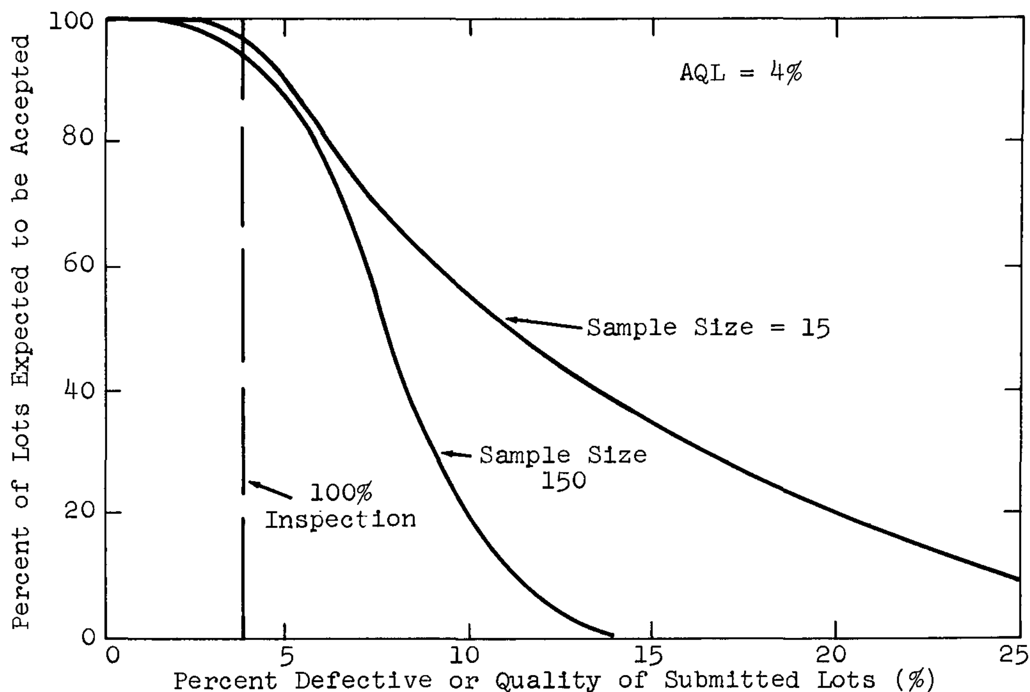

FIGURE 5-1

OPERATING CHARACTERISTICS FOR A 4% AQL

The LTPD's given in typical military specifications are generally larger than the AQL's formerly specified. Thus for large sample sizes greater protection might be obtained from a typical AQL military specification than from an LTPD specification; therefore, a modified LTPD plan is in general use today. Under this modified LTPD plan, a maximum acceptance number or minimum rejection number is specified. (Minimum rejection number equals maximum acceptance number plus one.) Under this procedure the maximum size of the sample is specified. The lot may be accepted after the testing of smaller sample sizes, but the permitted "percent defective" of the sample is lower.

This modified LTPD plan gives added consumer protection against the possibility of receiving defective or out-of-tolerance devices, which is greater with the small lot and small sample sizes of the AQL system.

Typical LTPD levels for current military semiconductor specifications are 5% with a minimum rejection number of 5 for major electrical characteristics, 10 or 20% with a minimum rejection number of 5 for mechanical and environmental tests, and an LTPD per 1000 hours* of 5, 10, or 20% for life test. A minimum rejection number is seldom given for life test because test cost will limit the

* LTPD per thousand hours is designated λ.

size of the samples that can be life-tested for 1000 hours. The cost of testing is a definite limitation on the level of reliability assurance that can be verified by acceptance testing -- especially when acceptance tests are performed by sampling logs that have been accumulated as a result of specific customer orders.

It is seldom economically practical to assure the operating-life reliability of a given lot of integrated circuits much below the 10% level. For example, to demonstrate a λ of 1% (assure with 90% confidence that the lots will have no worse a failure rate than 1% per 1000 hours), a sample size of 231 might be tested with no rejects permitted, or 1 reject might be allowed in a sample size of 390. The sample size would have to be 1,521 if 10 rejects were to be permitted. To demonstrate very low failure rates for lot acceptance, testing costs make it necessary to use sequential-test procedures in which the sample test results of a given lot are combined with test results of preceding lots to determine the average reliability level.

5.3.2 <u>End Points</u>

Generally, the criterion of failure for environmental testing is determined by the effect the stress condition has on the electrical characteristics of the device. These characteristics and their associated limits are referred to as end points.

When only one or two characteristics are used as end points, they should be the device characteristics that are the most sensitive to the particular environmental stress applied. Specifying all or a large number of end points is time-consuming, costly, and generally unnecessary.

Three methods of specifying end-point limits are in common use today:

(1) The end-point limits are the same as the initial electrical limits, e.g., Gain = 20 min., 40 max., initial and end of life.

(2) The end-point limits are relaxed from the initial limits, e.g., Gain = 20 min., 40 max., initial; and 15 min., 50 max., end of life.

(3) The maximum shift of parameter characteristics is specified on an individual basis; e.g., the change of Gain for any circuit must be less than ±20% during the life test.

The second method has been the most widely used. The first method is often used for "high reliability" specifications, but its value is somewhat questionable. This method of specifying end-of-life limits does not take into account any possible inaccuracy in repeating parameter measurements during a life test of several weeks. If minor shifts in characteristics are causing problems in meeting the

end-point limits, the manufacturer can institute a parameter screen to select devices to tighter limits then those initially specified. Thus, in effect, no greater parameter stability than that given by method 2 is assured.

The third method, which is to specify permitted parameter shift on an individual-unit basis, has considerable merit for assuring the delivery of stable circuits. This method is the most expensive of the three to implement because it requires that data on each characteristic be recorded and that calculations be performed on the shift of each characteristic for each unit to determine if the lot meets the specified quality-assurance provisions. A precaution that must be observed when this method is used is to be sure that measurement accuracy is much greater than the parameter shift permitted. For example, an integrated-circuit input diode may have a maximum reverse-current limit of 10 nanoamps (10×10^{-9} amperes), with the median of the distribution being a fraction of a nanoamp. It is most impractical to measure, after 1000 hours of life, even a 50% change in reverse current that was a fraction of a nanoamp initially. A specification that uses parameter shift as a criterion should specify a percentage shift or an absolute value, whichever is greater. For example, for an input diode with an initial limit for leakage current of 10 nanoamps, the end-of-life limit in relation to the initial values could be specified as +50% or +2 nanoamps, whichever is the greater current.

5.3.3 Electrical Performance Testing

Historically, tests at 25°C (room ambient temperature) have generally been used in the semiconductor industry to assure electrical performance. On occasion, an extreme temperature test, such as high-temperature leakage current and low-temperature current gain, have been included when performance under extreme temperatures was essential. Thus, for discrete semiconductor components, a minimum of high- and low-temperature testing has been required because the performance of transistors and diodes over a range of temperatures has been well understood and is quite predictable. The problem of extreme-temperature performance in integrated circuits is much more complex. All semiconductor devices exhibit changes in electrical performance that are a function of the temperature at which the characteristic is measured. The relationship of these temperature-dependent characteristics in an integrated circuit is often hard to predict.

Early in the procurement history of a particular integrated circuit, it may be necessary to measure several electrical parameters at other than room temperature. As data are accumulated on that particular circuit, it should be possible to reduce the number of parameters that must be measured at extreme temperatures and thereby reduce testing costs.

5.3.4 Reliability Screening Tests

Reliability screening tests are those tests performed on an entire lot of integrated circuits to eliminate potential failures. Such tests must be selected

with extreme care. They must be severe enough to eliminate potential failures, but not so severe as to weaken the circuits that survive. The development of proper reliability screening tests requires a detailed knowledge of potential failure mechanisms for circuits produced from the particular design and process being used. The most effective screening tests for circuits manufactured by one process are not necessarily the best for circuits of a different design or manufacturing process.

A screening often specified for integrated circuits in which reliability is of paramount importance is the power burn-in test -- operating each circuit under an accelerated life-test condition for a period between 24 and 250 hours. This operating life test, performed on a 100% basis, will remove early-life failures from the total population and assure a high degree of performance-characteristic stability.

5.3.5 Reliability-Assurance Testing

Reliability assurance tests often involve accelerated stresses applied to integrated circuits on a sample basis to assure the quality of a given production or customer lot. Many of the reliability-assurance-test sequences are destructive; i.e., the circuits subjected to these tests may not be shipped or subsequently used in electronic equipment. Usually, all of these test stresses are greater than those which will be encountered in integrated-circuit equipment operation. Table 5-1 shows a typical integrated-circuit reliability-assurance test plan. This schedule will include mechanical, environmental, and life tests. Where several tests are included in one subgroup, the same sample of circuits is subjected to the test in sequence. The failure criterion for these tests is visual damage or inability of the circuit to meet specified electrical end-point tests.

Further details on reliability assurance testing are given in Section 6.3.

The key element of an integrated-circuit procurement specification, from the cost and time viewpoint, consists of the reliability-assurance provisions. Reliability-assurance tests are expensive from the viewpoint of both test cost and the cost of units used. They are often very time-consuming and adversely affect delivery schedules. The importance of standardization cannot be appreciated as much by an individual systems manufacturer looking at his own circuit requirements as it can by an integrated-circuit manufacturer looking at the requirements of a number of his customers. Integrated circuits are often procured in lots of 10's and 100's. It is obviously not feasible to perform different reliability-assurance tests for all of these procurement lots. Standardization of reliability-assurance tests would materially reduce the cost of integrated

TABLE 5-1

INTEGRATED-CIRCUIT RELIABILITY ASSURANCE PLAN

Examination or Test	Conditions: Mil-Std-750 Method	Conditions: Specific Conditions	LTPD	Max. Acc. No.	Symbol	Limits: Min.	Limits: Max.	Unit
Subgroup 1								
Physical dimensions	2066	--	20	5	--	--	--	--
Subgroup 2								
Soldering heat	2031	1 cycle			--	--	--	--
Temperature cycling	1051	Test Cond.B, T(High) = 175°C			--	--	--	--
Thermal Shock (glass strain)	1056	--	20	5	--	--	--	--
Moisture resistance	1021	--			--	--	--	--
Endpoints: (Same as subgroup 7)								
Subgroup 3								
Shock	2016	5 Blows, X_1, Y_1, & Y_2, 1,5000 ½msec (Total 15 Blows)			--	--	--	--
Vibration fatigue	2046	20G (nonoperating)	20	5	--	--	--	--
Vibration variable frequency	2056				--	--	--	--
Constant acceleration	2006	20,000G, X_1, Y_1, Y_2			--	--	--	--
Endpoint: (Same as subgroup 7)								
[1,2] Subgroup 4								
Terminal strength*	2036 Cond. E	3 leads at random	20	5	--	--	--	--
[1] Subgroup 5								
Salt atmosphere [3] (corrosion)	1041	--	20	5	--	--	--	--
Subgroup 6								
High temperature life (nonoperating)	1031	$T_A = 175^oC$	λ=20	--	--	--	--	--
Endpoints: (Same as subgroup 7)								
Subgroup 7								
Steady state operation life	1026	$T_A = 125^oC$ [4] normal operating Bias applied 60 cps sine wave input	λ=20	--	--	--	--	--
Endpoints: D.C. output levels as indicated on the individual data sheet.								

[1] Tests listed in these subgroups are considered destructive.

[2] At the conclusion of the testing in subgroup 4, the device shall be examined for evidence of mechanical damage.

[3] The device shall be examined for destructive corrosion and illegible marking.

[4] If the normal power dissipation requirements of the circuit do not elevate the junction above the maximum rated 175°C condition. Otherwise special considerations must be taken for each circuit.

*For Flat Package: Weight - 3 oz.

circuits and at the same time increase the reliability assurance, i.e., permit larger sample sizes. If several manufacturers are buying to the same reliability-assurance test sequence, then the cost of testing can be distributed across these several customers.

The delivery-time element of high-reliability procurement specifications is often disregarded. Most writers of specifications for high-reliability parts include a special reliability screen, performance-assurance electrical test, and sample reliability-assurance sequences. If a unique reliability-assurance screen is required, the testing process cannot begin until the order is received, and the promised delivery date will be based on an estimate of the time required to perform the full screening-test sequence followed by performance and reliability-assurance tests on samples. Since the reliability-assurance tests alone often require two months to perform, the promised delivery dates are often far in the future. The possibility of missing a promised delivery date is great because there is no assurance that the lot submitted to reliability screening will successfully pass the reliability-assurance tests until the last end-point measurement is made. If the lot fails, the entire sequence must be repeated.

Table 5-2 outlines the interrelationships of reliability, cost, and delivery.

TABLE 5-2

RELIABILITY/COST/DELIVERY TRADE-OFFS

Test	Test Level*	Additional Cost ($)	Normal Delay In Delivery Time	Valve For Reliability
Power Burn-In	100%†	Moderate	Moderate	High
Drift	Sample 100%	Moderate High	Moderate Long	Medium Medium
High-Temperature Storage	Sample 100%	Low Low	Short Short	Low Low
Environmental	Sample 100%	Low High	Short Long	Medium Medium
Hermetic Seal	Sample 100%	Low Low	Short Moderate	High High

*Sample = 30% or less. †Normally.

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5.4 The Line-Qualification Concept

The practice of qualifying a manufacturer to produce a particular part has been commonplace in military specifications for a number of years. Part qualification generally depends on standardization of operating characteristics, since such qualification is based on a particular end-use item. On the other hand, most specifications utilizing the part-qualification concept contain no provisions for the standardization of various tests and processes. In essence, this approach attempts to force standardization in areas where it is considered unfeasible and to omit standardization in areas where it is practical. In addition, for any qualification concept to acquire the desired result, it is necessary that a reasonably continuous production process be maintained. This implies a continuous demand for a specific item, if the individual-part-qualification concept is to be successful. Technological innovations and economic factors usually prevent a long and reasonably constant demand for any specific item. Therefore, as standards or use patterns change, requalification or qualification for other items is required under the part-qualification concept.

The concept of line qualification has the potential for eliminating, or at least minimizing, many of the undesirable aspects of part procurement that are attributable to qualification based on specific part types. It is based on the fact that most production lines produce a variety of end-use items that differ only in their operational characteristics. The quality and reliability of parts fabricated from the same basic materials and processes are essentially identical. For example, a typical transistor production line may produce a family of six devices that cover a broad range of forward-transfer characteristics. Each transistor type in this family will possess unique operational characteristics suited to a particular application. However, the inherent reliabilities of all six devices in this family are identical. In other cases, minor alterations in a production process make it feasible to produce thousands of part types all of which possess unique operating characteristics but are essentially identical with regard to quality and reliability. For example, a production line that produces integrated circuits on a standard substrate, and has as its only process variable the pattern of the deposited intraconnections, could produce over 100,000 devices which, though operationally unique, would possess the same reliability.

Line qualification would qualify a manufacturer to produce a class of parts on a single production line. Current qualification procedures and tests, with slight modifications, can be utilized for this purpose. Limits on the operational characteristics would be established in all instances in which there is a known relationship between the part failure rate and a particular operating characteristic. In other instances, limits would be necessary to provide a reference for quality-assurance testing. Where such limits are established, they would constitute a "window" at the end of the production process through which only the acceptable parts could pass.

Effective use of the concept of line qualification will require that the quality decision be made on the parts before unique operating characteristics are established. Therefore, the failure criteria for quality-assurance testing cannot be established on end-use operating parameters. It is, however, feasible to use the delta-testing technique, in which failure criteria are based on a maximum allowable variation for a particular operating parameter.

An important condition in the concept of line qualification is that all quality- and reliability-assurance testing is performed before purchase orders are received. The parts are stored in controlled storage facilities (bonded warehouses) until subsequent screening is performed to select operational characteristics to a particular purchase order. Additional testing may be performed at the time of purchase to assure operation of the part in some unique application not covered by the established quality- and reliability-assurance program. Essentially, this additional testing, whether of an environmental or operational nature, will be in the form of screens. Controls are necessary to prevent return to the controlled storage area of parts that have been degraded by such screens.

Properly administered, the line-qualification concept will provide the following advantages over qualification by individual part types:

(1) The cost of parts will be reduced, since qualification costs are amortized over a broad product base. In addition, the removal of specialized testing and process specifications from the areas of manufacturing and quality-assurance testing would substantially increase the efficiency of these operations and further reduce cost.

(2) Delivery time will be shortened significantly. Under the part-qualification approach, which forces manufacturers to comply simultaneously with a large number of specialized testing and process specifications, delivery time often exceeds six months. Delivery time under the line-qualification approach is expected to be less than two weeks.

(3) The part manufacturer will be able to pace his production process at a reasonably steady rate and let the controlled storage area absorb the normally erratic influx of purchase orders. The degree of production control required to produce many types of parts -- to the requisite reliability level associated with their particular application -- is virtually impossible if the production and quality-assurance processes are not maintained at a continuous and steady rate.

Any approach to high-reliability procurement specifications must face the economic realities of industry. If manufacturers are to institute expensive qualification and reliability-assurance programs, there must exist a sufficient demand for the parts manufactured under these programs. Line qualification permits the manufacturer to associate a broad product base with a given program,

thereby increasing his market. Since his production-line and quality-assurance investment is not dependent on the market for specific part types, he is able to operate at a considerably lower financial risk.

5.5 Commercial Specifications

A typical digital-IC specification (Stewart-Warner DTL Dual NAND Gate) is shown as Exhibit 5-1.* This specification has a format similar to that used for transistors; included are (1) a description of the intended application, (2) a brief description of unique parameters, (3) absolute maximum ratings, (4) electrical characteristics, (5) schematic and logic diagrams, and (6) package configuration and dimensions. Note that the parameter terminology resembles that which describes a piece of electronic equipment. These parameters are the "black box" type, describing only the input and output characteristics of the IC device. The characteristics of individual components inside the IC are not usually specified in this document.

Exhibit 5-2 is a more complete specification (Signetics DTL Gate). It includes curves describing typical device characteristics, brief application notes, and a few test circuits.

What are the major features of a commercial specification? This question is best answered by a point-by-point examination of such a specification (in this case, one describing a J-K flip-flop produced by Sylvania; see Exhibit 5-3). The description of the fabrication process -- monolithic silicon epitaxial -- indicates that the device is produced by a standard technique. At the bottom of the first page is a brief discussion of how the circuit functions, information that may be helpful to the circuit designer if this function is complex.

A number of device parameters are specified on page 3, -- among them temperature ratings and thermal gradients, which should always be included in a specification but are often omitted in the commercial IC type. Note that this device has an operating-temperature range of 0° to 75°C, which may restrict its use in some airborne systems. The specification should give minimum/maximum limits for all critical design parameters, especially at the temperature extremes. Many of today's commercial specifications omit such limits for the majority of the parameters, giving typical values instead.

Any transient-response parameter listed in the specifications should be clearly defined, as is done in Figure 10 of Exhibit 5-3. A complete description of the test circuit and waveforms should be included, as shown; without this information, parameter limits are meaningless. Correlation of transient-response data is very poor unless all tests are performed on similar test equipment and under identical circuit conditions. The correlation problem is so acute that the manufacturer often builds two identical transient-test sets and allows his customer to use one of these sets for incoming inspection.

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* See page 5-23.

Exhibit 5-4 is a typical analog IC specification that describes a Motorola differential amplifier composed of two monolithic chips in a modified TO-5 package. The specification format is the same as that for the digital IC device except that the parameters and tests are usually more detailed, for reasons discussed below.

Exhibit 5-5 describes an 8-watt 4-chip servoamplifier (produced by Norden) which is housed in a TO-53 power-transistor package. The data sheet contains a pictorial description of the package contents, which is helpful for analyzing the circuit. Also, the gain stability is specified over a temperature range.

The specification appearing as Exhibit 5-6 describes a general-purpose amplifier designed by Autonetics and produced by Texas Instruments. Circuits of this type are being used in the Minuteman guidance system. Note that three basic test circuits check out the entire amplifier, which is contained in the $1/8 \times 1/4$ flat pack (14 leads).

5.5.1 Differences Between IC and Transistor Specifications

Typical IC and transistor specifications differ in several important respects:

(1) Since the IC is a combination of devices (even though it may be contained in a single monolithic chip), the specification parameters will be similar to those for an equipment composed of discrete parts. Instead of breakdown voltages there are supply voltages or minimum operating voltages, and rather than leakage currents there are input-reverse or power-drain currents. New terms in the IC specification include common-mode rejection ratio, discrimination factor, propagation delay time, and others. In many cases, detailed design parameters and application data will be quite limited in the IC specification. The user must work with each type of device to exploit its full capabilities; this is especially true with the analog (linear) types.

(2) The schematic presented in the IC specification represents only the basic device function, not the true electrical equivalent. As has been discussed, monolithic-circuit diodes are really shorted transistors; transistors are four-layer devices with associated, complementary transistors; and resistors have associated transistor-capacitor characteristics. One must therefore be careful in using the schematic for analyzing circuit response.

(3) Because of the newness of IC's, most IC specifications describe the tests necessary for checking the parameters specified in the document. These tests vary from vendor to vendor, even for the same parameter. The standard electrical tests of MIL-STD-750 are inadequate for integrated circuits.

5.5.2 Developing the IC Specification

Many types of analog and digital IC's are described by commercial specifications. The system designer can frequently use these commercial devices as off-the-shelf items (i.e., without modification). However, in many programs the general trend has been toward in-house specifications, especially for a new product. In-house specifications can be simple, consisting, for example, of a burn-in requirement imposed on a commercial specification; or they may be complex, perhaps describing a custom-type circuit. If the designer cannot utilize one of the standard commercial integrated circuits, he must prepare a specification and submit it to the solid-state industry for price quotations. This procedure might involve the following steps:

(1) The circuit must be analyzed to determine if it can be integrated by standard techniques, and whether it is to be the monolithic, thin-film, or hybrid type. These decisions often require close coordination between the device user and manufacturer.

(2) The decision must be made whether to specify parameters in a black-box or specified-point manner. The parameters discussed thus far are considered the former type, since they describe the sum of the individual components in the IC device. In some IC applications, the characteristics of one or more of the individual components (transistors, resistors) are required by the device user, in which case the specification must include specified-point as well as black-box information. An extreme example of specified-point parameters for IC's can be found in Exhibit 7, a specification for a master die*. Note that the individual characteristics of the resistors and transistors are specified under "Electrical Characteristics", even though these resistors and transistors are contained in a single monolithic silicon chip. Generally, however, IC's requiring specified-point parameter descriptions do so only for a few components in the silicon chip. The black-box description is usually preferred by both vendor and user.

(3) The minimum number of tests needed to describe the IC adequately must be determined. For analog IC's, some parameter tests can be quite complicated, and should therefore be completely described in the specification, including test parameters, minimum and maximum limits, a schematic description of the test circuit, types of equipment to use, and waveform and component values.

(4) The specification should classify the various tests according to inspection level. These levels establish the number of IC's to be

*The master die is generally used as a design tool. The resistors and transistors, contained in a single monolithic silicon chip, have their electrical contacts (base, emitter, etc.) brought out to a metalized island. This allows the circuit engineer to fabricate his own design by interconnecting the various components to form the circuit.

tested in various cases. Some tests (e.g., quality assurance) must be imposed on every IC. Other tests may be concerned with noncritical but still important parameters, in which case testing can be conducted on a sampling basis. Careful consideration should be given to which tests are to be performed on a 100% inspection level, since testing adds substantially to the cost of IC devices.

(5) Schematic and logic diagrams (if applicable) should be included. The schematic should indicate only the basic function, not the parasitics.

(6) The package configuration should be presented, its dimensions having wide enough tolerances to facilitate the selection of alternate manufacturing sources.

5.5.3 Quality-Assurance Requirements

The IC specification will contain additional requirements if it is of the military or high-reliability type. Electrical, environmental, and mechanical tests will be included in the specification to ensure the reliability of the circuit. One of the most valuable of these quality-assurance tests is electrical burn-in. For this test, care should be taken in specifying the burn-in time, since 100% inspection is required -- and device cost is directly related to test time. The time requirement should either be based on the vendor's data or established as test data become available. Dynamic burn-in is usually preferred over static burn-in for pinpointing potential failures, but is more complex and time-consuming with respect to test fixtures. Typical burn-in times for IC's are: commercial, 0-24 hours; military, 160-240 hours; and high reliability, 240-500 hours. The military and high-reliability devices are also given a 1000-hour life test on a sample basis.

5.5.4 The Alternate-Source Problem

A first impression of today's IC market is that device standardization is impossible. Until recently, JEDEC numbers (6N500, 10N80 etc.) were not assigned to IC's. Also, one manufacturer recommends DTL, another TTL, another RTL, and recently MOS-FET has taken its place in the field; the market offers various types of IC packages. Closer examination of the IC market, however, shows that alternate sources for established off-the-shelf circuits are appearing in increasing numbers. Several of the smaller IC manufacturers have negotiated with the semiconductor giants and have obtained the right to produce identical circuits. As mentioned previously, there are standardization trends toward the modified TO-5 and the $1/8 \times 1/4$ flat package.

Thus if one surveys the IC market with more than just a quick glance, he will find that the multiple-sourcing problem is not as difficult as it first appears, particularly with respect to digital circuits. Some multiple sourcing has been accomplished in analog-type IC's as a result of in-house specifications developed

by the large system manufacturers. An example is the Minuteman program, for which Texas Instruments and Westinghouse are alternate sources for several analog devices.

5.6 Checklist for Integrated-Circuit Specifications

The following items constitute a basic checklist for integrated-circuit procurement specifications:

(1) Is the circuit being specified as a standard circuit or does it require custom design? If it is a standard circuit, the procurement cycle is materially reduced because parts are already available at the integrated-circuit manufacturer.

(2) Are the required performance tests adequately specified? The difference between listing a performance requirement in general terms and listing it in specific terms must be understood. Most maximum ratings are included in specifications in general terms. When a specification is reviewed, the general ratings and requirements should be carefully analyzed and the specification not be accepted by the integrated-circuit manufacturer unless the general requirements are acceptable. It must, however, be realized that unless the general requirements are backed up with specific tests to be performed on each production lot, they will not be verified by test for each lot of integrated circuits. For example, if a specification contains a general statement that the integrated circuit shall operate over a temperature range of -55°C to 125°C and yet include only specific 25°C performance tests, it should not be expected that the same electrical limits that are guaranteed at 25°C by test will be applicable at the temperature extremes.

(3) Every specification should include quality-assurance requirements. Merely stating that an integrated circuit shall have specific characteristics is not sufficient. The specification should include the quality-assurance requirements to be applied to the various performance and reliability characteristics. It should list an LTPD or AQL for the specific electrical and reliability-assurance tests that are required. These LTPD's or AQL's should be carefully specified for the best compromise between the assurance required and the cost of this assurance. Certain electrical parameters should have tight quality-assurance requirements -- generally those which are critical to the circuit performance and which can vary as a result of process variations. Others that are perhaps less important to the performance of the circuit, or are strictly design considerations, should have looser LTPD and AQL provisions. The proper selection of the quality-assurance requirements will materially reduce the cost of integrated circuits without impairing the performance or reliability.

(4) The reliability screens that are specified should be effective in removing potentially poor individual circuits from the total population without impairing the quality and reliability of the circuits that are not removed from the population.

(5) The reliability-assurance tests should be in a standard format and should be an effective compromise between the reliability assurance required and the cost of reliability assurance.

(6) The element of delivery must be considered in the development of the procurement specification; otherwise, the integrated circuits may not be available on a timely basis.

(7) The element of cost is critical. Does the specification require special testing techniques that are not standard? If it does, the cost of the circuits will be materially increased. Does the specification have performance requirements that cannot be met with standard products? If it does, the cost will again be increased because the integrated-circuit manufacturer must start special material into the production line rather than use standard material from which he can select to a customer's specific electrical requirements. Does the specification impose severe selection criteria that will reduce yield and thus increase price? Does the specification have an excessive number of tests at extreme temperatures? This, too, will materially increase cost.

(8) The most difficult element in integrated-circuit procurement is the correlation of system reliability requirements with those which can be practically obtained on an individual lot of integrated circuits. Many system reliability engineers attempt to incorporate the system reliability requirements into the integrated-circuit procurement specifications. This is seldom practical. It is usually not economically feasible to test in a given production lot the number of circuits necessary to assure that a system's reliability goal will be met -- often a very difficult fact to accept. One solution is to specify procedures and controls that are known to minimize the failure mechanisms associated with the particular device, along with appropriate testing to remove defective and potentially defective devices from the procurement lot.

(9) The integrated-circuit purchaser must carefully evaluate the performance of the integrated circuits he is designing into his system and then specify the performance characteristics that are essential to his system's performance. If a characteristic is not important, it should not be specified, unless it is indicative of a failure mechanism. Adequate design margins are essential. Although initially a large number of characteristics may have to be specified, the specifications should constantly be reviewed to determine which characteristics tests can be eliminated. The performance and reliability tests specified must be those which are significant.

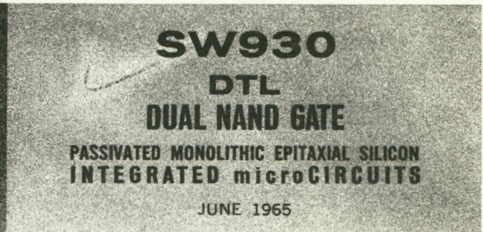
(10) The integrated-circuit manufacturer should be brought into the specifications-preparation picture. He can make suggestions on the most effective specification for obtaining maximum performance and reliability assurance at minimum cost. Experience shows that it is generally very difficult to change specifications once they have been established; therefore, competent manufacturers should be consulted before the specification is prepared. The integrated-circuit manufacturer is just as interested as his customer in having effective specifications. If the specifications are effective, his costs will be reduced and his customer-relations problems will be minimized.

(11) Since the equipment necessary to test integrated circuits is significantly more complex than that used for discrete semiconductor components, the tests to be performed by the customer's incoming inspection must be carefully considered. Most integrated-circuit manufacturers are willing to list the tests they have performed for a specific order and will give the test results if requested. Incoming inspection should utilize the most significant functional tests to assure that no gross performance problems exist. Such problems could result from a lack of specification clarity or improper handling of the circuits during shipment. The simplest test for a digital element is to measure the transfer characteristics; for a linear element, to measure the circuit gain. D-c tests are much more practical to perform than dynamic tests and generally easier to correlate with the integrated-circuit manufacturer. They usually assure that the circuit meets requirements and normally reveal shipment damage. It is generally not necessary for the customer to check high- and low-temperature characteristics, switching-time characteristics, or loading characteristics under more than one condition on a routine incoming inspection basis.

It must be remembered that the problem of integrated-circuit procurement specifications is complex. It can be solved only by a very high degree of cooperation and mutual effort between the integrated-circuit supplier and integrated-circuit user.

EXHIBITS

145

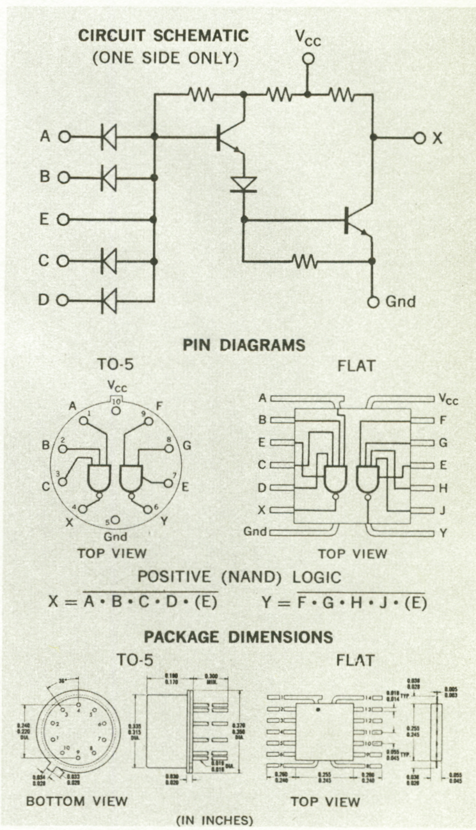


DUAL 4-INPUT NAND GATE WITH AND EXPANSION TERMINALS

HIGH NOISE IMMUNITY—LOW POWER

The SW930 Dual NAND Gate has been designed with a collector-tapped emitter follower to provide high gating efficiency with the attendant low power, high noise immunity of DTL circuitry. This versatile element may be used as a dual gate with expandable inputs, cross-coupled to form an R-S flip-flop, or paralleled at the output to provide a free logical OR function.

- **DC Noise Margin** $\geq$**700 mV**
- **Power Drain 8 mW**
- **Propagation Delay 20 nsec**
- **Fan-out 8**



ABSOLUTE MAXIMUM RATINGS

Supply Voltage (—55°C to +125°C)	+8 Volts
Supply Voltage (pulsed <1 second)	+12 Volts
Output Current (into outputs)	30 mA
Input Forward Current	—10 mA
Input Reverse Current	1 mA
Operating Temperature	—55°C to +125°C
Storage Temperature	—65°C to +150°C

ELECTRICAL CHARACTERISTICS (25°C)

CHARACTERISTIC	SYMBOL	MINIMUM	TYPICAL	MAXIMUM	UNIT
Power Supply	V_{CC}	3.5	5	6	Volts
Propagation Delay	t_{pd}		20	50	nsec
Power Dissipation (per gate @ V_{CC} = 5 V)	P_D		8		mW
Fan-Out (with "0" noise margin of $\geq$0.7 V)	N	7	9		
Output Low Voltage (fan-out = 8)	V_{OL}			0.40	Volts
Output High Voltage	V_{OH}	2.6			Volts
Input Low (threshold) Voltage	V_{IL}	1.1			Volts
Input High (threshold) Voltage	V_{IH}			2	Volts

Exhibit 5-1

DTL DUAL NAND/NOR EXCLUSIVE-OR GATE

SIGNETICS INTEGRATED CIRCUITS

SE115G
SE115K

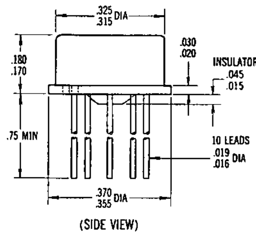
MARCH 1964

PHYSICAL OUTLINES

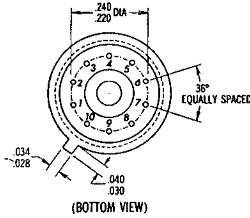
TWO AND A HALF TIMES ACTUAL SIZE

K - PACKAGE

(MODIFIED JEDEC TO-5)



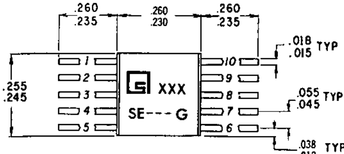
(SIDE VIEW)



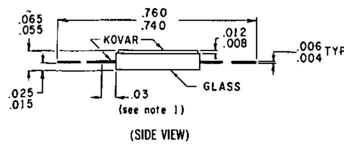
(BOTTOM VIEW)

G - PACKAGE

(MODULAR GLASS-KOVAR)



(TOP VIEW)



(SIDE VIEW)

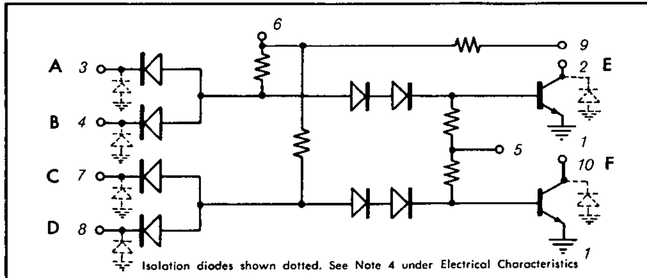
NOTES:
(1) Recommended minimum offset before lead bend.
(2) All leads weldable and solderable.
(3) Pin 1 on K-Package internally connected to case.
(4) All dimensions in inches.

The SE115 is a semiconductor intergrated circuit fabricated within a monolithic silicon substrate by the planar technique. It is intended for use in high speed, low-power computer systems, and is designed to meet or exceed the mechanical and environmental requirements of MIL-S-19500. Some of its outstanding features are:

- **High Noise Immunity**
- **High Speed**
- **High Fan-Out**
- **Full MIL Temperature Range**

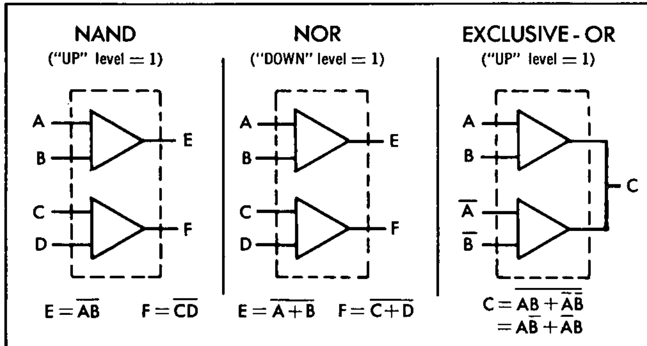
The SE115 is designed to allow maximum flexibility of application in that in addition to the 2-input Dual NAND/NOR Gate configuration, the Exclusive-OR function is provided by tying the outputs (Pins 2 and 10) together. Additional input and output characteristics of the SE115 are compatible with those of other Signetics SE100-series elements and, in general, with conventional DTL Solid-State digital circuits in the same voltage and power range.

SE115 — Schematic



Isolation diodes shown dotted. See Note 4 under Electrical Characteristics

SE115 — Logic Diagrams



$E=\overline{AB}$ $F=\overline{CD}$ | $E=\overline{A+B}$ $F=\overline{C+D}$ | $C=\overline{AB+\bar{A}\bar{B}}$ $=A\bar{B}+\bar{A}B$

DTL DUAL NAND/NOR EXCLUSIVE-OR GATE • SE115G • SE115K — MARCH 1964

SIGNETICS CORPORATION • 680 WEST MAUDE AVENUE, SUNNYVALE, CALIFORNIA • TEL: (408) 739-7700 • TWX: (408) 737-9965

Exhibit 5-2

SE115G
SE115K

DTL DUAL NAND/NOR

S I G N E T I C S   I N T E G

ABSOLUTE MAXIMUM RATINGS
(NOTES 1, 2, 3, 5)

VOLTAGE APPLIED	$V_{2,3,4,6,7,8,9,10}$ V_5	+8V −8V
CURRENT RATING (Note 4)	$I_{2,10}$ $I_{2,3,4,7,8,9,10}$	+30mA −30mA
STORAGE TEMPERATURE		−65°C to +175°C
OPERATING TEMPERATURE		−55°C to +125°C

ELECTRICAL CHARACTERISTICS
(Notes 1, 2—Standard Conditions: $V_6 = +4.0V$, $V_5 = -2.0V$, $V_1 = 0V$, $T = +25°C$ Unless Otherwise Specified)

CHARACTERISTIC	MEASUREMENT	MIN.	TYP.	MAX.	UNIT	CONDITIONS
"0" OUTPUT CURRENT (Note 7)	I_2, I_{10}	10			mA	$V_2, V_{10}=+0.6V$, $V_3, V_7=1.7V$
	I_2, I_{10}	10			mA	$V_2, V_{10}=+0.6V$, $V_3, V_7=1.3V$, $T=+125°C$
	I_2, I_{10}	10			mA	$V_2, V_{10}=+0.6V$, $V_3, V_7=2.0V$, $T=-55°C$
"I" OUTPUT CURRENT (Note 7)	I_2, I_{10}			50	μA	$V_2, V_{10}=+5.0V$, $V_3, V_7=1.1V$
	I_2, I_{10}			50	μA	$V_2, V_{10}=+5.0V$, $V_3, V_7=0.7V$, $T=+125°C$
	I_2, I_{10}			50	μA	$V_2, V_{10}=+5.0V$, $V_3, V_7=1.4V$, $T=-55°C$
OUTPUT BREAKDOWN VOLTAGE	V_2, V_{10}	8			V	$I_2, I_{10}=1\mu A$, $V_3, V_7=0V$
OUTPUT CAPACITANCE	C_2, C_{10}			10	pf	$V_2, V_{10}=+2.0V$, $V_3, V_7=0V$, Note 2, 6
INPUT BREAKDOWN VOLTAGE	V_3, V_4, V_7, V_8	8			V	$I_3, I_4, I_7, I_8=10\mu A$, $V_4, V_3, V_8, V_7=0V$
INPUT LEAKAGE CURRENT	I_3, I_4, I_7, I_8			250	nA	$V_3, V_4, V_7, V_8=+5.0V$, $V_4, V_3, V_8, V_7=0V$
	I_3, I_4, I_7, I_8			25	μA	$V_3, V_4, V_7, V_8=+5.0V$, $V_4, V_3, V_8, V_7=0V$, $T=+125°C$
INPUT TURN-OFF CURRENT	I_3, I_4, I_7, I_8			−1.8	mA	$V_3, V_4, V_7, V_8=0V$
	I_3, I_4, I_7, I_8			−1.9	mA	$V_3, V_4, V_7, V_8=0V$, $T=-55°C$ to $+125°C$
INPUT CAPACITANCE	C_3, C_4, C_7, C_8			10	pf	$V_3, V_4, V_7, V_8=+2.0V$, Note 2, 6
LOAD RESISTOR CURRENT	I_9	−1.6		−2.4	mA	$V_9=0V$
POWER CONSUMPTION						
FROM POWER SUPPLIES						
Output "OFF"				17	mW	$V_3=V_7=0V$
Output "ON"				12	mW	
SWITCHING TIMES						
Turn-On Delay	T_{on}			60	ns	See Figure 9
Turn-Off Delay	T_{off}			50	ns	See Figure 9
AVERAGE PROPAGATION DELAY	T_{pd}		30		ns	See Figure 8
FAN-OUT (To Signetics Standard Unit Load, Note 8)				5		$T=-55°C$ to $+125°C$

Notes:
(1) Voltage and current subscripts refer to pin numbers. Pins not specifically referenced are left electrically open.
(2) All voltage and capacitance measurements are referenced to Pin 1. Positive current flow is defined as into the pin referenced.
(3) Maximum ratings are limiting absolute values above which serviceability may be impaired.
(4) Precautionary measures should be taken to insure current limiting in accordance with maximum rating should the isolation diodes, shown at input and output pins, become forward biased.
(5) Maximum allowable power dissipation = 100Mw.
(6) Capacitance as measured on Boonton Electronic Corporation Model 75A-S8 Capacitance Bridge or equivalent. Frequency of 1Mc, Signal Amplitude 25mV$_{RMS}$. All pins not specifically referenced ,are tied to Pin 1 for capacitance tests.
(7) Positive NAND Logic Definition: "UP" level = 1, "DOWN" level = 0.
(8) Signetics Standard Unit Load is defined as an SE101 Gate input.
(9) Manufacturer reserves right to make design and process improvements.

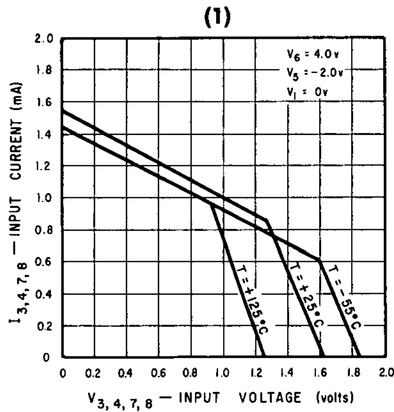
EXCLUSIVE-OR GATE

SE115G
SE115K

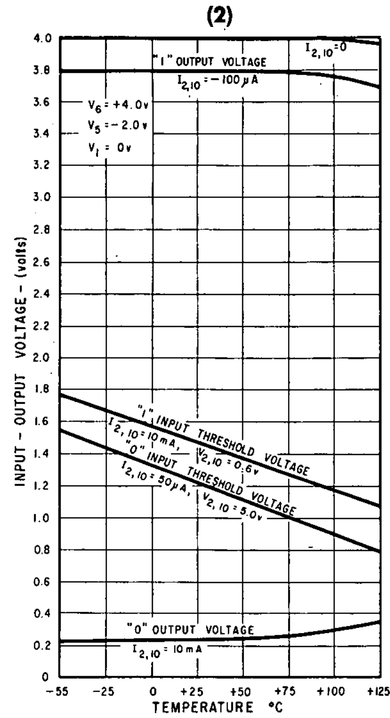
RATED CIRCUITS

TYPICAL CHARACTERISTICS

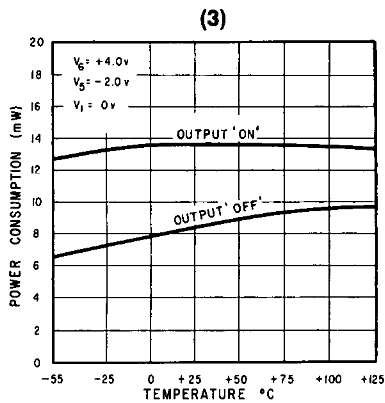
(1)



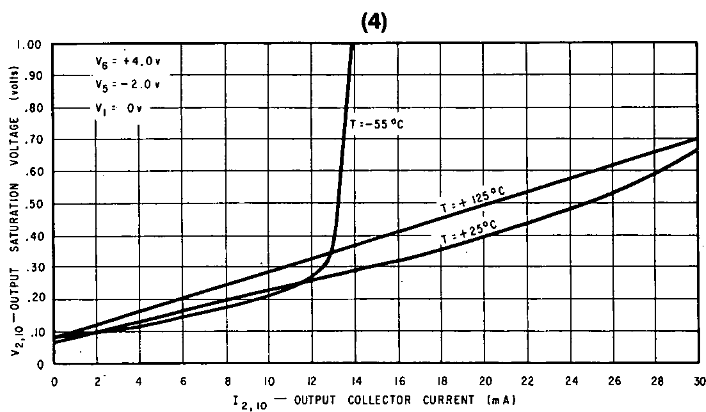
(2)



(3)



(4)



SE115G
SE115K

DTL DUAL NAND/NOR EXCLUSIVE-OR GATE

SIGNETICS INTEGRATED CIRCUITS

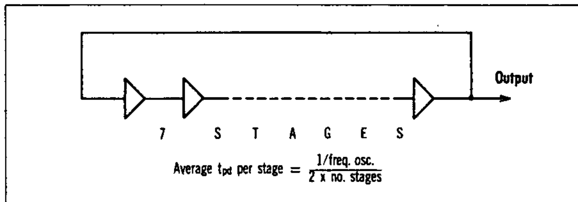
APPLICATION DATA

In any application (e.g. EXCLUSIVE-OR) in which the collectors of two or more SE115 gates are tied in common, the pull-up resistor, Pin 9, should be connected to Pins 2 and 10. Up to five gates may be used in such as configuration, but only one gate in the array need have its pull-up resistor connected. Use of the pull-up in these circumstances assures that at high temperatures, leakage current will not be drawn from the inputs of gates being driven by the SE115.

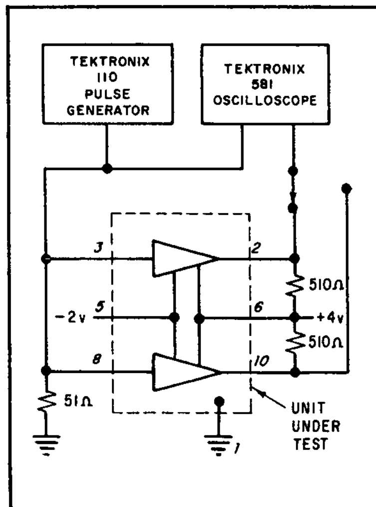
A more general configuration than the EXCLUSIVE-OR shown in the logic diagram on the front page would be one in which A and B are the inputs to one gate and C and D are inputs to the other. The output is then $\overline{AB+CD}$. By appropriate substitutions in this general equation, the EXCLUSIVE-OR function ($\overline{AB+\overline{A}\overline{B}} = A\overline{B}+\overline{A}B$, true for $A \neq B$) or the comparison function ($\overline{A\overline{B}+\overline{A}B} = AB+\overline{A}\overline{B}$, true for $A = B$) can be generated.

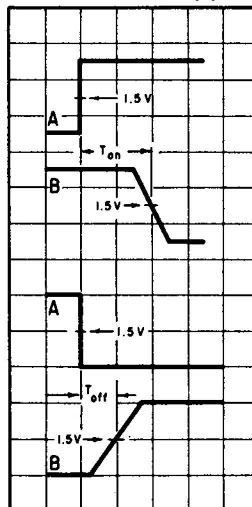
Two or more SE115 gates with the collectors tied in common can also be used in commutation applications. If the signals to be commutated (A,B,C,D. . . .) are connected to one of the two inputs on each gate, and appropriate timing signals (T_1, T_2, T_3, T_4 . . .) are connected to the other input on each gate, the function $\overline{AT_1+BT_2+CT_3+DT_4}$ is generated.

PROPAGATION DELAY MEASUREMENT CIRCUIT (8)



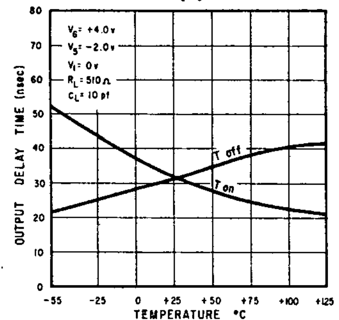
SWITCHING TIME TEST CIRCUIT AND WAVEFORMS (9)





OUTPUT DELAY CHARACTERISTICS

(5)



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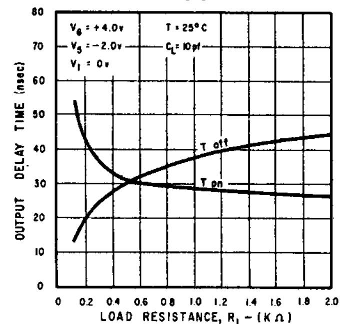

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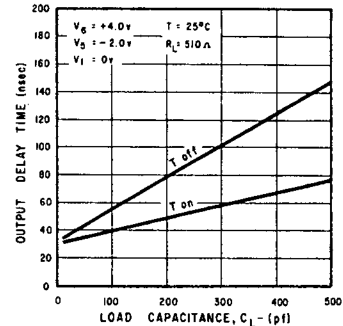
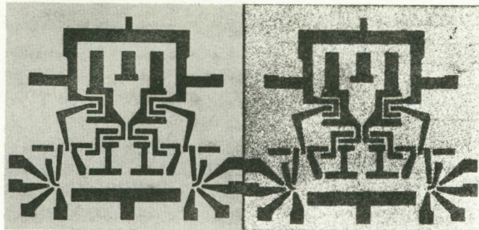


Copyright 1964

SF52 / SF53

J-K FLIP-FLOP



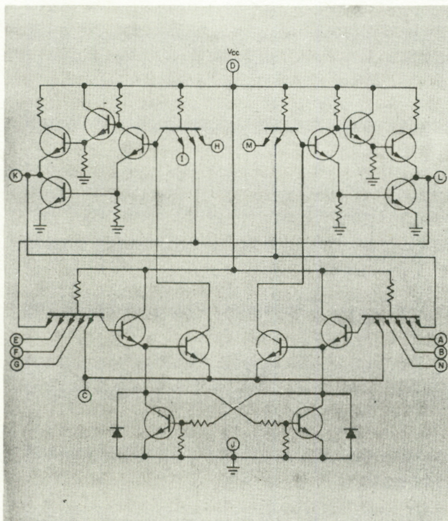
SYLVANIA

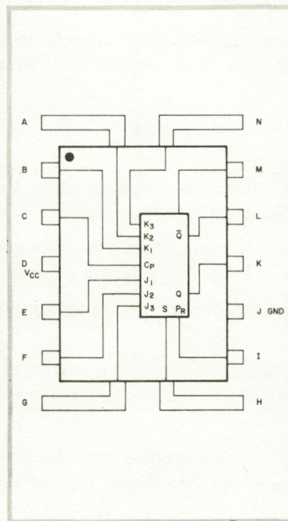
INTEGRATED CIRCUITS

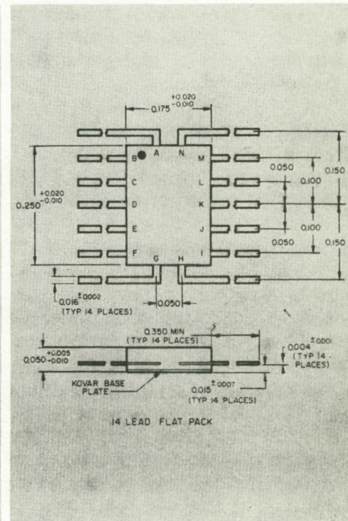
SUHL*

J-K FLIP-FLOP

monolithic silicon epitaxial circuit for temperature range 0°C to +75°C







CIRCUIT DESCRIPTION

The **SF-52** and **SF-53** are J-K flip-flop members of the SUHL* family, which is a monolithic epitaxial, saturated high speed type of logic. The circuit is designed with the system requirements in mind permitting high speed systems with a saving on gates and interconnections. The SF-52 and SF-53 operate up to 20 megacycles over the temperature range of 0°C to +75°C for military ground support and industrial systems while maintaining SUHL* characteristics of fan-out, logic swing, noise immunity and capacitance drive at low power. The SUHL* J-K flip-flop operates from a single 5.0V power supply.

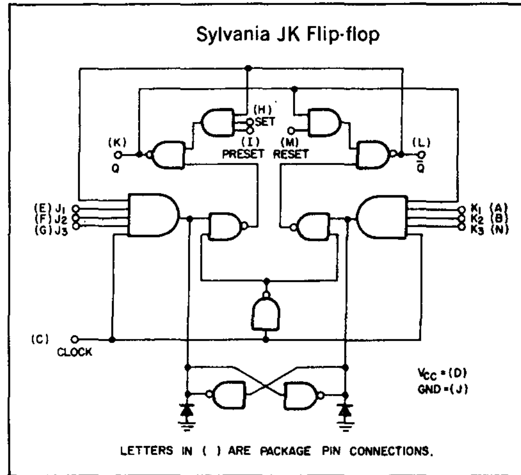
Information is fed into the J and/or K terminals while the clock is low. This new information is ANDed with the present state of the flip-flop (the state of the flip-flop is fed back to the input terminals via the connection from the Q and Q̄ terminals to the K and J terminals respectively) and stored in the depletion region of a diode when the clock goes high. When the clock returns low the stored information is ANDed with the inverted clock, causing the cross coupled NAND gates to be set accordingly.

*Sylvania Universal High level Logic

Exhibit 5-3

CHARACTERISTIC SUMMARY

1) Logic at the inputs — In addition to the basic J-K flip-flop function of determinate output states for every input condition, the Sylvania **SF-52** and **SF-53** have three J and three K data inputs which can be used to provide the AND function right in the flip-flop. This provides greater system speed equivalent to the speed of the flip-flop and reduces the number of external NAND gates necessary to perform system operations.**



J	K	Qn.	Qn + 1
0	0	0	0
0	0	1	1
0	1	0	0
0	1	1	0
1	0	0	1
1	0	1	1
1	1	0	1
1	1	1	0

WHERE $J = J_1 \cdot J_2 \cdot J_3$
$K = K_1 \cdot K_2 \cdot K_3$

TRUTH TABLES

$K = Qn + 1 = J\bar{Q}n + \bar{K}Qn$

$L = \bar{Q}n + 1 = \bar{J}\bar{Q}n + KQn$

LOGIC EQUATIONS

2) Internal Complementing — The circuits are internally complemented which means all J and K terminals are usable as data inputs in all systems. This provides maximum speed and maximum fan-out from the flip-flop itself and simplifies systems wiring.

3) Operation at low frequencies and clock edges as long as 200 nanosecs is made possible by use of charge control devices.

4) Operation at frequencies greater than 20 mc is made possible by using charge control devices (instead of a master slave operation) coupled with a discharge network which removes any excess stored charge at high frequency.

5) Negative edge triggering — Triggering is done when the clock goes negative. This permits the rest of the system to be inhibited (positive logic) at the time the flip-flop is going through its translation.

6) Raceless — The inhibiting action of the clock input also directly inhibits the J and K terminals thus preventing any race problem internal to the flip-flop.

7) Raceless in a system where one flip-flop drives another in that the J and the K information must be present 20 nanoseconds before the negative going edge of the clock to register and the delay through a flip-flop is greater than 8 nanosecond.

8) Triggers on clock pulses as narrow as 20 nanosecs;‡ the charge storage (memory of data on J and K terminals) is accomplished rapidly through low impedances. No master flip-flop has to be set.

9) Noise immune clock — Triggers on the voltage level of the clock and can therefore tolerate high noise or ringing on the clock when it is in the "1" or the "0" position the same as a SUHL gate. Because of this characteristic the clock input is also tolerant to overshoot in either direction.

10) Provides asynchronous (direct) SET, PRESET and RESET terminals each of which represents a gate load of 1 and is independent of the clock. The application of a "0" to any one of these will cause the corresponding side to go to "1"

11) All J and K terminals represent a gate loading of one. The clock terminal represents a gate loading of 1.5.

12) High fan-out: 12 min. for **SF-52;** 6 min. for **SF-53.**

13) High speed: 20 mc clock. Propagation delay times typically
13 nsec t_{off}, 25 nsec t_{on}

14) High noise immunity ±900 mv at 25°C and worse case fan-out
±600 mv from 0°C to +75°C and worse case fan-out.

15) High capacitance drive up to 600 pf.

16) High logic swing: Logic 0 is typically 0.26 volts, Logic 1 is typically 3.3 volts at 25°C.

17) Low power: typically 50 milliwatts.

18) Low output impedance in the "0" and "1" level reduces noise pick-up.

‡Unused emitters tied to greater than 3.0V
**See applications on back page.

Exhibit 5-3

RATINGS

VOLTAGE	Min.	Typical	Max.
Supply voltage (D.C.)			7.0 V_{DC}
Supply voltage (surge, 1 sec)			12.0 V
Supply voltage (operating)	4.5	5.0	6.0 V
Input voltage			5.5 V
Output voltage			5.5 V

TEMPERATURE and POWER	Min.	Typical	Max.
Operating	0		+75°C
Storage	−65		+200°C
Thermal gradient, junction to air (θja)			0.3°C/MW
Thermal gradient, junction to case (θjc)			0.1°C/MW
Power Dissipation per gate (50% Duty Cycle, V_{CC} = +5v)		50	MW

ELECTRICAL CHARACTERISTICS

Characteristics at V_{CC} = +5.0V	Symbol	Values at Required Temperatures 0 C	25 C	75 C	Units	Fig. No.
INPUT:						
Input Load Current (For set, preset, reset) @ V_{IN} = Other inputs: Q High when checking Reset Q Low when checking Set, Preset	I_L	1.66 0 +4.5	1.66 0 +4.5	1.66 0 +4.5	mA Max. Volts Volts	1
Input Load Current (For $J_1, J_2, J_3, K_1, K_2, K_3$) @ V_{IN} = Others Q Low when checking J_1, J_2, J_3 Q High when checking K_1, K_2, K_3	I_L	1.66 0 +4.5	1.66 0 +4.5	1.66 0 +4.5	mA Max. Volts Volts	1
Input Load Current (for Clock) @ V_{IN} = Others	I_L	3.0 0 +4.5	3.0 0 +4.5	3.0 0 +4.5	mA Max. Volts Volts	1
Input Leakage Current (All except Clock) @ V_{IN} = Other Inputs	$I_{IN\ LK}$	0.1 +4.5 0	0.1 +4.5 0	0.1 +4.5 0	mA Max. Volts Volts	2
Input Leakage Current (for Clock) @ V_{IN} = Other Inputs	$I_{IN\ LK}$	0.15 +4.5 0	0.15 +4.5 0	0.15 +4.5 0	mA Max. Volts Volts	2
Inverse Beta Current (All except Clock) @ V_{IN} = Other Inputs Q Low when checking Set, Preset, J_1, J_2, J_3 Q High when checking Reset, K_1, K_2, K_3	B_{INV}	0.1 +4.5 Open	0.1 +4.5 Open	0.1 +4.5 Open	mA Max Volts	3
Inverse Beta Current (Clock) @ V_{IN} Other Inputs: Q Low when checking Clock input at J Q High checking Clock K	B_{INV}	0.15 +4.5 Open	0.15 +4.5 Open	0.15 +4.5 Open	mA Max. Volts	2
Input (OFF Level) Breakdown Voltage @ I_{IN} = (for $J_1J_2J_3$, $K_1K_2K_3$) Other Inputs	BV_{IN}"1"	+5.5 1.0 0	+5.5 1.0 0	+5.5 1.0 0	Volts Min. mA Volts	2
Input (Off Level for set, preset) @ I_{IN} = Reset Input Other Inputs	BV_{IN}"1"	+5.5 1.0 +5.5 0	+5.5 1.0 +5.5 0	+5.5 1.0 +5.5 0	Volts Min. mA Volts Volts	2
Input (Off Level for Reset) (Momentarily GRD Q) @ I_{IN} = Set, Preset input Other Inputs	BV_{IN}"1"	+5.5 1.0 5.5 0	+5.5 1.0 5.5 0	+5.5 1.0 5.5 0	Volts Min. mA Volts Volts	2
Input (Off level for clock) @ I_{IN} = Other Inputs	BV_{IN} "1"	+5.5 2.0 0	+5.5 2.0 0	+5.5 2.0 0	Volts Min. mA Volts	2
Input (ON Level) Breakdown Voltage (All except Clock) @ I_{IN} = Other Inputs Q Low when checking Set, Preset, J_1, J_2, J_3 Q High when checking Reset, K_1, K_2, K_3	BV_{IN}"0"	+5.5 1.0 Open	+5.5 1.0 Open	+5.5 1.0 Open	Volts Min. mA	3
Input (ON Level) Breakdown Voltage (for Clock) @ I_{IN} = Other Inputs Q Low when checking clock input at "J" Q High when checking clock input at "K"	BV_{IN}"0"	+5.5 2.0 Open	+5.5 2.0 Open	+5.5 2.0 Open		3
Logic "1" Threshold Voltage (for Preset, Set, Reset) @ V_{OUT} = I_{OUT} (SF-52) I_{OUT} (SF-53)	V_{TH}"1"	1.9 0.45 20 10	1.8 0.45 20 10	1.7 0.45 20 10	Volts Min. Volts mA mA	8
Logic "0" Threshold Voltage (for Preset, Set, Reset) @ V_{OUT} = I_{OUT} (SF-52) I_{OUT} (SF-53)	V_{TH}"0"	1.1 2.5 1.2 −0.6	1.2 2.4 1.2 −0.6	1.1 2.5 1.2 −0.6	Volts Max. Volts mA mA	9
OUTPUT:						
Output Leakage Current @ V_{OUT} = Inputs	$I_{O\ LK}$	0.25 +5.5 0	0.25 +5.5 0	0.25 +5.5 0	mA Max. Volts Volts	5
Output Short Circuit Current Input @	I_{SC}	 0	20 60 0	 0	mA Min. mA Max. Volts	7
Logic "0" Level @ V_{IN} = I_{OUT} (SF-52) I_{OUT} (SF-53)	Logic "0"	0.40 2.8 20 10	0.40 2.8 20 10	0.45 2.8 20 10	Volts Max. Volts mA mA	8
Logic "1" Level @ V_{IN} = I_{OUT} (SF-52) I_{OUT} (SF-53)	Logic "1"	3.0 0.45 −1.2 0.6	3.1 0.45 −1.2 0.6	3.15 0.45 −1.2 0.6	Volts Min. Volts mA mA	9
POWER REQUIREMENTS:						
Breakdown Voltage @ I_{CC} = Inputs	BV		+7.0 14.0 0		Volts Min. mA Volts	4
"ON" State Current Drain Inputs	I_{CC}"0"	12 Open	12 Open	12 Open	mA Max.	6
"OFF" State Current Drain Inputs	I_{CC}"1"	9 0	9 0	9 0	mA Max. Volts	4

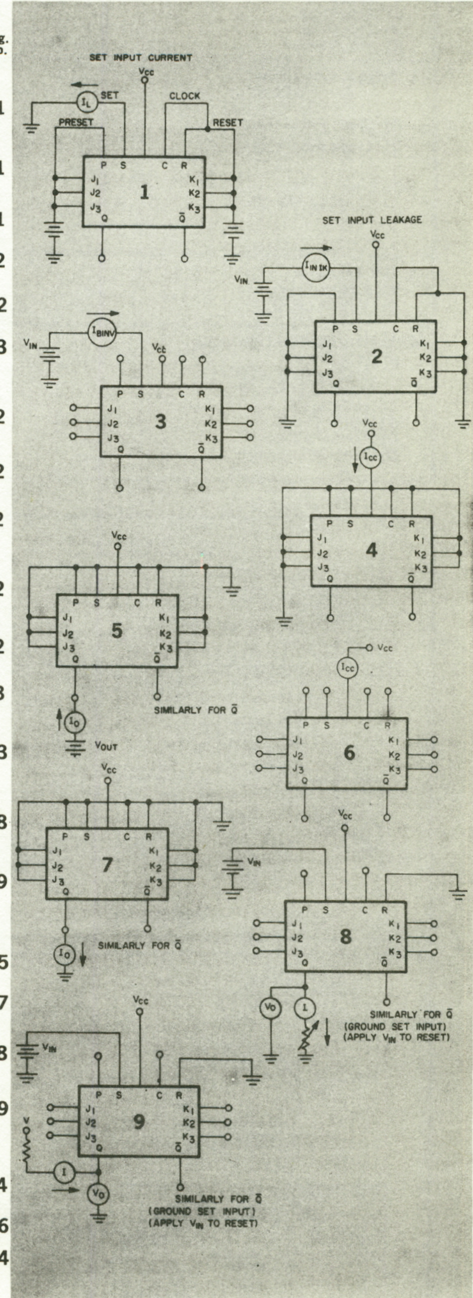


Exhibit 5-3

J-K SWITCHING CHARACTERISTICS

FOR ALL OPERATING CONDITIONS $T_A = +25°C$, $V_{CC} = 5.0V$, Load = F.O. = 1, $C_L = 15$ PF

TEST	SYMBOL	CONDITIONS: CLOCK	CONDITIONS	MIN.	MAX.	UNIT.	FIG.
1. Output Switching Charact. (Toggle Cond.)							10
A) Turn-Off Delay	t_{OFF}	$V_{CA} = 3.5$ V, $t_{CR} = t_{CF} \leqq 10$ nsec, $t_{CW} = 100$ nsec, Freq = 5 M.C.			20	nsec	
B) Turn-On Delay	t_{ON}				40	nsec	
C) Rise Time	t_R				5.0	nsec	
D) Fall Time	t_F				8.0	nsec	
E) Amplitude	V_A			3.2		Volts	
2. Trigger Conditions (Toggle Cond.)							10
A) Clock Pulse Width	t_{CW}	Same as in 1. Except for t_{CW}		20		nsec	
B) Clock Amplitude	V_{CA}	Same as in 1. Except V_{CA}		1.8		Volts	
C) Clock Slope (Neg. Going)	t_{CR}	$V_{CA} = 3.5$ V, $t_{CF} \leqq 50$ nsec, $t_{CW} = 100$ nsec, Freq = 1 M.C.			200	nsec	
3. J-K Terminal							11
A) Enable Level	V_{EN}	Same as in 1.			1.8	Volts	
B) Inhibit Level	V_{INH}			1.2		Volts	
4. Set-Preset-Reset Terminal							12
A) Post Time Setting time after clock has changed state of FF	t_P	Same as in 1.	Set-Preset-Reset (2 ϕ Clock) $t_R = t_F = 10$ nsec, $V_{CA} = 3.5$ V, Freq = 5 M.C.		100	nsec	
B) Pulse Width	t_{CW}			40		nsec	
C) Turn-ON Delay	t_{DON}				20	nsec	
D) Turn-OFF Delay	t_{DOFF}				40	nsec	

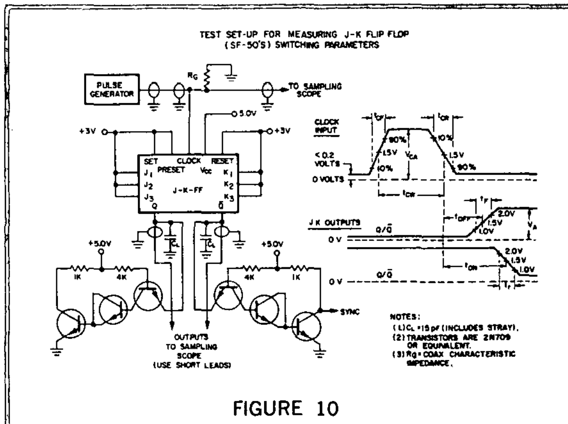


FIGURE 10

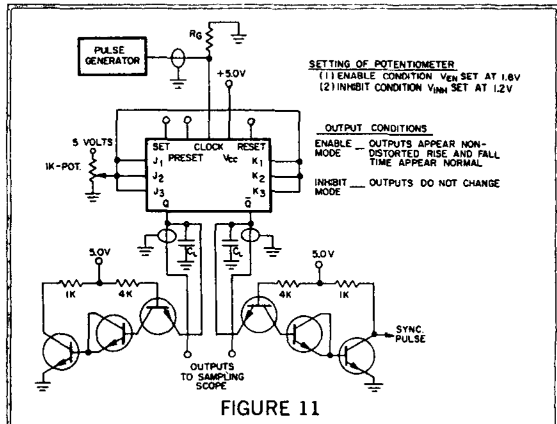


FIGURE 11

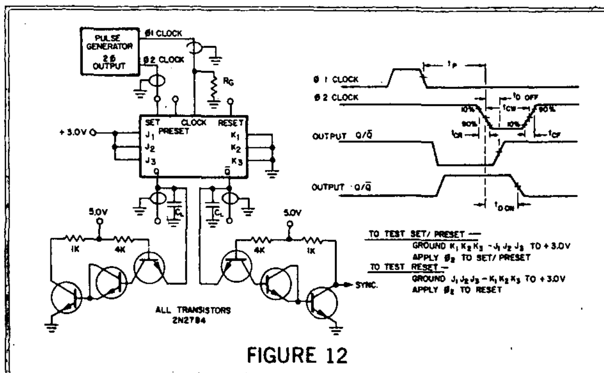
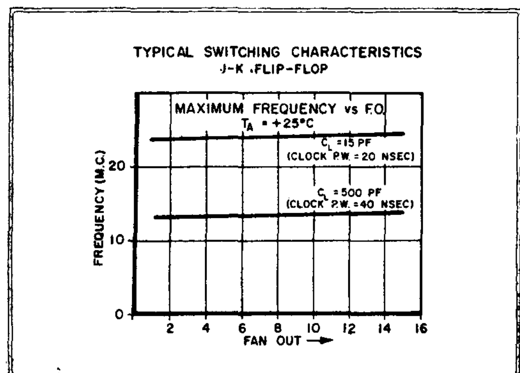


FIGURE 12



TYPICAL SWITCHING CHARACTERISTICS

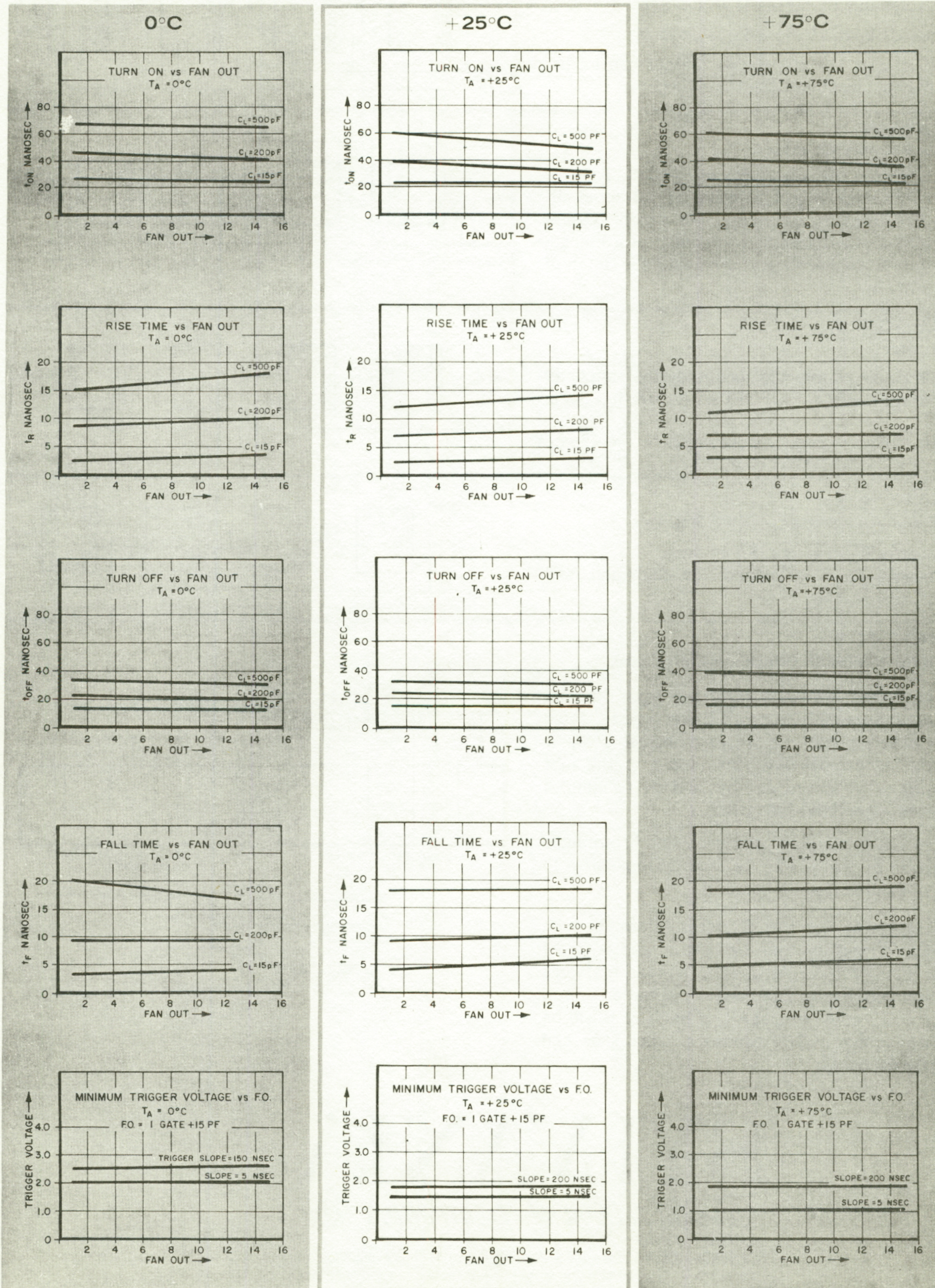


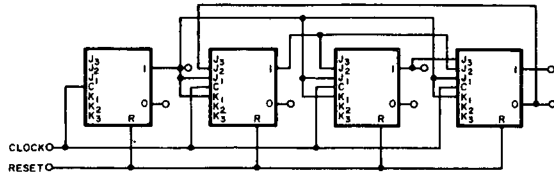
Exhibit 5-3

APPLICATION 1.
Synchronous Binary Decade Counter

Uses only 4 Sylvania SF 50 series JK flip flops.

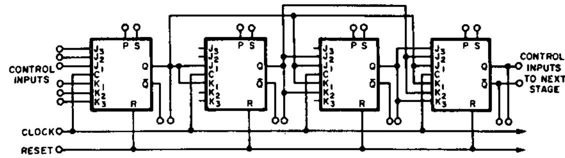
Clock frequency up to 20 mc. Counts up to 20 mc.

All outputs appear simultaneously. Output can be decoded on the next positive clock transition.



APPLICATION 2.
Synchronous Binary Counter

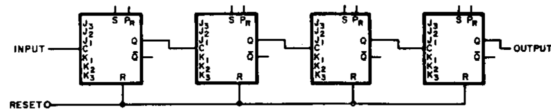
This demonstrates the advantage of multiple J and K terminals. This uses only 4 Sylvania SF 50 series JK flip flops. Because gating is done internally this circuit has no external gate delays and can count at 20 megacycles, using 4 packages and dissipating a total of less than 200 mw.



APPLICATION 3.
Ripple Counter

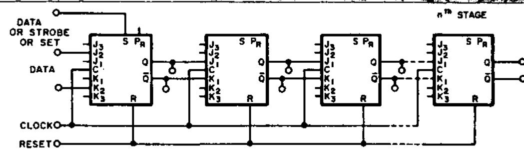
This simple ripple counter demonstrates the simplicity of systems with Sylvania SF 50 series JK flip-flops.

Counting speed $- \frac{1}{n \text{ stages}} \times 30\text{ns/stage} = \frac{1 \times 10^9}{n \times 30}$ cps



APPLICATION 4.
Serial to Parallel Converter — Shift Register

Uses 4 Sylvania SF 50 series JK Flip-flops.
Clock frequency up to 20 megacycles. Shift and read out up to 20 megacycles.

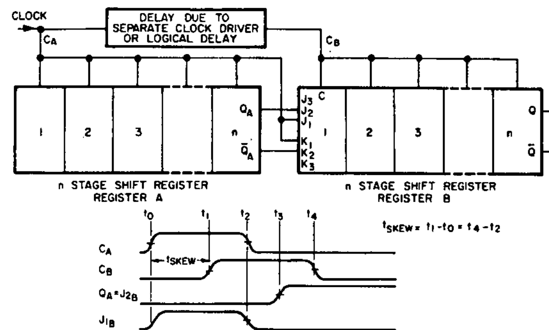


APPLICATION 5.
Technique for eliminating clock skew problems

In cases where **two** registers, are driven from different clock sources because one clock driver source could not drive both registers or where a logical delay is introduced in one clock line, the output of the first register may arrive ahead of time and be recognized by the second register erroneously.

This can be solved by use of multiple J and K terminals of Sylvania SF 50 series F.F. Tie clock of Register A to J_1 and K_1 of input stage of Register B.

The input stage of Register B stores information on J_{2B} (and K_{2B}) during the time between t_1 and t_2 (must be greater than 20 nsec). At t_2, when J_{1B} (and K_{1B}) goes negative it inhibits any additional information input. Any "1" or "0" stored in stage 1 of Register B will be held for a minimum of 100 nanosecs. Clock skew can be up to 100 nanosecs.



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SEMICONDUCTOR DIVISION • 100 SYLVAN ROAD • WOBURN, MASSACHUSETTS
TRANSISTORS • DIODES • MICROWAVE DIODES • RECTIFIERS

3/1/65
Exhibit 5-3

MOTOROLA Semiconductors

BOX 955 • PHOENIX, ARIZONA

MC1519

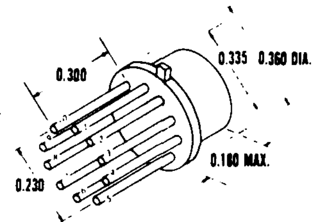
. . . featuring **NPN** inputs and **PNP** outputs. Two monolithic compatible* chips are used to provide a versatile and extremely stable amplifier.

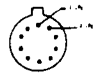
*Compatible — a Motorola process utilizing thin film resistors deposited on a silicon monolithic integrated circuit.

MONOLITHIC
SILICON EPITAXIAL PASSIVATED

AUGUST 1964 — DS 9036

Characteristic	Symbol	Rating	Unit
Power Supply Voltage	V_{CC}	+14	Vdc
Power Supply Voltage	V_{CC}	-14	Vdc
Differential Input Signal	V_{in}	±5	Vdc
Total Power Dissipation Derate above 25°C	P_D	500 3.3	mW mW/°C
PNP Output Transistor Power Dissipation (each) Derate above 25°C	P_D	100 0.4	mW mW/°C
Operating Temperature Range	T_J	-55 to +125	°C
Storage Temperature Range	T_{stg}	-65 to +175	°C





ALL PINS ELECTRICALLY ISOLATED FROM PACKAGE

LINEAR INTEGRATED CIRCUITS
MC1519
DS 9036

CIRCUIT SCHEMATIC

FIGURE 1

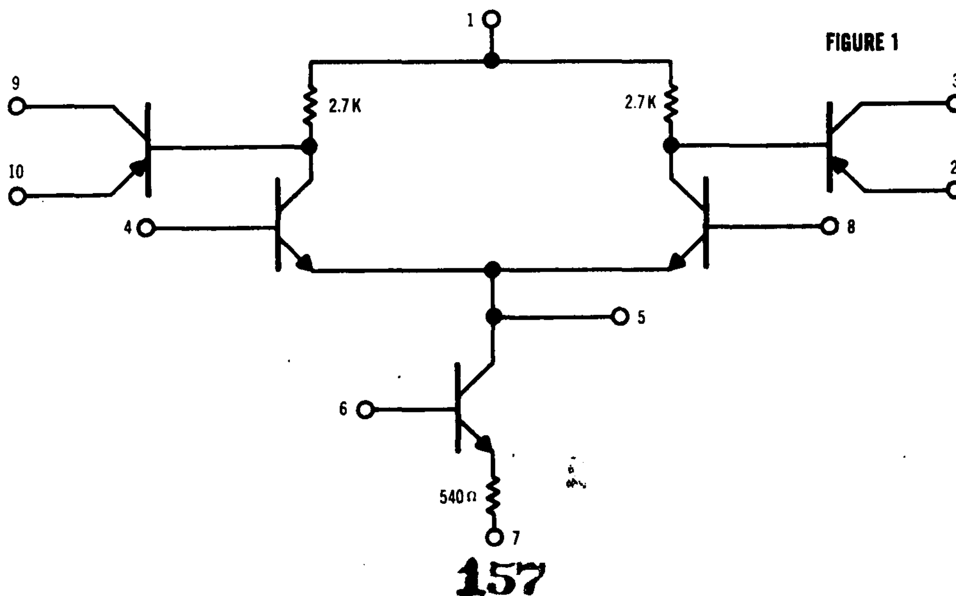


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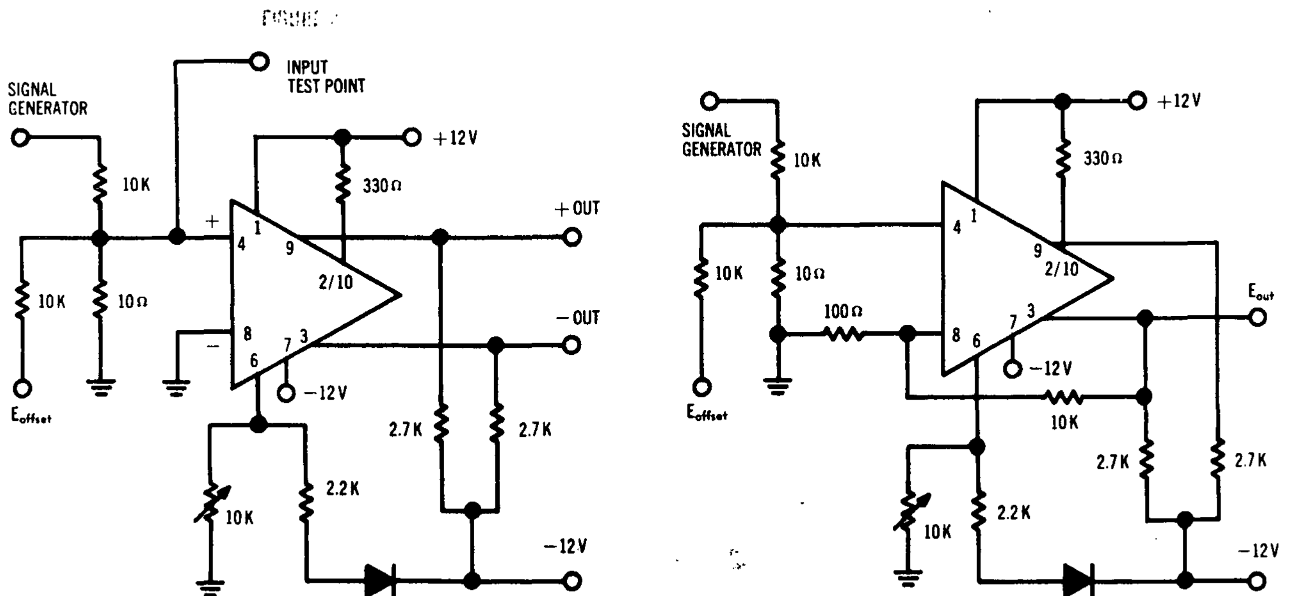
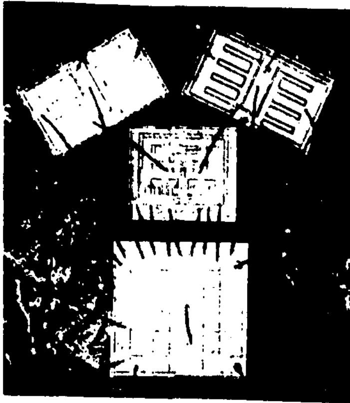
EXHIBIT 5-4

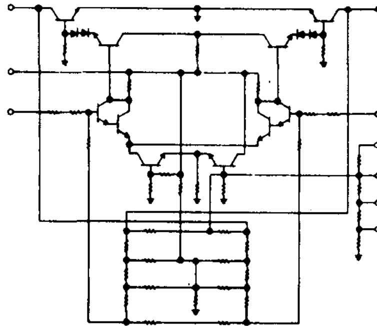
Characteristic	Symbol	Min	Typ	Max	Unit
Refer to Figure 2					
Differential Voltage Gain (V_{in} 10 mV, f 10 kc)	A_{dd}	60	66	70	db
AC Gain Match (V_{in} 10 mV, f = 10 kc)	—	—	5	—	%
Common-Mode Voltage Gain (V_{in} 1 V, f 100 kc)	A_{cc}	—	-14	—	db
Common Mode Discrimination Factor (F A_{dd}/A_{cc}, V_{in} = 1 V, f = 100 kc)	F	—	74	—	db
Maximum Output Swing	V_o	—	12	—	$V_{(p-p)}$
Input Drift Voltage (Constant Current Source = 3 mA, T_A = -55 to +125°C)	V_{id}	—	5	15	$\mu V/^oC$
Input Offset Voltage	V_{io}	—	3	10	mVdc
Input Offset Current	I_{io}	—	1.0	—	μAdc
Bandwidth	BW	—	1.0	—	mc
Differential Input Resistance	R_{in}	—	5	—	kΩ
PULSE AMPLIFIER OPERATION - Figure 3					
(V_{in} = 10 mV, T_D = 1 μsec, t_r = t_f = 10 nsec)					
Output Pulse Amplitude	V_o	—	1.0	—	Volts
Output Pulse Width	T_D	—	995	—	nsec
Delay Time	t_d	—	25	—	nsec
Rise Time	t_r	—	60	—	nsec
Storage Time	t_s	—	30	—	nsec
Fall Time	t_f	—	35	—	nsec
AC Gain	A_V	—	40	—	db
Input Impedance	Z_{in}	—	50	—	kΩ
Output Impedance	Z_{out}	—	200	—	Ω
Bandwidth (-3 db)	BW	—	10	—	mc
PNP OUTPUT TRANSISTOR					
Collector-Emitter Breakdown Voltage (I_C = 10 mAdc, I_B = 0)	BV_{CEO}	20	—	—	Vdc
Collector-Emitter Leakage Current (V_{CE} = 12 Vdc, I_B = 0)	I_{CEO}	—	—	1	μAdc
DC Forward Current Transfer Ratio (V_{CE} = 2 Vdc, I_C = 10 mAdc)	h_{FE}	15	30	—	—

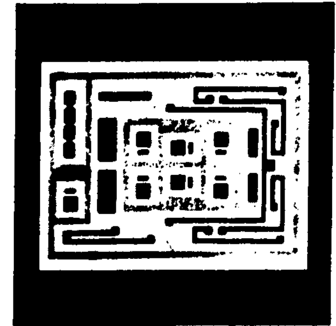


INTEGRAL CIRCUITRY

NM-1003, NM-1008







8-WATT SERVO AMPLIFIER

DATA SHEET IC104A/MAY '65
TENTATIVE SPECIFICATIONS

The NM-1003 is an integrated 8-watt, Class A, linear differential servo amplifier hermetically sealed in a modified TO-53 case. It is designed to operate with +28 volt power supply and a differential input signal from DC to 10 KC. The output is linear with no appreciable phase shift below a maximum output voltage of 36V rms. The amplifier is designed to power a center-tapped control winding of a servo motor with +28 volts on the center tap. The NM-1008 is identical to the NM-1003 except for voltage gain and output impedance ratings. Several choices of impedance ratios are offered on external leads to accommodate the characteristics of the motors with which the amplifiers are to be used. These servo amplifiers were developed by Norden for the Navy Bureau of Weapons, Engineering Division.

ABSOLUTE MAXIMUM RATINGS

Total Supply Voltage = V_{bb}	36 volts	Load Impedance Ratio, AC:DC Min	3:1
Minimum Operating Voltage	25 volts	Input Voltage	60 volts
Power Supply Current	1 amp.	Operating Temperature = T_c	+150°C
*Power Supply Power Input	17 watts	Storage Temperature = T_c	+300°C
*Power Output	8 watts	Power Transistor Saturation Resistance — R_s	10 ohms
Load Impedance Ratio, AC:DC Max	20:1		

*Power Derating Curve (@Tc = 100°C)

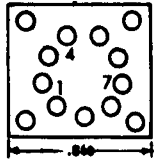
TYPICAL CHARACTERISTICS

V_{bb}	30 volts	Input Impedance @ T_A = 25°C	10K ± 25%
Load-Tuned center tapped Motor:		Phase Shift @ T_A = 25°C	0° ± 15°
R_d	125 ohms	Output, pin 3 to pin 2, agrees with input, pin 7 to pin 8.	
R_a	660 ohms		
Gain @ T_A = 25°C:		Output Impedance @ T_A = 25°C	
NM 1003	500 ± 15%	NM 1003	500 ohms
NM 1008	200 ± 10%	NM 1008	300 ohms
Gain Stability —54°C to +100°C:		Max. Output Voltage	40 volts rms
NM 1003	±15%		
NM 1008	±7%	Power Input @ Tc = 100°C	6 watts

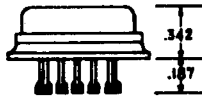
Norden

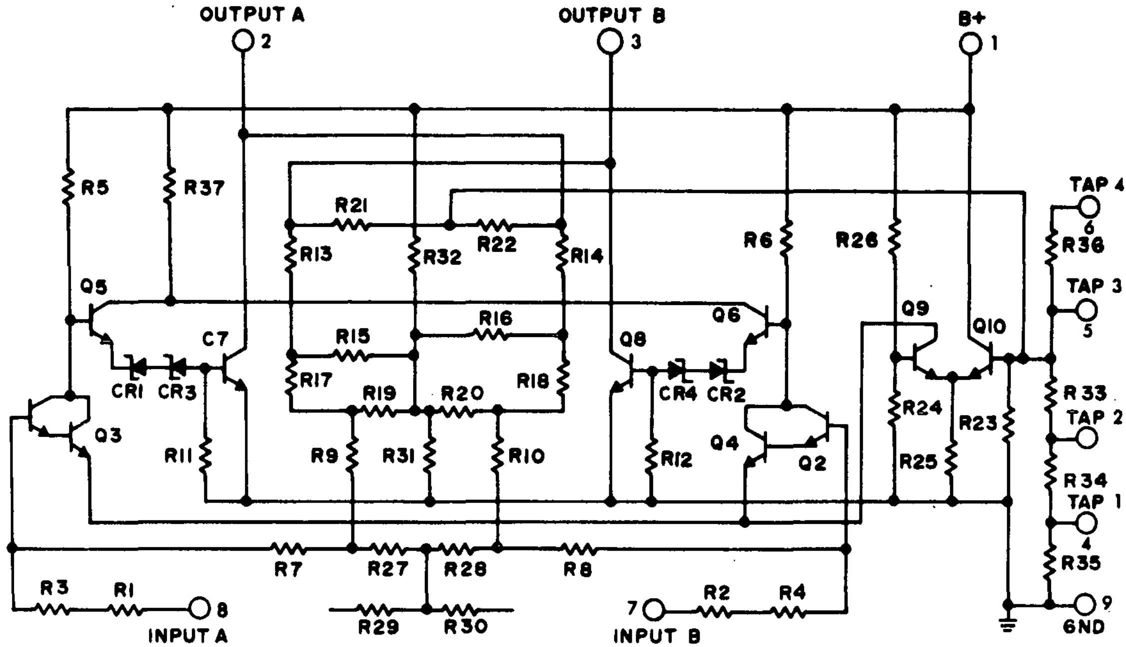
U A

Exhibit 5-5



BOTTOM VIEW
TO-53
CASE





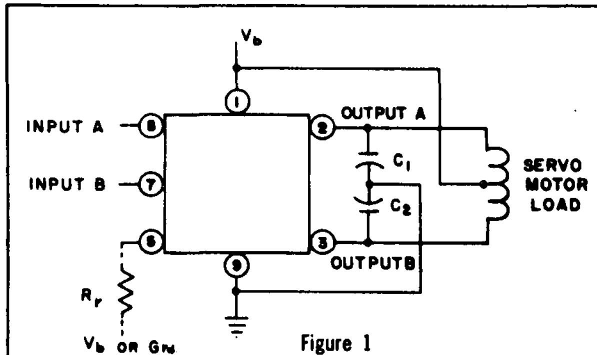


Figure 1

TYPICAL CIRCUIT APPLICATION
SERVO MOTOR LOAD

C_1, C_2 are used to tune the load at the operating frequency.
R_r can be used to shift the operating point dependent on the load.

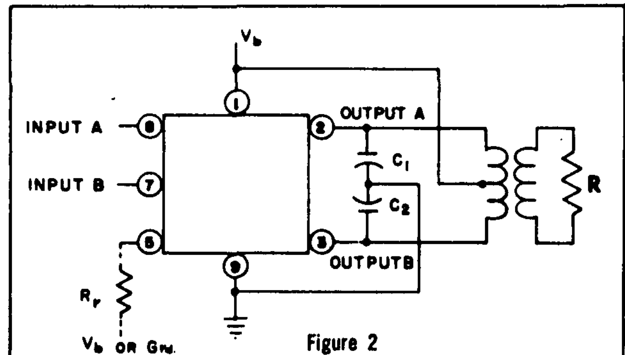


Figure 2

TYPICAL CIRCUIT APPLICATION
TRANSFORMER COUPLED LOAD

C_1, C_2 are used to tune the load at the operating frequency.
R_r can be used to shift the operating point dependent on the load.
R is the load resistance.

Exhibit 5-5

APPLICATION NOTES FOR THE 8-WATT SERVO AMPLIFIER

Figure 1 shows a typical application of the amplifier being used to drive a center tapped tuned servo motor. It can also be used to drive a center tapped tuned transformer load as shown on Figure 2.

Load Impedance

The load DC resistance and AC impedance determine the quiescent current and over-all linearity of the amplifier input-output voltage characteristic. The maximum DC load current is 1 ampere.

Load Impedance Ratio

The amplifier has been designed to operate with an AC to DC impedance ratio of either 5.1:1 or 9.8:1. In addition, provision has been made to accommodate ratios other than those given. If the 5.1:1 ratio is desired, pin 4 must be grounded. To change the ratio —5%, disconnect pin 4 from ground.

For the 9.8:1 ratio, ground both pins 4 and 6. To decrease this 5%, disconnect pin 4 from ground.

For ratios different than the design values, an external resistor R_r must be connected between pin 5 and either V_b or Ground. The approximate value of the resistance and its connection is determined in the following manner: first, the value of the output transistor collector voltage V_q is determined from the equation:

$$V_q = V_b \left[\frac{R_{bd} (R_{ba} + 2R_s)}{R_{ad} (R_{bd} + R_{ba} + 2R_s)} \right]$$

where: V_b = Power Supply Voltage

R_{bd} = Parallel resistance of ½ DC load resistance and 2300 ohms

$$= \frac{1}{\frac{2}{R_d} + \frac{1}{2.3K}}$$

R_{ba} = Parallel resistance of ½ AC load resistance and 2300 ohms

$$= \frac{1}{\frac{2}{R_a} + \frac{1}{2.3K}}$$

R_{ad} = Parallel resistance of ½ DC load resistance, and 9000 ohms

$$= \frac{1}{\frac{2}{R_d} + \frac{1}{9K}}$$

R_s = Power Transistor Collector Saturation Resistance

Second, if $V_q \leq .82\ V_b$, return resistor R_r to the power supply voltage. If $V_q > .82\ V_b$ then R_r should be connected to ground.

In the first instance given, the approximate value of R_r is determined from the following:

$$R_r \doteq \frac{15}{5.7 - 7\frac{V_q}{V_b}} \text{ K ohms}$$

and in the second case, use the equation;

$$R_r \doteq \frac{2.5}{7\frac{V_q}{V_b} - 5.7} \text{ K ohms}$$

The actual value of R_r should be adjusted so that the voltage V_q, determined above, is obtained. V_q is the average of the DC voltages measured between each output terminal and ground. In the first case, R_r should be increased to increase the voltage V_q and in the second case, R_r should be increased to decrease V_q.

Gain

The gain of these amplifiers is factory adjusted by internal resistor taps to give values between 200 and 1000 at specific loads and power supply voltages. Standard values are 200 or 500. The gain of any unit can be reduced externally by inserting resistors in series with the input signal leads. Gain will be increased for higher supply voltages and larger load impedances.

Maximum Output Voltage

The maximum sine wave output voltage that can be obtained for any given load with the operating point correctly established can be determined from the following equation:

$$E_{o(max)} = \sqrt{2}\, V_q \left[\frac{1}{1 + \frac{2R_s}{R_{ba}}} \right]$$

Power

Output power between 1 and 8 watts is possible with proper matching of amplifiers and load and with proper heat sink.

Power Output Derating Curve

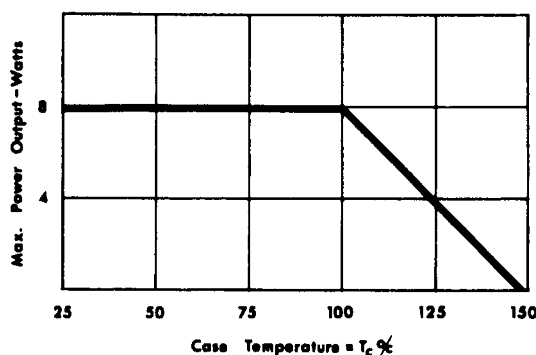


Figure 3

Devices should be derated for higher temperature operation by the curve of Figure 3.

SOLID CIRCUIT® TYPES SN717A, SN350A, SN351A, SN352A
DIFFUSED SILICON GENERAL PURPOSE AMPLIFIER NETWORKS

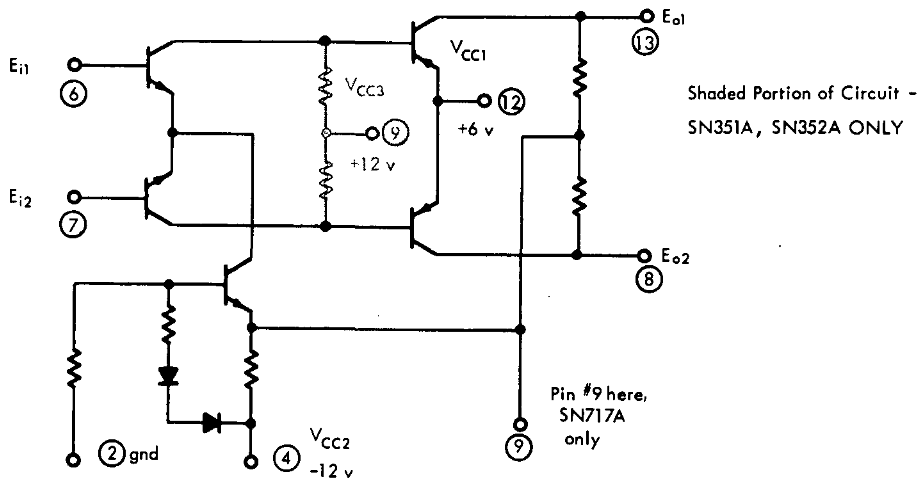
MINUTEMAN TYPE SEMICONDUCTOR NETWORK AMPLIFIERS FOR APPLICATION IN

Military & Industrial Control Systems • Analog-to-Digital Converters
Analog Computers

general operating characteristics

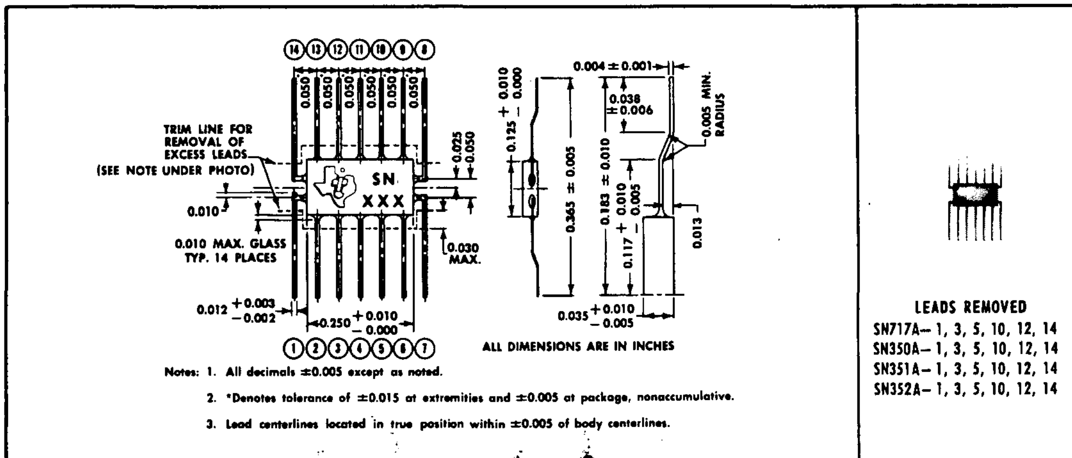
	SN717A	SN350A	SN351A	SN352A	UNITS
Differential DC Input Offset, max	7.5	7.5	7.5	14	mv
AC Voltage Gain, min	185	185	1950	2000	v/v
AC Signal Swing, min	17.5	17.5	17.5	17.5	V_{P-P}
Upper Cutoff Frequency, min	48	190	48	190	KC
Input Impedance, min	130	34	17	3.4	KΩ
Common Mode Rejection, min	80	80	80	80	db

circuit schematic



mechanical data

Solid Circuit semiconductor networks are mounted in a glass-to-metal hermetically sealed package. Leads are gold-plated Kovar. Weight: 0.1 gram. All external surfaces are metallic and isolated from leads and circuit. Mylar* insulators are available.



Notes: 1. All decimals ±0.005 except as noted.
2. *Denotes tolerance of ±0.015 at extremities and ±0.005 at package, nonaccumulative.
3. Lead centerlines located in true position within ±0.005 of body centerlines.

LEADS REMOVED
SN717A– 1, 3, 5, 10, 12, 14
SN350A– 1, 3, 5, 10, 12, 14
SN351A– 1, 3, 5, 10, 12, 14
SN352A– 1, 3, 5, 10, 12, 14

*Reg. trademark, E. I. du Pont

PRELIMINARY DATA SHEET: Supplementary data will be published at a later date.

TEXAS INSTRUMENTS
INCORPORATED
SEMICONDUCTOR-COMPONENTS DIVISION
POST OFFICE BOX 5012 • DALLAS 22, TEXAS

SOLID CIRCUIT® TYPES SN717A, SN350A, SN351A, SN352A
DIFFUSED SILICON GENERAL PURPOSE AMPLIFIER NETWORKS

absolute maximum ratings*

Supply Voltages: V_{cc1} . . . . 8 v
V_{cc2} . . . . −16 v
V_{cc3} . . . . 16 v
Power Dissipation . . . . 175 mw
Common Mode Input Voltage . . . . ±4 v_{p-p}
Storage Temperature Range . . . . −65°C to +150°C

$T_A = 25°C$

ELECTRICAL CHARACTERISTICS	TEST CIRCUIT	CONDITIONS	SYMBOL	SN717A MIN	SN717A MAX	SN350A MIN	SN350A MAX	SN351A MIN	SN351A MAX	SN352A MIN	SN352A MAX	UNITS
Power Drain Currents	Fig. 1	Outputs and test input open, Supply voltages ±0.5% nominal	ID_1	0.66	2.1	3.4	9.0	0.70	2.3	3.5	10.0	ma
			ID_2	1.0	3.0	3.7	10.0	1.0	3.4	4.2	11.0	ma
			ID_3	—	—	—	—	0.15	0.45	0.7	2.2	ma
Differential DC Input Voltage Offset	Fig. 1	Outputs and test input open, Supply voltages ±0.5% nominal	DIVO	—	7.5	—	7.5	—	7.5	—	14	mv
Common Mode DC Output Voltage Offset	Fig. 1	Outputs and test input open, Supply voltages ±0.5% nominal	CMOVO	—	350	—	350	—	350	—	700	mv
AC Voltage Gain	Fig. 1	$AV = E_{OUT}$ rms/E_I rms Supply voltages ±0.5% nominal See Note 1	AV	185	245	185	245	1950	6500	2000	8000	v/v
AC Signal Swing	Fig. 1	$ACSS = (E_{O1} - E_{O2})$ at point that clipping first occurs with E_I of increasing amplitude, 1000 cps sine wave. Supply voltages ±0.5% nominal	ACSS	17.5	—	17.5	—	17.5	—	17.5	—	V_{p-p}
Upper Frequency Cutoff	Fig. 1	Frequency at which E_{OUT} is 3 db down from value at 1000 cps with E_I of constant amplitude in fh	fh	48	—	190	—	48	—	190	—	KC
Differential DC Current Offset Input	Fig. 3	$DICO = \frac{V_A - DIVO}{R_S}$ where V_A is DC voltage from point A to ground. Supply voltages ±0.5% nominal	DICO	—	100	—	400	—	450	—	4000	na
Input Impedance	Fig. 3	See Note 2	Zin	130	—	34	—	17.0	—	3.4	—	KΩ
Midband Common Mode Rejection Ratio	See Note 3	See Note 3	CMRR	80	—	80	—	80	—	80	—	db

*absolute maximum ratings are limits, above which, operation and life expectancy may be impaired. See electrical characteristics for recommended operating conditions.

Supply voltages ±5% nominal unless otherwise stated.

Note 1. Test input, $E_I = 0.1$ mv rms ± 3%, 1000 cps sine wave for SN351A, SN352A; $E_I = 1.0$ mv rms ± 3%, 1000 cps sine wave for SN717A, SN350A.

Note 2. With device in test circuit of Figure 3, a 100 cps sine wave voltage input, E_I is imposed with switch S closed and E″ is measured as E_{OUT}; with E_I unchanged in frequency or amplitude switch S is opened and E′ is measured as E_{OUT}. $Zin = \frac{R_S}{E''/E' - 1}$

Note 3. With device in test circuit of Figure 1, a 1000 cps sine wave voltage input, E_I is imposed and G″ measured as ratio of E_{oI} to E_I; with device in test circuit of Figure 2, a 1000 cps sine wave voltage input, E_I is imposed and G′ measured as ratio of E_{oI} to E_I. $CMRR = 20 \log_{10} \left[\frac{G''}{G'}\right]$

Note 4. Thermal resistance equals .25°C/mw max.

SOLID CIRCUIT® TYPES SN717A, SN350A, SN351A, SN352A
DIFFUSED SILICON GENERAL PURPOSE AMPLIFIER NETWORKS

TEST CIRCUITS

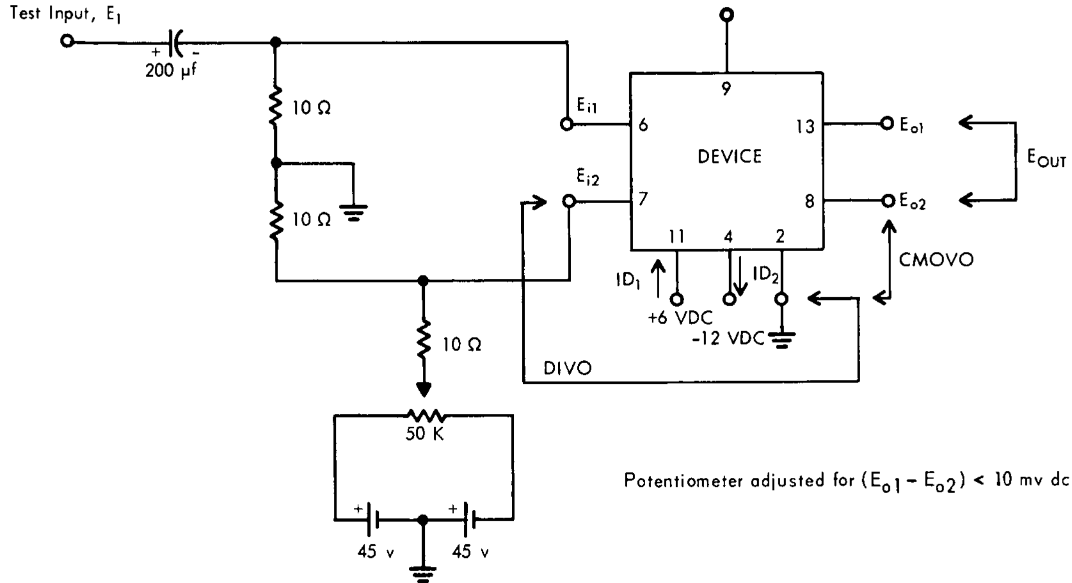


Figure 1 (See Note 5)

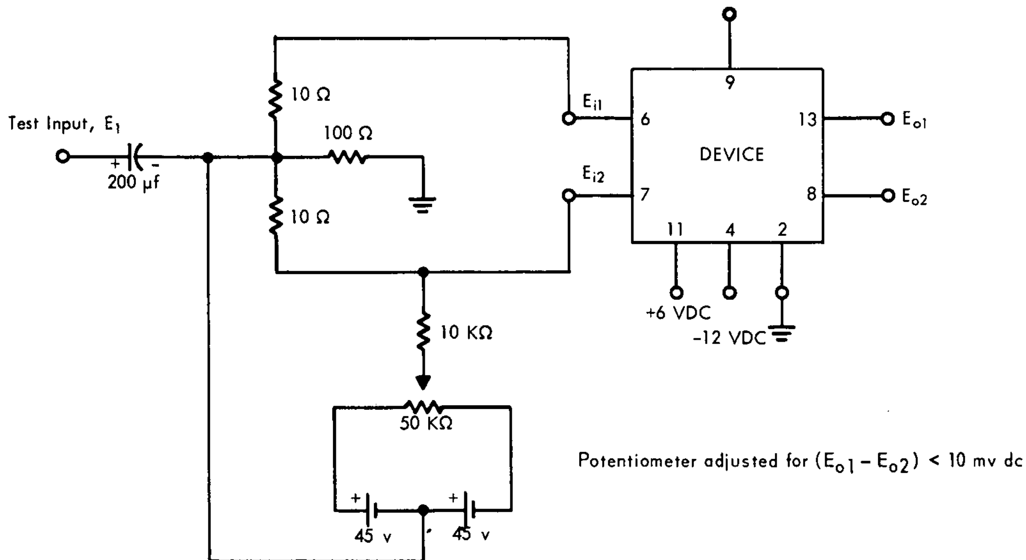
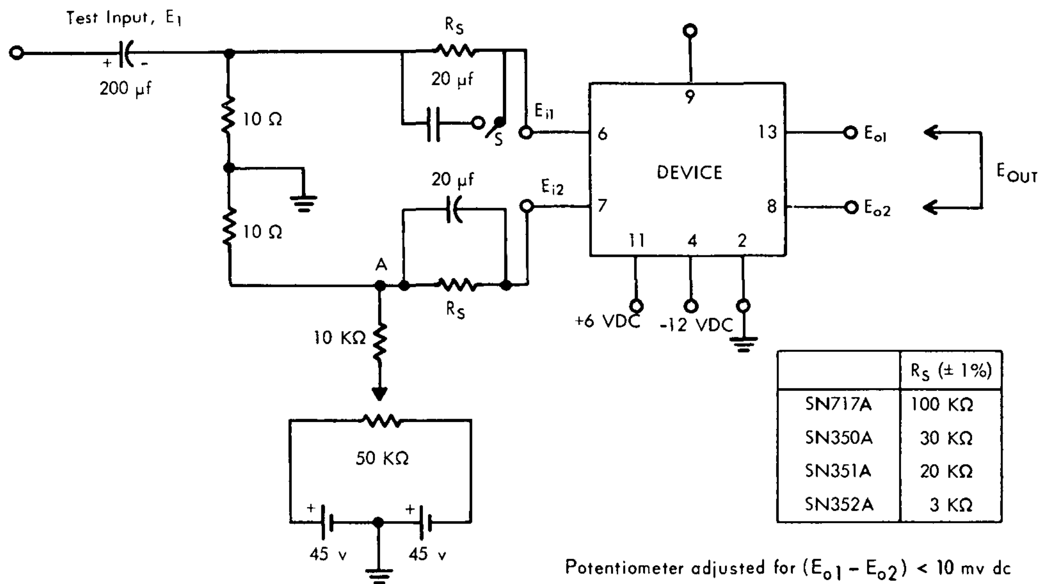


Figure 2 (See Note 5)

Note 5: Pin 9 connected to +12 v supply on SN351A and SN352A.
Pin 9 connected thru .01 µf ±10% capacitor to ground on SN717A.
Pin 9 not used on SN350A.

TEST CIRCUIT



	R_S (± 1%)
SN717A	100 KΩ
SN350A	30 KΩ
SN351A	20 KΩ
SN352A	3 KΩ

Figure 3 (See Note 5)

Note 5: Pin 9 connected to +12 v supply on SN351A and SN352A.
Pin 9 connected thru .01 µf ±10% capacitor to ground on SN717A.
Pin 9 not used on SN350A.

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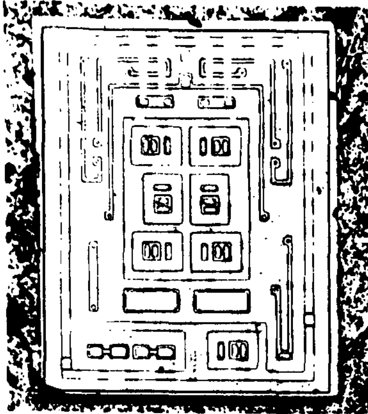
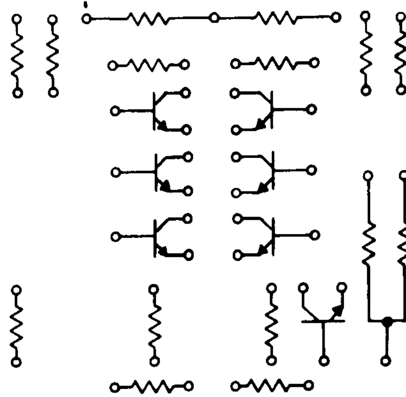
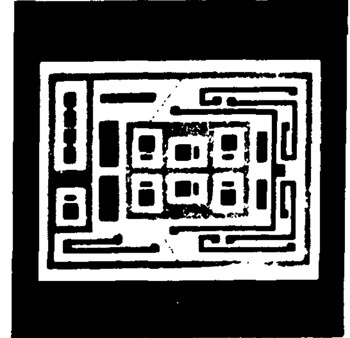
Exhibit 5-6

INTEGRAL CIRCUITRY

NM-3011, NM-3015







DATA SHEET IC105A/MAY '65
TENTATIVE SPECIFICATIONS

MASTER DICE BREADBOARDS

The NM-3011 and NM-3015 are single-crystal master dice breadboard chips containing all the elements of monolithic integrated micro-circuits but lacking interconnecting patterns. Instead, the connections to the individual elements within the dice are brought out to bonding pads.

Thus, a designer can produce his own circuit by bonding interconnections, or by providing Norden with a schematic for the connections, thereby making possible a fast, economical method of proving feasibility of an integrated circuit design.

CHARACTERISTICS*

RESISTORS		TRANSISTORS	TYPICAL VALUES	
R_1, R_8	3900 Ω ± 20%, ± 5% Match	Q_1 to Q_7 — NPN TYPE	NM-3011	NM-3015
R_2, R_7	5000 Ω ± 20%, ± 5% Match	BV_{CIO} $I_C = 0.01$ ma, $I_B = I_E = 0$	80V	100V
R_3, R_6	5000 Ω ± 20%, ± 5% Match	BV_{CBO} $I_C = 0.01$ ma, $I_E = 0$	30V	60V
R_4, R_5	165 Ω ± 20%, ± 5% Match	BV_{EBO} $I_E = 0.01$ ma, $I_C = 0$	9V	9V
R_9	750 Ω ± 20%	V_{CEO} (Sust) $I_C = 10$ ma, $I_B = 0$	15V	30V
R_{10}, R_{11}	250 Ω ± 20%, ± 5% Match	V_{CER} (Sust) $I_C = 10$ ma, $R_{BE} \leq 10\ \Omega$	20V	50V
R_{12}, R_{13}	25 Ω to 40 Ω	BETA $I_C = 1$ ma, $V_{CE} = 5V$	40	80
R_{14}	1700 Ω ± 20%	V_{CE} (Sat) $I_C = 5$ ma, $I_B = 0.5$ ma	0.8V	0.3V
R_{15}	2700 Ω ± 20%	V_{BE} (Sat) $I_C = 5$ ma, $I_B = 0.5$ ma	0.8V	0.75V
	TCR = +0.25%/°C			

*@ $T_A = 25°C$

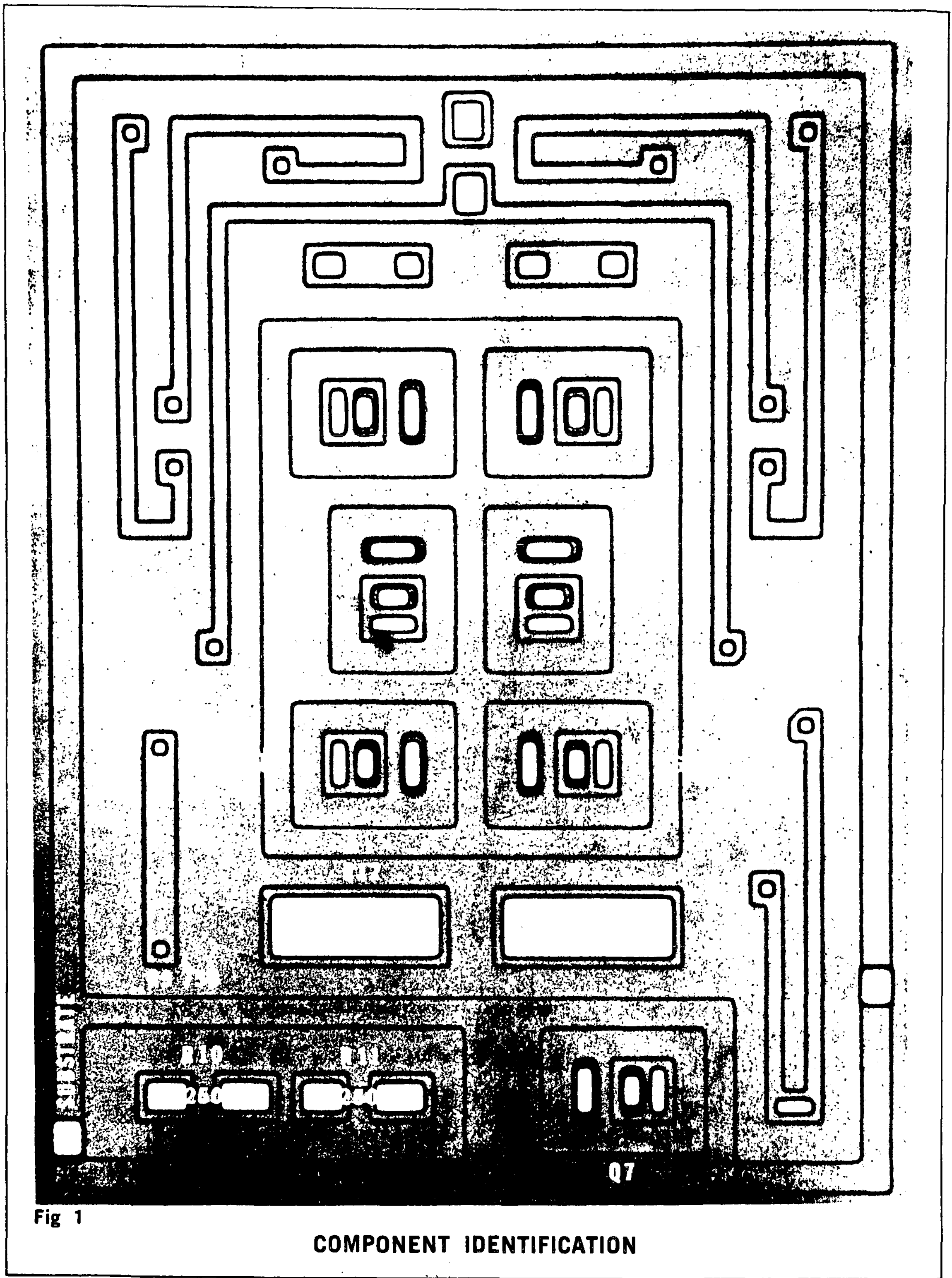


Fig 1

COMPONENT IDENTIFICATION

168

Exhibit 5-7

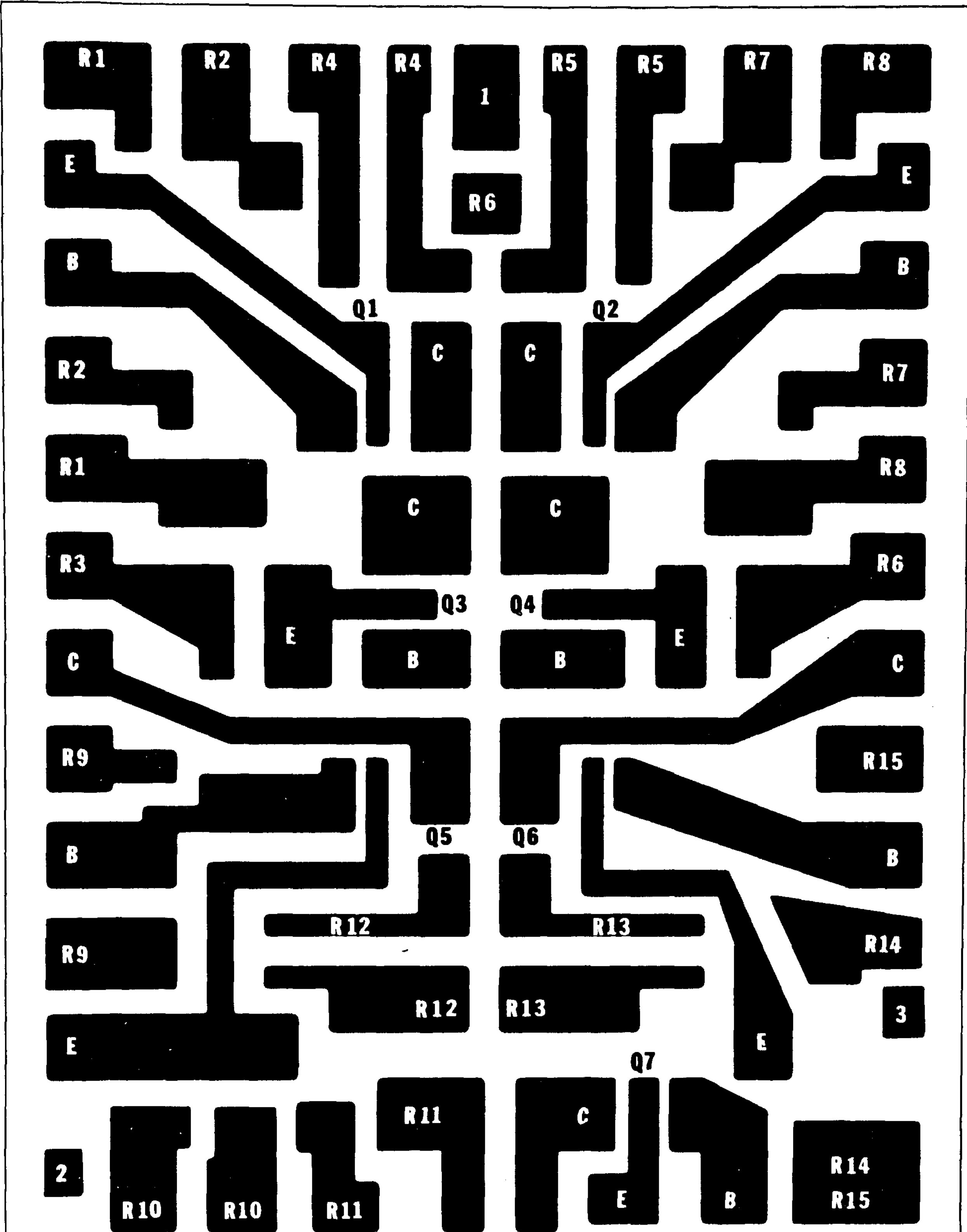


Fig 2

COMPONENT TERMINAL PAD LAYOUT

1 — Resistor substrate, connect to most positive potential   2, 3 — Chip substrate, connect to most negative potential

EXPERIMENTAL I.F. AMPLIFIER

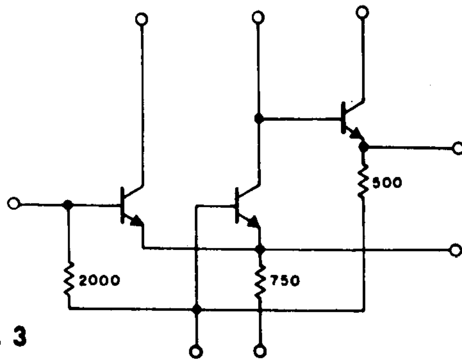


Fig. 3

MULTI-PURPOSE AMPLIFIER CIRCUIT

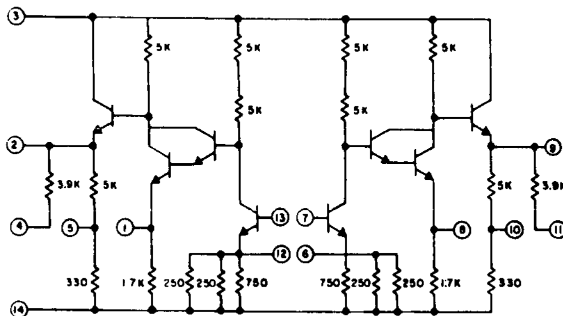
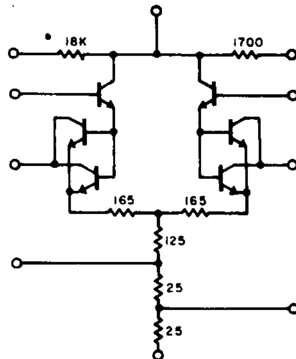


Fig. 4

GYRO CONTROL PRE-AMPLIFIER



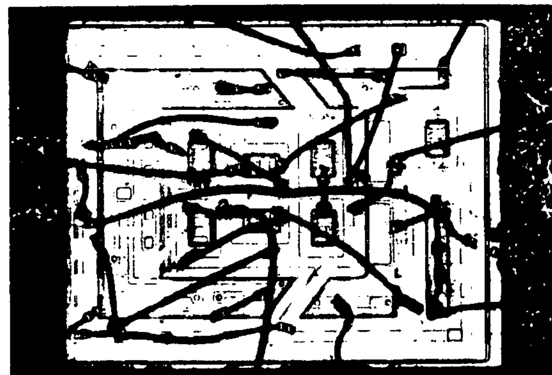


Fig. 5

Typical circuits breadboarded using the NM-3011 and NM-3015 are shown in figures 3, 4 & 5. Other circuits that have been successfully produced include 1-strobe and 2-strobe sense amplifiers, 2-stage differential amplifier, delay line read amplifier, voltage comparator, error amplifier, differential current amplifier, high-gain general purpose amplifier, low power audio amplifier, Schmitt trigger, high input impedance amplifier, filter amplifier, IF amplifier and several binary switching elements.

The NM-3011 is identical with the NM-3015 except for transistor parameters, as shown in the table on the front page. Either type can be supplied mounted on a 12-, 10-, or 8-lead TO-5 header, or in a flat pack. The dice themselves measure 0.065 by 0.085 inch. Unless otherwise specified, will be supplied on 12 pin header.

RELIABILITY AND PHYSICS OF FAILURE OF MICROELECTRONIC DEVICES

SIX

6.1 System Reliability Improvement

The potential for improved system reliability offered by semiconductor integrated circuits has been a major factor in the widespread introduction of microelectronics into aerospace programs. The effect of the microelectronic device on interconnections, resistance to environment, manufacturing, test, human factors, and system design will contribute greatly to improved system reliability. Investigations by both Government and industry indicate that the following system improvements will be achieved through the use of microelectronics:

(1) Reduction in the number of individual parts and connections

(2) Improved intraconnection and interconnection techniques

(3) Increased resistance to environment

(4) Improved design

(5) Improved manufacturing processes

(6) Improved testing techniques

(7) Fewer circuit configurations

(8) Fewer types of environmental effects

(9) More effective use of redundancy techniques

(10) Lower power consumption (in many cases)

6.1.1 Reduction in the Number of Parts and Connections

The reduction in the number of individual parts, with the attendant reduction in the number of interconnections, contributes substantially to system reliability improvement.

The reliability of a conventional circuit (nonredundant) is predicted on the basis of the failure rates of its constituent parts. Generally, the lower the complexity level, the higher the reliability. For example, the failure rate of a particular NAND gate in discrete form is the sum of the failure rates of its 34 components (13 resistors, 7 capacitors, and 17 transistors) and 215 interconnections. A monlithic integrated circuit performing the same circuit function, has one failure rate, which is lower than the sum of the transistor failure rates. Thus system reliability improves in proportion to the complexity of the discrete circuit being replaced by an integrated circuit.

6.1.2 Improved Connection Techniques

Connections will be considered herein as either intraconnections (conductors and connections within the integrated circuit or its discrete equivalent) or interconnections (conductors and connections that provide electrical continuity between the circuit and the outside world).

6.1.2.1 Intraconnections

The integrated circuit usually has less than half the number of intraconnections required by its discrete equivalent. In addition, the quality of the integrated circuit intraconnections is superior to that of the discrete-circuit intraconnections. Two types of intraconnections must be considered: the highly reliable aluminum evaporation intraconnection and the intraconnection resulting from thermocompression bonding.

The interface resulting from the deposition (evaporation) of a conductor on a compatible surface under ideal conditions is virtually equivalent to a continuous conductor. A failure within such an interface is highly unlikely in an operating device if strict process control is maintained during the deposition phase (see Failure Modes and Mechanisms).

Unfortunately, the current state of the art limits thin-film technology (used for the aluminum evaporation) to a uniform, smooth surface. Therefore, leads from the silicon chip to the package leads must be connected by another method, usually thermal-compression bonding. While this process is far from being perfected, it has been in use in transistor fabrication for several years.

Thermocompression bonds have no known failure mechansims when compatible materials are being bonded in an ideal environment, a circumstance that does not appear practical at the present. However, industry is making a determined effort to minimize the failure mechanisms that occur in the absence of such favorable conditions.

6.1.2.2 Interconnections

The quality of interconnections will also improve with the increased use of microelectronics. The importance of interconnection reliability can be seen if it is assumed that each integrated circuit with 10 leads will involve about 100 interconnections. So that the interconnections will not experience more failures than the devices, each interconnection must exhibit a failure rate at least two orders of magnitude lower than that of an integrated circuit. In other words, there is a distinct possibility that interconnections, rather than microelectronic devices, will be the major cause of unreliability in future systems. The importance of interconnection reliability in microelectronic systems makes it essential that industry devote considerably more attention to methods for improving reliability in this area.

Because of the small size and large number of leads of the integrated circuit, it is frequently advisable to use a multilayer etched-circuitry interconnection technique. The multilayer approach can provide a high level of reliability if careful design and stringent process controls are exercised.

The conventional circuit may include evaporated, thermocompression, welded, crimped, and soldered connections -- involving a number of different materials with different thermal-expansion, solid-state stress-strength, chemical, and manufacturing characteristics. This variance in characteristics leads to uncertainties in design, and in lower reliability than experienced in microelectronic systems, which require fewer connection techniques.

6.1.3 Increased Resistance to Environment

The integrated circuit offers greater resistance to its environment, primarily because of its small mass and size. It is less susceptible to forces of acceleration, i.e., shock and vibration; shielding from radiation, heat, etc., is not as great a problem.* Hermetic sealing reduces corrosion.

6.1.4 Improved Design

It is often said that most failures experienced in system operation were designed into the system. In other words, a significant portion of potential system unreliability can be avoided by careful design. If this is true, the

*However, as discussed in Chapter 5, small-size and encapsulation present some particular problems also.

effect of microelectronics on system design may well be the "dark horse" key to system reliability.

At the circuit level, the likelihood of improved design is obvious. Trained circuit designers are responsible for the design of each circuit. Since the economics of the circuit manufacturer depends on a large-volume market, he is willing to spend considerable time and effort proving the design of each circuit to protect his investment.

Not so obvious is the impact of the integrated circuit on system design and, consequently, on system reliability. Microelectronics in system design offers the following advantages, which directly or indirectly influence reliability:

(1) The design engineer has a wider job scope because of the availability of large building blocks: for the design of a given function, fewer engineers are required. This in turn reduces the communications problem, which should result in improved reliability. (An example of the effect of using larger building blocks is a ground checkout computer recently redesigned by an organization in the aerospace industry. The original, discrete version contained 26,000 parts; the microelectronic version of the same computer contained 3000 parts. If the microelectronics design were converted back to a discrete version on a part-for-part basis, the resulting discrete computer would contain about 12,000 parts -- a better-than 50% reduction from the number of parts in the original computer. Designers engaged in this project said that because two systems designers using microelectronics could replace the ten designers required by the original discrete approach, they were able to find functions that could be combined in a single circuit, drastically reduce interfacing, and condense other functions.)

(2) The designer has more time available to concentrate on potential reliability problems because design begins at the circuit level.

(3) Designers need to be familiar with the idiosyncrasies of a few different circuits as compared with 500 to 600 device characteristics, which should lower the probability of misapplication.

(4) Integrated circuits encourage the maximum use of digital design, which will usually improve system reliability by minimizing the number of out-of-tolerance failures.

6.1.5 Improved Manufacturing

From a manufacturing viewpoint, the reliability of a part is proportional to the continuity of production and the simplicity of the part's construction. The manufacture of an integrated circuit can be considered as two operations: pre-assembly and assembly. In the pre-assembly portion -- i.e., material preparation, masking, and diffusion -- the manufacturer, by necessity dependent on yield, must constantly improve and monitor his process control. Since the reliability of an integrated circuit depends on process control, the manufacturer is also obligated to improve and monitor reliability. In the assembly portion of the operation, i.e., when the silicon chip is mounted in a package and leads are made to the outside world, simplicity is the byword. As in the case of transistor assembly, automation or semi-automation will become commonplace.

In the manufacture of a discrete circuit, many suppliers have a role, but only the circuit designer is directly responsible to the customer. In the case of the integrated circuit, a single manufacturer is responsible for accepting raw material, processing the entire circuit, and assuring that the completed circuit performs in accordance with the specifications. Thus the single integrated-circuit manufacturer is better able to coordinate and control the factors that may influence circuit reliability.

It is generally acknowledged that process control is the key to reliability. Since the number of processes represented by an integrated circuit is far smaller than the number involved in a conventional circuit, a given degree of control on these relatively few processes results in a much higher effective control of processes and thus in higher reliability. When the different processes are totaled for a complete system, the relatively few processes represented by microelectronics will have a very significant effect on the reliability.

6.1.6 Improved Testing Techniques

Since the integrated circuit is more complex than the transistor, more effort is expended on functional testing before the circuit leaves the manufacturer. While testing alone does not improve reliability, it does strengthen quality control, as evidenced in both increased failure-free operation and improved process controls.

Generally, qualification testing of integrated circuits is more stringent than that of their discrete counterparts; that is, the testing is concentrated at the circuit level rather than at the component level, making the test results more meaningful.

At the system manufacturer's facility, incoming inspection is simplified because the quantity and variety of parts to be tested is reduced. After the system prototype is completed, the "debugging" test is simplified if integrated circuits are used. (In one case, test time was reduced from six months to two weeks by microelectronic design.)

System performance evaluation by the user is also easier because of the greater simplicity of system design. Built-in test and fault-isolation techniques are more productive in microelectronic systems, resulting in higher mission reliability.

6.1.7 Fewer Circuit Configurations

The variety of circuit configurations employed in a single microelectronic system will be quite small compared with that of a discrete-component system. The causes of unreliability can therefore be more easily predicted and prevented. Other reliability influences enhanced by the reduced circuit variety include human factors and system design.

6.1.8 Fewer Types of Environmental Effects

Excessive drift is a major factor in the failures of discrete systems. Designing to a single network's drift characteristics is considerably less complex than designing to the many drift characteristics of various transistors, diodes, resistors, and capacitors made of many different materials -- as is necessary with discrete-component circuits.

The ease of matching characteristics such as temperature coefficients of integrated-circuit elements can also be used to reduce the effects of environmental changes.

6.1.9 More Effective Use of Redundancy Techniques

The reduction in weight, volume, and cost associated with integrated circuits makes the use of redundancy practical even at the circuit-element level. The application of various forms of redundancy, e.g., circuit or functional, majority voting logic, and adaptive techniques, has started only recently, since microelectronics has become an accepted technology.

6.1.10 Lower Power Consumption

The low power requirements of the typical integrated circuit frequently allow minimum electrical stresses to be imposed on the microelectronic system. Since reliability is inversely proportional to stress, an increase in reliability is expected when the integrated circuits are used within specification.

6.2 Failure Modes and Mechanisms*

The failure modes and mechanisms of integrated circuits are similar to those of transistors, but, as would be expected, the distribution of these modes and mechanisms is different. The failure-mode distribution of integrated circuits differs according to manufacturer and logic type. The failures observed to date are the result of metallurgical defects, surface effects, mechanical imperfections, and bulk defects. Failure modes and mechanisms of integrated circuits are discussed below with respect to these general categories. Tables 6-1 and 6-2 summarize the results of surveys of integrated-circuit users and manufacturers, respectively; the purpose of these surveys was to determine the relative prevalence of the failure modes. Table 6-3 identifies some of the more important failure modes.

TABLE 6-1

PRINCIPAL FAILURE MODES IN ORDER OF PREVALENCE, AS REPORTED BY INTEGRATED-CIRCUIT USERS

User	No.	Failure Mode
User A		
	1.	Metallurgical Defects - plague
	2.	Metallurgical Defects - metalization problems
	3.	High leakage
User B		
	1.	Surface Effects caused by loss of hermetic integrity
User C		
	1.	Electrical Degradation - cause not specified
	2.	High Leakage - cause not specified
	3.	Mechanical Defect - chipped glass
User D (Flight Operational System)		
	1.	Intermittent between pins and flat-pack
	2.	Intermittent between printed circuit board and flat-pack leads that are soldered
	3.	Open aluminum paths
	4.	Mechanical defects from wire bonding, resulting in shorts and opens
	5.	Improperly etched aluminum evaporated leads, causing shorting
	6.	Broken die

*Most of the information on failure mechanisms (including all photographs) was supplied by the Univac Division of Sperry Rand Corporation.

TABLE 6-2

PRINCIPAL FAILURE PROBLEMS IN ORDER OF PREVALENCE,
AS REPORTED BY INTEGRATED-CIRCUIT MANUFACTURERS

Manufacturer 1

1. Bonding
2. Black plague

Manufacturer 2

1. Contacts
2. Surface
3. Bulk

Manufacturer 3

1. Bonding
2. Metalizing
3. Other mechanical problems, welds, and broken wires
4. Electrical overstress

Manufacturer 4

1. Bonding
2. Contacts
3. Improper encapsulant

Manufacturer 5

1. Contamination of Al films
2. Oxide growth
3. Electrical overstress
4. Epitaxial growth

Manufacturer 6

1. Deterioration of interconnections
2. Short through oxide layer
3. Purple plague
4. Other mechanical problems, welds, and broken wires

Manufacturer 7

1. Bonding
2. Contamination of Al films

Manufacturer 8

1. Bonding

Note: The distribution of integrated-circuit failure problems at Texas Instruments was determined to be as follows:

Surface effects, excluding metalization	34.5%	Design	5.5%
Bonding	28.8%	Bulk	2.7%
Metalization	22.9%	Other	5.8%

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TABLE 6-3

INTEGRATED-CIRCUIT FAILURE MODES

Mechanism	Mode	Control
Metallurgical Defects		
Formation of gold aluminum and gold-aluminum-silicon compounds around bonds, activated by excessive bonding or sealing temperatures (plague)	Decreased bond strength; high impedance; brittle joints	Adequate conductor thickness, strict control of bonding and sealing temperatures, or use of different materials (detected by extensive bake followed by shock or centrifuge test)
Improper wafer cleaning, insufficient bonding temperature, or pressure (under bonding), insufficient conductor thickness	Open bonds-electrolysis; gold leads pull away from aluminum conductor pattern -- open metalization patterns	Care in cleaning and bonding operations and adequate conductor thickness (detected by 20,000 acceleration test)
Overetched metalization	Opens in aluminum conductor path	Adherence to proper layout and bonding procedures (detected by shock, vibration and centrifuge tests)
Tensile fracture and melting due to abrupt changes in the level of surface passivation near contact areas, where high current densities are probable	Open in aluminum conductor path, particularly around contact areas	Process control and provision for adequate conductor thickness (detected by life tests)
Over-bonding, excessive bonding temperature and pressure	Bond, aluminum conductor, and part of the surface passivation layer are removed from the device surface.	Control of bonding temperature and pressure (detected by 20,000 G acceleration test)
Surface Effects		
Pin holes and entrapped impurities in passivation layers	Electrical breakdown in surface passivation from the aluminum conductor to component areas in the silicon	Control of surface-oxidation thickness and, possibly, oxide growth rate (detected by life testing)
Etchants or other processing materials not completely removed by cleaning	Opening of aluminum conductor pattern	Extreme care in cleaning operations (detected by life testing)
Ionic-surface effects	Channeling, accumulation, and depletion, resulting in changes in electrical characteristics	Changes in surface-preparation process, use of guard ring diffusion
Mechanical Imperfections		
Moisture content within the package	Shorts near surface scratches or steps in surface passivation where current densities in the conductor pattern are high	Low-moisture environment for sealing of packages (detected by life testing or filling packages with dry nitrogen)
Poor sealing, which permits moisture to enter the package	Intermittent or degraded operation	Improved sealing procedures and methods (detected by leak tests)
Wafer scribing process, accelerated by die-bonding operation	Progressive chipping or cracking of substrates, resulting in shorts and opens, respectively. Scribing too close to the bond, with resultant shorts	Extreme care and visual inspection during scribbing and die-bonding operations (detected by life tests)
Scratches and smears on the surface materials caused by faulty tools or mishandling	Open aluminum conductor paths, open bonds, shorts between aluminum paths, base-to-base shorts	Improved handling methods and procedures and increased visual inspection
Poor lead dress or excessive lead length due to poor layout of aluminum terminal pads with respect to the package leads	Open and shorted internal leads, intermittent operation	Proper layout and bonding procedures (detected by shock, vibration, and centrifuge tests)
Improper design fabrication or use of masks	Open contacts, high contact resistance, shorted junctions	Improved techniques for mask design and alignment (detected by electrical performance tests)
Improper packaging and labeling, and the inclusion of "junk" (glass or gold particles, etc.) in the package	Shorts, misapplication of the device, intermittent operation	Improved workmanship and in-process inspections

The system engineer's proper understanding of integrated-circuit failure modes and mechanisms is essential to optimum design, choice of vendor and logic, vendor testing specifications, and screening test design.

6.2.1 Metallurgical Defects

Failures resulting from metallurgical defects constitute the largest segment of integrated-circuit reliability problems. Such defects include those caused by plague, aluminum intraconnection problems, overbonding, and underbonding.

6.2.1.1 Plague

Plague is a term used to describe a time-dependent formation of a chemical compound at semiconductor-metal or metal-metal contacts that increases contact resistance and weakens bonds. It is one of the most significant integrated-circuit failure mechanisms. Plague has been the subject of many detailed physics-of-failure studies (not all in agreement) which are beyond the scope of this chapter. The following types of plague are most commonly encountered:

(1) Purple Plague - The time-temperature formation of the gold-aluminum $AuAl_2$. (Some studies argue that purple plague is not created during extended bakes at 200°C or less.)

(2) Black Plague - The time-temperature formation of the ternary Au-Si-Al compound formed at about 300°C. The silicon apparently acts as a catalyst. Figure 6-1 shows a device which failed because of black plague, causing opens in the narrow regions of the interconnect pattern near the ball bonds.

(3) White Plague - Aluminum hydroxide

(4) Silver Plague - Tin migration along the bond wire

(5) Periphery Plague - A situation in which a small amount of one of the plagues described above is present and the aluminum pad area is too small. Normally neither condition alone would cause a failure, but together they are likely to create an open. It is quite apparent that the bonding pads in Figure 6-2 are too small to accommodate the large ball bond, an example of periphery plague.

Plague is generally the result of a poorly controlled bonding procedure and is common to the transistor. It often can be screened either by visual inspection, by mechanical stress -- e.g., a tensile strength test, before the device is capped -- or by a high-linear-acceleration test after the capping.

6.2.1.2 Aluminum Intraconnection Problems

Aluminum intraconnection problems include the following:

(1) Poor Adherence - The result of applying aluminum metalization to a surface that has not been properly cleaned to permit good alloying of

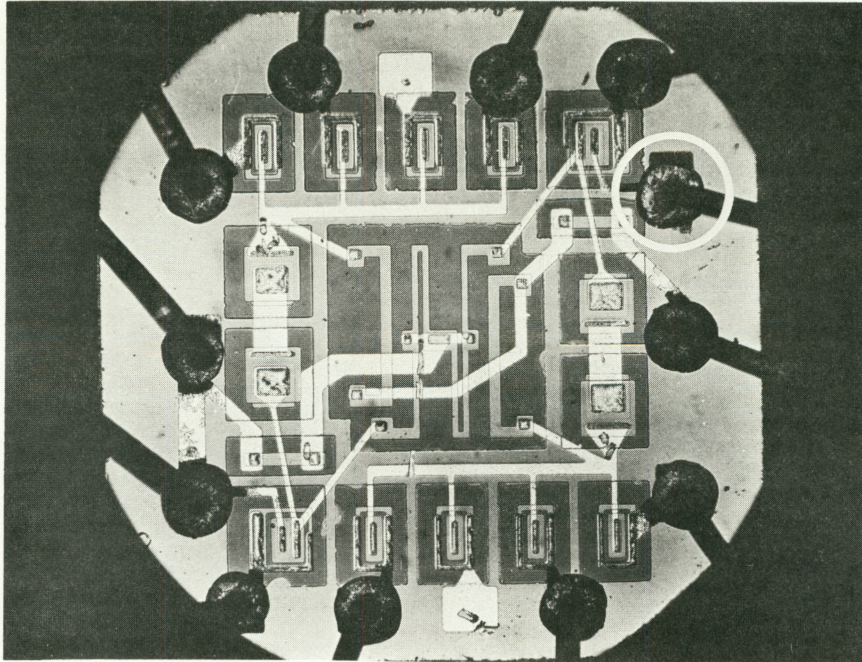

FIGURE 6-1

OPEN CIRCUIT CAUSED BY BLACK PLAGUE

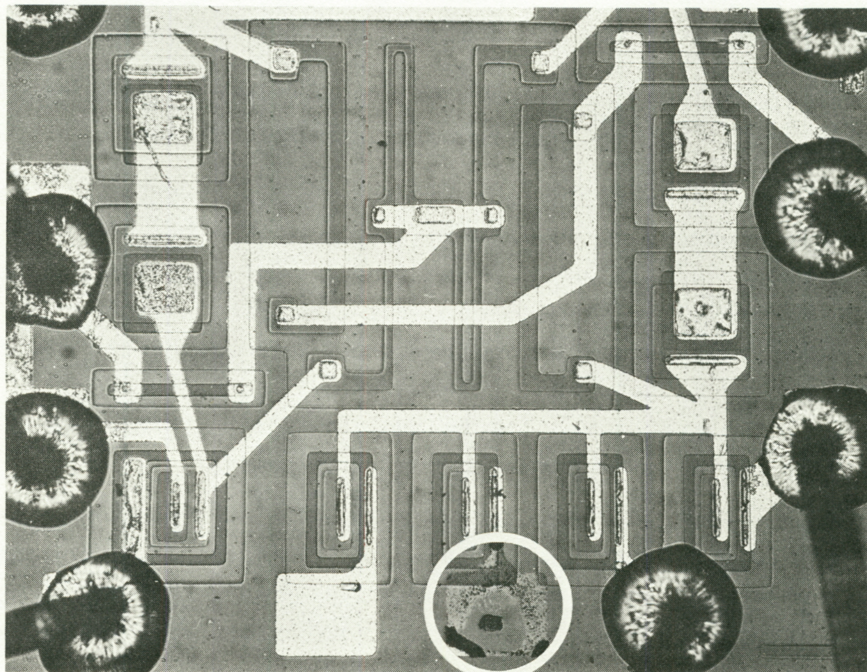

FIGURE 6-2

OPEN CIRCUIT CAUSED BY PERIPHERY PLAGUE

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the metalization to the silicon oxide. This failure mechanism is triggered by mechanical stress such as pulling, probing, or thermal shock.

(2) Overetched Metalization - The result of etching the metalized intro-connection to the extent that the conducting path is too narrow to carry required currents.

(3) Electrolysis - The result of the inclusion of ionic materials on the surface of a device and the effect these contaminants have on metalization when a potential is applied.

(4) Melted or Vaporized Metalization - Excessive currents can cause the metalized intraconnection to be vaporized or melted, particularly where the cross-sectional area is reduced. This reduction generally occurs where the metalization crosses an oxide cut.

(5) Insufficient Aluminum Metalization - Insufficient thickness of the deposited aluminum conductor can make it difficult to achieve adequate deposition over areas of vertical steps in the passivation without causing failure by plate-through on other surfaces. These steps result from the multiple oxidize-etch actions, which selectively operate on different areas; there are often as many as three or four steps. Thin plating on the vertically oriented surfaces may result in an open or a high resistance because of high current densities in the thin layer of metal. This problem can be aggravated when elevated temperature combines with the heat of the high-current density.

Metalized leads must always be considerably thicker than the oxide step height to assure continuity across the step.

Even when the metalization is considerably thicker than the step height, reduced cross sections occur if the step is very steep and the metal deposition is directional. This problem can be minimized by the use of multifilament metal-evaporation systems during deposition to assure an adequate nondirectional buildup of the deposited metal. Figure 6-3 illustrates, in exaggerated form, the type of directional metalization that results in the failure modes discussed above. Figure 6-4 is an example of the phenomenon.

(6) Other opens in Al Intraconnections - (a) Hydrated alumina (Al_2O_3) that has formed at dissimilar-metal contacts in the presence of excessive moisture (may be formed at room temperatures but is accelerated by power operation or baking); (b) hydrated alumina caused by faulty wash and dry techniques; and (c) aluminum corrosion at scratches.

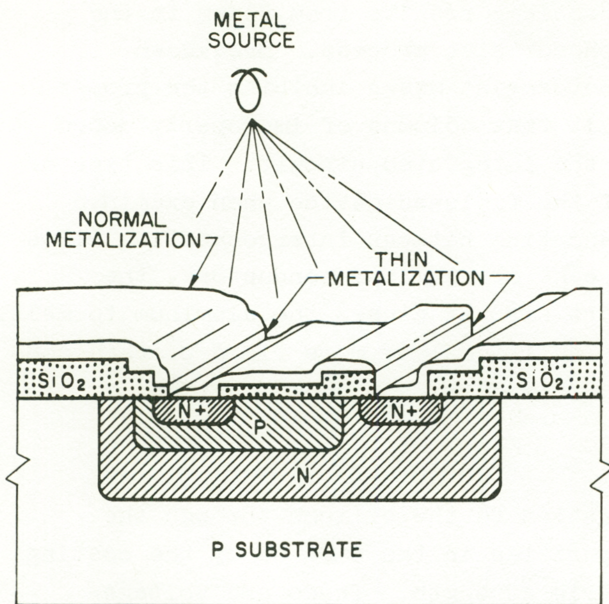

FIGURE 6-3

THIN METALIZATION RESULTING FROM DIRECTIONAL DEPOSITION

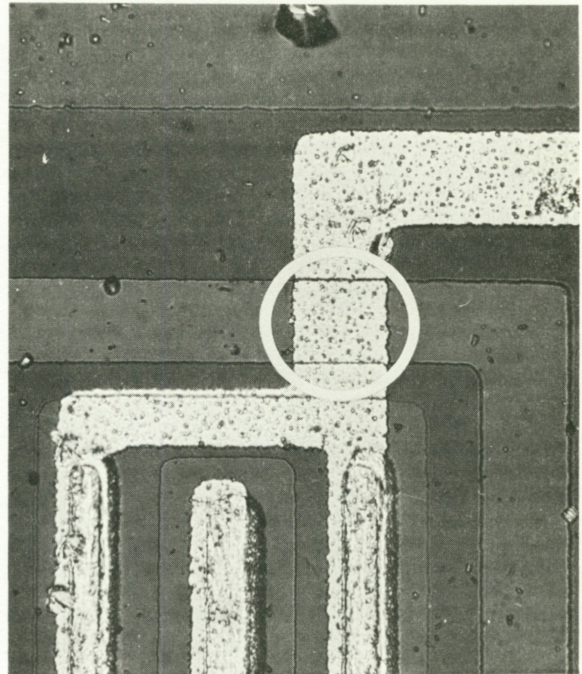

FIGURE 6-4

THIN METALIZATION ON INTEGRATED CIRCUIT

6.2.1.3 Overbonding

Overbonding, resulting from excessive temperature or pressure, or both, is a non-time-dependent failure mechanism. Under such conditions, SiO_2 pulls up, causing the aluminum to peel or lift, exposing raw silicon. A crack in the substrate, resulting in a short circuit, may also be caused by excessive pressure.

6.2.1.4 Underbonding

Underbonding, the result of insufficient temperature or pressure or both, during the bonding process, is another non-time-dependent failure mode that results in an inadequate metallurgical bond between the gold and the aluminum. This failure mode can be triggered by mechanical stressing.

6.2.2 Surface Effects

Surface effects also contribute significantly to integrated-circuit unreliability. Failure mechanisms in this category include the following: pinholes and other shorts through the SiO_2, corrosive etching, insulation layers, ionic surface effects, loss of hermetic integrity, and effects of environmental stresses.

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6.2.2.1 Pinholes

One of the major surface-instability problems results from flaws in the passivation caused by deficiencies in the photoresist process. Breakdown or the inclusion of foreign particles in photoresist masks inhibits the proper doping of the silicon wafers, with the result that columns of improperly doped materials may appear in a critical area of the integrated circuit. This type of flaw appears as a pinhole in the surface of the finished device when examined under dark-field illumination; it permits shorting between interconnecting films and other portions of the circuit. In the case of aluminum conductors, the high-density current resulting from the short circuit causes the aluminum to melt. This problem can be minimized by the use of additional or more rigid process controls for mask inspection, mask usage, dark-room dust, and contamination.

6.2.2.2 Other Shorts Through the SiO_2

Other shorts from the aluminum metalization to the silicon through the silicon-dioxide are caused by entrapped impurities in the SiO_2 or by the coating of the SiO_2 with substances of poor dielectric strength. These are voltage-dependent failure modes.

Pinholes and the other shorts mentioned above generally can be detected during parameter testing. A particular test for pinholes is the application of over-voltage to the various diodes while current is stringently limited. Unfortunately, complete shorting through the oxide does not always result. Partial oxide damage is often not detectable (except possibly by infrared techniques); consequently, this failure mode can be classified as time-dependent.

6.2.2.3 Corrosive Etching

Surface instability can result from the residue of corrosive contaminants. Integrated-circuit manufacturing techniques require the use of several extremely active etchants. Failure to completely remove these etchants can result in open aluminum conductors, as illustrated in Figure 6-5. This time-dependent failure mechanism is, of course, the result of inadequate process control.

FIGURE 6-5
OPEN CIRCUIT CAUSED BY CORROSION

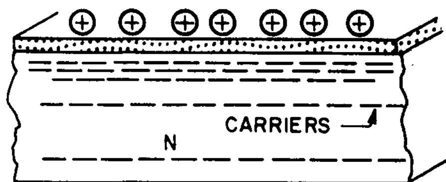
6.2.2.4 Insulation Layers

The formation of electrical insulation (dielectric) layers between the aluminum film and the silicon causes an interface at the window in the oxide. This is the result of

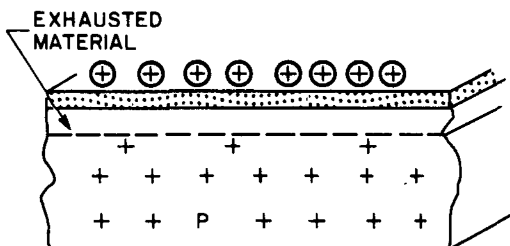
faulty oxide removal at the windows. Failures or incipient failures of this type are most rapidly detected after baking or operation. The dielectric layer can be broken through by microprobe pressure or voltage, temporarily healing the device; however, the unwanted insulation can be recreated by baking. Therefore, this failure mode is considered time-dependent.

6.2.2.5 Ionic Surface Effects

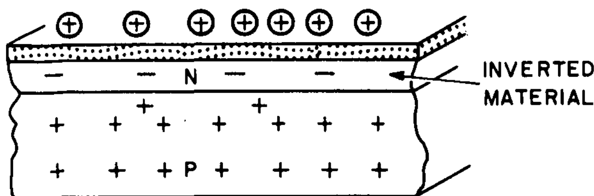
Surface-induced effects can take any of three forms (Figure 6-6): inversion or channeling where the surface has an excess of the opposite impurity (N on P or P on N); excessive, or accumulation of, P or N impurities on similarly doped material (P+ on P or N+ on N); and depletion of normal impurities (the opposite of accumulation).



(1) ACCUMULATION EFFECTS



(2) EXHAUSTION EFFECTS (DEPLETION)



(3) INVERSION EFFECTS (CHANNELING)

FIGURE 6-6
EXAMPLE OF IONIC SURFACE EFFECTS

These problems all result from P or N impurities (in the silicon-silicon dioxide interface or in the silicon-dioxide), that have translational or rotational freedom, which may become mobile, causing changes in the electrical characteristics. These failure mechanisms usually result in drift rather than catastrophic failures.

While channeling is the most important of the above-described failure mechanisms, any of the three may result from the "snow plow" effect that occurs during the growth of oxides on relatively high-resistivity silicon. This effect is based on the normal affinity of impurities for the liquid glass rather than the solid silicon. Most commonly the impurities are drawn into molten glass. (Glass has the basic properties of a liquid even at room temperature.)

These effects could be induced temporarily by an externally applied field and more or less permanently by a field that results from electrolysis, ion contamination, or ionizing

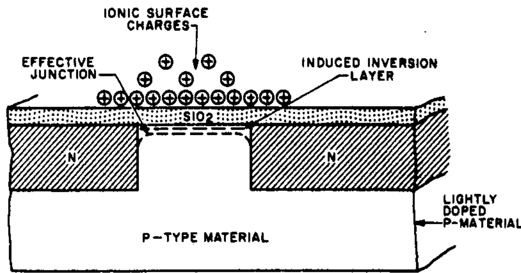


FIGURE 6-7

CHANNELING DUE TO IONIC SURFACE CHARGES

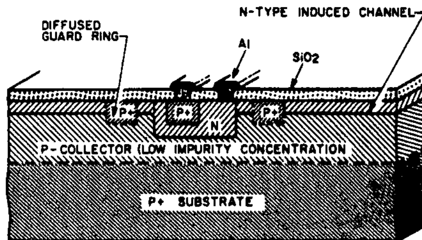


FIGURE 6-8

PNP TRANSISTOR WITH GUARD RING TO LIMIT CHANNELING EFFECTS

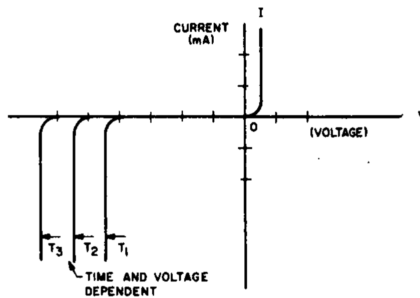


FIGURE 6-9

"WALKOUT" CHARACTERISTICS OF A P-N JUNCTION

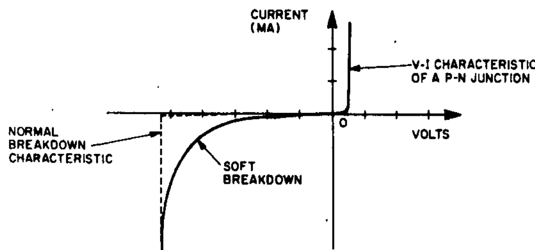


FIGURE 6-10

ILLUSTRATION OF A SOFT BREAKDOWN CHARACTERISTIC

radiation on the surface. The modification of the charge distribution pattern resulting from ionic contamination is illustrated in Figure 6-7. (A classic case of reversing this malfunction under appropriate voltage and moisture conditions was the well known correction of a Telstar malfunction.) "Guard ring" diffusion (Figure 6-8), used by several major integrated-circuit suppliers, limits the possible extent of channeling by immunizing the channel area, hence eliminating the shunting effects.

Depletion manifests itself as a low gain, while accumulation results in abnormally low breakdown voltage. Very thin inversion layers may be detected by their "walk-out" (Figure 6-9). The initial sweep of the breakdown characteristics on a curve tracer will be very low, the next higher, and in two or three sweeps the apparent breakdown voltage will have "walked" up to the level expected from the relative doping levels on either side of the junction.

These time-dependent failure mechanisms can be accelerated at elevated temperatures. Their effect can be minimized or eliminated through changes in surface-preparation processes.

6.2.2.6 Loss of Hermetic Integrity

Moisture in the package can cause shorts at surface scratches or in the surface passivation where the current densities in the conduction pattern are high (hot spots). Contamination on the top of the silicon can cause high leakage or soft breakdown characteristics (see Figure 6-10).

Sources of this contamination might be moisture; weld gasses; gas desorption from other parts; and mobile contaminants migrating to the junction area from within the sealed package, or from outside if the seal is broken.

6.2.2.7 Effects of Environmental Stresses

Ionic contamination, neutron radiation, and large local mechanical stresses can result in time-dependent failure. The first mechanism was discussed under Ionic Surface Effects; the latter mechanisms will be discussed under Bulk Defects.

6.2.3 Mechanical Imperfections

Mechanical imperfections, usually the result of workmanship errors, are a major source of failure in integrated circuits. Often an incipient failure resulting from one of these imperfections can be detected through careful inspection by the device manufacturer. Failures in this category result from improper scribing, improper handling of tools, bonding and lead dress problems, internal lead wire problems, unwanted residues, improper die attach, and other quality defects.

6.2.3.1 Improper Scribing

Three relatively minor problems can arise in the scribing process used to separate the individual dice from the parent wafer. The scribing can be misregistered, causing the crystal to be severed too closely to the circuit-lead bonds. The bond then overlaps the edge of the chip and may eventually short to the substrate.

Improper scribing can cause severe edge chipping of the oxide, exposing the substrate and permitting shorting (Figure 6-11). Chipping is a function of lattice orientation with respect to the scribing. Lattice orientation is, in turn, a function of the device characteristics. The problem can be circumvented if sufficient margin is left for expected chipping. Cracking may also be initiated by the scribing process (Figure 6-12). The cracks may be propagated by environmental factors, resulting in a time-dependent failure's appearing as an open.

6.2.3.2 Improper Handling of Tools

A careless smear from a tool removing a portion of the aluminum metalization (Figure 6-13) can create a situation similar to that of the insufficient metalization deposition, previously discussed. Cases in which smeared aluminum has bridged various circuit elements (Figure 6-14) have also been reported.

Scratches on the aluminum-metalization conduction pattern often caused opens. The scratch reduces the cross-section of the interconnection, resulting in electrical overheating and a subsequent open. If the scratch is not detected as

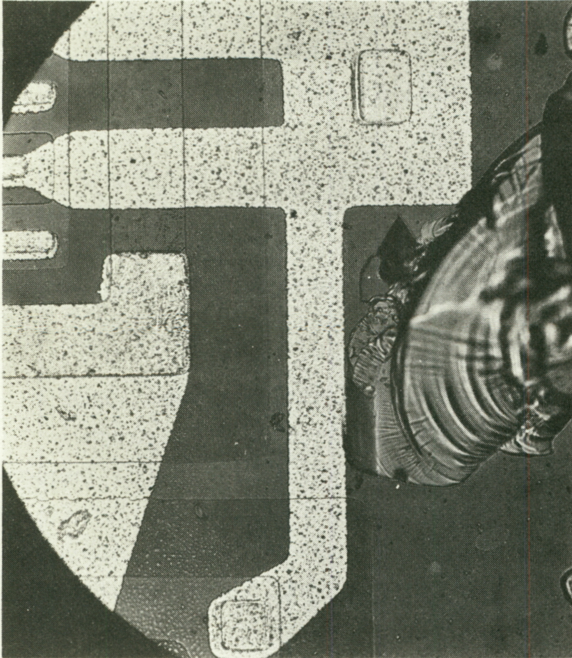


FIGURE 6-11

EXCESSIVE CHIPPING CAUSED BY
IMPROPER SCRIBING

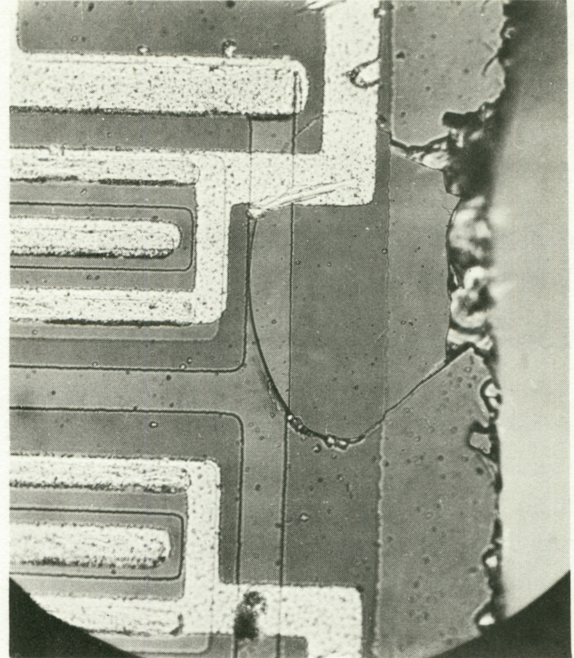


FIGURE 6-12

CRACKING CAUSED BY
IMPROPER SCRIBING

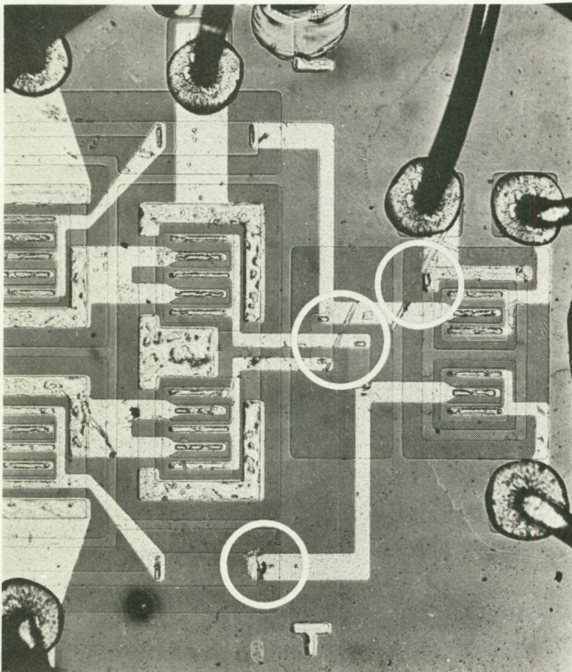


FIGURE 6-13

DAMAGED METALIZATION RESULTING
FROM HANDLING

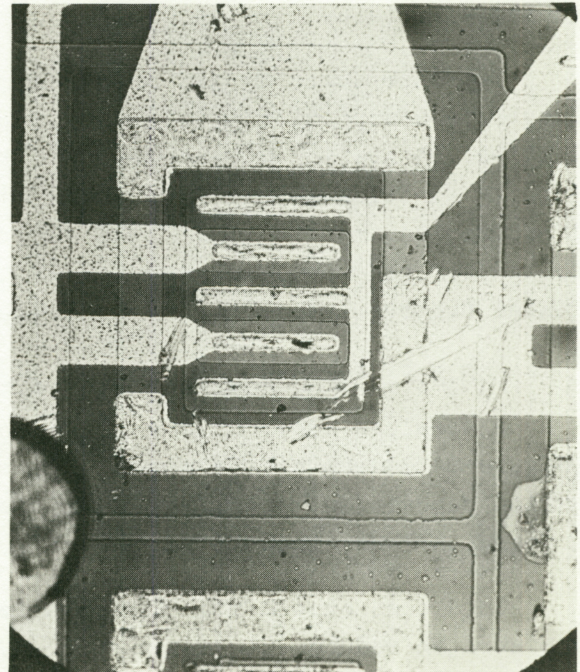


FIGURE 6-14

SHORT CIRCUIT CAUSED BY
SMEARED ALUMINUM

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an open before the circuit is used in a system, the circuit's tolerance to overstress pulses that it could otherwise withstand is markedly decreased; hence, the probability of a latent failure is significant.

A scratch on the chip surface can also cause a base-to-base type of shorting that would permit the integrated circuit to pass most operational tests as well as operate in a ring-oscillator circuit (series life test), and yet not perform properly in a computer circuit, where logic operations are required.

Because the ratio of the aluminized area to total crystal area is small in the case of the transistor, it is almost safe to handle individual transistor chips during their manufacture with well designed forceps. However, the high density of circuit elements on integrated circuits makes it clear that such liberties can no longer be tolerated. Still, a large proportion of failed circuits that are opened show evidence of some tool damage.

There is some tendency to overlook tool damage, apparently based on the feeling that the true problem units have opens or shorts that are identifiable at inspection and therefore are not installed in hardware. Experience indicates, however, that this assumption is over-simplified; often tool marks appear to be harmless, only to result in a failure in system operation. Figure 6-15 is a photograph of a device that has three tool marks on the deposited aluminum lead. At 1500X magnification (Figure 6-16) it is not easy to discern just where the path finally opened, but there are two points in the scuffed area where the path that remained after the accident is tenuous.

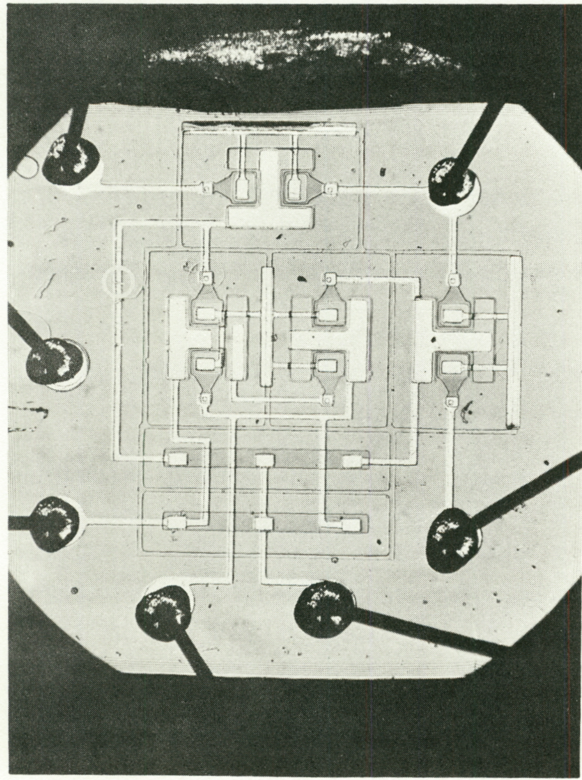

FIGURE 6-15

DAMAGED METALIZATION THAT MIGHT PASS TESTS

6.2.3.3 Bonding and Lead Dress Problems

Improper thermocompression bonding can induce cracks in the silicon substrate under nail head bonds, which may be further propagated by the application of thermal stress. Also, the die bonding operation can intercede to accelerate a crack that would otherwise have been harmless. This is especially true if the solder preform used to hold the substrate to its associated header is distributed unevenly or fails to wet well to either the substrate or the header.

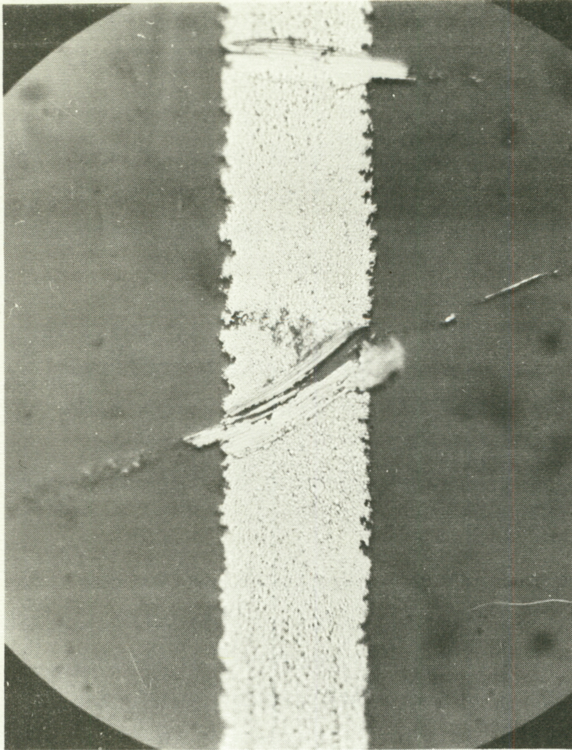

FIGURE 6-16

MAGNIFIED (1500X) VIEW OF AREA FROM FIGURE 6-15, SHOWING SEVERE DAMAGE

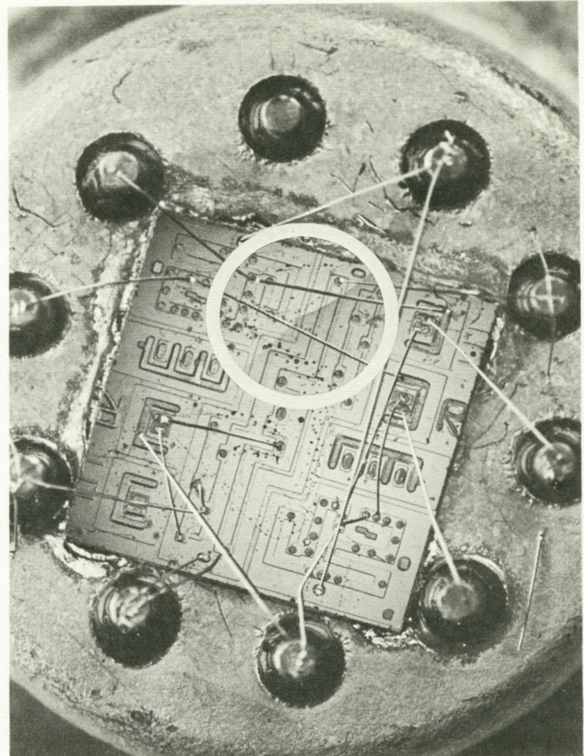

FIGURE 6-17

CRACKED CRYSTAL THAT PASSED ALL ACCEPTANCE TESTS

Figure 6-17 is a photograph of device that passed the vendor's functional test and the system manufacturers incoming inspection, but after some handling and a short operation in a laboratory experiment failed catastrophically because of a progressive crack.

In some situations it is necessary to fold a stitch-bonded lead back over itself, which may result in a severed lead or loosened bond.

In the case of ball bonds, it is very important to have the proper relationship between the ball size and the pad size as well as to apply the correct pressure to avoid cracking the passivation and causing a circuit short. Another type of failure is also attributed to ball bonds. The formation of oxide before the bond is made, or the presence of other types of contamination on the passivation layer, will cause an open circuit at the bond.

There have been several cases in which the pigtails of the ball-bond were shorted to the header.

Overheating during the thermocompression bonding process can cause embrittlement of the bonding wire (see Internal Lead-Wire Problems).

Some of the above-described problems can be classified as workmanship errors; others involve registration or the centering of leads in the glass holes of the header.

Poor pattern layout that requires bonding too close to the oxide edge on the surface of the chip causes failures. Shorts can occur when the gold overlaps the edge and goes across the SiO_2 to the silicon or shorts through the SiO_2, which tends to be thin near the edge of the substrate, thereby presenting a decreased dielectric. If a failure does not appear immediately, added strains on the device may rupture the dielectric.

6.2.3.4 Internal Lead-Wire Problems

Too little or too much tension on the internal leads can cause failure when the integrated circuit is operated in an environment of vibration (Figure 6-18). The probability of the leads shorting is increased when the package post is at a lower level than the surface of the chip, which is the case in many flat-packs. Excessively long lead wires may short to the lid, to the bottom of the package, to the surface of the chip, or to one another. Close proximity of leads results from either poor pattern layout or improper mounting in a package.

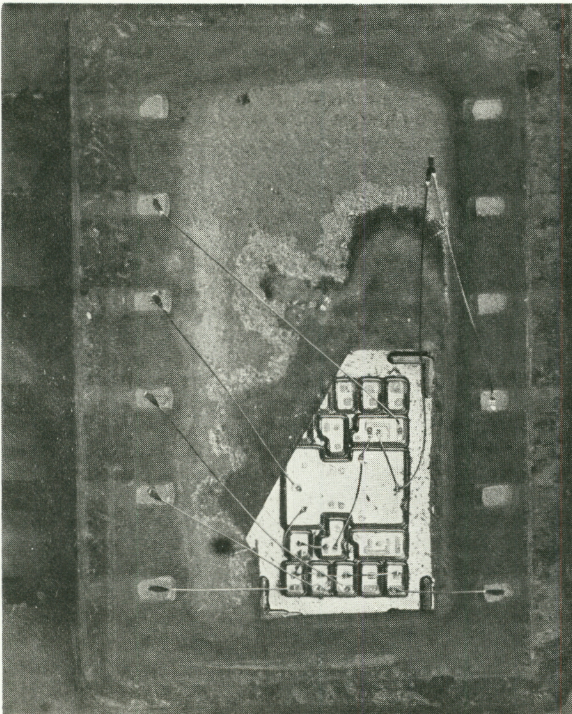

FIGURE 6-18

DAMAGE RESULTING FROM EXCESSIVE LEAD TENSION

Overheating during thermocompression bonding can cause embrittlement of the bonding wire adjacent to the bond. Subsequent mechanical or thermal stress thus can more readily cause such wires to break. Aluminum wire seems to be slightly more susceptible to this difficulty than gold. Several of the open-lead field failures have been attributed to this problem.

Opens can also occur in lead wires as the result of faulty handling, bending, and processing. Nicks and cuts may break during mechanical stressing. If bending causes extreme thinning of the wire or if the wire is constricted, it is susceptible to breaking open under minor stress. It is particularly noticeable at the post, where wedge bonds are made.

The above-described failure mechanisms can usually be accelerated and failures detected if the devices are subjected to the centrifuge test.

6.2.3.5 Unwanted Residues

Unwanted residues such as metallic fragments, etching residues, etc., can cause failures.

Loose materials and particles have been identified as the cause of failure in some integrated circuits. Broken pigtails and package tabs are two common examples of free conducting materials that have caused intermittent shorts. The X-ray of Figure 6-19 shows a relatively large foreign object inside the flat-pack of an integrated circuit. A photograph of the device (Figure 6-20) made after the package was opened shows the object to be a scrap of metal apparently chipped or torn from an external tab connector. Nonconducting material can cause mechanical damage.

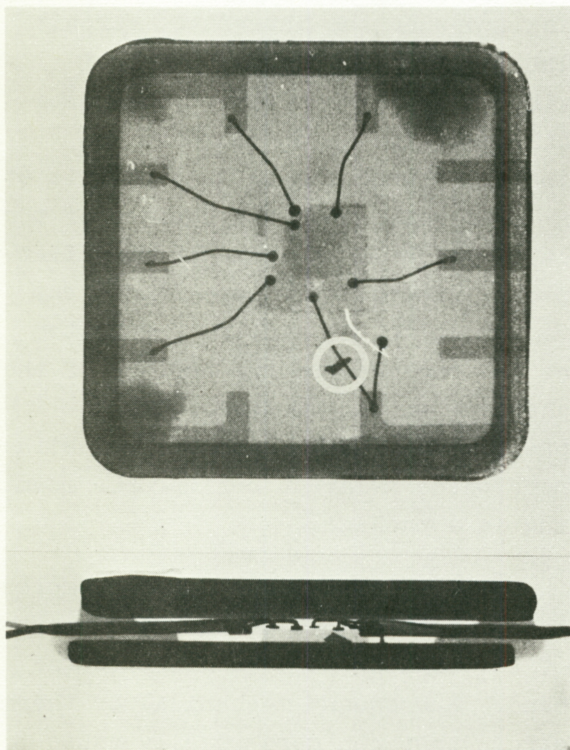

FIGURE 6-19

X-RAY VIEWS SHOWING LARGE FOREIGN OBJECT IN PACKAGE

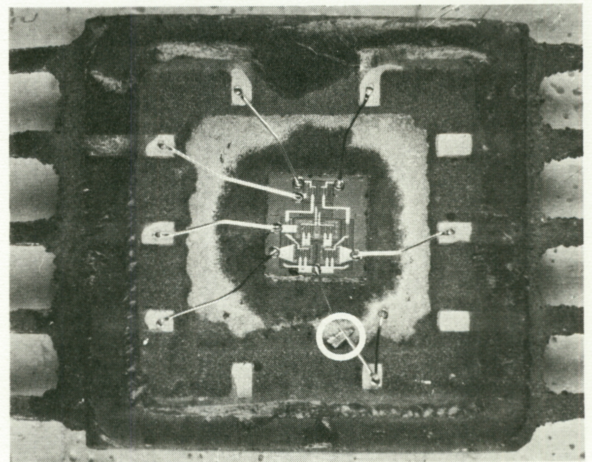

FIGURE 6-20

PHOTOGRAPH OF CIRCUIT FROM FIGURE 6-19 AFTER OPENING

An impurity in the substrate can create a small diode. If the diode is within the area of an active circuit element, the circuit fails.

It might logically be assumed that since integrated circuits are relatively expensive and require great care in production, adequate measures are taken to protect them from penetration by impurities. Yet it is not uncommon to see gold

and glass particles adhering to the substrate surfaces, and larger items are occasionally found.

6.2.3.6 Improper Die Attach

Strains set up during die attach, particularly when a silicon-gold eutectic has not been reached, may result in cracking of the silicon die. Excessive pressure on the substrate side of a flat pack, or thermal propagation of minute surface cracks of a silicon die mounted in any package, can induce total cleavage.

6.2.3.7 Electrical Overstressing and Improper Marking

Electrical overstressing by the test equipment and improper marking of the completed package have also caused some difficulties, in spite of numerous 100% inspections.

6.2.3.8 Other Mechanical Problems

Other mechanical problems, such as misregistration (poorly defined geometry, creating hot spots), masking flaws, packaging solder residue, package leakage, insufficient lead plating, and photolithographic-process deviations also cause failures of integrated circuits.

6.2.4 Bulk Defects

Bulk defects are responsible for a small percentage of the operational failures of integrated circuits in systems, and will be treated only briefly here. Failure mechanisms that fall in this category include dislocations (crystal lattice anomalies), impurity diffusions and precipitations, and resistivity gradients resulting from mechanical, nuclear, or thermal stresses. These defects can lead to diffusion spikes, which in turn cause hot spots, voltage breakdown, and other deviations from the desired electrical characteristics. Such defects are usually induced in the crystal-preparation process.

The steep concentration gradients found in epitaxial diffusion result in crystal lattice strain. This strain is subsequently released by the formation of dislocation structures that contain edge components perpendicular to the concentration gradient. The chip is structurally weaker at the dislocation fault plane; thus bulk failure can be triggered by mechanical stress.

Deviations in epitaxial growth, resulting in impurity diffusion, are another source of bulk failures. Impurity diffusion is more likely along edge dislocations, particularly along the arrays of edge dislocations that form small-angle grain boundaries. The precipitation of impurities at the resulting crystal-lattice-orientation fault planes is believed to lower the reverse breakdown voltage in epitaxial devices.

Resistivity gradients caused by a heat differential between the center and the outer surface of the chip can result in secondary breakdown.

Large local stresses can cause changes in resistivity and, hence, in electrical characteristics. These local stresses can be caused by mechanical shock or vibration, which would generally result in microphonics. The stress levels usually would have to be so high as to be destructive in other areas (seals, bonds, etc.). Sufficiently large stress concentrations can crack the die.

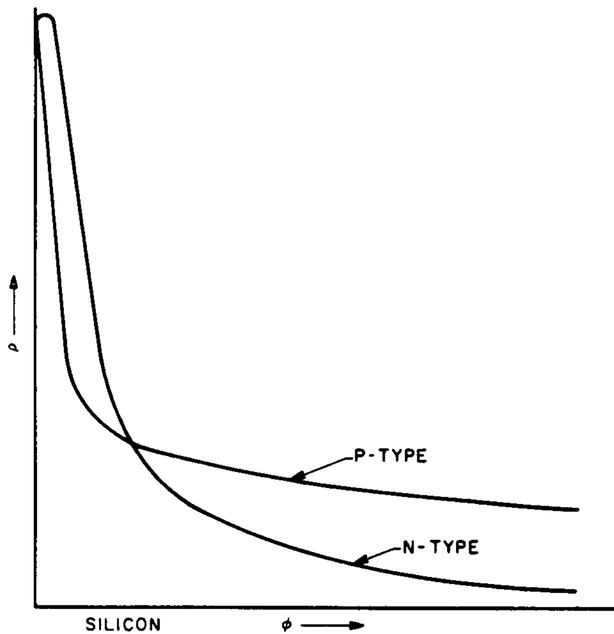

FIGURE 6-21
CHANGE IN SILICON RESISTIVITY VS. NUCLEAR RADIATION FLUX

Permanent local stress concentrations can be induced by neutron bombardment. Changes in resistivity (Figure 6-21) as a function of the intensity and amount of nuclear flux (NVT) have been observed. Figure 6-22 indicates the changes in crystal structural alignment from this high-energy collision. Integrated circuits, because of their relatively thin active region, are less sensitive to this form of damage than most discrete transistors (except the very-high-frequency types).

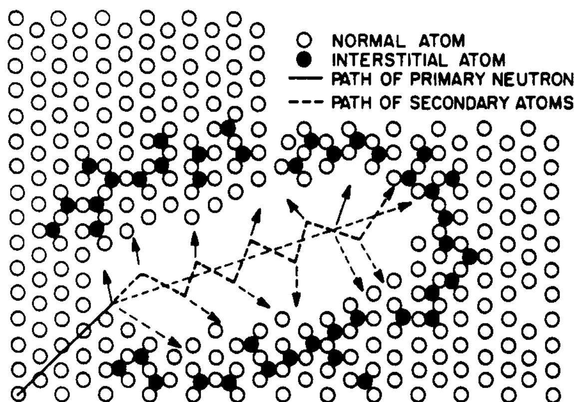

FIGURE 6-22
DEFECT CREATED IN SILICON STRUCTURE BY HIGH-ENERGY NEUTRON

Cracks in the bulk silicon and silicon oxide frequently result from thermal shock during processing (cooling very rapidly from about 1300°C to room temperature). Failures resulting from this source are usually eliminated by normal quality control procedures. Occasionally these cracks may either propagate to critical regions or result in breaks from additional shock or cycling.

Secondary breakdown that leads to localized alloying or diffusion in semiconductor junctions depends critically on collector voltage and mode of operation. In some transistor structures, the breakdown current

does not flow through the hot-spot regions, indicating that a different mechanism, associated with the presence of local defects, exists and manifests itself in a "soft" collector-junction characteristic.

The failure mode usually associated with bulk defects is bulk shorting, which results from secondary breakdown or uncontrolled PNPN switching when the circuit design is such as to allow floating internal junctions.

Also, there are punch-through effects between collector and emitter if the base region is narrow. In this case the collector-depletion region extends to the emitter at high collector voltages. This occurs most frequently in high-frequency transistors, since these devices have a minimum distance between emitter and collector to reduce recombination effects. This condition also occurs in transistors that have high base resistivity ($>300\Omega/\square$) and relatively narrow base regions.

Carriers entering and leaving a region through floating junctions are subject to multiplication within the junction. This effect lowers the breakdown level of the junction and leads to negative-resistance regions. This action is enhanced at higher currents and is evidenced in the isolation junctions of integrated circuits.

6.3 Sources of Quantitative Reliability Data on Integrated Circuits

Reliability data for integrated circuits are available from two broad categories of observations: device test and system operation. Within the device-test category are operating life tests, accelerated life tests, step-stress tests, environmental tests, and screening tests -- all performed by the device manufacturer -- as well as tests that are performed by the system manufacturer. Within the system operation category, reliability data are available from observations of prototype test and system demonstration by the system manufacturer and from observations of system operation by the user.

6.3.1 Device Testing

The following paragraphs present general descriptions of tests performed at the device level from which reliability data can be derived. Before such data are applied to a specific problem, it is essential that the engineer be familiar with the tests from which the data were drawn. Since an "ideal" source of reliability data does not exist, it is important to recognize the implications of data that result from controlled testing. Device tests other than those discussed below are used in certain situations; however, most of today's reliability data are drawn from operating-life, accelerated, step-stress, environmental, and screening tests.

6.3.1.1 Operating-Life Tests

Operating-life tests are performed on devices primarily to ascertain the probable (absolute) reliability level (MTBF and failure rate) of the lot of devices that the devices on test represent. A secondary objective is to generate failure-mode information. One of two stress conditions is generally used:

(1) Normal electrical conditions and 25°C free air ambient

(2) Maximum rated electrical and thermal (85°C or 125°C) conditions. In some instances, power is applied but switching operations are not performed.

Operating-life tests can be divided into three categories: static, parallel switching, and series switching. Of the three, most integrated-circuit manufacturers use the series-switching test because it enables them to accumulate the greatest number of a-c test hours (although it can be expected to result in lower observed failure rates than a parallel-switching test would show).

6.3.1.2 Static Bias Life Tests

The static life test is a d-c test similar to transistor life tests. D-C voltages are applied to the circuit and maintained. A test of this type is suitable for bias drivers and similar circuits. Its basic advantage is that it requires a minimum of connections. Its disadvantage is that it fails to stress the circuit adequately in that no siginals are applied to the network. Because of this, the results of static life tests are not a good indicator of the reliability of the circuits under test.

6.3.1.3 Parallel-Switching Life Tests

Each driver is given an independent switching signal (usually 60 cps) when a network is subjected to a parallel-switching life test, although the circuits have a common bias. This type of life test provides the best indication of circuit reliability because the devices operate independently and are adequately stressed. Because this test requires more connections than the static and series life tests and requires external signal sources, the number of circuits that can be tested simultaneously is limited because of the higher costs involved. Therefore, the quantity of reliability data available for analysis from parallel testing is smaller than desired.

6.3.1.4 Series-Switching Life Test

In a series-switching life test, each circuit is connected in series; i.e., the output of one circuit drives the input of the following circuit, etc. The frequency achieved (usually in the megacycle range) depends on the propagation

delays of the circuits. The advantage of such a test, often called a ring-counter or ring-oscillator test, is one of cost and time. Because of the smaller number of connections and the requirement for only a single signal source, many circuits can be tested simultaneously. For this reason, by far the largest quantity of reliability life-test data available today is based on this type of test. Its major disadvantage is that the performance of each circuit is dependent on the performance of each preceding and succeeding circuit. Critics of this type of test claim that the test does not stress the devices adequately, while proponents argue that the environment is similar to that experienced by devices in most systems.

Many of the life tests are conducted for only 1000 hours, although in some cases some of the specimens in the short-term tests are left on test for a long-term reliability analysis. Consideration is often given to the relationship of junction temperature with the combined effects of ambient temperature and dissipated power. These factors are then controlled to maintain a given junction temperature (usually the maximum rated).

6.3.1.5 Accelerated Life Tests

Accelerated life tests accelerate the failure mechanisms of a circuit in order to reduce the number of samples and test time required to obtain useful reliability data. Usually the acceleration factor is a thermal or electrical stress greater than that expected for the circuit in system operation. A detailed knowledge of the device failure mechanisms is necessary before the test is designed. If an accelerated life test introduces new failure mechanisms or does not accelerate all failure mechanisms, the test is not valid for predicting reliability at lower stress levels.

Integrated-circuit manufacturers usually run accelerated life tests only at elevated temperatures. This philosophy is carried over from the transistor technology: that is, the majority of failure modes of a semiconductor device are influenced by temperature. Storage tests are the most economical accelerated tests since they do not require elaborate test set-ups. Unfortunately, however, several known failure mechanisms are not significantly accelerated without the presence of electrical stimuli.

Accelerated life tests are used for the following:

(1) To predict failure rates at lower stresses

(2) To compare relative failure rates

(3) To assess potential problem areas

When circuit manufacturers have accelerated tests performed at three or more stress levels, failure rates are generally plotted on a logarithmic scale against stress (usually temperature, °C) on an absolute scale. The curve is then extrapolated to lower stress levels to estimate the failure rate at any lower stress

level. Using the acceleration factors to predict failure rates, however, opens the door to many uncertainties concerning the validity of the predicted rate; a small error in calculation of the true failure rate, or incomplete knowledge of the effect of other stresses, can cause significant errors in the estimates. For this and similar reasons, failure rates estimated from accelerated-test results are not universally accepted.

The possible errors introduced by the uncertainties discussed above can be minimized if the results of an accelerated test on a new circuit can be compared with those of an identical test on a circuit with a known reliability level. For this reason, accelerated life tests can be beneficial in determining the relative reliability of a new design or process when a quick reaction time is required. Accelerated life tests can also provide a continual indication of the quality of a given production line's output.

6.3.1.6 Step-Stress Tests

A step stress test is a reliability test in which a sample of a population is subjected to discrete stress levels of successively increasing severity until all or nearly all units fail. After the device is subjected to each discrete stress level, it is generally returned to its normal operating stress level. Its critical parameters are then measured and the number of rejects determined. The purpose of the step-stress-to-failure test is generally one of the following:

(1) To determine the safety factor inherent in the design with respect to a given stress

(2) To accelerate failure mechanisms or uncover failure modes in devices

(3) To predict failure rates at lower stress levels in a shorter calendar period and with fewer samples than required by operational life testing

(4) To compare the relative reliability of two or more integrated-circuit designs, manufacturing processes, etc.

The distribution of failures with respect to the applied stress can be plotted and used to indicate the strength of a particular device with respect to a given stress. The probability of failure with respect to this given stress can be estimated by comparison of the applied stress with the anticipated or actual operating stress.

The causes of failure can be reduced or eliminated if design and manufacturing procedures are improved through the use of information obtained by accelerating the failure mechanisms so that the cause of failure can be identified. The cumulative percentage of failures is plotted on a Gaussian probability scale and the stress level on an absolute scale. If the line that joins the points has a sharp discontinuity, it can be assumed that a new failure mechanism has been introduced

at the stress level indicated by the point of discontinuity. Failure analysis is then performed to determine failure modes. Failure mode information can be used to take corrective action to eliminate the cause of failure. Another step-stress test can then be run to measure improvements.

Assumptions are made regarding failure distributions and acceleration factors. Failure rates at lower temperatures are estimated from extrapolations of the step-stress-tests data. These estimations can be criticized for the same reasons for which estimates based on accelerated life tests are criticized. For the reasons given in the discussion of accelerated life testing, comparative failure rates can be more useful than absolute failure rates.

As is the case with accelerated life testing, temperature is the most common stress used for step-stressing of integrated circuits, although electrical stresses have been used.

6.3.1.7 Environmental Tests

Environmental tests are used to determine the capability of an integrated circuit to withstand certain operational stresses. These tests usually follow MIL-STD-19500 in accordance with procedures in MIL-STD-750 and MIL-STD-202. Some manufacturers have run tests exceeding the requirements of these military documents and have also conducted special environmental tests dictated by specific customer requirements, e.g., radiation tests.

6.3.1.8 Preconditioning and Screening Tests

Preconditioning and screening tests are tests performed on the integrated circuits prior to their installation in an operational system in order to identify potential failures. Screening tests usually do not include inspections. Particular screening tests and inspections are discussed in Chapter 5. Screening tests can be performed by the integrated-circuit vendor or the system manufacturer, or by both.

Reliability data generated by vendors' device tests are readily available to interested parties; similar data generated by system manufacturers are much more difficult to obtain. Generally, the latter are preferred since they can be assumed to be less biased. Vendor data may be very useful in assessing a circuit's potential reliability, but analyses from such data must be carefully scrutinized since they can easily be misinterpreted. The wise customer will request sufficient data to perform an independent analysis.

6.3.2 Reliability Data Generated from System Operation

Integrated-circuit reliability data are generated because a system manufacturer or user wants to know how reliable a proposed system using these circuits will be; what can be done to make the system more reliable, and at what cost; what system

failure modes can be expected, and their frequency; and what the spares-provisioning and maintenance requirements will be. The primary objective, then, is to predict how the integrated circuit will perform in the system environment. If available to the analyst, the data most relevant to the system studies are data drawn from experience with similar systems.

While a significant quantity of data on microelectronic system operation has been accumulated, it is not available to the general technical public in sufficiently detailed form. The data are often related to classified or proprietary programs and are thus more difficult to obtain than device data. Nevertheless, system and equipment engineers using integrated circuits should make every effort to obtain this type of information.

Reliability data based on system operation are of greater value than those based on device tests because the observed results may reflect system environment factors not reflected in device testing. The most important of these factors may be the failures that are not the direct result of a device failure but that can be attributed to the fact that a device is being used. For example, an interconnection failure between the device package and the circuit board, or within the board, would not be observed or, if observed, certainly not counted during a device test. Other factors include the following:

(1) The failures resulting from the interdependence of device operation, such as drift, noise, etc.

(2) The design problems associated with the implementation of the microelectronics technology

(3) The actual physical environment (rarely reflected exactly in device testing)

(4) The effect of failures, drift, etc., of other circuits or subsystems

(5) The effects of maintenance and built-in test equipment

(6) The system characteristics resulting from the use of particular logic types

Because the number of sources of system data is a function of the number of systems using microelectronics, there are considerably more such sources than there are sources of device test data, although the quantity of device operating hours from any given system source can be expected to be modest. Because of this and the problem of accessibility to the data, the engineer seeking system data usually will have to limit the number of data sources he interrogates. The following should be considered in the selection of systems as potential sources of integrated-circuit reliability data to be used in system development:

(1) Functional similarity

(2) Environmental similarity

(3) Common logic

(4) Packaging commonality

(5) Interconnection similarity

Microelectronics reliability data can be obtained from observations of field operation, demonstration, and prototype test.

6.3.2.1 Field Operation

Reliability data acquired in an analysis of field operations should theoretically be the most useful to the reliability engineer. Because the devices are operating in a "real" system, exposed to the actual physical and maintenance environment, the data include many of the factors that other data sources do not.

Practically, however, these data may have some drawbacks, including the following:

(1) Until more microelectronic systems become operational, there is insufficient operating time to draw confident conclusions in many areas.

(2) Failure reporting is rarely complete. This problem is compounded by retrofits, where the total operating time is often not known. Incomplete failure reporting or the absence of any reporting is common, and spaceborne microelectronic systems are particularly difficult because telemetry cannot monitor every circuit and cannot determine the failure mechanisms.

(3) Maintenance personnel are still in the early part of a learning curve. This lack of experience significantly contributes to the failure rate when a new technology is introduced.

(4) Many new systems are still not debugged; failures may reflect lack of design experience, which would not normally be evident in follow-on systems.

6.3.2.2 System Demonstration

Observations of system demonstration minimize the effects of the first three factors listed above. To date, a significant amount of system demonstration time has been accumulated. However, most of the pertinent data are not centrally located; they are in the possession of the manufacturers who performed the demonstrations. The biggest drawback to these data is that they do not reflect the operational environment. Some systems do undergo testing in a simulated environment, but generally the percentage of operating hours in environmental test is low.

6.3.2.3 Prototype Testing

Tests of prototype systems can also provide a significant amount of system time from which reliability knowledge can be drawn. The advantages and disadvantages of data drawn from this type of operation are similar to those mentioned above, with the additional complication of an unproven design and system fabrication procedure.

6.4 Reliability Data

Reliability information for microelectronic devices continues to be scarce; however, sufficient data are available to prove that these devices are indeed highly reliable and may well live up to the early predictions that appeared so optimistic when made.

Tables 6-4, 6-5, and 6-6 show the results of a reliability analysis of integrated circuits operating at two different temperatures.

Tables 6-7 summarizes a vendor reliability evaluation conducted by the MIT Instrumentation Laboratory for Apollo Program devices. This example has the advantage that it illustrates a decreasing failure rate within a particular sample, rather than with a tabulation of data from a number of different samples. The decrease in failure incidence as the evaluation progresses is evident for each of the three vendor samples. It is also significant that each manufacturer maintained his relative position for quality at each of the three evaluation stages.

While reliability data are still not plentiful, it can be reasonably argued that additional data of the type appearing in Tables 6-4, 6-5, and 6-6 would be of little value without further analysis. These data show the usual wide spread in failure rates (over three orders of magnitude) that results when samples of different quality are subjected to different test conditions and different failure criteria.

No effort has been made to combine the available reliability data to arrive at an average failure rate (or any other single measure of reliability). As discussed earlier in this chapter, there is no technical justification for combining these unrelated data, even though a single figure for predictions would be extremely valuable. It should be kept in mind that the restraints for combining data on devices from a single manufacturer, tested under identical conditions, are severe for valid statistical results. It is usually accepted that if a time period of several weeks passes between the manufacture of two groups of the same device type, it should not be assumed (without further evidence) that test data on the groups are statistically combinable even though the manufacturer may have had a continuous production line operating without any known process changes.

Briefly, data such as those in Tables 6-4, 6-5, and 6-6 are useful only for broad generalizations, and an expansion of the number of samples in these tables would have little utility. These data represent failure rates that have been obtained on specific samples; the reader is reminded that the source selected and specifications enforced for a particular item will determine the reliability for that particular item.

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TABLE 6-4

INTEGRATED-CIRCUIT OPERATING TESTS PERFORMED BY EQUIPMENT MANUFACTURERS/USERS

Level of Test	Network Test Hours	Failures	Failure Rate* (Multiply by 10^{-6})	Date	Remarks
System	13,000	0	77	5/64	Fairchild and Amelco circuits for AFCS
System	170,000	0	5.9	6/64	In-flight testing of ECM receiver, data link, LORAN C
Device	593,000	0	1.7	6/65	Fairchild DTL for LOS
System	600,000	0	1.7	6/65	Two failures caused by error in testing
ECM	800,000	1	1.2	6/65	Failure cause not known
Radar Indicator	1,000,000	2	2	7/66	
System	2,000,000	0	0.5	5/65	Time-Code Generating System -- Fairchild customer reporting
Device/ System	2,325,000	0	0.43	5/64	For advanced Minuteman
Device	2,850,000	0	0.35	5/65	Fairchild devices tested at 125°C for Viggen Fighter
Device/ System	3,408,000	1	0.29	9/64	T. I. Device
System	3,500,000	0	0.29	6/65	T. I. Series 51 for "EPIC" GCE on BOMARC prototype
Computer	5,200,000	0	0.19	5/65	Fairchild devices
LORAN C	5,250,000	0	0.19	6/64	LORAN-C and converter
ASA-27	6,000,000	36**	6	6/66	Actual flight results
Computer	6,470,460	0	0.15	6/65	Fairchild devices in computer
Computer	13,000,000	0	.007	12/63	One failure reported on MAGIC prototype due to error -- Fairchild devices
Computer	20,000,000	7	0.35	6/65	Signetics devices

*Failure rates are estimated by dividing the number of failures by the test hours (one failure is assumed where none are reported).

**Removals only are listed - failures were not verified.

TABLE 6-5

INTEGRATED-CIRCUIT OPERATING TESTS AT 125°C
PERFORMED BY DEVICE MANUFACTURERS

Test Agency	Network Test Hours	Failures	Failure Rate* (Multiply by 10^{-6})	Date	Remarks
Motorola	35,000	0	29	6/65	Custom circuit at maximum rating
Philco	148,000	0	6.8	5/65	TTL on ring counter
Sylvania	146,638	0	6.8	5/65	Parallel at 150°C
Motorola	165,000	0	6.1	1/65	Static D.C. (3-input gate) MECL
	231,074	1	4.3	1/65	Ring counter (3-input gate) MECL
Fairchild	240,672	0	4.1	6/64	Milliwatt logic on ring counter
	246,105	3	12	1/65	Parallel 60 cps (3-input gate) MECL
Raytheon	396,000	2	5.77	6/66	No special screening prior to life test
Siliconix	446,378	4	9	8/64	Five failures observed on ring counter
Philco	663,000	0	1.5	5/65	Epitaxial milliwatt logic on ring counter
Texas Instruments	1,183,000	9	7.6	9/64	Eleven failures reported
Sylvania	1,423,000	1	0.7	5/65	Ring counter
General Microelectronics	2,000,000	1	0.50	6/65	MOS Devices
Amelco	2,189,250	0	0.457	4/66	DCTL on ring counter
General Microelectronics	4,378,000	1	0.23	6/65	Ring Counter
Signetics	6,535,576	4	0.61	4/66	
Motorola	8,611,992	4	0.465	5/66	Ring counter DTL
Philco	13,529,000	1	0.074	5/65	Epitaxial logic on ring counter
Fairchild	37,500,000	8	0.21	4/64	Non-epitaxial logic on ring counter
Fairchild	38,338,644	0	0.026	5/65	Epitaxial logic on ring counter

*Failure rates are estimated by dividing the number of failures by the test hours (one failure is assumed when none are reported).

TABLE 6-6

INTEGRATED-CIRCUIT OPERATING TESTS AT 25°C
PERFORMED BY DEVICE MANUFACTURERS

Test Agency	Level of Test	Network Test Hours	Failures	Failure Rate* (Multiply by 10^{-6})	Date	Remarks
Sylvania	Device	11,945	0	84	6/64	Static D. C. at 25°C
Norden	Device	62,000	0	16	5/65	Analog at 25°C (Some multi-chip)
Signetics	Device	75,000	0	13	10/64	At -55°C
	Subsystem	84,000	0	12	10/64	Ripple Counter at 25°C
Philco	Device	88,000	0	11	5/65	Milliwatt logic on ring counter at 25°C
	Device	140,000	0	7.1	8/65	Micrologic on ring counter at 25°C
Signetics	Subsystem	220,100	0	4.5	10/64	Pre-production ring counter at 25°C
Motorola	Device	767,625	0	1.3	1/65	Maximum rating at 25°C
Signetics	Subsystem	1,419,000	0	0.7	10/64	Die sort tester at 25°C
Motorola	Device	1,613,429	0	0.62	1/65	Ring counter at 25°C
Signetics	Subsystem	2,010,300	0	0.5	10/64	Pre-production 4-stage shifting counter at 25°C
Signetics	Device	2,358,300	0	0.42	10/64	At 25°C
Signetics	Subsystem	3,229,200	0	0.31	10/64	Automatic Final tester at 25°C
Westinghouse		4,030,000	2	0.5	6/64	At 25°C

*Failure rates are estimated by dividing the number of failures by the test hours (one failure is assumed where none are reported).

TABLE 6-7

SUMMARY OF VENDOR RELIABILITY EVALUATION FOR THE APOLLO PROGRAM

Vendor	Initial Qualification (% Failures)	Screen and Burn-In (% Failures) Total**	Post Stress†	Failure Rates at Use Conditions (90% Confidence)
A	5	1.8	0.3	$0.005\%/10^3$ hours (0 Failures) (See Note)
B	26	3.8	1.7	$0.3\%/10^3$ Hours (2 Failures)
C	58	5.0	2.5	$1.8\%/10^3$ Hours (26 Failures)

* Source: "The Application of Failure Analysis In Procuring and Screening of Integrated Circuits", by L D. Hanley, et al; MIT Instrumentation Laboratory, October, 1965, presented at the Physics of Failure in Electronics Symposium, Chicago, Ill., November 1965.

** Total: All electrical and mechanical failures.

† Electrical failures after incoming electrical tests.

Note: As of 30 August 1965, Vendor A had exhibited a failure rate of $0.0018\%/10^3$ hours at 90% confidence with no operational failures.

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MANUFACTURER AND DEVICE INFORMATION

SEVEN

The primary purpose of this chapter is to present the major characteristics of integrated circuits available from stock. Section 7.1 is an index of device manufacturers. Section 7.2 catalogs the performance characteristics of digital and linear circuits. Outline drawings of packages are given, in addition to schematics for all circuits.

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7.1 Index of Manufacturers

Companies engaged in manufacturing standard microelectronic devices are listed in Table 7-1 along with basic information on the nature of their devices.

TABLE 7-1

INDEX OF MANUFACTURERS OF MICROELECTRONIC DEVICES

Manufacturer's Name and Address	Code in Devices Catalog	Basic Logic	Technology*
Alpha Microelectronics Co., Inc. 10501 Rhode Island Avenue Beltsville, Maryland			M
Amelco, Inc. Semiconductor Division 1300 Terra Bella Avenue Mountain View, California	AMEL	DCTL RTL	F
Burroughs Corporation Plainfield, New Jersey			M
Corning Electronics 3900 Electronics Drive Raleigh, North Carolina	CORN	DTL	D
CTS Research, Inc. 2101 Cumberland Avenue West Lafayette, Indiana			O
Fairchild Semiconductor 545 Whisman Road Mountain View, California	FSC	RTL TTL DTL	A
General Electric Semiconductor Products Dept. Electronics Park Syracuse 1, New York	GESP	ECL	A F G
General Electric Light Military Electronics Dept. Utica, New York	GELM		N
General Instruments Corporation 600 W. John Street Hicksville, New York	GI	DTL	H K
General Micro-electronics, Inc. 2920 San Ysidro Way Santa Clara, California	GME	RTL TTL	A F K
Halex 139 Maryland Street El Segundo, California			M
Hoffman Electronics Corporation Semiconductor Division El Monte, California	HOFF	DTL	B
Hughes Aircraft Company Semiconductor Division Newport Beach, California	HUGH	TTL	M
Intellux, Inc. P. O. Box 929 Santa Barbara, California	INTX	TRL	L
Mepco, Inc. 35 Abbett Avenue Morristown, New Jersey	MEPC	DTL	E
Motorola Semiconductors Box 955 Phoenix, Arizona	MOTA	DTL ECL	A F J
National Semiconductor Corp. Danbury, Connecticut	NSC	RTL	A M
Norden Division of United Aircraft Norwalk, Connecticut	NORD	RTL	R F
Philco Lansdale Division Lansdale, Pennsylvania	PHIL	RTL	A J
Radiation, Inc. Melbourne, Florida	RAD	DTL	C J
Radio Corporation of America Harrison, New Jersey	RCA	ECL DTL	A
Raytheon Semiconductor Division 350 Ellis Street Mountain View, California	RAY	DTL	A
Signetic Corporation 680 West Maude Avenue Sunnyvale, California	SIGN	TTL DTL	A
Siliconix, Inc. 1140 W. Evelyn Avenue Sunnyvale, California	SILX	DTL Mod.DTL TTL	A
Sperry Semiconductor Norwalk, Connecticut, 06852	SPER	RTL	B
Sprague Electric Company North Adams, Massachusetts	SPRG	RCTL	F M
Stewart-Warner Microcircuits, Inc. 730 East Evelyn Avenue Sunnyvale, California	SW	DTL TTL ECL	A
Sylvania Electric Products, Inc. Semiconductor Division Woburn, Massachusetts	SYL	TTL	B
Texas Instruments, Incorporated Semiconductor Components Div. P. O. Box 5012 Dallas 22, Texas	TI	RCTL Mod. DTL TTL	A F J
Transitron Electronic Corp. Wakefield, Massachusetts	TRAN	TTL	B
Varo, Incorporated 2201 Walnut Street Garland, Texas	VARO	DTL TRL	E
Westinghouse Electric Corp. Molecular Electronics Division P. O. Box 1836, Baltimore Elkridge, Maryland	WMED	ECL DTL	A J

*Indicates technology of devices listed in devices catalog only and, hence, does not necessarily indicate total capability. See Table 7-4 for explanation of code.

7.2 Catalog of Devices

7.2.1 General

The catalog of microelectronic devices is restricted to those devices which are integral units and which cannot be broken down into smaller segments without destruction of the entire unit. The catalog is further restricted, in general, to those devices in which all active and passive elements necessary to a fully-operable circuit are included and intraconnected in one package. A few of the devices tabulated offer questionable compliance with these requirements; however, these exceptions are readily identifiable in their schematic diagrams (see Section 7.2.5).

It cannot be stressed too strongly that this catalog must be considered as an initial reference and used accordingly. Detailed appraisal of a circuit must include reference to the manufacturer's data sheet or consultation with the manufacturer. In the extraction of data for the catalog from the individual manufacturers' data sheets, a number of factors made it impossible to provide a standard tabulation with values that were exactly comparable from one circuit to another. These factors included the variety of formats used, the variety of information presented, the variety of words used to describe the same item, the variety of definitions applied to the same words, and the variety of testing conditions. The reported characteristics and the manner of their presentation, however, have been restricted and selected so that the values listed from circuit to circuit are reasonably comparable. The user is urged to read carefully Section 7.2.2 entitled "Notes Concerning Column Headings" in order to avoid misunderstandings from some of the arbitrary definitions that were necessary to maintain a reasonable degree of uniformity in the catalog.

The catalog has been developed with separate formats for linear circuits and digital circuits. The only essential difference between the two formats is the column headings for electrical characteristics.

7.2.2 Notes Concerning Column Headings

7.2.2.1 Digital and Linear Formats

CIRCUIT DESCRIPTION - Devices are listed alphabetically according to circuit function. However, descriptive titles for circuit functions are by no means standard throughout the electronics industry. For example, one manufacturer's

"Driver" is another manufacturer's "Buffer", and yet another manufacturer's "Inverter". In the device catalog, all like functions have been assigned the same descriptive title -- regardless of the manufacturer's terminology -- according to the following criteria:

(1) All logic functions are described in the positive logic mode. For example, a function is described as an "AND" gate if all inputs are required to be at the high level (logic "1") to acquire a high-level output.

(2) If a slash mark appears between two descriptive terms, the device can be used to perform either of the two functions described. For example, if circuitry for a complementary output were added to the device described in Note 1, it would be described as an "AND/NAND" gate, and cross-listed as "NAND/AND" gate.

(3) When a hyphen appears between two or more descriptive terms, the device is a multifunction circuit which performs functions in series or series-parallel as described, and in the order listed, in the title. For example, if the outputs from two "AND" gates are applied to the input of a "NAND" gate, the circuit is described as an "AND-NAND" gate. If multifunction circuits contain stages that operate in parallel, the parallel functions are listed in alphabetical order. For example, if one of the input "AND" gates in the prior example were an "OR" gate, the device would be described as an "AND-OR-NAND" gate. The circuit schematic must be consulted to determine the precise configuration.

(4) If a device contains more than a single circuit and the circuits are functionally independent, the term "DUAL", "TRIPLE", or "QUAD", as appropriate, will follow the generic name. The circuits are usually identical but not in every case; the majority of exceptions involve a difference in the number of gate inputs. For example, if a device contained three identical "NAND" gates, each with three inputs, the device would be described as a "NAND, TRIPLE 3 INPUT" gate. On the other hand, if one of the circuits had only two inputs, the description would be "NAND, TRIPLE 2-3-3 INPUT" gate.

(5) All abbreviations are explained in Section 3.

MFR (Manufacturer) - The code name can be interpreted by reference to the Index of Manufacturers of Microelectronic Devices (Table 7-1).

TECH (Technology) - The code letter can be interpreted by reference to Table 7-4. These codes should not be confused with the Electrical Characteristic Codes. (Letter symbols are used for both.)

OPER TEMP CNTGRDE (Operating Temperature, Centrigrade) - The temperatures defined by the MIN and MAX columns represent absolute limits. Operation outside this range may be detrimental to the device. The sign has been omitted in the MAX column on the format for linear devices and should be understood as being positive in every case.

SUPPLY VOLTAGE VDC (Supply Voltage, DC Volts) - This field, divided into three separate columns, indicates a requirement for multiple supplies if data appear in column No. 2 or column No. 3. The voltage(s) listed are consistent with the values listed for other electrical characteristics of the device; however, the majority of digital devices may be operated at different voltage supply levels with corresponding trade-offs in the values of the other characteristics. The values coded as maximums are absolute; operation above these maximums may be detrimental to the device.

PACKAGE TYPE - The number or numbers appearing in this column refer to the Outline Drawings which are compiled in numerical order in Section 7.2.4. Because of space limitations, a maximum of two package types are shown for any single device tabulated, although a few manufacturers offer the devices in three or more types. Generally there will be a price differential, in favor of the can, between the can and rectangular type packages.

7.2.2.2 Digital Format Only

SUPPLY POWER MILLIWATTS - This field is divided into three separate columns, each of which presents typical power supply current drain at 25°C. The values in the column headed AVE represent the average power drain at a 50% duty cycle. The values in the columns headed ON and OFF represent the power drain when the output stage is conducting (logic "0") and not conducting (logic "1"), respectively. When multiple-circuit devices (dual, triple, etc.) are encountered, the values presented are per circuit.

FAN OUT - The value in this column represents the number of like-stage inputs that can be direct-coupled to each output of the circuit, over the stated operating temperature range. When the value is coded as maximum, it represents the fan out possible under the most favorable conditions and usually at 25°C. When two values appear in this column, the circuit has two output terminals with different fan-out capabilities. In this case, one of the outputs will usually be from an emitter follower. Generally, such multiple outputs can drive the stated loads simultaneously.

INPUT THRESHOLD VOLTS - The value in the column headed ZERO indicates the maximum voltage that can be applied to the circuit without turning on the input transistor. Any voltage below this level will be processed by the circuit as a "logic zero". The values under the ONE column represent the minimum voltage that can be applied to the input without turning off the input transistor. Any level

above this value will be processed by the circuit as a "logic one". Values in both columns are worst case at 25°C. Values shown are negative when the value in the ZERO column is greater than that in the ONE column.

NOISE IMMUNITY VOLTS - This is the difference between the input threshold level and the corresponding output level of the circuit. The column is included only as a convenience, since noise immunity voltage is simply the lower of the following two differences:

(1) Input threshold zero minus output level zero

(2) Output level one minus input threshold one

DELAY NANOSECS - The value in this column is the typical average propagation delay at 25°C. It is the sum of the turn-on delay and turn-off delay divided by 2. The values should be considered as gross approximations since they are highly dependent upon the conditions under which they are measured and upon the various definitions used to define turn-on time and turn-off time.

OPERATING SPEED MEGACYCLES - The value in this column represent the maximum clock rates for which the circuit was designed to operate, over the stated temperature range. Values coded as maximum indicate possible operating speeds under the most favorable conditions and at 25°C.

OUTPUT LEVEL VOLTS - The value in the column headed ZERO indicates the maximum low-level voltage that will appear at the output. The values in the column headed ONE indicate the minimum high-level voltage that will appear at the output. Both columns are worst-case values at 25°C. Values shown are negative when the value in the ZERO column is greater than that in the ONE column.

7.2.2.3 Linear Format Only

SUPPLY POWER MILLIWATTS - The value in this column represents the typical power drain from the supply at 25°C with no signal applied to the input. When a multiple circuit device (dual, triple, etc.) is encountered, the value shown is the power drain per circuit. A value coded as maximum indicates the absolute maximum power that can be dissipated by the device. Operation beyond this value may be detrimental to the device.

IMPEDANCE - The value shown is typical at 25°C.

GAIN - The value appearing in the VOLTAGE V/V column represents the ratio of output voltage to input voltage and is typical at 25°C. The value in the POWER DB column represents the ratio of output power to input power expressed in decibels. The values shown are typical at 25°C.

3 DB B.W. MCPS (Three-db Bandwidth, Megacycles) - The value shown is typical at 25°C and represents the upper frequency at which gain is 3 db down from the flat response. The lower 3-db frequency is generally a few hundred cycles per second or less.

N.F. DB (Noise Figure) - The value shown is typical at 25°C. Units are decibels.

COM.MODE REJ.DB (Common Mode Rejection) - The value shown is typical at 25°C. Units are decibels.

DIR.OFFSET MV (Differential Offset, Millivolts) - The value shown is the maximum input differential offset voltage and is typical at 25°C.

H.D. % MAX (Harmonic Distortion) - The value is shown as a percentage; it represents the maximum harmonic distortion at 25°C.

OUTPUT SIGNAL - The value shown under the column headed SWING represents the peak-to-peak voltage that can be obtained without clipping and is typical at 25°C. The value shown in the column headed POWER represents the available load power consistent with the specified distortion or, in cases where distortion is not applicable, the rated power-dissipation characteristic of the device.

7.2.3 Codes and Abbreviations

Codes and abbreviations used are presented in Tables 7-2, 7-3, and 7-4.

TABLE 7-2

ELECTRICAL CHARACTERISTIC CODES

Code	Explanation
*	Maximum
#	Minimum
A	Divide by 1000
B	Multiply by 1000
C	Divide by 100
D	Multiply by 100
E	Divide by 10
F	Multiply by 10
J	Microwatts divided by 10
K	Maximum forward current in milliamps
L	Diode reverse recovery time
M	Multiply by 10^{10}
P	Single ended
R	Input
S	Output
T	Typical
W	Worst case
X	Maximum milliamps

TABLE 7-3

ABBREVIATIONS

Abbreviation	Explanation
BCD to B	Binary Coded Decimal to Binary
BCD to D	Binary Coded Decimal to Decimal
CLCKD	Clocked
CPS	Cycles per second
DB	Decibel
DIFF	Differential
DIR	Direct
D to A	Digital to Analog
EX	Expandable
GND	Ground
H.D.	Harmonic Distortion
IF	Intermediate Frequency
INP	Input
MCPS	Megacycles per second
MONO	Monostable
N.F.	Noise Figure
PH	Phase
REV	Reverse
TRNSTRS	Transistors
SP	Split
VDC	Volts DC
VF	Variable Feedback
WC	With Complement

TABLE 7-4

MANUFACTURER TECHNOLOGY CODES

Code	Explanation
A	Silicon, monolithic, planar-diffused, epitaxial, passivated. Gold leads to aluminum metalization.
B	Same as A, except that all intraconnections are aluminum to aluminum.
C	Same as A, but also has polycrystalline isolation.
D	Alumina substrate glazed with alkali-free glass. Resistors formed by photoresist masking and subsequent etching of tin oxide deposited by non-vacuum process. Copper conductor material is applied by an electroless silk screen process. Transistors are discrete silicon face-bonded chips.
E	Alumina substrate. Resistors are vacuum-deposited nichrome. Transistors, diodes, and capacitors are attached discrete components.
F	Same as A, but without epitaxy.
G	Alumina substrate; Cermet resistors; metal slurry intraconnections and capacitors applied by silk screen process and brazed to substrate. Active devices are planar passivated silicon chips bonded to wafer. Connections from chips are thermocompression-bonded wire leads.
H	Multichip; all circuit elements are separate planar epitaxial passivated silicon chips bonded to a nonconductive substrate. Intraconnections are thermocompression-bonded wires. Multiple internal connections to a single node are made to vacuum-deposited or brazed metal-slurry lands. When possible, chips are bonded directly to metal header or header post for greater heat dissipating and reduced lead length. Construction details will depend in large measure on circuit type and design.
J	Same as A except that resistors are vacuum-deposited on the monocrystalline substrate
K	Monolithic device consisting of metal-oxide-silicon transistors. Source and drain regions are planar-diffused. Isolation layer is silicon monoxide. Gate electrodes and intraconnections are vacuum-deposited aluminum.
L	Resistors formed by photoresist masking of pyrolytically-deposited tin oxide on glass of matched expansivity. Film thickness is typically 2500°A, and line widths are 0.003" minimum. Terminations and capacitor plates are silk-screened silver slurry; after silk-screening, they are fired. Passive components are hermetically sealed by a fusible powdered glass, which also serves as a dielectric for the capacitor. Intraconnection patterns are electroplated and photo-etched. Active devices are cased in TO-18 or TO-46 cans and are attached by welding.
M	Thin film passive components with active devices separately attached.
N	Thin film resistors and conductors vacuum-deposited on ceramic substrate. A monolithic diffused silicon chip containing all active devices is die-attached to the ceramic substrate, and intraconnections between chip, subtrate, and bonding posts are thermocompression-bonded leads.
O	Cermet resistors; discrete active devices separately attached.
P	Conductors and capacitors deposited on a nonconducting substrate. Inductor leads are bonded to conductor pads on the substrate.
R	Multichip; selected portions of the circuit are planar diffused into two or more silicon chips. The chips are intraconnected with thermocompression-bonded wire leads.

7.2.4 Outline Drawings

Outline drawings of packages used for microelectronic devices are shown on the following pages. The specific configurations are cross-referenced -- by type number -- to the Catalog of Devices. The dimensions shown are in inches.

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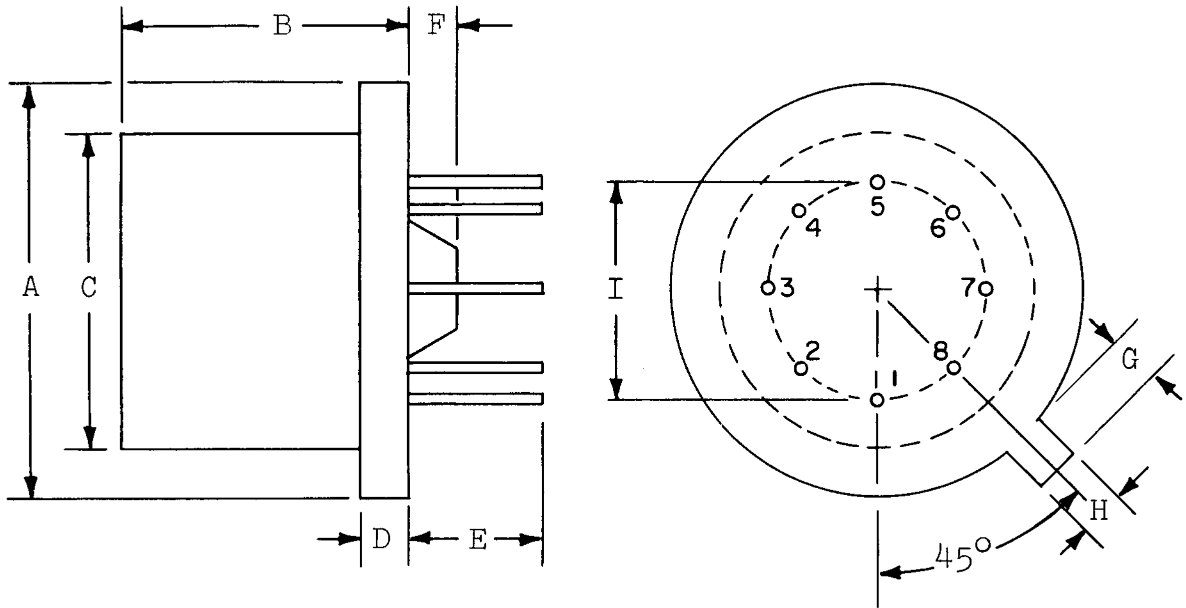
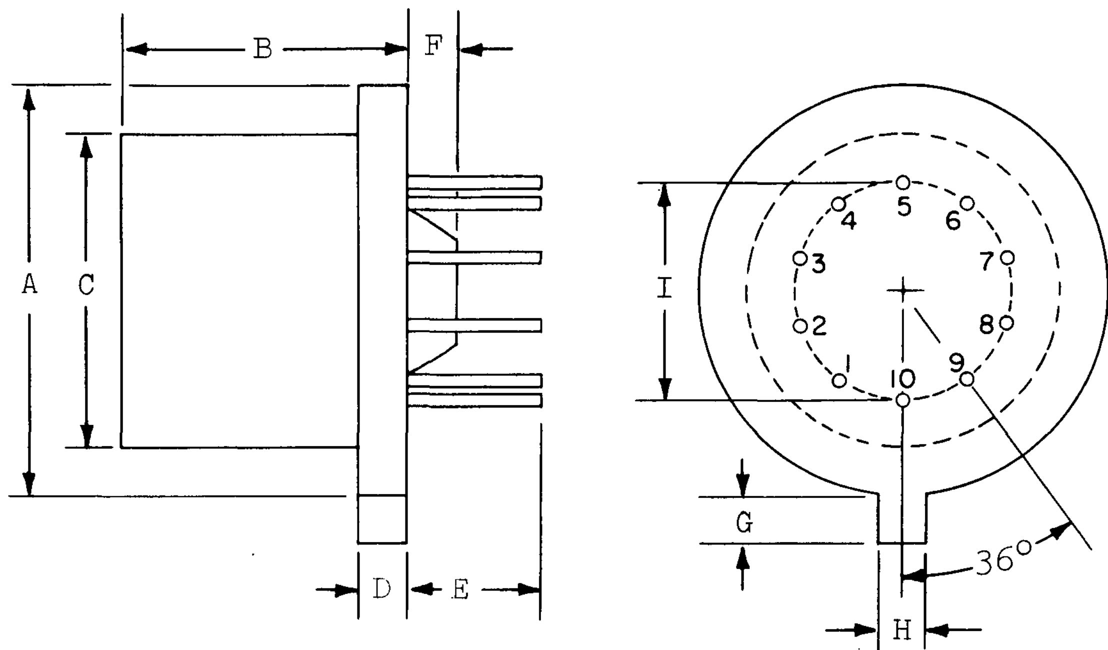


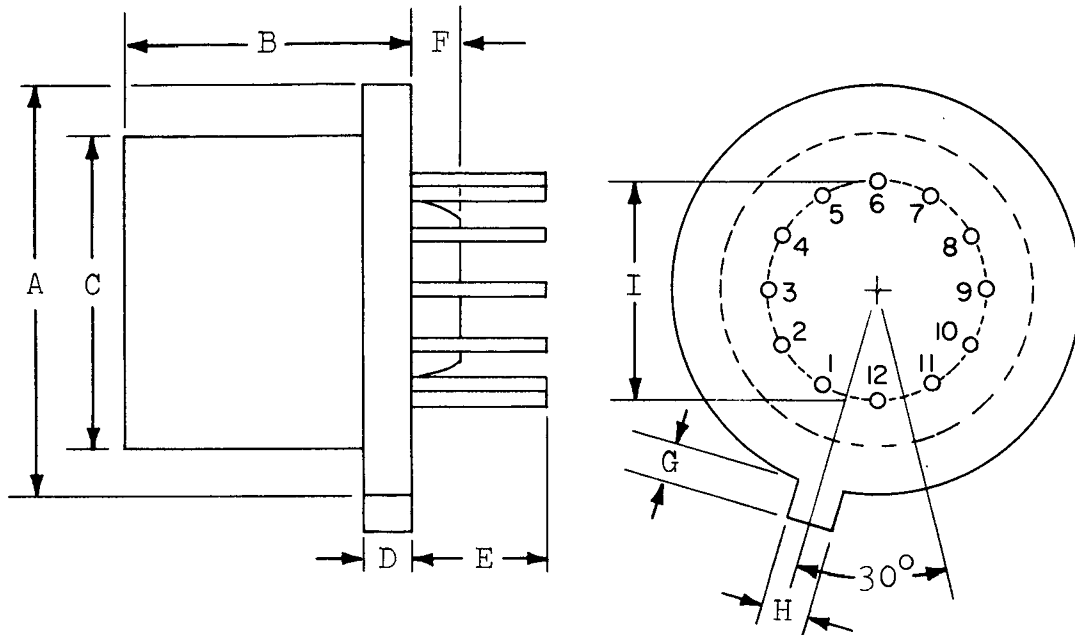
Type No.*	A	B	C	D	E	F	G	H	I	Lead Dia.
0	0.370 0.290	0.180 0.160	0.335 0.290	0.125 0.009	1.500 Min.		0.029 Min.	0.034 0.028	0.210 0.190	0.019 0.016
1	0.370 0.335	0.185 0.165	0.335 0.305	0.040 Max.	0.500 Min.	0.050 Max.	0.045 0.029	0.034 0.028	0.200	0.019 0.016
2	0.370 0.355	0.180 0.170	0.325 0.315	0.030 0.020	1.500 Min.	0.045 0.015	0.033 0.028	0.034 0.028	0.210 0.190	0.019 0.016
3	0.365 Max.	0.180 Max.	0.327 Max.	0.030 Max.	0.750 Min.	0.040 Max.	0.033 0.029	0.034 0.028	0.210 0.190	0.019 0.016
4	0.360	0.180 Max.	0.335		0.750					0.230
5	0.362 0.358	0.185 0.165	0.328 0.322	0.025	1.530	0.030	0.034 0.029	0.034 0.028	0.200	0.019 0.016
6	0.270 0.240	0.085 0.065	0.240 0.205	0.040 Max.	0.500 Min.	N/A	0.025 0.015	0.025 0.015	0.141	0.019 0.016
7	0.370 0.355	0.180 0.170	0.305 0.335		1.500 Min.		0.045 0.029	0.028 0.034	0.210 0.190	0.019 0.016
8	0.270 0.240	0.080 0.060	0.240 0.220	0.040 Max.	1.5 Min.		0.025 0.015	0.025 0.015	0.141	0.019 0.016
9	0.365 0.355	0.180 0.170	0.325 0.315		0.500 Min.		0.033 0.029	0.034 0.028	0.210 0.190	0.019 0.016

*Package Type



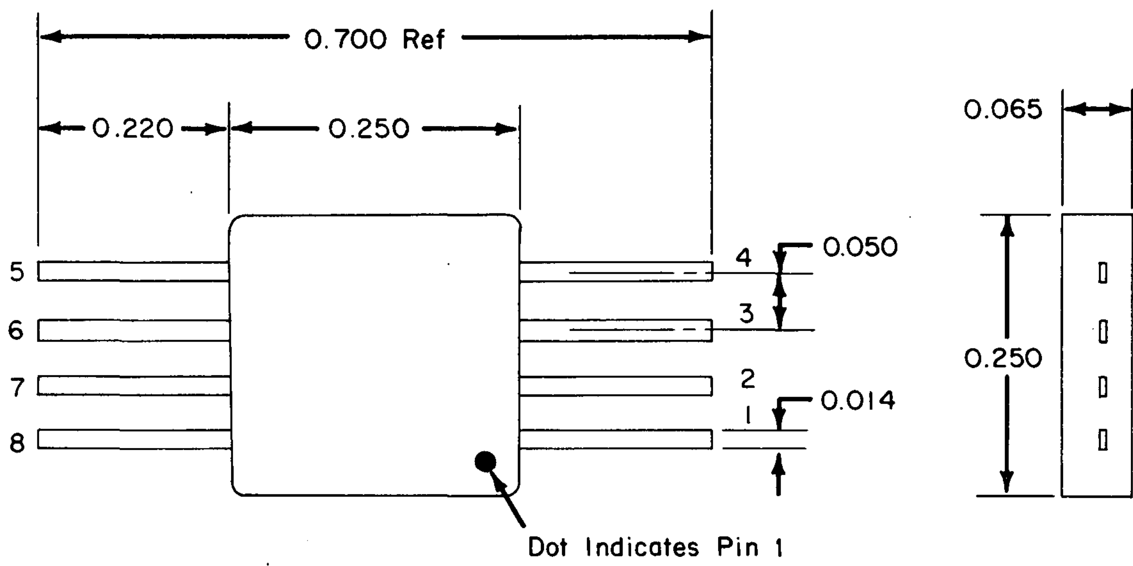
Type No.*	A	B	C	D	E	F	G	H	I	Lead Dia.
10	0.360	0.180	0.325		0.300 Min.		0.034 0.026	0.034 0.028	0.230	0.019 0.016
11	0.370 0.335	0.185 0.165	0.335 0.305	0.040 Max.	0.500 Min.	0.050 Max.	0.045 0.029	0.034 0.028	0.230	0.019 0.016
12	0.370 0.355	0.180 0.170	0.325 0.315	0.030 0.020	0.750 Min.	0.045 0.015	0.040 0.030	0.034 0.028	0.240 0.220	0.019 0.016
13	0.360	0.180 Max.	0.335		0.750				0.230	
14	0.362 0.358	0.102 0.096	0.302 0.298	0.025	1.53	0.025	0.034 0.029	0.034 0.028	0.230	0.019 0.016
15	0.370 0.350	0.175 Max.	0.335 0.322	0.035	0.165 0.150				0.200	0.019 0.016
16	0.370 0.290	0.180 0.160	0.335 0.290	0.125 0.009	1.50 Min.		0.029 Min.	0.034 0.028	0.210 0.190	0.019 0.016
17	0.365 Max.	0.180 Max.	0.327 Max.	0.030 Max.	0.750	0.040 Max.	0.033 0.029	0.034 0.028	0.235 0.220	0.019 0.016
18	0.370 0.290	0.180 0.140	0.335 0.290	0.125 0.009	1.50 Min.		0.029 Min.	0.034 0.028	0.230	0.019 0.016
19	0.370 0.335	0.260 0.240	0.335 0.305	0.040 Max.	0.500 Min.	0.050 Max.	0.045 0.029	0.034 0.028	0.230	0.019 0.016

*Package Type



Type No.*	A	B	C	D	E	F	G	H	I	Lead Dia
20	0.370 0.355	0.180 0.170	0.335 0.305		1.500 Min.		0.045 0.029	0.034 0.028	0.210 0.190	0.019 0.016
21	0.365 0.355	0.180 0.170	0.325 0.315		0.500 Min.		0.033 0.029	0.034 0.028	0.210 0.190	0.019 0.016
22	0.370 0.355	0.180 0.170	0.325 0.315	0.030 0.020	0.750 Min.	0.045 0.015	0.040 0.030	0.034 0.028	0.240 0.220	0.019 0.016
23	0.370 0.350	0.160 0.140	0.335 0.305	0.040 Max.	0.250 Min.	0.040 0.010	0.045 0.029	0.034 0.028	0.160 0.140	0.019 0.016
24	0.362 0.358	0.185 0.165	0.328 0.322	0.025 Typ	1.530 Typ	0.030 Typ	0.034 0.029	0.034 0.028	0.200 Typ	0.019 0.016
25	0.370 0.335	0.180 Max.	0.335 0.305		0.500 Min.		0.045 0.024	0.034 0.028	0.245 0.215	0.020 0.016
26	0.360	0.180 Max.	0.325 Max.		0.300 Min.		0.034 0.026	0.034 0.028	0.200	0.019 0.016
27	0.370 0.350	0.190 0.170	0.335 0.315	0.030 0.020	0.300 Min.		0.33 0.28	0.34 0.28	0.240 0.220	0.019 0.016

*Package Type



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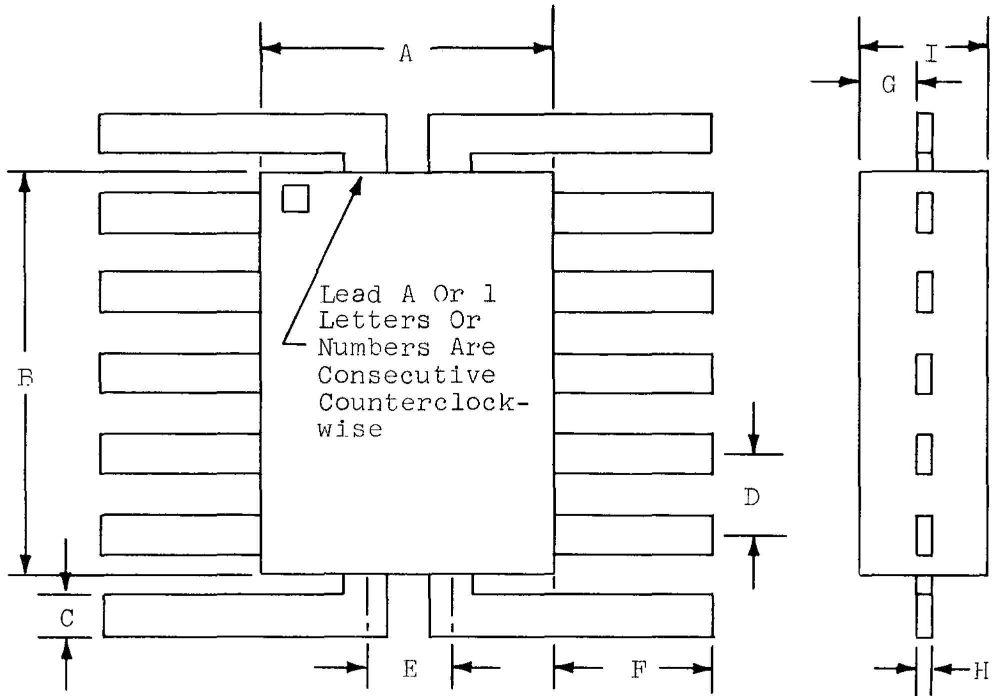
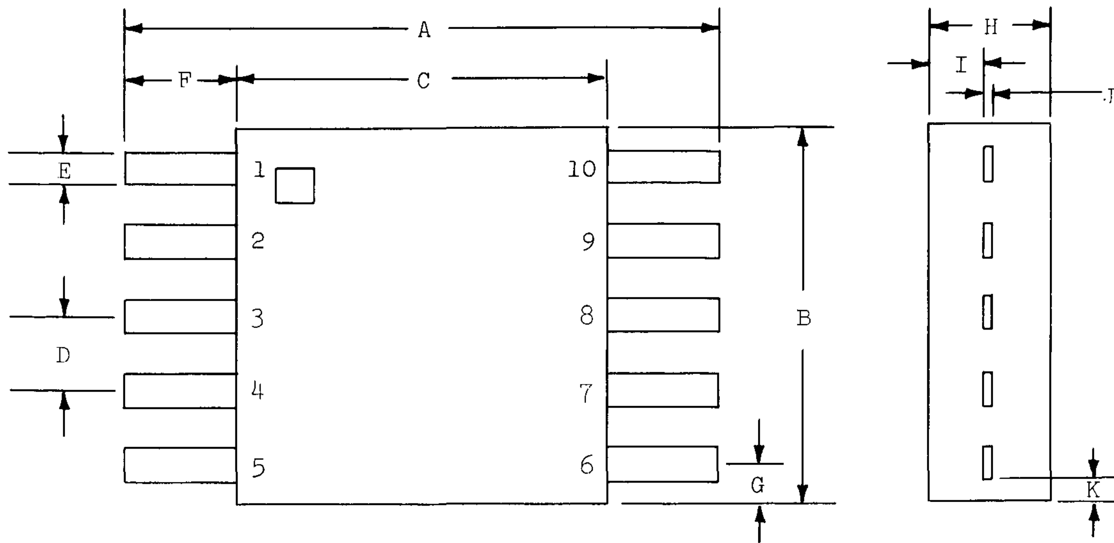
PACKAGE TYPE 31



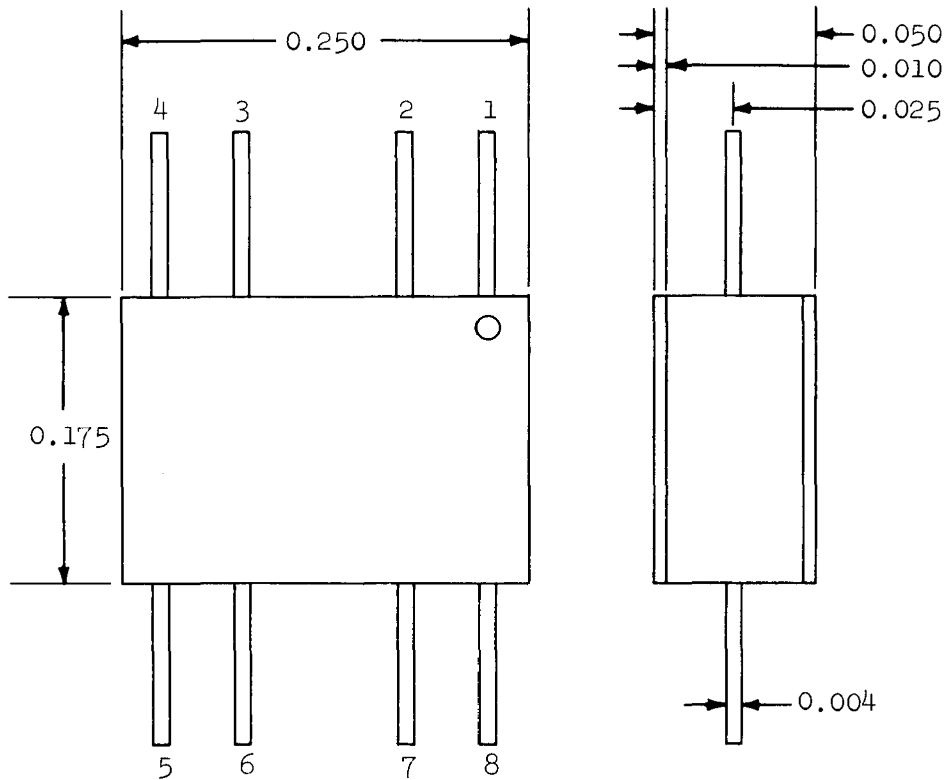
Type No.*	A	B	C	D	E	F	G	H	I
37	0.250	0.250	0.017	0.050		0.375 Max.			0.065
38	0.140	0.250	0.012	0.050		0.180			0.055 Max.
40	0.195 0.165	0.270 0.240	0.018 0.014	0.050	0.050	0.350 Min.	0.008 0.022	0.005 0.003	0.055 0.040
41	0.240 0.230	0.240 0.230	0.018 0.016	0.050			0.010 Min.	0.004 0.003	0.060 0.048
42	0.135 0.115	0.260 0.240	0.012	0.050		0.180 Min.	0.018 0.008	0.004	0.045 0.025
43	0.125	0.250	0.012	0.050		0.185		0.004	0.055 Max.
44	0.265 Max.	0.265		0.050		0.188			0.050
45	0.175	0.250		0.050			0.030	0.004	0.060
46	0.125 0.135	0.250 0.260	0.010 0.013			0.130 Min.	0.008 0.016	0.003 0.005	0.040 0.050
47	0.195 0.175	0.275 0.240	0.019 0.016	0.050		0.300 Min.	0.030 0.015	0.006 0.003	0.055 0.040
48	0.135 0.125	0.260 0.250	0.015 0.010	0.050		0.122 0.112	0.013	0.005 0.003	0.045 0.030
49	0.250	0.250	0.015 Typ	0.050 Typ		0.150 Min.	0.030	.0035 .0055	0.055 Max.

*Package Type

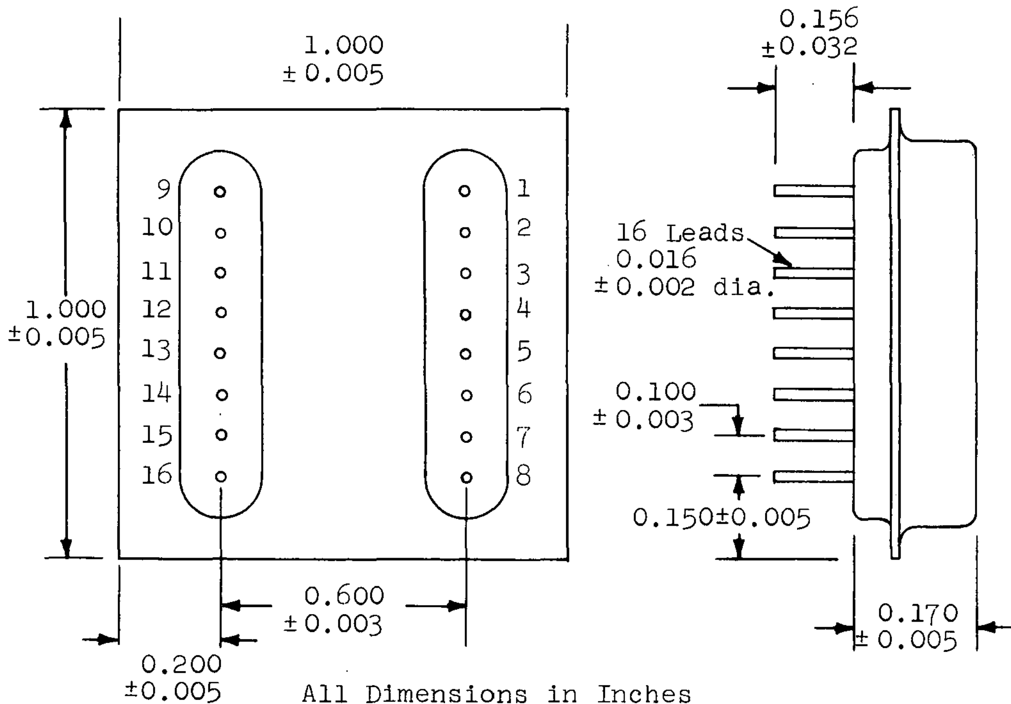


Type No.*	A	B	C	D	E	F	G	H	I	J	K
50	0.550	0.250	0.250	0.050	0.015	0.150 Min.		0.055 Max.	0.030	0.06 0.03	
51		0.240 0.230	0.240 0.230	0.052 0.048	0.018 0.016	0.210 Min.		0.070 Max.	0.010 Min.	0.004 0.003	0.015 0.005
52	0.750 0.730	0.255 0.245	0.260 0.240	0.050 0.005	0.014 0.015	0.250 0.230	0.038 0.012	0.063 0.051	0.027 0.006	0.006 0.004	
53	0.750	0.275 Max	0.250	0.050	0.015	0.460		0.060 Max.		0.005	
54		0.260 Max.	0.260 Max.	0.050	0.017	0.235 Min.		0.070 Max.	0.020	0.004	
55	0.760 0.740	0.265 0.245	0.265 0.240	0.055 0.045	0.018 0.015	0.260 0.235		0.065 0.055		0.006 0.004	
56	0.760 0.740	0.255 0.245	0.260 0.230	0.055 0.045	0.018 0.015	0.260 0.235	0.038 0.012	0.065 0.055	0.025 0.015	0.006 0.004	0.030 0.003
57	0.505 0.495	0.260 0.250	0.135 0.125	0.050	0.013 0.010	0.0185		0.045 0.030	0.013 Min.	0.005	0.020 0.018
58	0.290 0.380	0.255 0.245	0.130 0.120	0.050	0.010	0.080	0.025	0.040 0.030	0.012 Min.	0.003	
59		0.250	0.175					0.060	0.035	0.004	
60		0.500	0.500	0.100	0.020		0.050	0.125	0.050	0.010	
61		0.275 Max.	0.190 Max.	0.050		0.200 Min.		0.070 Max.		0.005	
62		0.275 0.255	0.170 0.150	0.050	0.017 0.013	0.249 0.187		0.060 0.040	0.017 Min.	0.006 0.004	
63		0.260 0.240	0.260 0.240	0.055 0.045	0.019 0.010	0.070 Min.		0.070 0.030	0.030 0.005	0.006 0.003	
64	0.780 0.720	0.260 0.240	0.260 0.240	0.055 0.045	0.019 0.015			0.060 0.045	0.029 0.015	0.006 0.003	
65	0.500	0.250	0.140	0.050	0.012	0.180		0.055 Max.			
66		0.260 0.240	0.260 0.240	0.050	0.019 0.015	0.250 Min.		0.060 0.050		0.006 0.003	

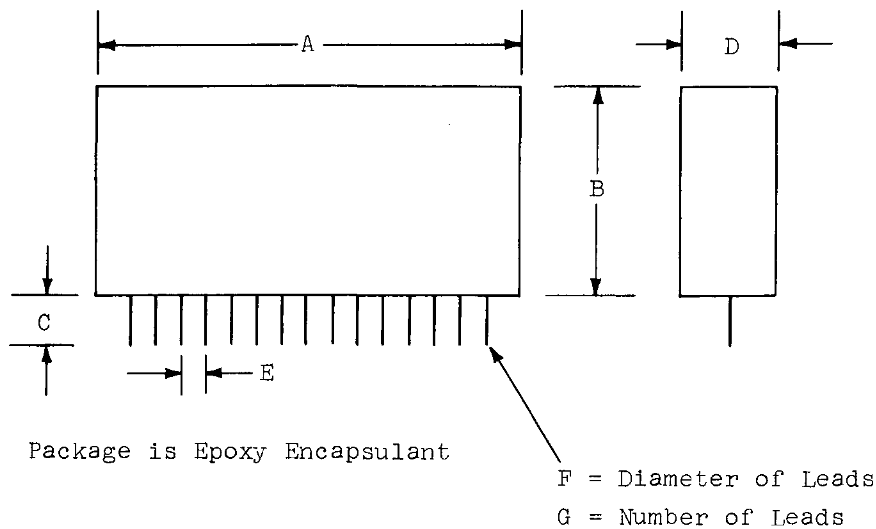
* Package Type



PACKAGE TYPE 70

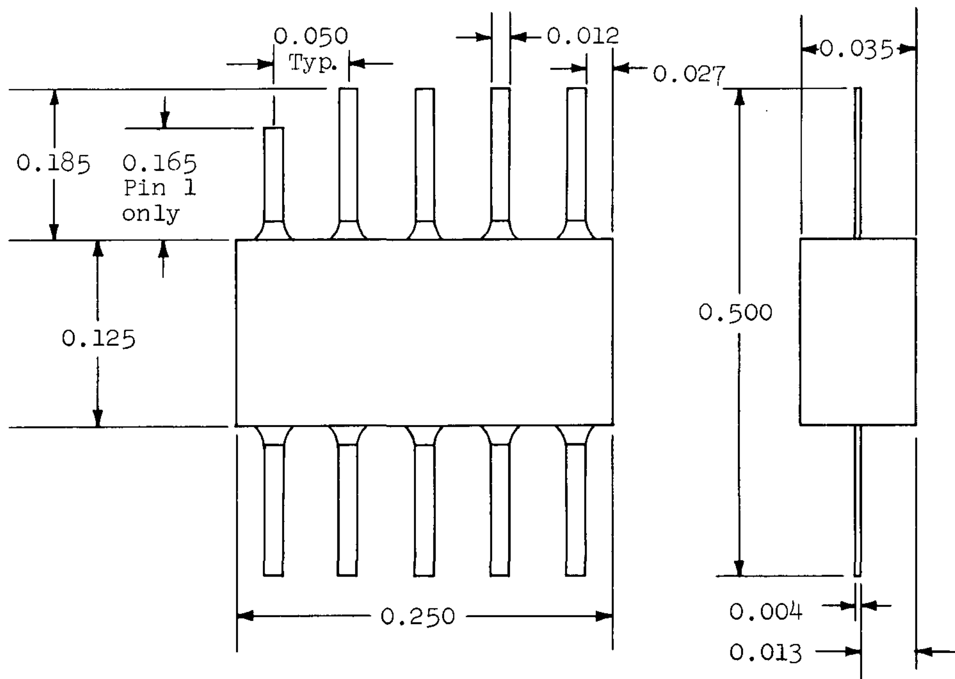


PACKAGE TYPE 71



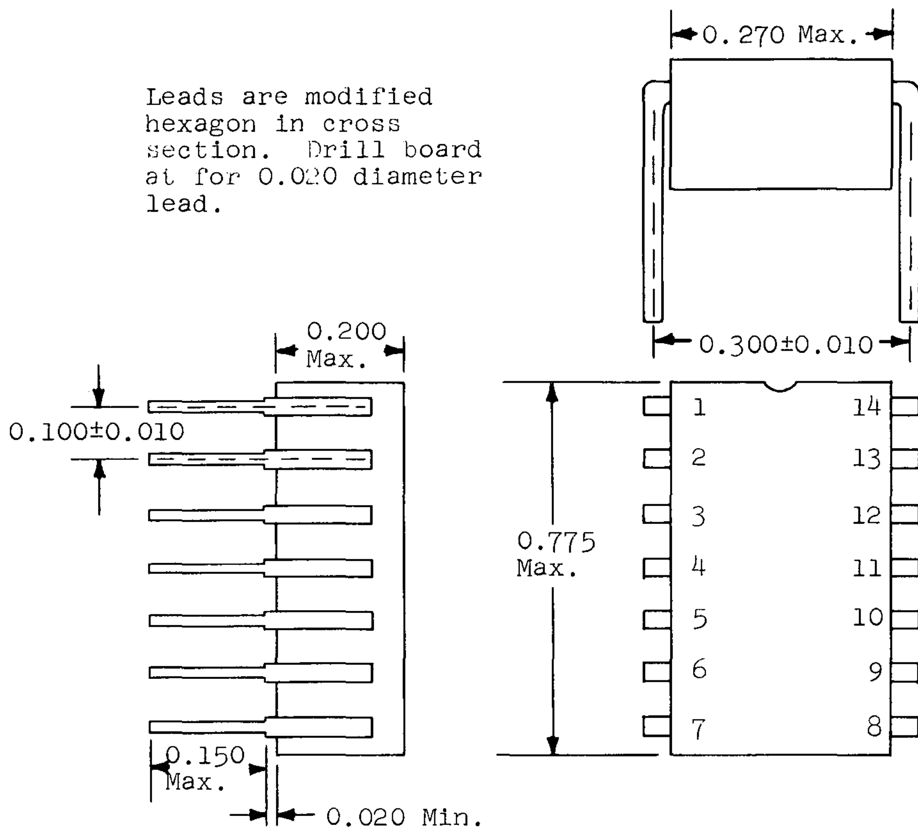
Type	A	B	C	D	E	F	G
72	0.804 Max.	0.604 Max.	0.300 Min.	0.85 Max.	0.050 Typ.	0.015	15
73	0.650 Max.	0.700 Max.	0.500 Max.	0.200 Max.			5

PACKAGE TYPE 72 AND 73

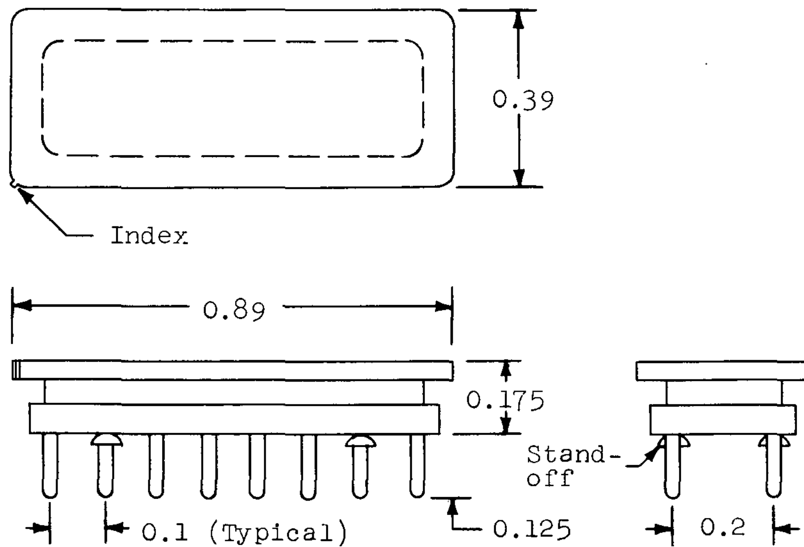


All dimensions in inches

PACKAGE TYPE 74



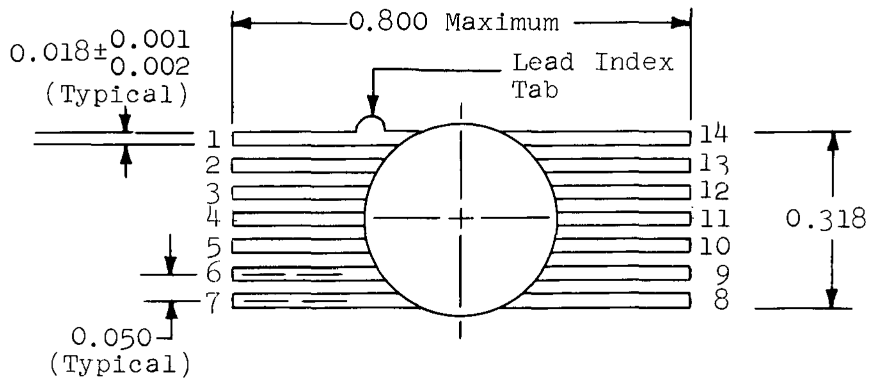
PACKAGE TYPE 75

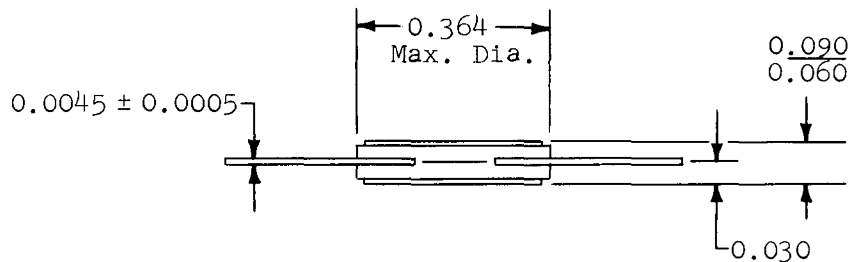


Notes:

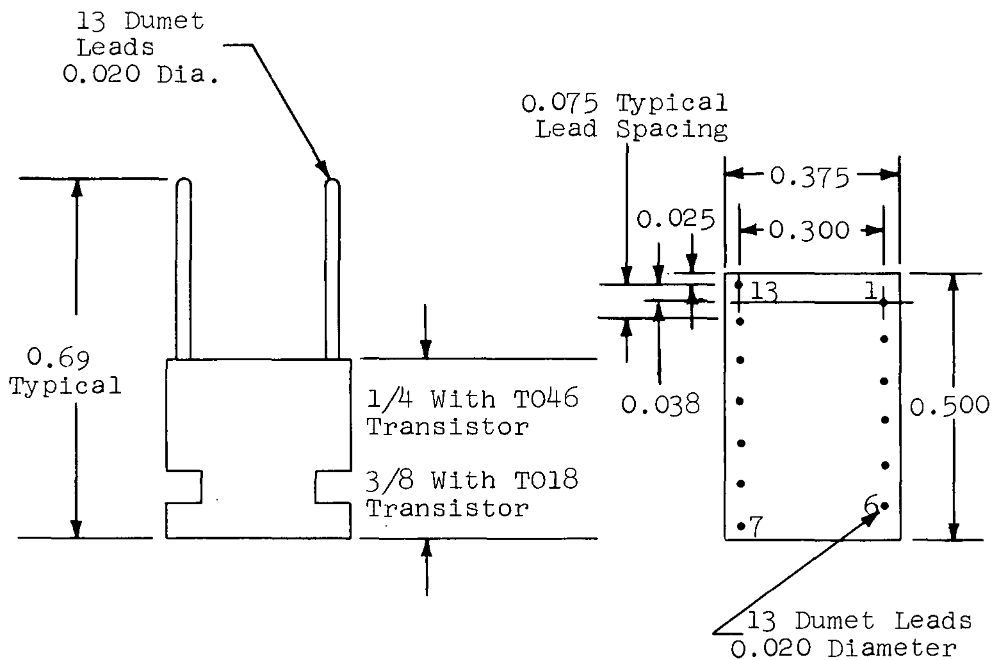
1. All dimensions are nominal in inches.
2. All pins are 0.02 diameter.

PACKAGE TYPE 76

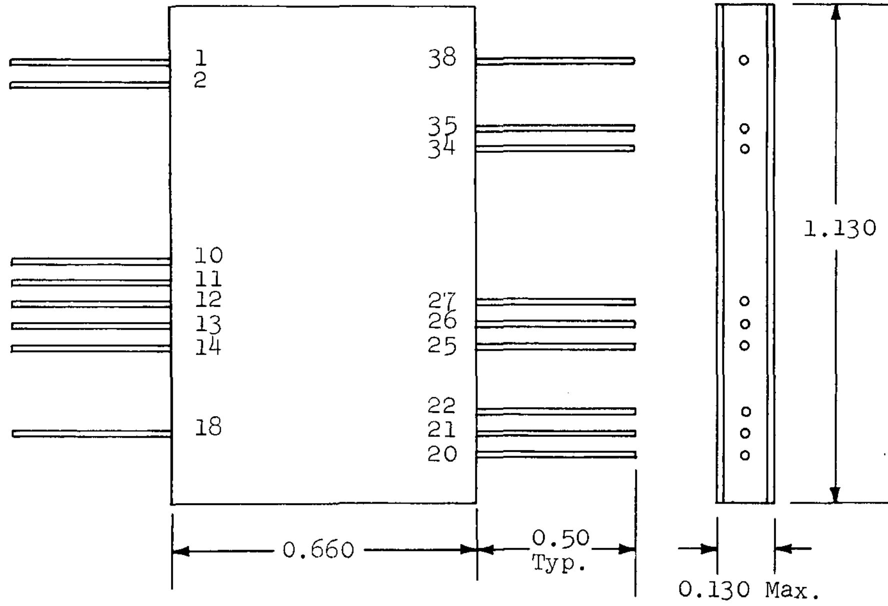




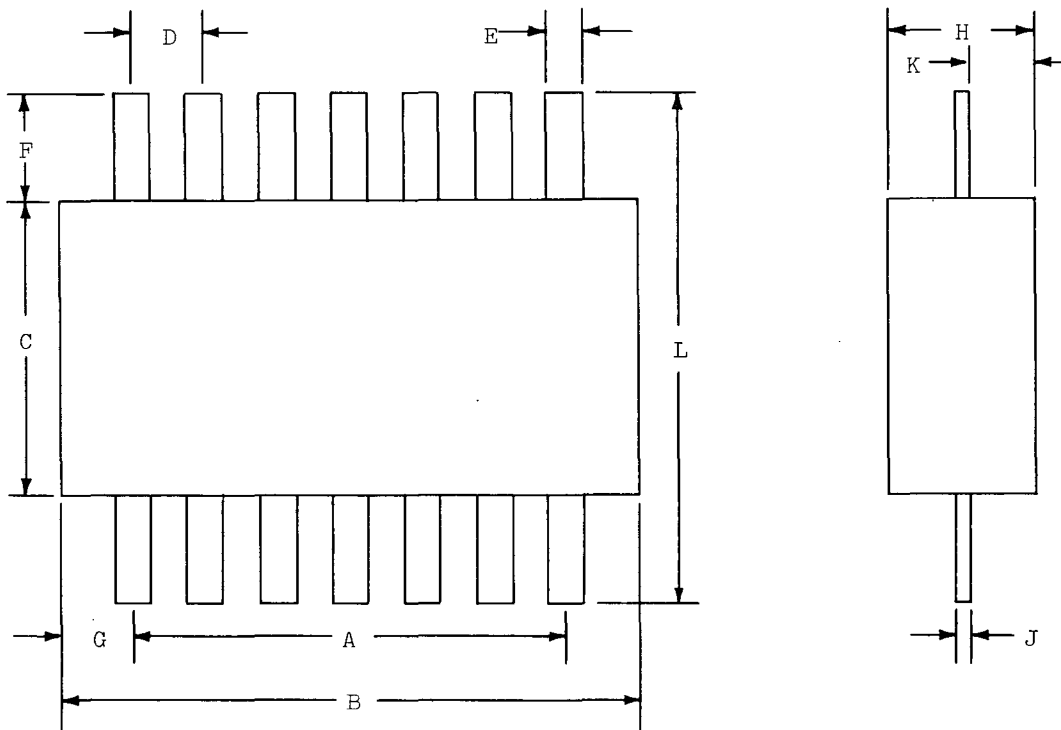
PACKAGE TYPE 77



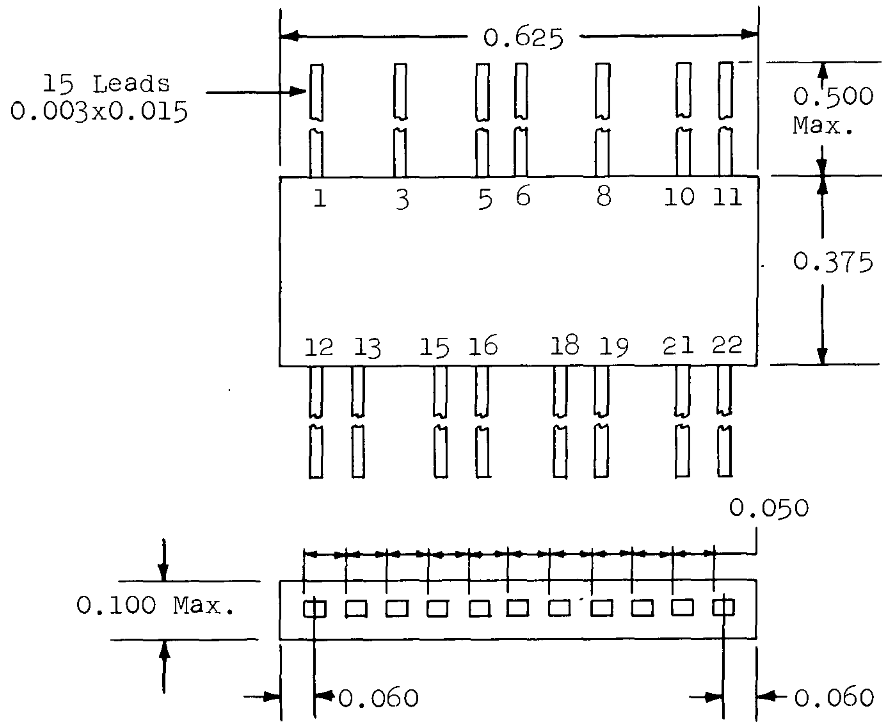
PACKAGE TYPE 78



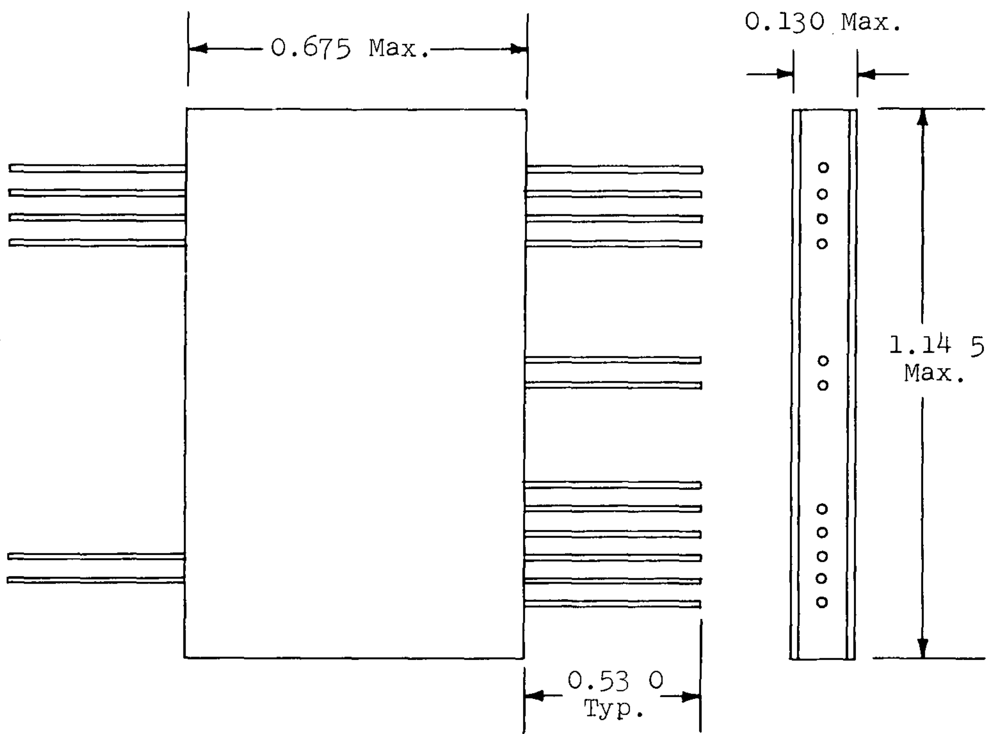
PACKAGE TYPE 79



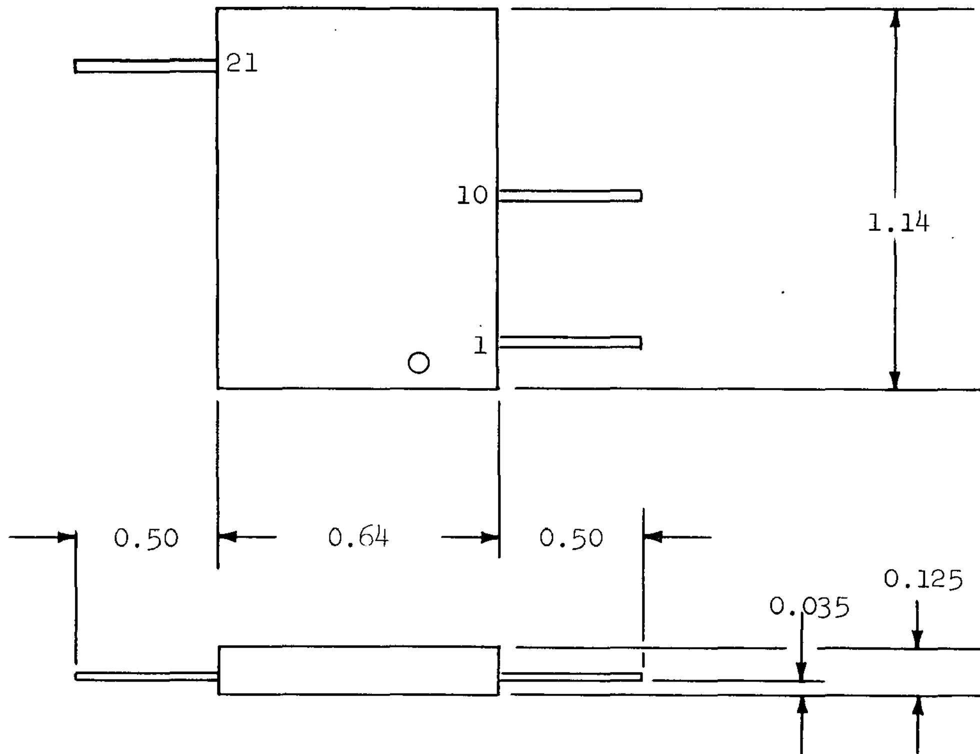
Type No.	A	B	C	D	E	F	G	H	J	K	L
80	0.300	0.360 0.380	0.140 0.160	0.047 0.053	0.014 0.016	0.125 Min.	0.035	0.065 Max.	0.0035 0.0045	0.015	
81		0.330 0.350	0.240 0.260	0.045 0.055	0.015 0.019	0.230 0.250	0.013 0.028	0.051 0.065	0.004 0.006	0.006 0.027	0.730 0.750
82		0.385 0.365	0.260 0.240	0.051 0.049	0.017 0.015	0.250 Min.		0.080 Max	0.006 0.004	0.012 0.004	
83		0.390 0.375	0.390 0.375	0.55 0.45	0.017 0.015	0.500 Min.	0.038	0.075 Max.			



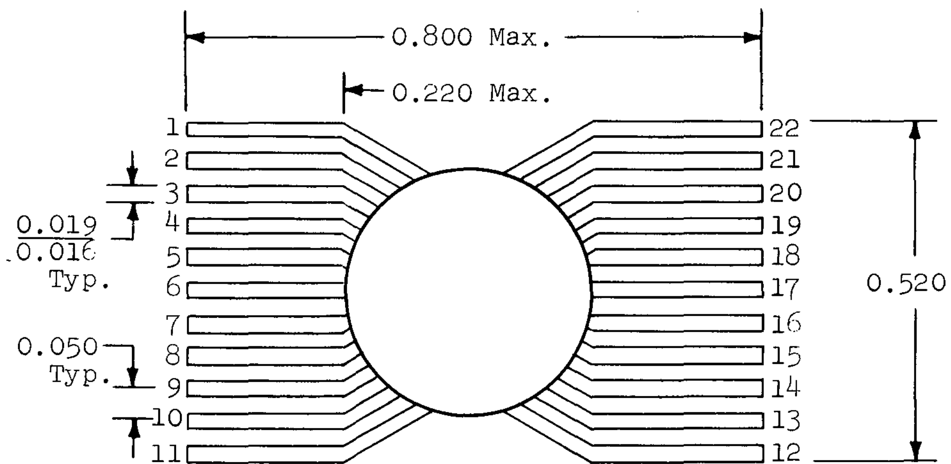
PACKAGE TYPE 85

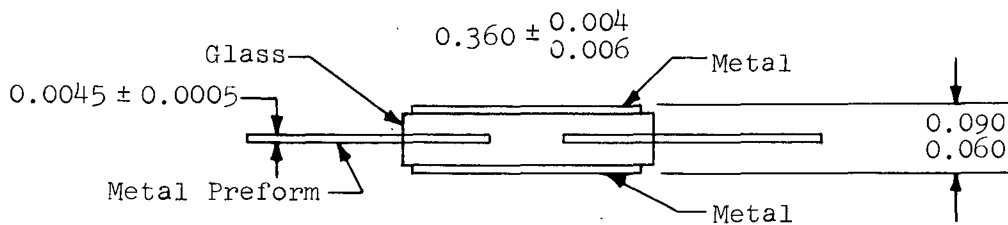


PACKAGE TYPE 86

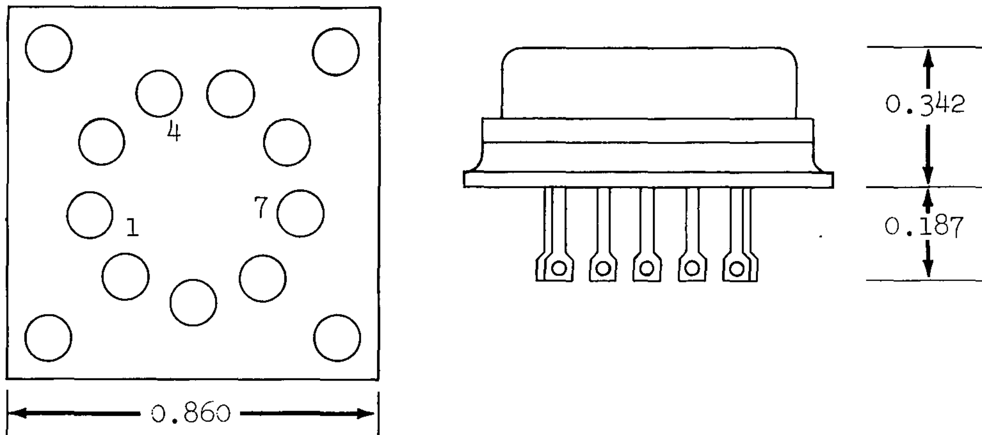


PACKAGE TYPE 87

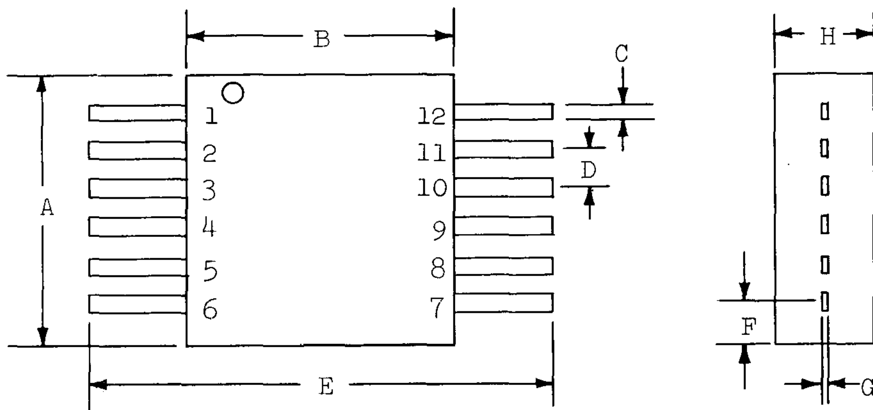




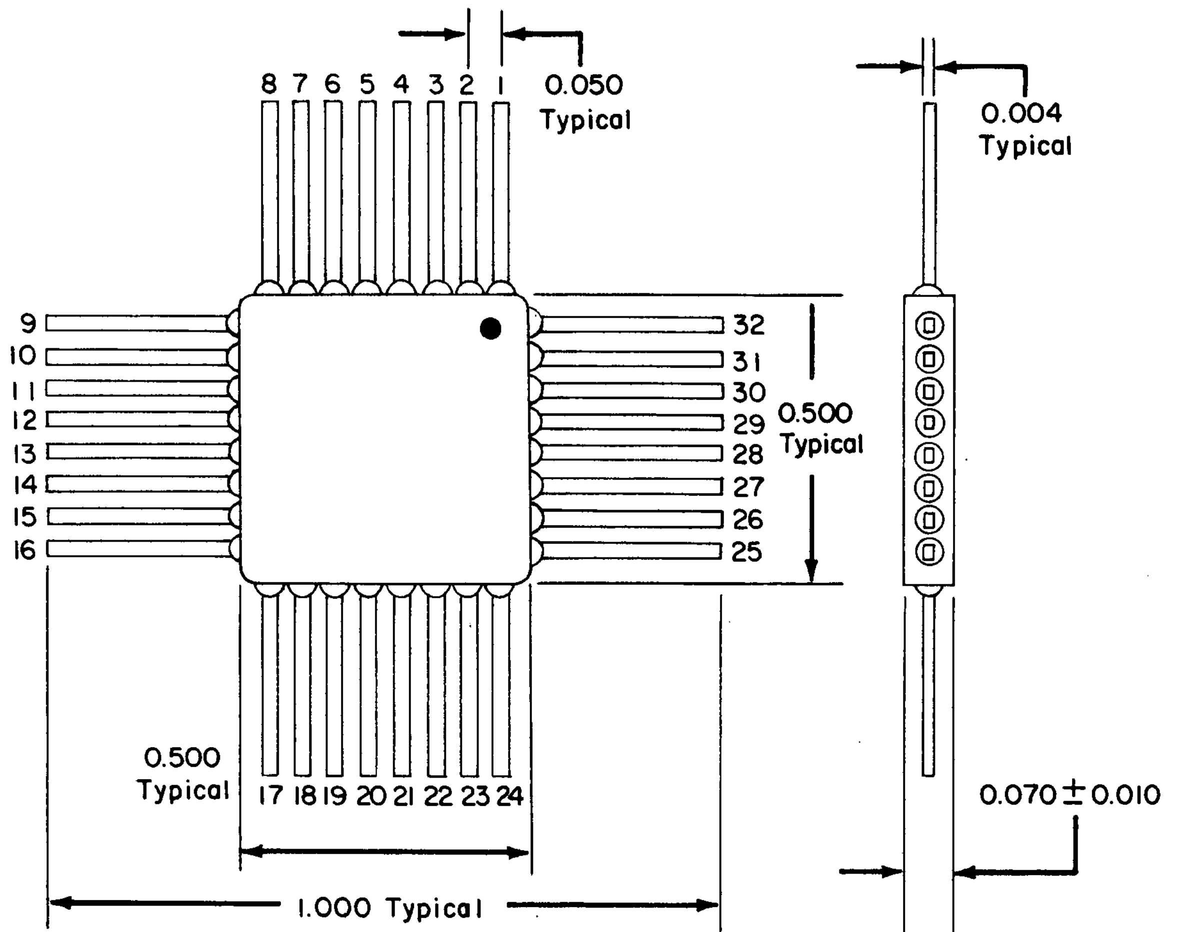
PACKAGE TYPE 88



PACKAGE TYPE 89



Type No.	A	B	C	D	E	F	G	H
90	0.375	0.375	0.015	0.050		0.062	0.003	0.085 Max.
91	0.375	0.250	0.015	0.050	0.690		0.005	0.060 Max.
92	0.406 0.375	0.406 0.375	0.017 0.013	0.055 0.045			0.006 0.004	0.055 Max.
93	0.390 Max.	0.390 Max.	0.015	0.050		0.062	0.003	0.100 Max.



PACKAGE TYPE 96

7.2.5 Schematic Drawings

Schematic drawings of microelectronic devices are presented on the following pages, preceded by an index that is cross-referenced -- by manufacturer's name and part number -- to the Catalog of Devices. In many instances the circuit configuration shown is only a basic representation of the actual circuit. The descriptive terms following the generic name in the Circuit Description column of the Catalog of Devices must be applied to modify as necessary the circuit shown. The Circuit Description column may indicate a need for modification in the following characteristics:

(1) Multiple circuit (dual, triple, etc.)

(2) Number of inputs

(3) Expandable nodes

Where appropriate, additional differences between the configuration shown and the actual configuration are indicated by notes in the Exceptions column of the index.

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INDEX OF SCHEMATIC DIAGRAMS

MFR	MFRS PART NUMBER	FIG NO.	EXCEPTIONS
AMEL	A13-251	506	
AMEL	B-INDUS	142	
AMEL	B-PREM	142	
AMEL	B-STAND	142	
AMEL	B11-501	142	
AMEL	B11-504	142	
AMEL	B11-508	142	
AMEL	B12-001	197	
AMEL	C-INDUS	118	
AMEL	C-PREM	118	
AMEL	C-STAND	118	
AMEL	D13-000	507	
AMEL	D13-001	507	
AMEL	D13-002	507	
AMEL	E-INDUS	140	NO PULL-UP RESISTOR
AMEL	E-PREM	140	NO PULL-UP RESISTOR
AMEL	E-STAND	140	NO PULL-UP RESISTOR
AMEL	E12-001	113	
AMEL	E13-401	537	
AMEL	E13-511	538	
AMEL	E16-511	538	
AMEL	F-INDUS	226	
AMEL	F-PREM	226	
AMEL	F-STAND	226	
AMEL	G-INDUS	140	
AMEL	G-PREM	140	
AMEL	G-STAND	140	
AMEL	G12-002	196	
AMEL	G12-003	103	
AMEL	H-INDUS	129	
AMEL	H-PREM	129	
AMEL	H-STAND	129	
AMEL	I-INDUS	140	
AMEL	I-PREM	140	
AMEL	I-STAND	140	
AMEL	J-INDUS	140	
AMEL	J-PREM	140	
AMEL	J-STAND	140	
AMEL	K-INDUS	140	
AMEL	K-PREM	140	
AMEL	K-STAND	140	
AMEL	L-INDUS	140	
AMEL	L-PREM	140	
AMEL	L-STAND	140	
AMEL	M-INDUS	140	
AMEL	M-PREM	140	
AMEL	M-STAND	140	
AMEL	N-INDUS	140	
AMEL	N-PREM	140	
AMEL	N-STAND	140	
AMEL	011-001	169	
AMEL	011-004	169	
AMEL	011-008	169	
AMEL	012-001	170	
AMEL	042-001	170	
AMEL	P-INDUS	251	R1,R2,Q1 OMITTED
AMEL	P-PREM	251	R1,R2,Q1 OMITTED
AMEL	P-STAND	251	R1,R2,Q1 OMITTED
AMEL	Q-INDUS	140	
AMEL	Q-PREM	140	
AMEL	Q-STAND	140	
AMEL	R-INDUS	251	
AMEL	R-PREM	251	
AMEL	R-STAND	251	
AMEL	R12-001	152	
AMEL	R12-002	148	
AMEL	S-INDUS	249	
AMEL	S-PREM	249	
AMEL	S-STAND	249	
AMEL	T-INDUS	251	TERMINAL A OMITTED
AMEL	T-PREM	251	TERMINAL A OMITTED
AMEL	T-STAND	251	TERMINAL A OMITTED
AMEL	U-INDUS	250	
AMEL	U-PREM	250	
AMEL	U-STAND	250	
CORN	0065	109	
CORN	0067	236	
CORN	0094	146	
FSC	A702	515	
FSC	A702A	515	
FSC	A702C	515	
FSC	A709	552	
FSC	A709C	552	
FSC	A710	553	
FSC	A710C	553	
FSC	A711	554	
FSC	A711C	554	
FSC	CL958		
FSC	CS700	198	NO PULL-UP RESISTOR
FSC	CS701	198	A AND B INTRACONNECTED
FSC	CS704	231	
FSC	CS705	113	
FSC	CS709	113	
FSC	CTL952		
FSC	CTL953	116	
FSC	CTL954	116	
FSC	CTL955	116	
FSC	CTL956	122	
FSC	DTL930	192	
FSC	DTL931	149	

(continued)

INDEX OF SCHEMATIC DIAGRAMS (continued)

MFR	MFRS PART NUMBER	FIG NO.	EXCEPTIONS
FSC	DTL932	189	
FSC	DTL933	113	
FSC	DTL944	185	
FSC	DTL945	150	
FSC	DTL946	192	
FSC	DTL948	150	
FSC	DTL950		
FSC	DTL951		
FSC	DTL962	192	
FSC	FL90029	142	
FSC	FL90329	140	
FSC	FL90529	249	
FSC	FL91029	140	
FSC	FL91129	213	
FSC	FL91429	140	
FSC	FL91529	140	
FSC	FL92129	140	NO PULL-UP RESISTOR
FSC	FL92328	155	
FSC	FL92329	155	
FSC	FL92629	155	
FSC	FL92729	145	
FSC	FL93029	192	
FSC	FL93129	149	
FSC	FL93229	189	
FSC	FL93329	113	
FSC	FL94429	185	
FSC	FL94529	150	
FSC	FL94629	192	
FSC	FL94829	150	
FSC	FL95029		
FSC	FL95129		
FSC	FL96229	192	
FSC	FSA1400	121	
FSC	FSA2000	121	
FSC	FSA2001	121	
FSC	FSA2002	113	NO RESISTOR,REV DIODES
FSC	FSA2003	113	NO RESISTOR
FSC	L900	142	
FSC	L900C	142	
FSC	L901	118	
FSC	L901C	118	
FSC	L902	226	
FSC	L902C	226	
FSC	L903	140	
FSC	L903C	140	
FSC	L904	129	
FSC	L904C	129	
FSC	L905	249	
FSC	L905C	249	
FSC	L906	249	INVERTING STAGE OMITTED
FSC	L906C	249	INVERTING STAGE OMITTED
FSC	L907	140	
FSC	L907C	140	
FSC	L914	140	
FSC	L914C	140	
FSC	L915	140	
FSC	L915C	140	
FSC	L924	212	
FSC	L926	153	
FSC	L926C	153	
FSC	L927	145	
FSC	L927C	145	
FSC	LPDT9040	288	
FSC	LPDT9041	182	
FSC	LPDT9042	182	A AND B ARE CONNECTED
FSC	MWL908	144	
FSC	MWL909	217	
FSC	MWL910	140	
FSC	MWL911	213	
FSC	MWL912	135	
FSC	MWL913	240	
FSC	MWL921	140	NO PULL-UP RESISTOR
FSC	SE101	198	
FSC	SE102	198	
FSC	SE105	113	
FSC	SE110	200	
FSC	SE115	198	
FSC	SE124	231	
FSC	SE150	197	
FSC	SE160	174	
FSC	SH2100		
FSC	SH2101		
FSC	TTL103	205	
FSC	TTL104	205	
GELM	473104	546	
GELM	7736078	547	
GELM	7736079	115	
GELM	7736134	545	
GELM	7739750	543	
GESP	4JPA107	560	
GESP	4JPA113	504	SHORT OUT R2
GESP	4JPA114	504	SHORT OUT R1,R2
GESP	4JPA126	504	
GESP	12X101	198	
GESP	12X218	536	
GESP	12X248	171	
GESP	12X2071	501	
GESP	12X2072	501	
GESP	4JPA112	539	
GESP	4JPA135	560	

(continued)

MFR	MFRS PART NUMBER	FIG NO.	EXCEPTIONS
GESP	4JPA345	292	
GESP	4JPA358	292	
GI	MEM503	263	
GI	MEM507		
GI	MEM508		
GI	MEM509		
GI	MEM522	263	
GI	MEM529	264	
GI	MEM900	265	
GI	MEM901	266	
GI	MEM1000		
GI	MEM2001	268	
GI	MEM3020		
GI	MEM3021		
GI	MEM4000	267	
GI	MEM5001	268	
GI	MEM5002	268	
GI	MEM5003	268	
GI	MEM5005	268	
GI	MEM5006	268	
GI	NC10	221	
GI	NC11	201	
GI	NCPC8	239	S2,S3,C2,C3 OMITTED
GI	NCPC9	253	
GI	NCPC12	123	
GI	NCPC16	172	
GI	NCPC17	248	
GI	NCPC101	540	
GI	NCPC511	261	PNP TRNSTRS,REV DIODES
GI	NCPC513	261	
GI	NCS675A		
GI	PC10	221	
GI	PC11	201	
GI	PC13	239	
GI	PC14	221	
GI	PC15	201	
GI	PC18	172	
GI	PC200	508	
GI	PC201	509	
GI	PC210	551	
GI	PC212	551	
GI	PC250		
GI	PC251		
GI	PC401	254	
GI	PC402	255	
GI	PC501	260	
GI	PC502	260	
GI	PC503	260	PNP TRNSTRS,REV DIODES
GI	PC504	260	PNP TRNSTRS,REV DIODES
GI	PC512	261	
GI	PC514	261	PNP TRNSTRS,REV DIODES
GI	PC521	262	
GI	PC523	262	PNP TRNSTRS,REV DIODES
GME	134A	144	
GME	134B	217	
GME	134D2	140	
GME	134D3	140	
GME	134E	140	NO PULL-UP RESISTOR
GME	134G	213	
GME	134H	135	
GME	134R	240	
GME	254D3	113	A AND B INTRACONNECTED
GME	254DD	113	NO RESISTOR
GME	254G3	199	
GME	254G4	199	
GME	254G6	113	
GME	263Q	192	
GME	263Q2	192	
GME	264B	231	
GME	264B3	189	
GME	264B4	189	
GME	264D2	198	
GME	264D3	189	
GME	264D4	180	A AND B INTRACONNECTED
GME	264D5	198	NO PULL-UP RESISTOR
GME	264DR	198	A AND B INTRACONNECTED
GME	264E3	180	
GME	264E4	189	
GME	264G9	192	
GME	264JK		
GME	264L	197	
GME	264P	200	
GME	PL4C01	119	
GME	PL4G01	223	
GME	PL4G02	290	
GME	PL4G03	291	
GME	PL4M01	160	
GME	PL4R01	289	
GME	PL4R02		
GME	PL4S01	256	
GME	PL4S02	117	
GME	PL5050	120	
GME	PL5100	252	
HOFF	HMC001		
HOFF	HMC002		
HOFF	HMC003	197	
HOFF	HMC004	198	
HOFF	HMC005	231	
HOFF	HMC1001	198	
HOFF	HMC1002	197	

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MFR	MFRS PART NUMBER	FIG NO.	EXCEPTIONS
HOFF	HMC1003	231	
INTX	DMXXXXX	173	
INTX	FFXXXXX	229	
INTX	GBXXXXX	124	
INTX	GGXXXXX	220	
INTX	MVXXXXX	168	
INTX	STXXXXX	247	
MEPC	640702		
MEPC	640703	229	
MEPC	640704	229	
MOTA	MC201	198	
MOTA	MC202	198	
MOTA	MC203	113	
MOTA	MC204	200	
MOTA	MC205	197	
MOTA	MC206	198	
MOTA	MC207	198	NO PULL-UP RESISTOR
MOTA	MC208	198	A AND B INTRACONNECTED
MOTA	MC209	234	
MOTA	MC212	196	NO PULL-UP RESISTOR
MOTA	MC213	196	
MOTA	MC215	113	A AND B INTRACONNECTED
MOTA	MC217	113	NO RESISTOR
MOTA	MC251	198	
MOTA	MC252	198	
MOTA	MC253	113	
MOTA	MC254	200	
MOTA	MC255	197	
MOTA	MC256	198	
MOTA	MC257	198	NO PULL-UP RESISTOR
MOTA	MC258	198	A AND B INTRACONNECTED
MOTA	MC259	231	
MOTA	MC260	231	
MOTA	MC262	196	NO PULL-UP RESISTOR
MOTA	MC263	196	
MOTA	MC265	113	A AND B INTRACONNECTED
MOTA	MC267	113	NO RESISTOR
MOTA	MC301	211	
MOTA	MC302	241	
MOTA	MC303	128	
MOTA	MC304	246	
MOTA	MC305	138	
MOTA	MC306	211	
MOTA	MC307	211	OUTPUT RESISTORS OMITTED
MOTA	MC308	154	
MOTA	MC309	216	
MOTA	MC310	216	R2 OMITTED
MOTA	MC311	216	R1,R2 OMITTED
MOTA	MC312	216	
MOTA	MC351	211	

MFR	MFRS PART NUMBER	FIG NO.	EXCEPTIONS
MOTA	MC352	241	
MOTA	MC353	128	
MOTA	MC354	246	
MOTA	MC355	138	ND OMITTED
MOTA	MC356	211	
MOTA	MC357	211	OUTPUT RESISTORS OMITTED
MOTA	MC358	154	
MOTA	MC359	216	
MOTA	MC360	216	R2 OMITTED
MOTA	MC361	216	R1,R2 OMITTED
MOTA	MC362	216	
MOTA	MC401	205	
MOTA	MC402	205	
MOTA	MC650	183	
MOTA	MC651	183	
MOTA	MC652	259	
MOTA	MC800	142	
MOTA	MC801	118	
MOTA	MC802	226	
MOTA	MC803	140	
MOTA	MC804	129	
MOTA	MC805	249	
MOTA	MC806	249	INVERTING STAGE OMITTED
MOTA	MC807	140	
MOTA	MC814	140	
MOTA	MC815	140	
MOTA	MC816	155	
MOTA	MC830F	192	
MOTA	MC830G	192	
MOTA	MC831F	149	
MOTA	MC831G	149	
MOTA	MC832F	187	
MOTA	MC832G	187	
MOTA	MC833F	113	NO RESISTOR
MOTA	MC833G	113	NO RESISTOR
MOTA	MC844F	185	
MOTA	MC844G	185	
MOTA	MC845F	150	
MOTA	MC845G	150	
MOTA	MC846	192	
MOTA	MC848F	150	
MOTA	MC848G	150	
MOTA	MC862	192	
MOTA	MC900	142	
MOTA	MC901	118	
MOTA	MC902	226	
MOTA	MC903	140	
MOTA	MC904	129	
MOTA	MC905	249	
MOTA	MC906	249	INVERTING STAGE OMITTED

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MFR	MFRS PART NUMBER	FIG NO.	EXCEPTIONS
MOTA	MC907	140	
MOTA	MC908	144	
MOTA	MC909	217	
MOTA	MC910	140	
MOTA	MC911	213	
MOTA	MC912	135	
MOTA	MC913	240	
MOTA	MC914	140	
MOTA	MC915	140	
MOTA	MC916	155	
MOTA	MC918	140	
MOTA	MC921	140	
MOTA	MC930F	192	
MOTA	MC930G	192	
MOTA	MC931F	149	
MOTA	MC931G	149	
MOTA	MC932F	187	
MOTA	MC932G	187	
MOTA	MC933F	113	NO RESISTOR
MOTA	MC933G	113	NO RESISTOR
MOTA	MC944F	185	
MOTA	MC944G	185	
MOTA	MC945F	150	
MOTA	MC945G	150	
MOTA	MC946	192	
MOTA	MC948F	150	
MOTA	MC948G	150	
MOTA	MC962	192	
MOTA	MC1111	111	
MOTA	MC1112	111	
MOTA	MC1113	111	
MOTA	MC1114	113	A AND B INTRACONNECTED
MOTA	MC1115	143	
MOTA	MC1116	113	NO RESISTOR
MOTA	MC1117	113	REV DIODES,NO RESISTOR
MOTA	MC1118	121	
MOTA	MC1519A	510	
MOTA	MC1519B	510	
MOTA	MC1524	505	
MOTA	MC1525	511	NPN DEVICES
MOTA	MC1526	512	NPN DEVICES
MOTA	MC1527	511	
MOTA	MC1528	512	
MOTA	MC1530	513	OMIT Q1,Q5 INPUT TO Q2,Q4
MOTA	MC1531	513	
NORD	NM1003	548	
NORD	NM1005	549	
NORD	NM1008	548	
NORD	NM2002	550	
NORD	NM2007	550	
NORD	NM2012	550	
NORD	NM4002	141	
NSC	NB1000	142	
NSC	NB1001	118	
NSC	NB1002	226	
NSC	NB1003	140	
NSC	NB1004	129	
NSC	NB1005	249	
NSC	NB1007	140	
NSC	NB1014	140	
NSC	NB1015	140	
NSC	NB1017	140	
NSC	NB1018	242	
NSC	NB1019	226	
NSC	NB1020	243	
NSC	NB1023	130	
NSC	NB2000	142	
NSC	NB2001	118	
NSC	NB2002	226	
NSC	NB2003	140	
NSC	NB2004	129	
NSC	NB2005	249	
NSC	NB2007	140	
NSC	NB2014	140	
NSC	NB2015	140	
NSC	NB2017	140	
NSC	NB2018	242	
NSC	NB2019	226	
NSC	NB2020	243	
NSC	NB2023	227	
NSC	NC1008	144	
NSC	NC1009	217	
NSC	NC1010	140	
NSC	NC1011	213	
NSC	NC1012	135	
NSC	NC1021	140	NO PULL-UP RESISTOR
NSC	NC2008	144	
NSC	NC2009	217	
NSC	NC2010	140	
NSC	NC2011	213	
NSC	NC2012	135	
NSC	NC2021	140	NO PULL-UP RESISTOR
NSC	NS7037	514	
PHIL	PA702	516	
PHIL	PA710	553	
PHIL	PA712	515	
PHIL	PA713	534	
PHIL	PA7600	558	
PHIL	PA7601	559	
PHIL	PL103	205	

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MFR	MFRS PART NUMBER	FIG NO.	EXCEPTIONS
PHIL	PL104	205	
PHIL	PL900	142	
PHIL	PL901	118	
PHIL	PL902	226	
PHIL	PL903	140	
PHIL	PL904	129	
PHIL	PL905	249	
PHIL	PL906	249	INVERTING STAGE OMITTED
PHIL	PL907	140	
PHIL	PL908	144	
PHIL	PL909	217	
PHIL	PL910	140	
PHIL	PL911	213	
PHIL	PL912	135	
PHIL	PL913	240	
PHIL	PL914	140	
PHIL	PL915	140	
PHIL	PL916	155	
PHIL	PL921	140	NO PULL-UP RESISTOR
PHIL	PL930	192	
PHIL	PL931	149	
PHIL	PL932	189	
PHIL	PL933	113	NO RESISTOR
PHIL	PL939	140	
PHIL	PL940	155	
PHIL	PL944	185	
PHIL	PL945	150	
PHIL	PL946	192	
PHIL	PL948		
PHIL	PL949	192	
PHIL	PL961	192	
PHIL	PL962		
PHIL	PL963		
PHIL	PL975	144	
PHIL	PL976	217	
PHIL	PL977	140	
PHIL	PL978	140	
PHIL	PL979	140	NO PULL-UP RESISTOR
PHIL	PL980	213	
PHIL	PL981	135	
PHIL	PL983	140	
PHIL	PL984	240	
PHIL	PL985	140	
PHIL	PL9600	278	
PHIL	PL9602	217	
PHIL	PL9603	218	NO CAPACITORS
PHIL	PL9605	279	
PHIL	PL9606	275	
PHIL	PL9608	192	
PHIL	PL9609	217	
PHIL	PL9610	276	
PHIL	PL9611	277	
PHIL	PL9923	280	
PHIL	PL9926	153	
PHIL	PL9940	281	
PHIL	PL9974	153	
PHIL	PL9986	273	
PHIL	PL9987	273	
PHIL	PL9988	274	
RAD	RD205	196	NO PULL-UP RESISTOR
RAD	RD206	196	NO PULL-UP RESISTOR
RAD	RD208	245	
RAD	RD209	186	
RAD	RD210	196	NO PULL-UP RESISTOR
RAD	RD305	196	NO PULL-UP RESISTOR
RAD	RD306	196	NO PULL-UP RESISTOR
RAD	RD308	245	
RAD	RD309	186	
RAD	RD310	196	NO PULL-UP RESISTOR
RAD	RD505	196	NO PULL-UP RESISTOR
RAD	RD506	196	NO PULL-UP RESISTOR
RAD	RD508	245	
RAD	RD509	186	
RAD	RD510	196	NO PULL-UP RESISTOR
RAD	RM10	269	
RAD	RM12	269	
RAD	RM30	269	
RAD	RM31	269	
RAD	RM50	269	
RAD	RM53	269	
RAD	RM56	269	
RAD	RM59	269	
RAD	RM62	269	
RAD	RM65	269	
RAD	RM68	269	
RAD	RM71	269	
RAD	RM74	269	
RAY	RM201	196	NO PULL-UP RESISTOR
RAY	RM202	245	
RAY	RM204	196	NO PULL-UP RESISTOR
RAY	RM206	196	NO PULL-UP RESISTOR
RAY	RM210	179	
RAY	RM211	196	NO PULL-UP RESISTOR
RAY	RM212	245	
RAY	RM213	233	
RAY	RM214	196	NO PULL-UP RESISTOR
RAY	RM215	167	
RAY	RM216	196	
RAY	RM217	113	NO RESISTOR
RAY	RM221	196	NO PULL-UP RESISTOR

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MFR	MFRS PART NUMBER	FIG NO.	EXCEPTIONS
RAY	RM224	196	NO PULL-UP RESISTOR
RAY	RM227	113	NO RESISTOR
RAY	RM231	196	NO PULL-UP RESISTOR
RCA	CA3000	516	
RCA	CA3001	517	
RCA	CA3002	518	
RCA	CA3004	519	
RCA	CA3005	519	SHORT OUT R6,R7
RCA	CA3006	519	SHORT OUT R6,R7
RCA	CA3007	520	
RCA	CA3008	521	
RCA	CA3010	521	
RCA	CD2100	209	
RCA	CD2101	209	
RCA	CD2150	210	
RCA	CD2151	210	
RCA	CD2152	214	
RCA	CD2200	188	
RCA	CD2201	188	
RCA	CD2203	151	
SIGN	CS700	198	NO PULL-UP RESISTOR
SIGN	CS701	198	A AND B INTRACONNECTED
SIGN	CS704	231	
SIGN	CS705	113	A AND B INTRACONNECTED
SIGN	CS709	113	NO RESISTOR
SIGN	CS715	197	
SIGN	CS716	180	
SIGN	CS720	192	NO PULL-UP RESISTOR
SIGN	CS721	192	NO PULL-UP RESISTOR
SIGN	CS727	192	
SIGN	CS729	231	
SIGN	CS730	192	
SIGN	CS731	113	NO RESISTOR
SIGN	CS732	113	NO RESISTOR
SIGN	LU300	138	
SIGN	LU305	114	
SIGN	LU306	114	
SIGN	LU314	222	
SIGN	LU315	222	
SIGN	LU316	222	
SIGN	LU320	156	
SIGN	LU331	224	
SIGN	LU332	224	
SIGN	SE101	198	
SIGN	SE102	198	
SIGN	SE105	113	
SIGN	SE106	113	NO RESISTOR
SIGN	SE110	200	
SIGN	SE111	180	A AND B INTRACONNECTED
SIGN	SE112	180	A AND B INTRACONNECTED
SIGN	SE113	180	A AND B INTRACONNECTED
SIGN	SE115	198	
SIGN	SE116	192	
SIGN	SE124	231	
SIGN	SE125	293	
SIGN	SE150	197	
SIGN	SE155	189	
SIGN	SE156	189	
SIGN	SE157	189	
SIGN	SE160	174	
SIGN	SE161	175	
SIGN	SE170	192	
SIGN	SE180	192	
SIGN	SE181	192	
SIGN	SE416	190	
SIGN	SE424	237	
SIGN	SE455	184	
SIGN	SE480	184	CR1 OMITTED
SIGN	SE500	533	
SIGN	SE501	541	
SIGN	SE505	522	
SIGN	SE506	562	
SIGN	SE518	561	
SIGN	SE806	139	
SIGN	SE808	205	R1 OFF GND AND TO OUTPUT
SIGN	SE816	205	R1 OFF GND AND TO OUTPUT
SIGN	SE825	294	
SIGN	SE840	295	
SIGN	SE855	205	
SIGN	SE870	205	R1 OFF GND AND TO OUTPUT
SIGN	SE880	205	R1 OFF GND AND TO OUTPUT
SIGN	SU300	138	
SIGN	SU305	114	
SIGN	SU306	114	
SIGN	SU314	222	
SIGN	SU315	222	
SIGN	SU316	222	
SIGN	SU320	156	
SIGN	SU331	224	
SIGN	SU332	224	
SILX	A01	202	
SILX	A02	202	
SILX	A03		
SILX	A04	113	NO RESISTOR
SILX	A05	202	
SILX	A06	202	
SILX	A07	202	
SILX	A08		
SILX	A09		
SILX	A10	202	

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MFR	MFRS PART NUMBER	FIG NO.	EXCEPTIONS
SILX	A12	202	
SILX	A13	202	
SILX	A14	202	
SILX	A15	202	
SILX	A20	202	
SPER	203	523	
SPER	900	142	
SPER	914	140	
SPER	915	140	
SPER	925	140	
SPER	926	153	
SPRG	US-0100	235	R1,C1,Q1 OMITTED
SPRG	US-0101	235	R1,C1,Q1 OMITTED
SPRG	US-0102	218	
SPRG	US-0103	218	
SPRG	US-0104	218	
SPRG	US-0105	130	
SPRG	US-0106	218	
SPRG	US-0107	125	
SPRG	US-0108	177	
SPRG	US-0110	235	
SPRG	US-0111	235	
SPRG	US-0112	218	
SPRG	US-0113	218	
SPRG	US-0114	219	
SPRG	US-0115	219	
SPRG	US-0708	144	
SPRG	US-0709	217	
SPRG	US-0710	140	
SPRG	US-0711	213	
SPRG	US-0712	135	
SPRG	US-0713	240	
SPRG	US-0721	140	NO PULL-UP RESISTOR
SW	SW301	211	
SW	SW302	241	
SW	SW303	128	
SW	SW304	246	
SW	SW305	138	
SW	SW306	211	
SW	SW307	211	
SW	SW308	154	
SW	SW309	216	
SW	SW310	216	R2 OMITTED
SW	SW311	216	R1,R2 OMITTED
SW	SW930	192	
SW	SW931	149	
SW	SW932	189	
SW	SW933	113	NO RESISTOR
SW	SW944	185	
SW	SW945	150	
SW	SW946	192	
SW	SW948	150	
SW	SW962Y	192	
SW	SW962Z	192	
SW	SWF10	244	
SW	SWF11	244	
SW	SWF12	244	
SW	SWF13	244	
SW	SWF20	234	
SW	SWF21	234	
SW	SWF22	234	
SW	SWF23	234	
SW	SWF30	238	
SW	SWF31	238	
SW	SWF32	238	
SW	SWF33	238	
SW	SWF50	157	
SW	SWF51	157	
SW	SWF52	157	
SW	SWF53	157	
SW	SWG40	206	
SW	SWG41	206	
SW	SWG42	206	
SW	SWG43	206	
SW	SWG50	105	
SW	SWG51	105	
SW	SWG52	105	
SW	SWG53	105	
SW	SWG60	206	
SW	SWG61	206	
SW	SWG62	206	
SW	SWG63	206	
SW	SWG90	131	
SW	SWG91	131	
SW	SWG92	131	
SW	SWG93	131	
SW	SWG100	105	
SW	SWG101	105	
SW	SWG102	105	
SW	SWG103	105	
SW	SWG110	105	
SW	SWG111	105	
SW	SWG112	105	
SW	SWG113	105	
SW	SWG120	206	
SW	SWG121	206	
SW	SWG122	206	
SW	SWG123	206	
SW	SWG130	206	
SW	SWG131	206	

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MFR	MFRS PART NUMBER	FIG NO.	EXCEPTIONS
SW	SWG132	206	
SW	SWG133	206	
SW	SWG140	193	
SW	SWG141	193	
SW	SWG142	193	
SW	SWG143	193	
SW	SWG150	258	
SW	SWG151	258	
SW	SWG152	258	
SW	SWG153	258	
SW	SWG170	139	
SW	SWG171	139	
SW	SWG172	139	
SW	SWG173	139	
SW	SWG180	132	
SW	SWG181	132	
SW	SWG182	132	
SW	SWG183	132	
SYL	SF10	244	
SYL	SF11	244	
SYL	SF12	244	
SYL	SF13	244	
SYL	SF20	234	
SYL	SF21	234	
SYL	SF22	234	
SYL	SF23	234	
SYL	SF30	238	
SYL	SF31	238	
SYL	SF32	238	
SYL	SF33	238	
SYL	SF50	157	
SYL	SF51	157	
SYL	SF52	157	
SYL	SF53	157	
SYL	SF60		
SYL	SF61		
SYL	SF62		
SYL	SF63		
SYL	SF250	157	
SYL	SF251	157	
SYL	SF252	157	
SYL	SF253	157	
SYL	SF260		
SYL	SF261		
SYL	SF262		
SYL	SF263		
SYL	SG40	206	
SYL	SG41	206	
SYL	SG42	206	
SYL	SG43	206	

MFR	MFRS PART NUMBER	FIG NO.	EXCEPTIONS
SYL	SG50	105	
SYL	SG51	105	
SYL	SG52	105	
SYL	SG53	105	
SYL	SG60	206	
SYL	SG61	206	
SYL	SG62	206	
SYL	SG63	206	
SYL	SG90	131	
SYL	SG91	131	
SYL	SG92	131	
SYL	SG93	131	
SYL	SG100	105	
SYL	SG101	105	
SYL	SG102	105	
SYL	SG103	105	
SYL	SG110	105	
SYL	SG111	105	
SYL	SG112	105	
SYL	SG113	105	
SYL	SG120	206	
SYL	SG121	206	
SYL	SG122	206	
SYL	SG123	206	
SYL	SG130	205	
SYL	SG131	205	
SYL	SG132	205	
SYL	SG133	205	
SYL	SG140	206	
SYL	SG141	206	
SYL	SG142	206	
SYL	SG143	206	
SYL	SG150	258	
SYL	SG152	258	
SYL	SG160	271	
SYL	SG161	271	
SYL	SG162	271	
SYL	SG163	271	
SYL	SG170	139	
SYL	SG172	139	
SYL	SG180	132	
SYL	SG181	132	
SYL	SG182	132	
SYL	SG183	132	
SYL	SG190	206	
SYL	SG191	206	
SYL	SG192	206	
SYL	SG193	206	
SYL	SG210	272	
SYL	SG211	272	

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MFR	MFRS PART NUMBER	FIG NO.	EXCEPTIONS
SYL	SG212	272	
SYL	SG213	272	
SYL	SG220	205	
SYL	SG221	205	
SYL	SG222	205	
SYL	SG223	205	
SYL	SG230	258	
SYL	SG232	258	
SYL	SG240	205	
SYL	SG241	205	
SYL	SG242	205	
SYL	SG243	205	
SYL	SG250	272	
SYL	SG251	272	
SYL	SG252	272	
SYL	SG253	272	
SYL	SG260	205	
SYL	SG261	205	
SYL	SG262	205	
SYL	SG263	205	
SYL	SG270	139	
SYL	SG272	139	
TI	SN337	228	
TI	SN341	204	
TI	SN343	161	
TI	SN344	196	NO PULL-UP RESISTOR
TI	SN346	162	
TI	SN347	204	
TI	SN359	204	
TI	SN472		
TI	SN510	235	R1,C1,Q1 OMITTED
TI	SN511	235	R1,C1,Q1 OMITTED
TI	SN512	218	
TI	SN513	218	
TI	SN514	218	
TI	SN515	130	
TI	SN516	218	
TI	SN517	125	
TI	SN518	177	
TI	SN521	524	
TI	SN522	525	
TI	SN523	526	
TI	SN524	527	
TI	SN525		
TI	SN526		
TI	SN530	165	R4,Q1 OMITTED
TI	SN531	108	
TI	SN532	112	
TI	SN533	108	
TI	SN534	112	
TI	SN535	147	
TI	SN729		
TI	SN730	140	
TI	SN731	140	
TI	SN732		
TI	SN733		
TI	SN734		
TI	SN735		
TI	SN1005	176	
TI	SN5101	235	
TI	SN5111	235	
TI	SN5112	235	R1,C1,Q1 OMITTED
TI	SN5161	218	
TI	SN5162	218	
TI	SN5191	133	
TI	SN5302	165	R4,Q1 OMITTED
TI	SN5304	165	
TI	SN5311	194	
TI	SN5331	194	
TI	SN5360	194	
TI	SN5370	136	
TI	SN5380	176	
TI	SN5400	195	
TI	SN5410	195	
TI	SN5420	195	
TI	SN5430	195	
TI	SN5440	205	
TI	SN5450	137	
TI	SN5460	139	
TI	SN5470		
TI	SN5500	535	
TI	SN5510	528	
TI	SN7000	208	
TI	SN7300	165	R4,Q1 OMITTED
TI	SN7301	165	
TI	SN7302	165	R4,Q1 OMITTED
TI	SN7304	165	
TI	SN7310	194	
TI	SN7311	194	
TI	SN7320	138	PNP DEVICES
TI	SN7330	194	
TI	SN7331	194	
TI	SN7350	147	
TI	SN7360	194	
TI	SN7370	136	
TI	SN7380	176	
TI	SN7400	195	
TI	SN7410	195	
TI	SN7420	195	
TI	SN7430	195	

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MFR	MFRS PART NUMBER	FIG NO.	EXCEPTIONS
TI	SN7440	205	
TI	SN7450	137	
TI	SN7460	139	
TI	SN7470		
TRAN	TFF3011	234	
TRAN	TFF3012	234	
TRAN	TFF3013	234	
TRAN	TFF3014	234	
TRAN	TFF3015	234	GATES ARE 2 INP PLUS CLCK
TRAN	TFF3016	234	GATES ARE 2 INP PLUS CLCK
TRAN	TFF3017	234	GATES ARE 2 INP PLUS CLCK
TRAN	TFF3018	234	GATES ARE 2 INP PLUS CLCK
TRAN	TFF3031	234	GATES ARE1-2INP PLUS CLCK
TRAN	TFF3111	158	GATES ARE 4 INP PLUS CLCK
TRAN	TFF3112	158	GATES ARE 4 INP PLUS CLCK
TRAN	TFF3113	158	GATES ARE 4 INP PLUS CLCK
TRAN	TFF3114	158	GATES ARE 4 INP PLUS CLCK
TRAN	TFF3115	158	
TRAN	TFF3116	158	
TRAN	TFF3117	158	
TRAN	TFF3118	158	
TRAN	TFF3121	282	GATES ARE 4 INP PLUS CLCK
TRAN	TFF3122	282	GATES ARE 4 INP PLUS CLCK
TRAN	TFF3123	282	GATES ARE 4 INP PLUS CLCK
TRAN	TFF3124	282	GATES ARE 4 INP PLUS CLCK
TRAN	TFF3125	282	
TRAN	TFF3126	282	
TRAN	TFF3127	282	
TRAN	TFF3128	282	
TRAN	TFF3131	282	
TRAN	TFF3211	157	
TRAN	TFF3212	157	
TRAN	TFF3213	157	
TRAN	TFF3214	157	
TRAN	TFF3251	157	
TRAN	TFF3252	157	
TRAN	TFF3253	157	
TRAN	TFF3254	157	
TRAN	TFF3512	283	
TRAN	TFF3514	283	
TRAN	TNG3011	206	
TRAN	TNG3012	206	
TRAN	TNG3013	206	
TRAN	TNG3014	206	
TRAN	TNG3015	206	
TRAN	TNG3016	206	
TRAN	TNG3017	206	
TRAN	TNG3018	206	
TRAN	TNG3031	206	
TRAN	TNG3041	206	
TRAN	TNG3042	206	
TRAN	TNG3043	206	
TRAN	TNG3044	206	
TRAN	TNG3045	206	
TRAN	TNG3046	206	
TRAN	TNG3047	206	
TRAN	TNG3048	206	
TRAN	TNG3051	206	
TRAN	TNG3052	206	
TRAN	TNG3053	206	
TRAN	TNG3054	206	
TRAN	TNG3111	206	
TRAN	TNG3112	206	
TRAN	TNG3113	206	
TRAN	TNG3114	206	
TRAN	TNG3115	206	
TRAN	TNG3116	206	
TRAN	TNG3117	206	
TRAN	TNG3118	206	
TRAN	TNG3131	206	
TRAN	TNG3141	206	
TRAN	TNG3142	206	
TRAN	TNG3143	206	
TRAN	TNG3144	206	
TRAN	TNG3145	206	
TRAN	TNG3146	206	
TRAN	TNG3147	206	
TRAN	TNG3148	206	
TRAN	TNG3211	105	
TRAN	TNG3212	105	
TRAN	TNG3213	105	
TRAN	TNG3214	105	
TRAN	TNG3215	105	
TRAN	TNG3216	105	
TRAN	TNG3217	105	
TRAN	TNG3218	105	
TRAN	TNG3231	105	
TRAN	TNG3241	105	
TRAN	TNG3242	105	
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TRAN	TNG3244	105	
TRAN	TNG3245	105	
TRAN	TNG3246	105	
TRAN	TNG3247	105	
TRAN	TNG3248	105	
TRAN	TNG3251	105	
TRAN	TNG3252	105	
TRAN	TNG3253	105	
TRAN	TNG3254	105	
TRAN	TNG3311	206	

(continued)

MFR	MFRS PART NUMBER	FIG NO.	EXCEPTIONS
TRAN	TNG3312	206	
TRAN	TNG3313	206	
TRAN	TNG3314	206	
TRAN	TNG3331	206	
TRAN	TNG3411	206	
TRAN	TNG3412	206	
TRAN	TNG3413	206	
TRAN	TNG3414	206	
TRAN	TNG3431	206	DELETE DASHED LINE AREA
TRAN	TNG3511	132	
TRAN	TNG3512	132	
TRAN	TNG4011	139	
TRAN	TNG4012	139	
TRAN	TNG4031	132	
TRAN	TNG4131	206	
TRAN	TNG4211	105	
TRAN	TNG4212	105	
TRAN	TNG4213	105	
TRAN	TNG4214	105	
TRAN	TNG4251	105	
TRAN	TNG4252	105	
TRAN	TNG4253	105	
TRAN	TNG4254	105	
TRAN	TNG4311	105	
TRAN	TNG4312	105	
TRAN	TNG4313	105	
TRAN	TNG4314	105	
TRAN	TNG4315	105	
TRAN	TNG4316	105	
TRAN	TNG4317	105	
TRAN	TNG4318	105	
TRAN	TNG4415	105	
TRAN	TNG4416	105	
TRAN	TNG4417	105	
TRAN	TNG4418	105	
TRAN	TNG4511	258	
TRAN	TNG4512	258	
TRAN	TNG4611	131	
TRAN	TNG4612	131	
TRAN	TNG4613	131	
TRAN	TNG4614	131	
TRAN	TNG5121	206	
TRAN	TNG5122	206	
TRAN	TNG5123	206	
TRAN	TNG5124	206	
TRAN	TNG5221	206	
TRAN	TNG5222	206	
TRAN	TNG5223	206	
TRAN	TNG5224	206	
TRAN	TNG5321	206	DELETE DASHED LINE AREA
TRAN	TNG5322	206	DELETE DASHED LINE AREA
TRAN	TNG5421	206	DELETE DASHED LINE AREA
TRAN	TNG5422	206	DELETE DASHED LINE AREA
TRAN	TNG6222	284	
TRAN	TNG6224	284	
TRAN	TNG6252	285	
TRAN	TNG6254	285	
TRAN	TNG6262	284	
TRAN	TNG6264	284	
TRAN	TNG6522	284	
TRAN	TNG6524	284	
TRAN	TNG7252	286	
TRAN	TNG7254	286	
TRAN	TNG7712	287	
TRAN	TNG7812	287	
TRAN	TNG7912	287	
VARO	8102	220	
VARO	8105	230	
VARO	8107	229	
VARO	8200	232	
VARO	8201	101	
VARO	8202	101	
VARO	8203	178	
VARO	8204	215	
VARO	8205	225	
VARO	8207		
VARO	8208	110	
VARO	8209	110	
VARO	8210	110	
VARO	8213	126	
VARO	8214	203	
VARO	8502	502	
WMED	WC183	556	
WMED	WC201	196	NO PULL-UP RESISTOR
WMED	WC202	245	
WMED	WC204	196	NO PULL-UP RESISTOR
WMED	WC206	196	NO PULL-UP RESISTOR
WMED	WC208	164	
WMED	WC210	179	
WMED	WC211	196	NO PULL-UP RESISTOR
WMED	WC212	245	
WMED	WC213	233	
WMED	WC214	196	NO PULL-UP RESISTOR
WMED	WC215	167	
WMED	WC216	196	NO PULL-UP RESISTOR
WMED	WC217	113	NO RESISTOR
WMED	WC221	196	NO PULL-UP RESISTOR
WMED	WC224	196	NO PULL-UP RESISTOR
WMED	WC226	196	
WMED	WC227	113	NO RESISTOR

(continued)

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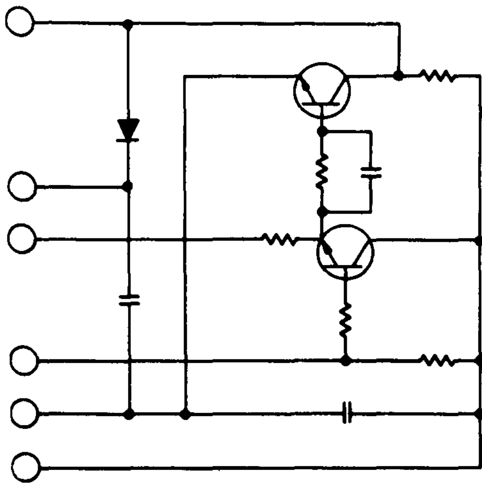
MFR	MFRS PART NUMBER	FIG NO.	EXCEPTIONS
WMED	WC231	196	NO PULL-UP RESISTOR
WMED	WC236	196	
WMED	WC241	196	
WMED	WC246	196	NO PULL-UP RESISTOR
WMED	WC261	196	
WMED	WC266	196	
WMED	WC286	196	NO PULL-UP RESISTOR
WMED	WC296	196	
WMED	WM169		
WMED	WM201	196	NO PULL-UP RESISTOR
WMED	WM202	245	
WMED	WM204	196	NO PULL-UP RESISTOR
WMED	WM206	196	NO PULL-UP RESISTOR
WMED	WM208	164	
WMED	WM210	179	
WMED	WM211	196	NO PULL-UP RESISTOR
WMED	WM212	245	
WMED	WM213	233	
WMED	WM214	196	NO PULL-UP RESISTOR
WMED	WM215	167	
WMED	WM216	196	NO PULL-UP RESISTOR
WMED	WM217	113	NO RESISTOR
WMED	WM221	196	NO PULL-UP RESISTOR
WMED	WM224	196	NO PULL-UP RESISTOR
WMED	WM225	270	
WMED	WM226	196	
WMED	WM227	113	NO RESISTOR
WMED	WM231	196	NO PULL-UP RESISTOR
WMED	WM234	196	
WMED	WM236	196	
WMED	WM241	196	
WMED	WM246	196	NO PULL-UP RESISTOR
WMED	WM261	196	
WMED	WM266	196	
WMED	WM286	196	NO PULL-UP RESISTOR
WMED	WM296	196	
WMED	WM503	159	
WMED	WM506	196	
WMED	WM510	191	
WMED	WM556	196	
WMED	WM701	205	
WMED	WM704	205	
WMED	WM1108	503	
WMED	WM1146	557	
WMED	WS107		
WMED	WS112	542	
WMED	WS115	529	
WMED	WS123	530	
WMED	WS141	531	R1,R2 OMITTED
WMED	WS142	531	R1,R2 OMITTED
WMED	WS143	531	
WMED	WS144	531	
WMED	WS150	163	
WMED	WS151	127	
WMED	WS161	532	
WMED	WS167		
WMED	WS174	555	
WMED	WS371	210	
WMED	WS374	210	
WMED	WS810	107	
WMED	WS811	179	
WMED	WS812	107	
WMED	WS813	102	
WMED	WS814	106	
WMED	WS815	166	
WMED	WS817	179	
WMED	WS840		
WMED	WS934	544	



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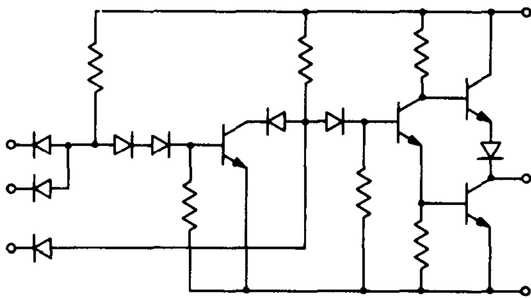

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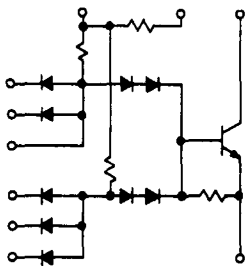

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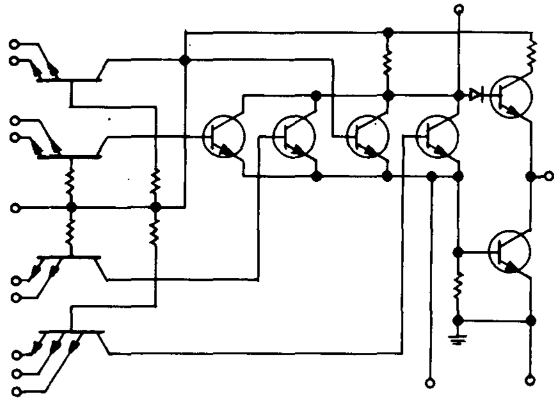

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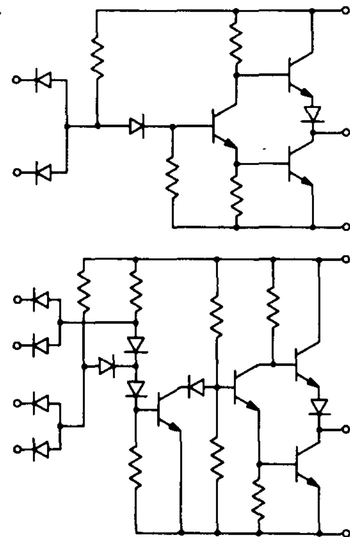

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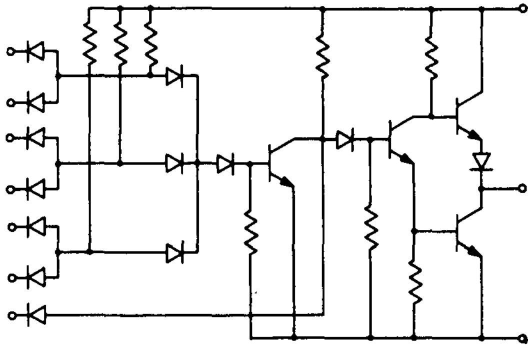

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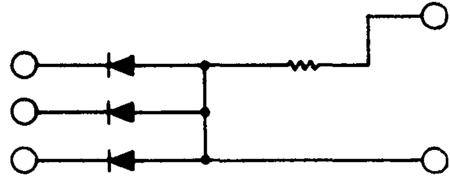

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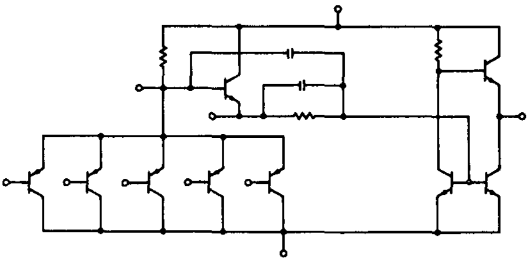

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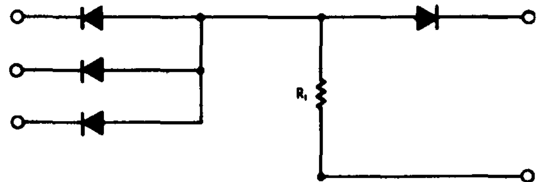

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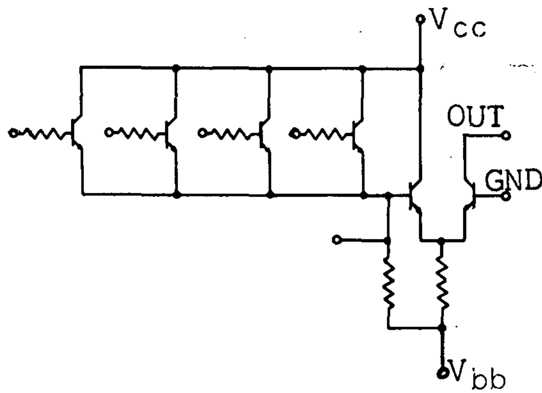

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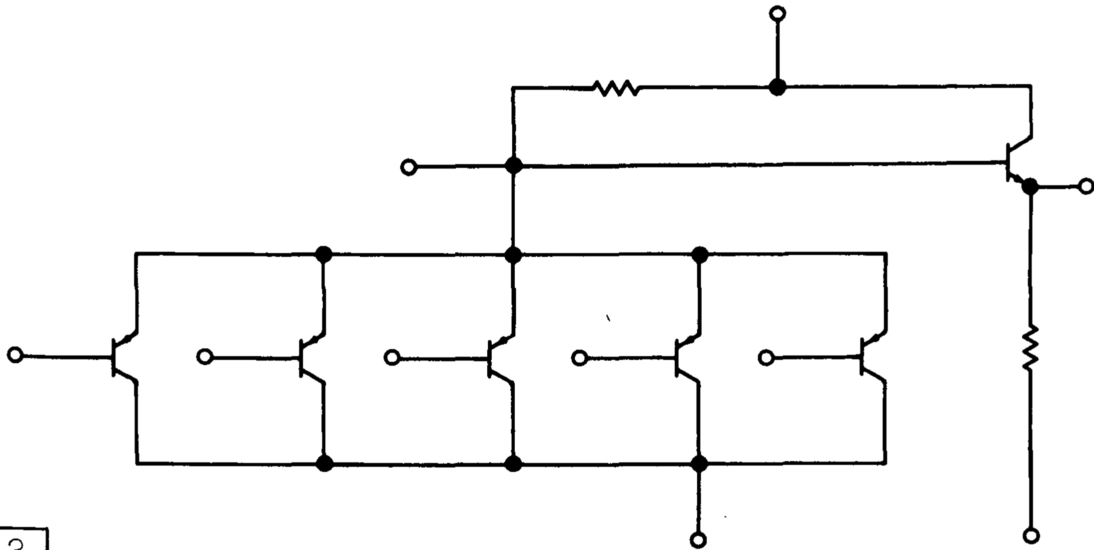

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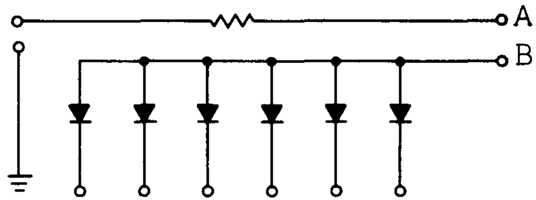

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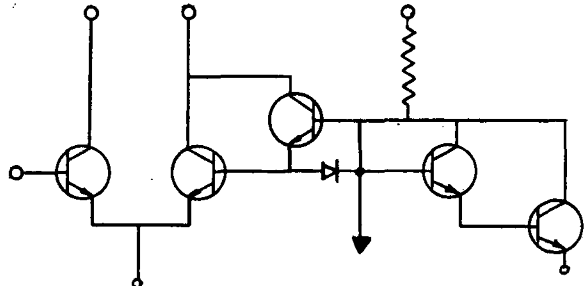
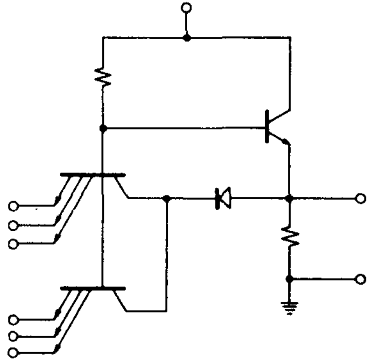


Schematic
for
one
stage
of
D/A
Converter

115



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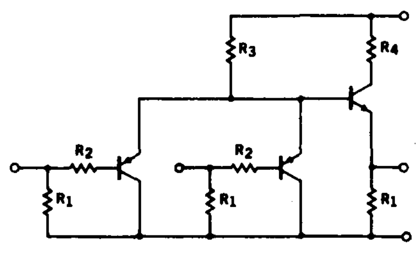

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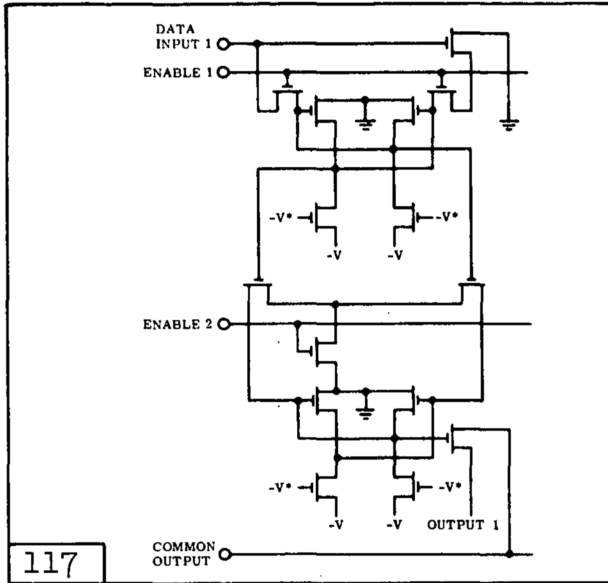
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-V*
-V
ENABLE 2
OUTPUT 1
COMMON
OUTPUT
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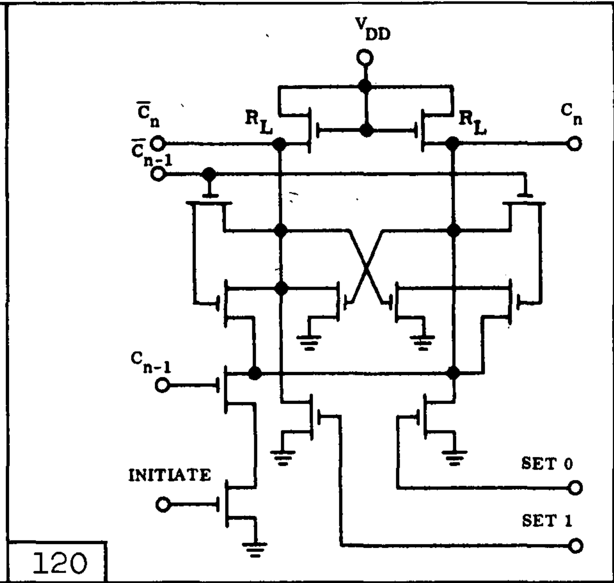
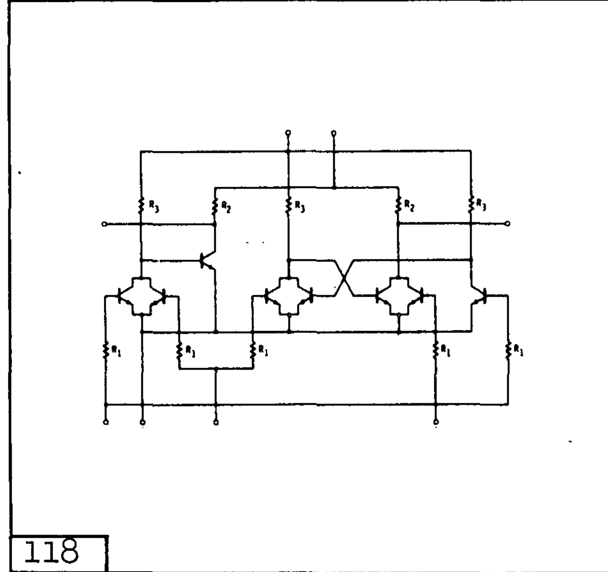

V_{DD}
$\overline{C}_n$
R_L
R_L
C_n
$\overline{C}_{n-1}$
C_{n-1}
INITIATE
SET 0
SET 1
120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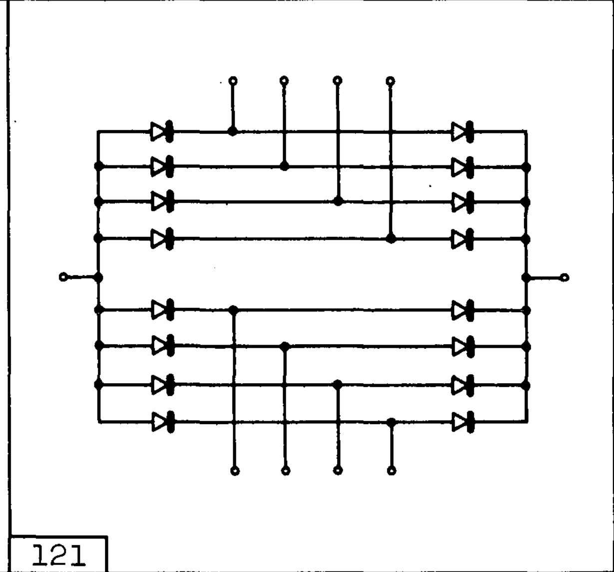
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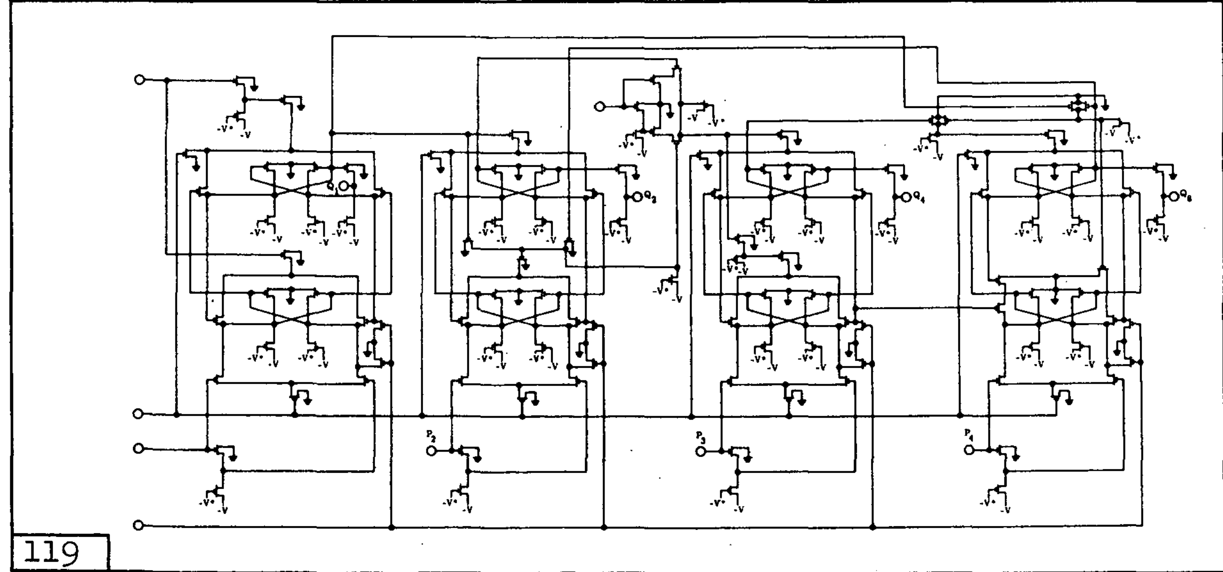
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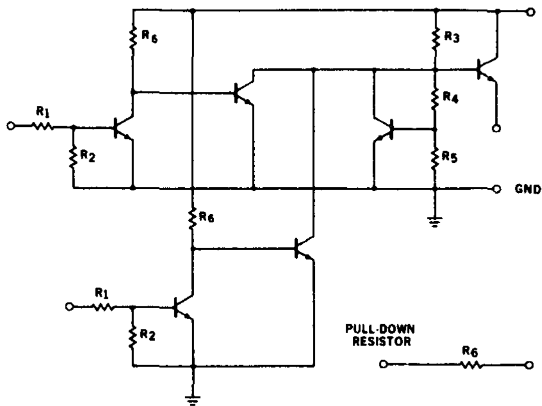

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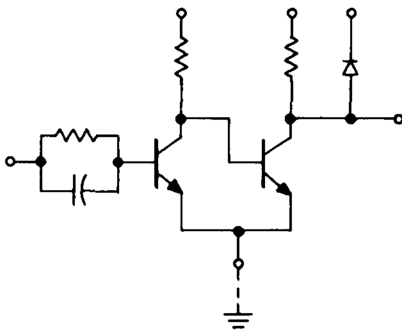

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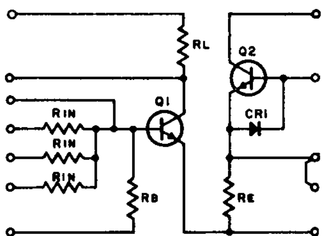

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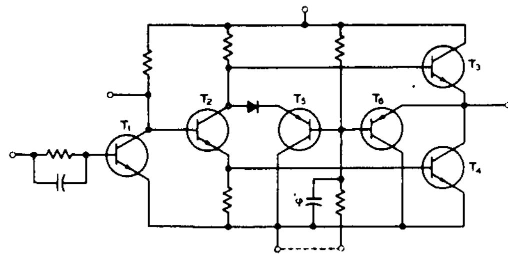

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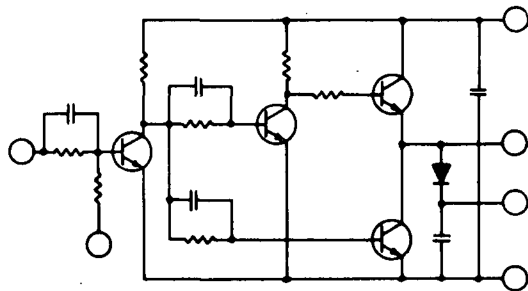

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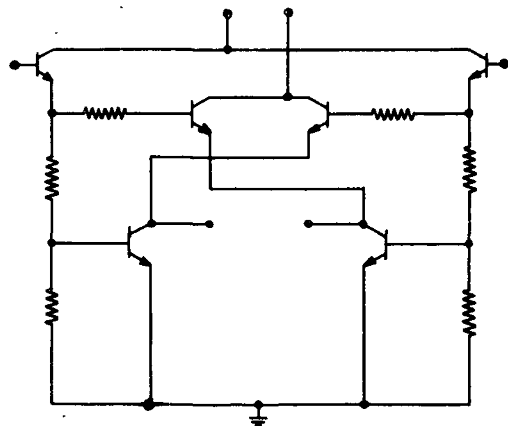

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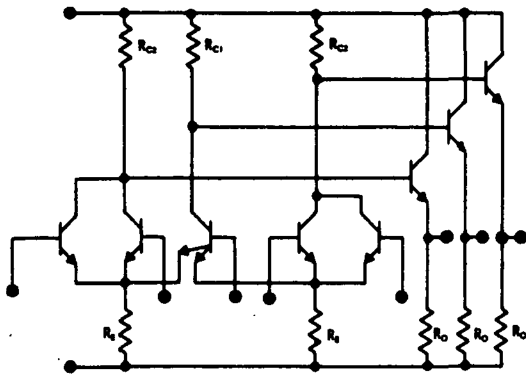

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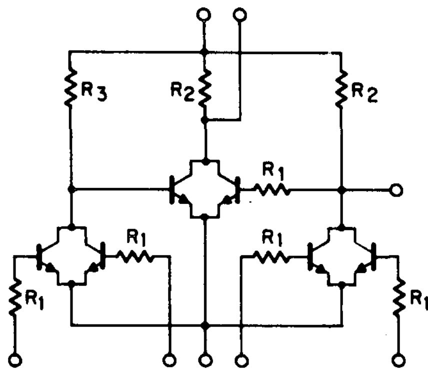

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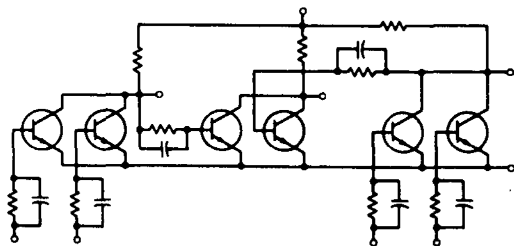

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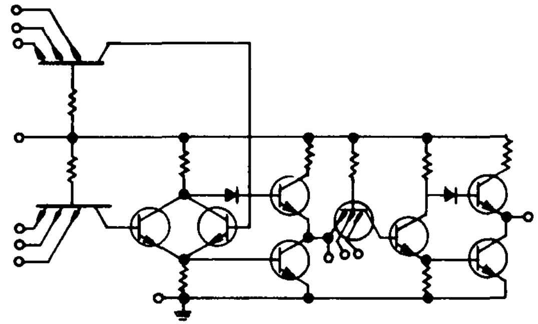

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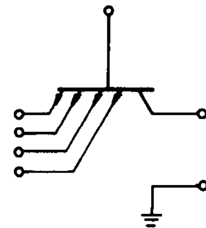

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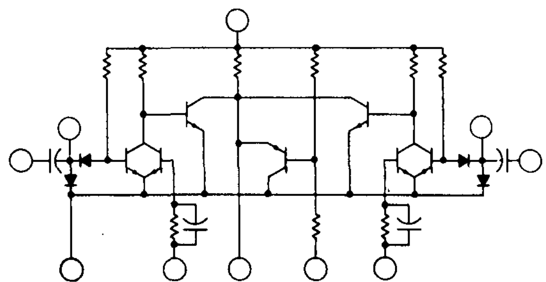

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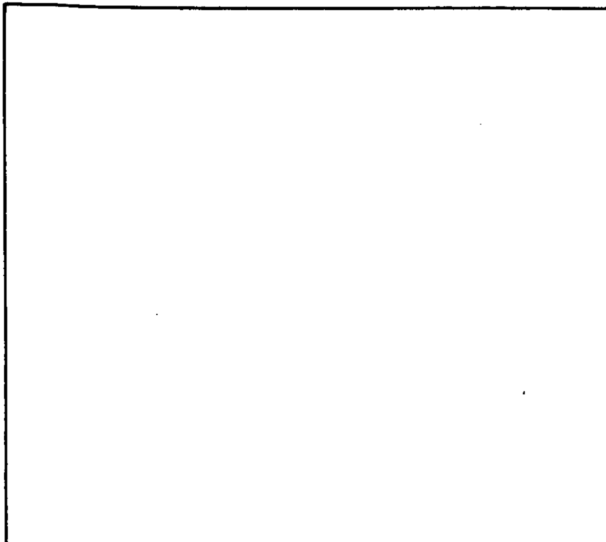
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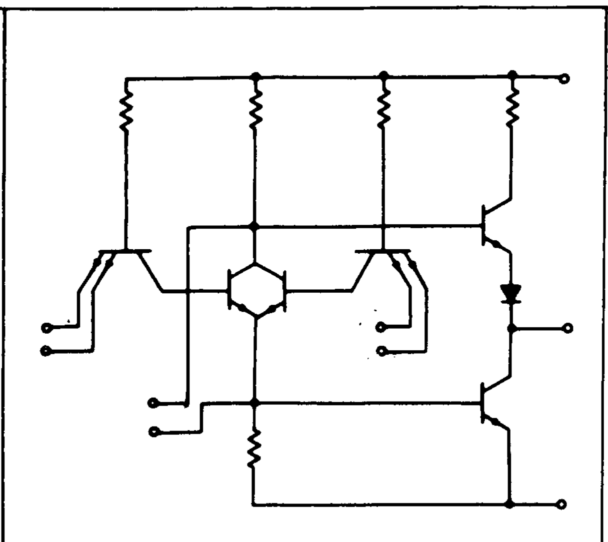
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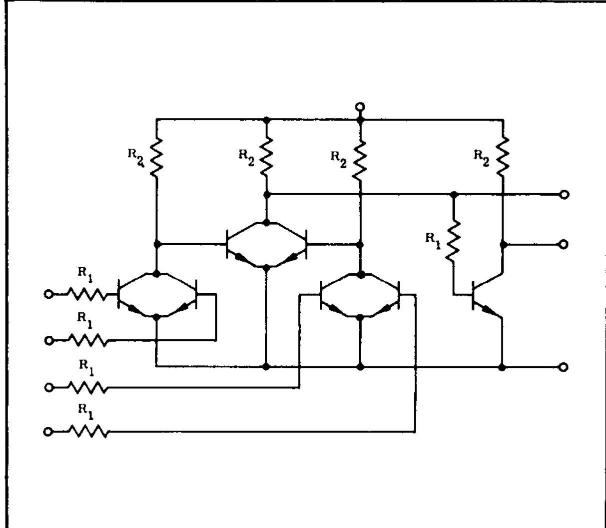
R2
R2
R2
R2
R1
R1
R1
R1
R1
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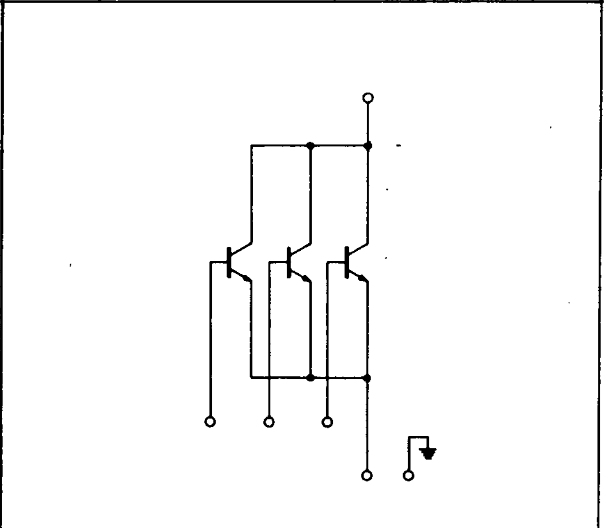
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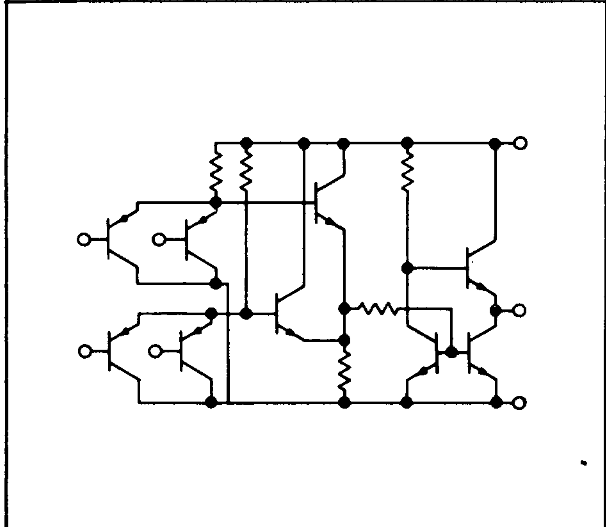
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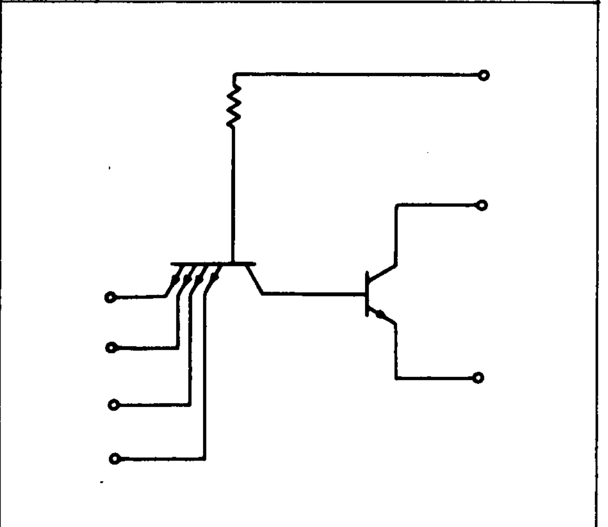
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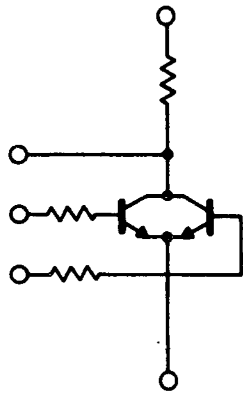

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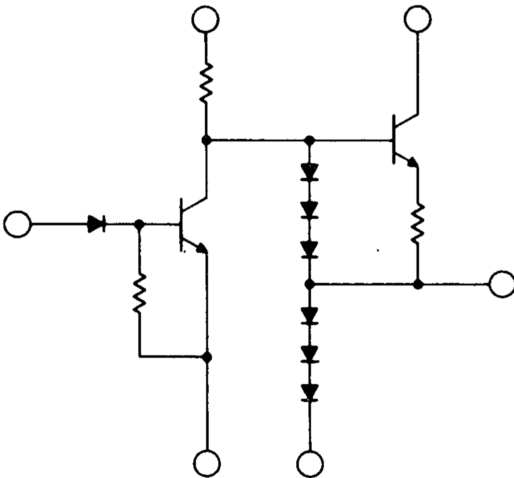

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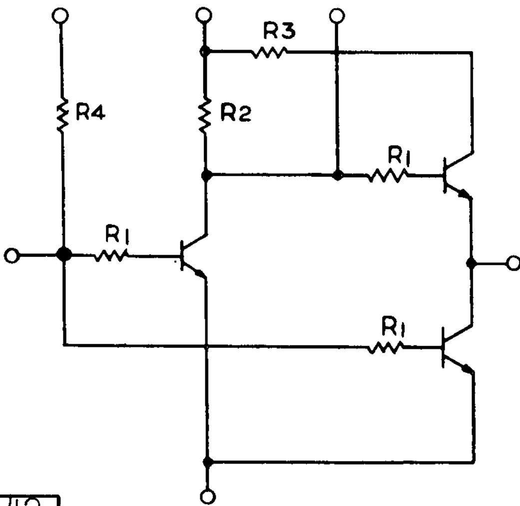

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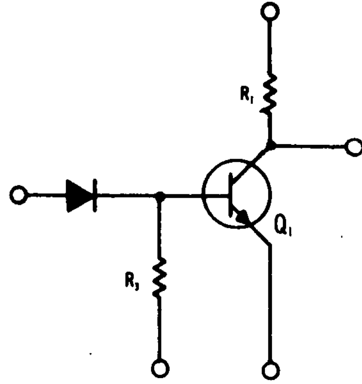

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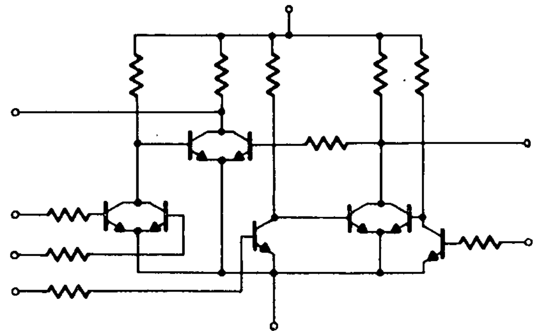

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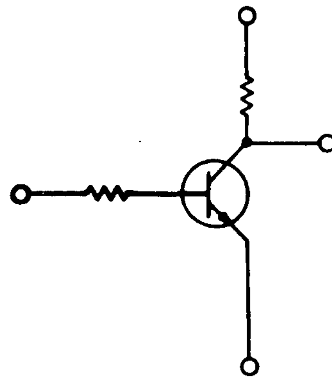

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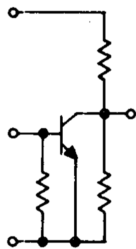

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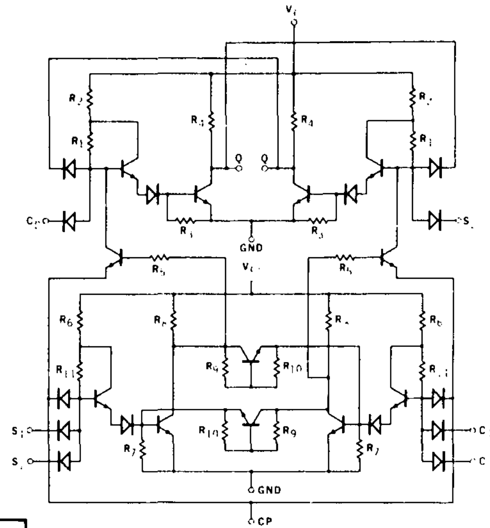

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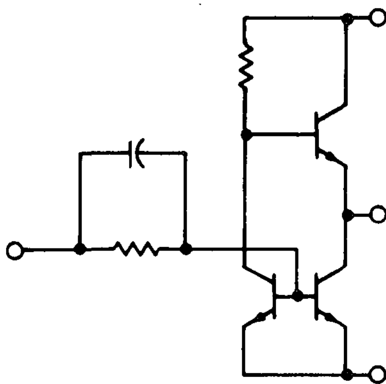

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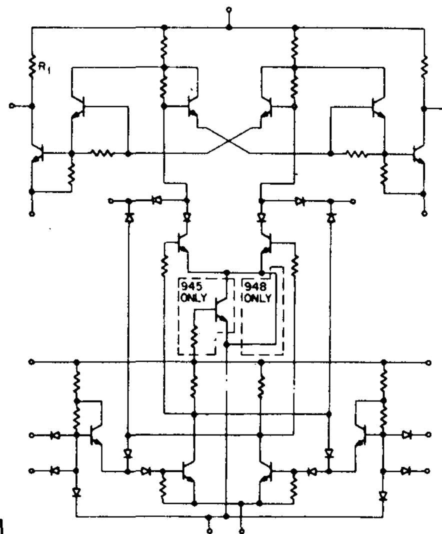

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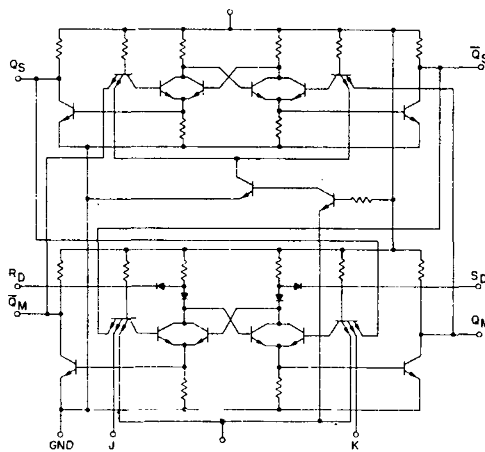

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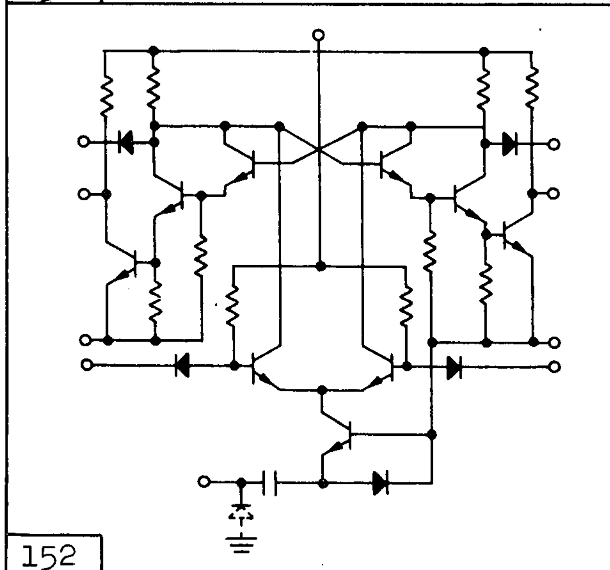

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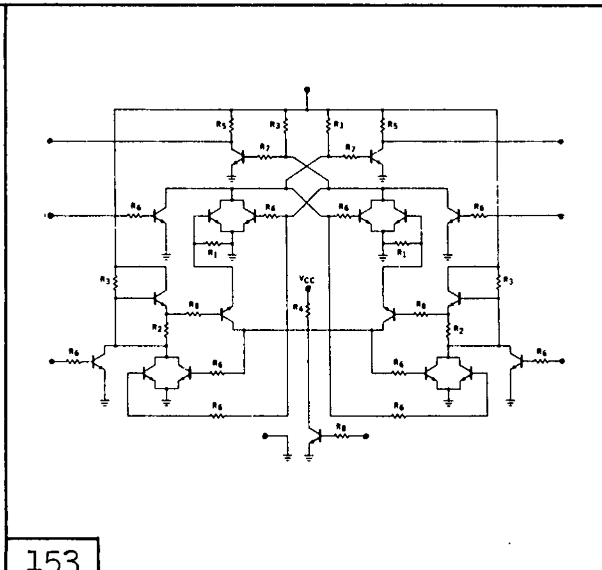

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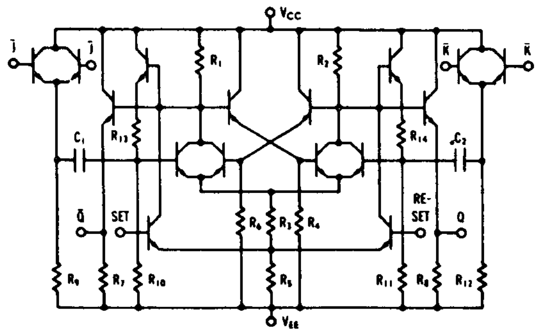

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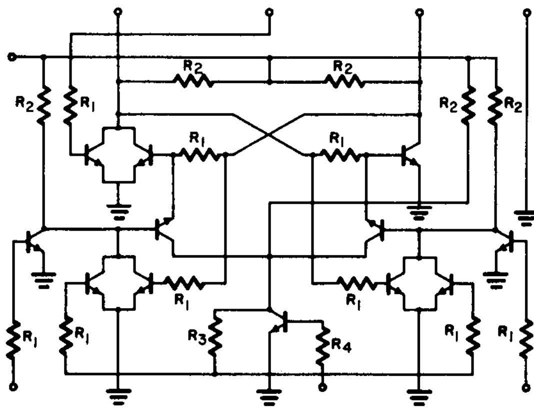

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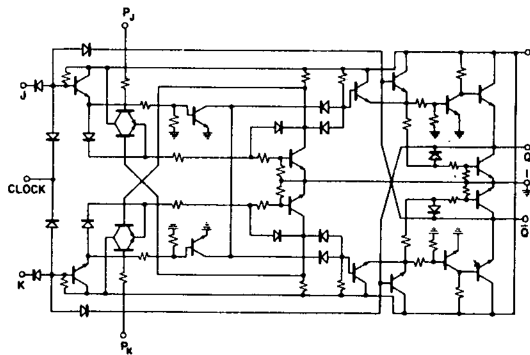

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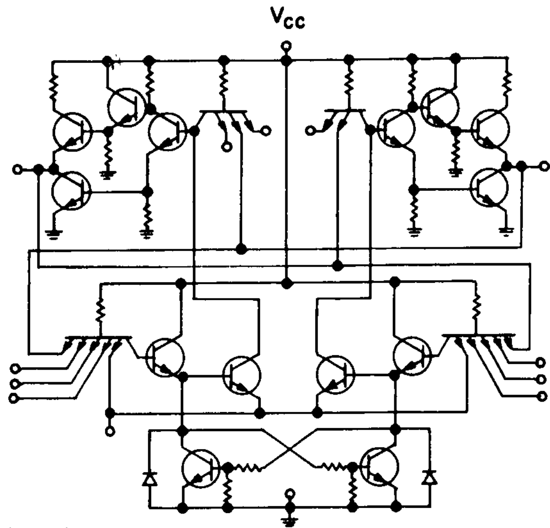

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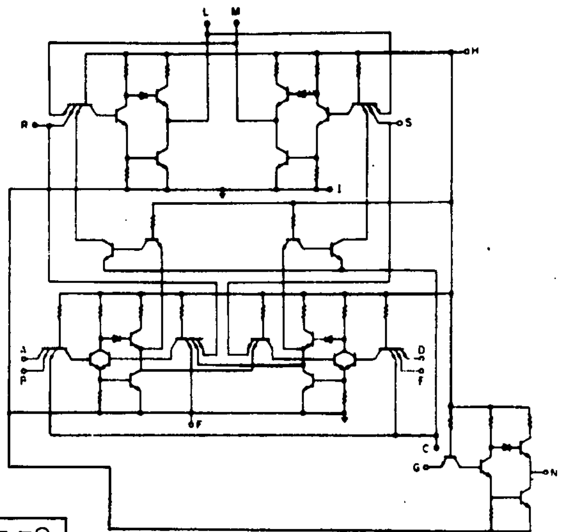

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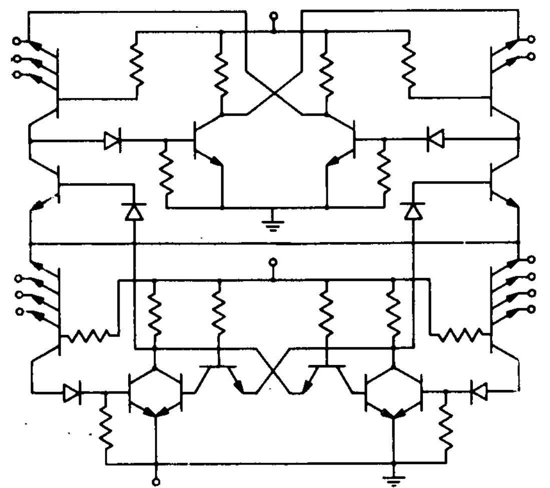

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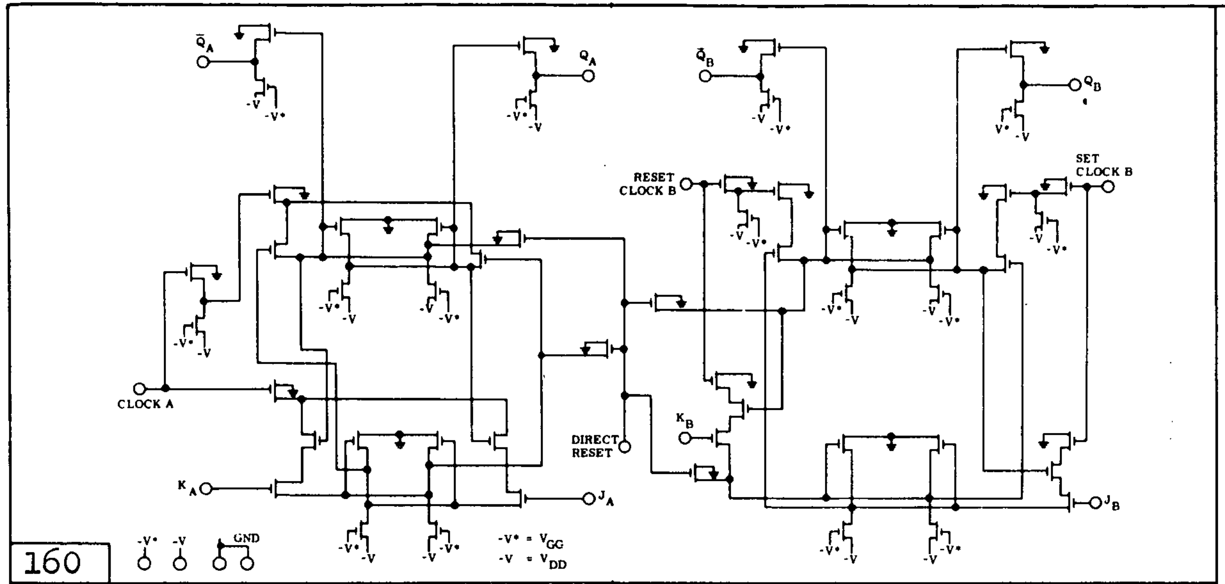
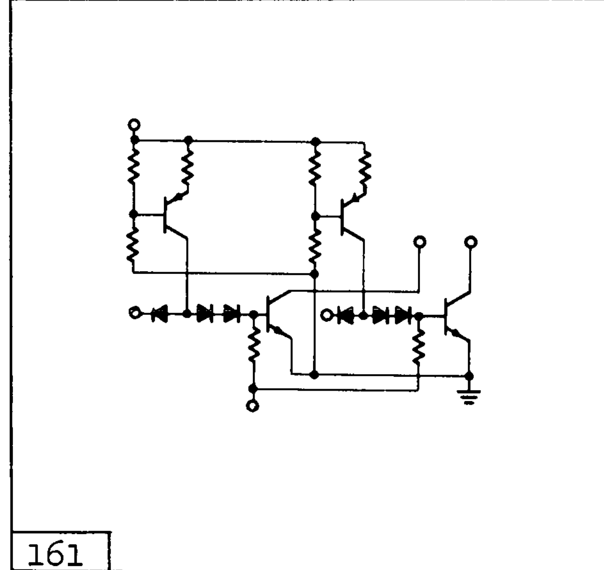

Q̄A
QA
Q̄B
QB
RESET
CLOCK B
SET
CLOCK B
CLOCK A
KA
JA
DIRECT
RESET
KB
JB
-V* = VGG
-V = VDD
GND
160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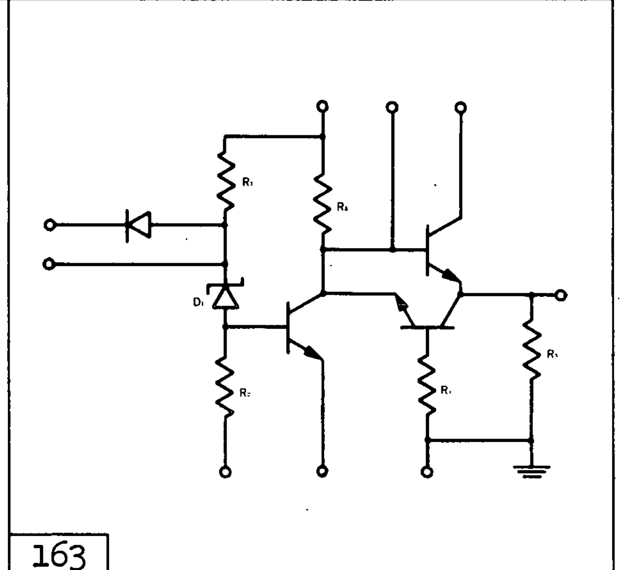
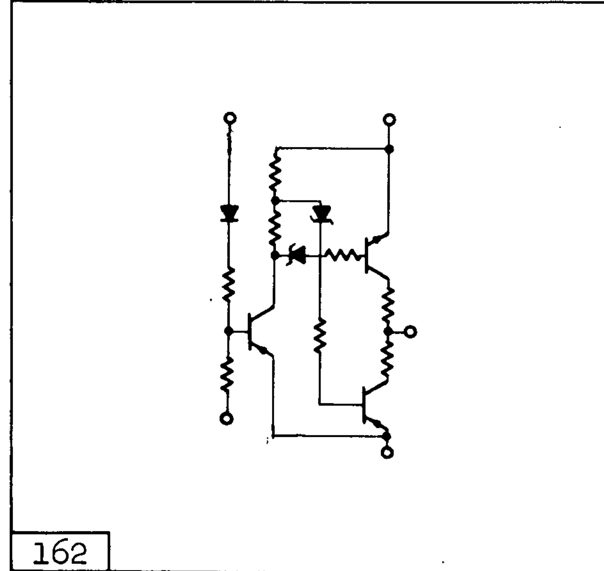

D1
163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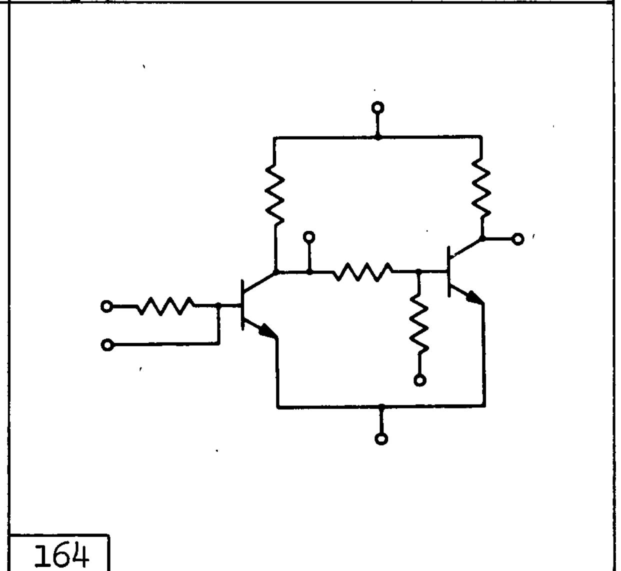
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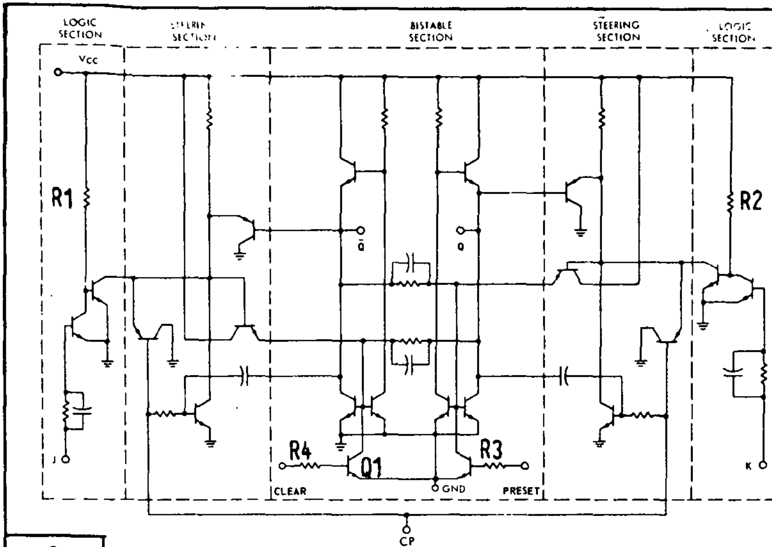
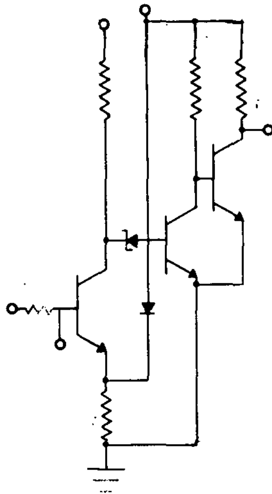


Note:

TI-SN530,SN7300, SN7301 have capacitors in parallel with R1, R2, R3, R4 (SN7301 only) and R1, R2, are not intraconnected to V_{CC}

165



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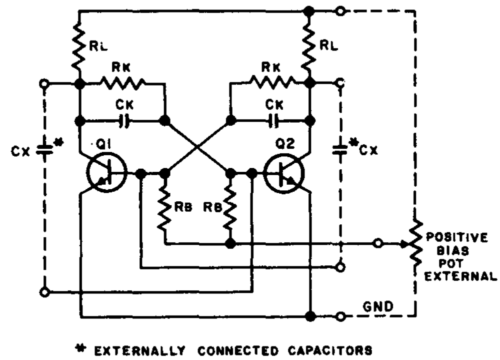

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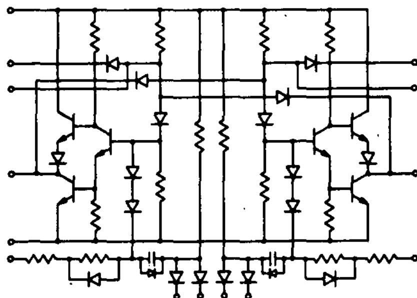
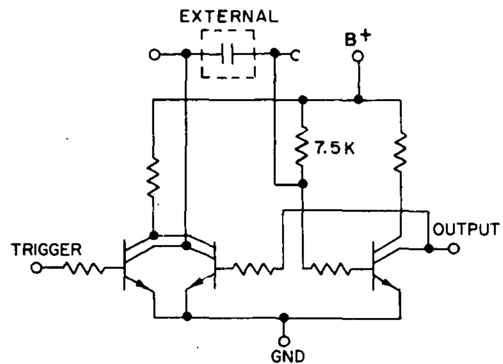


167



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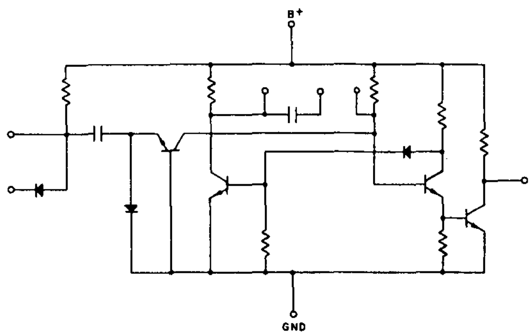

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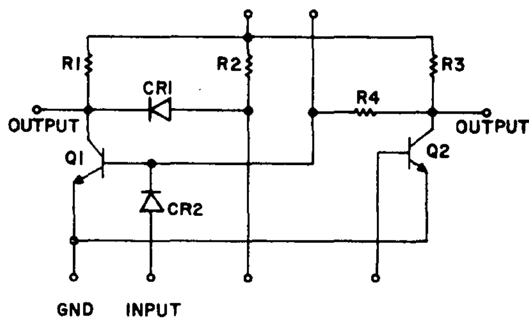

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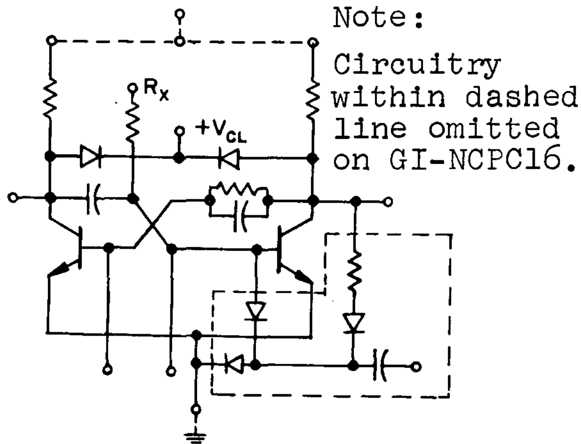
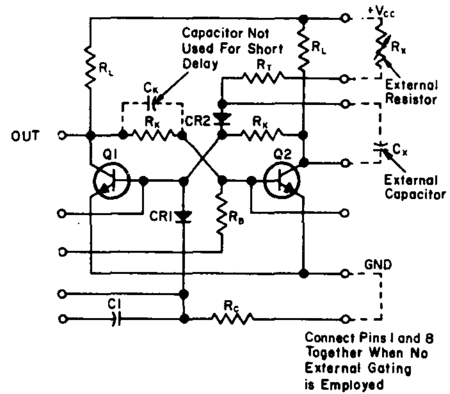


Note:
Circuitry within dashed line omitted on GI-NCPC16.

172



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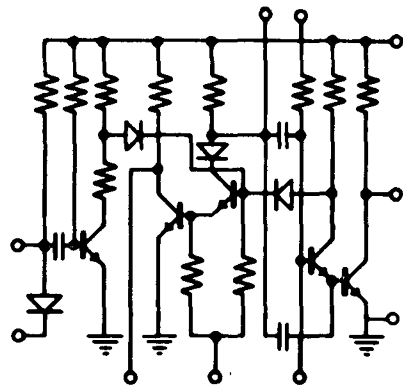

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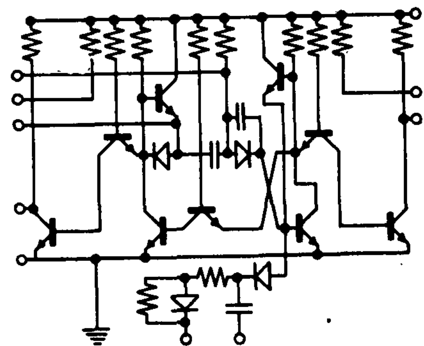

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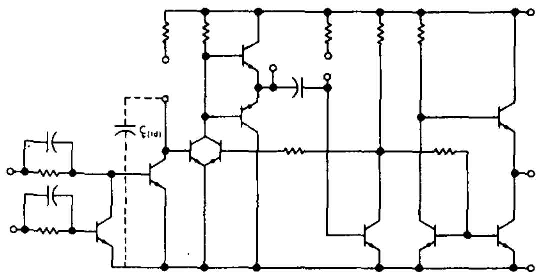

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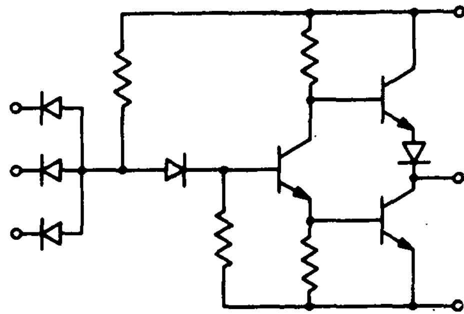

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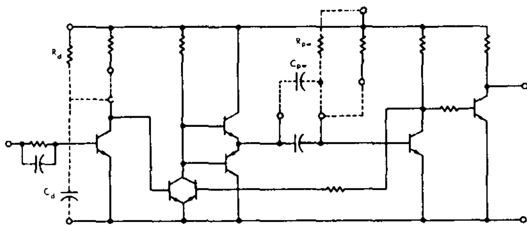

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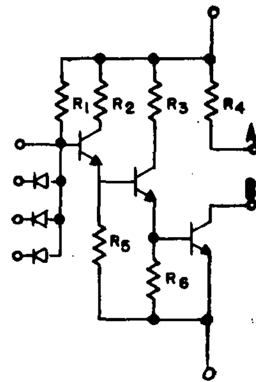

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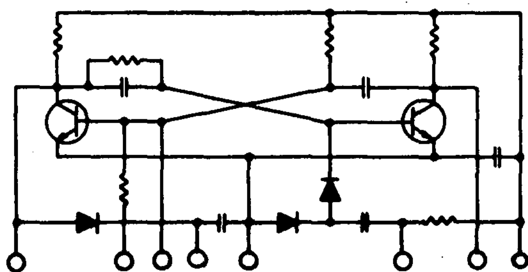

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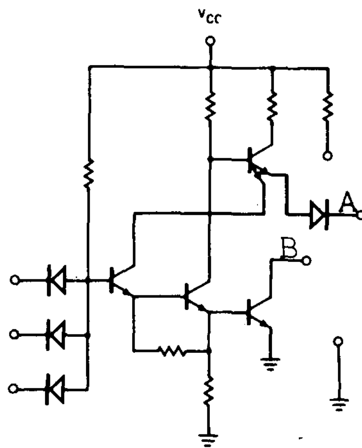

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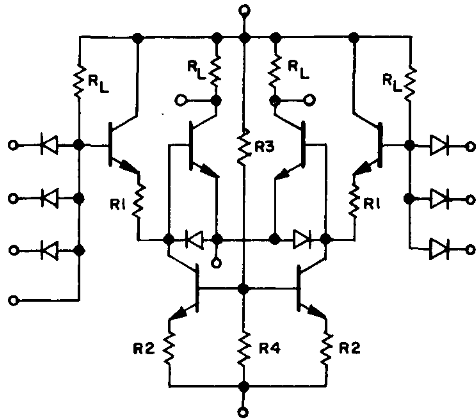

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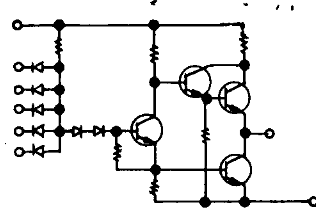

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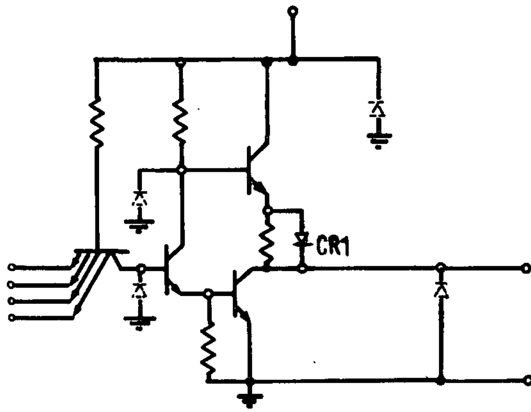

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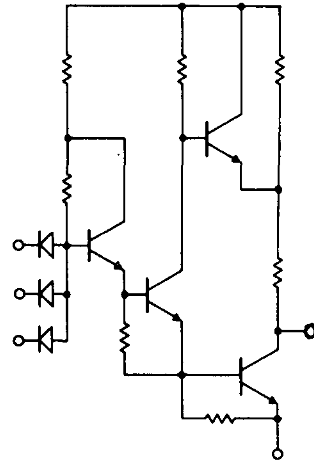

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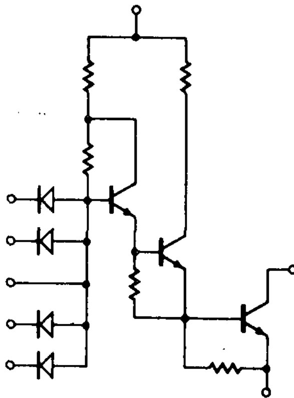

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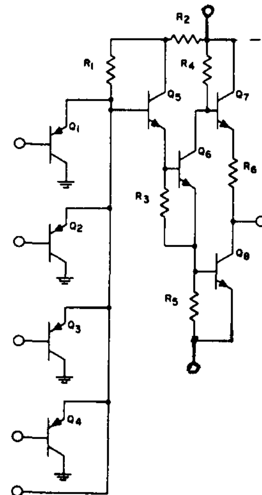

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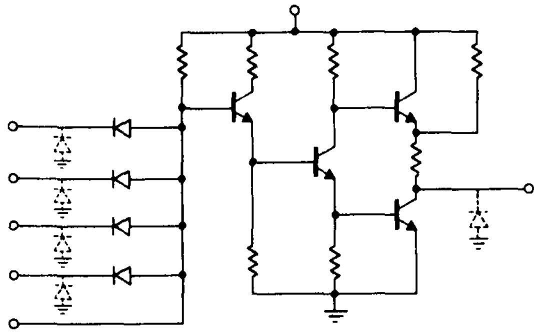

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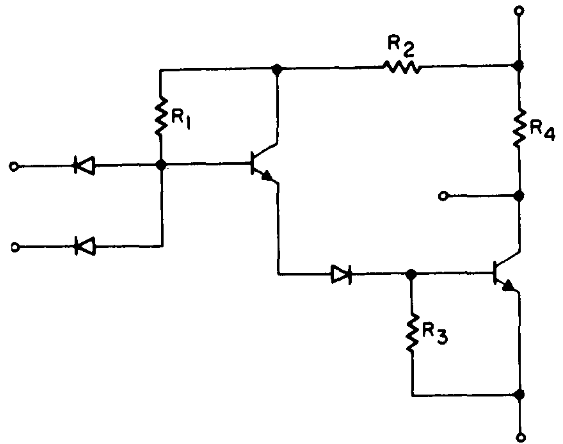

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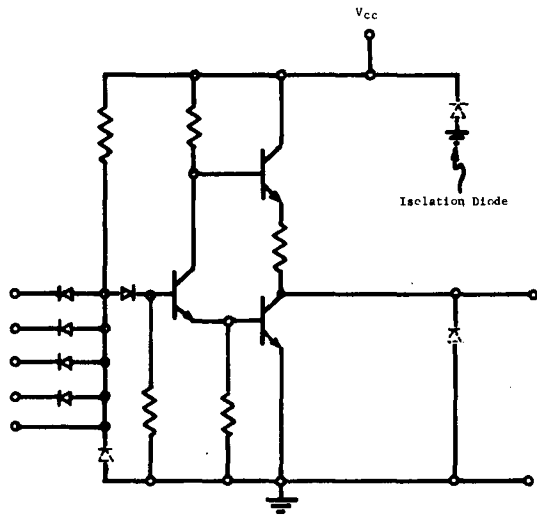

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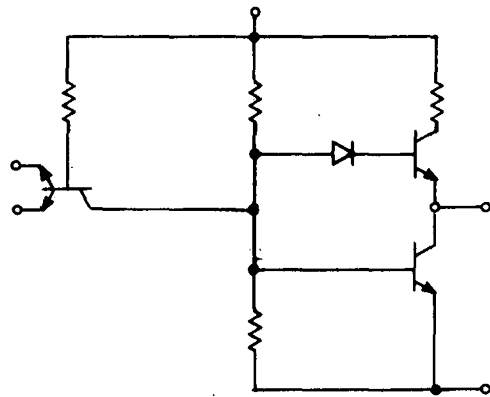

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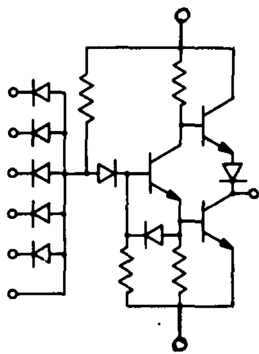

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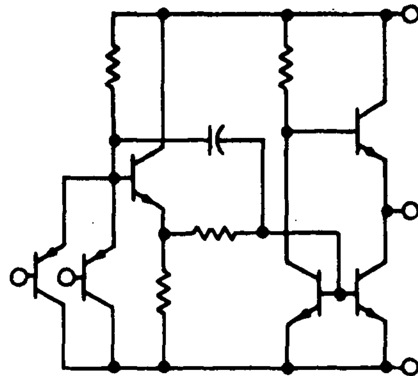

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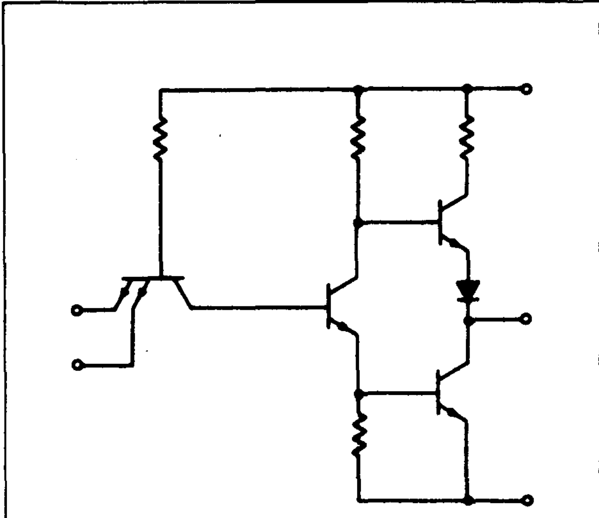
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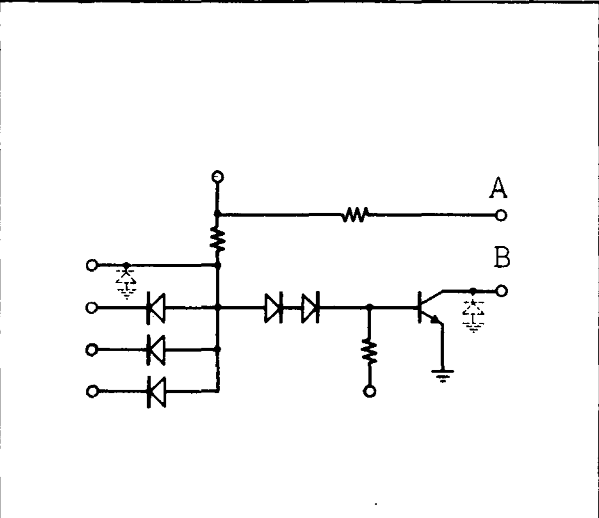
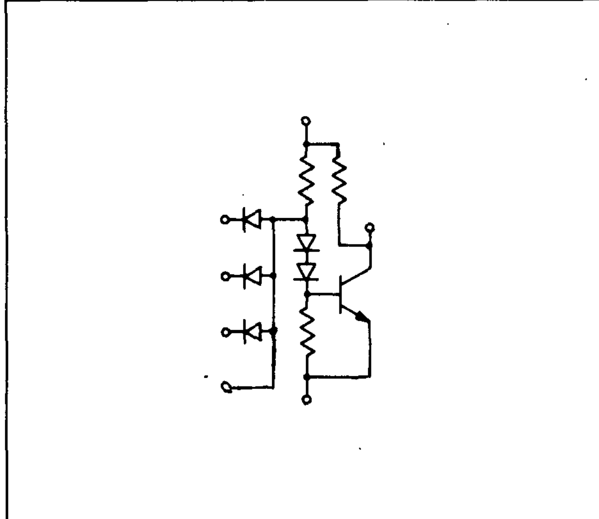

A
B
198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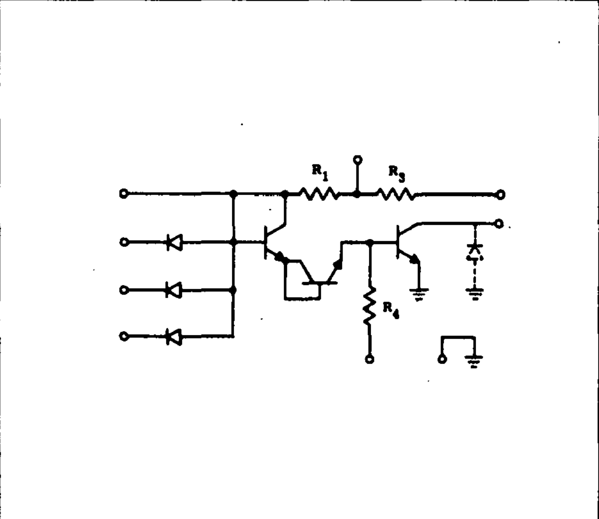
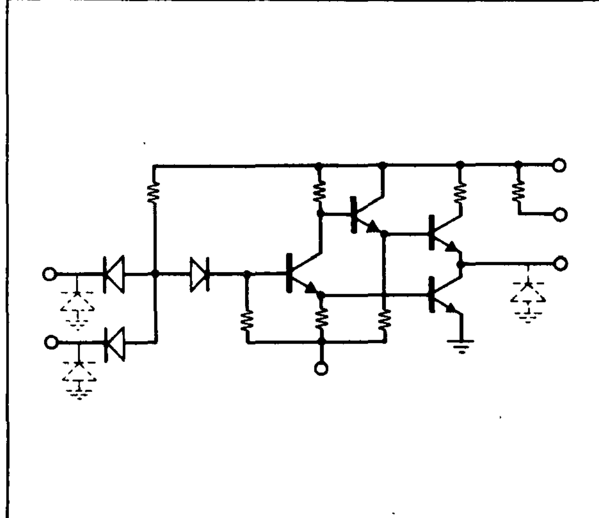

R1
R3
R4
199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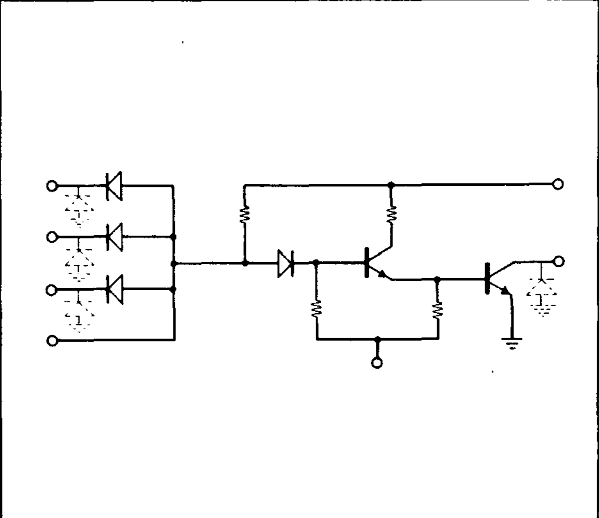
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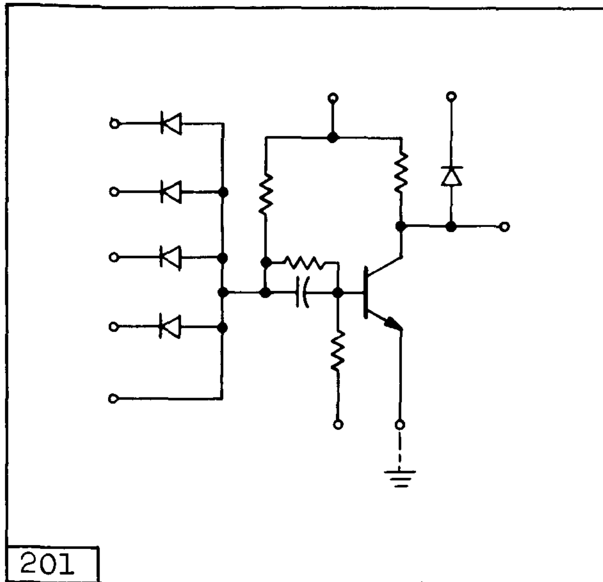
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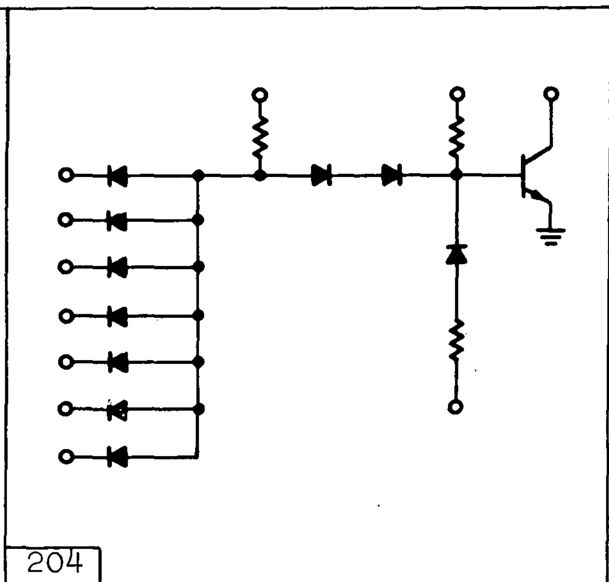
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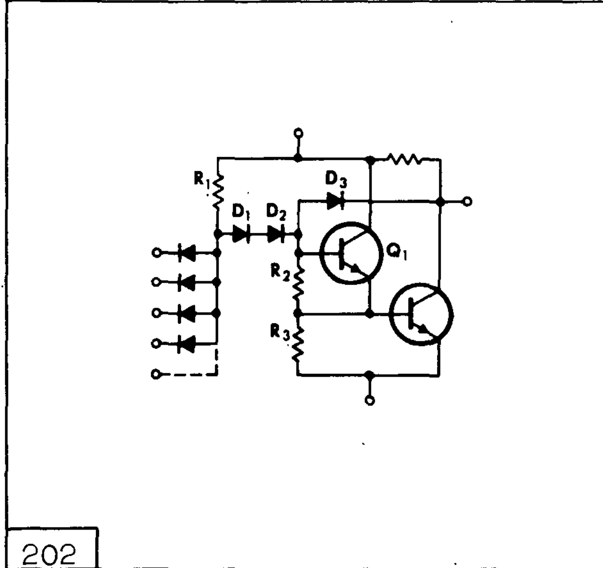
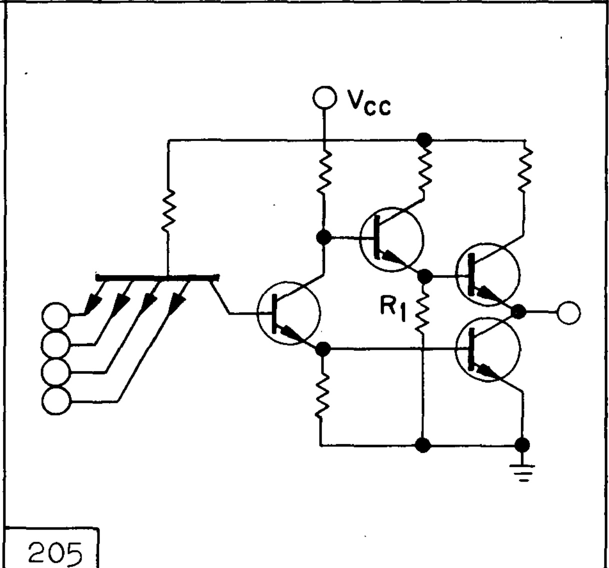
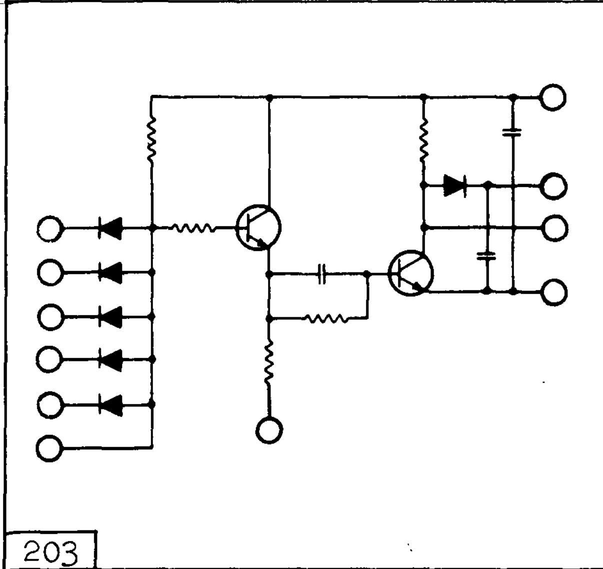

R1
D1
D2
D3
Q1
R2
R3
202


Vcc
R1
205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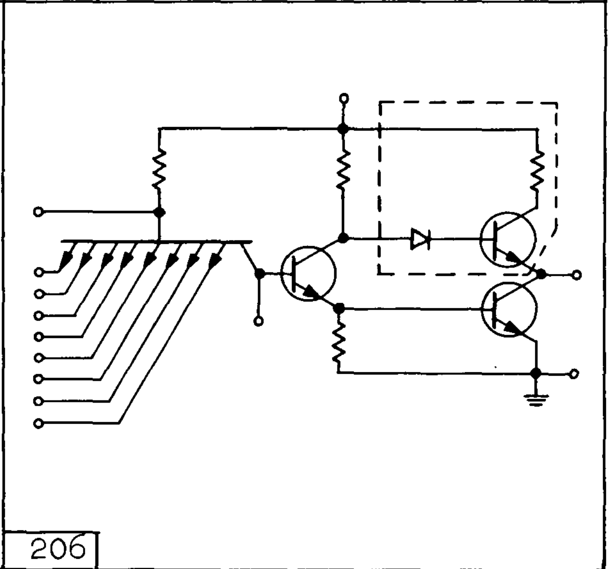
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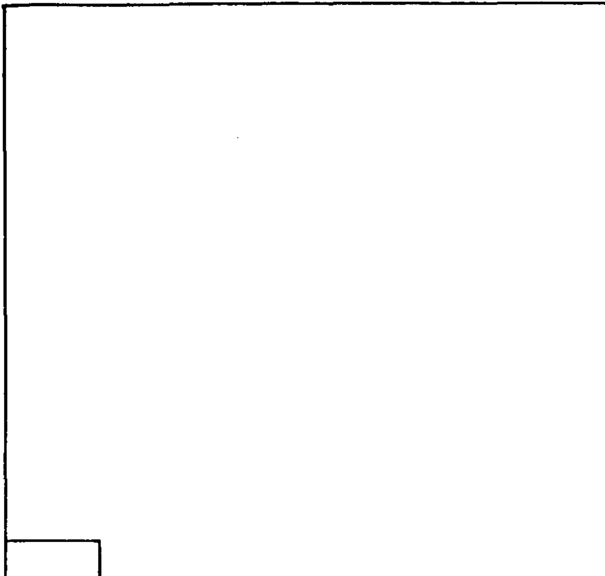

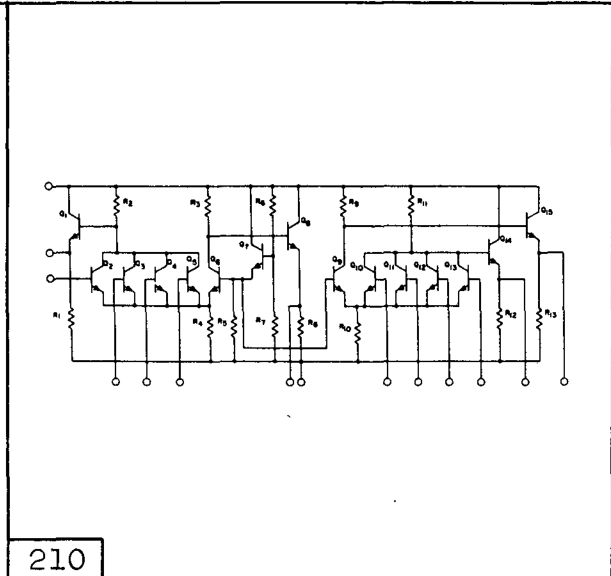

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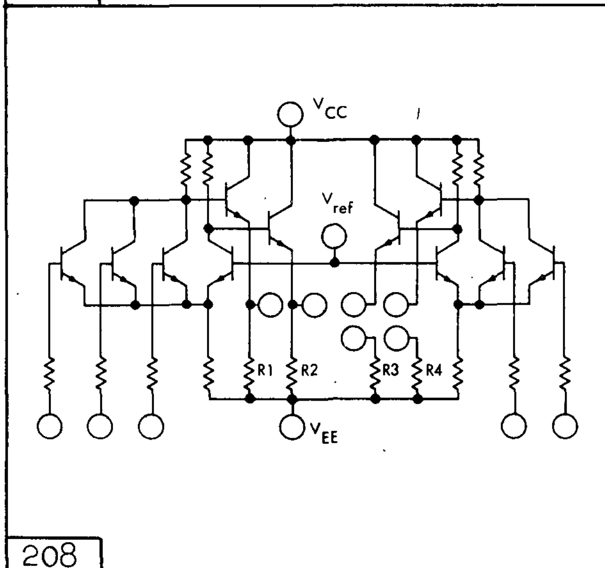

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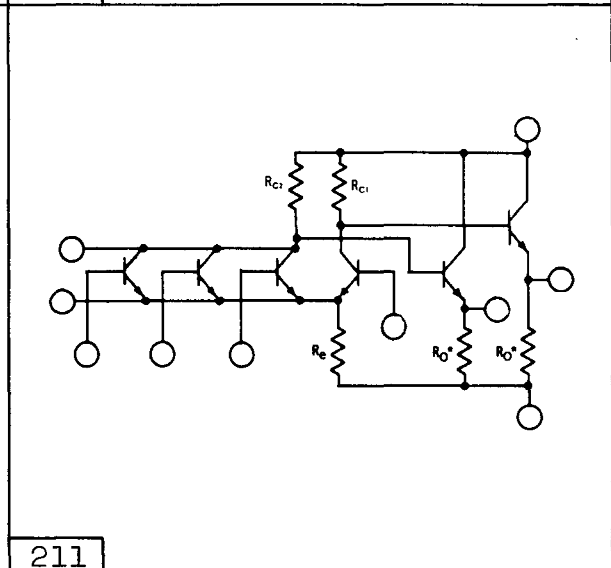

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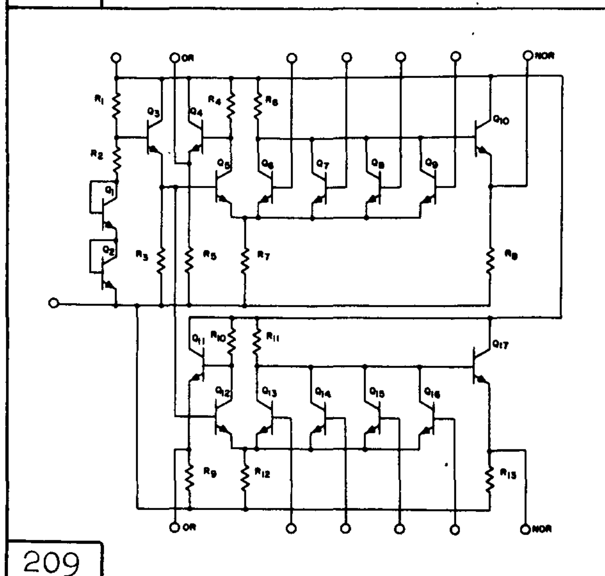
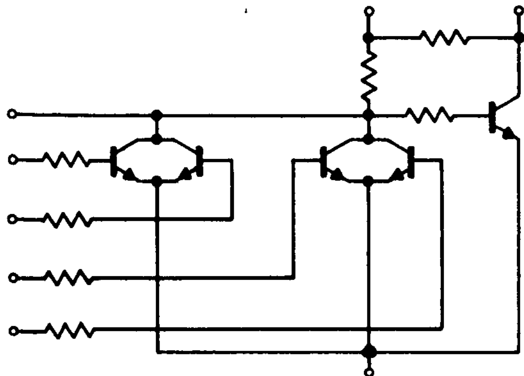
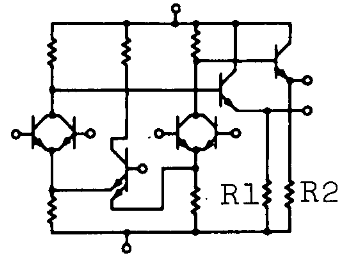


209

212

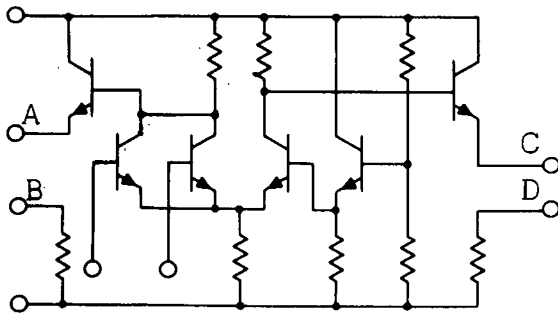


213

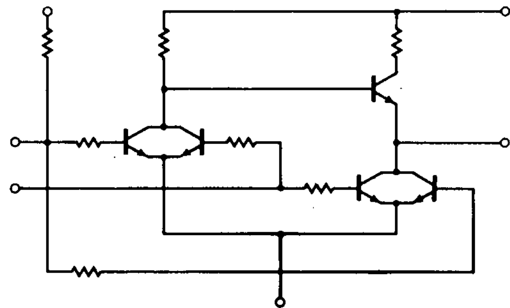


Note: Circuit shown is dual with common reference source

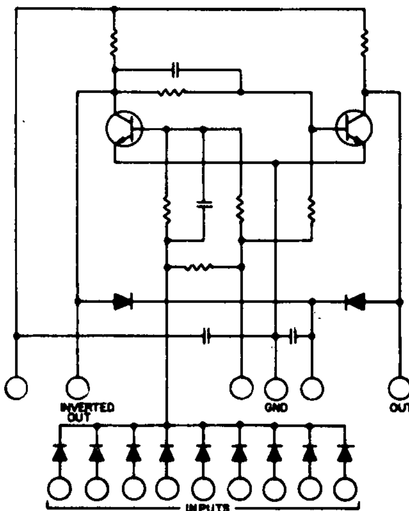
216



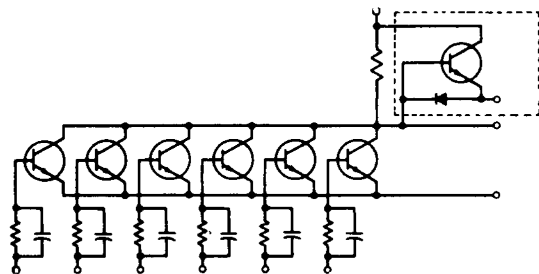
214



217

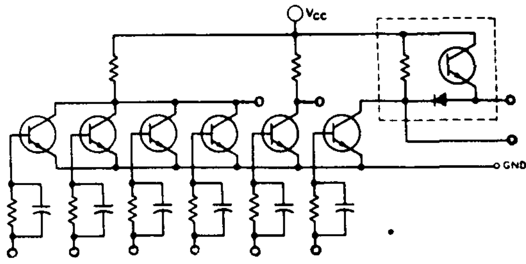


215



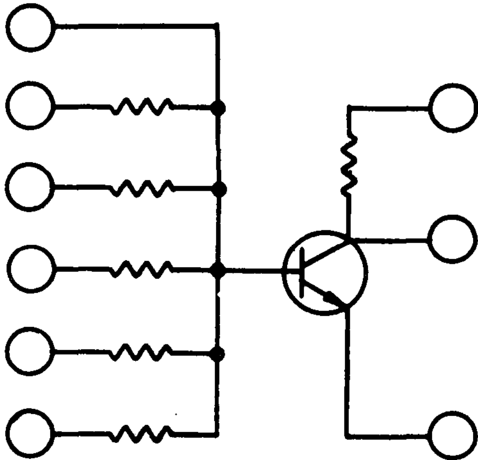
Note: Circuitry within dashed line applies only to TI-SN513, SN5162 and SPRG-US-103,US0113

218



Note: Circuitry within dashed line applies only to SPRG-US0115

219



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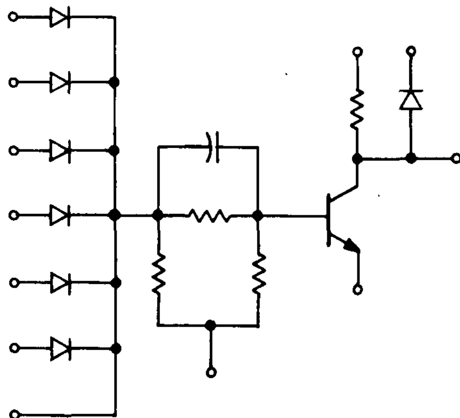

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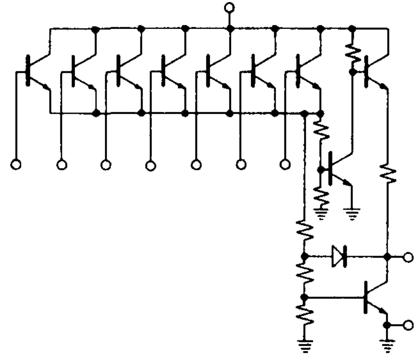
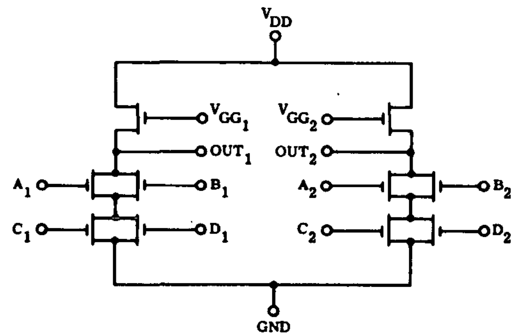
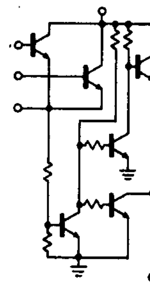


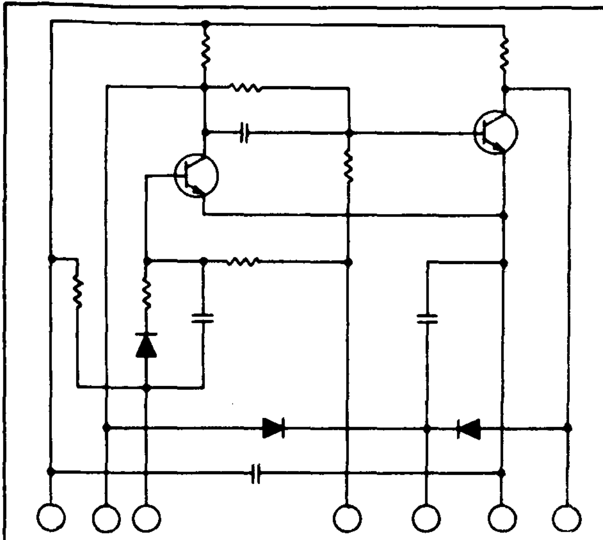
222

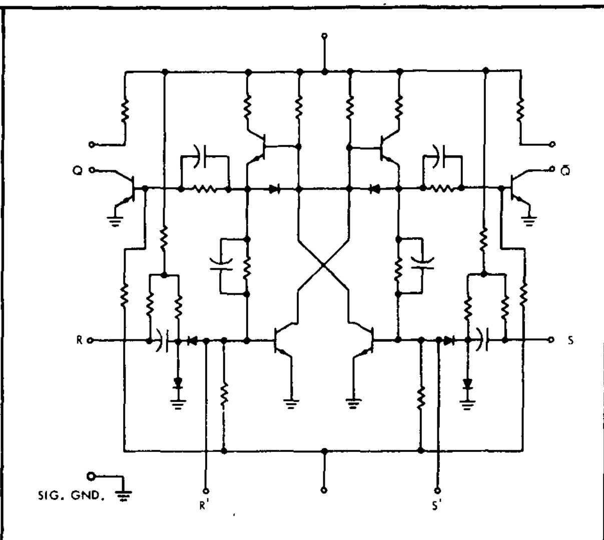


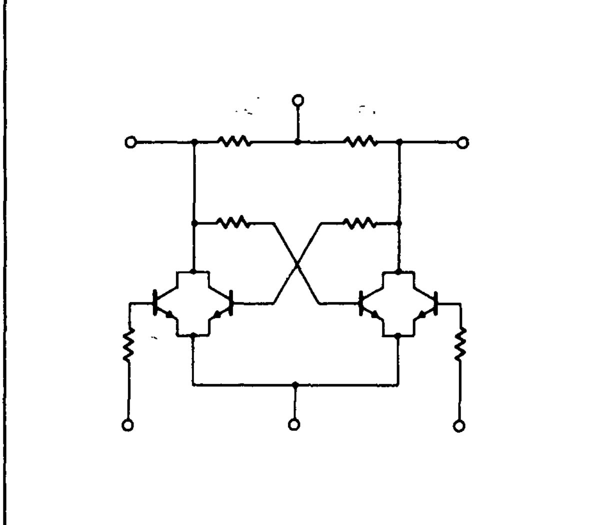
223

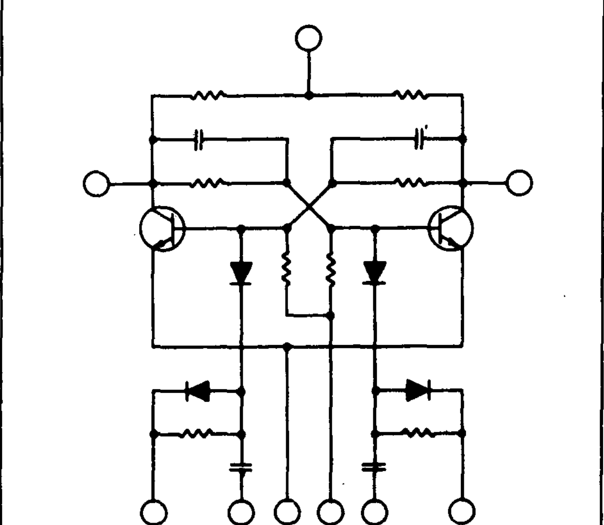


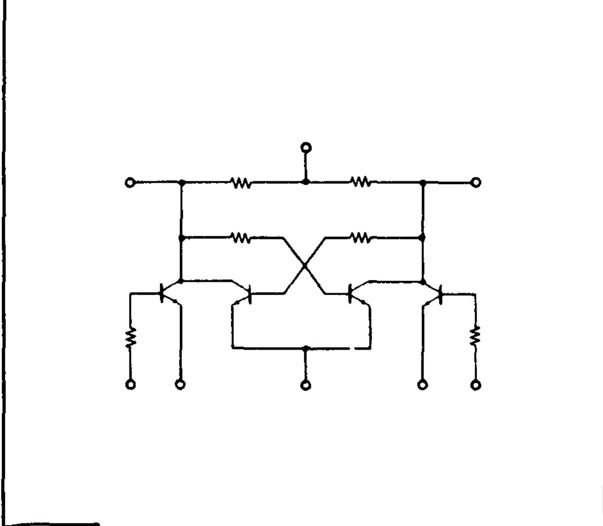
224

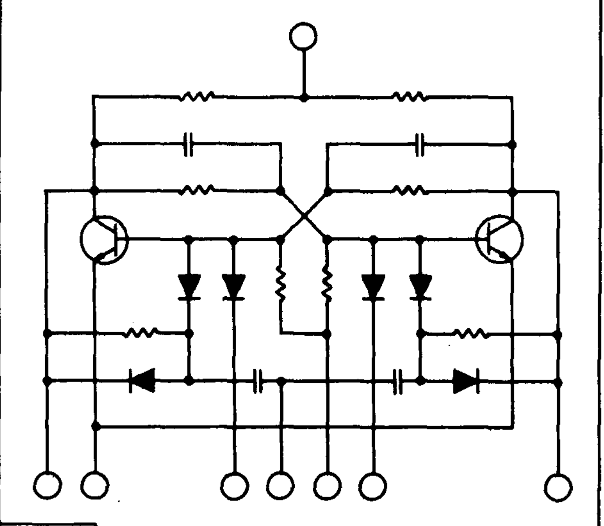

225

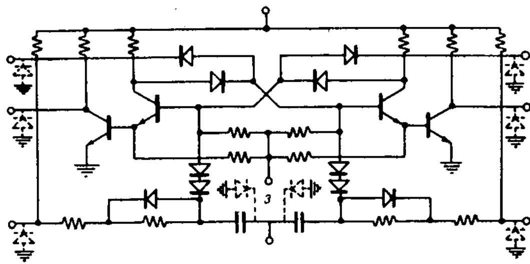

Q
Q̄
R
S
R'
S'
SIG. GND.
228


226

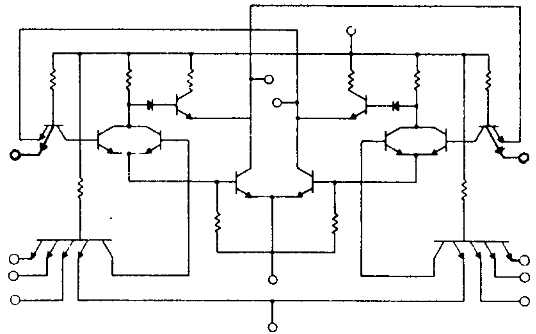

229


227

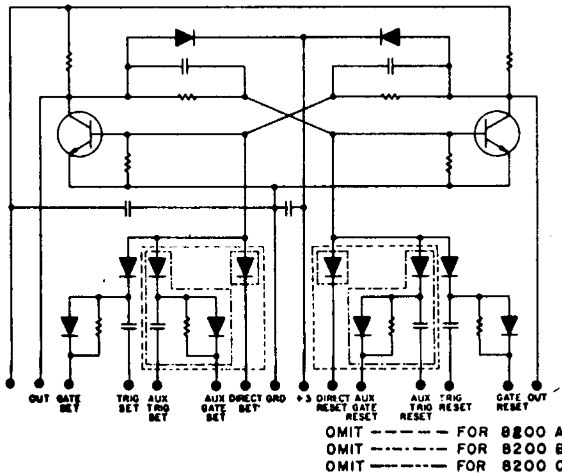

230



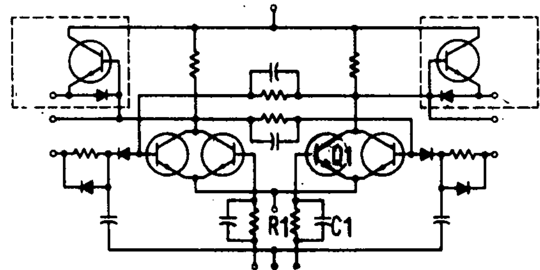
231



234

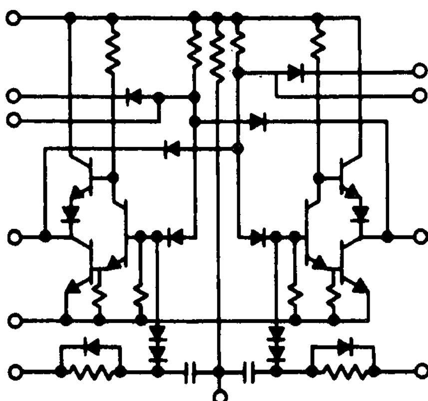


232



Note: Portion of circuitry within dotted line applies only to II-SN511, SN5112, SN5111; SPRG-US0111, US0101

235



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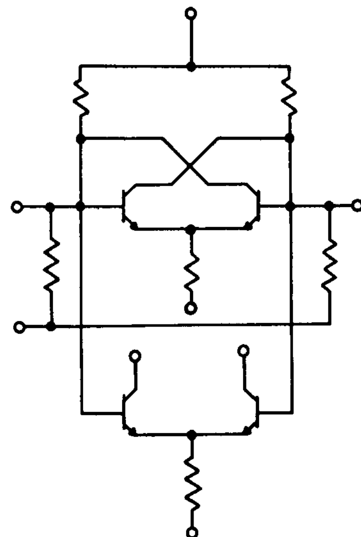
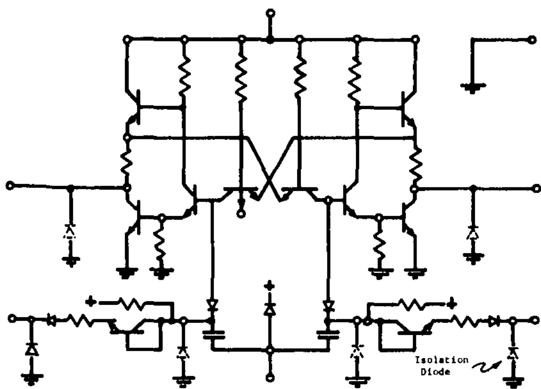
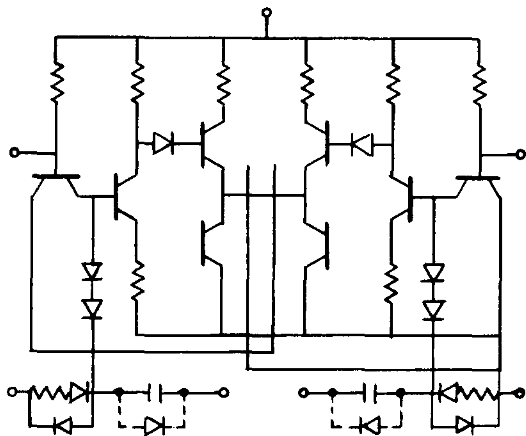


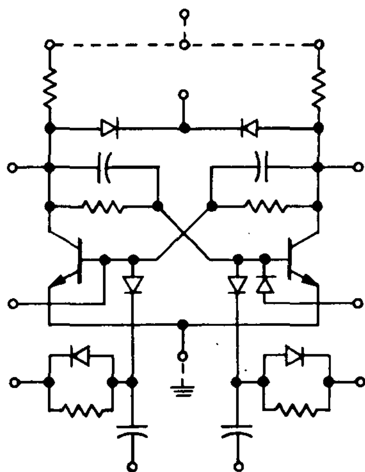
236



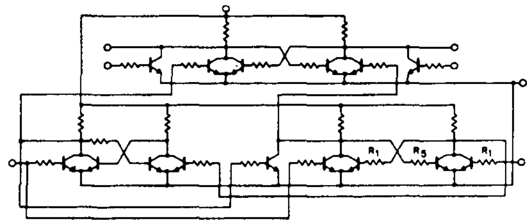
237



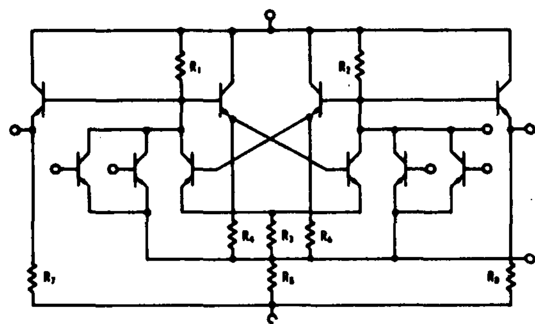
238



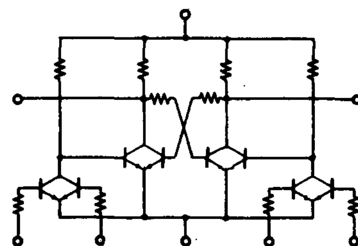
239



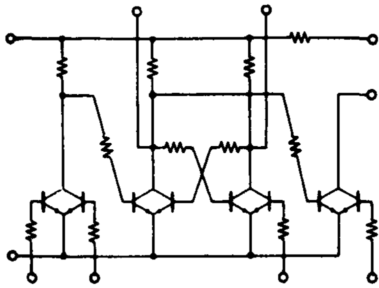
240



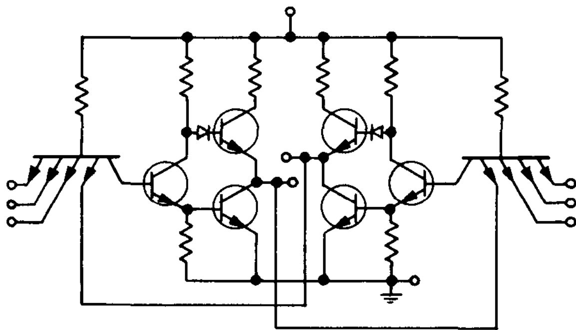
241



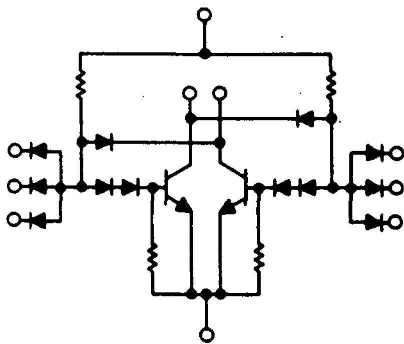
242



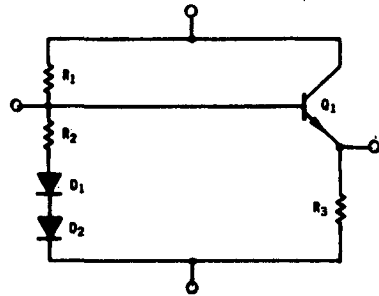
243



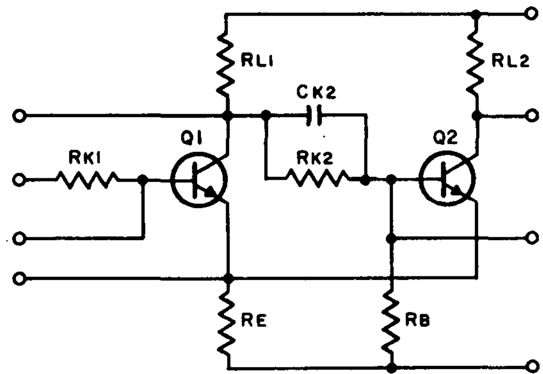
244



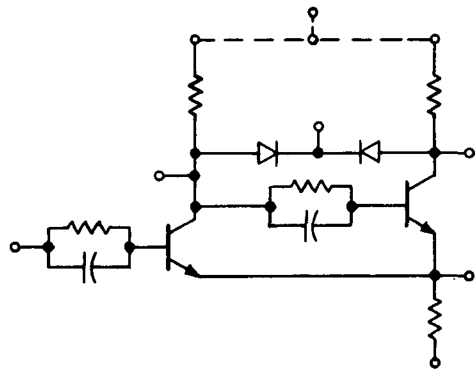
245



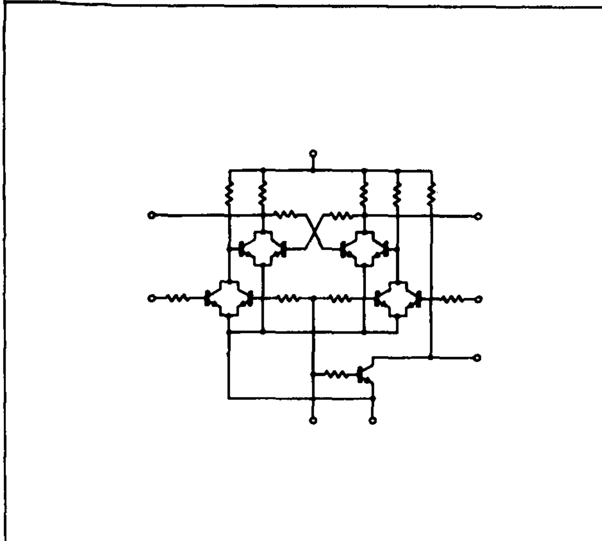
246

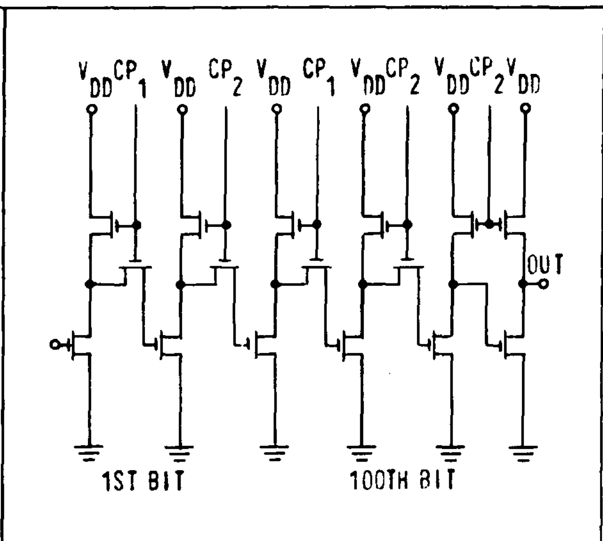


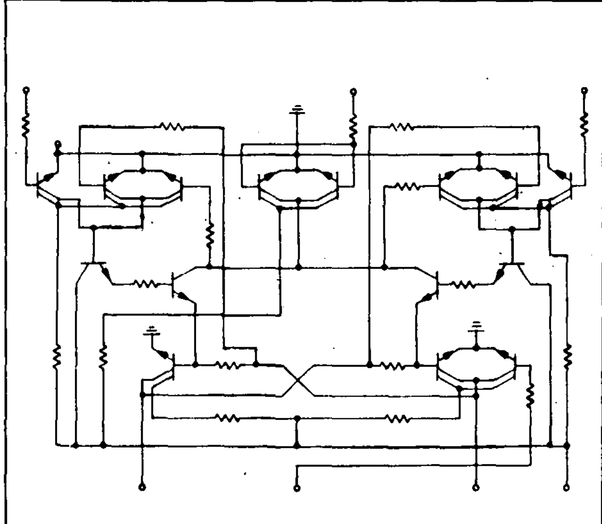
247

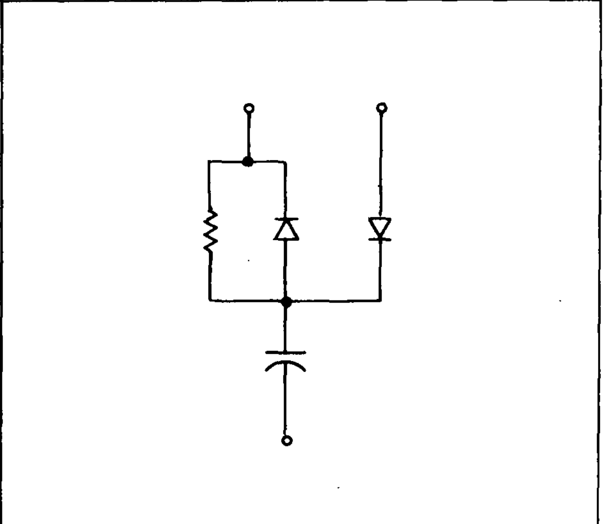


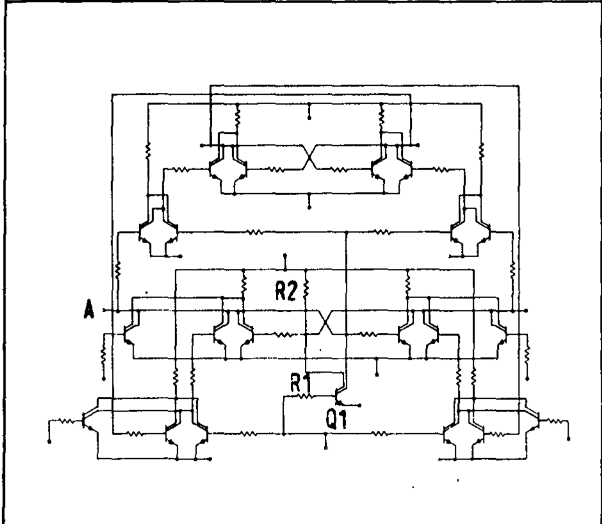
248

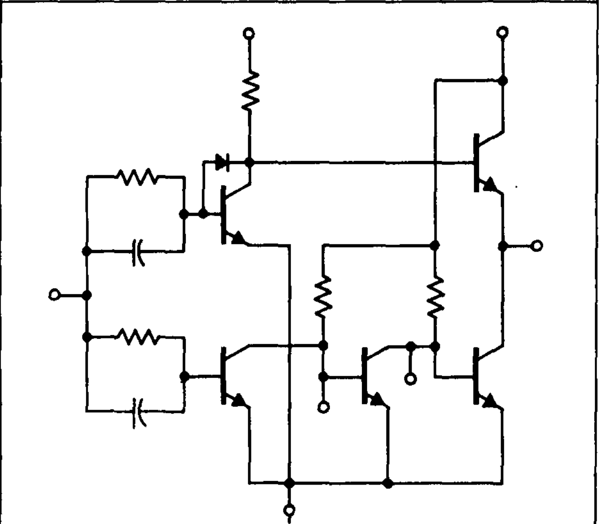

249

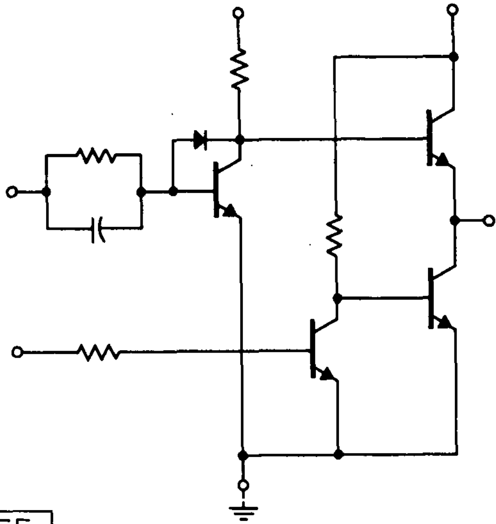

V_{DD} CP_1 V_{DD} CP_2 V_{DD} CP_1 V_{DD} CP_2 V_{DD} CP_2 V_{DD}
OUT
1ST BIT
100TH BIT
252


250


253


A
R2
R1
Q1
251


254



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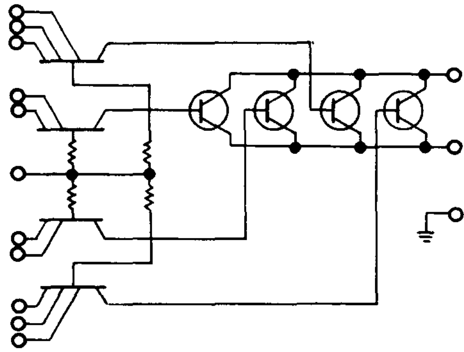
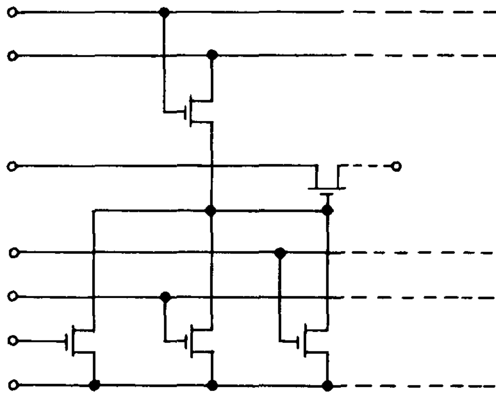
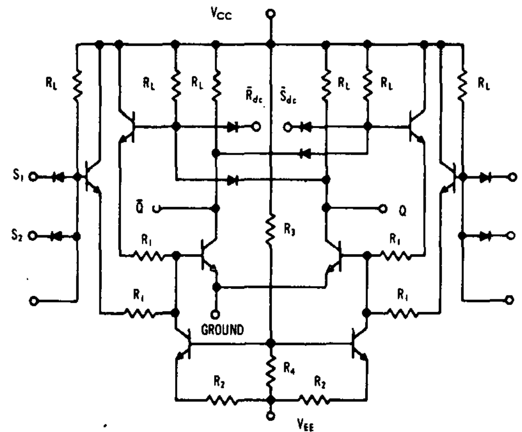


258

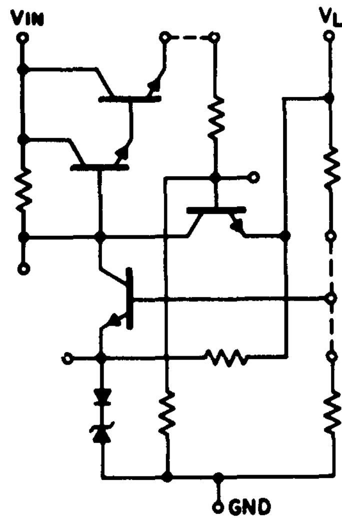


256

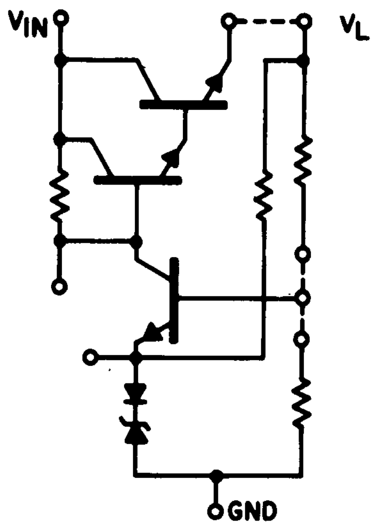


259

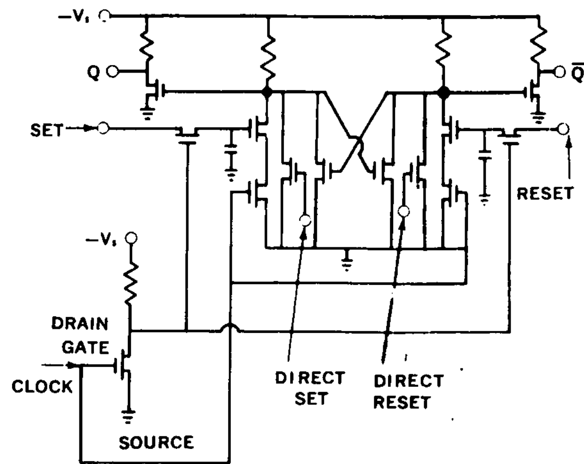
257



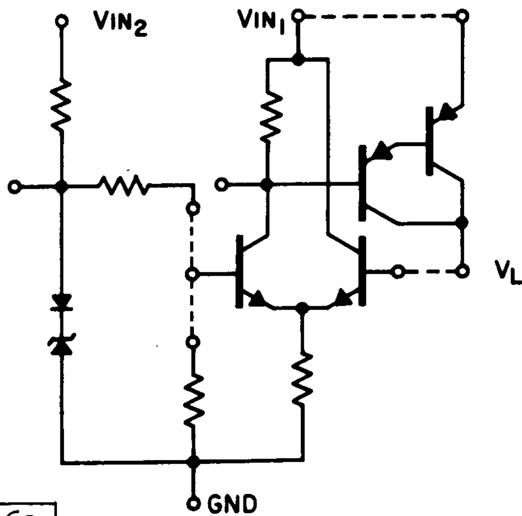
260



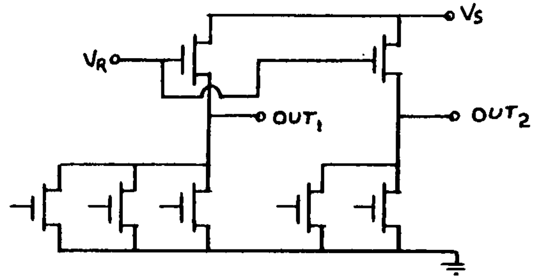
261



264



262



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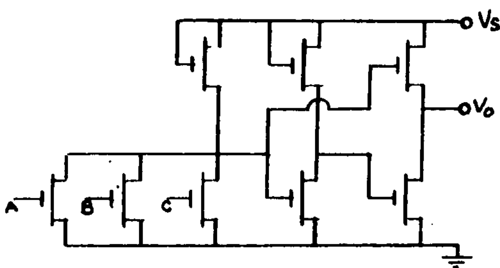

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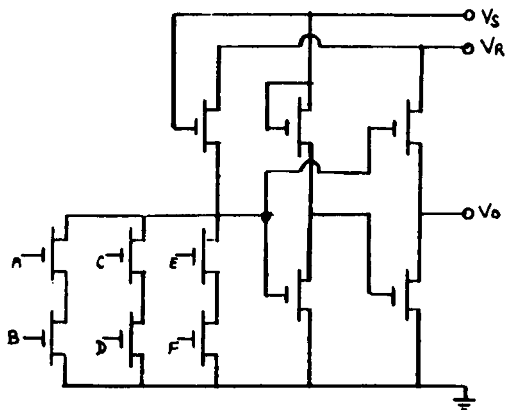
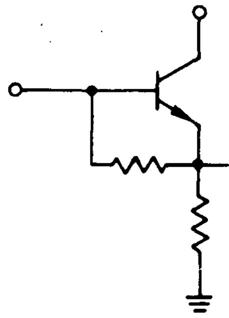
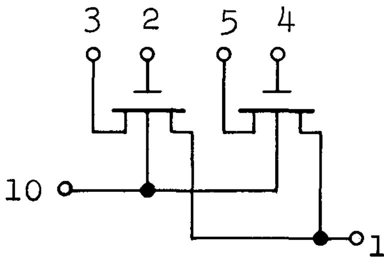


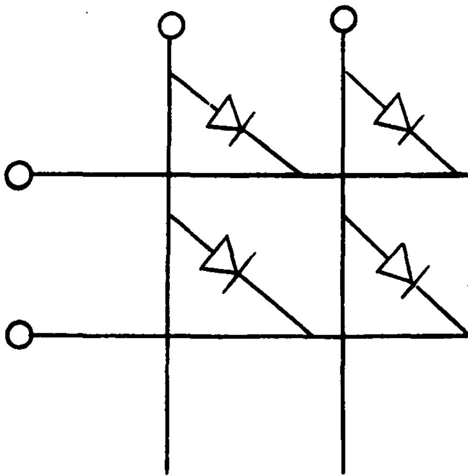
266



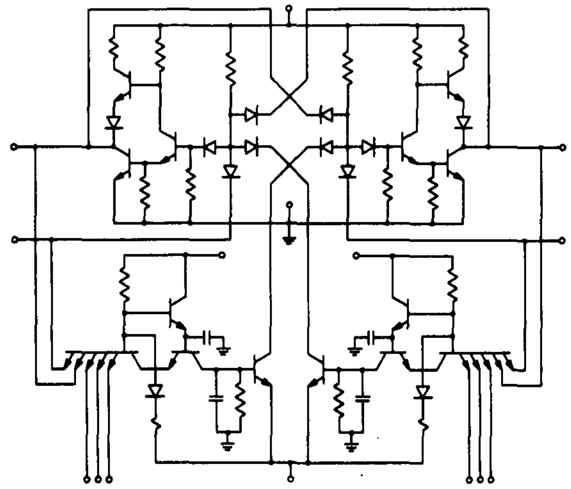
267



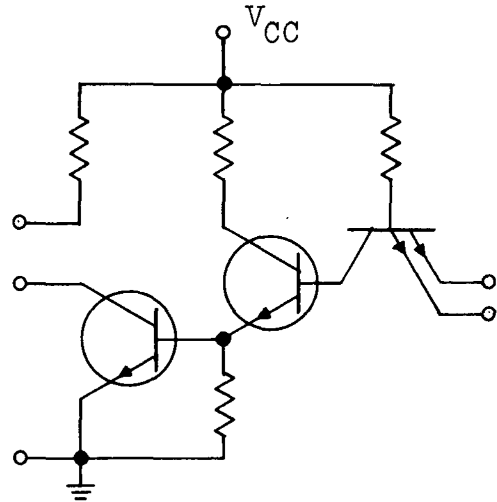
268



269



270



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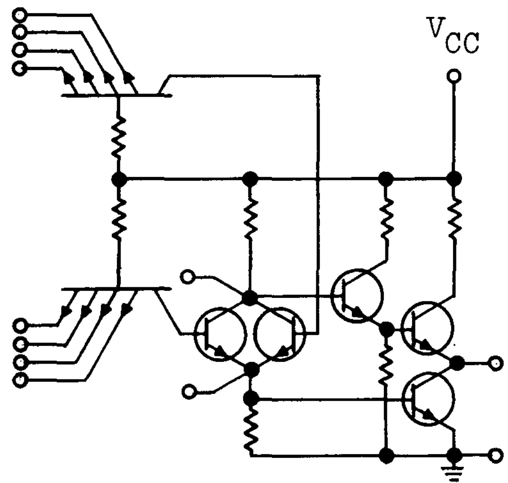

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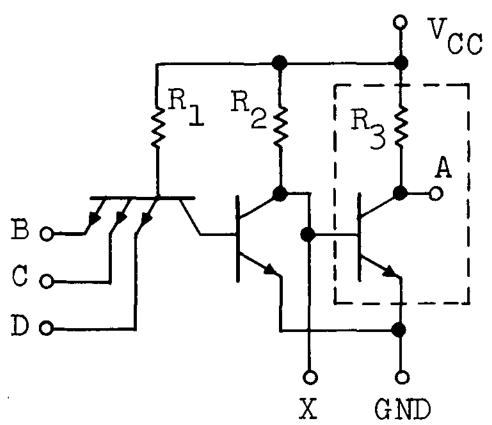

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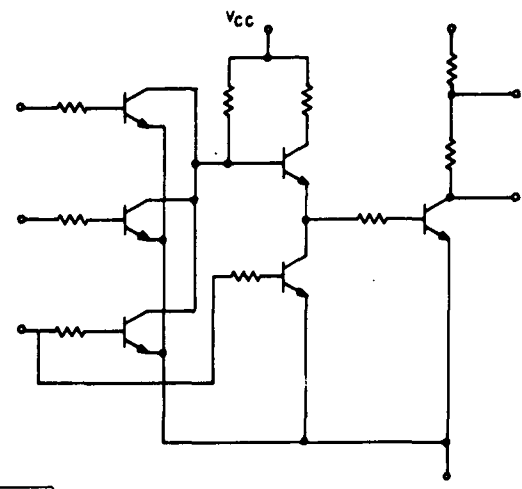

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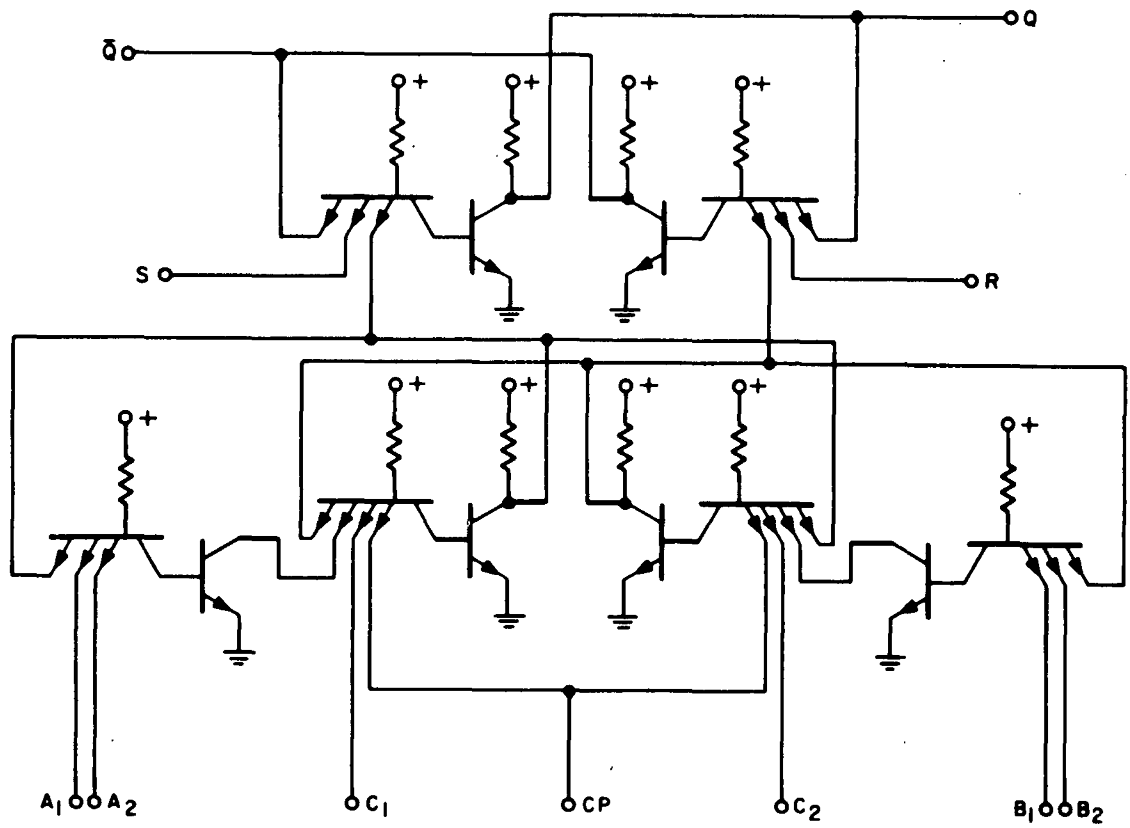

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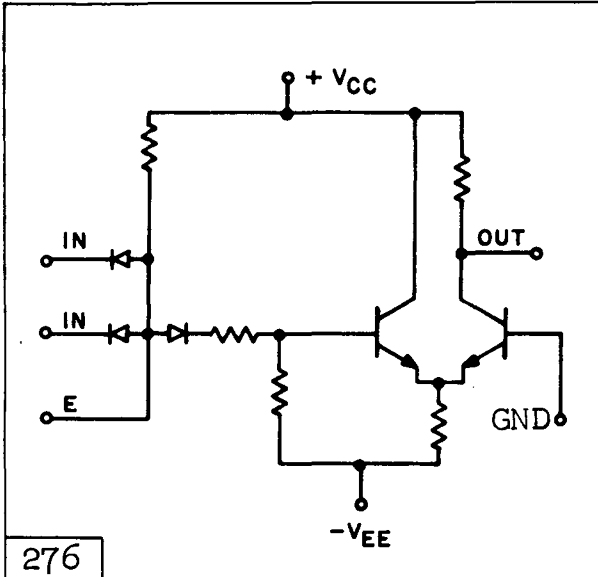
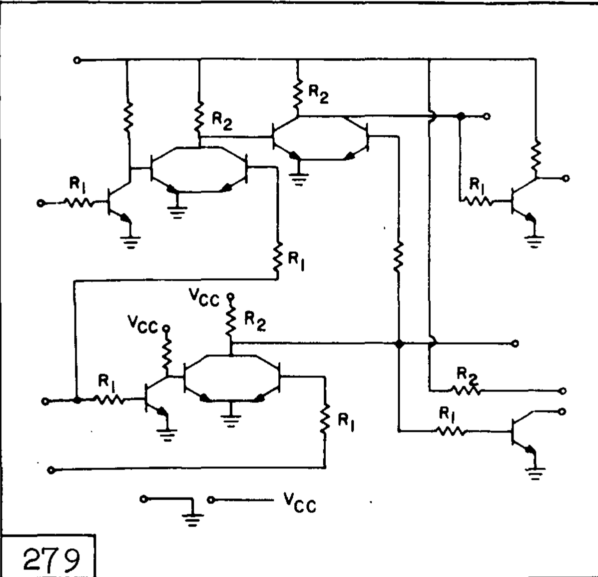
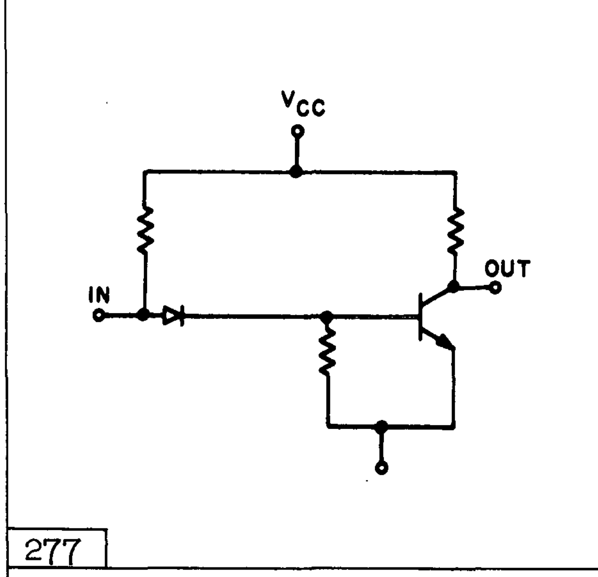
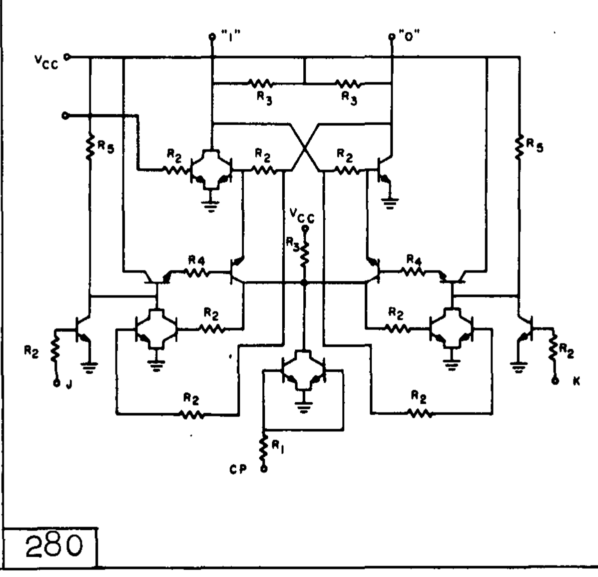
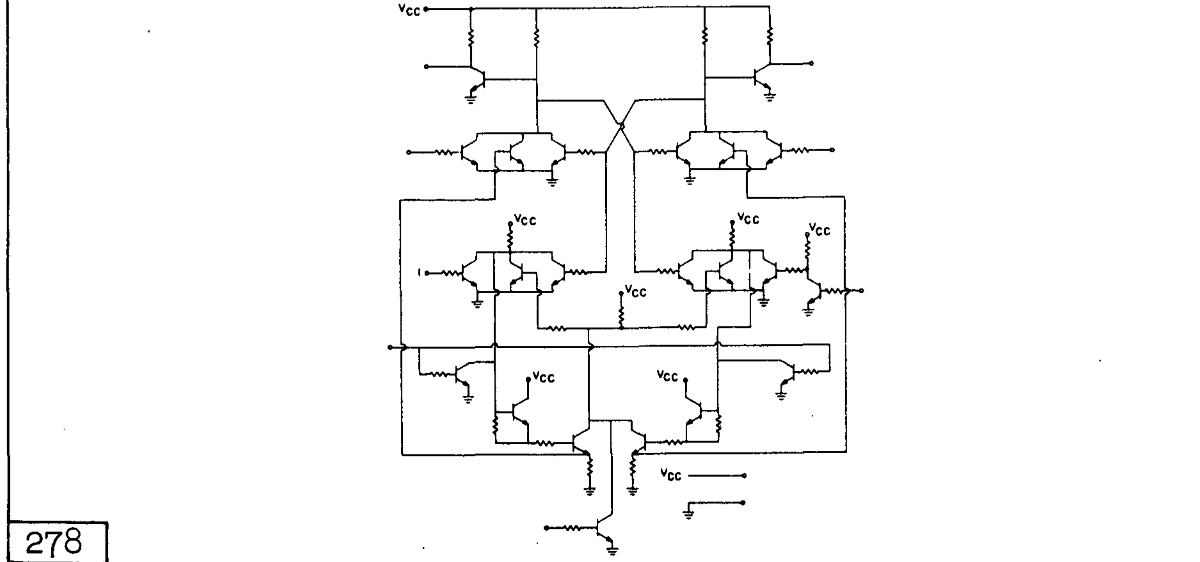
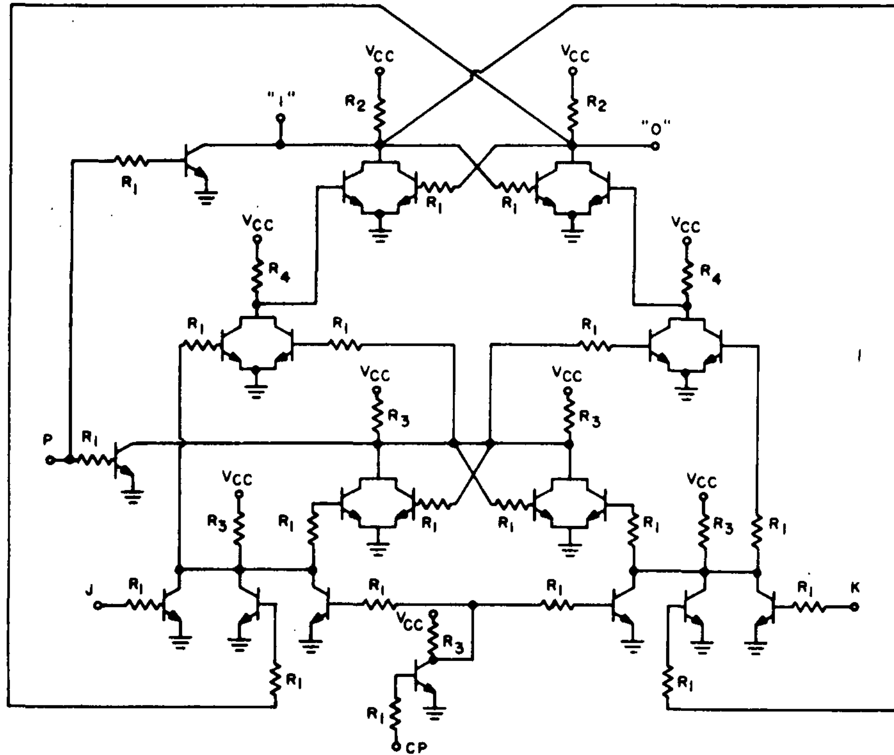

+ VCC
IN
IN
E
OUT
GND
-VEE
276


R2
R2
R1
R1
R1
VCC
R2
VCC
R1
R1
R2
R1
VCC
279

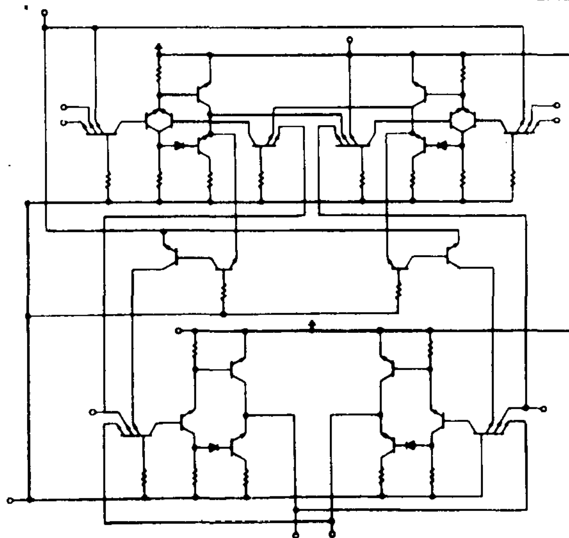

VCC
IN
OUT
277


"1"
"0"
VCC
R3
R3
R5
R2
R2
R2
R5
VCC
R3
R4
R4
R2
R2
R2
R2
J
K
R2
R2
R1
CP
280

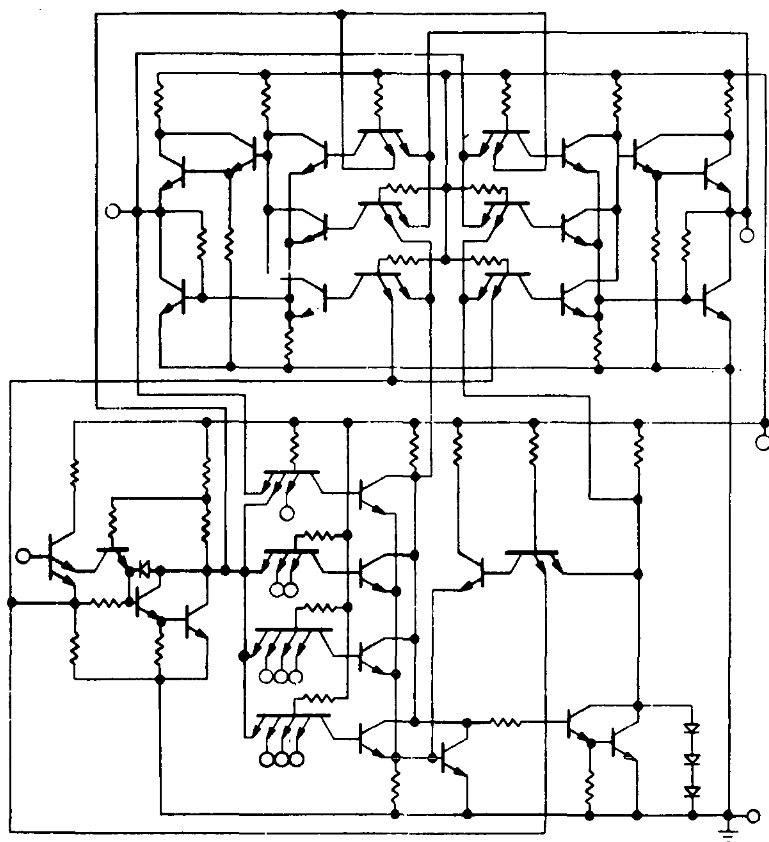

VCC
VCC
VCC
VCC
VCC
VCC
VCC
VCC
278



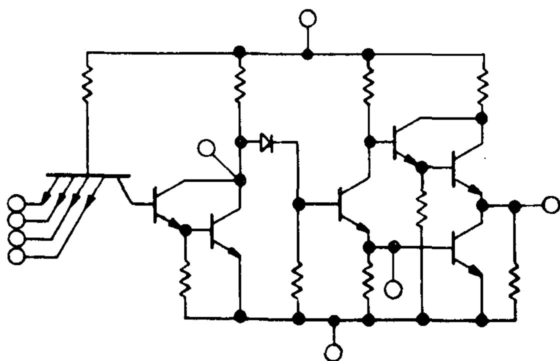
281



282



283



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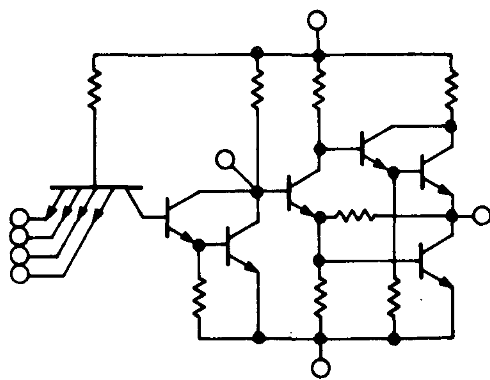

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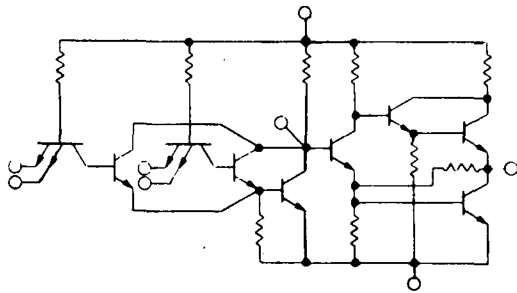

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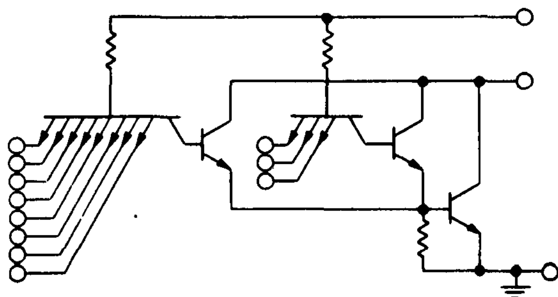

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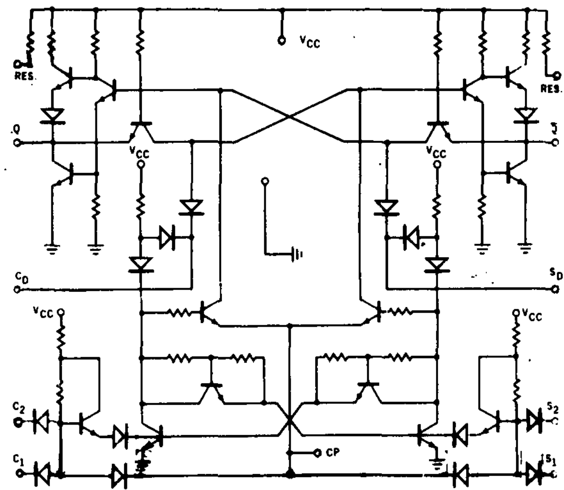

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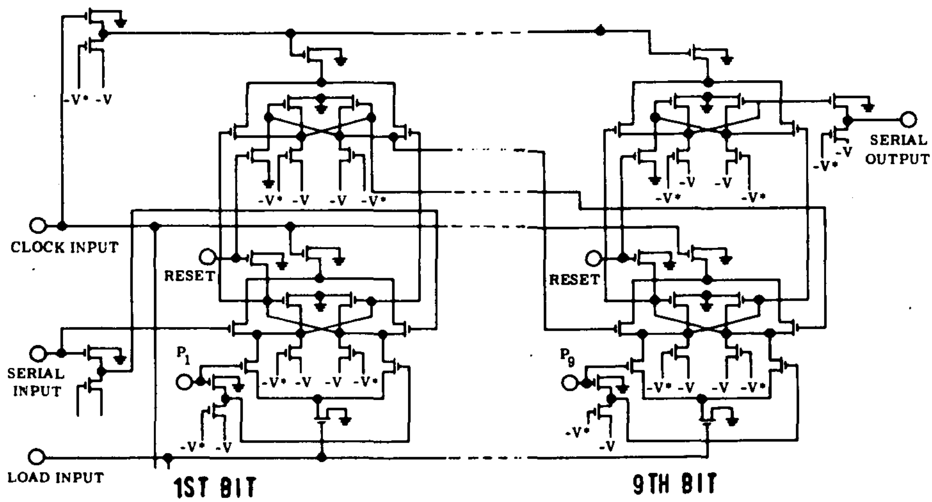

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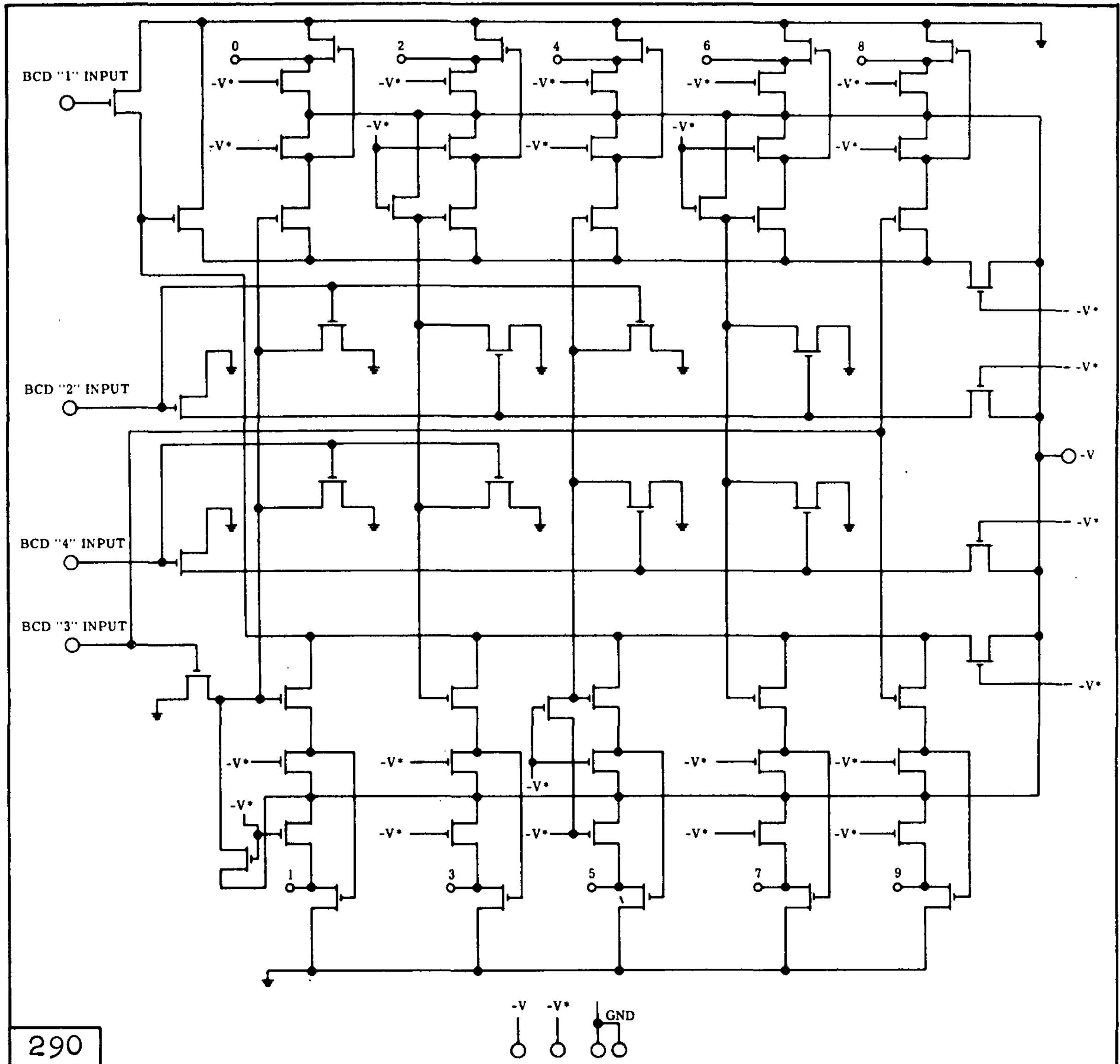
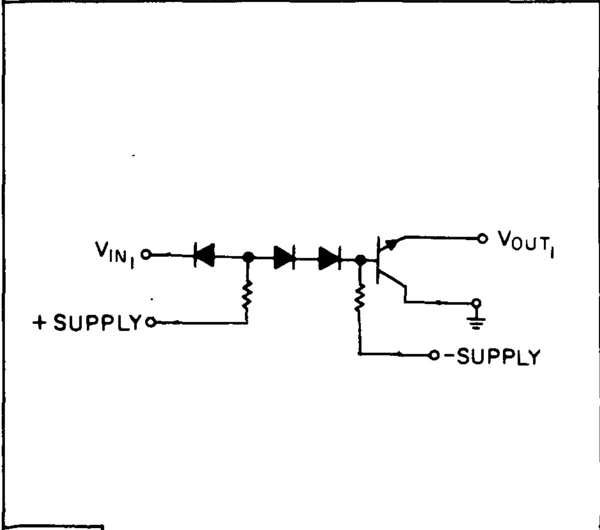

BCD "1" INPUT
BCD "2" INPUT
BCD "4" INPUT
BCD "3" INPUT
0
2
4
6
8
1
3
5
7
9
-V*
-V
GND
290

D10 1 D2 D4 D8 D20 D40 B2 B4 B8 B16 B32 -V $-V_{DD}$

291



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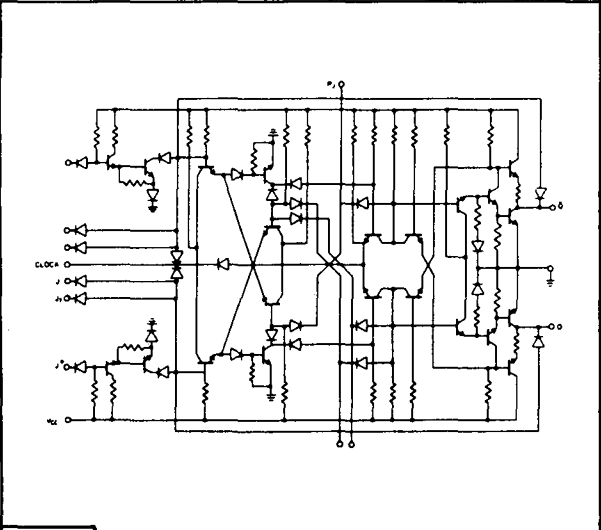

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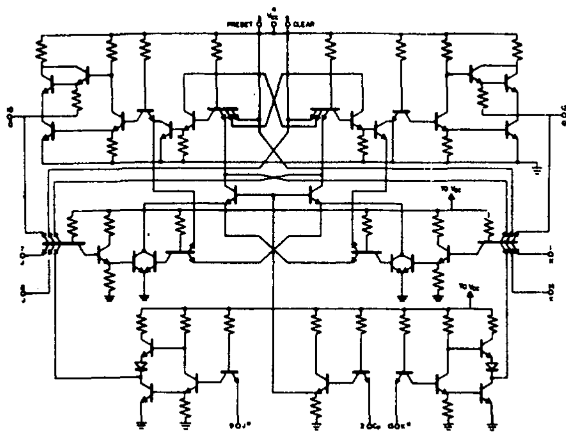

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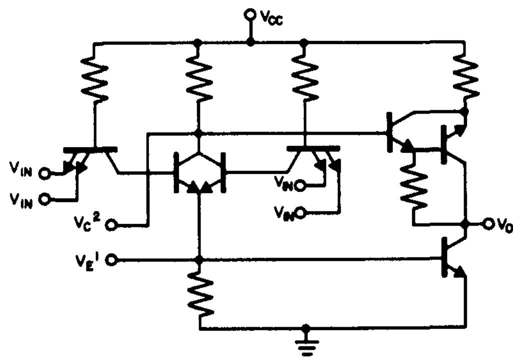

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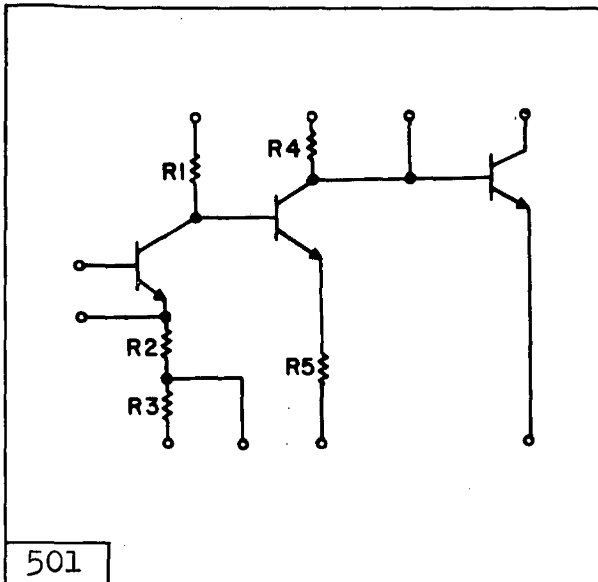
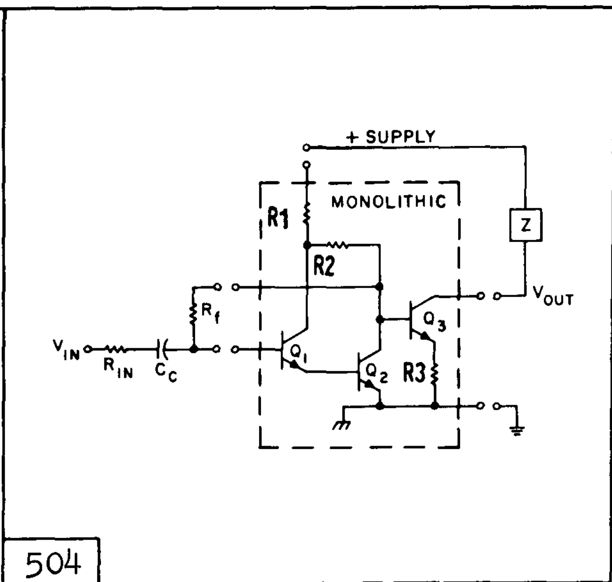
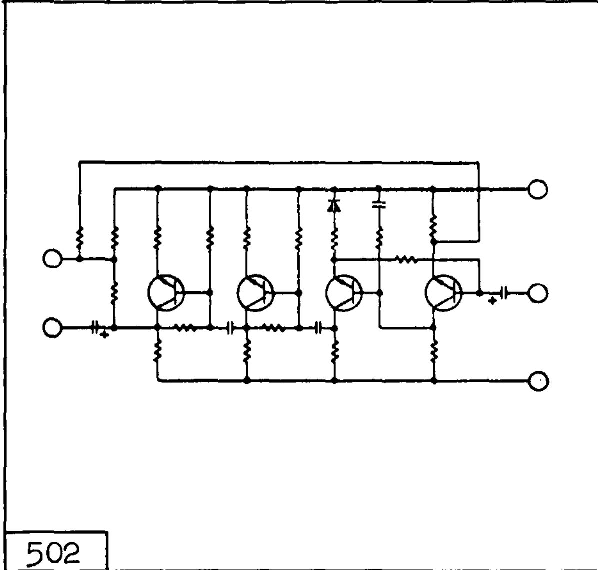

R1
R4
R2
R5
R3
501


+ SUPPLY
MONOLITHIC
R1
R2
Z
VOUT
Rf
VIN
RIN
CC
Q1
Q2
Q3
R3
504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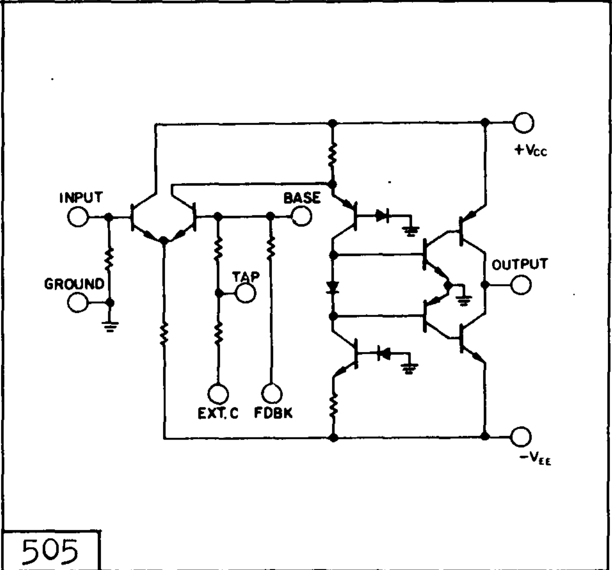
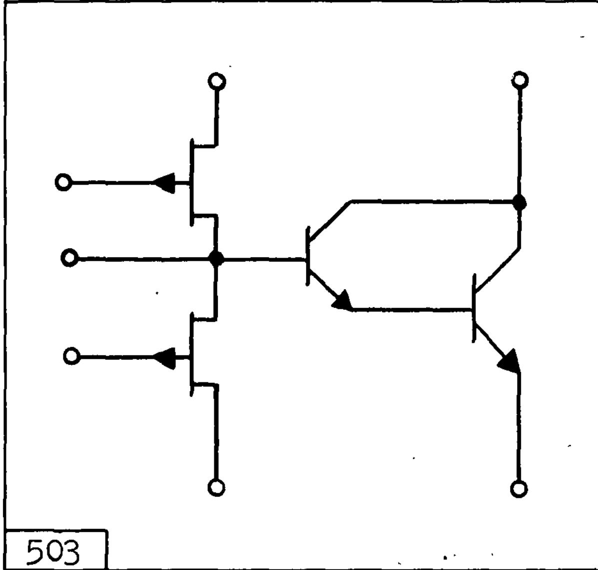

INPUT
BASE
+Vcc
OUTPUT
TAP
GROUND
EXT.C
FDBK
-VEE
505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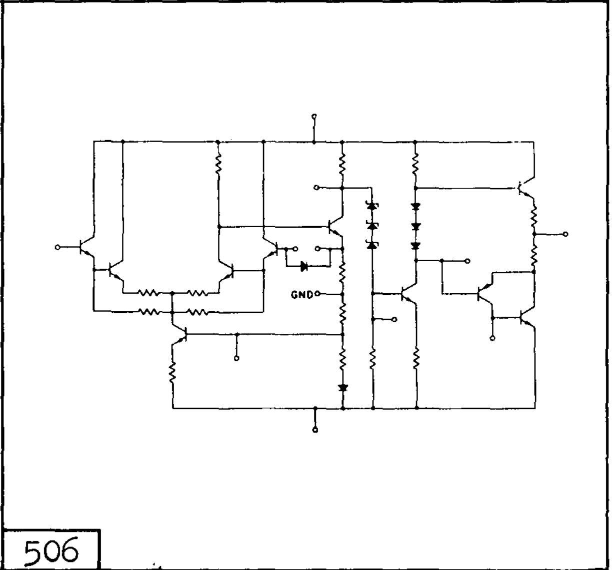
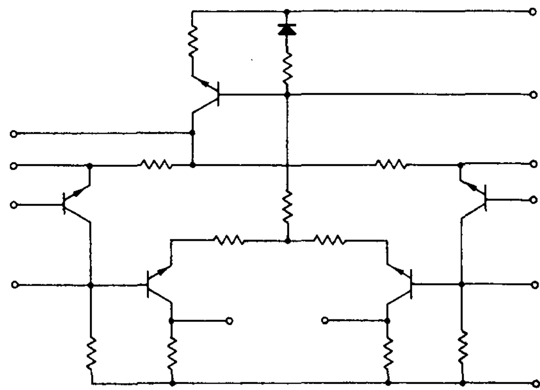

GND
506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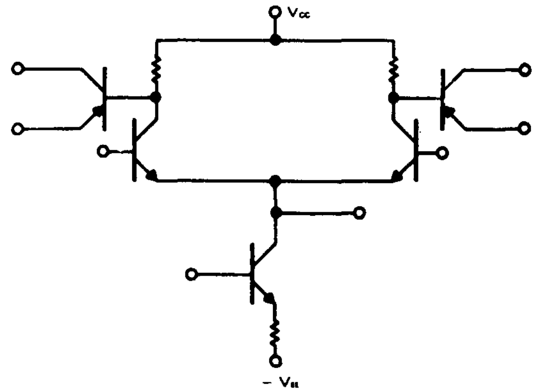

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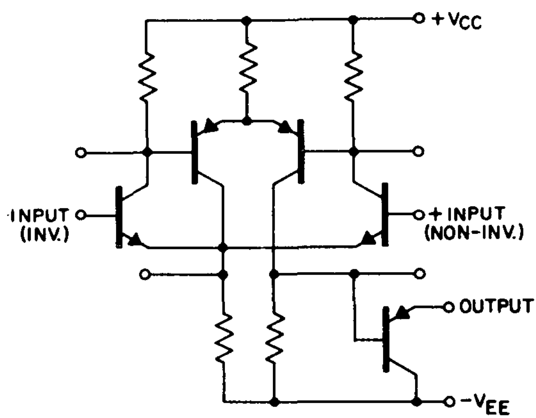

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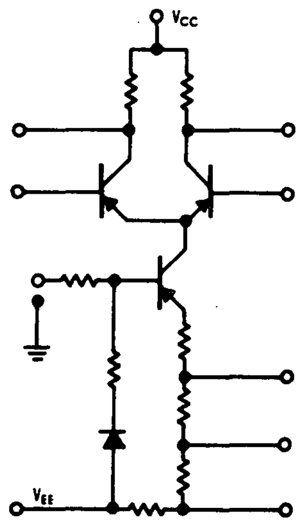

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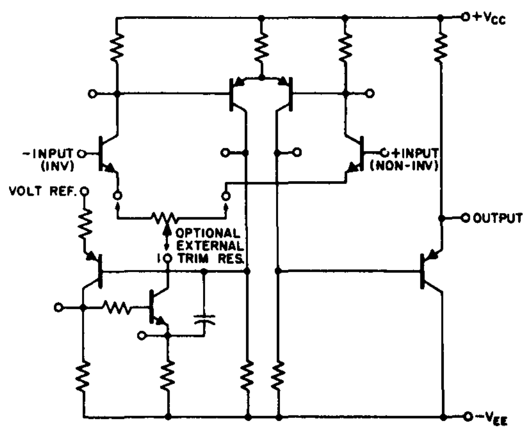

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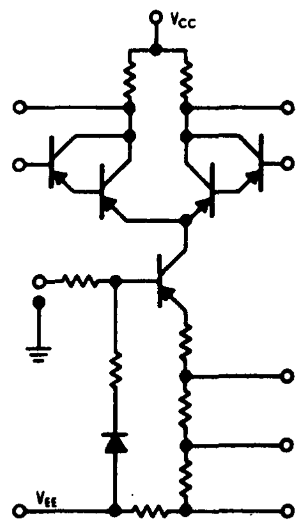

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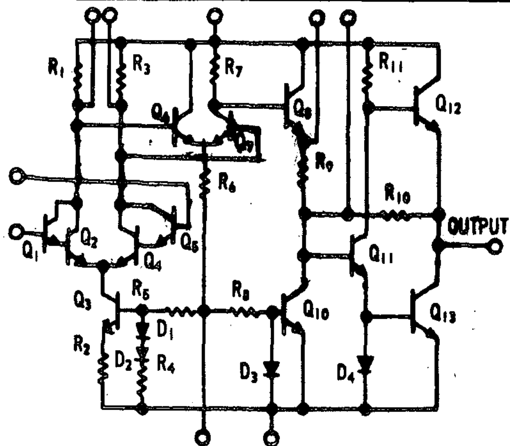
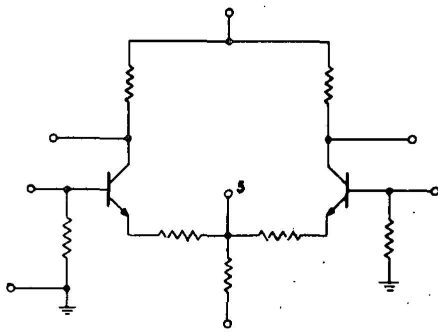


Note: Q1 and Q5 are omitted from MOTA MC1530. Inputs are to bases of Q2 and Q4.

513



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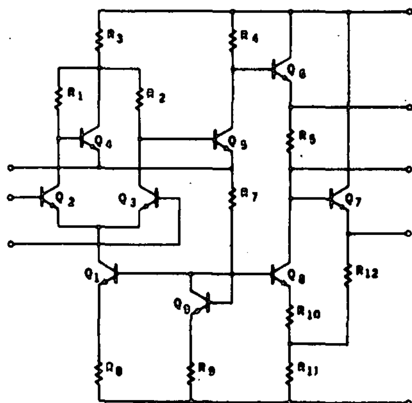

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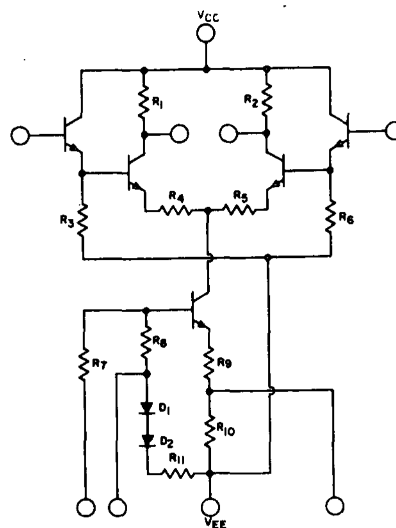

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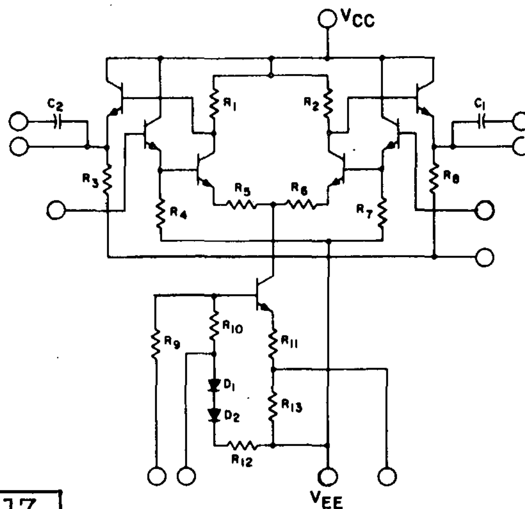

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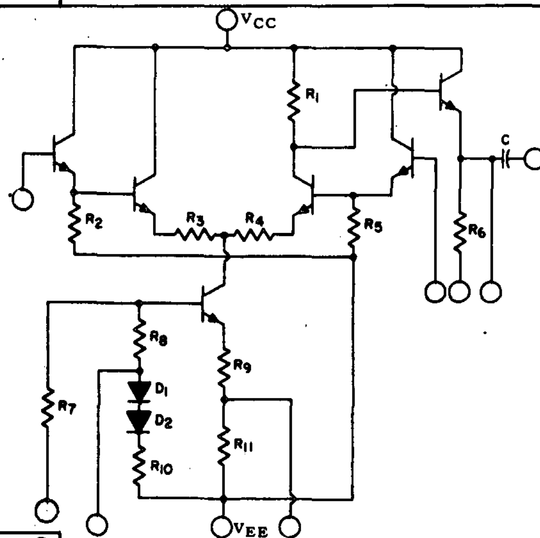

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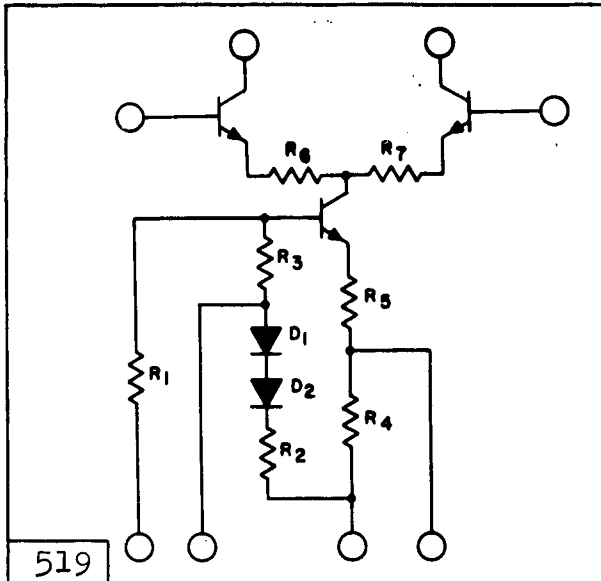

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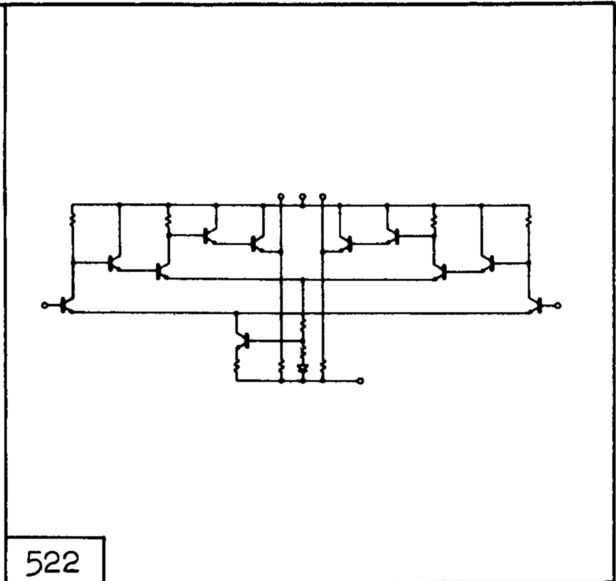
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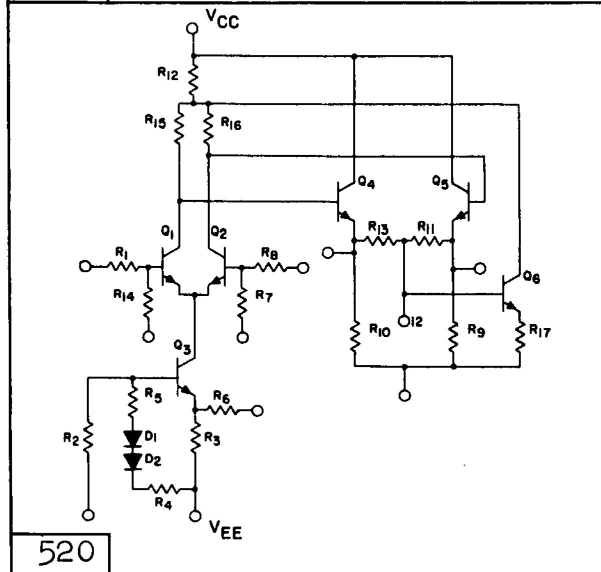

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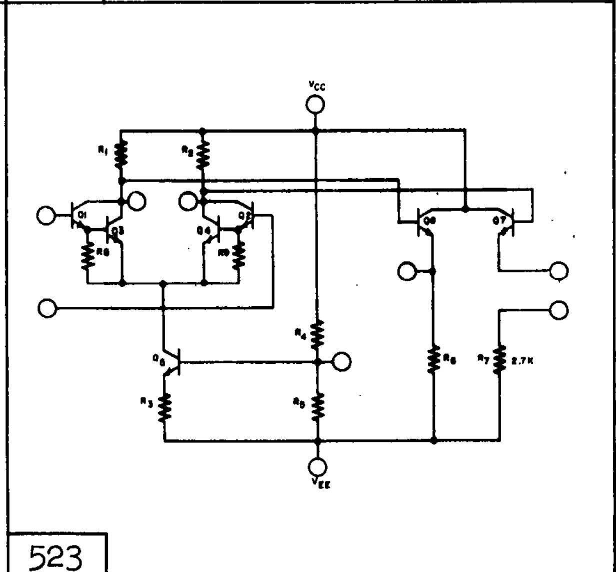

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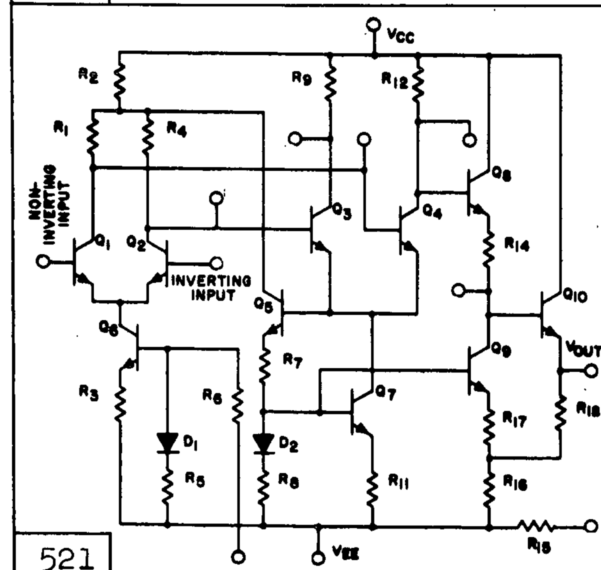

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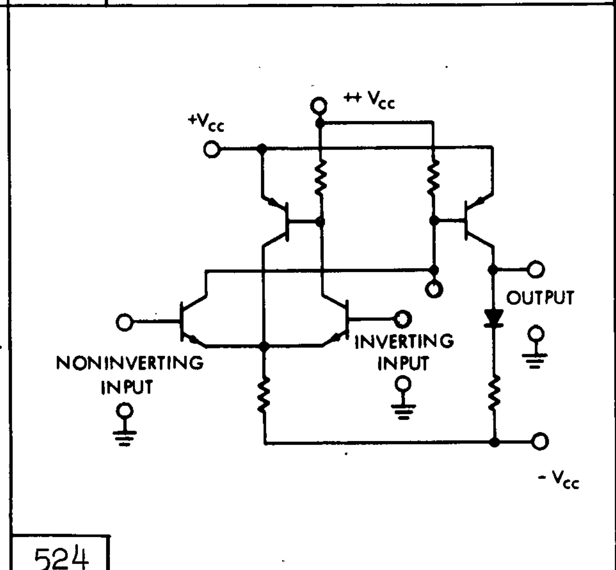

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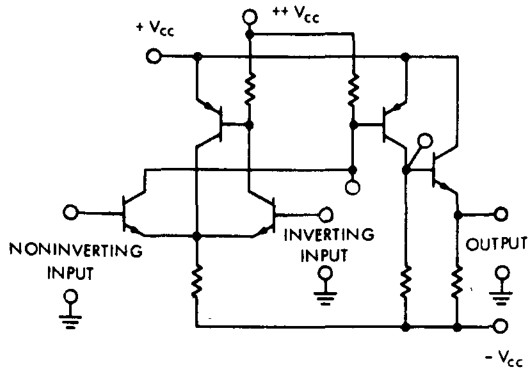

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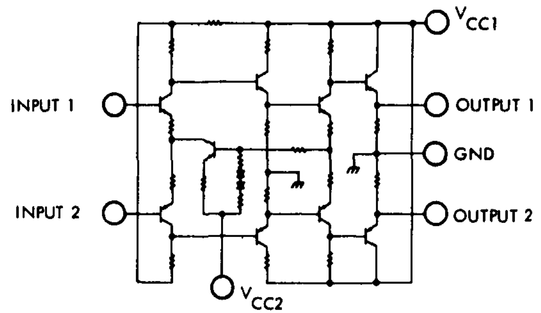

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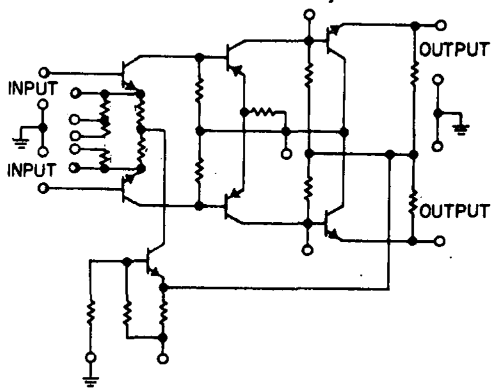

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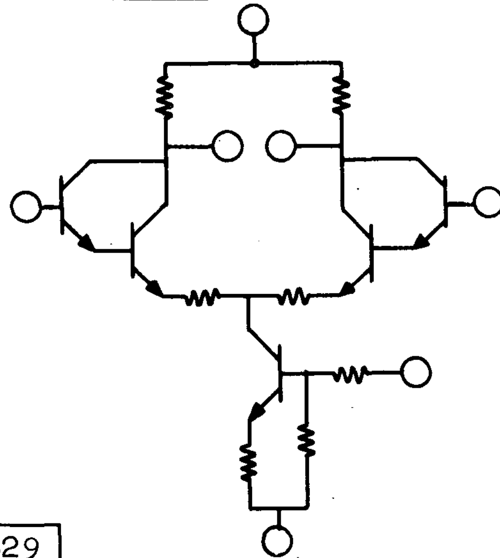

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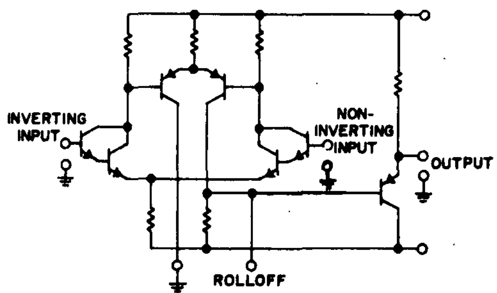

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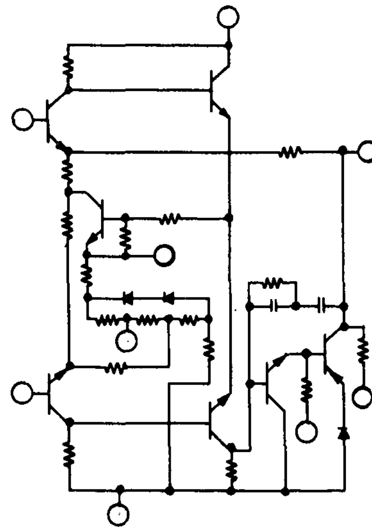

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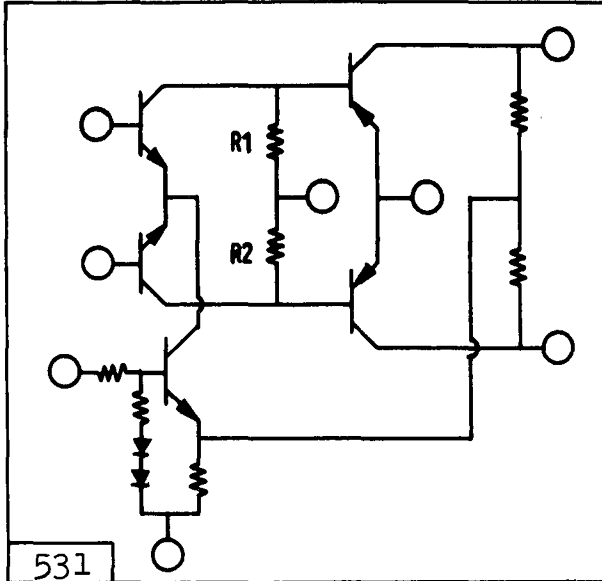

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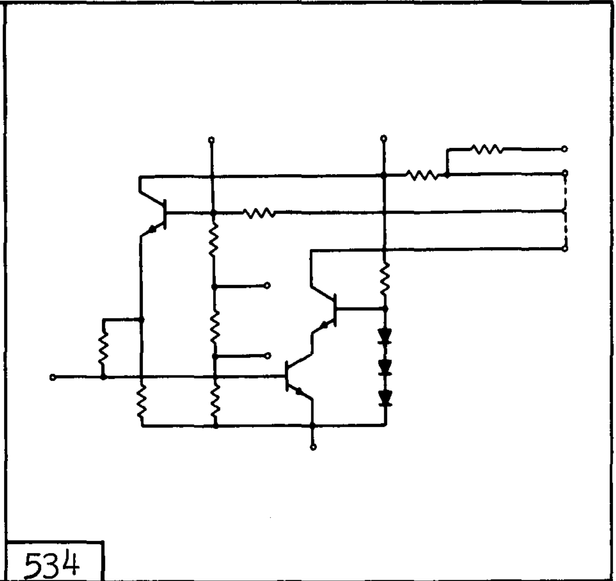
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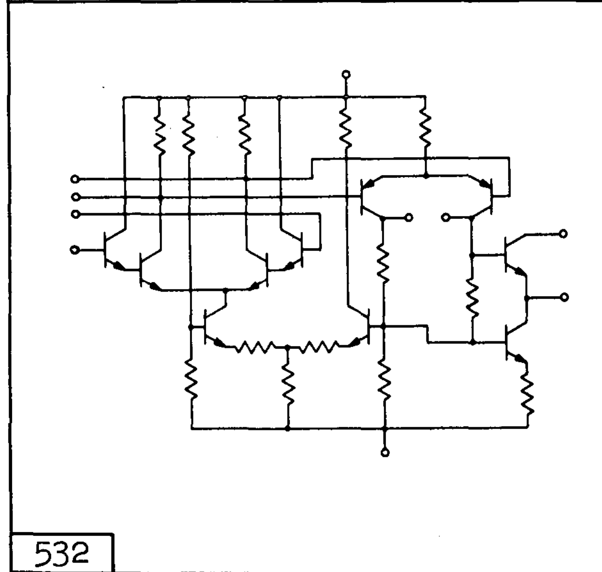
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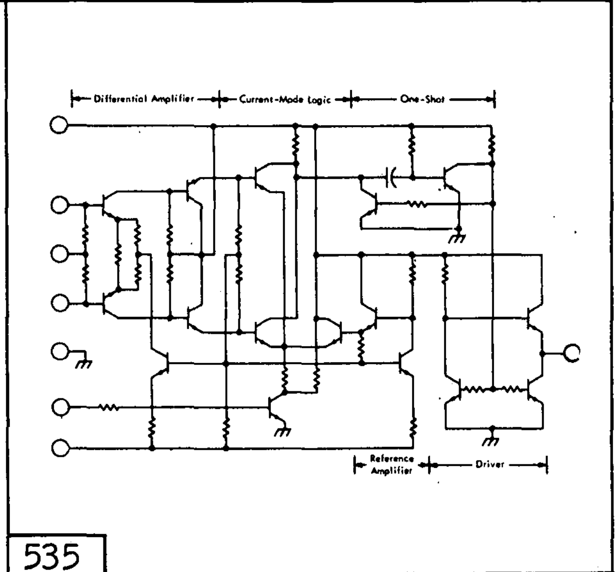

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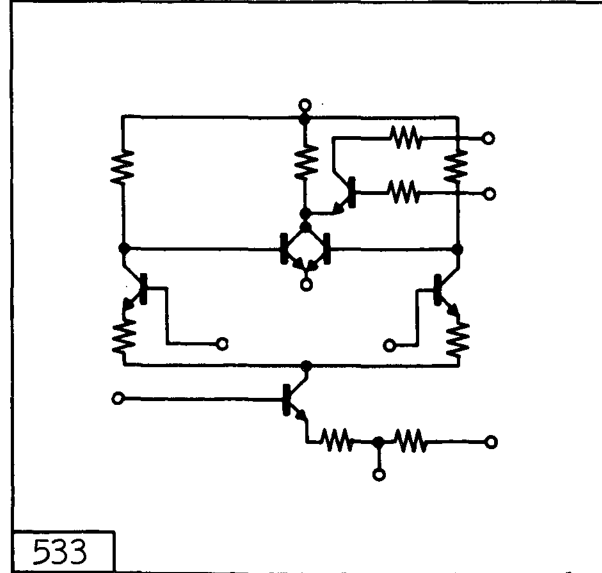
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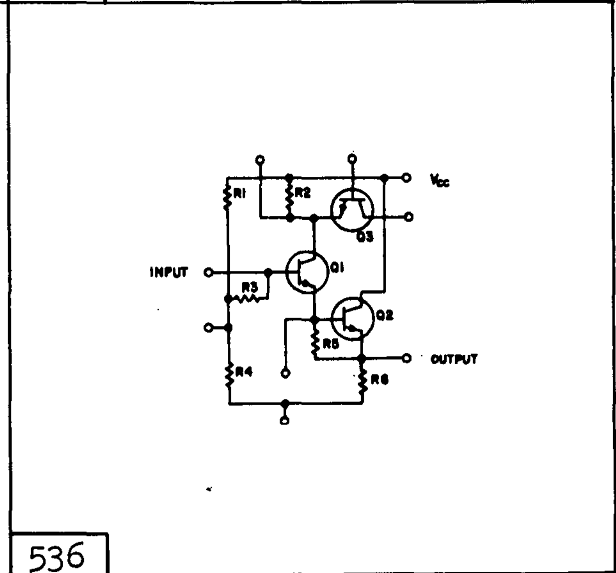

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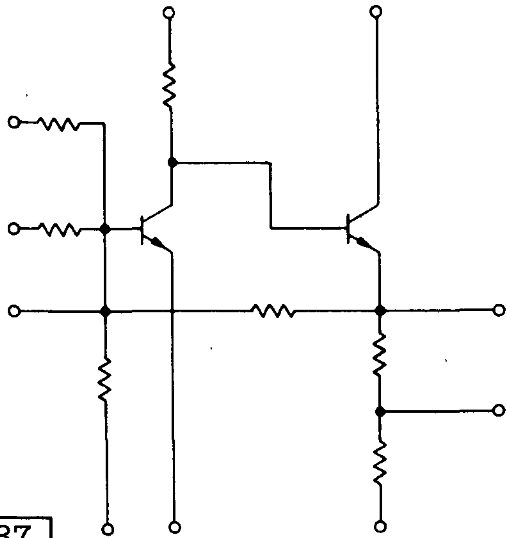

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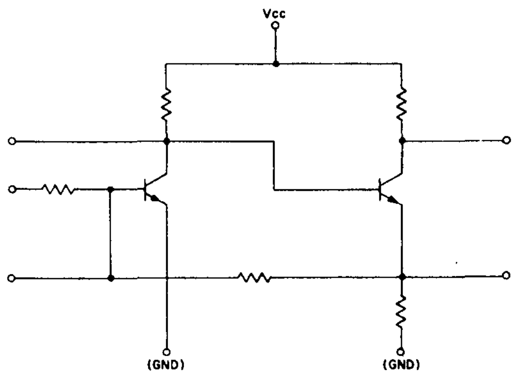

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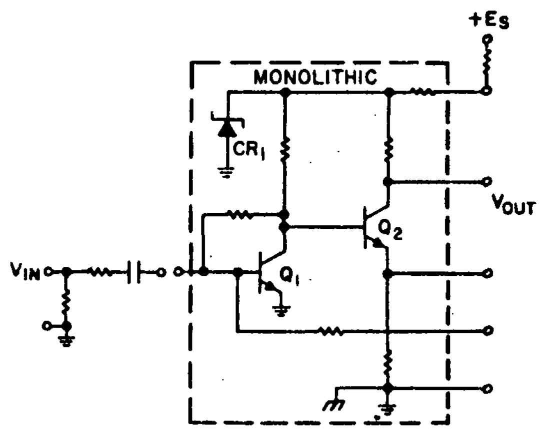

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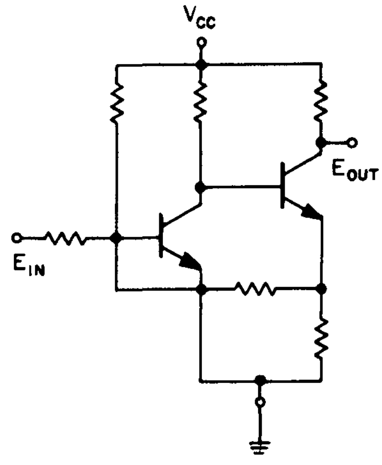

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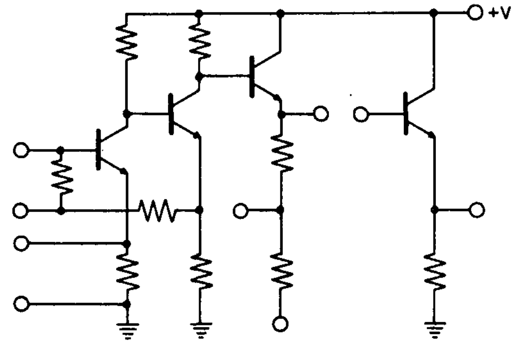

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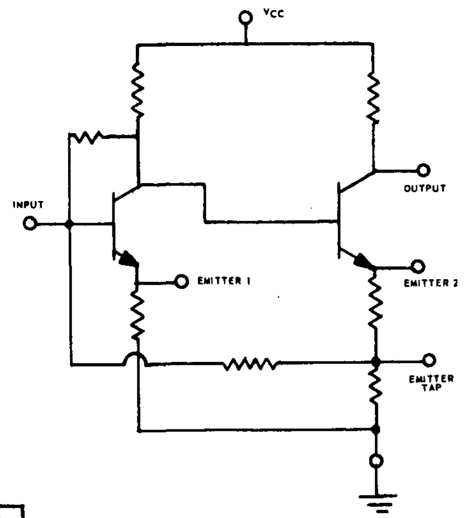

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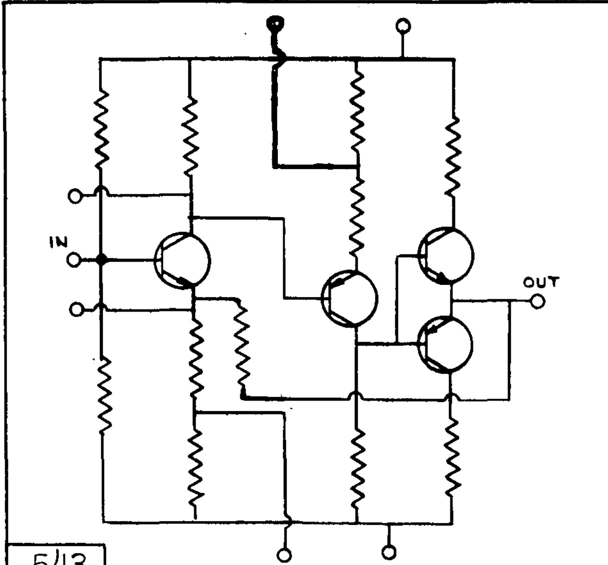
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OUT
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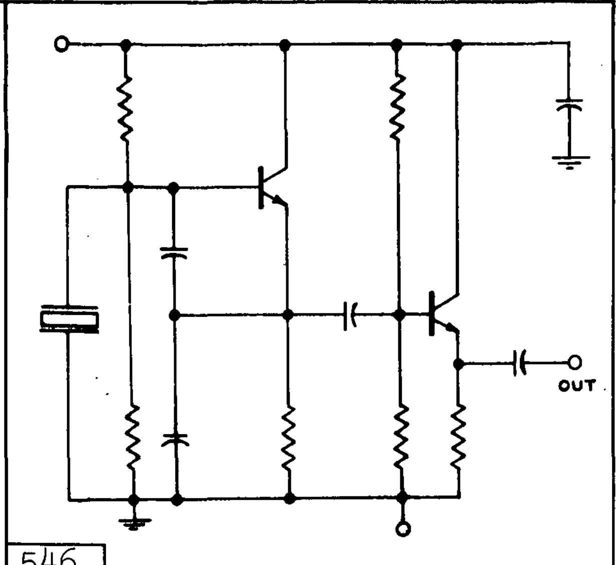
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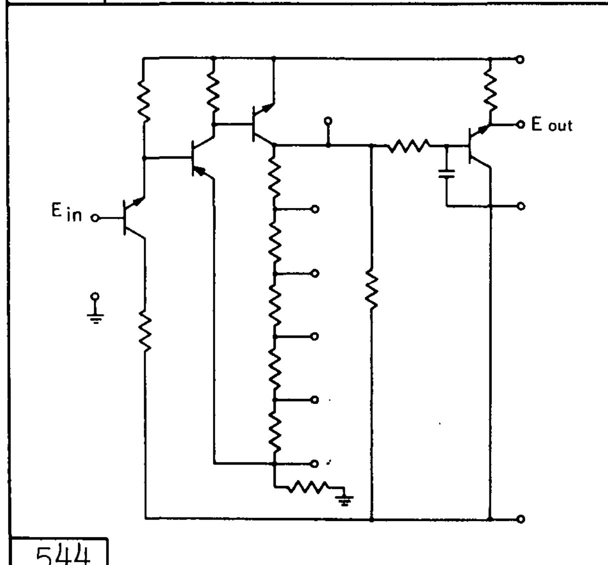
E out
E in
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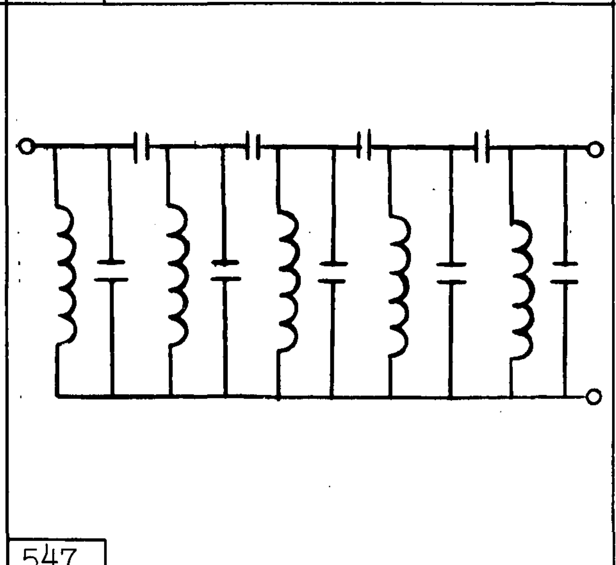
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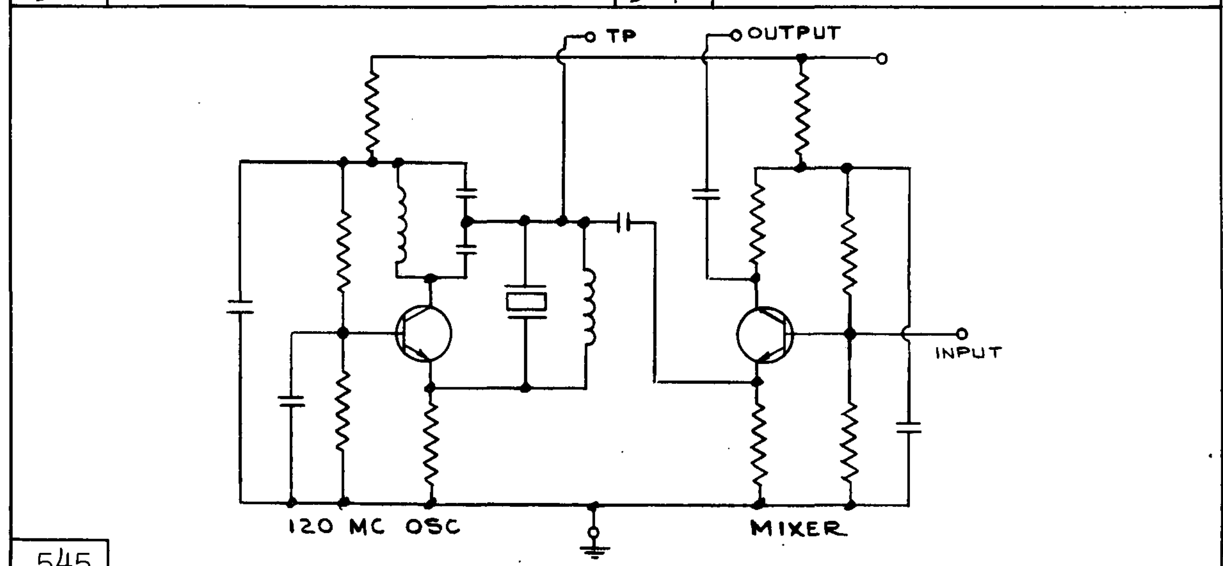
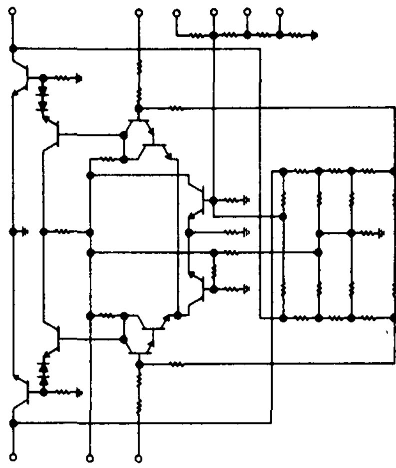

TP
OUTPUT
INPUT
120 MC OSC
MIXER
545



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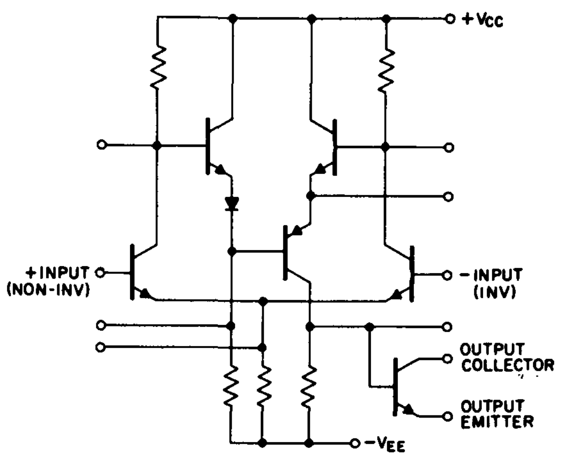

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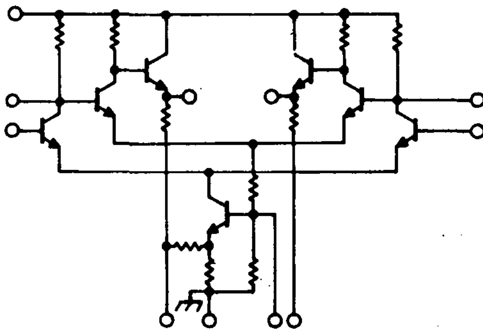

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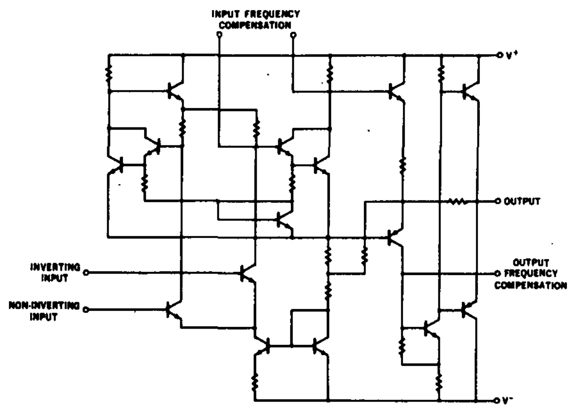

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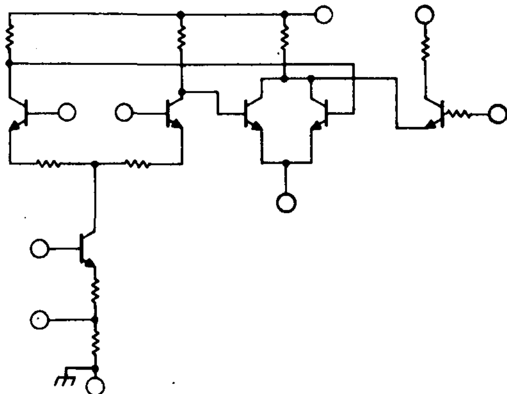

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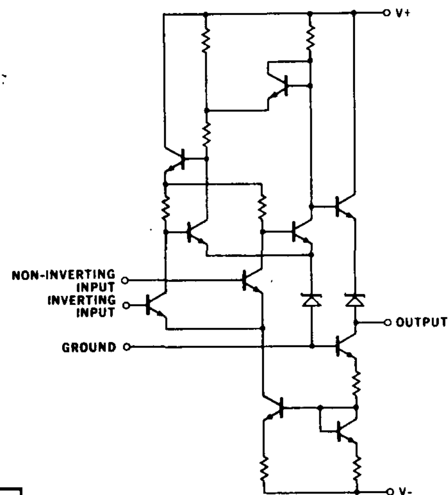

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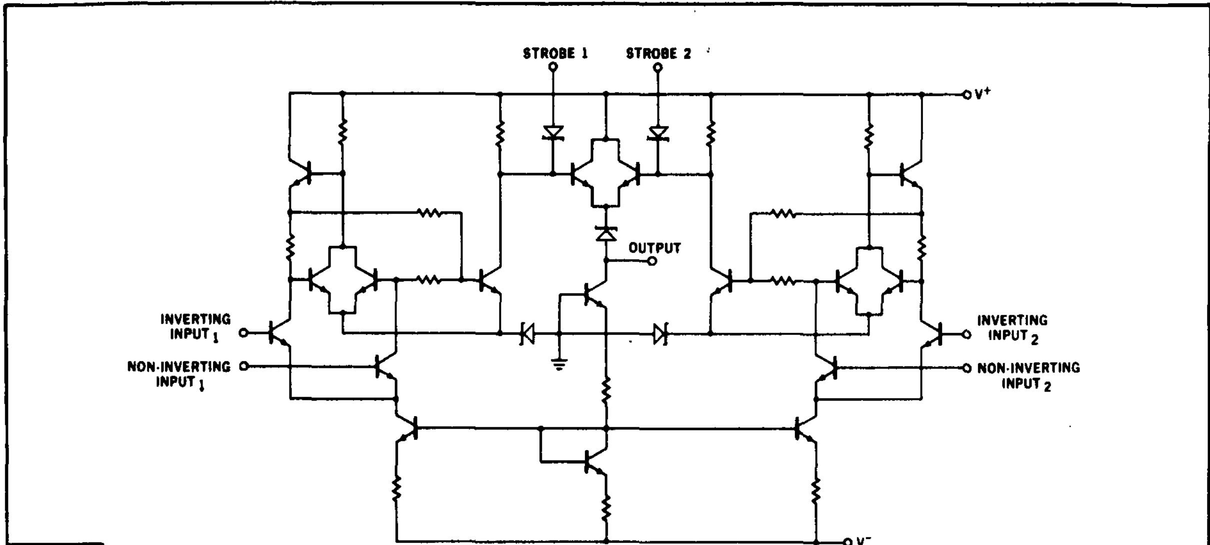

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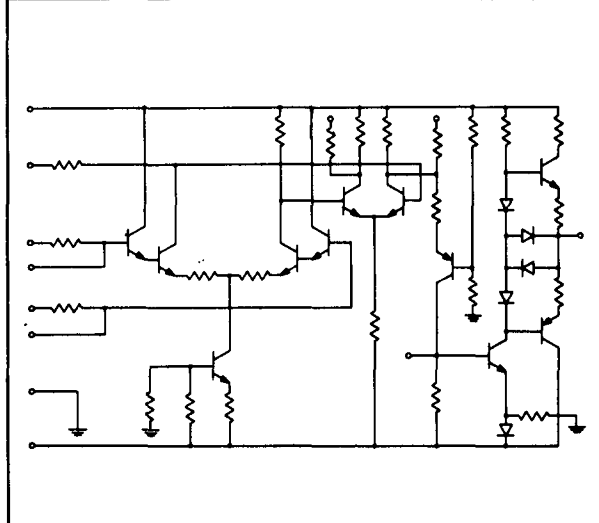

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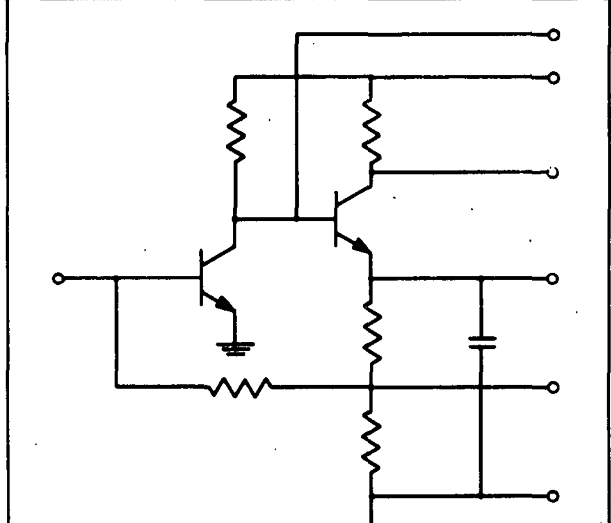

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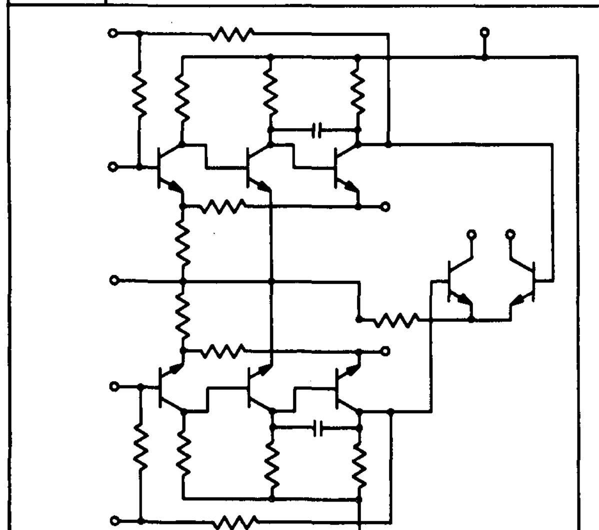

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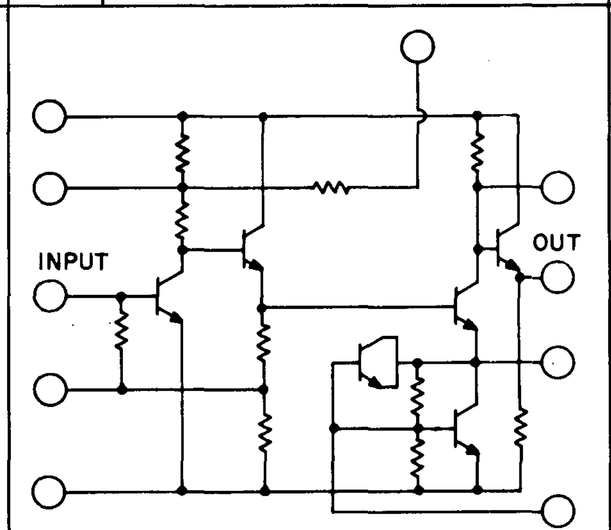
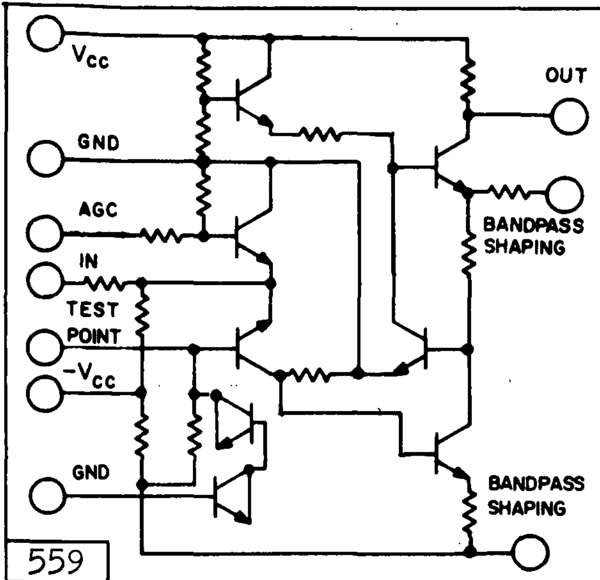
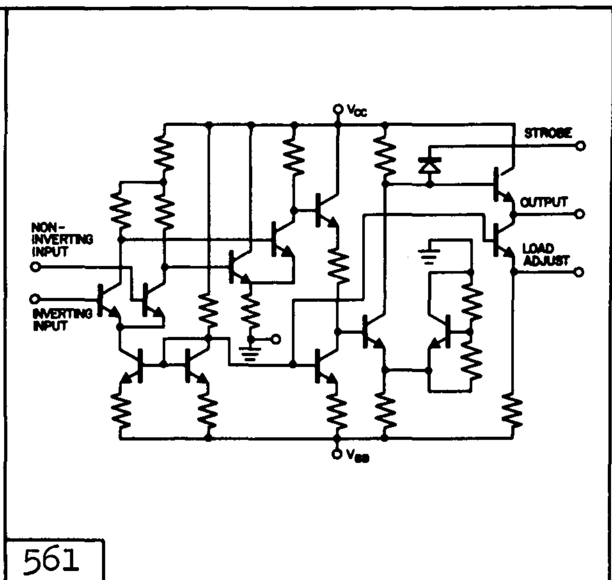
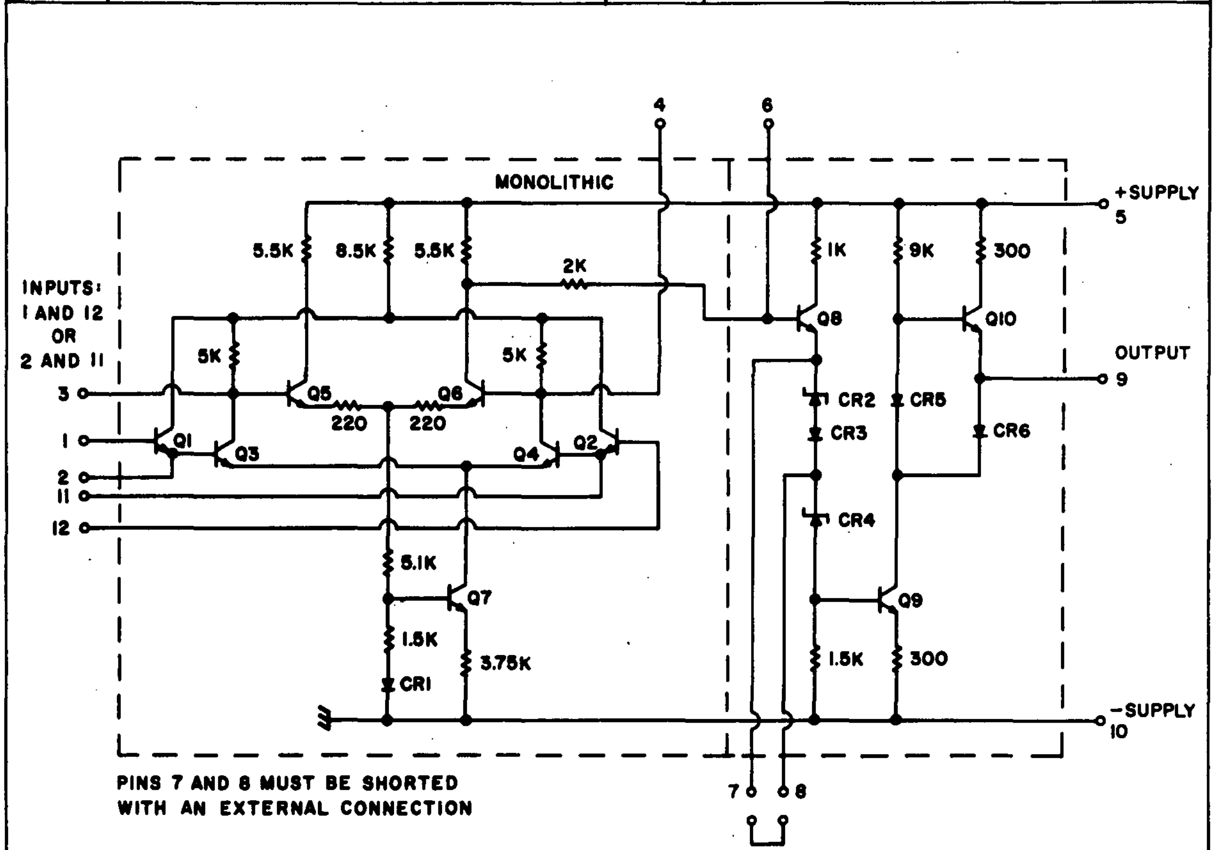


558

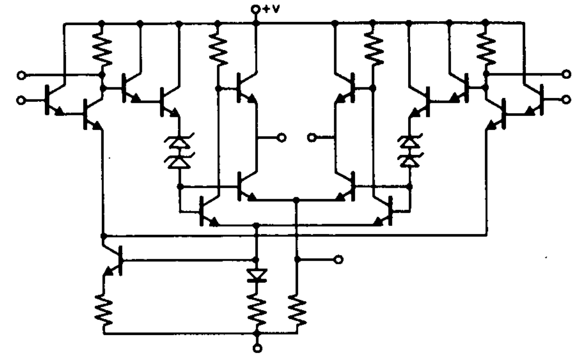






Note 1. The output stages of this amplifier operate in a class B condition. If class A operation of the output stages is desired, a 9K resistor is connected between pins 9 and 10.

560



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7.2.6 Printout of Catalog

The catalog of devices is stored on magnetic tape to facilitate updating, searching, and presentation in formats suitable for differing needs. The complete catalog is presented in two sections -- Digital and Linear -- on the following pages.

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DIGITAL CIRCUITS

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CIRCUIT DESCRIPTION	MFR	MFRS PART NUMBER	TECH	TYPE OF LOGIC	OPER. TEMP. CENTGRDE MIN	MAX	SUPPLY VOLTAGE VDC NO. 3	NO. 2	NO. 1	SUPPLY POWER MILLIWATTS AVE	ON	OFF	FAN-OUT	INPUT THRESHOLD VOLTS ZERO	ONE	NOISE IMMUNITY VOLTS	DELAY NANO-SECS	OPERATING SPEED MCPS	OUTPUT LEVEL VOLTS ZERO	ONE	PACKAGE TYPE
ADDER,DUAL	GI	MEM1000	K		-55	125		-12.0	-26.0	40				9.0	4.0	1.0			10.0	.10	82
AMPLIFIER,DUAL PULSE	VARO	8202	E	DTL	-55	125	6.0	3.0	-3.0	171			4	.50	3.00		10		.50	3.50	72
AMPLIFIER,PULSE	VARO	8201	E	DTL	-55	125	6.0	3.0	-3.0	171			4	.50	3.00		10		.50	3.50	72
AND-NAND,DUAL 1-2 INPUT	WMED	WS813	A	DTL	0	125			4.0	10			10	.70	1.75	.25			.45	2.50	53
AND-NAND,DUAL2-2 INP EX	TRAN	TNG7252	B	TTL	0	75			5.0	40			15	1.2	1.8	.800	* 18		.40	3.1	47,75
AND-NAND,4 INPUT	MEPC	640702	E	DTL	-55	125		6.0	-3.0				5				10	10	.60		60
AND-NOR,DUAL 2-3 INP EX	TRAN	TNG4251	B	TTL	-55	125			5.0		*30	*15	15	1.2	1.7	.700	* 18		.45	2.4	47
AND-NOR,DUAL 2-3 INP EX	TRAN	TNG4252	B	TTL	0	75			5.0		*30	*15	15	1.2	1.7	.700	* 18		.45	2.4	47
AND-NOR,DUAL 2-3 INP EX	TRAN	TNG4253	B	TTL	-55	125			5.0		*30	*15	7	1.2	1.7	.700	* 18		.45	2.4	47
AND-NOR,DUAL 2-3 INP EX	TRAN	TNG4254	B	TTL	0	75			5.0		*30	*15	7	1.2	1.7	.700	* 18		.45	2.4	47
AND-NOR,DUAL 2-3 INPUT	TRAN	TNG4211	B	TTL	-55	125			5.0		*30	*15	15	1.2	1.7	.700	* 18		.45	2.4	47
AND-NOR,DUAL 2-3 INPUT	TRAN	TNG4212	B	TTL	0	75			5.0		*30	*15	15	1.2	1.7	.700	* 18		.45	2.4	47
AND-NOR,DUAL 2-3 INPUT	TRAN	TNG4213	B	TTL	-55	125			5.0		*30	*15	7	1.2	1.7	.700	* 18		.45	2.4	47
AND-NOR,DUAL 2-3 INPUT	TRAN	TNG4214	B	TTL	0	75			5.0		*30	*15	7	1.2	1.7	.700	* 18		.45	2.4	47
AND-NOR,2-2 INPUT	TRAN	TNG3231	B	TTL	15	55			5.0		*30	*15	7	1.0	2.0	.500	* 25		.50	2.5	1
AND-NOR,2-2-2-3 INP EX	SW	SWG50	A	TTL	-55	125			5.0	20			15				14	20			49
AND-NOR,2-2-2-3 INP EX	SW	SWG51	A	TTL	-55	125			5.0	20			7				14	20			49
AND-NOR,2-2-2-3 INP EX	SW	SWG52	A	TTL	0	75			5.0	20			12				14	20			49
AND-NOR,2-2-2-3 INP EX	SW	SWG53	A	TTL	0	75			5.0	20			6				14	20			49
AND-NOR,2-2-2-3 INP EX	SYL	SG250	B	TTL	-55	125			5.0	43			11	1.1	1.7	.75	8		.45	3.00	40
AND-NOR,2-2-2-3 INP EX	SYL	SG251	B	TTL	-55	125			5.0	43			6	1.1	1.7	.75	8		.45	3.00	40
AND-NOR,2-2-2-3 INP EX	SYL	SG252	B	TTL	0	75			5.0	43			9	1.1	1.7	.75	8		.45	3.00	40
AND-NOR,2-2-2-3 INP EX	SYL	SG253	B	TTL	0	75			5.0	43			5	1.1	1.7	.75	8		.45	3.00	40
AND-NOR,2-2-2-3 INP EX	SYL	SG50	B	TTL	-55	125			5.0	30			15	1.20	1.70	.800	12	20	.40	3.20	40
AND-NOR,2-2-2-3 INP EX	SYL	SG51	B	TTL	-55	125			5.0	30			7	1.20	1.70	.800	12	20	.40	3.20	40
AND-NOR,2-2-2-3 INP EX	SYL	SG52	B	TTL	0	75			5.0	30			12	1.20	1.80	.800	12	20	.40	3.10	40
AND-NOR,2-2-2-3 INP EX	SYL	SG53	B	TTL	0	75			5.0	30			6	1.20	1.80	.800	12	20	.40	3.10	40
AND-NOR,2-2-2-3 INP EX	TRAN	TNG4415	B	TTL	-55	125			5.0		*30	*15	15	1.2	1.7	.700	* 18		.45	2.4	47
AND-NOR,2-2-2-3 INP EX	TRAN	TNG4416	B	TTL	0	75			5.0		*30	*15	15	1.2	1.7	.700	* 18		.45	2.4	47
AND-NOR,2-2-2-3 INP EX	TRAN	TNG4417	B	TTL	-55	125			5.0		*30	*15	7	1.2	1.7	.700	* 18		.45	2.4	47
AND-NOR,2-2-2-3 INP EX	TRAN	TNG4418	B	TTL	0	75			5.0		*30	*15	7	1.2	1.7	.700	* 18		.45	2.4	47
AND-NOR,2-2-3-3 INPUT	TRAN	TNG4511	B	TTL	-55	125			5.0		*30	*15		1.2	1.7		* 18				47
AND-NOR,2-2-3-3 INPUT	TRAN	TNG4512	B	TTL	0	75			5.0		*30	*15		1.2	1.7		* 18				47
AND-NOR,2EX-3 INPUT	AMEL	G12-003	F	DTL	-55	125			4.0	* 2			5	1.05	1.35	.750	115		.30	3.50	14
AND-NOR,3-3 INPUT	TRAN	TNG3215	B	TTL	-55	125			5.0		*30	*15	15	1.2	1.7	.700	* 18		.45	2.4	23,47
AND-NOR,3-3 INPUT	TRAN	TNG3216	B	TTL	0	75			5.0		*30	*15	15	1.2	1.7	.700	* 18		.45	2.4	23,47
AND-NOR,3-3 INPUT	TRAN	TNG3217	B	TTL	-55	125			5.0		*30	*15	7	1.2	1.7	.700	* 18		.45	2.4	23,47
AND-NOR,3-3 INPUT	TRAN	TNG3218	B	TTL	0	75			5.0		*30	*15	7	1.2	1.7	.700	* 18		.45	2.4	23,47
AND-NOR,3-3 INPUT	TRAN	TNG3245	B	TTL	-55	125			5.0		*30	*15	15	1.2	1.7	.700	* 10		.45	2.4	23,47
AND-NOR,3-3 INPUT	TRAN	TNG3246	B	TTL	0	75			5.0		*30	*15	15	1.2	1.7	.700	* 10		.45	2.4	23,47
AND-NOR,3-3 INPUT	TRAN	TNG3247	B	TTL	-55	125			5.0		*30	*15	7	1.2	1.7	.700	* 10		.45	2.4	23,47
AND-NOR,3-3 INPUT	TRAN	TNG3248	B	TTL	0	75			5.0		*30	*15	7	1.2	1.7	.700	* 10		.45	2.4	23,47
AND-NOR,3-3-3 INPUT	TRAN	TNG4311	B	TTL	0	75			5.0		*30	*15	7	1.2	1.7	.700	* 18		.45	2.4	47
AND-NOR,3-3-3 INPUT	TRAN	TNG4312	B	TTL	-55	125			5.0		*30	*15	7	1.2	1.7	.700	* 18		.45	2.4	47
AND-NOR,3-3-3 INPUT	TRAN	TNG4313	B	TTL	-55	125			5.0		*30	*15	15	1.2	1.7	.700	* 18		.45	2.4	47
AND-NOR,3-3-3 INPUT	TRAN	TNG4314	B	TTL	0	75			5.0		*30	*15	15	1.2	1.7	.700	* 18		.45	2.4	47
AND-NOR,3-3-3 INPUT EX	SW	SWG100	A	TTL	-55	125			5.0	25			15				15	20			49
AND-NOR,3-3-3 INPUT EX	SW	SWG101	A	TTL	-55	125			5.0	25			7				15	20			49
AND-NOR,3-3-3 INPUT EX	SW	SWG102	A	TTL	0	75			5.0	25			12				15	20			49

CIRCUIT DESCRIPTION	MFR	MFRS PART NUMBER	TECH	TYPE OF LOGIC	OPER. TEMP. CENTGRDE MIN	MAX	SUPPLY VOLTAGE VDC NO. 3	NO. 2	NO. 1	SUPPLY POWER MILLIWATTS AVF	ON	OFF	FAN-OUT	INPUT THRESHOLD VOLTS ZERO	ONE	NOISE IMMUNITY VOLTS	DELAY NANOSECS	OPERATING SPEED MCPS	OUTPUT LEVEL VOLTS ZERO	ONE	PACKAGE TYPE
AND-NOR,3-3-3 INPUT EX	SW	SWG103	A	TTL	0	75			5.0	25			6				15	20			49
AND-NOR,3-3-3 INPUT EX	SYL	SG100	B	TTL	-55	125			5.0	60			15	1.2	1.7	.800	12		.40	3.20	40
AND-NOR,3-3-3 INPUT EX	SYL	SG101	B	TTL	-55	125			5.0	60			7	1.2	1.7	.800	12		.40	3.20	40
AND-NOR,3-3-3 INPUT EX	SYL	SG102	B	TTL	0	75			5.0	23			12	1.20	1.80	.800	12	20	.40	3.10	40
AND-NOR,3-3-3 INPUT EX	SYL	SG103	B	TTL	0	75			5.0	23			6	1.20	1.80	.800	12	20	.40	3.10	40
AND-NOR,3-3-3 INPUT EX	TRAN	TNG4315	B	TTL	-55	125			5.0		*30	*15	15	1.2	1.7	.700	* 18		.45	2.4	47
AND-NOR,3-3-3 INPUT EX	TRAN	TNG4316	B	TTL	0	75			5.0		*30	*15	15	1.2	1.7	.700	* 18		.45	2.4	47
AND-NOR,3-3-3 INPUT EX	TRAN	TNG4317	B	TTL	-55	125			5.0		*30	*15	7	1.2	1.7	.700	* 18		.45	2.4	47
AND-NOR,3-3-3 INPUT EX	TRAN	TNG4318	B	TTL	0	75			5.0		*30	*15	7	1.2	1.7	.700	* 18		.45	2.4	47
AND-NOR,4-4 INPUT	TRAN	TNG3211	B	TTL	-55	125			5.0		20	10	* 20	1.20	1.70	.700	* 18		.45	2.4	23,47
AND-NOR,4-4 INPUT	TRAN	TNG3212	B	TTL	0	75			5.0		20	10	* 20	1.20	1.70	.700	* 18		.45	2.4	23,47
AND-NOR,4-4 INPUT	TRAN	TNG3213	B	TTL	-55	125			5.0		20	10	* 7	1.20	1.70	.700	* 18		.45	2.4	23,47
AND-NOR,4-4 INPUT	TRAN	TNG3214	B	TTL	0	75			5.0		20	10	* 7	1.20	1.70	.700	* 18		.45	2.4	23,47
AND-NOR,4-4 INPUT	TRAN	TNG3241	B	TTL	-55	125			5.0		*30	*15	15	1.2	1.7	.700	* 10		.45	2.4	23,47
AND-NOR,4-4 INPUT	TRAN	TNG3242	B	TTL	0	75			5.0		*30	*15	15	1.2	1.7	.700	* 10		.45	2.4	23,47
AND-NOR,4-4 INPUT	TRAN	TNG3243	B	TTL	-55	125			5.0		*30	*15	7	1.2	1.7	.700	* 10		.45	2.4	23,47
AND-NOR,4-4 INPUT	TRAN	TNG3244	B	TTL	0	75			5.0		*30	*15	7	1.2	1.7	.700	* 10		.45	2.4	23,47
AND-NOR,4-4 INPUT EX	SW	SWG110	A	TTL	-55	125			5.0	20			15				13	20			49
AND-NOR,4-4 INPUT EX	SW	SWG111	A	TTL	-55	125			5.0	20			7				13	20			49
AND-NOR,4-4 INPUT EX	SW	SWG112	A	TTL	0	75			5.0	20			12				13	20			49
AND-NOR,4-4 INPUT EX	SW	SWG113	A	TTL	0	75			5.0	20			6				13	20			49
AND-NOR,4-4 INPUT EX	SYL	SG110	B	TTL	-55	125			5.0	20			15	1.20	1.70	.800	12	20	.40	3.20	40
AND-NOR,4-4 INPUT EX	SYL	SG111	B	TTL	-55	125			5.0	20			7	1.20	1.70	.800	12	20	.40	3.20	40
AND-NOR,4-4 INPUT EX	SYL	SG112	B	TTL	0	75			5.0	20			12	1.20	1.80	.800	12	20	.40	3.10	40
AND-NOR,4-4 INPUT EX	SYL	SG113	B	TTL	0	75			5.0	20			6	1.20	1.80	.800	12	20	.40	3.10	40
AND-NOR,4-4 INPUT EX	SYL	SG210	B	TTL	-55	125			5.0	30			11	1.1	1.7	.65	7		.45	3.00	40
AND-NOR,4-4 INPUT EX	SYL	SG211	B	TTL	-55	125			5.0	30			6	1.1	1.7	.65	7		.45	3.00	40
AND-NOR,4-4 INPUT EX	SYL	SG212	B	TTL	0	75			5.0	30			9	1.1	1.7	.65	7		.45	3.00	40
AND-NOR,4-4 INPUT EX	SYL	SG213	B	TTL	0	75			5.0	30			5	1.1	1.7	.65	7		.45	3.00	40
AND-NOR,4-4 INPUT EX	TRAN	TNG3251	B	TTL	-55	125			5.0		*30	*15	15	1.2	1.7	.700	* 18		.45	2.4	47
AND-NOR,4-4 INPUT EX	TRAN	TNG3252	B	TTL	0	75			5.0		*30	*15	15	1.2	1.7	.700	* 18		.45	2.4	47
AND-NOR,4-4 INPUT EX	TRAN	TNG3253	B	TTL	-55	125			5.0		*30	*15	7	1.2	1.7	.700	* 18		.45	2.4	47
AND-NOR,4-4 INPUT EX	TRAN	TNG3254	B	TTL	0	75			5.0		*30	*15	7	1.2	1.7	.700	* 18		.45	2.4	47
AND-OR-NAND,1-2-2-2 INP	WMED	WS810	A	DTL	0	125			4.0	*20			10	.70	1.75	.25	* 50		.45	2.50	53
AND-OR-NAND,2-2-2 INPUT	WMED	WS814	A	DTL	0	125			4.0	20			10	.70	1.75	.25	* 50		.45	2.50	53
AND-OR-NAND,2-2-3 INPUT	WMED	WS812	A	DTL	0	125			4.0	*15			10	.70	1.75	.25	* 50		.45	2.50	53
AND-OR,DUAL 2-2 INP EX	TRAN	TNG7254	B	TTL	0	75			5.0	40			7	1.2	1.8	.800	* 18		.40	3.1	47,75
AND/NAND/NOR,5 INPUT EX	TI	SN531	F	DTL	-55	125			3.5	18			* 10	.30	1.70		25		.30	2.20	74
AND,DUAL 2-3 INPUT	TI	SN534	F	DTL	-55	125		3.5	-3.0	*40			4				5				74
AND,DUAL 3 INPUT	FSC	CS705	A		-55	125			* 8.0	K30							L 3				11,55
AND,DUAL 3 INPUT	GME	254D3	A	DTL	-55	125			* 8.0	K30							L 4				17,59
AND,DUAL 3 INPUT	PHIL	PL9986	A	TTL	-55	125			3.0	E23			15	.50	.85		25		.23	1.00	41
AND,DUAL 3 INPUT	SIGN	CS705	A	DTL	-55	125			* 8.0	K30							*L 4				12,52
AND,DUAL 3 INPUT	SIGN	LU306	A		10	55			4.5	5			* 10				15				2
AND,DUAL 3 INPUT	SIGN	SU306	A	TTL	-20	85			4.5	10							25				2,52
AND,DUAL 3 INPUT EX	MOTA	MC215	A	DTL	-55	125			* 8.0	K30							L 4				4,50
AND,DUAL 3 INPUT EX	MOTA	MC265	A	DTL	0	75			* 8.0	K30							L 4				4
AND,DUAL 3 INPUT EX	TRAN	TNG6262	B	TTL	0	75			5.0	40			15	1.2	1.8	.800	* 18		.40	3.1	47,75
AND,DUAL 3 INPUT EX	TRAN	TNG6264	B	TTL	0	75			5.0	40			7	1.2	1.8	.800	* 18		.40	3.1	47,75

CIRCUIT DESCRIPTION	MFR	MFRS PART NUMBER	TECH	TYPE OF LOGIC	OPER. TEMP. CENTGRDE MIN	MAX	SUPPLY VOLTAGE VDC NO. 3	NO. 2	NO. 1	SUPPLY POWER MILLIWATTS AVE	ON	OFF	FAN-OUT	INPUT THRESHOLD VOLTS ZERO	ONE	NOISE IMMUNITY VOLTS	DELAY NANO-SECS	OPERATING SPEED MCPS	OUTPUT LEVEL VOLTS ZERO	ONE	PACKAGE TYPE
AND,DUAL 4 INPUT	FSC	CTL954	A	RTL	15	55		4.5	-2.0	55			15				4				75
AND,DUAL 4 INPUT	TRAN	TNG6222	B	TTL	0	75			5.0	40			15	1.2	1.8	.800	* 18		.40	3.1	47,75
AND,DUAL 4 INPUT	TRAN	TNG6224	B	TTL	0	75			5.0	40			7	1.2	1.8	.800	* 18		.40	3.1	47,75
AND,DUAL 4 INPUT EX	TRAN	TNG6252	B	TTL	0	75			5.0	40			15	1.2	1.8	.800	* 18		.40	3.1	47,75
AND,DUAL 4 INPUT EX	TRAN	TNG6254	B	TTL	0	75			5.0	40			7	1.2	1.8	.800	* 18		.40	3.1	47,75
AND,DUAL 5-7 INPUT	VARO	8210	E	DTL	-55	125			6.0												72
AND,QUAD 2-2-3-3 INPUT	VARO	8208	E	DTL	-55	125			6.0												72
AND,TRIPLE 2-2-3 INPUT	FSC	CTL953	A	RTL	15	55		4.5	-2.0	55			15				4				75
AND,TRIPLE 2-2-6 INPUT	VARO	8207	E	DTL	-55	125			6.0												72
AND,TRIPLE 3 INPUT	VARO	8209	E	DTL	-55	125			6.0												72
AND,1-1-1-2 INPUT	MOTA	MC1113	F	DTL	-55	125			*10.0	K20							L 15				13
AND,2 INPUT EXPANDABLE	PHIL	PL9610	A	RTL	-55	125		6.5	-6.5					1.0	1.5		25				
AND,2-2-2 INPUT	MOTA	MC1112	F	DTL	-55	125			*10.0	K20							L 15				13
AND,3 INPUT	PHIL	PL9606	A	RTL	-55	125		10.0	3.0		170			.49	.82					.88	
AND,3-4 INPUT	MOTA	MC1111	F	DTL	-55	125			*10.0	K20							L 20				13
AND,4 INPUT EXPANDABLE	TRAN	TNG6522	B	TTL	0	75			5.0	80			40	1.2	1.8	.800	* 18		.40	3.1	47,75
AND,4 INPUT EXPANDABLE	TRAN	TNG6524	B	TTL	0	75			5.0	80			24	1.2	1.8	.800	* 18		.40	3.1	47,75
AND,5 INPUT EXPANDABLE	TI	SN532	F	DTL	-55	125		3.5	-3.0	*20			4				5				74
AND,6 INPUT	AMEL	E12-001	F	DTL	-55	125			*10.0												14,63
AND,6 INPUT	FSC	SE105	A		-55	125			* 8.0	K30							L 3				11,55
AND,6 INPUT	MOTA	MC203	A	DTL	-55	125			* 8.0	K30							L 4				4,50
AND,6 INPUT	MOTA	MC253	A	DTL	0	75			* 8.0	K30							L 4				4
AND,6 INPUT	SIGN	LU305	A		10	55			4.5	5			* 10				15				2
AND,6 INPUT	SIGN	SU305	A	TTL	-20	85			4.5	5			* 10				25				2,52
AND,6 INPUT EXPANDABLE	GME	25466	A	DTL	-55	125			* 8.0	K30							L 4				17,59
AND,6 INPUT EXPANDABLE	SIGN	SE105	A	DTL	-55	125			* 8.0	K30							*L 4				12,52
AND,8 INPUT	FSC	CTL955	A	RTL	15	55		4.5	-2.0	55			15				4				75
AND,8 INPUT	MOTA	MC1114	F	DTL	-55	125			*10.0	K20							L 15				13
CONVERTER,BCD TO B	GME	PL4G03	K		-20	70		-24.0	-12.0					9.0	3.0	1.0	1000		10.0	2.0	88,77
CONVERTER,BCD TO D	GME	PL4G02	K		-20	70		-24.0	-12.0					9.0	3.0	1.0	800		10.0	2.0	88
CONVERTER,D TO A	GELM	7736079	N		-55	125		28.0	-1.0*	X20								1.5			79
CONVERTER,D TO A	GME	PL4S02	K		-55	125		-12.0	-24.0	*75				3.00	9.00			.100			45,77
COUNTER ADAPTER	AMEL	C-INDUS	F	RTL	0	70			3.0	50				.55	.85		* 50		.30		5,6
COUNTER ADAPTER	AMEL	C-PREM	F	RTL	-55	125			3.0	50				.55	.80		* 38		.25		5,54
COUNTER ADAPTER	AMEL	C-STAND	F	RTL	-55	125			3.0	50				.56	.82		* 38		.30		5,54
COUNTER ADAPTER	FSC	L901	A	RTL	-55	125			3.0	55			5	.56	.82		* 26		.30		1,6
COUNTER ADAPTER	FSC	L901C	A	RTL	0	100			3.0	55			5	.55	.84		* 26		.40		1,6
COUNTER ADAPTER	MOTA	MC801	F	RTL	0	100			3.0	55			5	.55	.84		* 42		.40	.34	4
COUNTER ADAPTER	MOTA	MC901	F	RTL	-55	125			3.0	55			5	.56	.82	.022	* 42		.30	.84	4
COUNTER ADAPTER	NSC	NB1001	A	RTL	-55	125			3.0	55			13	.69	.77		16		.15		2
COUNTER ADAPTER	NSC	NB2001	A	RTL	0	100			3.0	55			13	.69	.77		16		.15		2
COUNTER ADAPTER	PHIL	PL901	A	RTL	-55	125			3.0	55			5	.56	.82	.260	* 26		.30	.34	1,41
COUNTER,DECADE	FSC	CL958	A		0	75			4.5	190				.45	1.40		* 200	* 2	.45	1.40	1
COUNTER,DECADE	GME	PL4C01	K		-55	125		-12.0	-24.0	*75				3.00	9.00	1.000	800	.100	2.00	10.0	88
COUNTER,DUAL DECADE	GME	PL5050	K		-55	125			-25.0	25				-4.0	-13	1.000		*. 5	-3.0	-14	45
DIODE ARRAY,DUAL 3 INP	FSC	CS709	A		-55	125			* 8.0	K30							L 3				11,55
DIODE ARRAY,DUAL 3 INP	GME	254DD	A	DTL	-55	125			* 8.0								4				3,70
DIODE ARRAY,DUAL 3 INP	MOTA	MC217	A	DTL	-55	125			* 8.0	K30							*L 4				13,50
DIODE ARRAY,DUAL 3 INP	MOTA	MC267	F	DTL	0	75			* 8.0	K30							L 4				13,50

CIRCUIT DESCRIPTION	MFR	MFRS PART NUMBER	TECH	TYPE OF LOGIC	OPER. TEMP. CENTGRDE MIN	MAX	SUPPLY VOLTAGE VDC NO. 3	NO. 2	NO. 1	SUPPLY POWER MILLIWATTS AVE	ON	OFF	FAN-OUT	INPUT THRESHOLD VOLTS ZERO	ONE	NOISE IMMU-NITY VOLTS	DELAY NANO-SECS	OPER-ATING SPEED MCPS	OUTPUT LEVEL VOLTS ZERO	ONE	PACK-AGE TYPE
DIODE ARRAY,DUAL 3 INP	SIGN	CS709	A	DTL	-55	125			* 8.0	K30							*L 4				12,52
DIODE ARRAY,DUAL 4 INP	FSC	DTL933	A	DTL	-55	125			* 8.0	K10							*L 4				44
DIODE ARRAY,DUAL 4 INP	FSC	FL93329	A	DTL	0	70			* 8.0	K10							*L 4				44
DIODE ARRAY,DUAL 4 INP	MOTA	MC833F	A	DTL	0	75			* 8.0	K10											39
DIODE ARRAY,DUAL 4 INP	MOTA	MC933F	A	DTL	-55	125			* 8.0	K10											39
DIODE ARRAY,DUAL 4 INP	PHIL	PL933	A	DTL	-55	125			* 8.0	K10							*L 4				41
DIODE ARRAY,DUAL 4 INP	SW	SW933	A	DTL	-55	125			* 5.0	K50							L 3				27,49
DIODE ARRAY,DUAL 5 INP	SIGN	SE106	A	DTL	-55	125			* 8.0	K30							*L 4				81
DIODE ARRAY,DUAL3-4 INP	MOTA	MC833G	A	DTL	0	75			* 8.0	K10											11
DIODE ARRAY,DUAL3-4 INP	MOTA	MC933G	A	DTL	-55	125			* 8.0	K10											11
DIODE ARRAY,DUAL3-4 INP	RAY	RM217	A	DTL	-55	125			*15.0	K30							*L 4				21,43
DIODE ARRAY,DUAL3-4 INP	WMED	WC217	A	DTL	0	75			6.0	8			6	1.0	1.8		30		.45		21,43
DIODE ARRAY,DUAL3-4 INP	WMED	WM217	A	DTL	-55	125			*15.0	K30							*L 4				21,43
DIODE ARRAY,QUAD 2 INP	SIGN	CS731	A	DTL	-55	125			* 8.0	K30							*L 4				81
DIODE ARRAY,TRIPLE3-3-4	RAY	RM227	A	DTL	-55	125			*15.0	K30							*L 4				43
DIODE ARRAY,TRIPLE3-3-4	WMED	WC227	A	DTL	0	75			6.0	8			6	1.0	1.8		30		.45		43
DIODE ARRAY,TRIPLE3-3-4	WMED	WM227	A	DTL	-55	125			*15.0	K30							*L 4				43
DIODE ARRAY,12 INPUT	SIGN	CS732	A	DTL	-55	125			* 8.0	K30							*L 4				81
DIODE ARRAY,6 INPUT	SILX	A04	A	DTL	-55	125			* 6.0	K2							*L 4				7,46
DIODE ARRAY,8 INPUT	FSC	FSA2002	A		-65	175			* 40	*D4							*L 25				11,66
DIODE ARRAY,8 INPUT	FSC	FSA2003	A		-65	175			* 40	*D4							*L 25				11,66
DIODE ARRAY,9 INPUT	MOTA	MC1116	F	DTL	-55	125			*40.0	KD3							L 90				13
DIODE ARRAY,9 INPUT	MOTA	MC1117	F	DTL	-55	125			*40.0	KD3							L 90				13
DIODE MATRIX,10X10	RAD	RM65	C		-55	125			*60.0	KD1							L 10				96
DIODE MATRIX,10X15	RAD	RM59	C		-55	125			*60.0	KD1							L 10				96
DIODE MATRIX,10X5	RAD	RM68	C		-55	125			*60.0	KD1							L 10				96
DIODE MATRIX,15X10	RAD	RM53	C		-55	125			*60.0	KD1							L 10				96
DIODE MATRIX,15X15	RAD	RM50	C		-55	125			*60.0	KD1							L 10				96
DIODE MATRIX,15X5	RAD	RM56	C		-55	125			*60.0	KD1							L 10				96
DIODE MATRIX,2X4	FSC	FSA1400	A		-65	175			* 50	*D4							*L 4				11,66
DIODE MATRIX,2X4	FSC	FSA2001	A		-65	175			* 40	*D4							*L 25				11,66
DIODE MATRIX,2X8	FSC	FSA2000	A		-65	175			* 40	*D4							*L 25				11,66
DIODE MATRIX,2X8	MOTA	MC1118	F		-55	125			*40.0	KD3							L 90				13
DIODE MATRIX,5X10	RAD	RM71	C		-55	125			*60.0	KD1							L 10				96
DIODE MATRIX,5X15	RAD	RM62	C		-55	125			*60.0	KD1							L 10				96
DIODE MATRIX,5X5	RAD	RM74	C	DTL	-55	125			*60.0	KD1							L 10				42
DIODE MATRIX,5X8	RAD	RM10	C		-55	125			*60.0	KD1							L 7				38
DIODE MATRIX,5X8	RAD	RM12	C		-55	125			*60.0	KD1							L 11				38
DIODE MATRIX,6X8	RAD	RM30	C		-55	125			*60.0	KD1							L 7				38
DIODE MATRIX,6X8	RAD	RM31	C		-55	125			*60.0	KD1							L 11				38
DRIVER	FSC	SH2100		RTL	-55	125			3.0	65			*200	.56	.82		* 75		.30		1
DRIVER	GI	NCPC12	H	DTL	-55	125		12.0	4.2	200			20				55	12	.30	5.00	0,90
DRIVER	INTX	GBXXXXX	L		-55	125			*12.0				* 20					* 5			78
DRIVER	SPRG	US-0107	F	RCTL	-55	125			3.0	5			* 20	.40	1.15	.050	200		.35	2.50	57
DRIVER	TI	SN517	F	RCTL	-55	125			3.0	5			* 20	.40	1.15	.050	200		.35	2.50	74
DRIVER	VARO	8213	E	DTL	-55	125	6.0	3.0	-3.0				10	.50	3.00		15		.50	3.50	72
DRIVER,DUAL 2 INPUT	FSC	CTL956	A	RTL	15	55		4.5	-2.0	150			25	.92	1.20	1.200	15		-.60	2.40	73
DRIVER,QUAD	GI	MEM4000	K																		18,82
DRIVER,2 INPUT	WMED	WS151	A	DTL	0	125			10.0	150							175		1		53

CIRCUIT DESCRIPTION	MFR	MFRS PART NUMBER	TECH	TYPE OF LOGIC	OPER. TEMP. CENTGRDE MIN	MAX	SUPPLY VOLTAGE VDC NO. 3	NO. 2	NO. 1	SUPPLY POWER MILLIWATTS AVE	ON	OFF	FAN-OUT	INPUT THRESHOLD VOLTS ZERO	ONE	NOISE IMMUNITY VOLTS	DELAY NANO-SECS	OPERATING SPEED MCPS	OUTPUT LEVEL VOLTS ZERO	ONE	PACKAGE TYPE
EXCLUSIVE OR	AMEL	H-INDUS	F	RTL	0	70			3.0	42			10	.55	.85		* 32		.30		5,6
EXCLUSIVE OR	AMEL	H-PREM	F	RTL	-55	125			3.0	42			10	.55	.80		* 28		.25		5,54
EXCLUSIVE OR	AMEL	H-STAND	F	RTL	-55	125			3.0	42			10	.56	.82		* 30		.30		5,54
EXCLUSIVE OR	FSC	L904	A	RTL	-55	125			3.0	45			5,4	.55	.80	.250	* 22		.30	1.45	1,6
EXCLUSIVE OR	FSC	L904C	A	RTL	0	100			3.0	45			5,4	.55	.80	.250	* 22		.30	1.45	1,6
EXCLUSIVE OR	FSC	MWL912	A	RTL	-55	125			3.0	8			4,3	.45	.75	.150	75		.30	.90	1,55
EXCLUSIVE OR	MOTA	MC303	A	ECL	-55	125		-1.15	-5.2	35			25	1.35	1.00	.200	6		1.55	.75	10,50
EXCLUSIVE OR	MOTA	MC353	A	ECL	0	75		-1.15	-5.2	60			25	1.35	1.00	.200	6		1.55	.75	10,50
EXCLUSIVE OR	MOTA	MC804	F	RTL	0	100			3.0	45			5,4	.55	.84		* 36		.40	.84	4
EXCLUSIVE OR	MOTA	MC904	F	RTL	-55	125			3.0	45			5,4	.56	.82	.020	* 36		.30	.84	4
EXCLUSIVE OR	NSC	NB1004	A	RTL	-55	125			3.0	#45			13	.69	.77		16		.15		2
EXCLUSIVE OR	NSC	NB2004	A	RTL	0	100			3.0	#45			13	.69	.77		16		.15		2
EXCLUSIVE OR	PHIL	PL904	A	RTL	-55	125			3.0	45			5,4	.56	.82		* 22		.30		1
EXCLUSIVE OR	PHIL	PL912	A	RTL	-55	125			3.0	8			4,3	.45	.75	.050	* 120		.30	.80	1
EXCLUSIVE OR	PHIL	PL981	A	RTL	-55	125			4.0	8			5,4	.45	.82		27		.40		11,51
EXCLUSIVE OR	SIGN	SE840	A	TTL	-55	125			5.0		19	10	10				13		.20	2.4	81
EXCLUSIVE OR	SPRG	US-0105	F	RCTL	-55	125			3.0	3			5	.46	1.16				.46	1.16	57
EXCLUSIVE OR	SPRG	US-0712	F	RTL	-55	125			3.0	8							* 120				57,62
EXCLUSIVE OR	SW	SW303	A	ECL	-55	125		-1.15	-5.2	35			* 25	1.35	1.0	.20	6		1.55	.75	10,50
EXCLUSIVE OR	TI	SN515	F	RCTL	-55	125			3.0	3			5,4	.46	1.16		250		.46	1.16	58
EXCLUSIVE OR	TI	SN5191	F	RCTL	-55	125			3.0	6			5								58
EXCLUSIVE OR	TI	SN734	A	RTL	-55	125			3.0	8			4				70				
EXCLUSIVE OR WC	GME	134H	A	RTL	-55	125			3.0	*10			4	.55	.75	.050	* 100		.50	.83	3,70
EXCLUSIVE OR WC	MOTA	MC912	A	RTL	-55	125			3.0	8				.45	.75	.050	90		.30	.80	1
EXCLUSIVE OR WC	NSC	NC1012	A	RTL	-55	125			3.0	8			4,3	.69	.77		16		.15		2
EXCLUSIVE OR WC	NSC	NC2012	A	RTL	0	100			3.0	8			4,3	.69	.77		16		.15		2
EXCLUSIVE OR WC	SW	SWG90	A	TTL	-55	125			5.0	14			15				14	20			27,49
EXCLUSIVE OR WC	SW	SWG91	A	TTL	-55	125			5.0	14			7				14	20			27,49
EXCLUSIVE OR WC	SW	SWG92	A	TTL	0	75			5.0	14			12				14	20			27,49
EXCLUSIVE OR WC	SW	SWG93	A	TTL	0	75			5.0	14			6				14	20			27,49
EXCLUSIVE OR WC	SYL	SG90	B	TTL	-55	125			5.0	35			15	1.20	1.70	.750	* 45		.45	3.20	40
EXCLUSIVE OR WC	SYL	SG91	B	TTL	-55	125			5.0	35			7	1.20	1.70	.750	* 49		.45	3.20	40
EXCLUSIVE OR WC	SYL	SG92	B	TTL	0	75			5.0	35			12	1.20	1.80	.730	* 46		.47	3.10	40
EXCLUSIVE OR WC	SYL	SG93	B	TTL	0	75			5.0	35			6	1.20	1.80	.730	* 47		.47	3.10	40
EXCLUSIVE OR WC	TRAN	TNG4611	B	TTL	-55	125			5.0				15	1.2	1.7	.700	* 18		.45	2.4	47
EXCLUSIVE OR WC	TRAN	TNG4612	B	TTL	0	75			5.0				15	1.2	1.7	.700	* 18		.45	2.4	47
EXCLUSIVE OR WC	TRAN	TNG4613	B	TTL	-55	125			5.0				7	1.2	1.7	.700	* 18		.45	2.4	47
EXCLUSIVE OR WC	TRAN	TNG4614	B	TTL	0	75			5.0				7	1.2	1.7	.700	* 18		.45	2.4	47
EXCLUSIVE OR,DUAL	TI	SN5370	F	DTL	-55	125			3.5	*24			10								58
EXCLUSIVE OR,DUAL	TI	SN7370	F	DTL	0	70			3.0		10	4	10	.40	1.70		65		.30	1.70	48,76
EXCLUSIVE OR,DUAL EX	TI	SN5450	A	TTL	-55	125			5.0	10			10								58
EXCLUSIVE OR,DUAL EX	TI	SN7450	F	TTL	0	70			5.0		18	10	* 10	.80	2.00	.400	13		.40	2.40	48,76
EXPANDER,AND-NOR2-2-3-3	SYL	SG150	A	TTL	-55	125			5.0	*30				1.20	1.70	.550		20	.65	4.80	40
EXPANDER,AND-NOR2-2-3-3	SYL	SG152	A	TTL	0	75			5.0	*35				1.80	1.20	1.150		20	.65	4.80	40
EXPANDER,AND-NOR2-2-3-3	SYL	SG230	B	TTL	-55	125			5.0	28				1.1	1.7		2		.45		40
EXPANDER,AND-NOR2-2-3-3	SYL	SG232	B	TTL	0	75			5.0	28				1.1	1.7		2		.45		40
EXPANDER,AND-NOR2-2-4-4	SW	SWG150	A	TTL	-55	125			5.0	20			15					20			49
EXPANDER,AND-NOR2-2-4-4	SW	SWG151	A	TTL	-55	125			5.0	20			7					20			49
EXPANDER,AND-NOR2-2-4-4	SW	SWG152	A	TTL	0	75			5.0	25			12					20			49

CIRCUIT DESCRIPTION	MFR	MFRS PART NUMBER	TECH	TYPE OF LOGIC	OPER. TEMP. CENTGRDE MIN	MAX	SUPPLY VOLTAGE VDC NO. 3	NO. 2	NO. 1	SUPPLY POWER MILLIWATTS AVE	ON	OFF	FAN-OUT	INPUT THRESHOLD VOLTS ZERO	ONE	NOISE IMMU-NITY VOLTS	DELAY NANO-SECS	OPER-ATING SPEED MCPS	OUTPUT LEVEL VOLTS ZERO	ONE	PACK-AGE TYPE
EXPANDER,AND-NOR2-2-4-4	SW	SWG153	A	TTL	0	75			5.0	20			6					20			49
EXPANDER,AND-NOR3-8 INP	TRAN	TNG7712	B	TTL	0	75			5.0	40				1.2	1.8		* 18		.40		47,75
EXPANDER,AND-OR 3-4-4	TRAN	TNG7812	B	TTL	0	75			5.0	40				1.2	1.8		* 18		.40		47,75
EXPANDER,DUAL 2 INP NOR	FSC	FL92129	A	RTL	15	55			3.6					.45	.75	.050	25		.30	.80	1
EXPANDER,DUAL 2 INP NOR	FSC	MWL921	A	RTL	-55	125			3.0					.45	.75	.050	25		.30	.80	1
EXPANDER,DUAL 2 INP NOR	GI	MEM5005	K																		82
EXPANDER,DUAL 2 INP NOR	GME	134E	A	RTL	-55	125			3.0						.75		40		.50	.83	3
EXPANDER,DUAL 2 INP NOR	MOTA	MC921	A	RTL	-55	125			3.0					.45	.75	.050			.30	.80	4
EXPANDER,DUAL 2 INP NOR	NSC	NC1021	A	RTL	-55	125			3.0					.69	.77				.15		2
EXPANDER,DUAL 2 INP NOR	NSC	NC2021	A	RTL	0	100			3.0					.69	.77				.15		2
EXPANDER,DUAL 2 INP NOR	PHIL	PL921	A	RTL	-55	125			3.0					.45	.75	.050	40		.30	.80	1
EXPANDER,DUAL 2 INP NOR	PHIL	PL979	A	RTL	-55	125			4.0					.45	.82				.40		1,51
EXPANDER,DUAL 2 INP NOR	SPRG	US-0721	F	RTL	-55	125			3.0	15							* 120				57,62
EXPANDER,DUAL 2 INP NOR	TI	SN732	A	RTL	-55	125			3.0								35				1,58
EXPANDER,DUAL 3 INP NOR	AMEL	E-INDUS	F	RTL	0	70			3.0					.55	.85		16		.30		14
EXPANDER,DUAL 3 INP NOR	AMEL	E-PREM	F	RTL	-55	125			3.0					.55	.80		12		.25		14
EXPANDER,DUAL 3 INP NOR	AMEL	E-STAND	F	RTL	-55	125			3.0					.56	.82		12		.30		14
EXPANDER,DUAL 3 INP NOR	SIGN	LU300	A		10	55											5				12
EXPANDER,DUAL 3 INP NOR	SIGN	SU300	A		-20	85			* 5.5	K10							4				12,52
EXPANDER,DUAL 4 INP AND	SW	SWG180	A	TTL	-55	125			5.0	1								20			49
EXPANDER,DUAL 4 INP AND	SW	SWG181	A	TTL	-55	125			5.0	1								20			49
EXPANDER,DUAL 4 INP AND	SW	SWG182	A	TTL	0	75			5.0	1								20			49
EXPANDER,DUAL 4 INP AND	SW	SWG183	A	TTL	0	75			5.0	1								20			49
EXPANDER,DUAL 4 INP AND	SYL	SG180	A	TTL	-55	125			5.0					.60	1.70	.350	* 3		.25	3.70	40
EXPANDER,DUAL 4 INP AND	SYL	SG181	A	TTL	-55	125			5.0					.60	1.70	.350	* 3		.25	3.70	40
EXPANDER,DUAL 4 INP AND	SYL	SG182	A	TTL	0	75			5.0					.60	1.70	.350	* 3		.25	3.70	40
EXPANDER,DUAL 4 INP AND	SYL	SG183	A	TTL	0	75			5.0					.60	1.70	.350	* 3		.25	3.70	40
EXPANDER,DUAL 4 INP AND	TRAN	TNG3511	B	TTL	-55	125			5.0		*30	*15		1.2	1.7		* 18				47
EXPANDER,DUAL 4 INP AND	TRAN	TNG3512	B	TTL	0	75			5.0		*30	*15		1.2	1.7		* 18				47
EXPANDER,DUAL2-3AND-NOR	TRAN	TNG7912	B	TTL	0	75			5.0	40				1.2	1.8		* 18		.40		47,75
EXPANDER,DUAL4 INP NAND	SIGN	SE806	A	TTL	-55	125			5.0								13		.20		81
EXPANDER,DUAL4 INP NAND	SW	SWG170	A	TTL	-55	125			5.0	5								20			49
EXPANDER,DUAL4 INP NAND	SW	SWG171	A	TTL	-55	125			5.0	5								20			49
EXPANDER,DUAL4 INP NAND	SW	SWG172	A	TTL	0	75			5.0	5								20			49
EXPANDER,DUAL4 INP NAND	SW	SWG173	A	TTL	0	75			5.0	5								20			49
EXPANDER,DUAL4 INP NAND	SYL	SG170	A	TTL	-55	125			5.0	*14				1.20	1.70	.550		20	.65	4.80	40
EXPANDER,DUAL4 INP NAND	SYL	SG172	A	TTL	0	75			5.0	*17				1.20	1.80	.550		20	.65	4.80	40
EXPANDER,DUAL4 INP NAND	SYL	SG270	B	TTL	-55	125			5.0	7				1.1	1.7		2		.45		40
EXPANDER,DUAL4 INP NAND	SYL	SG272	B	TTL	0	75			5.0	7				1.1	1.7		2		.45		40
EXPANDER,DUAL4 INP NAND	TI	SN5460	A	TTL	-55	125			5.0	5				.80	2.00		15		.40		48
EXPANDER,DUAL4 INP NAND	TI	SN7460	F	TTL	0	70			5.0		3	5	* 10	.80	2.00		10		.40		48,76
EXPANDER,DUAL4 INP NAND	TRAN	TNG4011	B	TTL	-55	125			5.0		*30	*15		1.2	1.7		* 18				47
EXPANDER,DUAL4 INP NAND	TRAN	TNG4012	B	TTL	0	75			5.0		*30	*15		1.2	1.7		* 18				47
EXPANDER,1-2 INPUT NOR	GI	MEM5006	K																		18
EXPANDER,1-4 INPUT NOR	GI	MEM5002	K																		82
EXPANDER,4 INPUT AND	TRAN	TNG4031	B	TTL	15	55			5.0		*30	*15	7	1.0	2.0	.500	* 25		.50	2.5	1
EXPANDER,4 INPUT NOR	GI	MEM5003	K																		18
EXPANDER,5 INPUT AND	TI	SN7320	F	DTL	0	70			3.0											2.10	57,76
EXPANDER,5 INPUT NOR	GI	MEM2001	K																		82

CIRCUIT DESCRIPTION	MFR	MFRS PART NUMBER	TECH	TYPE OF LOGIC	OPER. TEMP. CENTGRDE MIN	OPER. TEMP. CENTGRDE MAX	SUPPLY VOLTAGE VDC NO. 3	SUPPLY VOLTAGE VDC NO. 2	SUPPLY VOLTAGE VDC NO. 1	SUPPLY POWER MILLIWATTS AVE	SUPPLY POWER MILLIWATTS ON	SUPPLY POWER MILLIWATTS OFF	FAN-OUT	INPUT THRESHOLD VOLTS ZERO	INPUT THRESHOLD VOLTS ONE	NOISE IMMU-NITY VOLTS	DELAY NANO-SECS	OPER-ATING SPEED MCPS	OUTPUT LEVEL VOLTS ZERO	OUTPUT LEVEL VOLTS ONE	PACK-AGE TYPE
EXPANDER,5 INPUT NOR	MOTA	MC305	A	ECL	-55	125			*10.0					1.55	.75		6				13,50
EXPANDER,5 INPUT NOR	MOTA	MC355	A	ECL	0	75			*10.0					1.55	.75		6				13,50
EXPANDER,5 INPUT NOR	SW	SW305	A	ECL	-55	125			*10.0					1.55	.75		6				13,50
EXPANDER,6 INPUT NOR	GI	MEM5001	K																		82
HALF ADDER	FSC	MWL908	A	RTL	-55	125			3.0	10			4,3	.50	.85	.050	75		.10	.90	1
HALF ADDER	GME	134A	A	RTL	-55	125			3.0	10			4		.75		105		.50	.83	3,70
HALF ADDER	MOTA	MC908	A	RTL	-55	125			3.0	10			4,3	.45	.80		90		.30		1
HALF ADDER	NSC	NC1008	A	RTL	-55	125			3.0	10			4,3	.69	.77		75		.15		
HALF ADDER	NSC	NC2008	A	RTL	0	100			3.0	10			4,3	.69	.77		75		.15		
HALF ADDER	PHIL	PL908	A	RTL	-55	125			3.0	10			4,3	.50	.85	.050	75		.10	.90	1
HALF ADDER	PHIL	PL9605	A	RTL	-55	125			3.0				4,3	.49	.82	.06	18		.35	.88	
HALF ADDER	PHIL	PL975	A	RTL	-55	125			4.0	10			5,4	.45	.82		30		.40		1
HALF ADDER	SPRG	US-0708	F	RTL	-55	125			3.0	10							* 120				57,62
HALF ADDER	TI	SN729	A	RTL	-55	125			3.0	10			4				105				1,74
INVERTER	AMEL	B-INDUS	F	DCTL	0	70			3.0		54	16	31	.55	.85		18		.30		5,6
INVERTER	AMEL	B-PREM	F	DCTL	-55	125			3.0		54	16	66	.55	.80		15		.25		5,6
INVERTER	AMEL	B-STAND	F	DCTL	-55	125			3.0		54	16	29	.65	.82		18		.30		5,6
INVERTER	AMEL	B11-501	F	RTL	-55	125			3.0		100	16	*167	.55	.80		* 20		.25		5,63
INVERTER	AMEL	B11-504	F	RTL	0	70			3.0		100	16	*114	.55	.85		* 36		.30		5
INVERTER	AMEL	B11-508	F	RTL	-55	125			3.0		100	16	*115	.56	.82		* 30		.30		5,63
INVERTER	FSC	FL90029	A	RTL	15	55			3.6	30			80				15				1
INVERTER	FSC	L900	A	RTL	-55	125			3.0		45	16	25	.56	.82		16		.30		1
INVERTER	FSC	L900C	A	RTL	0	100			3.0		45	16	25	.55	.84		16		.40		1
INVERTER	MOTA	MC800	F	RTL	0	100			3.0		45	16	25,5	.55	.84		* 30		.40	.84	4
INVERTER	MOTA	MC900	F	RTL	-55	125			3.0		45	16	25,5	.56	.82	.020	* 30		.30	.84	4
INVERTER	NORD	NM4002	F	RTL	-55	125			13.0	590							25				
INVERTER	NSC	NB1000	A	RTL	-55	125			3.0	16			80	.69	.77		15		.15		2
INVERTER	NSC	NB2000	A	RTL	0	100			3.0	16			80	.69	.77		15		.15		2
INVERTER	PHIL	PL900	A	RTL	-55	125			3.0		45	16	25	.56	.82		16		.30		1
INVERTER	SPER	900	A	RTL	-55	125			3.0		16	45	* 25	.56	.82		* 30		.30		1,64
INVERTER	SPRG	US-0106	F	RCTL	-55	125			3.0		2		25								57,62
INVERTER	TI	SN516	F	RCTL	-55	125			3.0		2		25	.46	1.16		175		.46	1.16	58
INVERTER,DUAL	MOTA	MC1115	F	DTL	-55	125		*10.0	7.0	250							* 32				13
INVERTER,DUAL	SPRG	US-0114	F	RCTL	-55	125			3.0	2			* 5								57,62
INVERTER,DUAL	SPRG	US-0115	F	RCTL	-55	125			3.0	4			* 25								57,62
INVERTER,QUAD	AMEL	I-INDUS	F	RTL	0	70			3.0		52	20	5	.55	.85		16		. 30		14
INVERTER,QUAD	AMEL	I-PREM	F	RTL	-55	125			3.0		52	20	10	.55	.80		12		.25		14
INVERTER,QUAD	AMEL	I-STAND	F	RTL	-55	125			3.0		52	20	6	.56	.82		12		.30		14
INVERTER,QUAD	FSC	FL92729	A	RTL	15	55			3.6	80			16				12				11
INVERTER,QUAD	FSC	L927	A	RTL	-55	125			3.0	48			5				12				11
INVERTER,QUAD	FSC	L927C	A	RTL	0	100			3.0	48			5				12				11
INVERTER,QUAD	GME	263Q	A	DTL	-55	125			4.0		*20	* 9	* 8	.80	2.00	.400	20		.40	3.50	17,59
INVERTER,QUAD	SIGN	SE181	A	DTL	-55	125			4.0	*19			* 5	.40	1.95	.700	* 32		1.10	3.90	12
INVERTER,QUAD	TI	SN535	F	RTL	-55	125			3.5	15			* 10	.30	1.50		20		.30	2.20	74
INVERTER,QUAD	TI	SN7350	F	RCTL	0	70			3.0		10		10	.40	1.70		25		.30	1.70	58,76
INVERTER,SEXTUPLE	CORN	0094	D		-55	70			10.0	*40			6	.87	2.17	.550	35		.32	2.72	71
INVERTER,SEXTUPLE	PHIL	PL9608	A	DTL	-55	125			5.0	*13			8	1.10	2.0	.600	20		.4	2.60	41
INVERTER,SEXTUPLE	WMED	WC286	A	DTL	0	75			6.0	8			6	1.0	1.8		30		.45		43
INVERTER,SEXTUPLE	WMED	WC296	A	DTL	0	75			6.0	8			6	1.0	1.8		30		.45		43

CIRCUIT DESCRIPTION	MFR	MFRS PART NUMBER	TECH	TYPE OF LOGIC	OPER. TEMP. CENTGRDE MIN	MAX	SUPPLY VOLTAGE VDC NO. 3	NO. 2	NO. 1	SUPPLY POWER MILLIWATTS AVE	ON	OFF	FAN-OUT	INPUT THRESHOLD VOLTS ZERO	ONE	NOISE IMMUNITY VOLTS	DELAY NANO-SECS	OPER-ATING SPEED MCPS	OUTPUT LEVEL VOLTS ZERO	ONE	PACK-AGE TYPE
INVERTER,SEXTUPLE	WMED	WM286	A	DTL	-55	125			6.0	5			6	1.00	2.00	.55	23		.45		43
INVERTER,SEXTUPLE	WMED	WM296	A	DTL	-55	125			6.0	11			9	1.00	2.00	.55	32		.45	5.8	43
INVERTER,TRIPLE	PHIL	PL9611	A	RTL	-55	125			3.0								27				
INVERTER,TRIPLE	TI	SN344	A		0	65		6.0	-3.0	85			12				120		.70		48
J-K,CLCKD OR SET DIRECT	GME	264JK	A	DTL	-55	125			5.0	45			10	1.10	2.00	.600	25	21	.40	2.60	17,45
J-K,CLCKD OR SET DIRECT	MOTA	MC816	F	RTL	0	100			3.0	54			3	.55	.84		60	* 8	.40	.84	4
J-K,CLCKD OR SET DIRECT	MOTA	MC831G	A	DTL	0	75			5.0		*90		7	1.10	1.90		* 75		.45		11
J-K,CLCKD OR SET DIRECT	MOTA	MC845G	A	DTL	0	75			5.0		*90		12	1.10	1.90		* 75		.45		11
J-K,CLCKD OR SET DIRECT	MOTA	MC848G	A	DTL	0	75			5.0				11	1.10	1.90		* 65		.45		11
J-K,CLCKD OR SET DIRECT	MOTA	MC916	F	RTL	-55	125			3.0	54			3	.56	.82	.020	60	* 8	.30	.84	4
J-K,CLCKD OR SET DIRECT	MOTA	MC931G	A	DTL	-55	125			5.0		*70		7	1.10	2.00		* 75		.40		11
J-K,CLCKD OR SET DIRECT	MOTA	MC945G	A	DTL	-55	125			5.0		*70		10	1.10	2.00		* 75		.40		11
J-K,CLCKD OR SET DIRECT	MOTA	MC948G	A	DTL	-55	125			5.0		*95		9	1.10	2.00		* 65		.40		11
J-K,CLCKD OR SET DIRECT	PHIL	PL940	A	RTL	-55	125			3.0	15			2	.45	.75	.050	* 100		.30	.80	1,51
J-K,CLCKD OR SET DIRECT	PHIL	PL9923	A	RTL	15	55			3.6				10					1			
J-K,CLCKD OR SET DIRECT	PHIL	PL9940	A	RTL	-55	125			3.0	15			2					6			
J-K,CLCKD OR SET DIRECT	PHIL	PL9974	A	RTL	-55	125			3.0	54			5	.56	.82	.02		20	.21	.84	
J-K,CLCKD OR SET DIRECT	SYL	SF260	B	TTL	-55	125			5.0	55			11	1.1	1.7	.75		30	.45	3.00	40
J-K,CLCKD OR SET DIRECT	SYL	SF261	B	TTL	-55	125			5.0	55			6	1.1	1.7	.75		30	.45	3.00	40
J-K,CLCKD OR SET DIRECT	SYL	SF262	B	TTL	0	75			5.0	55			9	1.1	1.7	.75		30	.45	3.00	40
J-K,CLCKD OR SET DIRECT	SYL	SF263	B	TTL	0	75			5.0	55			5	1.1	1.7	.75		30	.45	3.00	40
J-K,CLCKD OR SET DIRECT	SYL	SF60	B	TTL	-55	125			5.0	50			15	1.2	1.7	.75		20	.45	3.00	40
J-K,CLCKD OR SET DIRECT	SYL	SF61	B	TTL	-55	125			5.0	50			7	1.2	1.7	.75		20	.45	3.00	40
J-K,CLCKD OR SET DIRECT	SYL	SF62	B	TTL	0	75			5.0	50			12	1.2	1.7	.75		20	.45	3.00	40
J-K,CLCKD OR SET DIRECT	SYL	SF63	B	TTL	0	75			5.0	50			6	1.2	1.7	.75		20	.45	3.00	40
J-K,CLCKD OR SET DIRECT	TI	SN530	F	DTL	-55	125			3.5	37			* 10	.30	1.50		45		.30	2.00	74
J-K,CLCKD OR SET DIRECT	TI	SN7300	F	RCTL	0	70			3.0	27			10	.40	1.70		20		.30	1.70	58,76
J-K,CLCKD OR SET DIRECT	TRAN	TFF3131	B	TTL	15	55			5.0		*30	*15	7	1.0	2.0	.500	* 25		.50	2.5	1
J-K,CLOCKED OR DIRECT	AMEL	R12-001	F	DTL	-55	125			4.0	* 5			4	.30	1.70		160	* 4	.30	3.50	14,63
J-K,CLOCKED OR DIRECT	AMEL	R12-002	F	DTL	-55	125			4.0	10			# 3	.30	1.70		230		.30	3.00	24
J-K,CLOCKED OR DIRECT	FSC	DTL931	A	DTL	-55	125			4.0	20			7	1.03	1.33		50		.23		44
J-K,CLOCKED OR DIRECT	FSC	DTL945	A	DTL	-55	125			4.0	42			9				50				44
J-K,CLOCKED OR DIRECT	FSC	DTL948	A	DTL	-55	125			5.0	48			8				40				44
J-K,CLOCKED OR DIRECT	FSC	FL92328	A	RTL	15	55			3.6	54			8				40				1
J-K,CLOCKED OR DIRECT	FSC	FL92329	A	RTL	15	55			3.6	54			10				40				1
J-K,CLOCKED OR DIRECT	FSC	FL92629	A	RTL	15	55			3.6	55			16				40				11
J-K,CLOCKED OR DIRECT	FSC	FL93129	A	DTL	0	70			4.0	20			7	1.03	1.33		50		.23		11,44
J-K,CLOCKED OR DIRECT	FSC	FL94529	A	DTL	0	70			4.0	42			9				50				11,44
J-K,CLOCKED OR DIRECT	FSC	FL94829	A	DTL	0	70			5.0	48			8				40				
J-K,CLOCKED OR DIRECT	FSC	LPDT9040	A	DTL	-55	125			5.0	E35			10	.9	1.7	.7		2.5	.2	2.7	44,75
J-K,CLOCKED OR DIRECT	FSC	L926	A	RTL	-55	125			3.0	56			5	.56	.82		40	20	.30		11,55
J-K,CLOCKED OR DIRECT	FSC	L926C	A	RTL	0	100			3.0	56			5	.55	.84		40	20	.40		11,55
J-K,CLOCKED OR DIRECT	MOTA	MC308	A	ECL	-55	125			-5.2	52							12	30	1.56	.82	13,50
J-K,CLOCKED OR DIRECT	MOTA	MC358	A	ECL	0	75			-5.2	52							10	30	1.55	.75	13,50
J-K,CLOCKED OR DIRECT	MOTA	MC831F	A	DTL	0	75			5.0		*90		7	1.10	1.90		* 75		.45		39
J-K,CLOCKED OR DIRECT	MOTA	MC845F	A	DTL	0	75			5.0		*90		12	1.10	1.90		* 75		.45		39
J-K,CLOCKED OR DIRECT	MOTA	MC848F	A	DTL	0	75			5.0				11	1.10	1.90		* 65		.45		39
J-K,CLOCKED OR DIRECT	MOTA	MC931F	A	DTL	-55	125			5.0		*70		7	1.10	2.00		* 75		.40		39
J-K,CLOCKED OR DIRECT	MOTA	MC945F	A	DTL	-55	125			5.0		*70		10	1.10	2.00		* 75		.40		39

CIRCUIT DESCRIPTION	MFR	MFRS PART NUMBER	TECH	TYPE OF LOGIC	OPER. TEMP. CENTGRDE		SUPPLY VOLTAGE VDC			SUPPLY POWER MILLIWATTS			FAN-OUT	INPUT THRESHOLD VOLTS		NOISE IMMU-NITY VOLTS	DELAY NANO-SECS	OPER-ATING SPEED MCPS	OUTPUT LEVEL VOLTS		PACK-AGE TYPE
					MIN	MAX	NO. 3	NO. 2	NO. 1	AVE	ON	OFF		ZERO	ONE				ZERO	ONE	
J-K,CLOCKED OR DIRECT	MOTA	MC948F	A	DTL	-55	125			5.0		*95		9	1.10	2.00		* 65		.40		39
J-K,CLOCKED OR DIRECT	PHIL	PL916	A	RTL	-55	125			3.0	54			3	.56	.82		35		.30		1
J-K,CLOCKED OR DIRECT	PHIL	PL931	A	DTL	-55	125			5.0				7	1.00	1.30	.600	80	10	.40	2.60	41
J-K,CLOCKED OR DIRECT	PHIL	PL945	A	DTL	-55	125			4.0	42			9				50				41
J-K,CLOCKED OR DIRECT	PHIL	PL948	A	DTL	-55	125			5.0	48			8				40				41
J-K,CLOCKED OR DIRECT	PHIL	PL9600	A	RTL	-55	125			3.0				4	.49	.82	.06		30	.35	.88	
J-K,CLOCKED OR DIRECT	PHIL	PL9926	A	RTL	-55	125			3.0	56			5	.56	.82	.02		20	.21	.84	
J-K,CLOCKED OR DIRECT	SIGN	LU320	A		-55	125			4.5	90			* 17	.80	2.70	.200	65		.60	3.30	12
J-K,CLOCKED OR DIRECT	SIGN	SE125	A	DTL	-55	125		4.0	-2.0	20			7	1.22	1.48	1.0		20	.22	3.8	81
J-K,CLOCKED OR DIRECT	SIGN	SE825	A	TTL	-55	125			5.0	70							30		.20	2.4	81
J-K,CLOCKED OR DIRECT	SIGN	SU320	A	TTL	-55	125			4.5	90			* 17	.80	2.70	.200	76		.60	3.30	12,52
J-K,CLOCKED OR DIRECT	SPER	926	A	RTL	-55	125			3.0	56			5	.56	.82		35	20	.30		1,64
J-K,CLOCKED OR DIRECT	SW	SWF50	A	TTL	-55	125			5.0	50			15					20			49
J-K,CLOCKED OR DIRECT	SW	SWF51	A	TTL	-55	125			5.0	50			7					20			49
J-K,CLOCKED OR DIRECT	SW	SWF52	A	TTL	0	75			5.0	50			12					20			49
J-K,CLOCKED OR DIRECT	SW	SWF53	A	TTL	0	75			5.0	50			6					20			49
J-K,CLOCKED OR DIRECT	SW	SW308	A	ECL	-55	125			-5.2	52							10	30	1.56	.82	13,50
J-K,CLOCKED OR DIRECT	SW	SW931	A	DTL	-55	125			5.0	35			9	.95	2.0	.55		8	.40	2.6	10,49
J-K,CLOCKED OR DIRECT	SW	SW945	A	DTL	-55	125			5.0	45			# 10	.95	2.0	.55			.40	2.6	10,49
J-K,CLOCKED OR DIRECT	SW	SW948	A	DTL	-55	125			5.0	45			# 10	.95	2.0	.550			.40	2.60	10,49
J-K,CLOCKED OR DIRECT	SYL	SF250	B	TTL	-55	125			5.0	55			11	1.1	1.7	.75		30	.45	3.00	40
J-K,CLOCKED OR DIRECT	SYL	SF251	B	TTL	-55	125			5.0	55			6	1.1	1.7	.75		30	.45	3.00	40
J-K,CLOCKED OR DIRECT	SYL	SF252	B	TTL	0	75			5.0	55			9	1.1	1.7	.75		30	.45	3.00	40
J-K,CLOCKED OR DIRECT	SYL	SF253	B	TTL	0	75			5.0	55			5	1.1	1.7	.75		30	.45	3.00	40
J-K,CLOCKED OR DIRECT	SYL	SF50	A	TTL	-55	125			5.0	50			15	1.20	1.70	.750	19	20	.45	3.20	40
J-K,CLOCKED OR DIRECT	SYL	SF51	A	TTL	-55	125			5.0	50			7	1.20	1.70	.750	19	20	.45	3.20	40
J-K,CLOCKED OR DIRECT	SYL	SF52	A	TTL	0	75			5.0	50			12	1.20	1.70	.800	19		.40	3.20	40
J-K,CLOCKED OR DIRECT	SYL	SF53	A	TTL	0	75			5.0	50			6	1.20	1.70	.800	19		.40	3.20	40
J-K,CLOCKED OR DIRECT	TI	SN5470	A	TTL	-55	125			5.0	70			10	.80	2.00	.400		25	.40	2.40	48
J-K,CLOCKED OR DIRECT	TI	SN7301	F	RCTL	0	70			3.0	27			10	.40	1.70		20		.30	1.70	48,76
J-K,CLOCKED OR DIRECT	TI	SN7470	F	TTL	0	70			5.0	70			* 10	.80	2.00	.400	30		.40	2.40	48,76
J-K,CLOCKED OR DIRECT	TRAN	TFF3111	B	TTL	0	75			5.0	75			15	1.2	1.7	.700		20	.45	2.4	47
J-K,CLOCKED OR DIRECT	TRAN	TFF3112	B	TTL	-55	125			5.0	75			15	1.2	1.7	.700		20	.45	2.4	47
J-K,CLOCKED OR DIRECT	TRAN	TFF3113	B	TTL	-55	125			4.0	75			7	1.2	1.7	.700		20	.45	2.4	47
J-K,CLOCKED OR DIRECT	TRAN	TFF3114	B	TTL	0	75			4.0	75			7	1.2	1.7	.700		20	.45	2.4	47
J-K,CLOCKED OR DIRECT	TRAN	TFF3115	B	TTL	-55	125			5.0		*30	*15	15	1.2	1.7	.700	* 18		.45	2.4	23,47
J-K,CLOCKED OR DIRECT	TRAN	TFF3116	B	TTL	0	75			5.0		*30	*15	15	1.2	1.7	.700	* 18		.45	2.4	23,47
J-K,CLOCKED OR DIRECT	TRAN	TFF3117	B	TTL	-55	125			5.0		*30	*15	7	1.2	1.7	.700	* 18		.45	2.4	23,47
J-K,CLOCKED OR DIRECT	TRAN	TFF3118	B	TTL	0	75			5.0		*30	*15	7	1.2	1.7	.700	* 18		.45	2.4	23,47
J-K,CLOCKED OR DIRECT	TRAN	TFF3121	B	TTL	-55	125			5.0		*30	*15	15	1.2	1.7	.700	* 18		.45	2.4	23,47
J-K,CLOCKED OR DIRECT	TRAN	TFF3122	B	TTL	0	75			5.0		*30	*15	15	1.2	1.7	.700	* 18		.45	2.4	23,47
J-K,CLOCKED OR DIRECT	TRAN	TFF3123	B	TTL	-55	125			5.0		*30	*15	7	1.2	1.7	.700	* 18		.45	2.4	23,47
J-K,CLOCKED OR DIRECT	TRAN	TFF3124	B	TTL	0	75			5.0		*30	*15	7	1.2	1.7	.700	* 18		.45	2.4	23,47
J-K,CLOCKED OR DIRECT	TRAN	TFF3125	B	TTL	-55	125			5.0		*30	*15	15	1.2	1.7	.700	* 18		.45	2.4	23,47
J-K,CLOCKED OR DIRECT	TRAN	TFF3126	B	TTL	0	75			5.0		*30	*15	15	1.2	1.7	.700	* 18		.45	2.4	23,47
J-K,CLOCKED OR DIRECT	TRAN	TFF3127	B	TTL	-55	125			5.0		*30	*15	7	1.2	1.7	.700	* 18		.45	2.4	23,47
J-K,CLOCKED OR DIRECT	TRAN	TFF3128	B	TTL	0	75			5.0		*30	*15	7	1.2	1.7	.700	* 18		.45	2.4	23,47
J-K,CLOCKED OR DIRECT	TRAN	TFF3211	B	TTL	-55	125			5.0		*30	*15	15	1.2	1.7	.700	* 18		.45	2.4	47
J-K,CLOCKED OR DIRECT	TRAN	TFF3212	B	TTL	0	75			5.0		*30	*15	15	1.2	1.7	.700	* 18		.45	2.4	47

CIRCUIT DESCRIPTION	MFR	MFRS PART NUMBER	TECH	TYPE OF LOGIC	OPER. TEMP. CENTGRDE MIN	OPER. TEMP. CENTGRDE MAX	SUPPLY VOLTAGE VDC NO. 3	SUPPLY VOLTAGE VDC NO. 2	SUPPLY VOLTAGE VDC NO. 1	SUPPLY POWER MILLIWATTS AVE	SUPPLY POWER MILLIWATTS ON	SUPPLY POWER MILLIWATTS OFF	FAN-OUT	INPUT THRESHOLD VOLTS ZERO	INPUT THRESHOLD VOLTS ONE	NOISE IMMUNITY VOLTS	DELAY NANO-SECS	OPERATING SPEED MCPS	OUTPUT LEVEL VOLTS ZERO	OUTPUT LEVEL VOLTS ONE	PACKAGE TYPE
J-K,CLOCKED OR DIRECT	TRAN	TFF3213	B	TTL	-55	125			5.0		*30	*15	7	1.2	1.7	.700	* 18		.45	2.4	47
J-K,CLOCKED OR DIRECT	TRAN	TFF3214	B	TTL	0	75			5.0		*30	*15	7	1.2	1.7	.700	* 18		.45	2.4	47
J-K,CLOCKED OR DIRECT	TRAN	TFF3251	B	TTL	-55	125			5.0		*30	*15	15	1.2	1.7	.700	* 18		.45	2.4	47
J-K,CLOCKED OR DIRECT	TRAN	TFF3252	B	TTL	0	75			5.0		*30	*15	15	1.2	1.7	.700	* 18		.45	2.4	47
J-K,CLOCKED OR DIRECT	TRAN	TFF3253	B	TTL	-55	125			5.0		*30	*15	7	1.2	1.7	.700	* 18		.45	2.4	47
J-K,CLOCKED OR DIRECT	TRAN	TFF3254	B	TTL	0	75			5.0		*30	*15	7	1.2	1.7	.700	* 18		.45	2.4	47
J-K,CLOCKED OR DIRECT	WMED	WM225	A	TTL	-55	125			6.0	*55			10	1.0	2.0	.55	60	* 14	.45	3.30	38
J-K,CLOCKED OR DIRECT	WMED	WM503	A	DTL	-55	125			4.5	47			10				20	20	.40		43
J-K,DUAL CLOCKED OR DIR	GME	PL4M01	K		-55	125		-12.0	-24.0	100				3.00	9.00	1.000	550	.500	2.00	10.0	88
J-K,DUAL CLOCKED OR DIR	TI	SN5302	F	DTL	-55	125			3.5	37			* 10	.30	1.50		45		.30	2.00	48
J-K,DUAL CLOCKED OR DIR	TI	SN5304	F	DTL	-55	125			3.5	37			* 10	.30	1.50		45		.30	2.00	48
J-K,DUAL CLOCKED OR DIR	TI	SN7302	F	RCTL	0	70			3.0	27			10	.40	1.70		20		.30	1.70	48,76
J-K,DUAL CLOCKED OR DIR	TI	SN7304	F	RCTL	0	70			3.0	27			10	.40	1.70		20		.30	1.70	48,76
J-K,SP CLOCKED OR DIR	RAY	RM215	A	DTL	-55	125			6.0	45			# 9	.60	1.10	.300	80	5	.30	3.50	21,53
J-K,SP CLOCKED OR DIR	RCA	CD2203	A	DTL	-55	125			4.0	8			* 5				167		.25	3.23	82
J-K,SP CLOCKED OR DIR	SILX	A03	A	DTL	-55	125			5.0	40			* 5	1.70	2.70	.700	50		1.00	4.60	20,46
J-K,SP CLOCKED OR DIR	SILX	A09	A	DTL	-55	125			5.0	54			* 5	1.70	2.70	.700	42	10	1.00	4.60	20,46
J-K,SP CLOCKED OR DIR	WMED	WC215	A	DTL	0	75			6.0	45			7	1.0	1.8		30	4	.45		43
J-K,SP CLOCKED OR DIR	WMED	WM215	A	DTL	-55	125			6.0	45			9	.70	1.80	.400	80	5	.30	3.50	21,53
LEVEL TRANSLATOR	TI	SN343	F	DTL	0	65	24.0	6.0	-3.0	*30				.	2.50		500		.70	5.70	48
LEVEL TRANSLATOR	WMED	WC208	A	DTL	0	75			6.0	8			6	1.0	1.8		30		.45		9,43
LEVEL TRANSLATOR	WMED	WM208	A		-55	125			6.0	14								1	.30	2.50	9
LEVEL TRANSLATOR	WMED	WS150	A	DTL	-55	125		10.0	-6.4	100									-6.3	6.30	53
LEVEL TRANSLATOR	WMED	WS815	A	DTL	0	70		20.0	4.0	*60				1.50	5.50	1.050			.45	2.00	53
LEVEL TRANSLATOR,DUAL	TI	SN346	F		0	65	12.0	6.0	-12.0	160			11				850		1.80	.95	48
MULTIVIBRATOR,FREE-RUN	INTX	MVXXXXX	L	TRL	-55	125			12.0	107			3,3					* 1			78
MULTIVIBRATOR,MONO	AMEL	011-001	J	RTL	-55	125			3.0	20			10	.55	.80				.25		5
MULTIVIBRATOR,MONO	AMEL	011-004	J	RTL	0	70			3.0	20			5	.55	.85				.30		5
MULTIVIBRATOR,MONO	AMEL	011-008	J	RTL	-55	125			3.0	20			6	.56	.82				.30		5
MULTIVIBRATOR,MONO	AMEL	012-001	F	DTL	-55	125			4.0	* 5			# 4	.30	.30	1.700	250		2.00	3.50	14
MULTIVIBRATOR,MONO	AMEL	042-001	F	DTL	-55	125			4.0	* 5			# 4	.30	.30	1.700	250		2.00	3.50	63
MULTIVIBRATOR,MONO	FSC	DTL951	A	DTL	-55	125			5.0	35			10				25				
MULTIVIBRATOR,MONO	FSC	FL95129	A	DTL	0	70			5.0	35			10				25				
MULTIVIBRATOR,MONO	FSC	SE160	A	DTL	-55	125			4.0	*32							19				11,55
MULTIVIBRATOR,MONO	GESP	12X248	A		-55	125			6.0	*D3										5.50	2
MULTIVIBRATOR,MONO	GI	NCPC16	H	DTL	-55	125		12.0	4.2	*D2			* 8		3.00		25	10	.30	5.00	0,90
MULTIVIBRATOR,MONO	GI	PC18	H	DTL	-55	125		12.0	4.2	*D2			* 8		3.00		25	10	.30	5.00	0,90
MULTIVIBRATOR,MONO	INTX	DMXXXXX	L	TRL	-55	125			9.0	180			* 6								78
MULTIVIBRATOR,MONO	MEPC	640704	M	DTL	-55	125		6.0	-3.0				5				10	5			60
MULTIVIBRATOR,MONO	SIGN	SE160	A	DTL	-55	125		4.0	-2.0	*32			4				45		.40	3.90	12,52
MULTIVIBRATOR,MONO	SIGN	SE161	A	DTL	-55	125			4.0	*40			5				45		.40	3.90	12,52
MULTIVIBRATOR,MONO	SILX	A08	A	DTL	-55	125			5.0	42			* 5	1.70	2.70		40	4	1.00		20,80
MULTIVIBRATOR,MONO	SPRG	US-0108	F		-55	125			3.0	4			* 5								57
MULTIVIBRATOR,MONO	TI	SN1005	F	DTL	-55	125			3.0	30			* 10	.30	1.70		* 75		.30	1.70	58
MULTIVIBRATOR,MONO	TI	SN518	F	RCTL	-55	125			3.0	2			5	.22	1.15		800		.22	1.15	58
MULTIVIBRATOR,MONO	TI	SN5380	F	RCTL	-55	125			3.0	14			* 10	.30	1.70		90		.30	1.70	58
MULTIVIBRATOR,MONO	TI	SN7380	F	RCTL	0	70			3.0		10	4	10	.40	1.70		90		.30	1.70	48,76
MULTIVIBRATOR,MONO	VARO	8203	E	DTL	-55	125		6.0	3.0	165			4		3.00		* 30	* 10	.50	3.50	72
MULTIVIBRATOR,MONO	WMED	WS840	A	DTL	-55	125							* 6								53

CIRCUIT DESCRIPTION	MFR	MFRS PART NUMBER	TECH	TYPE OF LOGIC	OPER. TEMP. CENTGRDE MIN	OPER. TEMP. CENTGRDE MAX	SUPPLY VOLTAGE VDC NO. 3	SUPPLY VOLTAGE VDC NO. 2	SUPPLY VOLTAGE VDC NO. 1	SUPPLY POWER MILLIWATTS AVE	SUPPLY POWER MILLIWATTS ON	SUPPLY POWER MILLIWATTS OFF	FAN-OUT	INPUT THRESHOLD VOLTS ZERO	INPUT THRESHOLD VOLTS ONE	NOISE IMMUNITY VOLTS	DELAY NANO-SECS	OPERATING SPEED MCPS	OUTPUT LEVEL VOLTS ZERO	OUTPUT LEVEL VOLTS ONE	PACKAGE TYPE
NAND-OR,2-2-2 INPUT	GI	MEM901	K					-12.0	-24.0	20				8.0	3.0	2.0	250		10.0	.20	18,82
NAND/AND/NOR,5 INPUT EX	TI	SN531	F	DTL	-55	125			3.5	18			* 10	.30	1.70		25		.30	2.20	74
NAND,DUAL 2 INPUT	FSC	SE115	A	DTL	-55	125			4.0	14				1.10	1.70	.650	15		.45	3.50	11,55
NAND,DUAL 2 INPUT	GME	264D2	A	DTL	-55	125		4.0	-2.0	6			5				30		.40		17,59
NAND,DUAL 2 INPUT	MOTA	MC206	A	DTL	-55	125		4.0	-2.0		*17	*12	5				30				13,50
NAND,DUAL 2 INPUT	MOTA	MC256	A	DTL	0	70		4.0	-2.0		*12	*20	5				30				13
NAND,DUAL 2 INPUT	SIGN	SE115	A	DTL	-55	125		4.0	-2.0		*12	*17	5	1.22	1.48	1.000	30		.22	3.80	12,56
NAND,DUAL 2 INPUT	TRAN	TNG3131	B	TTL	15	55			5.0		*30	*15	7	1.0	2.0	.500	* 25		.50	2.5	1
NAND,DUAL 2 INPUT	TRAN	TNG5221	B	TTL	-55	125			5.0		*60	*30	40	1.2	1.7	.700	* 18		.45	2.4	23,47
NAND,DUAL 2 INPUT	TRAN	TNG5222	B	TTL	0	75			5.0		*60	*30	40	1.2	1.7	.700	* 18		.45	2.4	23,47
NAND,DUAL 2 INPUT	TRAN	TNG5223	B	TTL	-55	125			5.0		*60	*30	24	1.2	1.7	.700	* 18		.45	2.4	23,47
NAND,DUAL 2 INPUT	TRAN	TNG5224	B	TTL	0	75			5.0		*60	*30	24	1.2	1.7	.700	* 18		.45	2.4	23,47
NAND,DUAL 2 INPUT	TRAN	TNG5421	B	TTL	-55	125			5.0		*60	*30		1.2	1.7						23,47
NAND,DUAL 2 INPUT	TRAN	TNG5422	B	TTL	0	75			5.0		*60	*30		1.2	1.7						23,47
NAND,DUAL 2 INPUT EX	SIGN	CS715	A	DTL	-55	125			4.0		45	8	* 15				17		.35	3.80	12,81
NAND,DUAL 2 INPUT EX	SIGN	CS716	A	DTL	-55	125			4.0		55	8	* 15				17		.35	3.80	12,81
NAND,DUAL 2-3 INPUT	FSC	CS700	A	DTL	-55	125			4.0	15				1.10	1.70	.650	15		.45	3.50	11,55
NAND,DUAL 2-3 INPUT	FSC	CS701	A	DTL	-55	125			4.0	25				1.10	1.70	.650	15		.45	3.50	11,55
NAND,DUAL 2-3 INPUT	GME	264DR	A	DTL	-55	125		4.0	-2.0	20			4				* 45		.40	3.50	17,59
NAND,DUAL 2-3 INPUT	GME	264D5	A	DTL	-55	125		4.0	-2.0	12			5				* 45		.40		17,59
NAND,DUAL 2-3 INPUT	MOTA	MC207	A	DTL	-55	125		4.0	-2.0		*17	*12	5				30				13,50
NAND,DUAL 2-3 INPUT	MOTA	MC208	A	DTL	-55	125		4.0	-2.0		*30	*17	4				30		.60	3.50	13,50
NAND,DUAL 2-3 INPUT	MOTA	MC257	A	DTL	0	70		4.0	-2.0		*12	*20	5				30				13
NAND,DUAL 2-3 INPUT	MOTA	MC258	A	DTL	0	70		4.0	-2.0		*34	*20	4				30		.55	3.50	13
NAND,DUAL 2-3 INPUT	SIGN	CS700	A	DTL	-55	125		4.0	-2.0	12			5				* 55		.60		12,56
NAND,DUAL 2-3 INPUT	SIGN	CS701	A	DTL	-55	125		4.0	-2.0	20			4				* 55		.60	3.50	12,56
NAND,DUAL 2EX-3 INPUT	MOTA	MC830G	A	DTL	0	75			5.0		*20		8	1.10	1.90		* 55		.45		11
NAND,DUAL 2EX-3 INPUT	MOTA	MC832G	A	DTL	0	75			5.0		*75		25	1.10	1.90		* 60		.45		39
NAND,DUAL 2EX-3 INPUT	MOTA	MC844G	A	DTL	0	75			5.0		*55		27	1.10	1.90		* 42		.45		11
NAND,DUAL 2EX-3 INPUT	MOTA	MC930G	A	DTL	-55	125			5.0		*16		8	1.10	2.00		* 55		.40		11
NAND,DUAL 2EX-3 INPUT	MOTA	MC932G	A	DTL	-55	125			5.0		*66		25	1.10	2.00		* 60		.40		39
NAND,DUAL 2EX-3 INPUT	MOTA	MC944G	A	DTL	-55	125			5.0		*50		27	1.10	2.00		* 42		.40		11
NAND,DUAL 3 INPUT	FSC	LPDT9041	A	DTL	-55	125			5.0		E15	E 6	10	.9	1.7	.7	63		.2	2.7	44,75
NAND,DUAL 3 INPUT	GI	PC15	H	DTL	-55	125	12.0	4.2	-3.0	*60			5				8		.30	5.00	16
NAND,DUAL 3 INPUT	GME	264B3	A	DTL	-55	125			4.0		*55	* 9	15	.80	2.00	.400	* 35		.40	3.00	17,59
NAND,DUAL 3 INPUT	GME	264D3	A	DTL	-55	125			4.0		*55	* 9	15	.80	2.00	.400	* 35		.40	3.00	17,59
NAND,DUAL 3 INPUT	HOFF	HMC002	B	TTL	-55	125			6.0	25			15				25		.35	3.50	12
NAND,DUAL 3 INPUT	MOTA	MC212	A	DTL	-55	125			4.0		*12	*15	5				30				13,50
NAND,DUAL 3 INPUT	MOTA	MC213	A	DTL	-55	125			4.0		*30	*15	4				30		.60	3.50	13,50
NAND,DUAL 3 INPUT	MOTA	MC262	A	DTL	0	70			4.0		*19	*12	5				30				13
NAND,DUAL 3 INPUT	MOTA	MC263	A	DTL	0	70			4.0		*33	*19	4				30		.55	3.50	13
NAND,DUAL 3 INPUT	PHIL	PL9987	A	TTL	-55	125			3.0	J44			4	.42	.85	.19	50		.23	1.00	51
NAND,DUAL 3 INPUT	RAY	RM201	A	DTL	-55	125			6.0	8			6	1.00	1.80		31		.25		21,53
NAND,DUAL 3 INPUT	RAY	RM210	A	DTL	-55	125			6.0	30			20	1.00	1.80	.800	45		.20	5.00	21,53
NAND,DUAL 3 INPUT	SIGN	SE113	A	DTL	-55	125			4.0		*55	* 8	* 15				17		.35	3.80	12,81
NAND,DUAL 3 INPUT	SIGN	SE157	A	DTL	-55	125			4.0		*55	* 8	15				17		.40	3.90	12,52
NAND,DUAL 3 INPUT	TI	SN472	A	DTL	0	125			4.0	4			5				40				74
NAND,DUAL 3 INPUT	TI	SN533	F	DTL	-55	125			3.5	18			10	.30	1.70		25		.30	2.20	74
NAND,DUAL 3 INPUT	TI	SN7330	F	DTL	0	70			3.0		10	4	10	.40	1.70		25		.30	1.70	58,76

CIRCUIT DESCRIPTION	MFR	MFRS PART NUMBER	TECH	TYPE OF LOGIC	OPER. TEMP. CENTGRDE		SUPPLY VOLTAGE VDC			SUPPLY POWER MILLIWATTS			FAN-OUT	INPUT THRESHOLD VOLTS		NOISE IMMUNITY VOLTS	DELAY NANO-SECS	OPERATING SPEED MCPS	OUTPUT LEVEL VOLTS		PACKAGE TYPE
					MIN	MAX	NO. 3	NO. 2	NO. 1	AVE	ON	OFF		ZERO	ONE				ZERO	ONE	
NAND,DUAL 3 INPUT	TRAN	TNG3145	B	TTL	-55	125			5.0		*30	*15	15	1.2	1.7	.700	* 10		.45	2.4	23,47
NAND,DUAL 3 INPUT	TRAN	TNG3146	B	TTL	0	75			5.0		*30	*15	15	1.2	1.7	.700	* 10		.45	2.4	23,47
NAND,DUAL 3 INPUT	TRAN	TNG3147	B	TTL	-55	125			5.0		*30	*15	7	1.2	1.7	.700	* 10		.45	2.4	23,47
NAND,DUAL 3 INPUT	TRAN	TNG3148	B	TTL	0	75			5.0		*30	*15	7	1.2	1.7	.700	* 10		.45	2.4	23,47
NAND,DUAL 3 INPUT	WMED	WC201	A	DTL	0	75			6.0	8			6	1.0	1.8		30		.45		21,43
NAND,DUAL 3 INPUT	WMED	WC210	A	DTL	0	75			6.0	33			12	1.0	1.8		45		.45		21,43
NAND,DUAL 3 INPUT	WMED	WM201	A	DTL	-55	125			6.0	8			6	1.00	1.80		30		.25		21,53
NAND,DUAL 3 INPUT	WMED	WM210	A	DTL	-55	125			6.0	*30			22	1.20	1.80	1.000	45		.20	6.00	21,43
NAND,DUAL 3 INPUT	WMED	WS811	A	DTL	0	125			4.0	*10			10	.70	1.75	.250	50		.45	2.50	53
NAND,DUAL 3 INPUT	WMED	WS817	A	DTL	0	125				7			25								43
NAND,DUAL 3 INPUT EX	FSC	LPDT9042	A	DTL	-55	125			5.0		E15	E 6	10	.9	1.7	.7	63	2.5	.2	2.7	44,75
NAND,DUAL 3 INPUT EX	GME	264E3	A	DTL	-55	125			4.0		*55	* 9	15	.80	2.00	.400	* 35		.40	3.00	45
NAND,DUAL 3 INPUT EX	MOTA	MC650	A	DTL	0	75		10.0	-10.0		132	*87	* 5	5.00	5.70	3.900	45		.72	9.60	26
NAND,DUAL 3 INPUT EX	RAY	RM221	A	DTL	-55	125			6.0	8			6	1.00	1.80		31		.25		21,43
NAND,DUAL 3 INPUT EX	SIGN	SE112	A	DTL	-55	125			4.0		*55	* 8	* 15				17		.35	3.80	12,81
NAND,DUAL 3 INPUT EX	WMED	WC221	A	DTL	0	75			6.0	8			6	1.0	1.8		30		.45		21,43
NAND,DUAL 3 INPUT EX	WMED	WM221	A	DTL	-55	125			6.0	8			6	1.00	1.80		30		.25		21,43
NAND,DUAL 4 INPUT	FSC	TTL103	A	TTL	-55	125			5.0		40	18	10	.70	1.65	.350	25		.35	3.00	11,44
NAND,DUAL 4 INPUT	GME	264B4	A	DTL	-55	125			4.0		*55	* 9	15	.80	2.00	.400	* 35		.40	3.00	45
NAND,DUAL 4 INPUT	GME	264D4	A	DTL	-55	125			4.0		*55	* 9	15	.80	2.00	.400	* 35		.40	3.00	45
NAND,DUAL 4 INPUT	MOTA	MC402	F	TTL	-55	125							15	.50	2.40		15				49
NAND,DUAL 4 INPUT	PHIL	PL103	A	TTL	-55	125			5.0	20	*12	*19	15	.33	.27		* 50				41
NAND,DUAL 4 INPUT	RAD	RD210	C	DTL	-55	125			5.0		12	8	8				7		.40	4.00	42
NAND,DUAL 4 INPUT	RAY	RM211	A	DTL	-55	125			6.0	8			6	1.00	1.80		31		.25		21,43
NAND,DUAL 4 INPUT	SIGN	SE111	A	DTL	-55	125			4.0		*55	* 8	* 15				17		.35	3.80	12,81
NAND,DUAL 4 INPUT	SIGN	SE155	A	DTL	-55	125			4.0		*55	* 8	* 15				17		.35	3.90	12,81
NAND,DUAL 4 INPUT	SIGN	SE455	A	TTL	-55	125			4.0		*16	* 4	15	.70	2.10	.400	* 150		.30	2.70	81
NAND,DUAL 4 INPUT	SIGN	SE816	A	TTL	-55	125			5.0		15	5	* 10				13		.20	2.4	81
NAND,DUAL 4 INPUT	SIGN	SE855	A	TTL	-55	125			5.0		43	10	30				13				81
NAND,DUAL 4 INPUT	SILX	A02	A	DTL	-55	125			5.0	7			15	1.70	2.70	.700	18		1.00	4.60	20,46
NAND,DUAL 4 INPUT	SILX	A05	A	DTL	-55	125			5.0	15			10	1.70	2.70	.700	12		1.00	4.60	20,80
NAND,DUAL 4 INPUT	SILX	A07	A	DTL	-55	125			5.0	7			5	1.70	2.70	.700	18		1.00	4.60	20,46
NAND,DUAL 4 INPUT	SILX	A12	A	DTL	-55	125			5.0	15			* 5	1.70	2.70	.700	12		1.00	4.60	20,80
NAND,DUAL 4 INPUT	SILX	A20	A	DTL	-55	125			5.0	7				1.70	2.70				1.00		20,46
NAND,DUAL 4 INPUT	SW	SWG40	A	TTL	-55	125			5.0	15			15				12	20			27,49
NAND,DUAL 4 INPUT	SW	SWG41	A	TTL	-55	125			5.0	15			7				12	20			27,49
NAND,DUAL 4 INPUT	SW	SWG42	A	TTL	0	75			5.0	15			12				12	20			27,49
NAND,DUAL 4 INPUT	SW	SWG43	A	TTL	0	75			5.0	15			6				12	20			27,49
NAND,DUAL 4 INPUT	SYL	SG130	B	TTL	-55	125			5.0	30			30	1.2	1.7	.75	25		.45	3.00	40
NAND,DUAL 4 INPUT	SYL	SG131	B	TTL	-55	125			5.0	30			15	1.2	1.7	.75	25		.45	3.00	40
NAND,DUAL 4 INPUT	SYL	SG132	B	TTL	0	75			5.0	30			24	1.2	1.7	.75	25		.45	3.00	40
NAND,DUAL 4 INPUT	SYL	SG133	B	TTL	0	75			5.0	30			12	1.2	1.7	.75	25		.45	3.00	40
NAND,DUAL 4 INPUT	SYL	SG240	B	TTL	-55	125			5.0	22			11	1.1	1.7	.75	6		.45	3.00	40
NAND,DUAL 4 INPUT	SYL	SG241	B	TTL	-55	125			5.0	22			6	1.1	1.7	.75	6		.45	3.00	40
NAND,DUAL 4 INPUT	SYL	SG242	B	TTL	0	75			5.0	22			9	1.1	1.7	.75	6		.45	3.00	40
NAND,DUAL 4 INPUT	SYL	SG243	B	TTL	0	75			5.0	22			5	1.1	1.7	.75	6		.45	3.00	40
NAND,DUAL 4 INPUT	SYL	SG40	B	TTL	-55	125			5.0	15			# 15	1.20	1.70	.800	10	20	.40	3.20	40
NAND,DUAL 4 INPUT	SYL	SG41	B	TTL	-55	125			5.0	15			# 7	1.20	1.70	.800	10	20	.40	3.20	40
NAND,DUAL 4 INPUT	SYL	SG42	B	TTL	0	75			5.0	15			# 12	1.20	1.80	.800	10	20	.40	3.10	40

CIRCUIT DESCRIPTION	MFR	MFRS PART NUMBER	TECH	TYPE OF LOGIC	OPER. TEMP. CENTGRDE MIN	MAX	SUPPLY VOLTAGE VDC NO. 3	NO. 2	NO. 1	SUPPLY POWER MILLIWATTS AVE	ON	OFF	FAN-OUT	INPUT THRESHOLD VOLTS ZERO	ONE	NOISE IMMUNITY VOLTS	DELAY NANO-SECS	OPERATING SPEED MCPS	OUTPUT LEVEL VOLTS ZERO	ONE	PACKAGE TYPE
NAND,DUAL 4 INPUT	SYL	SG43	B	TTL	0	75			5.0	15			# 6	1.20	1.80	.800	10	20	.40	3.10	40
NAND,DUAL 4 INPUT	TI	SN5420	A	TTL	-55	125			5.0	10			* 10	.90	2.20	.400	13		.40	2.60	48
NAND,DUAL 4 INPUT	TI	SN5440	A	TTL	-55	125			5.0	10			* 30	.90	2.20	.400	18		.40	2.60	48
NAND,DUAL 4 INPUT	TI	SN7420	F	TTL	0	70			5.0		15	5	* 10	.80	2.00	.400	13		.40	2.40	48,76
NAND,DUAL 4 INPUT	TI	SN7440	F	TTL	0	70			5.0		43	10	* 30	.80	2.00	.400	13		.40	2.40	48,76
NAND,DUAL 4 INPUT	TRAN	TNG3111	B	TTL	-55	125			5.0		20	10	15	1.2	1.7	.700	* 18		.45	2.4	23,47
NAND,DUAL 4 INPUT	TRAN	TNG3112	B	TTL	0	75			5.0		20	10	15	1.2	1.7	.700	* 18		.45	2.4	23,47
NAND,DUAL 4 INPUT	TRAN	TNG3113	B	TTL	-55	125			5.0		20	10	7	1.2	1.7	.700	* 18		.45	2.4	23,47
NAND,DUAL 4 INPUT	TRAN	TNG3114	B	TTL	0	75			5.0		20	10	7	1.2	1.7	.700	* 18		.45	2.4	23,47
NAND,DUAL 4 INPUT	TRAN	TNG3141	B	TTL	-55	125			5.0		*30	*15	15	1.2	1.7	.700	* 10		.45	2.4	23,47
NAND,DUAL 4 INPUT	TRAN	TNG3142	B	TTL	0	75			5.0		*30	*15	15	1.2	1.7	.700	* 10		.45	2.4	23,47
NAND,DUAL 4 INPUT	TRAN	TNG3143	B	TTL	-55	125			5.0		*30	*15	7	1.2	1.7	.700	* 10		.45	2.4	23,47
NAND,DUAL 4 INPUT	TRAN	TNG3144	B	TTL	0	75			5.0		*30	*15	7	1.2	1.7	.700	* 10		.45	2.4	23,47
NAND,DUAL 4 INPUT	WMED	WC211	A	DTL	0	75			6.0	8			6	1.0	1.8		30		.45		21,43
NAND,DUAL 4 INPUT	WMED	WC241	A	DTL	0	75			6.0	8			6	1.0	1.8		30		.45		43
NAND,DUAL 4 INPUT	WMED	WM211	A	DTL	-55	125			6.0	8			6	1.00	1.80		30		.25		21,43
NAND,DUAL 4 INPUT	WMED	WM241	A	DTL	-55	125			6.0	10			9	1.00	2.0	.55	32		.45	5.8	43
NAND,DUAL 4 INPUT	WMED	WM701	A	TTL	-55	125			5.0		22	45	15	.60	1.65	.250	50		.35	2.65	43,91
NAND,DUAL 4 INPUT EX	FSC	DTL930	A	DTL	-55	125			5.0	8			7	1.10	2.00	.600	20		.40	2.60	11,44
NAND,DUAL 4 INPUT EX	FSC	DTL932	A	DTL	-55	125			5.0	25			25	1.10	2.00	.600	35		.40	2.60	50
NAND,DUAL 4 INPUT EX	FSC	DTL944	A	DTL	-55	125			5.0		38	6	27	1.10	1.90	.600	32		.40	2.50	11,44
NAND,DUAL 4 INPUT EX	FSC	FL93029	A	DTL	0	70			5.0	8			7	1.10	2.00	.600	20		.40	2.60	11,44
NAND,DUAL 4 INPUT EX	FSC	FL93229	A	DTL	0	70			5.0	25			25	1.10	2.00	.600	35		.40	2.60	50
NAND,DUAL 4 INPUT EX	FSC	FL94429	A	DTL	0	70			5.0		38	6	27	1.10	1.90	.600	32		.40	2.50	11,44
NAND,DUAL 4 INPUT EX	GME	264E4	A	DTL	-55	125			4.0		*55	* 9	15	.80	2.00	.400	* 35		.40	3.00	45
NAND,DUAL 4 INPUT EX	MOTA	MC651	A	DTL	0	75		10.0	-10.0		132	*87	* 5	5.00	5.70	3.900	45		.72	9.60	49
NAND,DUAL 4 INPUT EX	MOTA	MC830F	A	DTL	0	75			5.0		*20		8	1.10	1.90		* 55		.45		39
NAND,DUAL 4 INPUT EX	MOTA	MC832F	A	DTL	0	75			5.0		*75		25	1.10	1.90		* 60		.45		39
NAND,DUAL 4 INPUT EX	MOTA	MC844F	A	DTL	0	75			5.0		*55		27	1.10	1.90		* 42		.45		39
NAND,DUAL 4 INPUT EX	MOTA	MC930F	A	DTL	-55	125			5.0		*16		8	1.10	2.00		* 55		.40		39
NAND,DUAL 4 INPUT EX	MOTA	MC932F	A	DTL	-55	125			5.0		*66		25	1.10	2.00		* 60		.40		39
NAND,DUAL 4 INPUT EX	MOTA	MC944F	A	DTL	-55	125			5.0		*50		27	1.10	2.00		* 42		.40		39
NAND,DUAL 4 INPUT EX	PHIL	PL930	A	DTL	-55	125			5.0				8	1.10	2.0	.600	20		.40	2.60	41
NAND,DUAL 4 INPUT EX	PHIL	PL932	A	DTL	-55	125			5.0	25			25	1.10	2.00	.600	35		.40	2.60	41
NAND,DUAL 4 INPUT EX	PHIL	PL944	A	DTL	-55	125			5.0	50	38	6	27	1.10	1.90	.600	32		.40	2.50	41
NAND,DUAL 4 INPUT EX	PHIL	PL961	A	DTL	-55	125			5.0	27			8	1.10	2.0	.600	* 48		.40	2.60	41
NAND,DUAL 4 INPUT EX	RAD	RD209	C	DTL	-55	125			5.0		26	18	12				7		.40	2.60	42
NAND,DUAL 4 INPUT EX	RAD	RD309	C	DTL	-55	125			5.0		26	18	8				7		.40	2.60	42
NAND,DUAL 4 INPUT EX	RAD	RD310	C	DTL	-55	125			5.0		12	8	5				7		.40	4.00	42
NAND,DUAL 4 INPUT EX	RAD	RD509	C	DTL	0	75			5.0		26	18	12				7		.40	2.60	42
NAND,DUAL 4 INPUT EX	RAD	RD510	C	DTL	0	75			5.0		15	10	8				7		.40	4.00	42
NAND,DUAL 4 INPUT EX	RAY	RM231	A	DTL	-55	125			6.0	8			6	1.00	1.80		31		.25		43
NAND,DUAL 4 INPUT EX	RCA	CD2200	A	DTL	-55	125			4.	2			* 6		3.50		85		.25	3.23	82
NAND,DUAL 4 INPUT EX	SIGN	SE116	A	DTL	-55	125			4.0		*19	* 9	* 6	1.20	2.50	.600	* 43		.35	3.10	81
NAND,DUAL 4 INPUT EX	SIGN	SE156	A	DTL	-55	125			4.0		*55	* 8	* 15				17		.35	3.90	12,81
NAND,DUAL 4 INPUT EX	SIGN	SE416	A	DTL	-55	125			4.0		* 9	* 4	5	.70	2.10	.400	* 100		.30	2.70	81
NAND,DUAL 4 INPUT EX	SW	SW930	A	DTL	-55	125			5.0	8			9	1.10	2.0	.60	20		.40	2.6	10,49
NAND,DUAL 4 INPUT EX	SW	SW932	A	DTL	-55	125			5.0	*13			30	1.1	2.0	.500	25		.40	2.5	10,49
NAND,DUAL 4 INPUT EX	SW	SW944	A		-55	125			5.0	100			30	1.1	2.0	.600	25		.40	2.60	10,49

CIRCUIT DESCRIPTION	MFR	MFRS PART NUMBER	TECH	TYPE OF LOGIC	OPER. TEMP. CENTGRDE		SUPPLY VOLTAGE VDC			SUPPLY POWER MILLIWATTS			FAN-OUT	INPUT THRESHOLD VOLTS		NOISE IMMU-NITY VOLTS	DELAY NANO-SECS	OPER-ATING SPEED MCPS	OUTPUT LEVEL VOLTS		PACK-AGE TYPE
					MIN	MAX	NO. 3	NO. 2	NO. 1	AVE	ON	OFF		ZERO	ONE				ZERO	ONE	
NAND, DUAL 4 INPUT EX	WMED	WC231	A	DTL	0	75			6.0	8			6	1.0	1.8		30		.45		43
NAND, DUAL 4 INPUT EX	WMED	WC261	A	DTL	0	75			6.0	8			6	1.0	1.8		30		.45		43
NAND, DUAL 4 INPUT EX	WMED	WM231	A	DTL	-55	125			6.0	8			6	1.00	1.80		30		.25		43
NAND, DUAL 4 INPUT EX	WMED	WM261	A	DTL	-55	125			6.0	10			6	1.00	2.00	.55	32		.45	5.8	43
NAND, DUAL 5 INPUT	SIGN	CS730	A	DTL	-55	125			4.0		*23	* 9	* 6	1.20	2.50	.600	* 43		.35	3.10	81
NAND, DUAL 5 INPUT	TI	SN5311	F	DTL	-55	125			3.5	*24			10				25				48
NAND, DUAL 5 INPUT	TI	SN7311	F	DTL	0	70			3.0		10	4	10	.40	1.70		25		.30	1.70	58,76
NAND, DUAL 5 INPUT EX	WMED	WM510	A	DTL	-55	125			4.5	10			27								43
NAND, QUAD 2 INPUT	FSC	DTL946	A	DTL	-55	125			5.0	8			8	1.10	2.00	.600	24		.40	2.60	11,44
NAND, QUAD 2 INPUT	FSC	FL94629	A	DTL	0	70			5.0	8			8	1.10	2.00	.600	24		.40	2.60	11,44
NAND, QUAD 2 INPUT	GME	263Q2	A	DTL	-55	125			4.0		*20	* 9	8	.80	2.00	.400	* 30		.40	3.50	45
NAND, QUAD 2 INPUT	MOTA	MC846	A	DTL	0	75			5.0		*20		8	1.10	1.90		* 55		.45		39
NAND, QUAD 2 INPUT	MOTA	MC946	A	DTL	-55	125			5.0		*16		8	1.10	2.00		* 55		.40		39
NAND, QUAD 2 INPUT	PHIL	PL946	A	DTL	-55	125			5.0				8	1.10	2.00	.600	20		.40	2.60	41
NAND, QUAD 2 INPUT	PHIL	PL949	A	DTL	-55	125			5.0	26			8	1.10	2.0	.600	* 48		.40	2.60	41
NAND, QUAD 2 INPUT	RAD	RD206	C	DTL	-55	125			5.0		12	8	8				7		.40	4.00	42
NAND, QUAD 2 INPUT	RAD	RD306	C	DTL	-55	125			5.0		12	8	5				7		.40	4.00	42
NAND, QUAD 2 INPUT	RAD	RD506	C	DTL	0	75			5.0		15	10	8				7		.40	4.00	42
NAND, QUAD 2 INPUT	RCA	CD2201	A	DTL	-55	125			4.	2			* 6		3.50		85		.25	3.23	82
NAND, QUAD 2 INPUT	SIGN	CS720	A	DTL	-55	125			4.0		*19	* 9	* 6	1.20	2.50	.600	* 43		.35	3.10	81
NAND, QUAD 2 INPUT	SIGN	SE180	A	DTL	-55	125			4.0		*19	* 9	* 6	1.20	2.50	.600	* 43		.35	3.10	81
NAND, QUAD 2 INPUT	SIGN	SE480	A	DTL	-55	125			4.0		* 9	* 3	7	.70	2.10	.400	* 67		.30	2.70	81
NAND, QUAD 2 INPUT	SIGN	SE870	A	TTL	-55	125			5.0		15	5	10				13		.20	2.4	81
NAND, QUAD 2 INPUT	SILX	A14	A	DTL	-55	125			5.0	7			* 5	1.70	2.70		18		1.00		46
NAND, QUAD 2 INPUT	SILX	A15	A	DTL	-55	125			5.0	7			* 10	1.70	2.70		18		1.00		46
NAND, QUAD 2 INPUT	SW	SWG140	A	TTL	-55	125			5.0	15			15				12	20			49
NAND, QUAD 2 INPUT	SW	SWG141	A	TTL	-55	125			5.0	15			7				12	20			49
NAND, QUAD 2 INPUT	SW	SWG142	A	TTL	0	75			5.0	15			12				12	20			49
NAND, QUAD 2 INPUT	SW	SWG143	A	TTL	0	75			5.0	15			6				12	20			49
NAND, QUAD 2 INPUT	SW	SW946	A	DTL	-55	125			5.0	8			9	1.10	2.0		20		.40	2.6	27,49
NAND, QUAD 2 INPUT	SYL	SG140	B	TTL	-55	125			5.0	15			15	1.20	1.70	.800	* 34	20	.40	3.20	40
NAND, QUAD 2 INPUT	SYL	SG141	B	TTL	-55	125			5.0	15			7	1.20	1.70	.800	* 37	20	.40	3.20	40
NAND, QUAD 2 INPUT	SYL	SG142	B	TTL	0	75			5.0	15			12	1.20	1.80	.800	* 34	20	.40	3.10	40
NAND, QUAD 2 INPUT	SYL	SG143	B	TTL	0	75			5.0	15			6	1.20	1.80	.800	* 36	20	.40	3.10	40
NAND, QUAD 2 INPUT	SYL	SG220	B	TTL	-55	125			5.0	22			11	1.1	1.7	.65	6		.45	3.00	40
NAND, QUAD 2 INPUT	SYL	SG221	B	TTL	-55	125			5.0	22			6	1.1	1.7	.65	6		.45	3.00	40
NAND, QUAD 2 INPUT	SYL	SG222	B	TTL	0	75			5.0	22			9	1.1	1.7	.65	6		.45	3.00	40
NAND, QUAD 2 INPUT	SYL	SG223	B	TTL	0	75			5.0	22			5	1.1	1.7	.65	6		.45	3.00	40
NAND, QUAD 2 INPUT	TI	SN5360	F	DTL	-55	125			3.5	10			* 10	. 3	2.10		25		.30	2.20	48
NAND, QUAD 2 INPUT	TI	SN5400	A	TTL	-55	125			5.0	10			* 10	.90	2.20	.400	13		.40	2.60	48
NAND, QUAD 2 INPUT	TI	SN7360	F	DTL	0	70			3.0		10	4	10	.40	1.70		25		.30	1.70	48,76
NAND, QUAD 2 INPUT	TI	SN7400	F	TTL	0	70			5.0		15	5	* 10	.80	2.00	.400	13		.40	2.40	48,76
NAND, QUAD 2 INPUT	TRAN	TNG3411	B	TTL	-55	125			5.0		*30	*15	15	1.2	1.7	.700	* 18		.45	2.4	47
NAND, QUAD 2 INPUT	TRAN	TNG3412	B	TTL	0	75			5.0		*30	*15	15	1.2	1.7	.700	* 18		.45	2.4	47
NAND, QUAD 2 INPUT	TRAN	TNG3413	B	TTL	-55	125			5.0		*30	*15	7	1.2	1.7	.700	* 18		.45	2.4	47
NAND, QUAD 2 INPUT	TRAN	TNG3414	B	TTL	0	75			5.0		*30	*15	7	1.2	1.7	.700	* 18		.45	2.4	47
NAND, QUAD 2 INPUT	WMED	WC246	A	DTL	0	75			6.0	8			6	1.0	1.8		30		.45		43
NAND, QUAD 2 INPUT	WMED	WC266	A	DTL	0	75			6.0	8			6	1.0	1.8		30		.45		43
NAND, QUAD 2 INPUT	WMED	WM246	A	DTL	-55	125			6.0	8			6	1.00	1.80		19		.25		43

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CIRCUIT DESCRIPTION	MFR	MFRS PART NUMBER	TECH	TYPE OF LOGIC	OPER. TEMP. CENTGRDE		SUPPLY VOLTAGE VDC			SUPPLY POWER MILLIWATTS			FAN-OUT	INPUT THRESHOLD VOLTS		NOISE IMMUNITY VOLTS	DELAY NANO-SECS	OPER-ATING SPEED MCPS	OUTPUT LEVEL VOLTS		PACK-AGE TYPE
					MIN	MAX	NO. 3	NO. 2	NO. 1	AVE	ON	OFF		ZERO	ONE				ZERO	ONE	
NAND,QUAD 2 INPUT	WMED	WM266	A	DTL	-55	125			6.0	10			9	1.00	2.00	.55	32		.45	5.8	43
NAND,TPIPLE 2EX-3-3 INP	WMED	WC206	A	DTL	0	75			6.0	8			6	1.0	1.8		30		.45		43
NAND,TPIPLE 3 INPUT	SYL	SG190	B	TTL	-55	125			5.0	15			15	1.2	1.7	.75	10		.45	3.00	40
NAND,TPIPLE 3 INPUT	SYL	SG191	B	TTL	-55	125			5.0	15			7	1.2	1.7	.75	10		.45	3.00	40
NAND,TPIPLE 3 INPUT	SYL	SG192	B	TTL	0	75			5.0	15			12	1.2	1.7	.75	10		.45	3.00	40
NAND,TPIPLE 3 INPUT	SYL	SG193	B	TTL	0	75			5.0	15			6	1.2	1.7	.75	10		.45	3.00	40
NAND,TRIPLE 1-2-2 INPUT	SW	SW962Z	A		-55	125			5.0	8			9	1.1	2.0				.40	2.60	10,49
NAND,TRIPLE 2 INPUT	SYL	SG160	B	TTL	-55	125			5.0	15			15	1.2	1.7	.75	15		.45	3.00	40
NAND,TRIPLE 2 INPUT	SYL	SG161	B	TTL	-55	125			5.0	15			7	1.2	1.7	.75	15		.45	3.00	40
NAND,TRIPLE 2 INPUT	SYL	SG162	B	TTL	0	75			5.0	15			12	1.2	1.7	.75	15		.45	3.00	40
NAND,TRIPLE 2 INPUT	SYL	SG163	B	TTL	0	75			5.0	15			6	1.2	1.7	.75	15		.45	3.00	40
NAND,TRIPLE 2 INPUT EX	SIGN	CS727	A	DTL	-55	125			4.0		*23	* 9	* 6	1.20	2.50	.600	* 43		.35	3.10	81
NAND,TRIPLE 2EX-3-3 INP	RAY	RM206	A	DTL	-55	125			6.0	22			6	1.00	1.80		30		.25		43
NAND,TRIPLE 2EX-3-3 INP	WMED	WC226	A	DTL	0	75			6.0	8			6	1.0	1.8		30		.45		43
NAND,TRIPLE 2EX-3-3 INP	WMED	WM206	A	DTL	-55	125			6.0	7			6	1.00	1.80		30		.25		43
NAND,TRIPLE 2EX-3-3 INP	WMED	WM226	A	DTL	-55	125			6.0	11			6	1.0	2.0	.55	23		.45	5.8	43
NAND,TRIPLE 3 INPUT	FSC	DTL962	A	DTL	-55	125			5.0	8			8				24				44
NAND,TRIPLE 3 INPUT	FSC	FL96229	A	DTL	0	70			5.0	8			8				24				44
NAND,TRIPLE 3 INPUT	GME	26469	A	DTL	-55	125			4.0		*20	* 9	8	.80	2.00	.400	* 30		.40	3.50	45
NAND,TRIPLE 3 INPUT	MOTA	MC862	A	DTL	0	75			5.0		*20		8	1.10	1.90		* 55		.45		39
NAND,TRIPLE 3 INPUT	MOTA	MC962	A	DTL	-55	125			5.0		*16		8	1.10	2.00		* 55		.40		39
NAND,TRIPLE 3 INPUT	PHIL	PL962	A	DTL	-55	125			5.0	17				1.10	2.0	.600	* 55		.40	2.60	41
NAND,TRIPLE 3 INPUT	PHIL	PL963	A	DTL	-55	125			5.0	26				1.10	2.0	.600	* 48		.40	2.60	41
NAND,TRIPLE 3 INPUT	RAD	RD205	C	DTL	-55	125			5.0		12	8	8				7		.40	4.00	42
NAND,TRIPLE 3 INPUT	RAD	RD305	C	DTL	-55	125			5.0		12	8	5				7		.40	4.00	42
NAND,TRIPLE 3 INPUT	RAD	RD505	C	DTL	0	75			5.0		15	10	8				7		.40	4.00	42
NAND,TRIPLE 3 INPUT	RAY	RM216	A	DTL	-55	125			6.0	22			6	1.00	1.80		30		.25		43
NAND,TRIPLE 3 INPUT	SIGN	CS721	A	DTL	-55	125			4.0		*19	* 9	* 6	1.20	2.50	.600	* 43		.35	3.10	81
NAND,TRIPLE 3 INPUT	SIGN	SE170	A	DTL	-55	125			4.0		*19	* 9	* 6	1.20	2.50	.600	* 43		.35	3.10	81
NAND,TRIPLE 3 INPUT	SIGN	SE880	A	TTL	-55	125			5.0		15	5	10				13		.20	2.4	81
NAND,TRIPLE 3 INPUT	SW	SW962Y	A		-55	125			5.0	8			9	1.1	2.0				.40	2.60	10,49
NAND,TRIPLE 3 INPUT	TI	SN5331	F	DTL	-55	125			3.5	10			* 10	.30	2.10		25		.30	2.20	48
NAND,TRIPLE 3 INPUT	TI	SN5410	A	TTL	-55	125			5.0	10			* 10	.90	2.20	.400	13		.40	2.60	48
NAND,TRIPLE 3 INPUT	TI	SN7331	F	DTL	0	70			3.0		10	4	10	.40	1.70		25		.30	1.70	58,76
NAND,TRIPLE 3 INPUT	TI	SN7410	F	TTL	0	70			5.0		15	5	* 10	.80	2.00	.400	13		.40	2.40	48,76
NAND,TRIPLE 3 INPUT	TRAN	TNG3311	B	TTL	-55	125			5.0		*30	*15	15	1.2	1.7	.700	* 18		.45	2.4	47
NAND,TRIPLE 3 INPUT	TRAN	TNG3312	B	TTL	0	75			5.0		*30	*15	15	1.2	1.7	.700	* 18		.45	2.4	47
NAND,TRIPLE 3 INPUT	TRAN	TNG3313	B	TTL	-55	125			5.0		*30	*15	7	1.2	1.7	.700	* 18		.45	2.4	47
NAND,TRIPLE 3 INPUT	TRAN	TNG3314	B	TTL	0	75			5.0		*30	*15	7	1.2	1.7	.700	* 18		.45	2.4	47
NAND,TRIPLE 3 INPUT	WMED	WC216	A	DTL	0	75			6.0	8			6	1.0	1.8		30		.45		43
NAND,TRIPLE 3 INPUT	WMED	WC236	A	DTL	0	75			6.0	8			6	1.0	1.8		30		.45		43
NAND,TRIPLE 3 INPUT	WMED	WM216	A	DTL	-55	125			6.0	7			6	1.00	1.80		30		.25		43
NAND,TRIPLE 3 INPUT	WMED	WM236	A	DTL	-55	125			6.0	11			6	1.00	2.0	.55	23		.45	5.8	43
NAND,TRIPLE 3 INPUT	WMED	WM506	A	DTL	-55	125			4.5	19			10								43
NAND,TRIPLE 3 INPUT	WMED	WM556	A	DTL	-55	125			4.5	10			12								43
NAND,2 INPUT	FSC	SE150	A	DTL	-55	125			4.0		*60	*30					27		.45	2.00	1,55
NAND,2 INPUT	GME	264L	A	DTL	-55	125		4.0	-2.0		*60	*30	* 20				40		.40	2.00	17,59
NAND,2 INPUT	HOFF	HMC003	B	DTL	-55	125			4.0	40			15				30		.40	4.00	12
NAND,2 INPUT	HOFF	HMC1002	B	DTL	0	80		4.5	-2.0	32	48	17	* 20				* 70		.60	2.00	52

CIRCUIT DESCRIPTION	MFR	MFRS PART NUMBER	TECH	TYPE OF LOGIC	OPER. TEMP. CENTGRDE MIN	MAX	SUPPLY VOLTAGE VDC NO. 3	NO. 2	NO. 1	SUPPLY POWER MILLIWATTS AVE	ON	OFF	FAN-OUT	INPUT THRESHOLD VOLTS ZERO	ONE	NOISE IMMUNITY VOLTS	DELAY NANO-SECS	OPERATING SPEED MCPS	OUTPUT LEVEL VOLTS ZERO	ONE	PACKAGE TYPE
NAND,2 INPUT	MOTA	MC205	A	DTL	-55	125		4.5	-2.0	32	*60	*30	*20				50		.60	2.00	50,53
NAND,2 INPUT	MOTA	MC255	A	DTL	0	70		4.5	-2.0	32	*65	*30	*20				50		.50	2.00	53
NAND,2 INPUT	SIGN	SE150	A	DTL	-55	125		4.0	-2.0		*60	*30	*20				60		.60	2.00	52,56
NAND,2 INPUT	SW	SWG130	A	TTL	-55	125			5.0	30			15				12	20			27,49
NAND,2 INPUT	SW	SWG131	A	TTL	-55	125			5.0	30			7				12	20			27,49
NAND,2 INPUT	SW	SWG132	A	TTL	0	75			5.0	30			12				12	20			27,49
NAND,2 INPUT	SW	SWG133	A	TTL	0	75			5.0	30			6				12	20			27,49
NAND,3 INPUT	AMEL	B12-001	F	DTL	-55	125			4.0	5			15				100		.30	3.50	14
NAND,3 INPUT	TRAN	TNG3115	B	TTL	-55	125			5.0		*30	*15	15	1.2	1.7	.700	*18		.45	2.4	23,47
NAND,3 INPUT	TRAN	TNG3116	B	TTL	0	75			5.0		*30	*15	15	1.2	1.7	.700	*18		.45	2.4	23,47
NAND,3 INPUT	TRAN	TNG3117	B	TTL	-55	125			5.0		*30	*15	7	1.2	1.7	.700	*18		.45	2.4	23,47
NAND,3 INPUT	TRAN	TNG3118	B	TTL	0	75			5.0		*30	*15	7	1.2	1.7	.700	*18		.45	2.4	23,47
NAND,3 INPUT EXPANDABLE	FSC	SE102	A	DTL	-55	125			4.0	*7				1.10	1.70	.650	15		.45	3.50	11,55
NAND,3 INPUT EXPANDABLE	FSC	SE110	A	DTL	-55	125			4.0		34	12					20				11,55
NAND,3 INPUT EXPANDABLE	GME	254G3	A	DTL	-55	125		4.0	-2.0		6	8	*5				30		.40		17,59
NAND,3 INPUT EXPANDABLE	GME	264P	A	DTL	-55	125		4.0	-2.0	30			*20				40		.50		17,59
NAND,3 INPUT EXPANDABLE	HOFF	HMC004	B	DTL	-55	125			4.0	10							30		.40	4.00	12
NAND,3 INPUT EXPANDABLE	HOFF	HMC1001	B	DTL	0	80		4.0	-2.0	10			5				*80		.60		12
NAND,3 INPUT EXPANDABLE	MOTA	MC202	A	DTL	-55	125		4.0	-2.0		*6	*8	5				30		.60		13,50
NAND,3 INPUT EXPANDABLE	MOTA	MC204	A	DTL	-55	125		4.0	-2.0		*60	*20	20				40				13,50
NAND,3 INPUT EXPANDABLE	MOTA	MC252	A	DTL	0	70		4.0	-2.0		*7	*10	5				30				13
NAND,3 INPUT EXPANDABLE	MOTA	MC254	A	DTL	0	70		4.0	-2.0		*66	*23	20				40				13
NAND,3 INPUT EXPANDABLE	SIGN	SE102	A	DTL	-55	125		4.0	-2.0		*8	*6	5				30		.20		12,56
NAND,3 INPUT EXPANDABLE	SIGN	SE110	A	DTL	-55	125		4.0	-2.0		*60	*20	*20	1.20	1.60		40		.30		12,56
NAND,3 INPUT EXPANDABLE	TRAN	TNG4131	B	TTL	15	55			5.0		*30	*15	7	1.0	2.0	.500	*25		.50	2.5	1
NAND,4 INPUT	TI	SN359	F		0	65		6.0	-3.0	22			6				140		.70		48
NAND,4 INPUT	TRAN	TNG3031	B	TTL	15	55			5.0		*30	*15	7	1.0	2.0	.500	*25		.50	2.5	1
NAND,4 INPUT	TRAN	TNG3331	B	TTL	15	55			5.0		*60	*30	20	1.0	2.0	.500	*25		.50	2.5	1
NAND,4 INPUT	TRAN	TNG3431	B	TTL	15	55			5.0					1.0	2.0	.400			.60		1
NAND,4 INPUT	TRAN	TNG5121	B	TTL	-55	125			5.0		*60	*30	40	1.2	1.7	.700	*18		.45	2.4	23,47
NAND,4 INPUT	TRAN	TNG5122	B	TTL	0	75			5.0		*60	*30	40	1.2	1.7	.700	*18		.45	2.4	23,47
NAND,4 INPUT	TRAN	TNG5123	B	TTL	-55	125			5.0		*60	*30	24	1.2	1.7	.700	*18		.45	2.4	23,47
NAND,4 INPUT	TRAN	TNG5124	B	TTL	0	75			5.0		*60	*30	24	1.2	1.7	.700	*18		.45	2.4	23,47
NAND,4 INPUT	TRAN	TNG5321	B	TTL	-55	125			5.0		*60	*30		1.2	1.7						23,47
NAND,4 INPUT	TRAN	TNG5322	B	TTL	0	75			5.0		*60	*30		1.2	1.7						23,47
NAND,4 INPUT CLOCKED	TI	SN347	F		0	65		6.0	-3.0	22			6				140		.70		48
NAND,4 INPUT EXPANDABLE	AMEL	G12-002	F	DTL	-55	125			4.0	*2			5	1.05	1.35	.750	100		.30	3.50	14
NAND,4 INPUT EXPANDABLE	FSC	SE101	A	DTL	-55	125			4.0	*7				1.10	1.70	.650	15		.45	3.50	11,55
NAND,4 INPUT EXPANDABLE	GESP	12X101	G	DTL	-55	125		4.0	-2.0	6			5				25				15
NAND,4 INPUT EXPANDABLE	GI	NC11	H	DTL	-55	125	12.0	4.2	-3.0	*60			5				8	15	.30	5.00	16
NAND,4 INPUT EXPANDABLE	GME	254G4	A	DTL	-55	125		4.0	-2.0		6	8	*5				30		.40		17,59
NAND,4 INPUT EXPANDABLE	MOTA	MC201	A	DTL	-55	125		4.0	-2.0		*6	*8	5				30		.60		13,50
NAND,4 INPUT EXPANDABLE	MOTA	MC251	A	DTL	0	70		4.0	-2.0		*7	*10	5				30				13
NAND,4 INPUT EXPANDABLE	RAY	RM204	A	DTL	-55	125			6.0	15			6	1.00	1.80		30		.25		21,53
NAND,4 INPUT EXPANDABLE	SIGN	SE101	A	DTL	-55	125		4.0	-2.0		*8	*6	5				30		.20		12,56
NAND,4 INPUT EXPANDABLE	SILX	A01	A	DTL	-55	125			5.0	7			15	1.70	2.70	.700	18		1.00	4.60	7,46
NAND,4 INPUT EXPANDABLE	SILX	A06	A	DTL	-55	125			5.0	7			5	1.70	2.70	.700	18		1.00	4.60	7,46
NAND,4 INPUT EXPANDABLE	SILX	A10	A	DTL	-55	125			5.0	15			*10	1.70	2.70	.700	12		1.00	4.60	7,80
NAND,4 INPUT EXPANDABLE	SILX	A13	A	DTL	-55	125			5.0	15			*5	1.70	2.70	.700	12		1.00	4.60	7,80

CIRCUIT DESCRIPTION	MFR	MFRS PART NUMBER	TECH	TYPE OF LOGIC	OPER. TEMP. CENTGRDE MIN	OPER. TEMP. CENTGRDE MAX	SUPPLY VOLTAGE VDC NO. 3	SUPPLY VOLTAGE VDC NO. 2	SUPPLY VOLTAGE VDC NO. 1	SUPPLY POWER MILLIWATTS AVE	SUPPLY POWER MILLIWATTS ON	SUPPLY POWER MILLIWATTS OFF	FAN-OUT	INPUT THRESHOLD VOLTS ZERO	INPUT THRESHOLD VOLTS ONE	NOISE IMMUNITY VOLTS	DELAY NANOSECS	OPERATING SPEED MCPS	OUTPUT LEVEL VOLTS ZERO	OUTPUT LEVEL VOLTS ONE	PACKAGE TYPE
NAND,4 INPUT EXPANDABLE	WMED	WC204	A	DTL	0	75			6.0	8			6	1.0	1.8		30		.45		9,43
NAND,4 INPUT EXPANDABLE	WMED	WM204	A	DTL	-55	125			6.0	8			6	1.00	1.80		28		.25		9,53
NAND,5 INPUT EXPANDABLE	TI	SN7310	F	DTL	0	70			3.0		10		10	.40	1.70		30		.30	1.70	58,76
NAND,5 INPUT EXPANDABLE	VARO	8214	E	DTL	-55	125	6.0	3.0	-3.0	108			4	.50	3.00		10		.50	3.50	72
NAND,6 INPUT	TRAN	TNG3015	B	TTL	-55	125			5.0		*30	*15	15	1.2	1.7	.700	* 18		.45	2.4	23,47
NAND,6 INPUT	TRAN	TNG3016	B	TTL	0	75			5.0		*30	*15	15	1.2	1.7	.700	* 18		.45	2.4	23,47
NAND,6 INPUT	TRAN	TNG3017	B	TTL	-55	125			5.0		*30	*15	7	1.2	1.7	.700	* 18		.45	2.4	23,47
NAND,6 INPUT	TRAN	TNG3018	B	TTL	0	75			5.0		*30	*15	7	1.2	1.7	.700	* 18		.45	2.4	23,47
NAND,6 INPUT	TRAN	TNG3045	B	TTL	-55	125			5.0		*30	*15	15	1.2	1.7	.700	* 10		.45	2.4	23,47
NAND,6 INPUT	TRAN	TNG3046	B	TTL	0	75			5.0		*30	*15	15	1.2	1.7	.700	* 10		.45	2.4	23,47
NAND,6 INPUT	TRAN	TNG3047	B	TTL	-55	125			5.0		*30	*15	7	1.2	1.7	.700	* 10		.45	2.4	23,47
NAND,6 INPUT	TRAN	TNG3048	B	TTL	0	75			5.0		*30	*15	7	1.2	1.7	.700	* 10		.45	2.4	23,47
NAND,6 INPUT EXPANDABLE	GI	PC11	H	DTL	-55	125	12.0	4.2	-3.0	*60			5				8		.30	5.00	90
NAND,6 INPUT EXPANDABLE	RAY	RM214	A	DTL	-55	125			6.0	15			6	1.00	1.80		30		.25		21,53
NAND,6 INPUT EXPANDABLE	WMED	WC214	A	DTL	0	75			6.0	8			6	1.0	1.8		30		.45		21,43
NAND,6 INPUT EXPANDABLE	WMED	WM214	A	DTL	-55	125			6.0	8			6	1.00	1.80		35		.25		21,53
NAND,7 INPUT CLOCKED	TI	SN341	F		0	65		6.0	-3.0	12			6				140		.70		48
NAND,8 INPUT	FSC	TTL104	A	TTL	-55	125			5.0		40	18	10	.70	1.65	.350	25		.35	3.00	11,44
NAND,8 INPUT	MOTA	MC401	F	TTL	-55	125							15	.50	2.40		15				49
NAND,8 INPUT	PHIL	PL104	A	TTL	-55	125			5.0	20			15	.33	.27		* 50				41
NAND,8 INPUT	SIGN	SE808	A	TTL	-55	125			5.0		15	5	* 10				13		.20	2.4	81
NAND,8 INPUT	SW	SWG60	A	TTL	-55	125			5.0	15			15				15	20			27,49
NAND,8 INPUT	SW	SWG61	A	TTL	-55	125			5.0	15			7				15	20			27,49
NAND,8 INPUT	SW	SWG62	A	TTL	0	75			5.0	15			12				15	20			27,49
NAND,8 INPUT	SW	SWG63	A	TTL	0	75			5.0	15			6				15	20			27,49
NAND,8 INPUT	SYL	SG260	B	TTL	-55	125			5.0	22			11	1.1	1.7	.75	8		.45	3.00	40
NAND,8 INPUT	SYL	SG261	B	TTL	-55	125			5.0	22			6	1.1	1.7	.75	8		.45	3.00	40
NAND,8 INPUT	SYL	SG262	B	TTL	0	75			5.0	22			9	1.1	1.7	.75	8		.45	3.00	40
NAND,8 INPUT	SYL	SG263	B	TTL	0	75			5.0	22			5	1.1	1.7	.75	8		.45	3.00	40
NAND,8 INPUT	SYL	SG60	B	TTL	-55	125			5.0	15			# 15	1.20	1.70	.800	12	20	.40	3.20	40
NAND,8 INPUT	SYL	SG61	B	TTL	-55	125			5.0	15			# 7	1.20	1.70	.800	12	20	.40	3.20	40
NAND,8 INPUT	SYL	SG62	B	TTL	0	75			5.0	15			# 12	1.20	1.80	.800	39	20	.40	3.10	40
NAND,8 INPUT	SYL	SG63	B	TTL	0	75			5.0	7			# 6	1.20	1.80	.800	40	20	.40	3.10	40
NAND,8 INPUT	TI	SN5430	A	TTL	-55	125			5.0	10			* 10	.90	2.20	.400	15		.40	2.60	48
NAND,8 INPUT	TI	SN7430	F	TTL	0	70			5.0		15	5	* 10	.80	2.00	.400	13		.40	2.40	48,76
NAND,8 INPUT	TRAN	TNG3011	B	TTL	-55	125			5.0		20	10	15	1.20	1.70	.700	* 18		.45	2.4	23,47
NAND,8 INPUT	TRAN	TNG3012	B	TTL	0	75			5.0		20	10	15	1.20	1.70	.700	* 18		.45	2.4	23,47
NAND,8 INPUT	TRAN	TNG3013	B	TTL	-55	125			5.0		20	10	7	1.20	1.70	.700	* 18		.45	2.4	23,47
NAND,8 INPUT	TRAN	TNG3014	B	TTL	0	75			5.0		20	10	7	1.20	1.70	.700	* 18		.45	2.4	23,47
NAND,8 INPUT	TRAN	TNG3041	B	TTL	-55	125			5.0		*30	*15	15	1.2	1.7	.700	* 10		.45	2.4	23,47
NAND,8 INPUT	TRAN	TNG3042	B	TTL	0	75			5.0		*30	*15	15	1.2	1.7	.700	* 10		.45	2.4	23,47
NAND,8 INPUT	TRAN	TNG3043	B	TTL	-55	125			5.0		*30	*15	7	1.2	1.7	.700	* 10		.45	2.4	23,47
NAND,8 INPUT	TRAN	TNG3044	B	TTL	0	75			5.0		*30	*15	7	1.2	1.7	.700	* 10		.45	2.4	23,47
NAND,8 INPUT	WMED	WM704	A	TTL	-55	125			5.0		12	22	15	.60	1.65	.250	50		.35	2.65	43,91
NAND,8 INPUT EXPANDABLE	RAY	RM224	A	DTL	-55	125			6.0	15			6	1.00	1.80		30		.25		21,53
NAND,8 INPUT EXPANDABLE	SW	SWG120	A	TTL	-55	125			5.0	15			15				16	20			49
NAND,8 INPUT EXPANDABLE	SW	SWG121	A	TTL	-55	125			5.0	15			7				16	20			49
NAND,8 INPUT EXPANDABLE	SW	SWG122	A	TTL	0	75			5.0	15			12				16	20			49
NAND,8 INPUT EXPANDABLE	SW	SWG123	A	TTL	0	75			5.0	15			6				16	20			49

CIRCUIT DESCRIPTION	MFR	MFRS PART NUMBER	TECH	TYPE OF LOGIC	OPER. TEMP. CENTGRDE		SUPPLY VOLTAGE VDC			SUPPLY POWER MILLIWATTS			FAN-OUT	INPUT THRESHOLD VOLTS		NOISE IMMUNITY VOLTS	DELAY NANO-SECS	OPER-ATING SPEED MCPS	OUTPUT LEVEL VOLTS		PACK-AGE TYPE
					MIN	MAX	NO. 3	NO. 2	NO. 1	AVE	ON	OFF		ZERO	ONE				ZERO	ONE	
NAND,8 INPUT EXPANDABLE	SYL	SG120	B	TTL	-55	125			5.0	15			# 15	1.20	1.70	.800	18	20	.40	3.20	40
NAND,8 INPUT EXPANDABLE	SYL	SG121	B	TTL	-55	125			5.0	15			# 7	1.20	1.70	.800	18	20	.40	3.20	40
NAND,8 INPUT EXPANDABLE	SYL	SG122	B	TTL	0	75			5.0	15			# 12	1.20	1.80	.800	18	20	.40	3.10	40
NAND,8 INPUT EXPANDABLE	SYL	SG123	B	TTL	0	75			5.0	15			# 6	1.20	1.80	.800	18	20	.40	3.10	40
NAND,8 INPUT EXPANDABLE	TRAN	TNG3051	B	TTL	-55	125			5.0		*30	*15	15	1.2	1.7	.700	* 18		.45	2.4	47
NAND,8 INPUT EXPANDABLE	TRAN	TNG3052	B	TTL	0	75			5.0		*30	*15	15	1.2	1.7	.700	* 18		.45	2.4	47
NAND,8 INPUT EXPANDABLE	TRAN	TNG3053	B	TTL	-55	125			5.0		*30	*15	7	1.2	1.7	.700	* 18		.45	2.4	47
NAND,8 INPUT EXPANDABLE	TRAN	TNG3054	B	TTL	0	75			5.0		*30	*15	7	1.2	1.7	.700	* 18		.45	2.4	47
NAND,8 INPUT EXPANDABLE	WMED	WC224	A	DTL	0	75			6.0	8			6	1.0	1.8		30		.45		21,43
NAND,8 INPUT EXPANDABLE	WMED	WM224	A	DTL	-55	125			6.0	7			6	1.00	1.80		35		.25		21,43
NAND,8 INPUT EXPANDABLE	WMED	WM234	A	DTL	-55	125			6.0	15	20	11	9	1.00	2.00	.550	19		.45	5.80	43
NOR/NAND/AND,5 INPUT EX	TI	SN531	F	DTL	-55	125			3.5	18			* 10	.30	1.70		25		.30	2.20	74
NOR/OR,DUAL 2-3 INPUT	TI	SN7000	F	RTL	0	70		1.2	-3.5	40							5			-.40	48,76
NOR/OR,DUAL 4 INPUT	RCA	CD2100	A	ECL	-55	125			-5.2	44			* 12	1.30	.95	.100	24		1.50	.85	82
NOR/OR,DUAL 4 INPUT	RCA	CD2150	A	ECL	10	60			-5.0	110			* 12	1.40	1.00	.150	7		1.60	.85	82
NOR/OR,DUAL 4 INPUT	RCA	CD2151	A	ECL	10	60			-5.0	88			* 12	1.40	1.00	.150	7		1.60	.85	82
NOR/OR,DUAL 4 INPUT	WMED	WS371	A	ECL	10	60			-5.0	115			* 15	1.63	.83		10		1.63	.83	37
NOR/OR,3 INPUT EX	MOTA	MC306	A	ECL	-55	125		-1.15	-5.2	35			* 26	1.30	1.00	.300	6		1.66	.70	13,50
NOR/OR,3 INPUT EX	MOTA	MC307	A	ECL	-55	125		-1.15	-5.2	35			* 26	1.30	1.00		6		1.66		13,50
NOR/OR,3 INPUT EX	MOTA	MC356	A	ECL	0	75		-1.15	-5.2	35			* 26				6		1.66	.70	13,50
NOR/OR,3 INPUT EX	MOTA	MC357	A	ECL	0	75		-1.15	-5.2	35			* 26				6		1.66	.70	13,50
NOR/OR,3 INPUT EX	SW	SW306	A	ECL	-55	125		-1.15	-5.2	35			26	1.30	1.0	.30	6		1.66	.70	13,50
NOR/OR,3 INPUT EX	SW	SW307	A	ECL	-55	125		-1.15	-5.2	35			26	1.30	1.0		6		1.66		13,50
NOR/OR,4 INPUT	FSC	FL91129	A	RTL	15	55			3.6	6			4				25				1
NOR/OR,4 INPUT	FSC	L924	A	RTL	15	55			3.6								* 30				1
NOR/OR,4 INPUT	FSC	MWL911	A	RTL	-55	125			3.0	4			4,3	.45	.75	.050	80		.30	.80	1,55
NOR/OR,4 INPUT	GME	134G	A	RTL	-55	125			3.0	4			4	.55	.75	.050	* 70		.50	.83	3
NOR/OR,4 INPUT	MOTA	MC911	A	RTL	-55	125			3.0	4			4	.45	.75	.050	80		.30	.80	4
NOR/OR,4 INPUT	NSC	NC1011	A	RTL	-55	125			3.0	4			4,3	.69		.540	12		.15		2
NOR/OR,4 INPUT	NSC	NC2011	A	RTL	0	100			3.0	4			4,3	.69		.540	12		.15		2
NOR/OR,4 INPUT	PHIL	PL911	A	RTL	-55	125			3.0	4			4,3	.45	.75	.050	* 80		.30	.80	1
NOR/OR,4 INPUT	PHIL	PL980	A	RTL	-55	125			4.0	3			5	.45	.82		25		.40		51
NOR/OR,4 INPUT	SPRG	US-0711	F	RTL	-55	125			3.0	4							* 80				57,62
NOR/OR,5 INPUT	MOTA	MC301	A	ECL	-55	125		-1.15	-5.2	35			* 26	1.30	1.00	.300	6		1.66	.70	13,50
NOR/OR,5 INPUT	MOTA	MC351	F	ECL	0	75		-1.15	-5.2	*50			* 25	1.35	.95	.100			1.45	.80	13,50
NOR/OR,5 INPUT	SW	SW301	A	ECL	-55	125		-1.15	-5.2	35			* 25	1.30	1.0	.30	6		1.66	.70	13,50
NOR/OR,8 INPUT	RCA	CD2152	A	ECL	10	60			-5.0	147			* 12	1.40	1.00	.150	7		1.60	.85	82
NOR/OR,8 INPUT	WMED	WS374	A	ECL	10	60			-5.0	115			* 15	1.63	.83		10		1.63	.83	37
NOR/OR,9 INPUT	VARO	8204	E	DTL	-55	125	6.0	3.0	-3.0	150			4	.50	3.50		* 20		.50	3.50	72
NOR,DUAL 2 INPUT	AMEL	L-INDUS	F	RTL	0	70			3.0		13	5		.55	.85		12		.30		5,6
NOR,DUAL 2 INPUT	AMEL	L-PREM	F	RTL	-55	125			3.0		13	5		.55	.80		12		.25		5,6
NOR,DUAL 2 INPUT	AMEL	L-STAND	F	RTL	-55	125			3.0		13	5		.56	.82		12		.30		5,6
NOR,DUAL 2 INPUT	FSC	CTL952	A	RTL	15	55		4.5	-2.0	55			* 12	.85	1.15	.250	12	30	.60	2.30	75
NOR,DUAL 2 INPUT	FSC	FL91029	A	RTL	15	55			3.6	6			4				25				1
NOR,DUAL 2 INPUT	FSC	FL91429	A	RTL	15	55			3.6	40			16				10				1
NOR,DUAL 2 INPUT	FSC	L914	A	RTL	-55	125			3.0		38	10	5	.56	.82	.260	12		.30	1.45	1,55
NOR,DUAL 2 INPUT	FSC	L914C	A	RTL	0	100			3.0		38	10	5	.55	.84	.150	12		.40	1.45	1,55
NOR,DUAL 2 INPUT	FSC	MWL910	A	RTL	-55	125			3.0	2			4	.45	.75	.050	45		.30	.80	1,55
NOR,DUAL 2 INPUT	GME	134D2	A	RTL	-55	125			3.0	4			4	.55	.75	.050	40		.50	.83	3,70

CIRCUIT DESCRIPTION	MFR	MFRS PART NUMBER	TECH	TYPE OF LOGIC	OPER. TEMP. CENTGRDE		SUPPLY VOLTAGE VDC			SUPPLY POWER MILLIWATTS			FAN-OUT	INPUT THRESHOLD VOLTS		NOISE IMMUNITY VOLTS	DELAY NANO-SECS	OPERATING SPEED MCPS	OUTPUT LEVEL VOLTS		PACKAGE TYPE
					MIN	MAX	NO. 3	NO. 2	NO. 1	AVE	ON	OFF		ZERO	ONE				ZERO	ONE	
NOR,DUAL 2 INPUT	MOTA	MC309	A	ECL	-55	125		-1.15	-5.2	49			* 26				6		1.66	.70	13,50
NOR,DUAL 2 INPUT	MOTA	MC310	A	ECL	-55	125		-1.15	-5.2	49			* 26				6		1.66	.70	13,50
NOR,DUAL 2 INPUT	MOTA	MC311	A	ECL	-55	125		-1.15	-5.2	49			* 26				6		1.66		13,50
NOR,DUAL 2 INPUT	MOTA	MC359	A	ECL	0	75		-1.15	-5.2	49			* 26				6		1.66	.70	13,50
NOR,DUAL 2 INPUT	MOTA	MC360	A	ECL	0	75		-1.15	-5.2	49			* 26				6		1.66	.70	13,50
NOR,DUAL 2 INPUT	MOTA	MC361	A	ECL	0	75		-1.15	-5.2	49			* 26				6		1.66		13,50
NOR,DUAL 2 INPUT	MOTA	MC814	F	RTL	0	100			3.0		19	5	5	.55	.84		* 24		.40	.84	4
NOR,DUAL 2 INPUT	MOTA	MC910	A	RTL	-55	125			3.0	4			4	.45	.75	.050	45		.30	.80	4
NOR,DUAL 2 INPUT	MOTA	MC914	F	RTL	-55	125			3.0		19	5	5	.56	.82	.020	* 24		.30	.84	4
NOR,DUAL 2 INPUT	NSC	NB1014	A	RTL	-55	125			3.0	*54			13	.69		.540	12		.15		2
NOR,DUAL 2 INPUT	NSC	NB2014	A	RTL	0	100			3.0	*54			13	.69		.540	12		.15		2
NOR,DUAL 2 INPUT	NSC	NC1010	A	RTL	-55	125			3.0	4			13	.69		.540	12		.15		2
NOR,DUAL 2 INPUT	NSC	NC2010	A	RTL	0	100			3.0	4			13	.69		.540	12		.15		2
NOR,DUAL 2 INPUT	PHIL	PL910	A	RTL	-55	125			3.0	4			4	.45	.75	.050	40		.30	.80	1
NOR,DUAL 2 INPUT	PHIL	PL914	A	RTL	-55	125			3.0		19	5	5	.56	.82		12		.30		1
NOR,DUAL 2 INPUT	PHIL	PL9609	A	RTL	-55	125			3.0	10							* 80				
NOR,DUAL 2 INPUT	PHIL	PL977	A	RTL	-55	125			4.0	3			5	.45	.82		11		.40		51
NOR,DUAL 2 INPUT	SPER	914	A	RTL	-55	125			3.0		38	10	5	.56	.82		12		.30		1,64
NOR,DUAL 2 INPUT	SPER	925	A	RTL	-55	125			3.0		38	10	5	.56	.82		12		.30		1,64
NOR,DUAL 2 INPUT	SPRG	US-0106	F	RCTL	-55	125			3.0		4		25,5								57,62
NOR,DUAL 2 INPUT	SPRG	US-0710	F	RTL	-55	125			3.0	4							40				57,62
NOR,DUAL 2 INPUT	SW	SW309	A	ECL	-55	125		-1.15	-5.2	49			* 26				6		1.66	.70	13,50
NOR,DUAL 2 INPUT	SW	SW310	A	ECL	-55	125			-5.2	49			* 26				6		1.66	.70	13,50
NOR,DUAL 2 INPUT	SW	SW311	A	ECL	-55	125			-5.2	49			* 26				6		1.66		13,50
NOR,DUAL 2 INPUT	TI	SN731	A	RTL	-55	125			3.0	2			4				35				1,58
NOR,DUAL 2 INPUT EX	SIGN	LU316	A		10	55			4.5	18			12	1.40	2.50	.800	40		.60	3.30	12
NOR,DUAL 2 INPUT EX	SIGN	SU316	A	TTL	-20	85			4.5	18			12	1.40	2.70	.600	30		.60	3.30	12,52
NOR,DUAL 2-3 INPUT	GI	MEM900	K														100				18,82
NOR,DUAL 3 INPUT	AMEL	M-INDUS	F	RTL	0	70			3.0		13	5		.55	.85	.250	12		.30	.22	14
NOR,DUAL 3 INPUT	AMEL	M-PREM	F	RTL	-55	125			3.0		13	5		.55	.80	.300	12		.25	.30	14
NOR,DUAL 3 INPUT	AMEL	M-STAND	F	RTL	-55	125			3.0		13	5		.56	.82	.260	12		.30	.25	14
NOR,DUAL 3 INPUT	AMEL	N-INDUS	F	RTL	0	70			3.0		13	10	5	.55	.85		16		.30		14
NOR,DUAL 3 INPUT	AMEL	N-PREM	F	RTL	-55	125			3.0		13	10	10	.55	.80		12		.25		14
NOR,DUAL 3 INPUT	AMEL	N-STAND	F	RTL	-55	125			3.0		13	10	6	.56	.82		12		.30		14
NOR,DUAL 3 INPUT	FSC	FL91529	A	RTL	15	55			3.6	40			16				10				11
NOR,DUAL 3 INPUT	FSC	L915	A	RTL	-55	125			3.0		38	10	5	.55	.84	.150	12		.40	1.45	1,55
NOR,DUAL 3 INPUT	FSC	L915C	A	RTL	0	100			3.0		38	10	5	.55	.84	.150	12		.40	1.45	1,55
NOR,DUAL 3 INPUT	GI	MEM522	K						-28.0	25				8.00	3.00	2.0	250		10.0	.20	
NOR,DUAL 3 INPUT	GI	PC14	H	DTL	-55	125	12.0	4.2	-3.0				5,4				8	12	.30	5.00	90
NOR,DUAL 3 INPUT	GME	134D3	A	RTL	-55	125			3.0	4			4	.55	.75	.050	40		.50	.83	17,59
NOR,DUAL 3 INPUT	MOTA	MC312	F	ECL	-55	125		-1.15	-5.2	63			* 26				6		1.66	.70	13,50
NOR,DUAL 3 INPUT	MOTA	MC362	F	ECL	0	70		-1.15	-5.2	84			25	1.35	.95	.100			1.45	.80	26,49
NOR,DUAL 3 INPUT	MOTA	MC815	F	RTL	0	100			3.0		19	5	5	.55	.84		* 24		.40	.84	13
NOR,DUAL 3 INPUT	MOTA	MC915	F	RTL	-55	125			3.0		19	5	5	.56	.82	.020	* 24		.30	.84	13
NOR,DUAL 3 INPUT	MOTA	MC918	A	RTL	-55	125			3.0	4			4	.45	.75	.050	45		.30	.80	11
NOR,DUAL 3 INPUT	NSC	NB1015	A	RTL	-55	125			3.0	*54			13	.69			12		.15		12
NOR,DUAL 3 INPUT	NSC	NB2015	A	RTL	0	100			3.0	*54			13	.69			12		.15		12
NOR,DUAL 3 INPUT	PHIL	PL915	A	RTL	-55	125			3.0		19	5	5	.56	.82		12		.30		1
NOR,DUAL 3 INPUT	PHIL	PL939	A	RTL	-55	125			3.0	4			4	.45	.75		* 45		.30		19,51

CIRCUIT DESCRIPTION	MFR	MFRS PART NUMBER	TECH	TYPE OF LOGIC	OPER. TEMP. CENTGRDE MIN	OPER. TEMP. CENTGRDE MAX	SUPPLY VOLTAGE VDC NO. 3	SUPPLY VOLTAGE VDC NO. 2	SUPPLY VOLTAGE VDC NO. 1	SUPPLY POWER MILLIWATTS AVE	SUPPLY POWER MILLIWATTS ON	SUPPLY POWER MILLIWATTS OFF	FAN-OUT	INPUT THRESHOLD VOLTS ZERO	INPUT THRESHOLD VOLTS ONE	NOISE IMMUNITY VOLTS	DELAY NANO-SECS	OPERATING SPEED MCPS	OUTPUT LEVEL VOLTS ZERO	OUTPUT LEVEL VOLTS ONE	PACKAGE TYPE
NOR,DUAL 3 INPUT	PHIL	PL978	A	RTL	-55	125			4.0	3			5	.45	.82		11		.40		51
NOR,DUAL 3 INPUT	SIGN	LU315	A		10	55			4.5	18			12	1.40	2.50	.800	40		.60	3.30	12
NOR,DUAL 3 INPUT	SIGN	SU315	A	TTL	-20	85			4.5	18			12	1.40	2.70	.600	30		.60	3.30	12,52
NOR,DUAL 3 INPUT	SPER	915	A	RTL	-55	125			3.0		38	10	5	.56	.82		12		.30		1,64
NOR,DUAL 3 INPUT	SPRG	US-0104	F	RCTL	-55	125			3.0	6			5	.46	1.16		130		.46	1.16	57,62
NOR,DUAL 3 INPUT	TI	SN514	F	RCTL	-55	125			3.0		2		5	.46	1.16		130		.46	1.16	58
NOR,DUAL 3 INPUT EX	PHIL	PL9603	A	RTL	-55	125			3.0				4	.49	.82	.06	8		.35	.88	
NOR,QUAD 2 INPUT	AMEL	Q-INDUS	F	RTL	0	70			3.0		52	20	5	.55	.85		16		.30		24
NOR,QUAD 2 INPUT	AMEL	Q-PREM	F	RTL	-55	125			3.0		52	20	10	.55	.80		12		.25		24
NOR,QUAD 2 INPUT	AMEL	Q-STAND	F	RTL	-55	125			3.0		52	20	6	.56	.82		12		.30		24
NOR,QUAD 2 INPUT	PHIL	PL983	A	RTL	-55	125			3.0	3			5	.45	.80		* 50		.35		51
NOR,QUAD 2 INPUT	RCA	CD2101	A	ECL	-55	125			-5.2	30			* 12	1.30	.95	.100	24		1.50	.85	82
NOR,TRIPLE 2 INPUT	SPRG	US-0112	F	RCTL	-55	125			3.0	4			5								57,62
NOR,TRIPLE 2 INPUT	SPRG	US-0113	F	RCTL	-55	125			3.0	4			10,5								57,62
NOR,TRIPLE 2 INPUT	TI	SN516	F	RCTL	-55	125			3.0		2		5	.46	1.16		150		.46	1.16	58
NOR,TRIPLE 2 INPUT	TI	SN5161	F	RCTL	-55	125			3.0		2		5	.46	1.16		68		.46	1.16	48
NOR,TRIPLE 2 INPUT	TI	SN5162	F	RCTL	-55	125			3.0		2		5	.46	1.16		68		.46	1.16	48
NOR,TRIPLE 3 INPUT	PHIL	PL985	A	RTL	-55	125			3.0	3			5	.45	.80		* 22		.35		41
NOR,2 INPUT	FSC	MWL909	A	RTL	-55	125			3.0	10			30	.45	.75	.050	80		.30	.80	1
NOR,2 INPUT	GME	134B	A	RTL	-55	125			3.0	10			30		.75		60		.50	.83	3
NOR,2 INPUT	MOTA	MC909	A	RTL	-55	125			3.0	10			30	.45	.75	.050	80		.30	.80	4
NOR,2 INPUT	NSC	NC1009	A	RTL	-55	125			3.0	10			30	.69	.77		* 24		.15		2
NOR,2 INPUT	NSC	NC2009	A	RTL	0	100			3.0	10			30	.69	.77		* 24		.15		2
NOR,2 INPUT	PHIL	PL909	A	RTL	-55	125			3.0	10			30	.45	.75	.050	80		.30	.80	1
NOR,2 INPUT	PHIL	PL976	A	RTL	-55	125			4.0	10			33	.45	.82		26		.40		1,51
NOR,2 INPUT	SPRG	US-0709	F	RTL	-55	125			3.0	10							80				57,62
NOR,2 INPUT	TI	SN730	A	RTL	-55	125			3.0	15			30				70				1,58
NOR,2 INPUT EXPANDABLE	PHIL	PL9602	A	RTL	-55	125			3.0				32,4	.49	.82	.06	10		.35	.88	
NOR,3 INPUT	AMEL	K-INDUS	F	RTL	0	70			3.0		14	5		.55	.85		12		.30		5,6
NOR,3 INPUT	AMEL	K-PREM	F	RTL	-55	125			3.0		14	5		.55	.80		12		.25		5,6
NOR,3 INPUT	AMEL	K-STAND	F	RTL	-55	125			3.0		14	5		.56	.82		12		.30		5,6
NOR,3 INPUT	FSC	FL90329	A	RTL	15	55			3.6	20			16				10				1
NOR,3 INPUT	FSC	L903	A	RTL	-55	125			3.0		19	5	5	.60	.90	.300	12		.30	1.45	1,55
NOR,3 INPUT	FSC	L903C	A	RTL	0	100			3.0		19	5	5	.60	.90	.300	12		.30	1.45	1,55
NOR,3 INPUT	GI	MEM503	K						-28.0	40				8.00	2.00	1.8			10.0	.20	
NOR,3 INPUT	MOTA	MC803	F	RTL	0	100			3.0		19	5	5	.55	.84		* 24		.40	.84	4
NOR,3 INPUT	MOTA	MC903	F	RTL	-55	125			3.0		19	5	5	.56	.82	.020	* 24		.30	.84	4
NOR,3 INPUT	NSC	NB1003	A	RTL	-55	125			3.0	*27			13	.69			12		.15		2
NOR,3 INPUT	NSC	NB2003	A	RTL	0	100			3.0	*27			13	.69			12		.15		2
NOR,3 INPUT	PHIL	PL903	A	RTL	-55	125			3.0		19	5	5	.56	.82		12		.30		1
NOR,3 INPUT EXPANDABLE	INTX	GBXXXXX	L	RTL	-55	125			*12.0				15,4					* 5			78
NOR,4 INPUT	AMEL	J-INDUS	F	RTL	0	70			3.0		16	5		.55	.85		12		.30		5,6
NOR,4 INPUT	AMEL	J-PREM	F	RTL	-55	125			3.0		16	5		.55	.80		12		.25		5,6
NOR,4 INPUT	AMEL	J-STAND	F	RTL	-55	125			3.0		16	5		.56	.82		12		.30		5,6
NOR,4 INPUT	FSC	L907	A	RTL	-55	125			3.0		19	5	5	.60	.90	.300	12		.30	1.45	1,55
NOR,4 INPUT	FSC	L907C	A	RTL	0	100			3.0		19	5	5	.60	.90	.300	12		.30	1.45	1,55
NOR,4 INPUT	MOTA	MC807	F	RTL	0	100			3.0		19	5	5	.55	.84		* 24		.40	.84	4
NOR,4 INPUT	MOTA	MC907	F	RTL	-55	125			3.0		19	5	5	.56	.82	.020	* 24		.30	.84	4
NOR,4 INPUT	NSC	NB1007	A	RTL	-55	125			3.0	*27			13	.69			12		.15		2

CIRCUIT DESCRIPTION	MFR	MFRS PART NUMBER	TECH	TYPE OF LOGIC	OPER. TEMP. CENTGRDE MIN	OPER. TEMP. CENTGRDE MAX	SUPPLY VOLTAGE VDC NO. 3	SUPPLY VOLTAGE VDC NO. 2	SUPPLY VOLTAGE VDC NO. 1	SUPPLY POWER MILLIWATTS AVE	SUPPLY POWER MILLIWATTS ON	SUPPLY POWER MILLIWATTS OFF	FAN-OUT	INPUT THRESHOLD VOLTS ZERO	INPUT THRESHOLD VOLTS ONE	NOISE IMMUNITY VOLTS	DELAY NANO-SECS	OPERATING SPEED MCPS	OUTPUT LEVEL VOLTS ZERO	OUTPUT LEVEL VOLTS ONE	PACKAGE TYPE
NOR,4 INPUT	NSC	NB2007	A	RTL	0	100			3.0	*27			13	.69			12		.15		2
NOR,4 INPUT	PHIL	PL907	A	RTL	-55	125			3.0		19	5	5	.56	.82		12		.30		1
NOR,4 INPUT	SPRG	US-0114	F	RCTL	-55	125			3.0	8			* 5								57,62
NOR,4 INPUT	SPRG	US-0115	F	RCTL	-55	125			3.0	8			* 5								57,62
NOR,4 INPUT	TI	SN733	A	RTL	-55	125			3.0	4			4,3				* 70				1,58
NOR,4 INPUT	VARO	8102	E	RTL	-55	100		20.0	-6.0												72
NOR,4 INPUT EXPANDABLE	GI	NC10	H	DTL	-55	125	12.0	4.2	-3.0				5,4				8	12	.30	5.00	16
NOR,5 INPUT	AMEL	G-INDUS	F	RTL	0	70			3.0		14	5		.55	.85		13		.30		5,6
NOR,5 INPUT	AMEL	G-PREM	F	RTL	-55	125			3.0		14	5		.55	.80		13		.25		5,6
NOR,5 INPUT	AMEL	G-STAND	F	RTL	-55	125			3.0		14	5		.56	.82		13		.30		5,6
NOR,6 INPUT	NSC	NB1017	A	RTL	-55	125			3.0	*27			13				12		.15		12
NOR,6 INPUT	NSC	NB2017	A	RTL	0	100			3.0	*27			13				12		.15		12
NOR,6 INPUT	SPRG	US-0102	F	RCTL	-55	125			3.0	2			5	.46	1.16		150		.46	1.16	57,62
NOR,6 INPUT	SPRG	US-0103	F	RCTL	-55	125			3.0	2			25,5	.46	1.16		175		.46	1.86	57,62
NOR,6 INPUT	TI	SN512	F	RCTL	-55	125			3.0		2		5	.46	1.16		150		.46	1.16	58
NOR,6 INPUT	TI	SN513	F	RCTL	-55	125			3.0		2		25,5	.46	1.16		175		.46	1.86	58
NOR,6 INPUT EXPANDABLE	GI	PC10	H	DTL	-55	125	12.0	4.2	-3.0				5,4				8	12	.30	5.00	90
NOR,7 INPUT	SIGN	LU314	A		10	55			4.5	18			12	1.40	2.50	.800	40		.60	3.30	12
NOR,7 INPUT	SIGN	SU314	A	TTL	-20	85			4.5	18			12	1.40	2.70	.600	30		.60	3.30	12,52
OR-NAND,DUAL 2-2 INPUT	GME	PL4601	K		-55	125		-12.0	-24.0	*20				3.00	9.00	1.000	800	.100	2.00	10.0	45,77
OR/NOR,DUAL 2-3 INPUT	TI	SN7000	F	RTL	0	70		1.2	-3.5	40							5			-.40	48,76
OR/NOR,DUAL 4 INPUT	RCA	CD2100	A	ECL	-55	125			-5.2	44			* 12	1.30	.95	.100	24		1.50	.85	82
OR/NOR,DUAL 4 INPUT	RCA	CD2150	A	ECL	10	60			-5.0	110			* 12	1.40	1.00	.150	7		1.60	.85	82
OR/NOR,DUAL 4 INPUT	RCA	CD2151	A	ECL	10	60			-5.0	88			* 12	1.40	1.00	.150	7		1.60	.85	82
OR/NOR,DUAL 4 INPUT	WMED	WS371	A	ECL	10	60			-5.0	115			* 15	1.63	.83		10		1.63	.83	37
OR/NOR,3 INPUT EX	MOTA	MC306	A	ECL	-55	125		-1.15	-5.2	35			* 26	1.30	1.00	.300	6		1.66	.70	13,50
OR/NOR,3 INPUT EX	MOTA	MC307	A	ECL	-55	125		-1.15	-5.2	35			* 26	1.30	1.00		6		1.66		13,50
OR/NOR,3 INPUT EX	MOTA	MC356	A	ECL	0	75		-1.15	-5.2	35			* 26				6		1.66	.70	13,50
OR/NOR,3 INPUT EX	MOTA	MC357	A	ECL	0	75		-1.15	-5.2	35			* 26				6		1.66	.70	13,50
OR/NOR,3 INPUT EX	SW	SW306	A	ECL	-55	125		-1.15	-5.2	35			26	1.30	1.0	.30	6		1.66	.70	13,50
OR/NOR,3 INPUT EX	SW	SW307	A	ECL	-55	125		-1.15	-5.2	35			26	1.30	1.0	.30	6		1.66		13,50
OR/NOR,4 INPUT	FSC	FL91129	A	RTL	15	55			3.6	6			4				25				1
OR/NOR,4 INPUT	FSC	L924	A	RTL	15	55			3.6								* 30				1
OR/NOR,4 INPUT	FSC	MWL911	A	RTL	-55	125			3.0	4			4,3	.45	.75	.050	80		.30	.80	1,55
OR/NOR,4 INPUT	GME	134G	A	RTL	-55	125			3.0	4			* 26	.55	.75	.050	* 70		.5	.83	3
OR/NOR,4 INPUT	MOTA	MC911	A	RTL	-55	125			3.0	4			4,3	.45	.75	.050	80		.30	.80	4
OR/NOR,4 INPUT	NSC	NC1011	A	RTL	-55	125			3.0	4			4,3	.69	.77		12		.15		2
OR/NOR,4 INPUT	NSC	NC2011	A	RTL	0	100			3.0	4			4,3	.69	.77		12		.15		2
OR/NOR,4 INPUT	PHIL	PL911	A	RTL	-55	125			3.0	4			4,3	.45	.75	.050	* 80		.30	.80	1
OR/NOR,4 INPUT	PHIL	PL980	A	RTL	-55	125			4.0	3			5	.45	.82		25		.40		51
OR/NOR,4 INPUT	SPRG	US-0711	F	RTL	-55	125			3.0	4							* 80				57,62
OR/NOR,5 INPUT	MOTA	MC301	A	ECL	-55	125		-1.15	-5.2	35			* 26	1.30	1.00	.300	6		1.66	.70	13,50
OR/NOR,5 INPUT	MOTA	MC351	F	ECL	0	75		-1.15	-5.2	*50			* 25	1.35	.95	.100			1.45	.80	13,50
OR/NOR,5 INPUT	SW	SW301	A	ECL	-55	125		-1.15	-5.2	35			* 25	1.30	1.0	.30	6		1.66	.70	13,50
OR/NOR,8 INPUT	RCA	CD2152	A	ECL	10	60			-5.0	147			* 12	1.40	1.00	.150	7		1.60	.85	82
OR/NOR,8 INPUT	WMED	WS374	A	ECL	10	60			-5.0	115			* 15	1.63	.83		10		1.63	.83	37
OR/NOR,9 INPUT	VARO	8204	E	DTL	-55	125	6.0	3.0	-3.0	150			4	.50	3.50		* 20		.50	3.50	72
OR,DUAL 2 INPUT EX	SIGN	LU331	A		10	55			4.5	36			* 12	1.40	2.50	.800	35		.60	3.30	12
OR,DUAL 2 INPUT EX	SIGN	SU331	A	TTL	-20	85			4.5	40			* 12	1.40	2.50	.800	35		.60	3.30	12

CIRCUIT DESCRIPTION	MFR	MFRS PART NUMBER	TECH	TYPE OF LOGIC	OPER. TEMP. CENTGRDE		SUPPLY VOLTAGE VDC			SUPPLY POWER MILLIWATTS			FAN-OUT	INPUT THRESHOLD VOLTS		NOISE IMMUNITY VOLTS	DELAY NANO-SECS	OPERATING SPEED MCPS	OUTPUT LEVEL VOLTS		PACKAGE TYPE
					MIN	MAX	NO. 3	NO. 2	NO. 1	AVE	ON	OFF		ZERO	ONE				ZERO	ONE	
OR,DUAL 3 INPUT	SIGN	LU332	A	TTL	10	55			4.5	36			* 12	1.40	2.50	.800	35		.60	3.30	12
OR,DUAL 3 INPUT	SIGN	SU332	A	TTL	-20	85			4.5	40			* 12	1.40	2.50	.800	35		.60	3.30	12
OR,DUAL 4 INPUT	CORN	0065	D	RTL	-55	125		1.8	-3.0	220			6				5				71
OR,3 INPUT EXPANDABLE	INTX	GGXXXXX	L	RTL	-55	125			*12.0				3					* 5			78
OR,4 INPUT	FSC	SH2101			-55	125			3.0					.45	.75		* 180		.22		1
PULSE SHAPER,W/C	VARO	8205	E	DTL	-55	125	6.0	3.0	-3.0	150			4,3	.50	3.50				.50	3.50	72
R-S	AMEL	F-INDUS	F	RTL	0	70			3.0	20			10	.55	.85		17		.30		5,6
R-S	AMEL	F-PREM	F	RTL	-55	125			3.0	20			10	.55	.80		13		.25		5,63
R-S	AMEL	F-STAND	F	RTL	-55	125			3.0	20			10	.56	.82		17		.30		5,63
R-S	FSC	L902	A	RTL	-55	125			3.0	22			4	.56	.82		14		.30		1
R-S	FSC	L902C	A	RTL	0	100			3.0	22			4	.55	.84		14		.40		1
R-S	GI	NCPC8	H		-55	125		12.0	4.2	*D2			5,3		3.00		25	20	.30	5.00	0,90
R-S	HOFF	HMC001	B	RCTL	-55	125			6.0	30			4				100		.20	4.00	12
R-S	MOTA	MC802	F	RTL	0	100			3.0	22			4	.55	.84		* 25		.40	.84	4
R-S	MOTA	MC902	F	RTL	-55	125			3.0	22			4	.56	.82	.020	* 25		.30	.84	4
R-S	NSC	NB1002	A	RTL	-55	125			3.0	22			12	.69	.77		* 25		.15		2
R-S	NSC	NB1023	A	RTL	-55	125			3.0	22			12	.69	.77		25		.15		2
R-S	NSC	NB2002	A	RTL	0	100			3.0	22			12	.69	.77		* 25		.15		2
R-S	NSC	NB2023	A	RTL	0	100			3.0	22			12	.69	.77		25		.15		2
R-S	PHIL	PL902	A	RTL	-55	125			3.0	22			4	.56	.82		14		.30		1
R-S	SW	SWF10	A	TTL	-55	125			5.0	30			15					20			27,49
R-S	SW	SWF11	A	TTL	-55	125			5.0	30			7					20			27,49
R-S	SW	SWF12	A	TTL	0	75			5.0	30			12					20			27,49
R-S	SW	SWF13	A	TTL	0	75			5.0	30			6					20			27,49
R-S	TI	SN337	A	DTL	0	65		6.0	- 3.0	90			12				250		.70		48
R-S,CLOCKED	GI	MEM529	K		-55	125			-28.0	*80				6.0	3.0	2.9		* 1	9.0	.10	18
R-S,CLOCKED	MEPC	640703	M	DTL	-55	125		6.0	-3.0				5				15	10			60
R-S,CLOCKED	VARO	8105	E	DTL	-55	125		20.0	-2.0	241			4					1	.50		72
R-S,CLOCKED OR DIR 2 PH	SYL	SF20	B	TTL	-55	125			5.0	*60			15	1.20	1.70	.800	* 25	20	.40	3.20	40
R-S,CLOCKED OR DIR 2 PH	SYL	SF21	B	TTL	-55	125			5.0	*60			7	1.20	1.70	.800	* 25	20	.40	3.20	40
R-S,CLOCKED OR DIR 2 PH	SYL	SF22	B	TTL	0	75			5.0	*60			12	1.20	1.80	.800	* 25	20	.40	3.10	40
R-S,CLOCKED OR DIR 2 PH	SYL	SF23	B	TTL	0	75			5.0	*60			6	1.20	1.80	.800	* 25	20	.40	3.10	40
R-S,CLOCKED OR DIR 2 PH	TRAN	TFF3011	B	TTL	-55	125			5.0	30			15	1.2	1.7	.700	* 18		.45	2.4	23,47
R-S,CLOCKED OR DIR 2 PH	TRAN	TFF3012	B	TTL	0	75			5.0		*30	*15	15	1.2	1.7	.700	* 18		.45	2.4	23,47
R-S,CLOCKED OR DIR 2 PH	TRAN	TFF3013	B	TTL	-55	125			5.0	30			7	1.2	1.7	.700	* 18		.45	2.4	23,47
R-S,CLOCKED OR DIR 2 PH	TRAN	TFF3014	B	TTL	0	75			5.0		*30	*15	7	1.2	1.7	.700	* 18		.45	2.4	23,47
R-S,CLOCKED OR DIR 2 PH	TRAN	TFF3015	B	TTL	-55	125			5.0		*30	*15	15	1.2	1.7	.700	* 18		.45	2.4	23,47
R-S,CLOCKED OR DIR 2 PH	TRAN	TFF3016	B	TTL	0	75			5.0		*30	*15	15	1.2	1.7	.700	* 18		.45	2.4	23,47
R-S,CLOCKED OR DIR 2 PH	TRAN	TFF3017	B	TTL	-55	125			5.0		*30	*15	7	1.2	1.7	.700	* 18		.45	2.4	23,47
R-S,CLOCKED OR DIR 2 PH	TRAN	TFF3018	B	TTL	0	75			5.0		*30	*15	7	1.2	1.7	.700	* 18		.45	2.4	23,47
R-S,CLOCKED OR DIRECT	FSC	SE124	A	DTL	-55	125			4.0	16							52	10	.50	2.50	11,55
R-S,CLOCKED OR DIRECT	GME	264B	A	DTL	-55	125		4.0	-2.0	16			* 8		2.50		25	25	.40		17,59
R-S,CLOCKED OR DIRECT	HOFF	HMC005	B	DTL	-55	125			4.0	16			16				45		.40	4.00	12
R-S,CLOCKED OR DIRECT	HOFF	HMC1003	B	DTL	0	80		4.0	-2.0	16			# 8		2.50		* 110	5	.60		12
R-S,CLOCKED OR DIRECT	INTX	FFXXXXX	L	RTL	-55	125			7.5	*92			4				17	* 5			78
R-S,CLOCKED OR DIRECT	INTX	FFXXXXX	L	RTL	-55	125			9.0	*65			4				16	* 5			78
R-S,CLOCKED OR DIRECT	MOTA	MC209	A	DTL	-55	125		4.0	-2.0	16			* 8	.60	2.00		* 88	10	.60	2.50	13,50
R-S,CLOCKED OR DIRECT	MOTA	MC652		DTL	0	75		10.0	-10.0	210			4				50		.72	9.6	26,49
R-S,CLOCKED OR DIRECT	MOTA	MC913	A	RTL	-55	125			3.0	12				.45	.75	.050			3.00	.80	4

CIRCUIT DESCRIPTION	MFR	MFRS PART NUMBER	TECH	TYPE OF LOGIC	OPER. TEMP. CENTGRDE MIN	MAX	SUPPLY VOLTAGE VDC NO. 3	NO. 2	NO. 1	SUPPLY POWER MILLIWATTS AVE	ON	OFF	FAN-OUT	INPUT THRESHOLD VOLTS ZERO	ONE	NOISE IMMUNITY VOLTS	DELAY NANO-SECS	OPER-ATING SPEED MCPS	OUTPUT LEVEL VOLTS ZERO	ONE	PACK-AGE TYPE
R-S,CLOCKED OR DIRECT	PHIL	PL9988	A	TTL	-55	125			3.0	E22			3	.42	.85	.19		5	.23	1.00	41
R-S,CLOCKED OR DIRECT	RAY	RM213	A	DTL	-55	125			6.0	*55			9	.70	1.60	.400	* 60	12	.30	3.50	21,53
R-S,CLOCKED OR DIRECT	SIGN	SE124	F	DTL	-55	125		4.0	-2.0	*26			* 8				* 40				12,56
R-S,CLOCKED OR DIRECT	SPRG	US-0110	A	RCTL	-55	125			3.0	2			4								57
R-S,CLOCKED OR DIRECT	SPRG	US-0111	F	RCTL	-55	125			3.0	3			20,4								57
R-S,CLOCKED OR DIRECT	SW	SWF20	A	TTL	-55	125			5.0	35			15					20			49
R-S,CLOCKED OR DIRECT	SW	SWF21	A	TTL	-55	125			5.0	35			7					20			49
R-S,CLOCKED OR DIRECT	SW	SWF22	A	TTL	0	75			5.0	35			12					20			49
R-S,CLOCKED OR DIRECT	SW	SWF23	A	TTL	0	75			5.0	35			6					20			49
R-S,CLOCKED OR DIRECT	TI	SN5101	F	RCTL	-55	125			3.0	2			4		1.15		* 500	.8	.22	1.15	58
R-S,CLOCKED OR DIRECT	TI	SN5111	F	RCTL	-55	125			3.0	2			20,4		1.15		* 500	.8	.22	1.50	58
R-S,CLOCKED OR DIRECT	VARO	8200	E	DTL	-55	125		6.0	3.0	165			4		3.00		10	20	.50	3.50	72
R-S,CLOCKED OR DIRECT	WMED	WC213	A	DTL	0	75			6.0	35			7	1.0	1.8		30	10	.45		21,43
R-S,CLOCKED OR DIRECT	WMED	WM213	A	DTL	-55	125			6.0	*55			9	.70	1.60	.400	* 60	11	.30	3.50	21,53
R-S,CLOCKED OR SET DIR	SPRG	US-0100	F	RCTL	-55	125			3.0	2			4		1.15		* 500	.800	.22	1.15	57
R-S,CLOCKED OR SET DIR	SPRG	US-0101	F	RCTL	-55	125			3.0	2			20,4		1.15		* 500	.800	.22	1.50	57
R-S,CLOCKED OR SET DIR	TI	SN510	F	RCTL	-55	125			3.0	2			4		1.15		* 500	.8	.22	1.15	58
R-S,CLOCKED OR SET DIR	TI	SN511	F	RCTL	-55	125			3.0	2			20,4		1.15		* 500	.8	.22	1.50	58
R-S,CLOCKED OR SET DIR	TI	SN5112	F	RCTL	-55	125			3.0	3			16,4	.40	1.15		430		.22	1.15	58
R-S,CLOCKED 2 PHASE	TRAN	TFF3031	B	TTL	15	55			5.0		*30	*15	7	1.0	2.0	.500	* 25		.50	2.5	1
R-S,DUAL	CORN	0067	D	RTL	0	70		1.8	-3.0	140			6				# 9	* 80			71
R-S,DUAL CLOCKED OR DIR	SIGN	SE424	A	DTL	-55	125			4.0	*14			* 7	.70	2.10	.400	* 150	9	.30	2.70	81
R-S,DUAL 2 INPUT AND	NSC	NB1019	A	RTL	-55	125			3.0	44			12	.69	.77		* 25		.15		2
R-S,DUAL 2 INPUT AND	NSC	NB2019	A	RTL	0	100			3.0	44			12	.69	.77		* 25		.15		2
R-S,SP CLCKD OR DIRECT	FSC	DTL950	A	DTL	-55	125			5.0	50			10				20				44
R-S,SP CLCKD OR DIRECT	FSC	FL95029	A	DTL	0	70			5.0	50			10				20				
R-S,SP CLCKD OR DIRECT	INTX	FFXXXXX	L	RTL	-55	125			7.5	*92			4				17	* 5			78
R-S,SP CLCKD OR DIRECT	SIGN	CS729	F	DTL	-55	125			4.0	*30			* 7				* 95		.35	3.10	81
R-S,SP CLCKD OR DIRECT	SW	SWF30	A	TTL	-55	125			5.0	30			15					12			27,49
R-S,SP CLCKD OR DIRECT	SW	SWF31	A	TTL	-55	125			5.0	30			7					12			27,49
R-S,SP CLCKD OR DIRECT	SW	SWF32	A	TTL	0	75			5.0	30			12					12			27,49
R-S,SP CLCKD OR DIRECT	SW	SWF33	A	TTL	0	75			5.0	30			6					12			27,49
R-S,SP CLCKD OR DIRECT	SYL	SF30	B	TTL	-55	125			5.0	30			15	1.2	1.7	.75		12	.45	3.00	40
R-S,SP CLCKD OR DIRECT	SYL	SF31	B	TTL	-55	125			5.0	30			7	1.2	1.7	.75		12	.45	3.00	40
R-S,SP CLCKD OR DIRECT	SYL	SF32	B	TTL	0	75			5.0	30			12	1.2	1.7	.75		12	.45	3.00	40
R-S,SP CLCKD OR DIRECT	SYL	SF33	B	TTL	0	75			5.0	30			6	1.2	1.7	.75		12	.45	3.00	40
R-S,SP CLCKD OR SET DIR	FSC	CS704	A	DTL	-55	125		4.0	-2.0	*26			* 8				* 40				11,55
R-S,SP CLCKD OR SET DIR	MOTA	MC260	F	DTL	0	75		4.0	-2.0	16							* 90		.55	2.50	13
R-S,SP CLCKD OR SET DIR	SIGN	CS704	A	DTL	-55	125		4.0	-2.0	*26			* 8				* 40				12,56
R-S,SPLIT CLOCKED	GI	PC13	H		-55	125		12.0	4.2	*D2			* 8		3.00				.30	5.00	90
R-S,SPLIT CLOCKED	VARO	8107	E	DTL	-55	125		20.0	-2.0	241			4					1	.50		72
R-S,TYPE D	FSC	MWL913	A	RTL	-55	125			3.0	12			3	.45	.75	.050	* 100		.30	.80	1
R-S,TYPE D	GME	134R	A	RTL	-55	125			3.0	10			3		.75		120		.50	.83	17,59
R-S,TYPE D	MOTA	MC259	F	DTL	0	75		4.0	-2.0	16				.55	2.00		* 90		.55	2.50	13
R-S,TYPE D	MOTA	MC913	F	RTL	-55	125			3.0	12				.45	.75	.050	* 100		.30	.80	4
R-S,TYPE D	PHIL	PL913	A	RTL	-55	125			3.0	12			3	.45	.75	.050	* 100		.30	.80	1
R-S,TYPE D	PHIL	PL984	A	RTL	-55	125			4.0	15			4	.45	.82		25		.40		51
R-S,TYPE D	SPRG	US-0713	F	RTL	-55	125			3.0	15							* 120				57,62
R-S,TYPE D	TRAN	TFF3512	B	TTL	0	75			5.0	150			15	1.2	1.8	.800		50	.40	3.0	47,75

CIRCUIT DESCRIPTION	MFR	MFRS PART NUMBER	TECH	TYPE OF LOGIC	OPER. TEMP. CENTGRDE		SUPPLY VOLTAGE VDC			SUPPLY POWER MILLIWATTS			FAN-OUT	INPUT THRESHOLD VOLTS		NOISE IMMUNITY VOLTS	DELAY NANO-SECS	OPERATING SPEED MCPS	OUTPUT LEVEL VOLTS		PACKAGE TYPE
					MIN	MAX	NO. 3	NO. 2	NO. 1	AVE	ON	OFF		ZERO	ONE				ZERO	ONE	
R-S,TYPE D	TRAN	TFF3514	B	TTL	0	75			5.0	150			7	1.2	1.8	.800		50	.40	3.C	47,75
R-S,2 INPUT NAND	MOTA	MC302	A	ECL	-55	125			-5.2	35			* 25				10		1.60	.70	13,50
R-S,2 INPUT NAND	MOTA	MC352	A	ECL	0	75			-5.2	35			* 25				10		1.60	.70	13,50
R-S,2 INPUT NAND	NSC	NB1018	A	RTL	-55	125			3.0	36			12	.69	.77		20		.15		2
R-S,2 INPUT NAND	NSC	NB2018	A	RTL	0	100			3.0	36			12	.69	.77		20		.15		2
R-S,2 INPUT NAND	SW	SW302	A	ECL	-55	125			-5.2	35			* 25				12		1.60	.70	13,50
R-S,2 INPUT OR	NSC	NB1020	A	RTL	-55	125			3.0	27			11	.69	.77		20		.15		12
R-S,2 INPUT OR	NSC	NB2020	A	RTL	0	100			3.0	27			11	.69	.77		20		.15		12
R-S,3 INPUT NAND	RAY	RM202	A	DTL	-55	125			6.0	15			10	1.00	1.80		32		.25		12,43
R-S,3 INPUT NAND	SYL	SF10	B	TTL	-55	125			5.0	*45			15	1.20	1.70	.800	* 25	20	.40	3.20	40
R-S,3 INPUT NAND	SYL	SF11	B	TTL	0	75			5.0	*45			7	1.20	1.70	.800	* 25	20	.40	3.20	40
R-S,3 INPUT NAND	SYL	SF12	B	TTL	0	75			5.0	*45			12	1.20	1.80	.800	* 25	20	.40	3.10	40
R-S,3 INPUT NAND	SYL	SF13	B	TTL	0	75			5.0	*45			6	1.20	1.80	.800	* 25	20	.40	3.10	40
R-S,3 INPUT NAND	WMED	WC202	A	DTL	0	75			6.0	8			6	1.0	1.8		30		.45		21,43
R-S,3 INPUT NAND	WMED	WM202	A	DTL	-55	125			6.0	15			10	1.00	1.80		32		.25		12,43
R-S,3 INPUT NAND EX	RAY	RM212	A	DTL	-55	125			6.0	15			10	1.00	1.80		32		.25		12,43
R-S,3 INPUT NAND EX	WMED	WC212	A	DTL	0	75			6.0	8			6	1.0	1.8		30		.45		21,43
R-S,3 INPUT NAND EX	WMED	WM212	A	DTL	-55	125			6.0	15			10	1.00	1.80		32		.25		12,43
R-S,4 INPUT NAND EX	RAD	RD208	C	DTL	-55	125			5.0		20	20	8				8		.40	4.00	42
R-S,4 INPUT NAND EX	RAD	RD308	C	DTL	-55	125			5.0		20	20	4				8		.40	4.00	42
R-S,4 INPUT NAND EX	RAD	RD508	C	DTL	0	75			5.0		20	20	7				8		.40	4.00	42
REGULATOR,-1.15 VDC	MOTA	MC304	A	ECL	-55	125			-5.2	*24			* 25								13,50
REGULATOR,-1.15 VDC	MOTA	MC354	A	ECL	0	75			-5.2	18			* 25								13,50
REGULATOR,-1.15 VDC	SW	SW304	A	ECL	-55	125			-5.2	18			* 25								13,50
REGULATOR,-12.0 VDC	GI	NCPC513	H		-55	125			-16.0	*D5											18,90
REGULATOR,-12.0 VDC	GI	PC503	H		-55	125			-16.0	*D5											93
REGULATOR,-24.0 VDC	GI	PC504	H		-55	125			-28.0	*D5											93
REGULATOR,-24.0 VDC	GI	PC514	H		-55	125			-28.0	*D5											93
REGULATOR,-6.0 VDC	GI	PC523	H		-55	125			-10.0	*D5											93
REGULATOR,12.0 VDC	GI	NCPC511	H		-55	125			16.0	*D5											18,90
REGULATOR,12.0 VDC	GI	PC501	H		-55	125			16.0	*D5											93
REGULATOR,24.0 VDC	GI	PC502	H		-55	125			28.0	*D5											93
REGULATOR,24.0 VDC	GI	PC512	H		-55	125			28.0	*D5											93
REGULATOR,5.0 VDC	GI	NCS675A	H		-55	125			11.0	*D5											93
REGULATOR,6.0 VDC	GI	PC521	H		-55	125			10.0	*D5											93
SCHMITT TRIGGER	GI	NCPC17	H	DTL	-55	125		12.0	4.2	*D2			9,8		1.20		25	5	.30	5.00	0,90
SCHMITT TRIGGER	INTX	STXXXXX	L	TRL	-55	125			*12.0	135			2		3.50		25	1.500			78
SHIFT REGISTER ELEMENT	AMEL	S-INDUS	F	RTL	0	70			3.0	50				.55	.85		* 50		.30		5,6
SHIFT REGISTER ELEMENT	AMEL	S-PREM	F	RTL	-55	125			3.0	50				.55	.8		* 32		.25		5,6
SHIFT REGISTER ELEMENT	AMEL	S-STAND	F	RTL	-55	125			3.0	50				.56	.82		* 40		.30		5,6
SHIFT REGISTER ELEMENT	FSC	FL90529	A	RTL	15	55			3.6	80			13				20				1
SHIFT REGISTER ELEMENT	FSC	L905	A	RTL	-55	125			3.0	53			5,4	.56	.82		* 22		.30		1,6
SHIFT REGISTER ELEMENT	FSC	L905C	A	RTL	0	100			3.0	53			5,4	.55	.84		* 22		.40		1,6
SHIFT REGISTER ELEMENT	FSC	L906	A	RTL	-55	125			3.0	36			4	.56	.82		22		.30		1,6
SHIFT REGISTER ELEMENT	FSC	L906C	A	RTL	0	100			3.0	36			4	.55	.84		22		.40		1,6
SHIFT REGISTER ELEMENT	MOTA	MC805	F	RTL	0	100			3.0	53			5,4	.55	.84		* 40		.40	.84	4
SHIFT REGISTER ELEMENT	MOTA	MC806	F	RTL	0	100			3.0	36			4	.55	.84		* 40		.40	.84	4
SHIFT REGISTER ELEMENT	MOTA	MC905	F	RTL	-55	125			3.0	53			5,4	.56	.82	.020	* 40		.30	.84	4
SHIFT REGISTER ELEMENT	MOTA	MC906	F	RTL	-55	125			3.0	36			4	.56	.82	.020	* 40		.30	.84	4

CIRCUIT DESCRIPTION	MFR	MFRS PART NUMBER	TECH	TYPE OF LOGIC	OPER. TEMP. CENTGRDE MIN	MAX	SUPPLY VOLTAGE VDC NO. 3	NO. 2	NO. 1	SUPPLY POWER MILLIWATTS AVE	ON	OFF	FAN-OUT	INPUT THRESHOLD VOLTS ZERO	ONE	NOISE IMMUNITY VOLTS	DELAY NANO-SECS	OPERATING SPEED MCPS	OUTPUT LEVEL VOLTS ZERO	ONE	PACKAGE TYPE
SHIFT REGISTER ELEMENT	NSC	NB1005	A	RTL	-55	125			3.0	53			13	.69	.77		20		.15		2
SHIFT REGISTER ELEMENT	NSC	NB2005	A	RTL	0	100			3.0	53			13	.69	.77		20		.15		2
SHIFT REGISTER ELEMENT	PHIL	PL905	A	RTL	-55	125			3.0	53			5,4	.56	.82		* 40		.30		1
SHIFT REGISTER ELEMENT	PHIL	PL906	A	RTL	-55	125			3.0	36			4	.56	.82		* 40		.30		1
SHIFT REGISTER,J-K	AMEL	R-INDUS	F	RTL	0	70			3.0	84			5	.55	.85		39		.30		24
SHIFT REGISTER,J-K	AMEL	R-PREM	F	RTL	-55	125			3.0	84			10	.55	.80		32		.25		24
SHIFT REGISTER,J-K	AMEL	R-STAND	F	RTL	-55	125			3.0	84			6	.56	.82		35		.30		24
SHIFT REGISTER,J-K	AMEL	T-INDUS	F	RTL	0	70			3.0	84			5	.55	.85		39		.30		14
SHIFT REGISTER,J-K	AMEL	T-PREM	F	RTL	-55	125			3.0	84			10	.55	.80		32		.25		14
SHIFT REGISTER,J-K	AMEL	T-STAND	F	RTL	-55	125			3.0	84			6	.56	.82		35		.30		14
SHIFT REGISTER,J-K	AMEL	U-INDUS	F	RTL	0	70			3.0	60			5	.55	.85		56		.30		5,6
SHIFT REGISTER,J-K	AMEL	U-PREM	F	RTL	-55	125			3.0	60			10	.55	.80		50		.25		5,6
SHIFT REGISTER,J-K	AMEL	U-STAND	F	RTL	-55	125			3.0	60			6	.56	.82		77		.30		5,6
SHIFT REGISTER,J-K 2 PH	AMEL	P-INDUS	F	RTL	0	70			3.0	84			10	.55	.85		39		.30		24
SHIFT REGISTER,J-K 2 PH	AMEL	P-PREM	F	RTL	-55	125			3.0	84			10	.55	.80		32		.25		24
SHIFT REGISTER,J-K 2 PH	AMEL	P-STAND	F	RTL	-55	125			3.0	84			10	.56	.82		35		.30		24
SHIFT REGISTER,R-S	TI	SN735	A	RTL	-55	125			3.0	15			3				70				58
SHIFT REGISTER,10-BIT	GI	MEM507	K					-12.0	-28.0					8.00	3.00	2.0		.500	10.0	.20	
SHIFT REGISTER,10-BIT	GI	MEM508	K					-12.0	-28.0					8.00	3.00	2.0		.500	10.0	.20	
SHIFT REGISTER,100-BIT	GME	PL5100	K		-55	125		-20.0	-27.0	250				8.00	4.00	1.000		* 1	9.00	3.00	17
SHIFT REGISTER,20-BIT	GI	MEM3020	K		-55	125			-26.0	150								1			16
SHIFT REGISTER,21-BIT	GI	MEM3021	K		-55	125			-28.0	150								*.500			16
SHIFT REGISTER,5-BIT	GI	MEM509	K					-12.0	-28.0					8.00	3.00	2.0		.500	10.0	.20	
SHIFT REGISTER,9-BIT	GME	PL4R01	K		-20	70		-24.0	-12.0					9.0	3.0	1.0		.100	10.0	2.0	88
SHIFT REGISTER,9-BIT	GME	PL4R02	K		-55	125		-12.0	-24.0	*75				9.00	3.00	1.000	800	.100	10.0	2.00	88
STEERING GATE,DUAL	GI	NCPC9	H		-55	125		12.0	4.2				* 5		3.00			20	.30	5.0	0,90
SWITCH,ANALOG 1 INPUT	GI	PC401	H	DTL	-55	125		45.0	28.0								50	*.200			90
SWITCH,ANALOG 2 INPUT	GI	PC402	H	DTL	-55	125		45.0	28.0								50	*.200			90
SWITCH,ANALOG 4 CHANNEL	GME	PL4S01	K		-55	125	10.0	-15.0	-30.0	150							*1000				45,77
SWITCH,DUAL ANALOG	GESP	4JPA345	A		-55	125		6.0	-3.0	*43							1000				
SWITCH,DUAL ANALOG	GESP	4JPA358	A		-55	125		6.0	-3.0	*52							1250				

LINEAR CIRCUITS

CIRCUIT DESCRIPTION	MFR	MFRS PART NUMBER	TECH	OPER. TEMP. CNTGRDE MIN	OPER. TEMP. CNTGRDE MAX	SUPPLY VOLTAGE VDC NO. 3	SUPPLY VOLTAGE VDC NO. 2	SUPPLY VOLTAGE VDC NO. 1	SUPPLY POWER MILLI-WATTS	IMPEDENCE IN-PUT KOHM	IMPEDENCE OUT-PUT OHMS	GAIN VOLT-AGE V/V	GAIN POW-ER DB	3 DB B.W. MCPS	N.F. DB	COM. MODE REJ. DB	DIFF OFF-SET MV	H.D. % MAX	OUTPUT SIG. SWING P-P VOLTS	OUTPUT SIG. POWER MILLI WATTS	PACK-AGE TYPE
AMPLIFIER,AUDIO	WMED	WS107	A	-55	125					250		2000		E .5				3.0		5000	53
AMPLIFIER,AUDIO	WMED	WM1108	A	-55	125			12.0		B 10		20		.1				3.0	5.0		53
AMPLIFIER,AUDIO	VARO	8502	E	-55	85			20.0	100	# 10	1000	200		.2							73
AMPLIFIER,AUDIO	GESP	12X2071	M	-55	125		25.0	-25.0		# 10	*700	* 850		E .4					16.8		15
AMPLIFIER,AUDIO	GESP	12X2072	M	-55	125		25.0	-25.0		# 10	D*16	* 700		E .4					12.6		15
AMPLIFIER,AUDIO	WMED	WC183	A	-55	75			1.5	C 135	40		400	C1.2					8.0		# 3	21,65
AMPLIFIER,AUDIO VF	GESP	4JPA113	A	-55	125			9.0	180	E 5	B 20		31	2.0				T1.5		50	
AMPLIFIER,AUDIO VF	GESP	4JPA114	F					6.0	75	.5	2000	B* 24		#1.0						45	2
AMPLIFIER,AUDIO VF	GESP	4JPA126	F					6.0	150	.5	1000	B* 24		#1.0						90	2
AMPLIFIER,AUDIO VF	MOTA	MC1524	A	-55	125		6.0	-6.0	18	8.6	E5.8	11.5	* 17	.8				3.0		1000	13
AMPLIFIER,DIFF	SPER	203	B	-55	125			18.0	*150	150	100	150		.8		80	7		6.5		64
AMPLIFIER,DIFF	AMEL	D13-000	F	-55	125		12.0	-12.0	96	40	BP 5	2000		.4		100	DS10		P#6.8		24,63
AMPLIFIER,DIFF	AMEL	D13-001	F	-55	125		12.0	-12.0	96	20	DP55	2000		.4		* 80	DS25		P#6.0		24,63
AMPLIFIER,DIFF	AMEL	D13-002	F	-25	85		12.0	-12.0	96	20	DP55	1500		.4		* 60	DS50		P#5.0		24,63
AMPLIFIER,DIFF	AMEL	A13-251	F	-55	125		12.0	-12.0	120	1000	400	20000		E .3		80	50		18.0		24
AMPLIFIER,DIFF	GESP	4JPA107	A	0	125		12.0	-12.0	120	750	100	3500		E1.0		100	8		# 20		
AMPLIFIER,DIFF	GESP	4JPA135	A	0	125		6.0	-6.0	30	1000	100	2000		E1.4		80	8		# 8		
AMPLIFIER,DIFF	FSC	A710	A	-55	125		12.0	-6.0	110		200	1500		20.0			5				1
AMPLIFIER,DIFF	FSC	A710C	A	0	70		12.0	-6.0	110		200	1200		20.0			8				1
AMPLIFIER,DIFF	GI	PC200	H	-55	125		12.0	-12.0	65	100	200	4500		E .2		80	5		*21.0		90
AMPLIFIER,DIFF	RCA	CA3000	A	-55	125		6.0	-6.0	30	P195	BP 8	P 40		.6		98	8	5.0	6.4		11
AMPLIFIER,DIFF	RCA	CA3001	A	-55	125		6.0	-6.0	80	50	70	P 80		16.0	5	70	T1.5		5.0		25
AMPLIFIER,DIFF	RCA	CA3002	A	-55	125		6.0	-6.0	55	100	70	P 160		11.0	4		T1.2		5.5		11
AMPLIFIER,DIFF	NORD	NM2002	F	-55	125			13.0	26			300		*1.0			10				
AMPLIFIER,DIFF	RCA	CA3004	A	-55	125		6.0	-6.0	26				# 10	D1.0		98	5				25
AMPLIFIER,DIFF	RCA	CA3005	A	-55	125		6.0	-6.0	26				# 14	D1.0	* 9	101	5				25
AMPLIFIER,DIFF	NORD	NM1005	F	-55	125		12.0	-6.0	162	3.2		18				70	4		16.0		
AMPLIFIER,DIFF	RCA	CA3006	A	-55	125		6.0	-6.0	26				# 14	D1.0	* 9	101	1				25
AMPLIFIER,DIFF	RCA	CA3007	A	-55	125		6.0	-6.0	30	4	60		22			77	5	E2.8			25
AMPLIFIER,DIFF	NORD	NM2007	F	-55	125			13.0	26			300		*1.0			20				
AMPLIFIER,DIFF	RCA	CA3008	A	-55	125		6.0	-6.0	30	14	200	1000		.3		94	5		6.7		25
AMPLIFIER,DIFF	GI	PC201	H	-55	125		12.0	-12.0		200	200	B#P 2		E .2		100	5		8.0		85
AMPLIFIER,DIFF	RCA	CA3010	A	-55	125		6.0	-6.0	30	14	200	1000		.3		94	5		6.7		82
AMPLIFIER,DIFF	NORD	NM2012	F	-55	125			13.0	26			300		*1.0			5				
AMPLIFIER,DIFF	PHIL	PA702	A	0	70		12.0	-6.0	80	20	200	2300		1.1		80	7		10.6		
AMPLIFIER,DIFF	NSC	NS7037	O	-60	100		10.0	-10.0	*500	5	4000	40		.8			10				2
AMPLIFIER,DIFF	SIGN	SE505	A	-55	125		4.0	-3.0	25	4		1800		1.0		100	4		4.3		13,50
AMPLIFIER,DIFF	SIGN	SE506	A				15.0	-15.0	160	200		17000		.3		100	5		22		
AMPLIFIER,DIFF	PHIL	PA710	A	-55	125		12.0	-6.0	110		200	1500					5				1,51
AMPLIFIER,DIFF	GI	PC210	K	-55	125		18.0	-18.0	200	90	50	P3200		1.5		80	3		14.0		93
AMPLIFIER,DIFF	PHIL	PA712		-55	125		6.0	-3.0	17	40	300	700		.8		80	5		5.4		1,51
AMPLIFIER,DIFF	GI	PC212	K	-55	125		12.0	-12.0	90	100	50	P1600		1.2		80	3		12.0		93
AMPLIFIER,DIFF	WMED	WS115	A	-55	125		12.0	-6.0	26	#300	9000	# 50		.2		80	7		13.0		43
AMPLIFIER,DIFF	SIGN	SE518	A				4.0	-2.0	70	2		500		8.0			5				
AMPLIFIER,DIFF	FSC	A702	A	-55	125		12.0	-6.0	70	25	200	2600		1.1		80	5		10.6		1,55
AMPLIFIER,DIFF	FSC	A702A	A	-55	125		12.0	-6.0	70	25	200	2600		.8		80	5		10.6		1,55
AMPLIFIER,DIFF	FSC	A702C	A	-25	100		12.0	-6.0	80	20	200	2300		1.1		80	15		10.6		1,55
AMPLIFIER,DIFF	TI	SN521	F	-20	85	10	6.0	-9.0	28	12	B 10	1250		E .5		60	DS20		# .5		58
AMPLIFIER,DIFF	TI	SN522	F	-20	85	10	6.0	-9.0	72	12	160	1250		E .5		60	DS20		# .5		58

CIRCUIT DESCRIPTION	MFR	MFRS PART NUMBER	TECH	OPER. TEMP. CNTGRDE MIN	MAX	SUPPLY VOLTAGE VDC NO. 3	NO. 2	NO. 1	SUPPLY POWER MILLI-WATTS	IMPEDENCE IN-PUT KOHM	OUT-PUT OHMS	GAIN VOLT-AGE V/V	POW-ER DB	3 DB B.W. MCPS	N.F. DB	COM. MODE REJ. DB	DIFF OFF-SET MV	H.D. % MAX	OUTPUT SIG. SWING P-P VOLTS	POWER MILLI WATTS	PACK-AGE TYPE
AMPLIFIER,DIFF	WMED	WS123	A	-55	125		12.0	-6.0	67	#150	*500	# 250		# .1		90	2		14.0		43
AMPLIFIER,DIFF	TI	SN523	F	-55	125		12.0	-12.0	90	10		4500		.1		90	12		26.0		48
AMPLIFIER,DIFF	TI	SN524	F	-55	125		12.0	-12.0	120	2000		1250	62	.1			T 12		15.0		58
AMPLIFIER,DIFF	TI	SN525	F	-55	125		12.0	-12.0	100	80	B 10	50000		.1		100	T 1		34.0		48
AMPLIFIER,DIFF	TI	SN526	F	-55	125		12.0	-12.0	100	2000	B 12	2400		.1		80	T 3		34.0		48
AMPLIFIER,DIFF	WMED	WS141	A	-55	125		6.0	-12.0	* 65	# 50		# 150		E#.5		80	10		#17.5		43
AMPLIFIER,DIFF	WMED	WS142	A	-55	125		6.0	-12.0	*232	# 20		# 150		# .1		80	15		17.5		43
AMPLIFIER,DIFF	WMED	WS143	A	-55	125	12.0	6.0	-12.0	* 72	# 10		#1000		E#.5		80	10		#17.5		43
AMPLIFIER,DIFF	WMED	WS144	A	-55	125	12.0	6.0	-12.0	*267	* 2		#1500		# .1		80	1	5.0	#17.5		43
AMPLIFIER,DIFF	GI	PC250	K	-55	85		12.0	-12.0		7 10		320		E .3		42	50				83
AMPLIFIER,DIFF	GI	PC251	K	-55	85		12.0	-12.0		7 10		320		E .3		42	50				83
AMPLIFIER,DIFF	TI	SN5510	F	-55	125		6.0	-6.0	165	3.5	50	200		40.0		60	3		4.0		58
AMPLIFIER,DIFF	MOTA	MC1519A	J	-55	125		12.0	-12.0	*300	2.6	DP27	4500		1.0		89	6		14.0		13
AMPLIFIER,DIFF	MOTA	MC1519B	J	-55	125		12.0	-12.0	*300	1.2	P48	180		8.0		86	6		10.0		13
AMPLIFIER,DIFF	MOTA	MC1525	J	-55	125		12.0	-12.0	*300	2	B*11	140		1.4		# 80	5		# 7.0		13
AMPLIFIER,DIFF	MOTA	MC1526	J	-55	125		12.0	-12.0	*300	60	B*11	65		.5		# 80	7		# 7.0		13
AMPLIFIER,DIFF	MOTA	MC1527	J	-55	125		12.0	-12.0	*300	2	B*11	140		1.4		# 80	5		# 7.0		13
AMPLIFIER,DIFF	MOTA	MC1528	J	-55	125		12.0	-12.0	*300	80	B*11	65		.3		# 80	7		# 7.0		13
AMPLIFIER,DIFF	MOTA	MC1530	A	-55	125		6.0	-6.0	110	20	25	5000		1.2		75	5		10.4		13
AMPLIFIER,DIFF	MOTA	MC1531	A	-55	125		6.0	-6.0	110	2000	25	3500		.4		75	10		10.4		13
AMPLIFIER,DIFF	WMED	WS161		-55	125		12.0	-12.0		300		2000		.5		83	10		#14.0		53
AMPLIFIER,DIFF	WMED	WS174	A	-55	125		12.0	-12.0	375	#100		50000		.5		# 60			*22.0		37
AMPLIFIER,DIFF	FSC	A709	A	-55	125		15.0	-15.0	80	400	150	45000		* .4		90	5		#20.0		1
AMPLIFIER,DIFF	FSC	A709C	A	0	70		15.0	-15.0	80	250	150	45000		* .4		90	8		#20.0		1
AMPLIFIER,DUAL DIFF	FSC	A711	A	-55	125		12.0	-6.0	65		200	1500		20.0			5				11
AMPLIFIER,DUAL DIFF	FSC	A711C	A	0	70		12.0	-6.0	65		200	1500		20.0			8				11
AMPLIFIER,RF-IF	PHIL	PA713		-55	125			6.0	21				11	D2.0	10						19
AMPLIFIER,RF-IF	WMED	WM1146	A	-55	125			12.0	48	A 82	1900		23	40.0	4				4.0		31
AMPLIFIER,RF-IF 90MC	PHIL	PA7601	A	-55	100		6.0	-6.0	180	A250	315		18	D1.0						1	
AMPLIFIER,SENSE	SIGN	SE500	A	-55	100			13.0				30		3.0			T2				12,52
AMPLIFIER,SENSE	TI	SN5500	F	-55	125		4.5	-4.5	*200	* .3							4				58
AMPLIFIER,SERVO	NORD	NM1003	R	-55	100			30.0	6000	10	500	500								8000	89
AMPLIFIER,SERVO	NORD	NM1008	R	-55	100			30.0	6000	10	300	200								8000	89
AMPLIFIER,SERVO	WMED	WM169						28.0		# 10											9
AMPLIFIER,UNITY GAIN	GESP	12X218	M	-25	125			25.0		#A10	D#15	E#9.9		.5							92
AMPLIFIER,VIDEO	AMEL	E13-401	J	-55	125		12.0	-6.0	120	E1.4	400	6		30.0					4.0		14
AMPLIFIER,VIDEO	AMEL	E13-511	A	-55	125			12.0	144	E5.2	520		24	50.0					7.0		5
AMPLIFIER,VIDEO	AMEL	E16-511	M	-55	125			12.0	144	C 52	520		24	45.0					4.0		5
AMPLIFIER,VIDEO	GESP	4JPA112	M					15.0	400	A 20	500	500	20						1.0		2
AMPLIFIER,VIDEO	GI	NCPC101	H	-55	125			6.0		E 12	500	100		20.0					4.5		0,90
AMPLIFIER,VIDEO	SIGN	SE501	A	-55	125			6.0	20	E 13	7.5	20		12.0	4				3.0		12,52
AMPLIFIER,VIDEO	WMED	WS112	A	-55	125			12.0	60			160		70.0							9
AMPLIFIER,VIDEO	PHIL	PA713		-55	125			6.0	21			7		55.0							19
AMPLIFIER,VIDEO VF	PHIL	PA7600	A	-55	125			6.0	84				51	18.0						E 25	
AMPLIFIER,400 CPS	GELM	7739750	M	-55	85		25.0	-25.0	150	20	10		24						30.0		86
FILTER,30 MCS	GELM	7736078	P	-20	85					.1	100		-3	9.0							86
OSCILLATOR,120 MCPS	GELM	7736134	M	-55	85			12.0	66												86
OSCILLATOR,16 MCPS	GELM	473104	M	-55	75			12.0	228		300								2.0		87
PREAMPLIFIER,READ	WMED	WS934	A	0	60		9.0	-9.0	41	20	100	* 32		1.0							43

CIRCUIT DESCRIPTION	MFR	MFRS PART NUMBER	TECH	OPER. TEMP. CNTGRDE		SUPPLY VOLTAGE VDC			SUPPLY POWER MILLI-WATTS	IMPEDENCE		GAIN		3 DB B.W. MCPS	N.F. DB	COM. MODE REJ. DB	DIFF OFF-SET MV	H.D. % MAX	OUTPUT SIG.		PACK-AGE TYPE
				MIN	MAX	NO. 3	NO. 2	NO. 1		IN-PUT KOHM	OUT-PUT OHMS	VOLT-AGE V/V	POW-ER DB						SWING P-P VOLTS	POWER MILLI WATTS	
PREAMPLIFIER, SERVO	WMED	WS167								E2.5	D 39	300		.2							9

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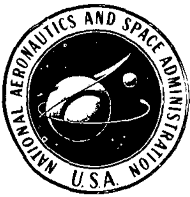

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ELECTRONICS RESEARCH CENTER
CAMBRIDGE, MASSACHUSETTS 02139

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TO: Distribution
Microelectronics Device Data Handbook
MPC 275-1 (Aug 1966 Edition)

FROM: CQ/Components Standards Branch

The enclosed Handbook has been recently completed by Arinc Research Corp. under NASA Contract NASw 1250.

The objective of the contract was to up-date and refine the Handbook in order to maximize its usefulness to those whose responsibility it is to select and utilize microelectronics in space hardware.

It is also our belief that we have advanced significantly toward this objective. You, as the user, however, will ultimately determine the value of this document. We, therefore, solicit your critical analysis so that future editions will more nearly satisfy your precise needs. Please forward your comments to the attention of Mr. Paul MacDonald, Code CQ.

C. W. Watt
C. W. Watt
Chief, Components Standards Branch
Qualifications & Standards Laboratory

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CASE FILE