High-speed quantum networking by ship

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Quantum communication will improve the security of cryptographic systems and decision-making algorithms[1–4], support secure client-server computation[5], and improve the sensitivity of scientific instruments[6–8]. As these applications consume quantum entanglement, a method for replenishing networked entanglement is essential[9–11]. Direct transmission of quantum signals over long distances is prevented by fibre attenuation and the no-cloning theorem[12]. This has motivated the development of quantum repeaters, which are designed to purify entanglement and extend its range[13–16]. Quantum repeaters have been demonstrated over short distances[17, 18], but an error-corrected repeater network with sufficient bandwidth over global distances will require new technology. In particular, no proposed hardware appears suitable for deployment along undersea cables, leaving the prospect of isolated metropolitan networks. Here we show that error-corrected quantum memories installed in cargo containers and carried by ship could provide a flexible and scalable connection between local networks, enabling low-latency, high-fidelity quantum communication across global distances. With recent demonstrations of quantum technology with sufficient fidelity to enable topological error correction[19], implementation of the necessary quantum memories is within reach, and effective bandwidth will increase with improvements in fabrication. Thus, our architecture provides a new approach to quantum networking that avoids many of the technological requirements of undersea quantum repeaters, providing an alternate path to a worldwide Quantum Internet [9–11].

Photons are traditionally proposed for the establishment of quantum entanglement between stationary quantum systems over moderate distances. Over longer distances, entanglement purification and entanglement swapping connecting a path comprised of shorter links will mitigate the exponential attenuation loss and effects of imperfect devices [13]. The repeat-until-success nature of these techniques allows the rate of entanglement generation to decrease polynomially with increasing distance, with the fidelity of entanglement limited by the accuracy of the quantum gates operating in the repeaters. Effective long range repeater networks requires incorporating fault-tolerant error correction methods, and numerous designs have been proposed [14–16, 20–22]. These designs do not offer bandwidth higher than about a MHz and require dense repeater arrays. A global network constructed in this way would require high-power, low-temperature quantum devices with active control deployed in very hostile environments. No known technology meets this requirement.

Despite the capabilities of modern classical networks, it is still routine to transfer classical information stored in removable media, an approach known as *sneakernet*. Here we adapt this approach to quantum information, introducing a new network architecture for the establishment of quantum entanglement over long distances based on the transport of error-corrected quantum memories [23]. Long-distance transport involves significant latency, but establishing entanglement involves no information exchange, meaning that this latency is irrelevant to network users—instead, the effective latency is the classical one-way communication time required for, for example, quantum teleportation [24]. Quantum memories may be transported to locations where entanglement is required or to intermediate locations to facilitate entanglement swapping between traditional repeater networks, enabling a complete network structure without the full deployment of physical links. Since trans-oceanic communication presents a particular challenge for quantum networking, we focus on the establishment of entanglement by ship.

Our architecture requires quantum memories with an effective coherence time of months, sufficient for transport along any traditional shipping channel. Since an error-corrected quantum memory is based on the same system architecture as a large-scale quantum computer, technology currently in development will fulfill our needs [25–27]. In particular, implementations of qubits based on several physical systems—including superconducting circuits and trapped ions—are nearing the accuracy threshold required for topological error correction to become effective [19]. Once this threshold is exceeded, it will be possible to arbitrarily lengthen the effective co-

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herence time of an error-corrected quantum memory with a poly-logarithmic qubit overhead. However, our architecture also requires quantum memories that are compatible with storage and transport in a shipping container, including a stable power source, ultra-high vacuum or refrigeration systems to maintain appropriate operating conditions, and classical-control infrastructure to perform error correction and decoding [28]. As yet, there are no implementations that are designed with this degree of portability in mind. Here, for concreteness, we focus on a potential implementation based on negatively-charged nitrogen vacancy (NV^-) centres in diamond, which may be integrated in dense arrays and are optically accessible at a temperature of 4 K[27, 29].

Each quantum memory consists of a two-dimensional array of optical cavities with a linear spacing of 2.5 mm, each containing a single NV^- centre comprising a spin-half N^{15} nucleus and a spin-one electron. Each nuclear spin represents a single qubit, and all operations (initialisation, readout, and interactions between neighbouring qubits) are achieved by hyperfine coupling to the electron spins and dipole-induced transparency in an external optical field. We assume that these operations are fixed to a 3.5 μs clock time and occur with an independent depolarising error rate of 0.1%, per gate. Coherent control of spins in diamond has already been demonstrated with an error rate below 1%, indicating that this target may be achievable in the near future [30–32]. Each quantum memory stores a single logical qubit encoded in the surface code, although other codes may also be suitable. The error-correction protocol involves the continuous execution of physical quantum circuits to determine the error syndrome. This information undergoes local classical processing to detect and correct errors introduced by decoherence, coupling inefficiency, and other sources, thereby preserving the state of the logical qubit. To determine the effective coherence time of the quantum memories, we undertook numerical simulations of the error-correction protocol for small arrays (see the Appendix). Extrapolating to large arrays, we find that quantum memories of 1600 qubits enable storage of logical qubits for two months with a logical error rate of 10^{-10}.

Quantum memories are installed in Twenty-foot Equivalent Unit (TEU) containers, the standard shipping unit with an internal volume of 40 m^3. We assume that 1 m^3 is occupied by quantum memories and the remaining 39 m^3 is reserved for power, refrigeration, and control infrastructure. Each of these units is the quantum equivalent of a memorystick. More efficient protocols may be achievable under different assumptions, but for simplicity we assume a single, dedicated Very Large Container Ship (VLCS)-class container ship with a capacity of 10^4 TEU. We consider a shipping channel between Japan and the United States, with freight terminals acting as primary network nodes for traditional repeater networks deployed in each country as shown in Figure 1. Allowing for local transport and maintenance, this requires a one-way transport time of 20 days [39].

Our network protocol ensures that the effective trans-oceanic bandwidth is limited only by the freight capacity and the transport time. The protocol is separated into three phases, which operate sequentially in each direction. In the first phase, each logical qubit is entangled with a stationary logical qubit at the origin to establish logical Bell pairs. The entangling operation is achieved with a lattice-surgery approach [33], requiring an external interface to each container to access a fraction of the physical qubits in every quantum memory (see the Appendix). The time required for this operation using the NV^- memory above is 1.7 ms per logical Bell pair, and operations may be parallelised if the interface allows simultaneous access to multiple quantum memories. In the second phase, one logical qubit in each logical Bell pair is transported from the origin to the terminus, undergoing continuous error correction. In the third phase, the logical qubits in the logical Bell pairs are entangled with additional logical qubits at the origin and the terminus and then measured. As before, these entangling operations are achieved with lattice surgery and with the the NV^- system described above can be achieved for a 1600 qubit memorystick in 1.7 ms (see the Appendix). This final phase consumes the entanglement between the origin and the terminus, either in service of an application or to connect distant points in a larger network. To enable continuous operation in both directions, ensuring that none of the freight capacity is used to transport unentangled quantum memories, our protocol requires an additional six containers for every one container in transport. We specify that the external interface to each container is sufficiently fast to allow logical qubits to be disentangled and re-entangled within the two-way transport time (see the Appendix).

Table 1 reports the effective trans-pacific bandwidth of the network architecture. Our results compare quantum memories based on NV^- centres in diamond to quantum memories based on a range of other qubit implementations [25–27, 34–38] illustrating the dependence of the bandwidth on the underlying physical parameters. Each implementation involves a unique set of technological challenges and our results are predicated on the development of portable architectures incorporating high-speed external interfaces to facilitate lattice-surgery operations between logical qubits. Nevertheless, bandwidth in excess of 1 THz is feasible under realistic physical assumptions, exceeding even the fastest proposals for traditional repeater networks. Our results assume a single container ship, but the total bandwidth scales linearly with the total freight capacity, allowing for incremental investment in infrastructure rather than the overhaul of thousands of kilometres of undersea cables. Furthermore, adding network nodes involves transport to additional locations rather than investment in wider area infrastructure, and can be done with minimal planning and only a few weeks lead time.

In addition to expanding the reach of traditional re-

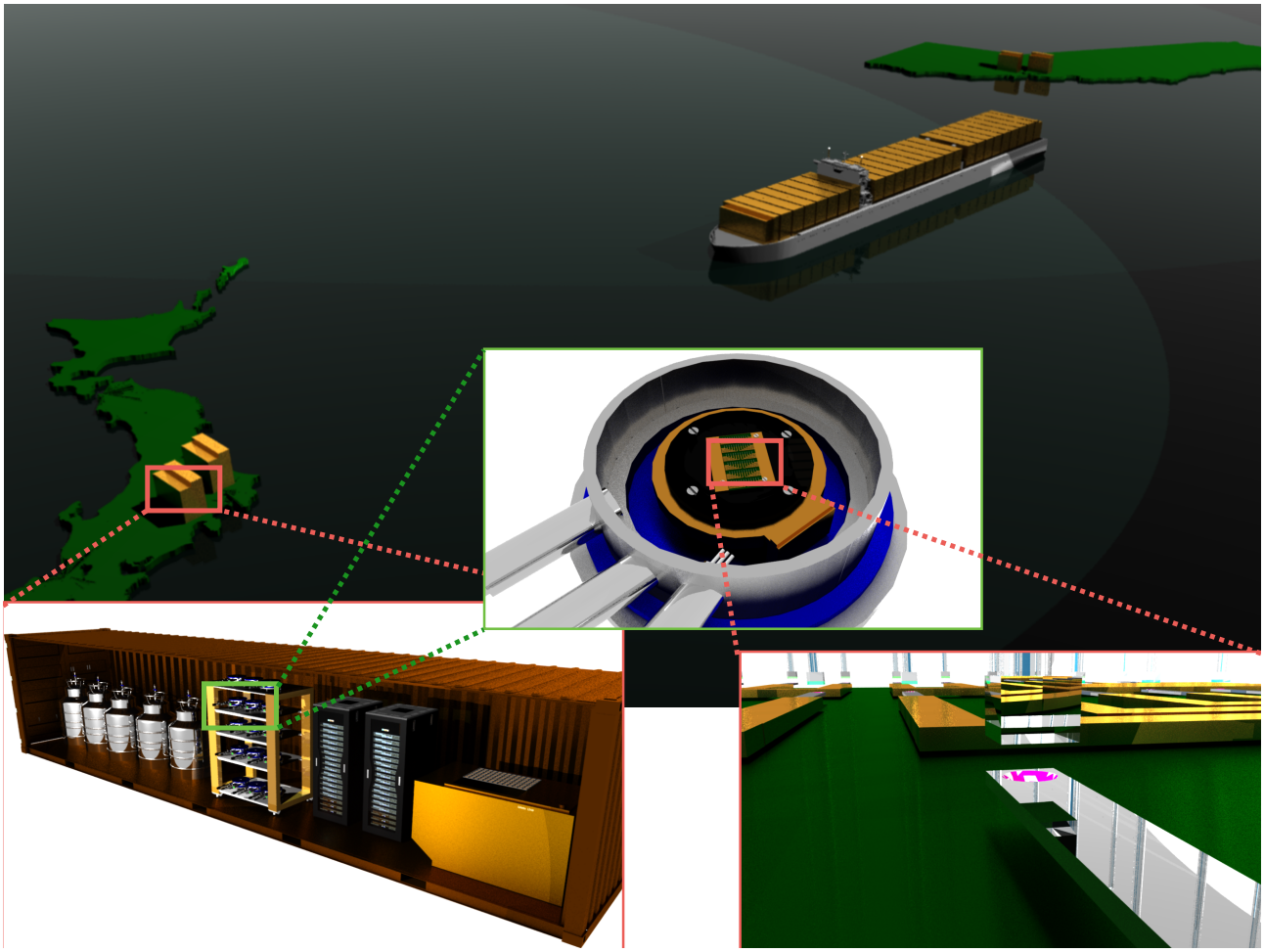

Figure 1: **Transport protocol for a single ship, Trans-Pacific, SneakerNet.** The transpacific connection shows the location of memory stick units both on shore in the U.S. and Japan and in transit of a VLCS-class ship. Each cargo container (memorystick) contains the actual memory units as well as any required control, cooling and power infrastructure. Each memory unit (for the specific hardware model of optically connected NV^- qubits [27]) consists of an array of diamond crystals within adjustable single sided cavities which are optically connected to perform individual qubit/qubit interactions. [29].

peater networks, our architecture may be used to hybridise networks with different operating regimes. For example, quantum memories may be used to interconvert between repeater networks with different networking protocols, qubit implementations, or operating rates. Quantum memories embedded in portable devices may allow mobile nodes to connect to static networks.

As quantum technology advances, a network architecture based on the transport of reliable quantum memories could enable the first fundamental tests of quantum mechanics over long distances and then increasingly sophisticated applications ranging from quantum cryptography to distributed quantum computing. Our architecture has the flexibility to service these applications as they develop, in addition to complementing traditional repeater networks as they are deployed. Eventually, once quantum computers are commonplace, entanglement will be the fungible resource that enables a vast range of distributed applications. The quantum sneakernet is the first architecture that could feasibly underpin an entanglement-based economy of this kind, connecting users of local quantum networks to a global Quantum Internet.

implementation	qubit pitch (m)	gate time (s)	physical error rate	Memorystick capacity	bandwidth (Hz)
NV^- (optical)	2.5×10^{-3}[29]	3.5×10^{-6}[27]	1×10^{-3}	1KEb	5.8×10^{1}
trapped ions	1.5×10^{-3}[35]	1.0×10^{-4}[34]	1×10^{-5}	5.4KEb	9.9×10^{2}
transmons	3.0×10^{-4}[38]	4.0×10^{-8}[19]	1×10^{-5}	435KEb	7.5×10^{4}
quantum dots	1.0×10^{-6}[25]	3.2×10^{-8}[25]	1×10^{-3}	11TEb	6.3×10^{10}
NV^-	3.0×10^{-7}[26]	1.0×10^{-3}[26]	1×10^{-3}	1.3PEb	7.5×10^{12}
silicon	2.0×10^{-7}[37]	5.0×10^{-8}[36]	1×10^{-3}	1.5PEb	8.7×10^{12}

TABLE I: **Effective trans-oceanic bandwidth of the network architecture.** Effective bandwidth achieved using a single VLCS-class container ship transporting error-corrected quantum memories between Japan and the United States, estimated for a range of qubit implementations for a fixed logical error rate of 10^{-10}. For several implementations, bandwidth exceeds the fastest proposals for traditional repeater networks. Memorystick capacities are estimated as $1/(40\times \text{ pitch})^3$ when utilising 1m^3 of space within each container. Figures for physical error rates are development targets for production-use hardware. They are chosen assuming more experimentally mature technologies can achieve a physical error lower than less mature technologies.

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Appendix

Capacity of a memory unit: Here we discuss the technical details of the quantum memory unit and how it uses topological planar codes to achieve a long memory. These codes are amenable to experimental implementation as they can be defined locally on an 2-dimensional nearest neighbour qubit array, have one of the highest fault-tolerant thresholds of any code and algorithmic optimisation and compilation can be detached from the underlying quantum hardware.

Illustrated in Figure 2 is the structure and performance of a memory unit. The device itself is a 2-dimensional nearest neighbour array of qubits designed to encode a single logical qubit of memory [Figure 2**a.**]. The logical Pauli operators are chains of physical X and Z operations that connect the top and bottom (logical X) or the left and right (logical Z) of the lattice. Through simulation, we numerically determine both the fault-tolerant threshold for the memory unit [Figure 2**c.**] and the expected failure rate as a function of QEC strength [Figure 2**d.**]. From the behaviour of the code for low values of the physical error rate, p, we can estimate the probability that a memory unit fails, P_L as a function of the distance of the topological planar code, d. For an operational device, we assume the error rate for each physical gate in the quantum memory is $p = 0.1\%$ (0.01%). We can perform a simple exponential fit to the data, to estimate the failure rate of the *logical* information, P_L, as a function of the code distance, $P_L = \alpha e^{-\beta d}$, where $\alpha \approx 0.312$ and $\beta \approx 1.112$ ($\alpha \approx 0.0085$ and $\beta \approx 3.6$ at $p = 0.01\%$). The total number of physical qubits in the memory unit is $N = (d+1)^2$ and the total time of a memory correction cycle is $T_{\rm corr} = 6td$, where t is the operational time of a *physical* quantum gate (initialisation, measurement or CNOT), the factor of 6 comes from the six elementary gates necessary to perform syndrome extraction in the topological code, and we require d rounds of error correction to correct for measurement errors.

The total memory time of the unit, $T_{\rm mem}$, is related to the failure probability of each error correction cycle, P_L, and the infidelity of the final entangled link, $1-F = P_{\rm link}$, where F is the link fidelity,

$$\begin{aligned} T_{\rm mem} &= \frac{\log(1-P_{\rm link})T_{\rm corr}}{\log(1-P_L)} \\ &\approx \frac{6t(\sqrt{N}-1)P_{\rm link}}{\alpha} e^{\beta(\sqrt{N}-1)} \end{aligned} \tag{1}$$

Figure 2b. plots the memory time for various values P_{link} for a device that has an $t = 10\mu$s physical gate time in the qubit array and the contour where the memory unit can maintain coherence for one year as a function of total number of physical qubits, N, and final link fidelity, P_{link}. Similar plots can be easily obtained from Eqn. 1 and since it is assumed that the physical system is at a physical error rate, $p = 0.1\%$ regardless of the intrinsic gate speed of the system, t, memory times will increase

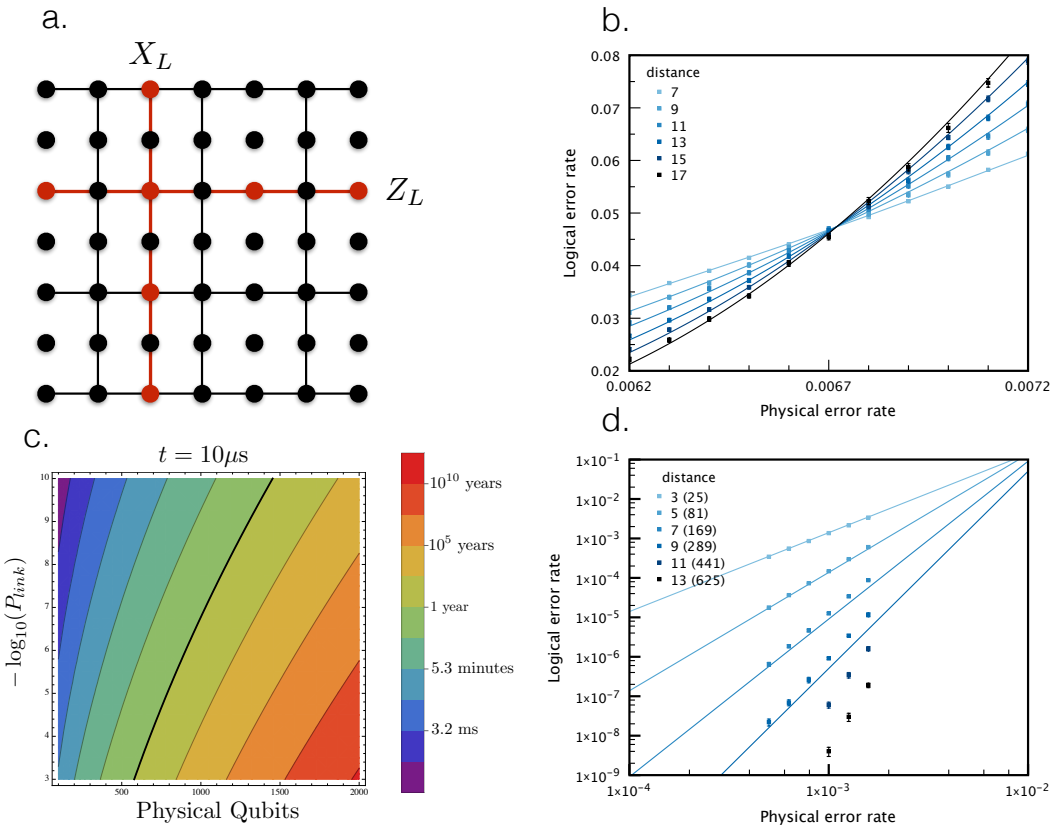

Figure 2: **Properties of the planar code.** The memory unit is a 2-dimensional nearest neighbour array of qubits encoded with the topological planar code [23]. In Figure **a.** Structure of the planar code with the single qubit X_L and Z_L operators illustrated (gridlines do not represent entanglement bonds). In Figure **b.** plots the memory time for various values P_{link} for a device that has an $t = 10\mu$s physical gate time in the qubit array and the contour where the memory unit can maintain coherence for one year. In Figure **c.** we show direct simulations of the fault-tolerant threshold of the planar code which lies at $p \approx 0.7\%$ under a standard error model. In Figure **d.** we show the logical error rate as a function of physical error rate for various different code distances. At a physical error rate, $p = 0.1\%$, we can estimate the logical failure rate, P_L, as a function of code distance, d.

with slower systems. i.e. ion trap computers will have a *longer* memory time that donor based system as we assume *both* technologies can achieve a $p = 0.1\%$ error rate on all fundamental gates. In the main text we assume a $N = 1600$ qubit memory unit. Taking $T_{\text{mem}} = 40$ days as our target memory time we find the link infidelity achievable is approximately $P_{\text{link}} \approx 10^{-10}$. 100

Lattice surgery operations. The planar code (and all toric code derivatives) allow logical two-qubit CNOT gates as a transversal operation. This would require individual CNOT gates to be applied between corresponding qubits in each memory unit. While fault-tolerant, this method of interaction may have implementation issues to ensure that all qubits in the 2D memory cell can be interacted with another cell. A different approach, called lattice surgery, partially solves this problem by realising a fault-tolerant CNOT gate between two memory units by only interacting qubits along an edge of each memory unit. 90

Lattice surgery works by merging two separate lattices, each containing a single logical qubit encoded in the planar code, into a single oblong lattice, then splitting up this single planar code again. The merging operation is done by matching the edges of two distinct logical qubits and measuring code stabilisers spanning the lattice cells. This effectively reduces a two qubit encoded system to a single encoded qubit. This merging takes the state $|\psi\rangle_L \otimes |\phi\rangle_L = (\alpha|0\rangle_L + \beta|1\rangle_L) \otimes (\alpha'|0\rangle_L + \beta'|1\rangle_L)$ to $\alpha|\phi\rangle_L + \beta|\bar{\phi}\rangle_L = \alpha'|\psi\rangle_L + \beta'|\bar{\psi}\rangle_L$, where $|\bar{A}\rangle = \sigma_x|A\rangle$. The measurement of the stabilisers to perform a merge must occur d times, where d is the effective code distance of each planar code. This is to protect against faulty qubit measurements for each stabiliser measurement. Given that the quantum circuit required to measure the stabilisers for the planar code requires 6 physical gates, the merge operation requires a time of $T = 6td$, for physical gate times t.

The splitting operation is executed by physically measuring the qubits along the merged edge to divide the single lattice back into two individual lattices. This effect of a split operation is to take the single logical state encoded

in the joint lattice, $\alpha |0\rangle_L + \beta |1\rangle_L$ to the two-qubit state, $\alpha |00\rangle_L + \beta |11\rangle_L$. Once again to protect against measurement errors, error correction of both lattices must be run for a total of d cycles, requiring a total time of $T = 6dt$ for the split operation.

Given these transformations, we can construct a Bell state between two encoded memory units by initialising a $d \times d$ lattice holding a logical qubit in one memory unit in the $|+\rangle_L$ state and a logical qubit in the other memory unit in the $|0\rangle_L$ state, merge the edges of the lattices across the optical interface between units to form a single state $|+\rangle_L$ in a $2d \times d$ lattice, and then split them again to create the state $(|00\rangle_L + |11\rangle_L)/\sqrt{2}$, with one logical qubit held in each memory unit. This state can be manipulated through transversal Hadamard operations on each memory cell and/or X_L and Z_L to any of the three other Bell states in either the X- or Z-basis. The total time for the split/merge operation will be $T = 12dt = 12(\sqrt{N} - 1)t$ for a physical gate time of t and a memory cell containing N qubits. For the NV^- design described in the main text, $t = 3.5\mu$s and for $N = 1600$, $T \approx 1.7$ms

Network operational procedures. The fixed constraints on our bandwidth are the 20-day latency of the ship, the capacity of a memory unit, and our logical gate time, from which we can derive additional operational procedures and hardware development goals. A total of seven shipping containers are utilised for each "online" pair. Two units are permanently located at each shipping terminal. Three mobile units rotate locations. At any point in time, one fixed unit sitting at one terminal is entangled with a mobile memory unit at the far terminal, and this pair is used as the online pair for supplying terminal-to-terminal entanglement to other parts of the network. After the remote entanglement supply in the mobile unit is exhausted, it will be re-entangled with another fixed memory unit at its current location. A second memory unit is aboard ship, entangled with a memory unit at the shipping terminal from which it departed. A third memory unit is creating entanglement with a local partner in preparation for shipping. This ensures that ships are never transporting inactive (unentangled) memory units.

The fixed 20-day transit time serves as an upper bound for completing the entanglement of a mobile memory unit with a fixed memory unit, and for consuming the entanglement after shipping. As this represents a system with low physical density, shipping capacity will limit the throughput. The $T = 1.7$ms logical Bell pair creation time in the main text arises from a surface code distance $d = 39$ and gate operation time $t = 3.5\mu$s, for an NV^- optical architecture, and assumes that inter-container operations can be executed at the same rate as operations local to each memory unit. At this operation rate, the entanglement is created or consumed of a memorystick containing approximately 1KEb (Kilo-Entangled-bit) in the NV^- optical approach in 1.7s, and at full rate an entire shipload of entanglement would be consumed in a few hours. Thus, inter-container operations may be $100\times$ slower without impacting the performance even if only one container at a time out of an entire shipload is used online. The denser memory subsystems, differing physical gate times, and varying code distances for other options in Table 1 will result in different demands on the inter-container interfaces. Because of the generic nature of the created entanglement, slow inter-container interfaces can be compensated for by having more than a single container online.