

# Multi-channel 180pJ/b 2.4GHz FBAR-based Receiver

Phillip M. Nadeau, Arun Paidimarri, Patrick P. Mercier, and Anantha P. Chandrakasan

Microsystems Technology Laboratories, Massachusetts Institute of Technology  
Cambridge, MA, 02139, USA

**Abstract** — A three-channel 2.4GHz OOK receiver is designed in 65nm CMOS and leverages MEMS to enable multiple sub-channels of operation within a band at a very low energy per received bit. The receive chain features an LNA/mixer architecture that efficiently multiplexes signal pathways without degrading the quality factor of the resonators. The single-balanced mixer and ultra-low power ring oscillator convert the signal to IF, where it is efficiently amplified to enable envelope detection. The receiver consumes a total of 180pJ/b from a 0.7V supply while achieving a BER= $10^{-3}$  sensitivity of  $-67$ dBm at a 1Mb/s data rate.

**Index Terms** — Body sensor networks, CMOS, radio frequency integrated circuits, low power electronics, film bulk acoustic resonators, envelope detector.

## I. INTRODUCTION

Research in Wireless Sensor Networks (WSNs) and, more recently, Wireless Body Area Networks (WBANs) has spurred interest in ultra low power wireless systems that maximize battery lifetime or enable energy-harvested operation. The RF circuits typically dominate the power budget [1]-[3]; hence a receiver architecture that consumes the minimum amount of energy per received bit is desirable. A further concern, particularly in crowded unlicensed spectrum, is separation among users, for which frequency division multiplexing is a key technique proposed by the IEEE 802.15.6 Narrowband (NB) PHY for WBANs. But achieving ultra-low power and energy consumption on the node is difficult with the additional constraints imposed by channelization of the bandwidth.

Recent single-channel NB architectures have achieved sub-nJ/b operation by relaxing the frequency synthesizer and sacrificing the front-end bandwidth [4], [5]. The receiver in [6] leveraged a Film Bulk Acoustic Resonator (FBAR) to provide much-improved channel filtering and a very low power design, but is inherently single-channel due to the small (less than 10MHz) effective tuning range of the resonator's parallel resonance. A two-channel two-resonator receiver has previously been presented in [7], but used envelope detection directly at RF, replicated downstream hardware, and consumed 50nJ/b.

This paper presents a 2.4GHz NB receiver architecture with down-conversion before detection that achieves both

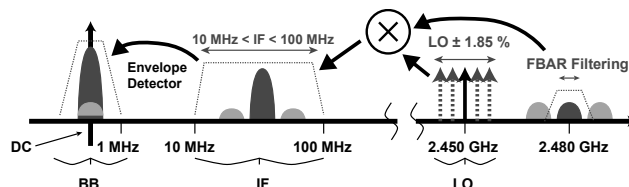


Fig. 1. Frequency plan for the FBAR-RX

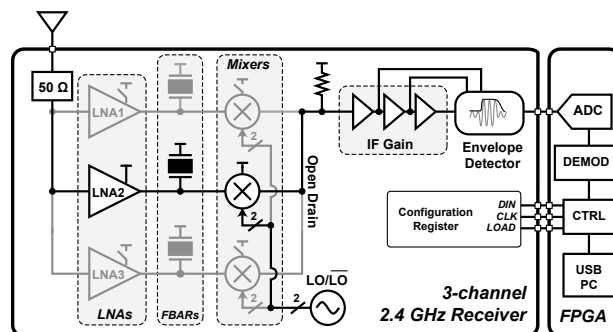


Fig. 2. Architecture of the FBAR-RX

sub-nJ/b energy efficiency and three-channel operation. Channelization is enabled by FBARs, which have an unloaded parallel resonance  $Q$  of roughly 1000, and a corresponding nominal  $-3$ dB bandwidth of 2.4MHz at 2.4GHz. The challenge in this work is to build an energy efficient architecture that multiplexes additional resonators to filter more channels without significantly degrading the resonance  $Q$  or the receiver sensitivity due to switch resistance, additional parasitic capacitance, or cross-coupling between the resonators.

## II. RECEIVER ARCHITECTURE

The receive chain builds on the low-power frequency plan presented in [6] and is shown in Fig. 1. The plan includes a power-efficient ring oscillator to down-convert the RF signal into an IF range from 10MHz to 100MHz that is wide enough to tolerate the LO inaccuracy after a one-time calibration for process variation. FBAR resonators provide high- $Q$  channel filtering at RF, thereby obviating the need to precisely tune the LO with a PLL since the sharp IF bandpass filters seen in conventional super-heterodyne designs can be removed.

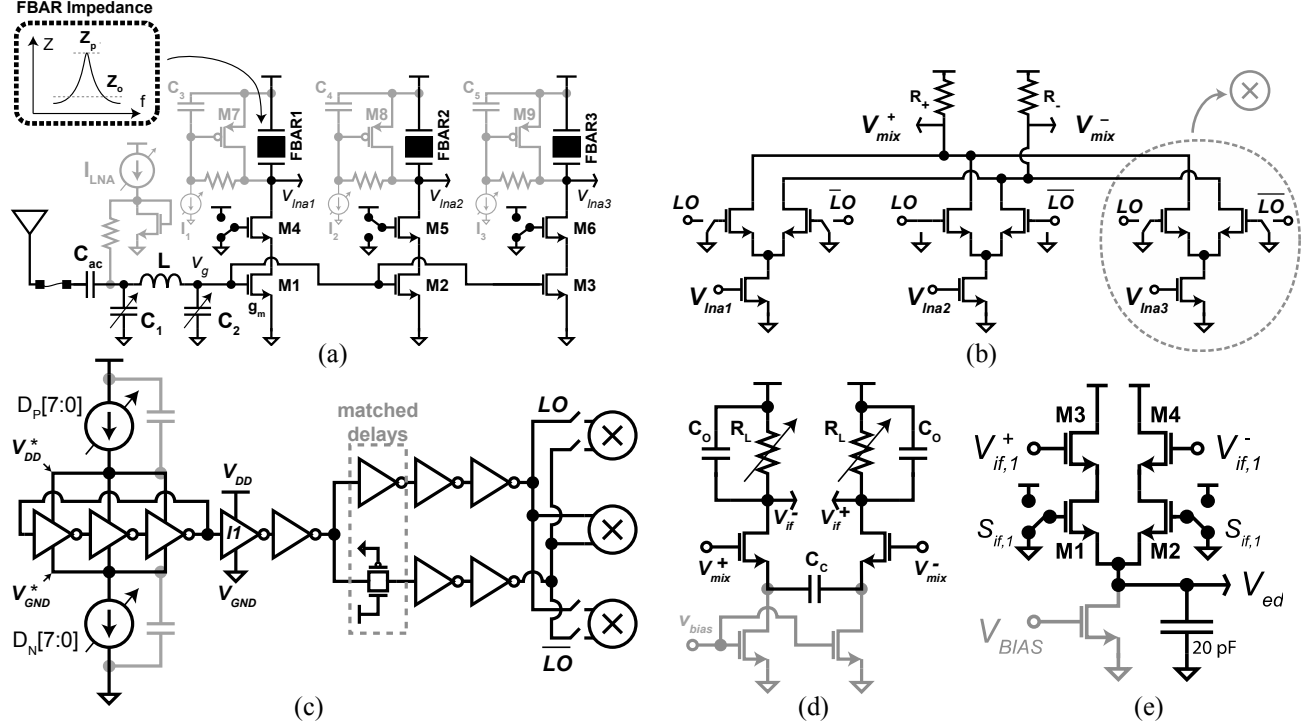


Fig. 3. Ultra-low power RX circuit schematics: (a) three-channel LNA and (b) mixer, with the middle channel active and the other two channels tri-stated, (c) ring-oscillator LO/LO generation, (d) one of the three fixed-gain IF stages, (e) envelope detector.

The architecture developed in this work is summarized in Fig. 2. An on-chip matching network tunes out the gate capacitance of the additional LNAs while simultaneously matching the input to  $50\Omega$  and providing 10dB of passive voltage gain. One stage of RF gain is used ahead of the noise-limiting wide-bandwidth mixer in order to improve the overall sensitivity. Separate LNA blocks for each channel provide isolation between the resonances of each FBAR. The LNAs have high gain at IF due to the high impedance of their bias networks at these frequencies, hence balanced mixers are used to prevent excessive noise from feeding through the mixer at IF. In simulation, this improves the input-referred noise at the antenna by 13.5dB. The signal pathways are then recombined after the mixer stage in an open-drain fashion in order to share IF gain and envelope detection hardware.

### III. CIRCUIT DESIGN

#### A. LNA with FBAR Multiplexing

The LNA circuit presented in Fig. 3(a) was developed to provide isolation between the FBARs while minimizing parasitic loading by the circuit. The design critically avoids series switches that would otherwise degrade the resonance peak.

In Fig 3(a), the antenna port input impedance is matched to  $50\Omega$  using the tunable on-chip  $\pi$ -match

network formed by  $C_1$ ,  $C_2$ , and  $L$ . The transistors M1 to M3 form three common-source LNAs operating in parallel, and M4 to M6 act both as cascode elements and as on-off switches that enable only one LNA pathway at a time. The added gate capacitance of M2 and M3 can be absorbed into  $C_2$  with minimal impact on performance compared to the single channel case. Also, the additional gate noise does not significantly impact sensitivity since the wideband (90MHz BW) mixer stage ultimately limits noise performance. In simulation, this design scales to 12 channels with only a 0.5dB degradation in LNA gain.

The FBARs are included as tuned LNA tank elements, and their filtering capability is governed by the ratio of the tank impedance on the parallel resonance,  $|Z_P| \approx 3k\Omega$ , to the tank impedance off-resonance,  $|Z_O| \approx 50\Omega$ . At DC, M7 to M9 allow bias current to flow past the FBAR to the amplifier, but at RF frequencies, the gates are shunted to the supply by C3 to C5, maintaining a high small-signal output resistance across the FBAR [7].

The LNA's bias current ( $I_{LNA}$ ) can be adjusted by the configuration interface to provide reconfigurable RF gain. Sources I1 to I3 allow tuning of the DC bias points at  $V_{LNA1}$  to  $V_{LNA3}$  for optimum small-signal performance.

In simulation, wirebonding from the IC to the FBAR increased the  $-3$ dB bandwidth of the LNA by 5.6% and the peak LNA voltage gain by 0.8dB ( $L = 1nH$ ,  $Q = 20$ ).

### B. Mixer and Oscillator

Fig. 3(b) shows the three single-balanced mixers that share a common resistive load ( $R_+$  and  $R_-$ ). The activated mixer is connected to the LO through a pass-gate while the inactive mixers are tri-stated by opening the pass-gate and grounding the LO port. This mixer also provides inherent single-ended to differential conversion.

A three-stage current-starved ring oscillator drives the LO port, where a delay-matched pass gate is used to generate the inverted LO (Fig. 3(c)). Eight tuning bits allow the nominal frequency to be tuned from 1.0 to 3.6GHz to accommodate process variations with a one-time calibration. A 50% duty cycle is critical for cancelling the DC feedthrough from the RF port of the mixer. This is achieved by centering the oscillation waveform about inverter  $I_1$ 's switching threshold with separate top and bottom current sources.

### C. IF Gain and Envelope Detector

Energy efficient wideband IF amplification is provided by resistively loaded differential amplifiers with a split source and capacitive coupling to reject DC [4], [6] (Fig. 3(d)). Three IF amplifiers are connected in series to provide reconfigurable gain, and unused amplifiers are power-gated to conserve energy. The differential envelope detector (ED) shown in Fig 3(e) down-converts the IF signal to baseband using an NMOS differential pair that is biased in subthreshold for maximum non-linearity (M3 and M4). By replicating M1 to M4 for each IF stage, the switches M1 and M2 allow the single integrating capacitor to be fed by any of the three IF stages.

## IV. MEASUREMENT RESULTS

The IC was fabricated in a 65nm CMOS technology and wirebonded to three FBARs in a QFN package (Fig. 4). The  $S_{11}$  measurement (Fig. 5(a)) demonstrates the  $50\Omega$  impedance match at the receiver's RF input, where the position of the notch is tunable across the ISM band via the on-chip matching network. In the figure, the notch has been placed at the 2.413GHz channel frequency. Fig. 5(b) demonstrates tuning the on-chip ring oscillator LO across its tuning range, providing coverage for process variation.

The performance of the channel filtering is demonstrated in Fig. 5(c) with a frequency response measurement from the RF input to the detector output superimposed for the three channels. Normalized to the DC level with zero input power, the measured  $-3\text{dB}$  bandwidth is 6MHz. The adjacent channel rejection is demonstrated in Fig. 5(d), where a desired OOK signal is jammed by a continuous wave blocker at various

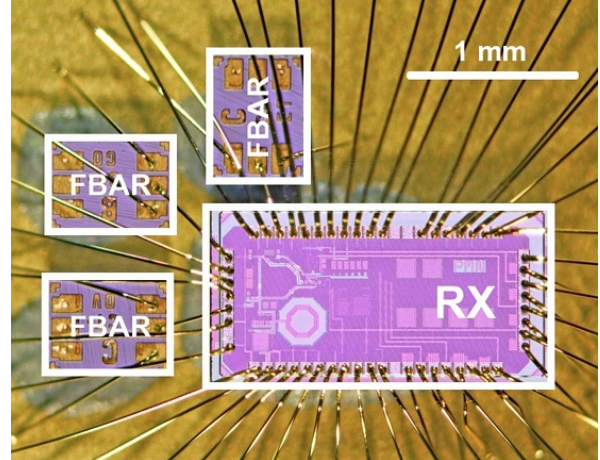


Fig. 4. Packaging photo showing the three FBARs bonded to the 65nm CMOS die

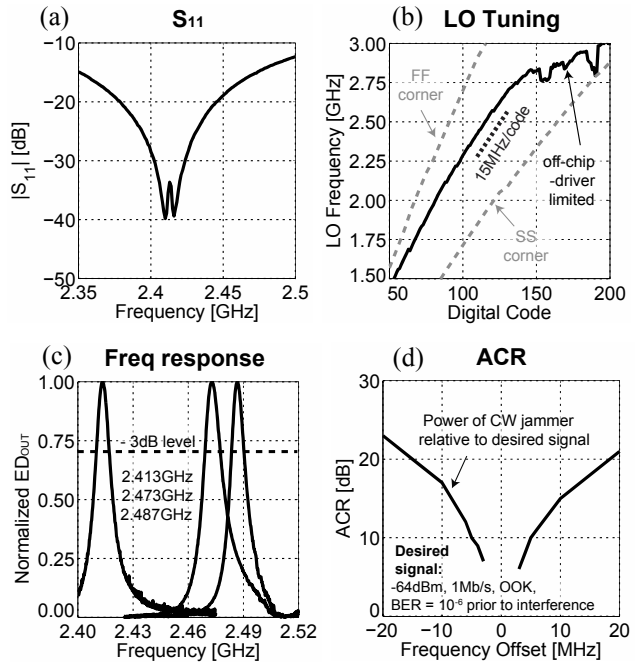


Fig. 5. Receiver measurements (a)  $S_{11}$  at the RF input, (b) measured LO frequency versus tuning code with overlaid corner simulations, (c) detector output for the three frequency channels, (d) adjacent channel rejection.

frequency offsets. The adjacent channel rejection ratio is taken as the interference power, relative to the desired signal strength, that causes the BER to degrade from  $10^{-6}$  to  $10^{-3}$ , and is measured as 11dB at a 6MHz offset.

The BER characteristics of the system for various energy levels and data rates are demonstrated in Fig. 6(a) for OOK demodulation on an external FPGA. With a 0.7V supply, the system achieved  $-67\text{dBm}$  sensitivity at an overall energy consumption of 180pJ/b. Additional

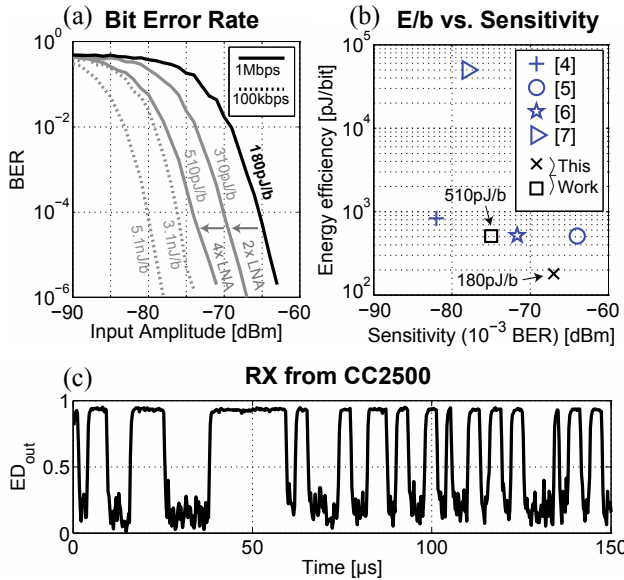


Fig. 6. (a) BER measurements, (b) plot of energy per bit (up to the ED) versus sensitivity for recent low power RX designs, (c) time-domain waveform received from a commercial OOK TX (TI CC2500, +0dBm, 500kb/s, 3m LOS, indoor/office).

measurements were taken showing that total energy consumption can be traded for better sensitivity by adjusting the LNA gain via its bias current and using a 1V LNA supply due to headroom concerns. Also, at slower data rates (eg. 100kb/s), the ADC samples can be averaged before demodulation leading to further sensitivity improvement, shown up to  $-82$  dBm in Fig. 6(a), as a trade-off with energy efficiency.

Fig 6(b) compares the results of this work with previously published low power 2-3GHz receivers, where it compares favorably in energy per bit versus sensitivity at 1Mb/s while still providing three selectable channels of operation. In these low energy designs, link robustness can be assured in a star-network topology by a more energy-abundant basestation (eg. a cellular phone) that compensates for the severely energy-constrained nodes. To demonstrate operability with current technology, Fig 6(c) shows the time-domain waveform received from a commercial low power radio transmitting at its maximum data rate of 500kb/s (Texas Instruments, CC2500).

Finally, Table I summarizes these specifications, including a fast startup time of  $6\mu$ s amenable to efficient duty-cycling in low power applications.

## VII. CONCLUSION

A three-channel ultra-low power 2.4GHz receiver leveraging resonators has been presented in this work. The LNA architecture provides efficient multiplexing to obtain channel selection, permitting the use of a low-

TABLE I  
SPECIFICATION SUMMARY

Technology	65nm CMOS	Power	180 $\mu$ W
Core Area	0.49mm <sup>2</sup>	Rate	1Mb/s
Supply	0.7V	E/bit	180pJ/b
Gain (sim.)	66.4dB	Sens. ( $10^{-3}$ )	$-67$ dBm
Startup time	6 $\mu$ s	No. chan	3

power ring oscillator for down-conversion and low power circuits for gain and detection. In this work, the packaging space consumed by single wirebonded resonators limits the design to a handful of channels, however, flip-chip bonding to an array of binary mass-loaded FBARs, or future integration of resonators in CMOS processes [8] could allow area-efficient expansion of the ideas presented here to many additional channels.

## ACKNOWLEDGEMENT

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