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A Compact 128-Element Schottky Diode Grid Frequency Doubler Generating 0.25 W of Output Power at 183 GHz

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Abstract—This paper presents a compact varactor grid frequency doubler encapsulated in a waveguide environment, thus providing single mode (H_{10}) waveguide connection at both input and output. Schottky diodes are used as varactors in this 128-element grid frequency doubler. By packaging the grid and its embedding network together with a stepped waveguide taper on the output, a module measuring 9 mm \times 19 mm by 19 mm is created. A peak output power of 0.25 W is produced at 183 GHz with 1.32 W of input power and a corresponding conversion efficiency of 19%. The peak conversion efficiency is 23% at 183 GHz with 666 mW of input power.

Index Terms—2-D grid, array, frequency multipliers, grid, millimeter wave, quasi-optical, Schottky diodes, terahertz (THz) sources, varactors.

I. INTRODUCTION

TERAHERTZ (THz) sources find use in applications ranging from satellite borne instruments to ground-based applications such as imaging radar and nondestructive inspection. Therefore, significant research effort is put into THz sources based on semiconductor frequency multipliers, as they offer the best alternative for increasing the available output power in the THz band [1].

High output power from the first multiplication stage is needed for frequency multiplier chains operating at THz frequencies due to the limited conversion efficiency in each stage. Modern millimeter-wave power amplifiers can deliver watt-level input powers at around 100 GHz, and this enables a new generation of high-power first-stage frequency multipliers.

Scalable high power handling capacity frequency multipliers can be realized by the use of grid power combining. Grid power combining here refers to 2-D diode grid structures inside an overmoded waveguide, a technique that in free-space applications is usually referred to as quasi-optical power combining. An advantage of grid multipliers is that the size and device density can be adapted to suit the available input power. A good summary and discussion of grid multiplier design can

be found in [2] and the quasi-optical equivalent in [3]. Other successful grid frequency multiplier demonstrators include an HBV grid with 684 mW of output power at 93 GHz [4] and 35 mW at 247 GHz [5].

In this letter, the design and realization of a first-stage high-power multiplier is presented using a waveguide encapsulated scalable grid topology. Initially, the design is discussed and then measurement data showing a maximum output power of 0.25 W is presented. Finally, this letter concludes with a discussion about the implications of this letter and deviations between the design model and the measured results.

II. DESIGN

The paralleled unit cell modeling approach outlined in [5] was used in the design of a 1-W input power multiplier module. The varactor grid consists of 128 square unit cells organized into 8 rows and 16 columns, with the columns aligned with the E -field of the waveguide. In the center of each cell is an 18- μm^2 Schottky diode varactor with $R_s = 3$ Ohm and $C_{j0} = 26$ fF on an $N_d = 2 \times 10^{17}$ cm^{-3} doped GaAs epi. The propagating input wave and the generated second harmonic are coupled to the varactors through 21- μm -wide inductive strips contacted with 15- μm -long and 3- μm -wide fingers. The inductive strips also provide a dc path that is used to serially reverse bias all eight varactors in each column. A filter made of 36- μm wide inductive strips serves as a back short for the input frequency and a high-pass filter for the second harmonic. Both the varactor and filter grids unit cells measure 160 $\mu\text{m} \times 160 \mu\text{m}$. The Schottky varactors and matching components were processed by the authors in the Chalmers Nanofabrication Laboratory (MC2).

On the input side, a GaAs matching slab acts as an input matching network, simultaneously rejecting the second harmonic generated in the grid. Bias is routed to the varactor chip through a channel in the waveguide wall. 25- μm bond wires are used to connect a contact pad on the edge of the varactor chip to a bias circuit in the channel. An identical bias pad connecting to the cathode side of the diodes is bonded to the earthed waveguide block.

The waveguide mechanical structure is divided into three shims, where the first holds the input matching substrate, the second the varactor grid and filter stack, and the third the output waveguide taper. The input waveguide measures

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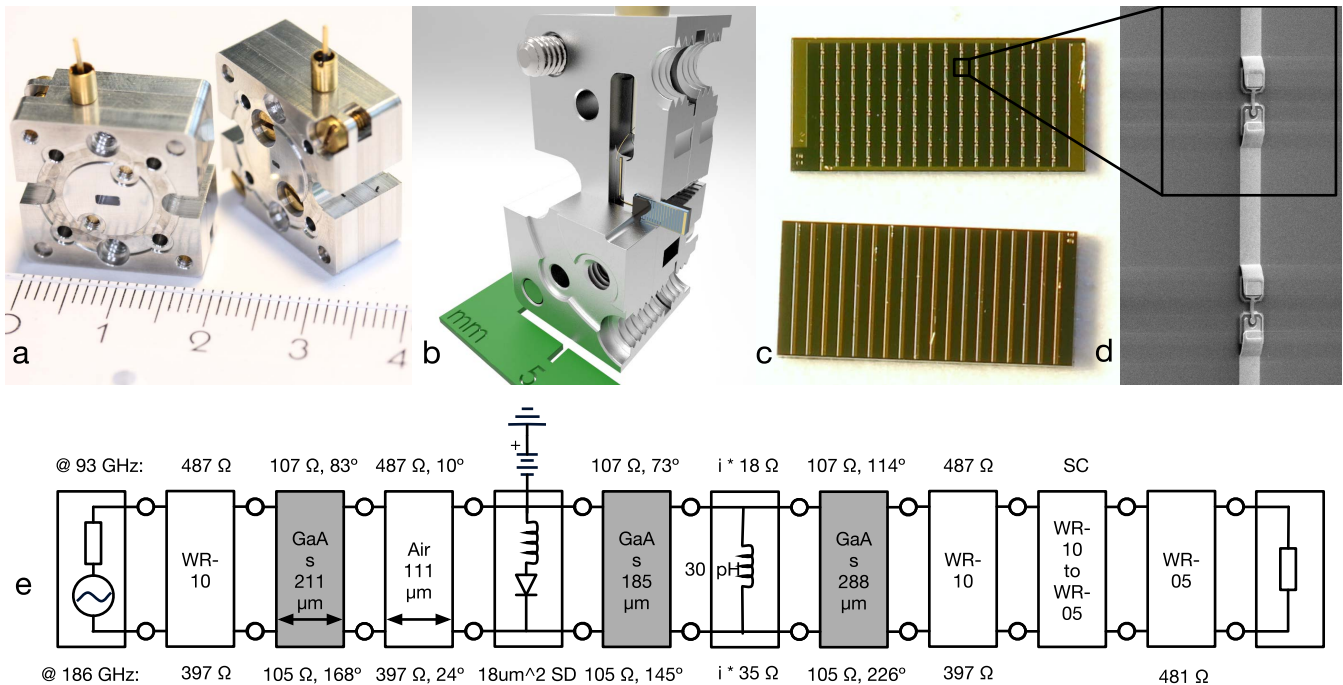


Fig. 1. (a) Photograph of two assembled modules. (b) Rendering of a module with parts of the waveguide shims cut away to reveal the input matching (mostly cut away to show the grid), varactor grid, and output filter. (c) Photograph of one fabricated varactor grid and one output filter. (d) SEM picture of a varactor diode in the grid, in which the unit cell boundary is marked by the overlaid black square. (e) Lumped component transmission line model showing one set of cascaded unit cells in the simulator finite element models accounting for the geometry-related parasitics is used for all unit cells. Altogether eight identical sets of unit cells are used in the harmonic balance simulation model, pumped with different input powers depending on their position in the grid.

1.27 mm \times 2.6 mm with a 0.3-mm corner radius, and thus it is impedance matched to a standard WR-10 waveguide. The matching substrate, varactor array, and filter all have the dimensions 1.40 mm \times 3.06 mm, with thicknesses 211 μm , 185 μm , and 288 μm , respectively. To enable mounting of the substrates in the shims, a pocket with a 50- μm clearance on each side of the substrates is designed into the shims. The output taper consists of a five-step transformer to an output WR-5.1 waveguide. The assembled module measures only 9 mm \times 19 mm \times 19 mm excluding the bias pin, with input and output MIL-DTL-3922/67C compatible waveguide flanges. All three shims are milled out of an aluminum alloy and the parts are used without additional surface treatments.

III. MEASUREMENT RESULTS

A high-power Quinstar QPN-940432220ICUT amplifier with an isolator on the output was used to pump the multiplier module during measurements and a calibrated diode sensor was used to measure the input power through a waveguide coupler. The output second harmonic was measured using a calorimetric waveguide power sensor. During output power measurements exceeding 200 mW, a 35-cm long WR-5.1 waveguide, with a 3.8-dB loss was used as an attenuator on the output to protect the power meter. On the input of the calorimetric power meter, a WR-5.1 to WR-10 taper and a 25-mm-long WR-10 waveguide is assumed to cause 0.5 dB of loss. This is considered to be a conservative estimate concerning the discussion in [6] and the fact that no compensation has been added for the 25-mm-long internal waveguide of the power meter.

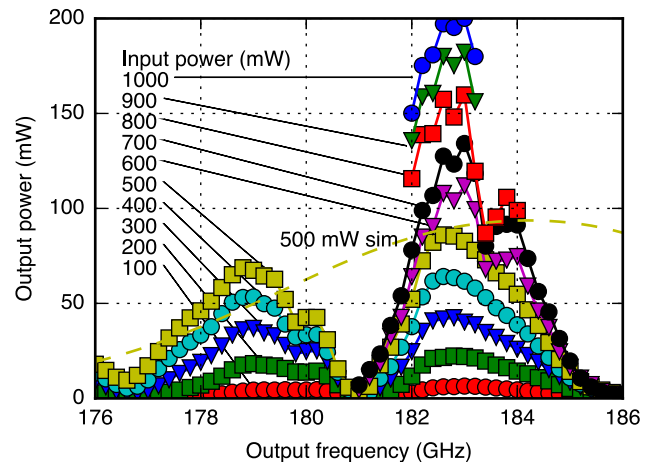


Fig. 2. Measured output power as a function of the output frequency and the input power. Input power is marked in the graph next to the data series. The bias voltage is -23.4 V up to input powers of 800 mW and -28 V for higher input powers. Simulated data for 500 mW of input power are plotted as a dashed line.

All presented data are thus the authors' best estimate of flange-to-flange performance of the multiplier module. In Fig. 2, the output power is plotted as a function of output frequency for input powers ranging from 100 to 1000 mW. Since the drive amplifier was operated at the lower edge of its operating band, no more than 500 mW of input power was available below the 90.5-GHz input frequency. The measured output power and conversion efficiency at 183 GHz as a function of input power are plotted in Fig. 3 for a reverse bias of -28 V . In addition, the conversion efficiencies at 183 GHz

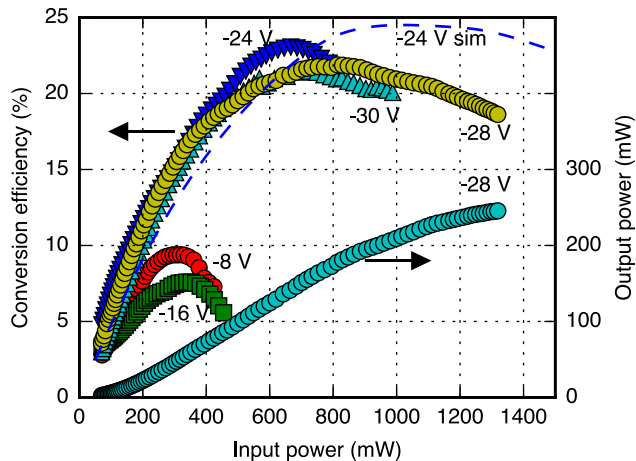


Fig. 3. Measured conversion efficiency as a function of the input power and the bias voltage at a 183-GHz output frequency. The dashed line is the simulated conversion efficiency at -24 V bias. The measured output power at -28 V bias is also plotted.

for different reverse bias voltages are plotted as a function of input power.

IV. DISCUSSION

The frequency response of the presented multiplier plotted in Fig. 2 shows periodic in-band zeros compared with the simulation data from the transmission line model. The authors have tried to locate the source of this and come to the conclusion that is likely due to a resonance in the input network, either in the form of an excited substrate mode or simply a matching condition that allows the generated second harmonic to propagate toward the input side. The second option is possible due to the fact that the design lacks a frequency selective input filter, an approach used to minimize input loss and simplify the design.

The current design was aiming for a peak efficiency with 1 W of input power and a -24 V bias, Fig. 3 shows that the peak efficiency occurs at approximately 0.7 W of input power. The bias voltage dependence shown in Fig. 3 reveals a quickly saturated conversion efficiency for low reverse bias voltages, i.e., -8 and -16 V. This is due to the fact that the varactors enter into forward conductance during the voltage swing, an effect that can be observed as an increasing rectified current at the bias port. In general, an increasing rectified current observed on the bias port correlates well with the maximum efficiency for all bias voltages. When biased at -30 V, abrupt changes in the bias current were observed for high drive levels, and this indicates that some varactors experience reverse breakdown, altogether this indicates that the varactors are operating close to their maximum voltage swing when driven at full input power and biased at -28 V.

As the available pump power increases, the grid can easily be scaled to handle higher input power by altering the diode density or anode area. Traditional design approaches for frequency multipliers still achieve higher peak efficiencies but lack the scalability in terms of power handling capability. The reduction of the average conversion efficiency caused by the uneven excitation of the grid is compensated for by the high conversion efficiency of the center elements,

TABLE I
COMPARISON OF STATE-OF-THE-ART HIGH-POWER FREQUENCY MULTIPLIERS IN THE 100–200 GHz RANGE

Type	P_{out}	$eff @ P_{out}$	Ref
X2 Schottky	135 mW @ 189 GHz	27 %	[7]
X3 Schottky	192 mW @ 116 GHz	24 %	[7]
X3 HBV	240 mW @ 111 GHz	18 %	[8]
X2 Schottky	430 mW @ 103 GHz	-	[9]
X2 Grid	250 mW @ 183 GHz	19 %	This work

simulated to be in excess of 40%. Grid multipliers can easily be adapted to higher operating frequencies as power amplifier technology continues to develop toward higher powers and higher frequencies.

V. CONCLUSION

A high-power waveguide embedded grid Schottky varactor frequency doubler with an output power of 0.25 W at 183 GHz has been presented. The peak conversion efficiency of 23% at 183 GHz is to the authors' knowledge the highest reported for waveguide-enclosed grids independent of output frequency; the previous record was achieved at 93 GHz [4]. We have shown that high-power grid frequency multipliers can be designed without significant penalty in conversion efficiency compared with traditional high power designs. However, more work is needed to remove the in-band resonances present in this first design iteration. Nevertheless, the output power, power handling, and conversion efficiency of this doubler is in the forefront of high-power frequency multipliers (see Table I).

Additionally, the grid multipliers can be scaled in frequency, as well as the ability to handle at least an order of magnitude higher input power than competing single chip designs.

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