Three-Dimensional Wiring for Extensible Quantum Computing: The Quantum Socket

J. H. Béjanin,[1,2] T. G. McConkey,[1,3] J. R. Rinehart,[1,2] C. T. Earnest,[1,2] C. R. H. McRae,[1,2] D. Shiri,[1,2,†] J. D. Bateman,[1,2,‡] Y. Rohanizadegan,[1,2] B. Penava,[4] P. Breul,[4] S. Royak,[4] M. Zapatka,[5] A. G. Fowler,[6] and M. Mariantoni[1,2,*]

[1]*Institute for Quantum Computing, University of Waterloo, 200 University Avenue West, Waterloo, Ontario N2L 3G1, Canada*
[2]*Department of Physics and Astronomy, University of Waterloo, 200 University Avenue West, Waterloo, Ontario N2L 3G1, Canada*
[3]*Department of Electrical and Computer Engineering, University of Waterloo, 200 University Avenue West, Waterloo, Ontario N2L 3G1, Canada*
[4]*INGUN Prüfmittelbau GmbH, Max-Stromeyer-Straße 162, D-78467 Konstanz, Germany*
[5]*INGUN USA, Inc., 252 Latitude Lane, Suite 102, Lake Wylie, South Carolina 29710-8152, USA*
[6]*Google Inc., Santa Barbara, California 93117, USA*

(Received 27 May 2016; revised manuscript received 7 August 2016; published 18 October 2016)

Quantum computing architectures are on the verge of scalability, a key requirement for the implementation of a universal quantum computer. The next stage in this quest is the realization of quantum error-correction codes, which will mitigate the impact of faulty quantum information on a quantum computer. Architectures with ten or more quantum bits (qubits) have been realized using trapped ions and superconducting circuits. While these implementations are potentially scalable, true scalability will require systems engineering to combine quantum and classical hardware. One technology demanding imminent efforts is the realization of a suitable wiring method for the control and the measurement of a large number of qubits. In this work, we introduce an interconnect solution for solid-state qubits: the *quantum socket*. The quantum socket fully exploits the third dimension to connect classical electronics to qubits with higher density and better performance than two-dimensional methods based on wire bonding. The quantum socket is based on spring-mounted microwires—the *three-dimensional wires*—that push directly on a microfabricated chip, making electrical contact. A small wire cross section (approximately 1 mm), nearly nonmagnetic components, and functionality at low temperatures make the quantum socket ideal for operating solid-state qubits. The wires have a coaxial geometry and operate over a frequency range from dc to 8 GHz, with a contact resistance of approximately 150 mΩ, an impedance mismatch of approximately 10 Ω, and minimal cross talk. As a proof of principle, we fabricate and use a quantum socket to measure high-quality superconducting resonators at a temperature of approximately 10 mK. Quantum error-correction codes such as the surface code will largely benefit from the quantum socket, which will make it possible to address qubits located on a two-dimensional lattice. The present implementation of the socket could be readily extended to accommodate a quantum processor with a (10×10)-qubit lattice, which would allow for the realization of a simple quantum memory.

DOI: 10.1103/PhysRevApplied.6.044010

I. INTRODUCTION

At present, one of the main objectives in the quantum computing community is to build prototypes of practical hardware technology for scalable architectures that may lead to the realization of a universal quantum computer [1]. In this work, we undertake the task of implementing an extensible wiring method for the operation of a quantum processor based on solid-state devices, e.g., superconducting qubits [2–4]. Possible experimental solutions based on wafer-bonding techniques [5–9] or coaxial through-silicon vias [10] as well as theoretical proposals [11,12] have recently addressed the wiring issue, highlighting it as a priority for quantum computing.

Building a universal quantum computer [13–18] will make it possible to execute quantum algorithms [19], which would have profound implications on science and society. For a quantum computer to be competitive with the most advanced classical computer, it is widely believed that the qubit operations will require error rates on the order of 10^{-15} or less. Achieving such error rates is possible only by means of quantum error-correction (QEC) algorithms [14,16,20], for example, the surface-code algorithm [21,22].

*Corresponding author.
matteo.mariantoni@uwaterloo.ca
†Present address: Department of Physics, Chalmers University of Technology, SE-412 96 Göteborg, Sweden.
‡Present address: The Edward S. Rogers Sr. Department of Electrical and Computer Engineering, University of Toronto, 10 King's College Road, Toronto, Ontario M5S 3G4, Canada.

Quantum-computing architectures are based on effective quantum-mechanical two-level systems, or physical qubits, which can be implemented using photons [23,24], trapped ions [25], spins in molecules [26] and quantum dots [27–31], spins in silicon [30,32], and superconducting quantum circuits [2–4]. The last are leading the way for the realization of the first surface-code logical qubit, which will be implemented as an ensemble of a large number of physical qubits. Recently, several experiments based on superconducting quantum circuits demonstrated the principles underlying the surface code. These works showed a complete set of physical gates with fidelities approximately at the surface-code threshold [33], the parity measurements necessary to detect quantum errors [34,35], and realized a classical version of the surface code on a one-dimensional array of nine physical qubits [36]. Notably, the planar design inherent in the superconducting qubit platform makes it possible to implement large two-dimensional qubit arrays, as required by the surface code.

Despite all of these accomplishments, a truly scalable qubit architecture has yet to be demonstrated. Wiring is one of the most basic unsolved scalability issues common to most solid-state qubit implementations, where qubit arrays are fabricated on a chip. The conventional wiring method based on wire bonding suffers from fundamental scaling limitations as well as mechanical and electrical restrictions. Wire bonding relies on bonding pads located at the edges of the chip. Given a two-dimensional lattice of $N \times N$ physical qubits on a square chip, the number of wire bonds that can be placed scales approximately as $4N$ (N bonds for each chip side). Wire bonding will thus never be able to reach the required N^2 law according to which physical qubits scale on a two-dimensional lattice. Furthermore, for a large N, wire bonding precludes the possibility of accessing physical qubits in the center region of the chip, which is unacceptable for a physical implementation of the surface code. In the case of superconducting qubits, for example, qubit control and measurement are typically realized by means of microwave pulses or, in general, pulses requiring large frequency bandwidths. By their nature, these pulses cannot be reliably transmitted through long sections of quasifiliform wire bonds. In fact, stray capacitances and inductances associated with wire bonds—as well as the self-inductance of the bond itself—limit the available frequency bandwidth, thus compromising the integrity of the control and measurement signals [37].

In this work, we set out to solve the wiring bottleneck common to almost all solid-state qubit implementations. Our solution is based on suitably packaged *three-dimensional microwires* that can reach any area on a given chip from above. We define this wiring system as the *quantum socket*. The wires are coaxial structures consisting of spring-loaded inner and outer conductors with diameters of 380 and 1290 μm, respectively, at the smallest point and with a maximum outer diameter of 2.5 mm. The movable section of the wire is characterized by a maximum stroke of approximately 2.5 mm, allowing for a wide range of on-chip mechanical compressions. All wire components are nearly nonmagnetic, thereby minimizing any interference with the qubits. The three-dimensional wires work both at room temperature and at cryogenic temperatures as low as approximately 10 mK. The wires' test-retest reliability (repeatability) is excellent, with marginal variability over hundreds of measurements. Their electrical performance is good from dc to at least 8 GHz, with a contact resistance smaller than 150 mΩ and an instantaneous impedance mismatch of approximately 10 Ω. Notably, the coaxial design of the wires strongly reduces unwanted cross talk, which we measured to be, at most, -45 dB for a realistic quantum-computing application.

This article is organized as follows. In Sec. II, we introduce the quantum-socket design and microwave simulations. In Sec. III, we show the socket physical implementation, with emphasis on materials and alignment procedures. In Sec. IV, we present a comprehensive dc and microwave characterization of the quantum-socket operation at room and cryogenic temperatures. In Sec. V, we show an application of the quantum socket relevant to superconducting quantum computing, where the socket is used to measure aluminum (Al) superconducting resonators at a temperature of approximately 10 mK. Finally, in Sec. VI, we envision an extensible quantum-computing architecture where a quantum socket is used to connect to a 10×10 lattice of superconducting qubits.

II. THE QUANTUM-SOCKET DESIGN

The development of the quantum socket requires a stage of meticulous micromechanical and microwave design and simulations. It is determined that a spring-loaded interconnect—the three-dimensional wire—is the optimal method to electrically access devices lithographically fabricated on a chip [38] and operated in a cryogenic environment. An on-chip contact pad geometrically and electrically matched to the bottom interface of the wire can be placed easily at any desired location on the chip as part of the fabrication process, thus making it possible to reach any point on a two-dimensional lattice of qubits. The coaxial design of the wire provides a wide operating frequency bandwidth, while the springs allow for mechanical stress relief during the cooling process. The three-dimensional wires used in this work take advantage of the knowledge in the existing field of microwave-circuit testing [39]. However, reducing the wire dimensions to a few hundred micrometers and using it to connect to quantum-mechanical microfabricated circuits at low temperatures results in a significant extension of existing implementations and applications.

A. Three-dimensional wires

Figure 1 shows the design of the quantum-socket components. Figure 1(a) displays a model of a three-dimensional wire. The coaxial design of the wire is visible from the image, which features a wire that is 30.5 mm long when uncompressed. The wire is characterized by an inner cylindrical pin with a diameter of 380 μm and an outer cylindrical body (the electrical ground) with a diameter of 1290 μm in its narrowest region; this region is the bottom-most section of the wire and, hereafter, will be referred to as

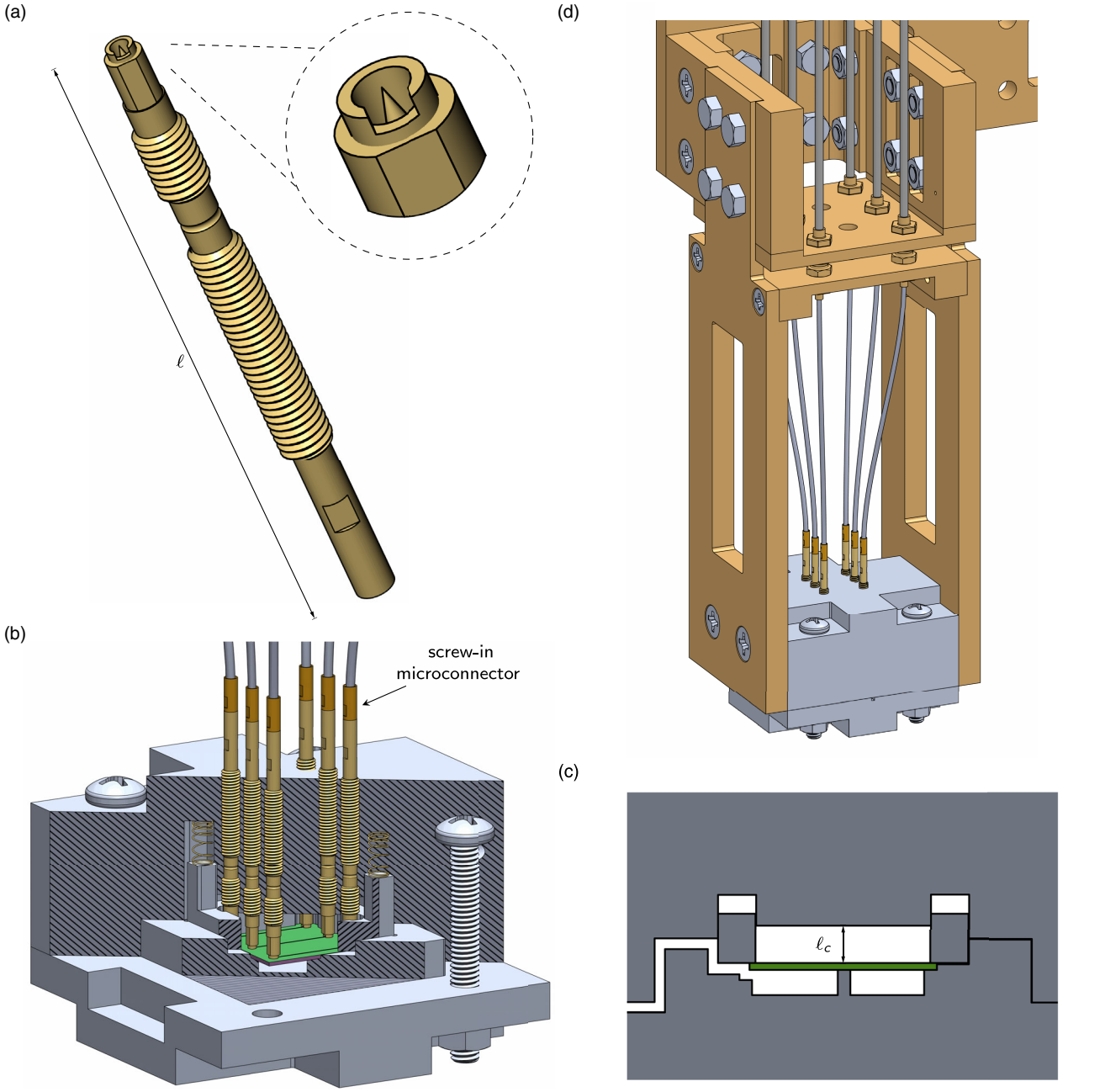

FIG. 1. Computer-aided designs of the three-dimensional wire, microwave package, and package holder. (a) A wire of length $\ell = 30.5$ mm along with a detail of the contact head (inset). (b) Assembled microwave package including six three-dimensional wires, washer, washer springs, and chip (shown in green). The arrow indicates the screw-in microconnector mated to the back end of the wire. Forward hatching indicates the washer cutaway, whereas backward hatching indicates both lid and sample-holder cutaways. (c) Cross section of the microwave package showing the height of the upper cavity, which coincides with the minimum compression distance ℓ_c of the three-dimensional wires (see Appendix A). (d) Microwave package mounted to the package holder, connected, in turn, to the mounting plate of a DR with SMP connectors. A channel with a cross-sectional area of 800×800 μm^2 connects the inner cavities of the package to the outside, thus making it possible to evacuate the inner compartments of the package. This channel meanders to prevent external electromagnetic radiation from interfering with the sample.

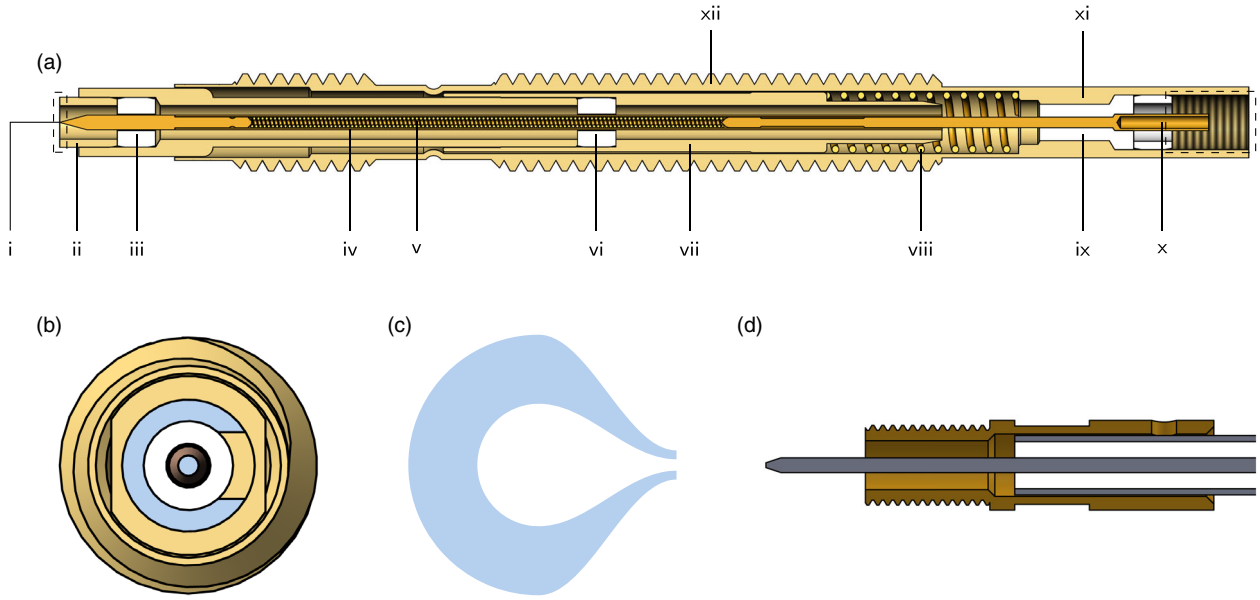

FIG. 2. Two-dimensional cut view of the three-dimensional wire, contact pad, and screw-in microconnector. (a) Side view of the wire cross section. The wire components are i spring-loaded center conductor of the contact head; ii spring-loaded outer conductor of the contact head; iii, vi, and ix dielectric spacers; iv center-conductor barrel; v center-conductor spring; vii outer-conductor barrel; viii outer-conductor spring; x center-conductor tail; xi outer-conductor tail; and xii threaded outer body. The dashed box on the left indicates the contact head, whereas that on the right indicates the female threads included for use with the screw-in microconnector. (b) Front view of the wire. The blue surface indicates the wire bottom interface. (c) On-chip contact pad. Here, the blue surface indicates the pad dielectric gap, whereas the white surfaces refer to conductors (thin metallic films deposited on a dielectric substrate). (d) Screw-in microconnector. The left end of the microconnector mates with the back end of the three-dimensional wire; the right end is soldered to a coaxial cable, the inner conductor of which serves as the inner conductor of the microconnector (slotting into x).

the wire *contact head* [see the inset of Fig. 1(a), as well as the dashed box on the left side of Fig. 2(a)]. The contact head terminates at the wire *bottom interface*; this interface is designed to mate with a pad on a chip [see Figs. 2(b) and 2(c)]. The outer body includes a rectangular aperture, the *tunnel*, to prevent shorting the inner conductor of an on-chip coplanar-waveguide (CPW) transmission line [40,41]; the transmission line can connect the pad with any other structure on the chip. Two different tunnel dimensions are designed, with the largest one reducing potential alignment errors [42]. The tunnel height is 300 μm in both cases, with a width of 500 or 650 μm. The internal spring mechanisms of the wire allow the contact head to be compressed; the maximum stroke is designed to be 2.5 mm, corresponding to a working stroke of 2.0 mm.

The outer body of the three-dimensional wire is an M2.5 male thread used to fix the wire to the lid of the microwave package [see Figs. 1(b) and 1(d)]. The thread is split into two segments 3.75 and 11.75 mm long that are separated by a constriction with an outer diameter of 1.90 mm. The constriction is necessary to assemble and maintain in place the inner components of the three-dimensional wire. A laser-printed marker is engraved into the top of the outer body. The marker is aligned with the center of the tunnel, making it possible to mate the wire bottom interface with a pad on the underlying chip with a high degree of angular precision.

Figure 2(a) shows a lateral two-dimensional cut view of the three-dimensional wire. Two of the main wire components are the inner and outer barrels, which compose part of the inner and outer conductors. The inner-conductor barrel is a hollow cylinder with outer and inner diameters of 380 and 290 μm [indicated as part iv in Fig. 2(a)], respectively. This barrel encapsulates the inner-conductor spring. The outer-conductor barrel is a hollow cylinder as well, in this case with an inner diameter of 870 μm [Figs. 2(a) part ii and 2(a) part vii]. Three polytetrafluoroethylene (PTFE) disks serve as spacers between the inner and outer conductors; such disks contribute marginally to the wire dielectric volume, the majority of which is air or vacuum. The outer spring is housed within the outer barrel towards its back end, just before the last PTFE disk on the right-hand side of the wire. The *back end* of the wire is a region comprising a female thread on the outer conductor and an inner-conductor barrel [see the dashed box on the right-hand side of Fig. 2(a)].

The inner-conductor tip is characterized by a conical geometry with an opening angle of 30°. Such a sharp design is chosen to ensure that the tip would pierce through any possible oxide layer forming on the contact-pad metallic surface, thus allowing for a good electrical contact.

Figure 2(c) shows the design of a typical on-chip pad used to make contact with the bottom interface of a three-dimensional wire. The pad comprises an inner and an outer

conductor, with the outer conductor being grounded. The pad in the figure is designed for a silver (Ag) film with a thickness of 3 μm. A variety of similar pads are designed for gold (Au) and Al films with a thickness ranging between approximately 100 and 200 nm. The pad inner conductor is a circle with a diameter of 320 μm that narrows to a linear trace (i.e., the inner conductor of a CPW transmission line) by means of a raised-cosine taper. The raised cosine makes it possible to maximize the pad area while minimizing impedance mismatch. As designed, the wire and the pad allow for lateral and rotational misalignments of ∓ 140 μm and $\mp 28°$, respectively. The substrate underneath the pad is assumed to be silicon (Si) with a relative electric permittivity of $\epsilon_r \simeq 11$. The dielectric gap between the inner and outer conductors is 180 μm in the circular region of the pad; the outer edge of the dielectric gap then follows a similar raised-cosine taper as the inner conductor. The pad's characteristic impedance is designed to be $Z_c = 50\ \Omega$.

B. Microwave package

The microwave package comprises three main parts: the lid, the sample holder, and the grounding washer. The package is a parallelepiped with a height of 30 mm and with a square base having a side length of 50 mm. The chip is housed inside the sample holder. All of these components mate as shown in Figs. 1(b) and 1(c).

In order to connect a three-dimensional wire to a device on a chip, the wire is screwed into an M2.5 female thread that is tapped into the lid of the microwave package, as depicted in Fig. 1(b). The pressure applied by the wire to the chip is set by the depth of the wire in the package. The wire stroke, package dimensions, thread pitch, and alignment constraints impose discrete pressure settings (see Appendix A). In the present implementation of the quantum socket, the lid is designed to hold a set of six three-dimensional wires, which are arranged in two parallel rows. In each row, the wires are spaced 5.75 mm from center to center, with the two rows being separated by a distance of 11.5 mm.

A square chip of lateral dimensions 15×15 mm^2 is mounted in the sample holder in a similar fashion as in Ref. [43]. The outer edges of the chip rest on four protruding lips, which are 1 mm wide. Hereafter, those lips will be referred to as the *chip recess*. For design purposes, a chip thickness of 550 μm is assumed. Correspondingly, the chip recess is designed so that the top of the chip protrudes by 100 μm with respect to the adjacent surface of the chip holder, i.e., the depth of the recess is 450 μm [see Fig. 1(c)]. The outer edges of the chip are pushed on by a spring-loaded grounding washer. The 100-μm chip protrusion ensures a good electrical connection between chip and washer, as shown in Fig. 1(c).

The grounding washer is designed to substitute the large number of lateral bonding wires that would otherwise be required to provide a good ground to the chip (as shown, for example, in Fig. 6 of Ref. [43]). The washer springs are visible in Fig. 1(b), which also shows a cut view of the washer. The washer itself is electrically grounded by means of the springs as well as through galvanic connection to the surface of the lid. The four feet of the washer, which can be seen in the cut view of Fig. 1(b), can be designed to be shorter or longer. This flexibility makes it possible to choose different pressure settings for the washer.

After assembling the package, there exist two electrical cavities [see Fig. 1(c)]: one above the chip, formed by the lid, washer, and metallic surface of the chip (the *upper cavity*), and one below the chip, formed by the sample holder and metallic surface of the chip (the *lower cavity*). The hollow cavity above the chip surface has the dimensions $14 \times 14 \times 3.05$ mm^3. The dimensions of the cavity below the chip surface are $13 \times 13 \times 2$ mm^3. The lower cavity helps mitigate any parasitic capacitance between the chip and the box (the ground). Additionally, it serves to lower the effective electric permittivity in the region below the chip surface, increasing the frequency of the substrate modes (see Sec. II D).

A pillar of a square cross section with a side length of 1 mm is placed right below the chip at its center; the pillar touches the bottom of the chip, thus providing mechanical support [44]. The impact of such a pillar on the microwave performance of the package is described in Sec. II D.

C. Package holder

The three-dimensional wires, which are screwed into the microwave package, must be connected to the qubit control and measurement electronics. In addition, for cryogenic applications, the package must be thermally anchored to a refrigeration system in order to be cooled to the desired temperature. Figure 1(d) shows the mechanical module we designed to perform both electrical and thermal connections. In this design, each three-dimensional wire is connected to a *screw-in microconnector*, which is indicated by an arrow in Fig. 1(b) and is shown in detail in Fig. 2(d). One end of the microconnector comprises a male thread and an inner-conductor pin that mate with the back end of the three-dimensional wire. The other end of the microconnector is soldered to a coaxial cable [45].

The end of each coaxial cable opposite to the corresponding three-dimensional wire is soldered to a subminiature push-on (SMP) connector. The SMP connectors are bolted to a horizontal plate attached to the microwave package by means of two vertical fixtures, as shown in Fig. 1(d). The vertical fixtures and the horizontal plate constitute the package holder. The package holder and the microwave package form an independent assembly. A horizontal mounting plate, designed to interface with the package holder, houses a set of matching SMP connectors. The mounting plate is mechanically and, thus, thermally

anchored to the mixing chamber (MC) stage of a dilution refrigerator (DR).

D. Microwave simulations

The three-dimensional wires, the 90° transition between the wire and the on-chip pad, and the inner cavities of a fully assembled microwave package are extensively simulated numerically at microwave frequencies [46]. The results for the electromagnetic field distribution at a frequency of approximately 6 GHz, which is a typical operation frequency for superconducting qubits, are shown in Fig. 3. Figure 3(a) shows the field behavior for a bare three-dimensional wire. The field distribution resembles that of a coaxial transmission line except for noticeable perturbations at the dielectric PTFE spacers. Figure 3(b) shows the 90° transition region. This region is critical for signal integrity since abrupt changes in physical geometry cause electrical reflections [39,48]. In order to minimize such reflections, an impedance-matched pad is designed. However, this design leads to a large electromagnetic volume in proximity to the pad, as seen in Fig. 3(b), possibly resulting in parasitic capacitance and cross talk.

In addition to considering the wire and the transition region, the electrical behavior of the inner cavities of the package is studied analytically and simulated numerically. As described in Sec. II B, the metallic surface of the chip effectively divides the cavity of the sample holder into two regions: a vacuum cavity above the metal surface and a cavity partially filled with a dielectric below the metal surface. The latter is of greater concern, as the dielectric acts as a perturbation to the cavity vacuum [49], thus lowering the box modes. For a simple rectangular cavity, the frequency f of the first mode due to this perturbation can be found as [41]

$$f = f_0 - \frac{f_0(\epsilon_r - 1)d_s}{2b}, \tag{1}$$

where f_0 is the frequency of the unperturbed mode, ϵ_r the relative electric permittivity of the dielectric, d_s the substrate thickness, and b the cavity height. From Eq. (1), we estimate this box mode to be 12.8 GHz. However, considering the presence of the pillar, the three-dimensional wires, etc., we have to use numerical simulations to obtain a more accurate estimate of the lowest box modes. The results for the first three modes are reported in Table I. Discounting the pillar, the analytical and simulated values are in good agreement with each other. The addition of the support pillar significantly lowers the frequency of the modes. In fact, it increases the relative filling factor of the cavity by confining more of the electromagnetic field to the dielectric than to the vacuum. Given the dimensions of this design, the pillar leads to a first mode which could interfere with typical qubit frequencies. In spite of this

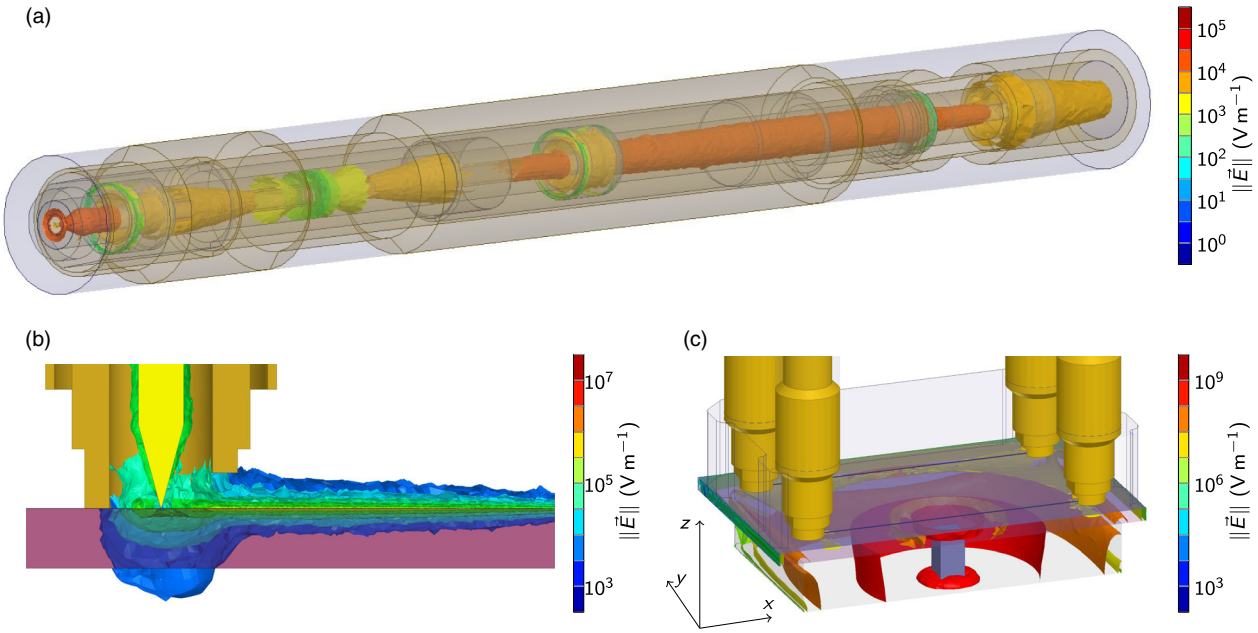

FIG. 3. Numerical simulations of the electric field distribution. (a) Field for a three-dimensional wire at 6 GHz. (b) Field in proximity to the 90° transition region, also at 6 GHz. (c) Field for the first box mode at 6.3 GHz. Color-bar scales are indicated in their respective panels. The x, y, and z directions of a Cartesian coordinate system are also indicated. In (b), the cross section of the transition region is shown. Note the large volume occupied by the electric field beneath the contact pad. In (c), an offset cross section of the first box mode is shown. The field confinement due to the pillar is clearly visible. Additionally, the simulation shows a slight field confinement in the region surrounding the chip recess. A time-domain animation of the simulated electric field distributions can be found in Sec. S3 of the Supplemental Material [47].

TABLE I. Simulation results for the first three box modes of the lower cavity inside the assembled microwave package shown in Fig. 1(b). The dielectric used for these simulations is Si at room temperature with a relative electric permittivity of $\epsilon_r = 11.68$. "Vacuum" indicates that no Si is present in the simulation, while "with pillar" indicates that the $(1.0 \times 1.0 \times 2.0)$-mm^3 support pillar is present. TE_{xyz} indicates the number of half wavelengths spanned by the electric field in the x, y, and z directions, respectively [see Fig 3(c)]. Note that the frequency of the first mode of the upper cavity is approximately 17.2 GHz.

	TE_{110} (GHz)	TE_{120} (GHz)	TE_{210} (GHz)
Vacuum	15.7	24.2	24.2
Vacuum with pillar	13.1	23.6	23.6
Si	13.5	16.8	16.8
Si with pillar	6.3	16.2	16.9

possibility, the pillar is included in the design in order to provide a degree of mechanical support. Note that the pillar can alternatively be realized as a dielectric material, e.g., PTFE; a dielectric pillar would no longer cause field confinement between the top surface of the pillar and the metallic surface of the chip.

III. IMPLEMENTATION

The physical implementation of the main components of the quantum socket is displayed in Fig. 4. In particular, Fig. 4(a) shows a macrophotograph of a three-dimensional wire. The inset shows a scanning electron microscope (SEM) image of the wire contact head, featuring the 500-μm version of the tunnel. This wire is cycled approximately ten times; as a consequence, the center conductor of

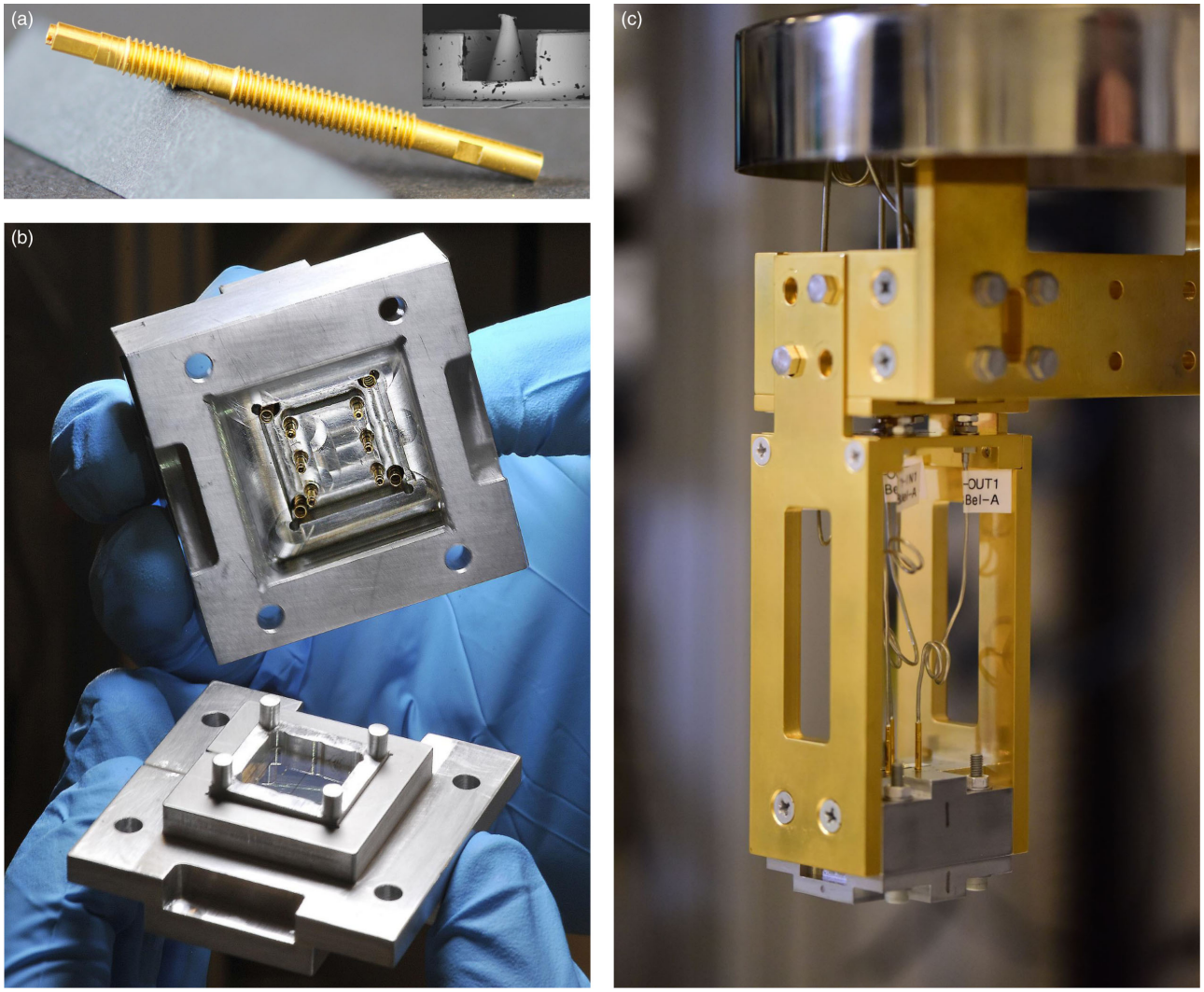

FIG. 4. Images of the quantum socket as implemented. (a) Macrophotograph of a three-dimensional wire. (Inset) SEM image of the contact head. The wire components are machined by means of a high-precision screw-type mill. Note that the tip of the inner conductor retains small metallic flakes that are scraped off the on-chip pads. (b) Microwave package lid with six three-dimensional wires and four washer springs, washer, and sample holder with chip installed. (c) Package holder with attached microwave package mounted to the MC stage of a DR. The lid of a custom-made magnetic shield can be seen at the top of the panel.

the contact head, which had a conical, sharp shape originally, flattens at the top. The metallic components of the wire are made from bronze and brass (see Sec. III A), and all springs from hardened beryllium copper (BeCu). Except for the springs, all of the components are gold plated, without any nickel (Ni) adhesion underlayer.

Figure 4(b) displays the entire microwave package in the process of locking the package lid and sample holder together, with a chip and grounding washer already installed. As shown in the figure, two rows of three-dimensional wires, for a total number of six wires, are screwed into the lid with pressure settings as described in Appendix A; each wire is associated with one on-chip CPW pad. The four springs that mate with the grounding-washer feet are embedded in corresponding recesses in the lid; the springs are glued in these recesses by way of a medium-strength thread locker that is tested at low temperatures. Figure 4(c) shows a picture of the assembled microwave package attached to the package holder; the entire structure is attached to the MC stage of a DR. More details about materials and microwave components can be found in Sec. S2 of the Supplemental Material [47].

A. Magnetic properties

An important stage in the physical implementation of the quantum socket is the choice of materials to be used for the three-dimensional wires. In fact, it has been shown that nonmagnetic components in proximity of superconducting qubits are critical to preserve long qubit coherence [50–53]. The three-dimensional wires are the closest devices to the qubits. For this reason, all of their components should be made using nonmagnetic materials. Because of machining constraints, however, alloys containing ferromagnetic impurities [iron (Fe), cobalt (Co), and Ni] have to be used. For the outer-conductor components, we use brass, which is easy to thread; the chosen type is CW724R [54]. For the inner-conductor components, brass CW724R does not meet the machining requirements. Consequently, we decide to use copper alloy (phosphor bronze) CW453K [55]. The chemical composition for these two materials is reported in Table IV of Appendix B. The dielectric spacers are made from PTFE and the rest of the components from hardened BeCu; both materials are nonmagnetic. The weight percentage of ferromagnetic materials is non-negligible for both CW453K and CW724R. Thus, we perform a series of tests using a zero-Gauss chamber (ZGC) in order to ensure that both materials are sufficiently nonmagnetic. The results are given in Appendix B and show that the magnetic impurities should be small enough not to disturb the operation of superconducting quantum devices.

The microwave package and the grounding washer are made from high-purity Al alloy 5N5 (99.9995% purity). The very low level of impurities in this alloy assures minimal stray magnetic fields generated by the package and the washer, as confirmed by the magnetic tests discussed in Appendix B.

B. Thermal properties

The thermal conductance of the three-dimensional wires is a critical parameter to be analyzed for the interconnection with devices at cryogenic temperatures. Low thermal conductivity would result in poor cooling of the devices, which, in the case of qubits, may lead to an incoherent thermal mixture of the qubit ground state $|g\rangle$ and the excited state $|e\rangle$ [56,57]. Even a slightly mixed state would significantly deteriorate the fidelity of the operations required for QEC [58]. It has been estimated that some of the qubits in the experiment of Ref. [36], which relies solely on Al-wire bonds as a means of thermalization, are characterized by an excited-state population $P_e \simeq 0.04$. Among other possible factors, it is believed that this population is due to the poor thermal conductance of the Al-wire bonds. In fact, these bonds become superconductive at the desired qubit operation temperature of approximately 10 mK, preventing the qubits from thermalizing and, thus, from being initialized in $|g\rangle$ with high fidelity.

In order to compare the thermal performance of an Al-wire bond with that of a three-dimensional wire, we estimate the heat-transfer rate per kelvin of a wire, Π_t, using a simplified coaxial geometry. At a temperature of 25 mK, we calculate $\Pi_t \simeq 6 \times 10^{-7}$ WK^{-1}. At the same temperature, the heat-transfer rate per kelvin of a typical Al-wire bound is estimated to be $\Pi_b \simeq 4 \times 10^{-12}$ WK^{-1} (see Appendix C for more details). A very large number of Al-wire bonds would thus be required to obtain a thermal performance comparable to that of a single three-dimensional wire.

C. Spring characterization

Another critical step in the physical implementation of the quantum socket is to select springs that work at cryogenic temperatures. In fact, the force that a wire applies to a chip depends on these springs. This force, in turn, determines the wire-chip contact resistance, which impacts the socket's dc and, possibly, microwave performance. Among various options, we choose custom springs made from hardened BeCu.

It is noteworthy to mention that the mean number of cycles before mechanical failure for the three-dimensional wires is larger than 200 000 at room temperature (see Appendix D for details); at 10 mK, we are able to use the same wire more than ten times without any mechanical or electrical damage.

To characterize the springs, their compression is assessed at room temperature, in liquid nitrogen (i.e., at a temperature $T \simeq 77$ K) and in liquid helium ($T \simeq 4.2$ K). Note that a spring working at 4.2 K is expected to perform similarly at a temperature of 10 mK. A summary of the

thermomechanical tests is reported in Appendix D. The main conclusion of the tests is that the springs do not break (even after numerous temperature cycles) and have similar spring constants at all measured temperatures.

D. Alignment

In order to implement a quantum socket with excellent interconnectivity properties, it is imperative to minimize machining errors and mitigate the effects of any residual errors. These errors are mainly due to dicing tolerances, tapping tolerances of the M2.5-threaded holes of the lid, tolerances of the mating parts for the inner cavities of the lid and sample holder, and tolerances of the chip recess. These errors can cause both lateral and rotational misalignment and likely become worse when cooling the quantum socket to low temperatures. More details on alignment errors can be found in Appendix E.

The procedure to obtain an ideal and repeatable alignment comprises three main steps: optimization of the contact pad and tunnel geometry, accurate and precise chip dicing, and accurate and precise package machining. For the quantum socket described in this work, the optimal tunnel width is found to be 650 μm. This tunnel width maintains reasonable impedance matching, while allowing greater CPW contact-pad and tapering dimensions. The contact-pad width W_p and taper length T_p are chosen to be $W_p = 320$ μm and $T_p = 360$ μm. These dimensions are the maximum ones allowable for accommodating the geometry of the wire bottom interface for a nominal lateral and rotational misalignment of ∓ 140 μm and $\mp 28°$, respectively. In order to select the given pad dimensions, we had to resort to a 50-Ω matched raised-cosine tapering.

A majority of the chips used in the experiments presented here are diced with a dicing saw from the DISCO Corporation (model DAD3240). To obtain a desired die length, both the precision of the saw-stage movement and the blade's kerf have to be considered. For the DAD3240 saw, the former is approximately 4 μm, whereas the latter changes with usage and materials. For the highest accuracy cut, we measure the kerf on the same type of wafer just prior to cutting the actual die. In order to achieve maximum benefit from the saw, rotational- and lateral-alignment dicing markers are incorporated on the wafer. Such a meticulous chip-dicing procedure is only effective in conjunction with a correspondingly high level of machining accuracy and precision. We used standard computer-numerical-control machining with a tolerance of 1 thou (25.4 μm), although electrical-discharge machining can be pursued if more stringent tolerances ($\lesssim 10$ μm) are required.

Following the aforementioned procedures, we are able to achieve the desired wire-pad matching accuracy and precision, which results in a repeatability of 100% over 94 instances. These figures of merit are tested in two steps: first, by microimaging several pads that are mated to a three-dimensional wire (see Sec. III D 1) and, second, by means of dc-resistance tests (see Sec. III D 2).

1. On-chip pad microimaging

Microimaging is performed on a variety of different samples, four of which are exemplified in Fig. 5. The figure shows a set of microimages for Ag and Al pads (details regarding the fabrication of these samples are available in Appendix F). Figures 5(a) and 5(b) show two Ag pads that are mated with the three-dimensional wires at room temperature. Figure 5(a) shows a mating instance where the wire bottom interface perfectly matches the on-chip pad. Figure 5(b) shows two mating instances that, even though not perfectly matched, remain within the designed tolerances. Notably, simulations of imperfect mating instances revealed that an off-centered wire does not significantly

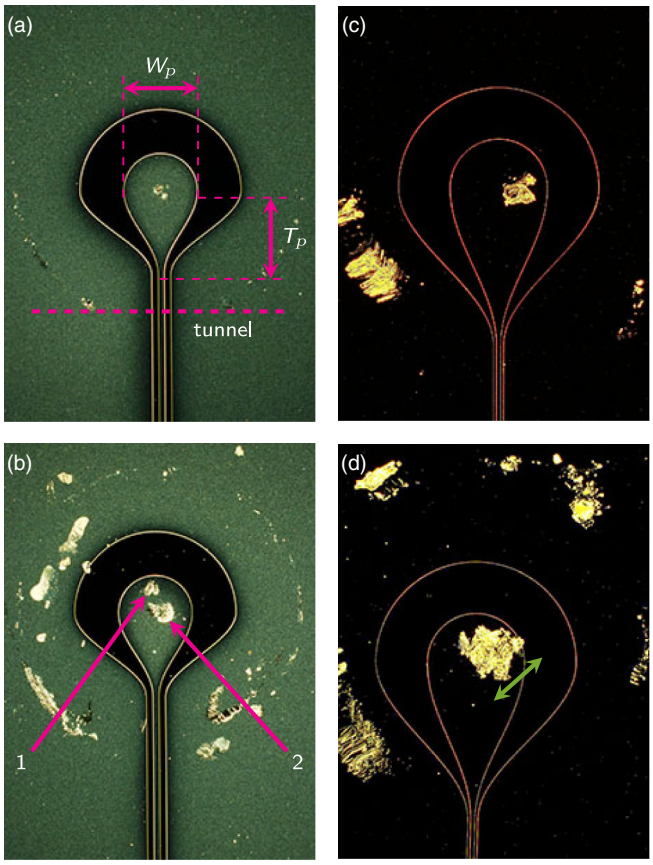

FIG. 5. Microimages used to evaluate the alignment procedure of the three-dimensional wires. (a),(b) Ag pads. The magenta arrows indicate the first (1) and second (2) mating instance. The lengths W_p and T_p are indicated in (a) by means of magenta double arrows. (c),(d) Al pad before and after a cooling cycle to approximately 10 mK. Center conductor dragging due to cooling is indicated by a green double arrow. The magenta (thick) dashed line in (a) indicates tunnel (i.e., rotational) alignment for the Ag pad. Note that the geometries for the pads in (a) and (b) are optimized for a 3-μm Ag film and, thus, are slightly different than those for the pads in (c) and (d), which are designed for a 120-nm Al film.

affect the microwave performance of the quantum socket. Finally, Figs. 5(c) and 5(d) display two Al pads which are both mated with a wire one time. While the pad in Fig. 5(c) is operated only at room temperature, the pad in Fig. 5(d) is part of an assembly that is cooled to approximately 10 mK for about three months. The image is taken after the assembly is cycled back to room temperature and shows a dragging of the wire by a few tens of micrometers. Such a displacement can likely be attributed to the difference in the thermal expansion of Si and Al (see Appendix E).

As a diagnostic tool, microimages of a sample already mounted in the sample holder after a mating cycle can be obtained readily by means of a handheld digital microscope.

2. dc-resistance tests

In contrast to the microimaging tests, which require the removal of the microwave package's lid, dc-resistance tests can be performed *in situ* at room temperature after the package and the package holder have been fully assembled. These tests are performed on all devices presented in this work, including the Au, Ag, and Al samples.

The typical test setup comprises a microwave package with two three-dimensional wires, each mating with an on-chip pad. The two pads are connected by means of a CPW transmission line with series resistance R^t. The back end of the wires is connected to a coaxial cable ending in a microwave connector, similar to the setup in Figs. 1(d) and 4(c). The dc-equivalent circuit of this setup can be represented by way of a four-terminal pi network. The circuit comprises an input i and output o terminal, two terminals connected to a common ground g, an input-output resistor with resistance R_{io}, and two resistors to ground with resistance R_{ig} and R_{og}. The i and o terminals correspond to the inner conductor of the two microwave connectors. The outer conductor of both connectors is grounded.

The resistance R_{io} is that of the center conductor of the CPW transmission line, including the contact resistance R^c for each wire-pad interface and the series resistance R^{wc} of the wire and coaxial cable's inner conductor, $R_{io} = R^t + 2(R^c + R^{wc})$. The resistances R_{ig} and R_{og} are those of the path between each center conductor and the ground and include the resistance of the inner and outer conductors of the various coaxial cables and wires, as well as any wire-pad contact resistance. Ideally, these ground resistances should be open circuits. In reality, they are expected to have a finite but large value because of the intrinsic resistance of the Si wafers used as a substrate.

The design parameters, the electrical properties, and the measurement conditions, as well as the measured values of R_{io}, R_{ig}, and R_{og} for various Au, Ag, and Al samples are reported in Table II. Measuring resistances significantly different from the expected values means that either a lateral or a rotational misalignment occurs. The resistances for some Au samples are also measured at 77 K to verify whether a good room-temperature alignment persists in cryogenic conditions. The cold measurements are realized by dunking the package holder into liquid nitrogen. Note that one chip with a sapphire substrate and Al conductors is also measured; in this case, both R_{ig} and R_{og} are larger than 500 MΩ. Notably, we find a 100% correlation between a successful dc test at room temperature and a microwave measurement at 10 mK.

The measured value of R_{io} for the Ag samples is larger than the estimated trace resistance by approximately

TABLE II. dc-resistance tests. Multiple Au samples are measured. For all samples, the length from the center of one pad to that of the opposite pad of the CPW center conductor is $L_{pp} = 11.5$ mm. The table reports the width W of each CPW transmission line; the thickness d of the metal; the metal-volume resistivity ρ at room temperature or at 77 K; the input- and output-wire pressure settings ℓ^i_p and ℓ^o_p, respectively; the operating temperature T; the number of measurements N; the estimated trace resistance R^t [for the Au samples, the very large parallel resistance of approximately 46 kΩ at room temperature due to the titanium (Ti) adhesion layer is neglected]; the measured resistances R_{io}, R_{ig}, and R_{og}. For a given chip, each resistance is measured independently N times under similar measurement conditions. The mean values and standard deviations of R_{io} are provided; the minimum values of R_{ig} and R_{og} are given. Note that because $R^c + R^{wc} \ll R^t$, we expect $R_{io} \approx R^t$. The discrepancy between the estimated and measured values (R^t and R_{io}) for the Au and Al samples is mainly due to uncertainties associated with the metal thickness d. The inaccuracies are smaller for thicker films, as in the case of the 3-μm Ag samples.

Metal	W (μm)	d (nm)	ρ (1×10^{-9} Ω m)	ℓ^i_p (mm)	ℓ^o_p (mm)	T (K)	N	R^t (Ω)	R_{io} (Ω)	R_{ig} (MΩ)	R_{og} (MΩ)
Au	10	100	22	4.52	4.44	300	30	253	218(3)	31	31
Au	10	100	22	4.97	4.89	300	2	253	223(0)	38	38
Au	10	100	22	4.18	4.11	300	2	253	217(0)	39	39
Au	10	100	22	4.57	4.45	300	2	253	229(0)	28.8	28.6
Au	10	200	22	4.60	4.70	300	10	126.5	98.0(7)	50	50
Au	10	200	4.55	4.60[a]	4.70[a]	77	6	26.16	36.02(2)	77.3	81.8
Ag	30	3000	16	4.60	4.70	300	6	2.04	2.71(4)	0.0043	0.0043
Al	15	120	26	4.25	4.07	300	24	166.1	171(1)	0.0042	0.0042

[a]At 300 K.

650 mΩ. This simple result makes it possible to find an upper-bound value for the contact resistance, $R^c \lesssim 325\,\mathrm{m\Omega}$. A more accurate estimate of the contact resistance based on four-point measurements is described in Sec. IV A.

The dc-resistance testing procedure presented here will be useful in integrated-circuit quantum-information processing, where, for example, CPW transmission lines can serve as qubit-readout lines [34–36]. These tests can be expanded to encompass different circuit structures such as the qubit control lines utilized in Ref. [36].

IV. CHARACTERIZATION

The three-dimensional wires are multipurpose interconnects that can be used to transmit signals over a wide frequency range, from dc to 10 GHz. These signals can be the current bias used to tune the transition frequency of a superconducting qubit; the Gaussian-modulated sinusoidal or the rectangular pulses that, respectively, make it possible to perform XY and Z control on a qubit; the continuous monochromatic microwave tones used to read out a qubit state or to populate and measure a superconducting resonator [2,34,36,53]. In general, the wires can be used to transmit any baseband-modulated carrier signal within the specified frequency spectrum, at room and cryogenic temperatures. In this section, we report experimental results for a series of measurements aiming at a complete electrical characterization of the quantum socket at room temperature and at approximately 77 K (i.e., in liquid nitrogen).

A. Four-point measurements

The wire-pad contact resistance R^c is an important property of the quantum socket. In fact, a large R^c would result in significant heating when applying dc-bias signals and rectangular pulses, thus deteriorating the qubit performance.

In order to assess R^c for the inner and outer conductors of a three-dimensional wire, we perform four-point measurements using the setup shown in the inset of Fig. 6. Using this setup, we are able to measure both the series resistance of the wire R^w and the contact resistance R^c.

The setup comprises a microwave package with a chip entirely coated with a 120-nm-thick Al film; no grounding washer is used. The package features three three-dimensional wires, of which two are actually measured; the third wire is included to provide mechanical stability. The package is attached to the MC stage of a DR and measured at room temperature by means of a precision source-measure unit; see details in Sec. S2 of the Supplemental Material [47].

We measure the resistance between the inner conductor of a wire and the ground, R_{ig}. This resistance comprises the inner-conductor wire resistance R_i^w in series with the inner-conductor contact resistance R_i^c and any resistance to ground, R_g. Note that, at the operation temperature of the experiment (approximately 10 mK), Al is superconducting, and thus the metal resistance can be neglected.

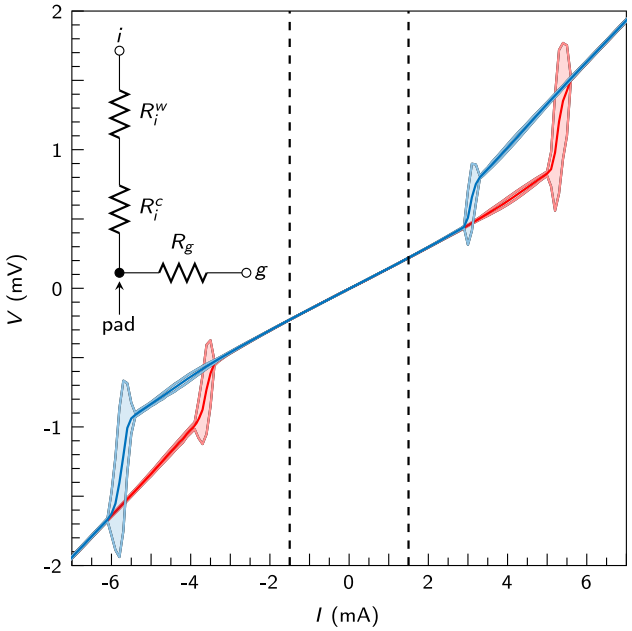

FIG. 6. I-V characteristic curve for R_{ig}. The sweeps are conducted by both increasing (red) and decreasing (blue) the applied current between −7 and +7 mA. The shaded region indicates two standard deviations. The dashed lines indicate the region (∓1.5 mA) for which the resistance value is found using linear regression. The origin of the hystereses is explained in the text. (Inset) Circuit diagram of the measurement setup, including all resistors, measured by means of the four-point measurement. The position of the pad is indicated by an arrow.

Figure 6 shows the current-voltage (I-V) characteristic curve for R_{ig}. With increasing bias currents, the contact resistance results in hot-spot generation leading to a local breakdown of superconductivity. For sufficiently high bias currents, superconductivity breaks down completely. At such currents, the observed hysteretic behavior indicates the thermal limitations of our setup. Note, however, that these currents are at least one order of magnitude larger than the largest bias current required in typical superconducting qubit experiments [59].

In order to estimate R_{ig} from the I-V characteristic curve, we select the bias-current region from −1.5 to +1.5 mA and fit the corresponding slope. We obtain $R_{ig} \simeq 148\,\mathrm{m\Omega}$. This value, which represents an upper bound for the wire resistance and the wire-pad contact resistance, $(R_i^w + R_i^c)$, is significantly larger than that associated with Al-wire bonds [60] or indium-bump bonds [9]. In future versions of the three-dimensional wires, we will attempt to reduce the wire-pad contact resistance by rounding the tip of the center conductor, stiffening the wire springs, using a thicker metal film for the pads, depositing Au or titanium nitride (TiN) on the pads, and plating the wires with TiN. We note, however, that even a large value of the wire and/or wire-pad contact

resistance does not significantly impair the quantum-socket microwave performance; for example, the quantum architecture in Ref. [11] would be mostly unaffected by the contact resistance of our three-dimensional wires.

B. Two-port scattering parameters

The two-port scattering parameter (S-parameter) measurements of a bare three-dimensional wire are realized by means of the setup shown in the inset of Fig. 7(a) and are described in detail in Sec. S2 of the Supplemental Material [47]. The device under test (DUT) comprises a cable assembly attached to a three-dimensional wire by means of a screw-in microconnector. The bottom interface of the wire is connected to a 2.92-mm end-launch connector, which is characterized by a flush coaxial back plane; this plane mates with the wire bottom interface well enough to allow for S-parameter measurements up to 10 GHz. In order to measure the S parameters of the DUT, we use a vector network analyzer (VNA) and perform a two-tier calibration (see the Supplemental Material [47]), which makes it possible to set the measurement planes to the ports of the DUT.

The magnitudes of the measured reflection and transmission S parameters are displayed in Fig. 7(a). We perform microwave simulations of a three-dimensional wire for the same S parameters (see Sec. II D for the electric field distribution), the results of which are plotted in Fig. 7(b). The S parameters are measured and simulated between 10 MHz and 10 GHz. The S parameters $|S_{21}|$ and $|S_{12}|$ show a featureless microwave response, similar to that of a coaxial transmission line. The attenuation at 6 GHz is $|S_{21}| \simeq -0.58$ dB, and the magnitude of the reflection coefficients at the same frequency is $|S_{11}| \simeq -13.8$ dB and $|S_{22}| \simeq -14.0$ dB. The phase of the various S parameters (not shown) behaves as expected for a coaxial transmission line. All measurements are performed at room temperature.

The S-parameter measurements of a three-dimensional wire indicate a very good microwave performance. However, these measurements alone are insufficient to fully characterize the quantum-socket operation. A critical feature that deserves special attention is the 90° transition region between the wire bottom interface and the on-chip CPW pad. It is well known that 90° transitions can cause significant impedance mismatch and, thus, signal reflection [48]. In quantum-computing applications, these reflections could degrade both the qubit control and the readout fidelity.

Figure 8 shows a typical setup for the characterization of a wiring configuration analogous to that used for qubit operations (see Sec. S2 of the Supplemental Material for details [47]). The setup comprises a DUT with ports 1 and 2 connected to a VNA; the DUT incorporates a microwave package with a pair of three-dimensional wires, which address one CPW transmission line on an Au or Ag chip. The microwave package is attached to the package holder, as described in Secs. II C and III [see also Figs. 1(d) and 4(c)]. The transmission-line geometrical dimensions

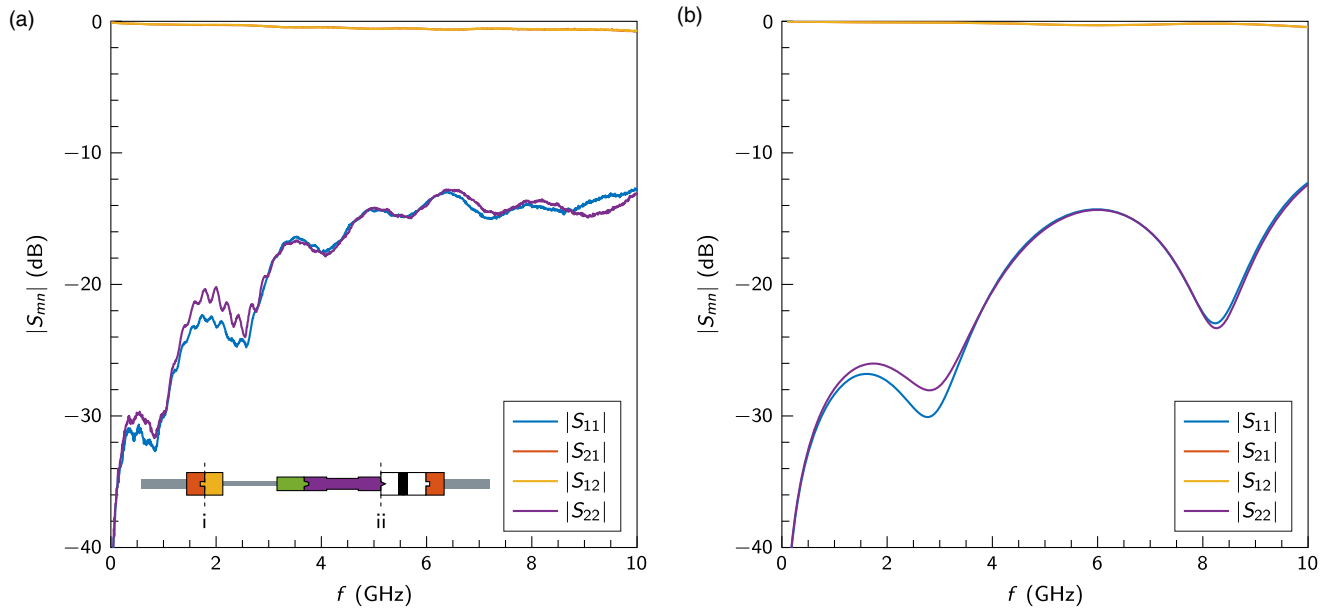

FIG. 7. S-parameter measurements and simulations for a three-dimensional wire at room temperature. (a) Magnitude of the measured S parameters $|S_{mn}|$, with $m, n = \{1, 2\}$. (Inset) Image of the measurement setup. Moving from left to right, find a segment of the flexible coaxial cable (gray); a subminiature type A (SMA) female connector (red); after plane i, an SMA male connector (orange); a segment of semirigid coaxial-cable EZ 47 cable (gray; see the Supplemental Material [47]); a screw-in microconnector (green); a three-dimensional wire (purple); after plane ii, a 2.92-mm end-launch connector (white and black); an SMA female connector (red); a segment of flexible coaxial cable (gray). (b) S-parameter simulations. The lower attenuation is due to idealized material properties and connections.

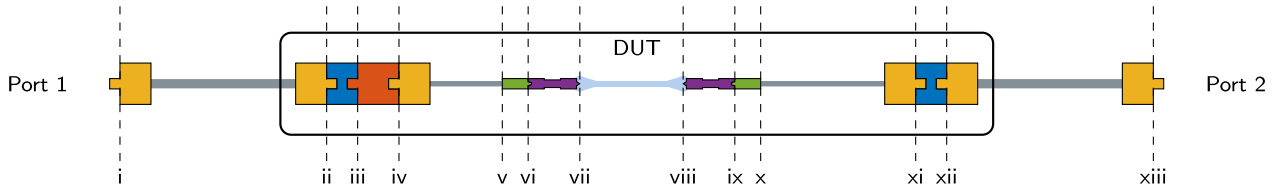

FIG. 8. Microwave-characterization setup. The vertical dashed lines indicate the main reflection planes. The yellow terminations correspond to SMA male connectors at the end of each cable. The input (output) flexible cable corresponds to the region between planes i and ii (xii and xiii), in gray; the blue blocks correspond to SMA female bulkhead adapters; the plane ii (xii) corresponds to the input (output) port of the DUT; the orange block corresponds to an SMA male to SMA female adapter; the EZ 47 input (output) cable corresponds to the region between planes iv and v (x and xi), in gray; the plane v (x) corresponds to the solder connection on the three-dimensional wire; the plane vi (ix) is associated with the screw-in microconnector; the plane vii (viii) corresponds to the 90° interface connecting each three-dimensional wire to the input (output) of the CPW transmission line (pale blue). The three-dimensional wires are indicated in purple.

and the wire pressure settings are reported in Table II; only the 200-nm Au samples and the Ag samples are characterized at microwave frequencies. The back end of each three-dimensional wire is connected to one end of an EZ 47 cable by means of the screw-in microconnector described in Sec. II C; the other end of the EZ 47 cable is soldered to an SMA male connector. A calibration is performed for all measurements.

We perform a two-port S-parameter measurement of the DUT from 10 MHz to 10 GHz. The measurement results at room temperature for the Au and Ag samples are shown in Figs. 9(a) and 10(a), respectively. The results for the Au sample at 77 K are shown in Fig. 9(b).

The S-parameter measurements of the Au sample show that the quantum socket functions well at microwave frequencies, both at room temperature and at 77 K. Since most of the mechanical shifts have already occurred when we cool to 77 K [61], this measurement allows us to deduce that the socket will continue functioning even at lower temperatures (e.g., at approximately 10 mK). The Au sample, however, is characterized by a large value of R_{io}, which may conceal unwanted features both in the

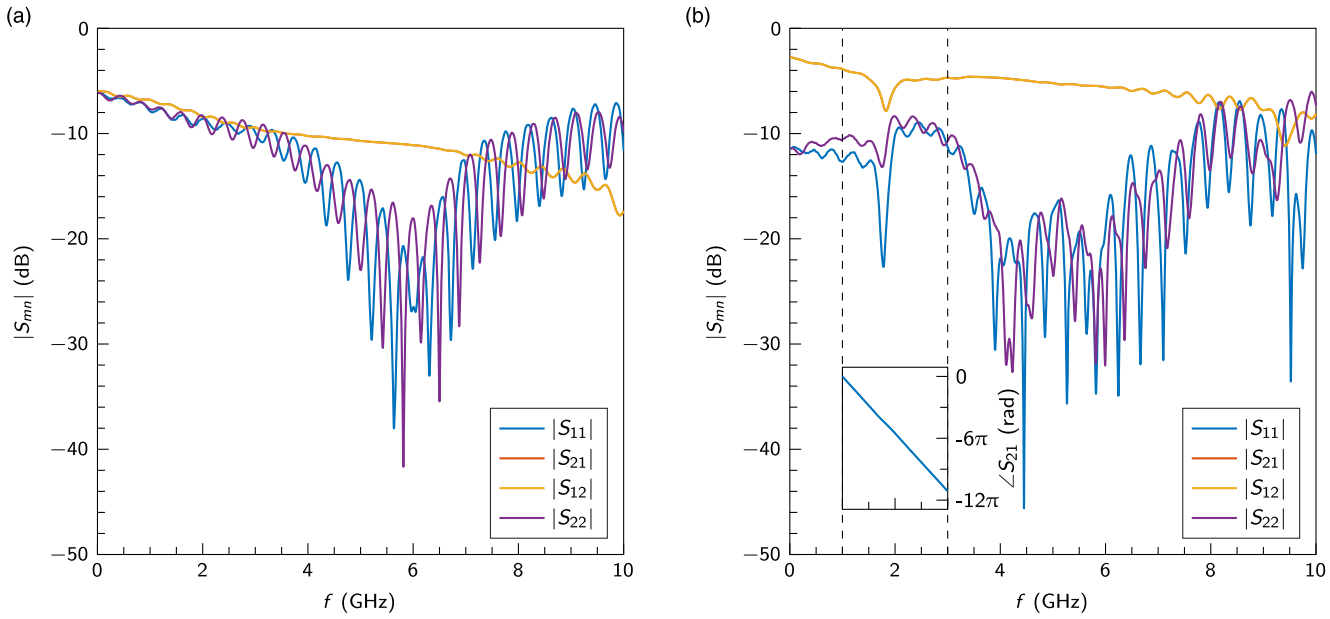

FIG. 9. S-parameter measurements for the Au sample. (a) $|S_{mn}|$ at room temperature. (b) $|S_{mn}|$ at 77 K. The transmission coefficients show that the DUT is a reciprocal device (i.e., $S_{21} \simeq S_{12}$), as expected for a passive structure. The inset in (b) shows the unwrapped phase angle $\angle S_{21}$; the dashed lines delimit the frequency region between 1 and 3 GHz. Note that the reflection coefficients S_{11} and S_{22} are relatively large at very low frequencies. This result is expected for a very lossy transmission line. In fact, the center conductor for the Au sample is characterized by a series resistance $R_{io} \simeq 98\ \Omega$ at room temperature (see Table II), which corresponds to $S_{11} \sim S_{22} \simeq -6$ dB at 10 MHz, and $R_{io} \simeq 36\ \Omega$ at 77 K, which corresponds to $S_{11} \sim S_{22} \simeq -12$ dB at 10 MHz. These findings are consistent with the time-domain results shown in Fig. 11, where the large impedance steps are also due to the large series resistance (see Sec. IV C). The low-loss Ag sample shows much lower reflection coefficients at low frequencies (cf. Fig. 10), whereas the lossy Al sample shows high reflections at low frequencies and at room temperature [cf. Fig. 15(a) in Sec. V].

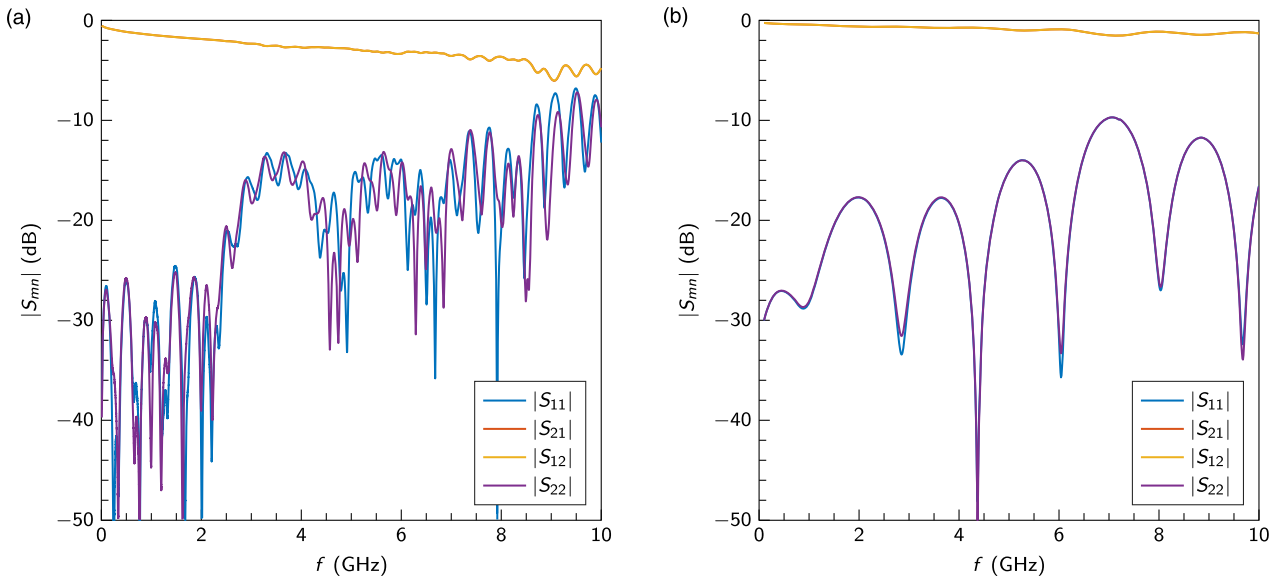

FIG. 10. S-parameter measurements for the Ag sample. (a) $|S_{mn}|$ measurement at room temperature. (b) $|S_{mn}|$ microwave simulation. Note that the attenuation for the measured data is larger than that in the simulation because the latter does not include the EZ 47 cables used in the DUT of Fig. 8.

transmission and reflection measurements. Therefore, we prepare an Ag sample that exhibits a much lower resistance even at room temperature. The behavior of the Ag S parameters is similar to that of a transmission line or a coaxial connector. For example, $|S_{11}|$ is approximately -15 dB; as a reference, for a high-precision SMA connector at the same frequency, $|S_{11}| \simeq -30$ dB.

The presence of the screw-in microconnector can occasionally deteriorate the microwave performance of the quantum socket. In fact, if the microconnector is not firmly tightened, a dip in the microwave transmission is observed. At room temperature, it is straightforward to remove the dip by simply retightening the connector when required. On the contrary, for the measurements at 77 K and for any other application in a cryogenic environment, assuring that the microconnector is properly torqued at all times can be challenging. Figure 9(b), for example, shows the S parameters for an Au sample measured at 77 K. A microwave dip appears at approximately 1.8 GHz, with a 3 dB bandwidth of approximately 200 MHz. The inset in Fig. 9(b) displays the phase angle of S_{21} between 1 and 3 GHz, showing that the dip is unlikely to be a Lorentzian-type resonance (more details are in Sec. S4 of the Supplemental Material [47]). Note that the dip is far from the typical operation frequencies for superconducting qubits. Additionally, as briefly described in Sec. VI, we will remove the screw-in microconnector from future generations of the three-dimensional wires.

Figure 10(b) shows a simulation of the S parameters for the Ag sample, for the same frequency range as the actual measurements. While there are visible discrepancies between the measured and simulated S parameters, the latter capture well some of the characteristic features of the microwave response of the DUT. In particular, the measured and simulated reflection coefficients display a similar frequency dependence. It is worth mentioning that we also simulated the case where the wire bottom interface is not perfectly aligned with the on-chip pad (results not shown). We consider lateral misalignments of 100 μm and rotational misalignments of approximately 20°. This approach allows us to study more realistic scenarios, such as those shown in Fig. 5. We find that the departure between the misaligned and the perfectly aligned simulations is marginal. For example, the transmission S parameters vary only by approximately ∓ 0.5 dB.

In Appendix G, we show a set of microwave parameters obtained from the measured S parameters for the Au sample at room temperature and at 77 K and for the Ag sample at room temperature. These parameters make it possible to characterize the input and output impedance as well as the dispersion properties of the quantum socket.

C. Time-domain reflectometry

In time-domain-reflectometry (TDR) measurements, a rectangular pulse with a fast rise time and a fixed length is applied to a DUT; the reflections (and all re-reflections) due to all reflection planes in the system (i.e., connectors, geometrical changes, etc.) are then measured by way of a fast electrical sampling module. The reflections are, in turn, related to the impedances of all of the system components. Thus, TDR makes it possible to estimate any impedance mismatch and its approximate spatial location in the system.

TDR measurements are performed on the DUT shown in Fig. 8, with the same Au or Ag sample as in the

measurements in Sec. IV B. As always, the Au sample is measured both at room temperature and at 77 K, whereas the Ag sample is measured only at room temperature. The TDR setup is analogous to that used in the S-parameter measurements, with the following differences: the DUT input and output reference planes are extended from planes ii and xii to planes i and xiii of Fig. 8; also, when testing the DUT input port, the output port is terminated in a load with impedance $Z_L = Z_c$, and vice versa when testing the DUT output port. The TDR measurements are realized by means of a sampling oscilloscope, with key features reported in Sec. S2 of the Supplemental Material [47]. The voltage reflected by the DUT, V^-, is acquired as a function of time t by means of the oscilloscope. The time t is the round-trip interval necessary for the voltage pulse to reach a DUT reflection plane and return back to the oscilloscope. The measured quantity is given by [62]

$$V_{\mathrm{meas}}(t) = V^+(t) + V^-(t), \tag{2}$$

where V^+ is the amplitude of the incident-voltage square wave. From Eq. (2), we can obtain the first-order instantaneous impedance as [63]

$$Z(t) = Z_c \frac{1+\xi(t)}{1-\xi(t)}, \tag{3}$$

where $\xi(t) = [V_{\mathrm{meas}}(t) - V^+]/V^+$.

Figure 11 shows $Z(t)$ for the DUT with the Au sample at room temperature and at 77 K; the measurement refers to the input port of the DUT, i.e., plane i in Fig. 8. The inset shows the room-temperature data for a shorter time interval. This time interval corresponds to a space interval beginning at a point between planes iv and v and ending at a point between planes vii and viii in Fig. 8.

Figure 12(a) shows $Z(t)$ for the Ag sample at room temperature. Figure 12(b) displays the data in (a) for a time interval corresponding to a space interval beginning at a point between planes iv and v and ending at a point between planes x and xi in Fig. 8; as a reference, the Au data are overlaid with the Ag data.

For the Au sample, the first main reflection plane (plane ii) is encountered at $t \simeq 18$ ns. The second main reflection plane (plane v) appears after approximately 2.5 ns relative to the first plane, at $t \simeq 20.5$ ns. From that time instant and for a span of approximately 250 ps, the TDR measurement corresponds to $Z(t)$ of the three-dimensional wire itself. The maximum impedance mismatch between the EZ 47 coaxial cable and the three-dimensional wire is approximately 10 Ω. The third main reflection plane (plane vii) corresponds to the 90° transition region; for the Au sample, it is impossible to identify features beyond this plane owing to the large series resistance of the on-chip CPW transmission line. From empirical evidence, the impedance $Z(t)$ of a lossy line with series resistivity ρ increases linearly

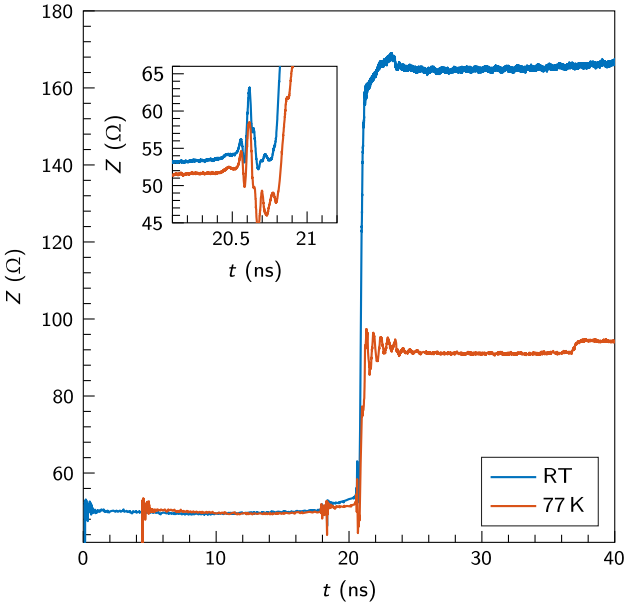

FIG. 11. TDR measurements for the Au sample at room temperature [(RT), blue curve] and at 77 K (red curve). (Inset) Room-temperature data associated with part of the EZ 47 cable, the input three-dimensional wire, and part of the CPW transmission line.

with the length of the line L as $\rho L/(Wd)$. In fact, for the Au sample, we measured an impedance step across the CPW transmission line of approximately 100 Ω at room temperature and 40 Ω at 77 K. These steps are approximately the R_{io} values reported in Table II.

In order to obtain a detailed measurement of the impedance mismatch beyond the 90° transition region, we resort to the TDR measurements of the DUT with the much less resistive Ag sample. First, we confirm that the $Z(t)$ of the input three-dimensional wire for the Ag sample is consistent with the TDR measurements of the Au sample; this consistency is readily verified by inspecting Fig. 12(b). The three-dimensional wire is the structure ending at the onset of the large impedance step shown by the Au overlaid data. The structure spanning the time interval from $t \simeq 20.75$ ns to $t \simeq 21$ ns is associated with the input transition region, the CPW transmission line, and the output transition region. The output three-dimensional wire starts at $t \simeq 21$ ns, followed by the EZ 47 coaxial cable, which finally ends at the SMA bulkhead adapter at $t \simeq 23.5$ ns. The maximum impedance mismatch associated with the transition regions and the CPW transmission line is approximately 5 Ω. Notably, this mismatch is smaller than the mismatch between the three-dimensional wire and the coaxial cable. This result is important. In fact, while it would be hard to diminish the impedance mismatch due to the transition region, it is feasible to minimize the wire mismatch by creating accurate lumped-element models of the wire and use them to minimize stray capacitances and/or inductances [64].

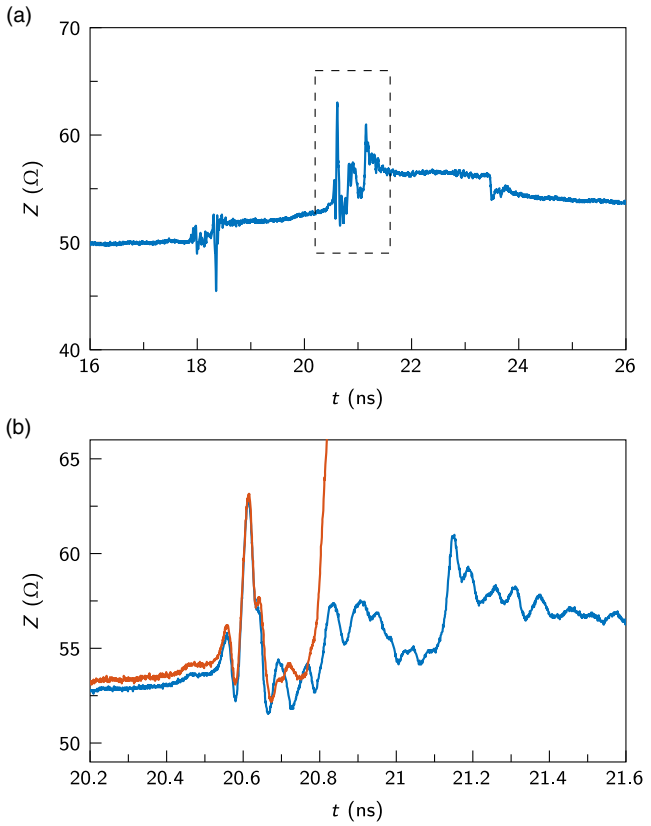

FIG. 12. TDR measurement for the Ag sample at room temperature. (a) Measurement of port 1 of the setup in Fig. 8. (b) Enlargement of (a) addressing the three-dimensional wire and the 90° transition region between the wire and the CPW transmission line (blue). The room-temperature Au data (red) are also displayed as a reference.

It is worth comparing $Z(t)$ of the quantum socket with that of a standard package for superconducting qubits, where wire bonds are used to make interconnections between a printed circuit board and the control and measurement lines of a qubit on a chip. A detailed study of the impedance mismatch associated with wire bonds is found in Ref. [37], where the authors have shown that a long wire bond (of a length between approximately 1 and 1.5 mm: the typical length in most applications) can lead to an impedance mismatch larger than 15 Ω (see Fig. S3 in the supplementary information of Ref. [37]); on the contrary, a short wire bond (of a length between approximately 0.3 and 0.5 mm that is less typical and more challenging to realize) results in a much smaller mismatch, approximately 2 Ω. In terms of impedance mismatch, the current implementation of the quantum socket, which is limited by the mismatch of the three-dimensional wires, lies between these two extreme scenarios.

D. Signal cross talk

Cross talk is a phenomenon where a signal being transmitted through a channel generates an undesired signal in a different channel. Interchannel isolation is the figure of merit that quantifies signal cross talk and that has to be maximized to improve signal integrity. Cross talk can be particularly large in systems operating at microwave frequencies, where, if not properly designed, physically adjacent channels can be significantly affected by coupling capacitances and/or inductances. In quantum-computing implementations based on superconducting quantum circuits, signal cross talk due to wire bonds has been identified to be an important source of errors, and methods to mitigate it have been developed [43,65,66]. However, cross talk remains an open challenge and isolations (the opposite of cross talk) lower than 20 dB are routinely observed when using wire bonds [67]. The coaxial design of the three-dimensional wires represents an advantage over wire bonds. The latter, being open structures, radiate more electromagnetic energy that is transferred to adjacent circuits. The former, being enclosed by the outer conductor, limit cross talk due to electromagnetic radiation.

In realistic applications of the quantum socket, the three-dimensional wires must land in close proximity to several on-chip transmission lines. In order to study interchannel isolation in such scenarios, we design a special device comprising a pair of CPW transmission lines, as shown in the inset of Fig. 13(a). One transmission line connects two three-dimensional wires (ports 1 and 2), exactly as for the devices studied in Secs. IV B and IV C; the other line, which also connects two three-dimensional wires (ports 3 and 4), circumvents the wire at port 1 by means of a CPW semicircle. The distance between the semicircle and the wire outer conductor is designed to be as short as possible, approximately 100 μm.

The chip employed for the cross-talk tests is similar to the Ag sample used for the quantum-socket microwave characterization and is part of a DUT analogous to that shown in Fig. 8. The dc resistances of the center trace of the 1-2 and 3-4 transmission lines are measured and found to be approximately 2.8 and 4.5 Ω, respectively (note that the 3-4 transmission line is approximately 18.0 mm long—hence the larger resistance). All dc resistances to the ground and between the two transmission lines are found to be on the order of a few kilohms, demonstrating the absence of undesired short-circuit paths. A four-port calibration and a measurement of the DUT are conducted by means of a VNA (see Sec. S2 of the Supplemental Material for details [47]). Among the 16 S parameters, Fig. 13(a) shows the magnitude of the transmission coefficients S_{21} and S_{43}, along with the magnitude of the cross-talk coefficients S_{31}, S_{41}, S_{32}, and S_{42}.

The results show that the isolation in the typical qubit operation bandwidth, between 4 and 8 GHz, is larger than approximately 45 dB. Note that the cross-talk coefficients shown in Fig. 13(a) include attenuation, owing to the series resistance of the Ag transmission lines. The actual

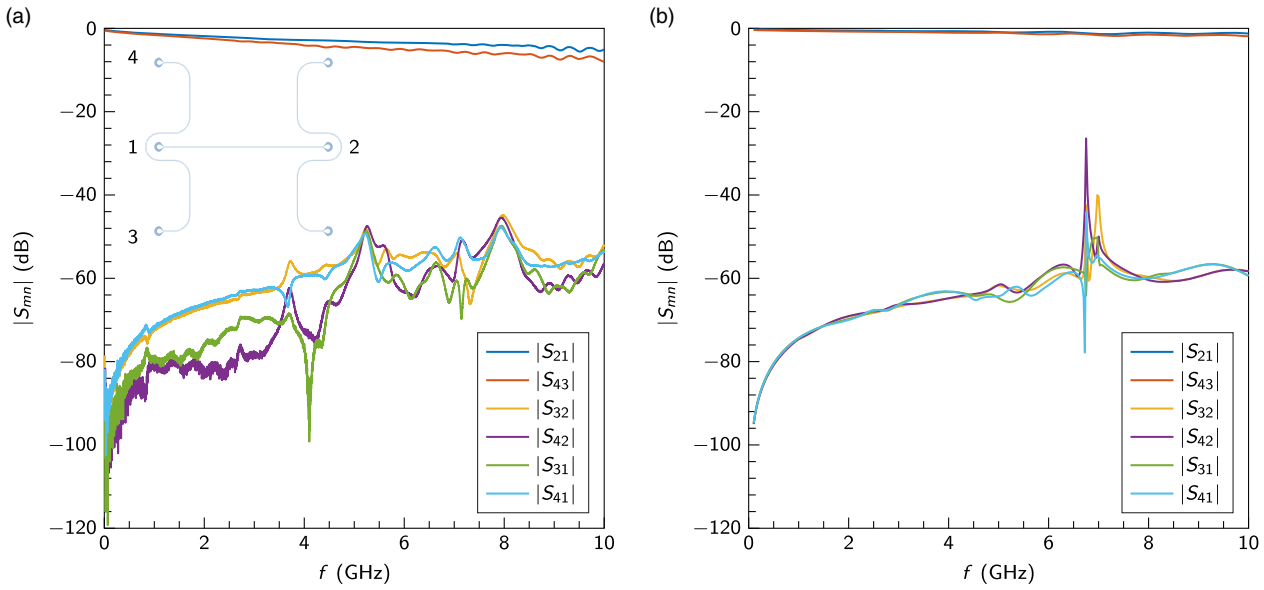

FIG. 13. Signal cross talk. (a) Transmission and cross-talk coefficients for the Ag sample shown in the inset. The numbers adjacent to the pads in the inset correspond to the device ports. Reciprocal and reflection S parameters are not shown. (b) Microwave simulation of the same device. The origin of the peaks at approximately 7 GHz is explained in the text.

isolation, due only to spurious coupling, would thus be smaller by a few decibels.

Figure 13(b) shows the microwave simulations of the cross-talk coefficients, which agree reasonably well with the experimental results. These simulations are based on the models explained in Sec. II D. From simulations, we believe the isolation is limited by the cross talk between the CPW transmission lines, instead of the three-dimensional wires. Note that the peaks at approximately 7 GHz correspond to an enhanced cross talk due to a box mode in the microwave package. The peaks appear in the simulations, which are made for a highly conductive package, and may appear in measurements performed below approximately 1 K, when the Al package becomes superconductive. For the room-temperature measurements shown in Fig. 13(a), these peaks are smeared out due to the highly lossy Al package.

V. APPLICATIONS TO SUPERCONDUCTING RESONATORS

Thus far, we have shown a detailed characterization of the quantum socket in dc and at microwave frequencies, both at room temperature and at 77 K. In order to demonstrate the quantum socket operation in a realistic quantum computing scenario, we use a socket to wire a set of superconducting CPW resonators cooled to approximately 10 mK in a DR. We are able to show an excellent performance in the frequency range from 4 to 8 GHz, which is the bandwidth of our measurement apparatus. Multiple chips are measured over multiple cycles using the same quantum socket, which demonstrates the high level of repeatability of our wiring method. We measure five Al-on-Si samples, as well as one Al–on–gallium-arsenide (GaAs) sample [68] (data not shown) and one Al-on-sapphire sample. The Al-on-sapphire device in particular, features a few resonators with a quality factor comparable to the state of the art in the literature [53], both at high and low excitation power.

The experimental setup is described in Sec. S2 of the Supplemental Material and shown in Fig. S1 [47]. Figure 14 shows a macrophotograph of a (15×15)-mm^2 chip housed in the sample holder; the chip is the Al-on-Si sample described in Sec. III D, with geometrical and dc electrical parameters reported in Table II. The sample comprises a set of three CPW transmission lines, each connecting a pair of three-dimensional wire pads; multiple shunted CPW resonators are coupled to each transmission line. In this section, we focus only on transmission line 3 and its five resonators. The transmission line has a center conductor width of 15 μm and a gap width of 9 μm, resulting in a characteristic impedance of approximately 50 Ω. The resonators are $(\lambda/4)$-wave resonators, each characterized by a center conductor of width W and a dielectric gap of width G. The open end of the resonators runs parallel to the transmission line for a length ℓ_κ, providing a capacitive coupling; a 5-μm ground section separates the gaps of the transmission line and the resonators (see Fig. S3 in Sec. S5 of the Supplemental Material [47]). The nominal resonance frequency $\tilde{f}_0$ as well as all of the other resonator parameters are reported in Table III.

A typical DR experiment employing the quantum socket consists of the following steps. First, the chip is mounted in

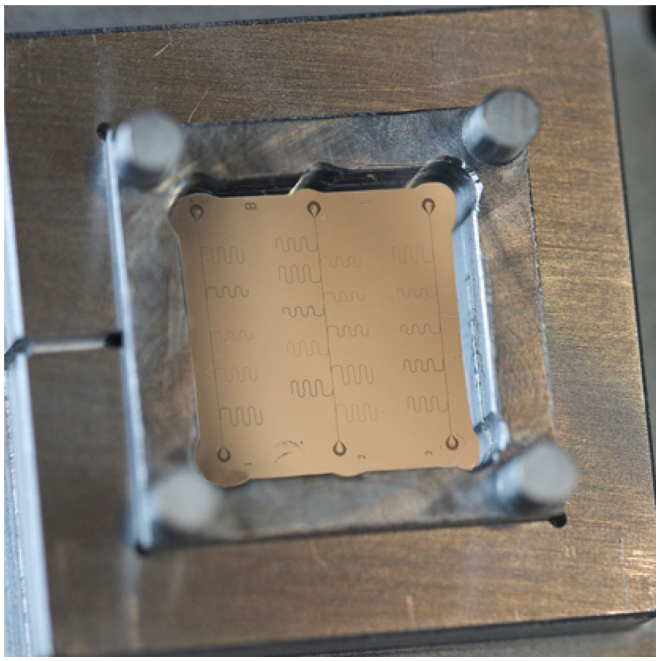

FIG. 14. Macrophotograph of an Al chip on a Si substrate mounted in a sample holder with a grounding washer. The image shows three CPW transmission lines, each coupled to a set of ($\lambda/4$)-wave resonators. The grounding washer, with its four protruding feet, is placed above the chip covering the chip edges. The marks imprinted by the bottom interface of the three-dimensional wires on the Al pads are noticeable. More detailed images of these marks are shown in Fig. 5. This chip and similar other chips with analogous microwave structures and geometries, including one Al-on-GaAs sample as well as one Al-on-sapphire sample, are used in the measurements at approximately 10 mK in the DR.

the microwave package, which has already been attached to the package holder (see Secs. II C and III). Second, a series of dc tests is performed at room temperature. The results for a few Al-on-Si samples are reported in Table II. Third, the package-holder assembly is characterized at room temperature by measuring its S parameters. The results of such a measurement are shown in Fig. 15(a). Fourth, the package holder is mounted by means of the SMP connectors to the MC stage of the DR, and an S_{21} measurement is performed. The results (magnitude only) are shown in Fig. 15(b) in the frequency range between 10 MHz and 10 GHz. Fifth, the various magnetic and radiation shields of the DR are closed and the DR is cooled down. Sixth, during cooldown, the S_{21} measurement is repeated first at approximately 3 K, then at the DR base temperature of approximately 10 mK. The results are shown in Figs. 15(b) and 15(c), respectively. At approximately 3 K, we note the appearance of a shallow dip at approximately 5.7 GHz, probably due to a screw-in microconnector becoming sightly loose during cooling (see Sec. IV B). It is important to mention that in the next generation of three-dimensional wires we will eliminate the screw-in microconnector since we believe we have found a technique to overcome the soldering issues detailed in Sec. II C (see Sec. VI for a brief description). At the base temperature, all five resonators are clearly distinguishable as sharp dips on the relatively flat microwave background of the measurement network. We then select a narrower frequency range around each resonator and make a finer S_{21} measurement. For example, Fig. 15(d) shows the magnitude and the phase of the resonance dip associated with resonator 2.

TABLE III. Resonator parameters. The measured resonance frequency is f_0. The rescaled coupling and internal quality factors Q_c^* and Q_i, respectively, are obtained from the fits of the measured transmission coefficients (see the text for details). These quality factors are measured at a high resonator excitation power, corresponding to $\langle n_{\rm ph}\rangle > 10^5$.

i	$\tilde{f}_0$ (MHz)	f_0 (MHz)	W (μm)	G (μm)	ℓ_κ (μm)	Q_c^*	Q_i
1	4600.0	4673.2	8	5	400	5012	21 243
2	5000.0	5064.5	15	9	300	16 002	165 790
3	5800.0	5872.9	25	15	400	10 269	47 165
4	7000.0	7091.7	15	9	300	6230	54 894
5	7400.0	7520.1	8	5	400	4173	28 353
6	4700.0	4717.6	15	9	45	244 960	1 977 551

The normalized inverse transmission coefficient $\tilde{S}_{21}^{-1}$ is fitted as in Ref. [53]. This procedure makes it possible to accurately estimate both the internal Q_i and the rescaled coupling Q_c^* quality factors of a resonator. The fit results are shown in Table III. The plot of the fits for the magnitude and phase of S_{21} for resonator 2 are overlaid with the measured data in Fig. 15(d). The real and imaginary parts of $\tilde{S}_{21}^{-1}$ for the same resonator, as well as the associated fit, are shown in Fig. S4 in Sec. S5 of the Supplemental Material [47].

The resonator mean photon number $\langle n_{\rm ph}\rangle$ can be estimated from the room-temperature power at the input channel $P_{\rm in}$ and the knowledge of the total input-channel attenuation α (see Sec. S2 of the Supplemental Material [47,69,70]). From basic circuit theory and Ref. [71], we obtain

$$\langle n_{\rm ph}\rangle = \frac{2}{h\pi^2}\frac{Q_l^2}{Q_c^*}\frac{P'_{\rm in}}{\tilde{f}_0^2}, \tag{4}$$

where h is the Planck constant, $1/Q_l = 1/Q_i + 1/Q_c^*$ is the inverse loaded quality factor of the resonator, and $P'_{\rm in} = P_{\rm in}/\alpha$ is the power at the resonator input. For example, $\langle n_{\rm ph}\rangle \simeq 4.1 \times 10^7$ for resonator 2.

The fabrication process of the resonators described in Table III is not optimized for high values of Q_i, which,

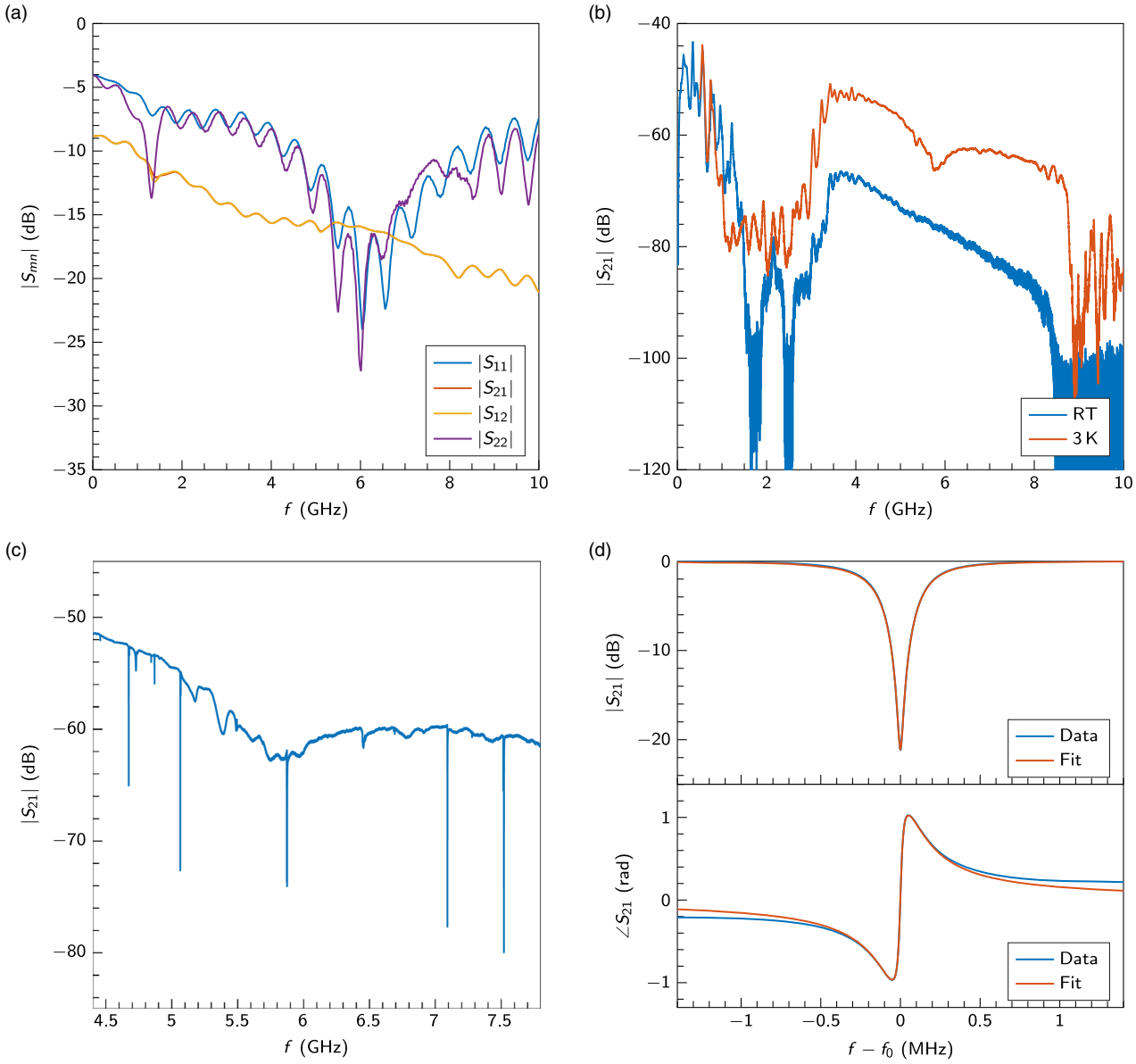

FIG. 15. Measurements of Al-on-Si resonators. (a) Benchtop measurement of the S parameters of the CPW transmission line 3 conducted at room temperature. (b) $|S_{21}|$ measurement of the same line with the chip mounted on the MC stage of the DR at room temperature (blue) and at approximately 3 K (red). (c) $|S_{21}|$ measurement of the sample at approximately 10 mK. The five dips correspond to $(\lambda/4)$-wave resonators. (d) Magnitude and phase of S_{21} for resonator 2.

however, is an important figure of merit for applications to quantum computing. In order to verify the compatibility of the quantum socket with resonators of higher quality, we decide to fabricate a sample featuring an Al thin film deposited by means of a ultrahigh-vacuum electron-beam physical vapor-deposition (EBPVD) system; the substrate of choice is, in this case, sapphire. The sample design is similar to that shown in Fig. 14 and the sample preparation analogous to that in Ref. [53]; fabrication details are in Appendix F. We are able to measure a few resonators with $Q_i > 10^6$ for large values of $\langle n_{\rm ph}\rangle$. For one of these resonators, we measure Q_i as a function of $\langle n_{\rm ph}\rangle$, as shown in Fig. 16. As expected from measurements in the literature [53], Q_i decreases by approximately one order of magnitude when the resonator mean photon number is reduced from $\langle n_{\rm ph}\rangle \simeq 10^6$ to $\simeq 10^{-2}$. For the lowest mean photon number, $Q_i \simeq 2.8 \times 10^5$; such a quality factor is a good indication that the quantum socket will likely preserve quantum coherence sufficiently well when utilized for the manipulation of superconducting qubits.

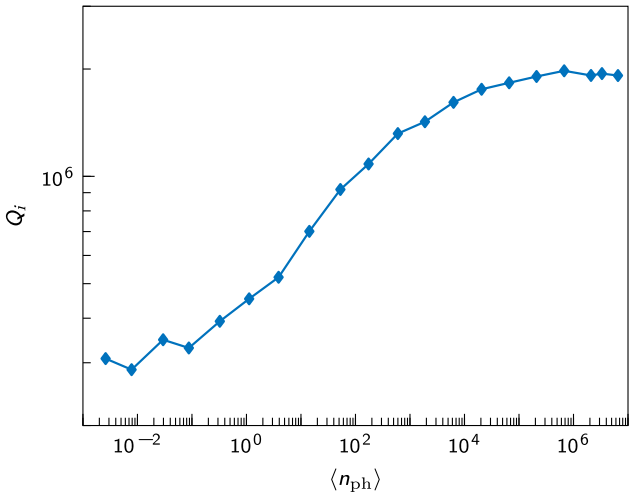

FIG. 16. Measurement of Q_i as a function of $\langle n_{\rm ph}\rangle$ for one of the Al-on-sapphire resonators. The experimental settings used in the measurements are reported in Sec. S2 of the Supplemental Material [47]; the confidence intervals are evaluated from the standard errors of the fitting parameters of the normalized inverse transmission coefficient $\tilde{S}_{21}^{-1}$ and are smaller than the diamond symbols. All measurements are performed at approximately 10 mK. The typical-quality-factor "S curve" is observed; the plateaus on the leftmost and rightmost regions of the curve indicate the reaching of low values of $\langle n_{\rm ph}\rangle$ and saturation of the two-level systems, respectively [53].

VI. CONCLUSIONS

In a recent work [3], seven sequential stages necessary to the development of a quantum computer were introduced. At that time, the next stage to be reached was the implementation of a single logical qubit characterized by an error rate that was at least one order of magnitude lower than that of the underlying physical qubits. In order to achieve this task, a two-dimensional lattice of 10×10 physical qubits with an error rate of at most 10^{-3} was required [22].

Figure 17 shows an extensible quantum computing architecture where a two-dimensional square lattice of superconducting qubits is wired by means of a quantum socket analogous to that introduced in this work. The architecture comprises three main layers: the quantum hardware; the shielding interlayer; the three-dimensional wiring mesh.

As shown in Fig. 17(a), the quantum hardware is realized as a two-dimensional lattice of superconducting qubits with nearest-neighbor interactions. The qubits are a modified version of the Xmon presented in Ref. [59]. Each qubit is characterized by seven arms for coupling to one *XY* and one *Z* control line as well as one measurement resonator and four interqubit-coupling resonators. We name this type of qubit the *heptaton*. The interqubit coupling is mediated by means of superconducting CPW resonators that allow the implementation of control-*Z* (*CZ*) gates between two neighboring qubits [72,73]. A set of four heptatons can be read out by way of a single CPW transmission line connected to four CPW resonators, each with a different resonant frequency. Figure 17 also shows the on-chip pads associated with each three-dimensional wire. In Sec. S7 of the Supplemental Material [47], we propose an extended architecture where each qubit can be measured by means of two different resonators, one with a frequency above and the other with a frequency below all of the coupling-resonator frequencies.

Assuming a pitch between two adjacent three-dimensional wires of 1 mm, the lateral dimension of one square cell having four heptatons at its edges is 8 mm. The three distances *A*, *B*, and *C* between the wire pads and the resonators leading to this quantity are indicated in Fig. 17(b). It is thus possible to construct a two-dimensional lattice of 10×10 heptatons on a square chip with a lateral dimension 9×8 mm$^2 = 72$ mm^2. A (72×72)-mm^2 square chip is the largest chip that can be diced from a standard 4-in. wafer. This procedure will allow for the implementation of a logical qubit based on the surface code, with a distance of at least 5 [22]. In this architecture, the coupling resonators act as a *coherent spacer* between pairs of qubits; i.e., they allow a sufficient separation to accommodate the three-dimensional wires, while maintaining quantum coherence during the *CZ* gates. Additionally, these resonators will help mitigate qubit cross talk compared to architectures based on direct capacitive coupling between adjacent qubits (see Ref. [36]). In fact, they will suppress qubit-mediated coupling between neighboring control lines (a similar coupling mechanism to that shown in Ref. [74]). It is worth noting that adjacent coupling resonators can be suitably designed to be at different frequencies, thus further diminishing qubit-mediated cross talk.

Implementing a large qubit chip with a lateral dimension of 72 mm presents significant challenges to the qubit operation at microwave frequencies. A large chip must be housed in a large microwave package, causing the appearance of box modes that can interfere with the qubit control and measurement sequences [43]. Moreover, a large chip will inevitably lead to floating ground planes that can generate unwanted slotline modes [43]. All of these parasitic effects can be suppressed by means of the shielding interlayer, as shown in Fig. 17(a). This layer can be wafer bonded [5–8] to the quantum layer. Through-holes and cavities on the bottom part of the layer can be readily fabricated using standard Si-etching techniques. The holes will house the three-dimensional wires, whereas the cavities will accommodate the underlying qubit and resonator structures. Large substrates also generate chip modes that, however, can be mitigated using buried metal layers and/or metalized through-silicon vias [65].

The three-dimensional wires to be used for the (10×10)-qubit architecture will be an upgraded version

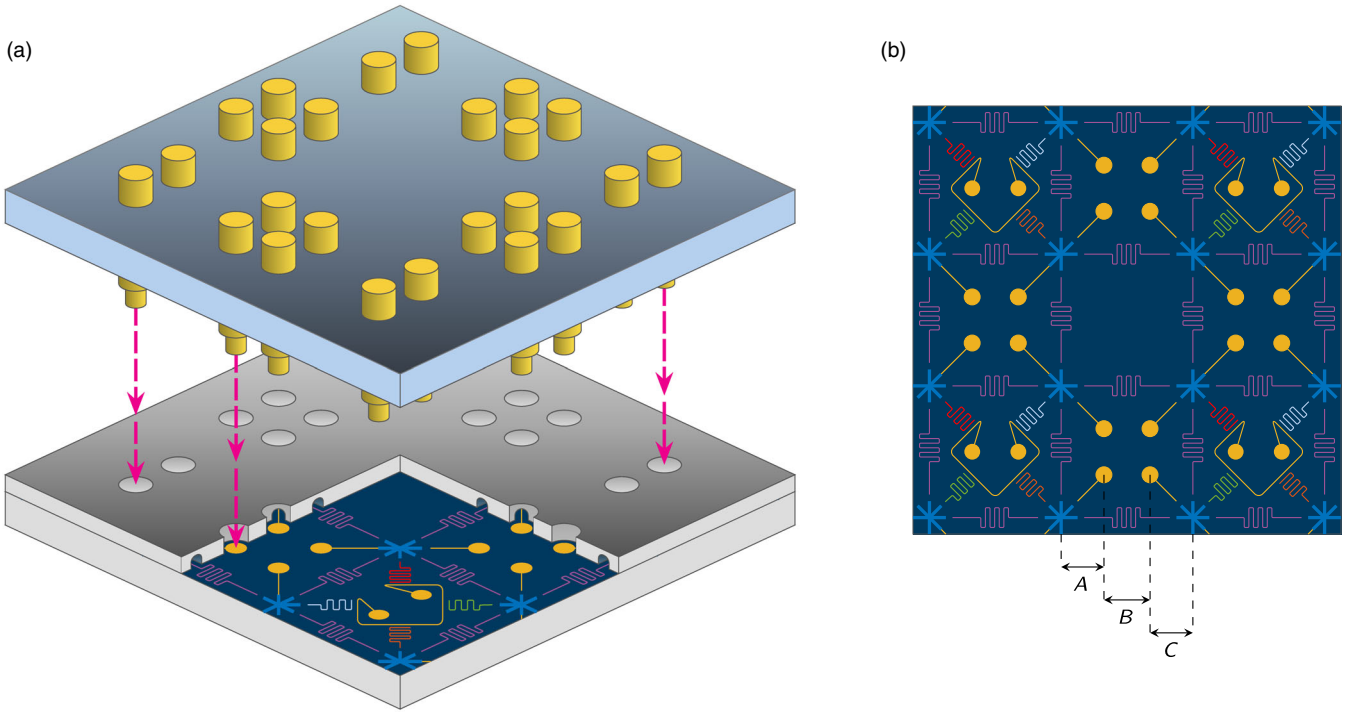

FIG. 17. Extensible quantum-computing architecture. (a) The three main layers of the architecture: the quantum hardware (bottom layer), the shielding interlayer (middle layer), and the three-dimensional wiring mesh (top layer), with wires indicated in yellow. The vertical dashed lines with double arrows show the mounting procedure to be used to prepare the assembly. The (thinner) middle layer will be metalized on the bottom and wafer bonded to the quantum layer beneath; both the through-holes that accommodate the three-dimensional wires and the tunnels above the qubits and manipulation lines are shown. The back end of the wires (top layer) will be connected to SMPS connectors (not shown). (b) Two-dimensional view of the quantum hardware. The substrate is indicated in dark blue, the heptatons in light blue, the coupling resonators in magenta, the four readout resonators in red, green, orange, and cyan, and, finally, the wire pads and associated lines in yellow. The distances between the coupling resonators and the wire pads are $A = C = 2.25$ mm and $B = 3.5$ mm. Note that the Z control lines are represented as galvanically connected to the heptatons, in a fashion similar to Ref. [59]. The measurement can be multiplexed so that four qubits are read out by one line only.

of the wires used in this work. In particular, the M2.5 thread will be removed and the wires will be inserted in a dedicated substrate [see Fig. 17(a)]; additionally, the screw-in microconnector will be substituted by a direct connection to a subminiature push-on submicroconnector (SMPS) (not shown in the figure).

In future applications of the quantum socket, we envision an architecture where the three-dimensional wires will be used as an interconnect between the quantum layer and a classical control or measurement layer. The classical layer could be realized using rapid single-flux quantum (RSFQ) digital circuitry [75,76]. For example, high-sensitivity digital down-converters (DDCs) have been fabricated based on RSFQ electronics [77]. Such circuitry is operated at very low temperatures and can substitute for the room-temperature electronics used for qubit readout. Note that cryogenic DDC chips with dimensions of less than 5×5 mm^2 can perform the same operations presently carried out by room-temperature microwave equipment with an overall footprint of approximately 50×50 cm^2. Recent interest in reducing dissipation in RSFQ electronics [78] will possibly enable the operation of the classical electronics in close proximity to the quantum hardware. We also believe it is feasible to further miniaturize the three-dimensional wires so that the wire's outer diameter would be on the order of 500 μm. Assuming a wire-wire pitch also of 500 μm, it will therefore be possible to realize a lattice of 250 000 wires connecting to approximately 10^5 qubits arranged on a 315×315 two-dimensional qubit grid with dimensions of 1×1 m^2. This lattice will allow for the implementation of simple fault-tolerant operations between a few tens of logical qubits [22].

ACKNOWLEDGMENTS

Matteo Mariantoni and the Digital Quantum Matter Laboratory acknowledge the Alfred P. Sloan Foundation as well as the Natural Sciences and Engineering Research Council of Canada (NSERC), the Ministry of Research and Innovation (MRI) of Ontario, and the Canadian Microelectronics Corporation (CMC) Microsystems. C. R. H. M. acknowledges support from a Waterloo

TABLE IV. Chemical composition (wt %) of the two main materials used in the three-dimensional wires. Copper, Cu; tin, Sn; zinc, Zn; lead, Pb; phosphorus, P.

Material	Cu	Sn	Zn	Fe	Ni	Pb	P	Si	Others
CW724R[a]	73–77	0.3	rest	0.3	0.2	≤ 0.09	0.04–0.10	2.7–3.4	Al = 0.05, manganese = 0.05
CW453K[b]	rest	7.5–8.5	≤ 0.2	≤ 0.1	≤ 0.2	≤ 0.02	0.01–0.4	···	0.2

[a]See Ref. [80].
[b]See Ref. [81].

Institute for Nanotechnology (WIN) Nanofellowship–2013 and J. H. B. a Provost's Entrance Award of the University of Waterloo (UW). We acknowledge our fruitful discussions with John M. Martinis and the Martinis Group, Eric Bogatin, and William D. Oliver. We thank the group of Adrian Lupascu as well as Patrick Smutek of Plassys-Bestek SAS for their assistance in the deposition of Al films and Nathan Nelson-Fitzpatrick and the UW's Quantum NanoFab Facility for their support with device fabrication. We thank Dario Mariantoni and Alexandra V. Bardysheva for their help with a few images and figures.

J. H. B. and T. G. M. contributed equally to this work.

APPENDIX A: WIRE COMPRESSION

In this appendix, we discuss the pressure settings of the three-dimensional wires. In the current implementation of the quantum socket, the pressure exerted by the three-dimensional wires on the chip is controlled by the installation depth of the wire in the lid. This depth depends on the number of rotations used to screw the wire into the M2.5-threaded hole of the lid. Since the wire's tunnel has to be aligned with the corresponding on-chip pad, a discrete number of wire pressure settings is allowed. For the package shown in Figs. 1(b) and 4(b), the minimum length an unloaded wire has to protrude from the ceiling of the lid's internal cavity to touch the top surface of the chip is $\ell_c = 3.05$ mm [see Fig. 1(c)]. For a maximum wire stroke $\Delta L = 2.5$ mm, the maximum length an unloaded wire can protrude from the cavity ceiling without breaking when loaded is $\ell_c + \Delta L = 5.55$ mm. The first allowed pressure setting, with wire and pad perfectly aligned, is for $\ell_p = 3.10$ mm. The pitch for an M2.5 screw is 0.45 mm. Hence, five pressure settings are nominally possible, for $\ell_p = 3.10 + 0.45k$ mm, with $k = 1, 2, \ldots, 5$. We find the ideal pressure setting to be when $k = 3$, corresponding to a nominal $\ell_p = 4.45$ mm; the actual average setting for 12 wires is measured to be $\ell_p = 4.48 \mp 0.28$ mm, with standard deviation due to the machining tolerances. For greater depths, we experience occasional wire damage; lesser depths are not investigated. Possible effects on the electrical properties of the three-dimensional wires due to different pressure settings will be studied in a future work.

APPENDIX B: MAGNETISM

In this appendix, we describe the measurement setup employed to characterize the magnetic properties of the materials used in the quantum socket and present the main measurement results. Additionally, we give an estimate of the strength of the magnetic field caused by one three-dimensional wire inside the microwave package.

The ZGC used in our tests comprises three nested cylinders, each with a lid with a central circular hole; the hole in the outermost lid is extended into a chimney that provides further magnetic shielding. The walls of the ZGC are made of an alloy of Ni and Fe (or a mu-metal alloy) with a high relative magnetic permeability μ_r. The alloy used for the chamber is a Co-Netic® AA alloy and is characterized by a dc-relative magnetic permeability at 40 G, $\mu_{\mathrm{dc}}^{40} = 80\,000$, and an ac-relative magnetic permeability at 60 Hz and at 40 G, $\mu_{\mathrm{ac}}^{40} = 65\,000$. As a consequence, the nominal magnetic-field attenuation lies between 1000 and 1500. The ZGC used in our tests is manufactured by the Magnetic Shield Corporation (model ZG-209).

The flux-gate magnetometer used to measure the magnetic field $\vec{B}$ is a three-axis dc milligauss meter from AlphaLab, Inc. (model MGM3AXIS). Its sensor is a $(38 \times 25 \times 25)$-mm^3 parallelepiped at the end of an approximately 1.2-m-long cable; the orientation of the sensor is calibrated to within 0.1° and has a resolution of 0.01 mG (i.e., 1 nT) over a range of ∓ 2000 mG (i.e., ∓ 200 μT).

The actual attenuation of the chamber is tested by measuring the value of Earth's magnetic field with and without the chamber in two positions, vertical and horizontal; inside the chamber, the measurements are performed a few centimeters from the chamber's base, approximately on the axis of the inner cylinder. In these and all subsequent tests, the magnetic sensor is kept in the same orientation and position. The results are reported in Table V, which shows the type of measurement performed, the magnitude of the measured magnetic field $\|\vec{B}\|$, and the attenuation ratio α. The maximum measured attenuation is $\alpha \simeq 917$ in the horizontal position.

The ZGC characterization of Table V also serves as a calibration for the measurements on the materials used for the quantum socket. In these measurements, each test sample is positioned approximately 1 cm away from the magnetic sensor. The results, which are reported in

TABLE V. ZGC calibration. The margins of error indicated in parentheses are estimated from the fluctuation of the magnetic sensor.

Measurement	$\|\vec{B}\|$ (mG)	α
Vertical position, background field	554(20)	···
Vertical position, with ZGC	0.66(5)	842(34)
Horizontal position, background field	539(20)	···
Horizontal position, with ZGC	0.59(5)	917(44)

Table VI, are obtained by taking the magnitude of the calibrated field of each sample. The calibrated field itself is calculated by subtracting the background field from the sample field, component by component. Note that the background and sample fields are on the same order of magnitude (between 0.10 and 0.80 mG), with background fluctuations on the order of 0.10 mG. Thus, we record the maximum value of each x, y, and z component. Considering that the volume of the measured samples is significantly larger than that of the actual quantum-socket components, we are confident that the measured magnetic fields of the materials should be small enough not to significantly disturb the operation of superconducting quantum devices. As part of our magnetism tests, we measure a block of approximately 200 g of 5N5 Al in the ZGC; as shown in Table VI, the magnitude of the magnetic field is found to be within the noise floor of the measurement apparatus [79].

A simple geometric argument allows us to estimate the actual magnetic field due to one three-dimensional wire, without taking into account effects due to superconductivity (most of the wire is embedded in an Al package, which is superconductive at the qubit operation temperatures). We assume that one wire generates a magnetic field of 0.25 mG (i.e., the maximum field value in Table VI; this overestimate is large, considering that the tested samples have volumes much larger than any component in the wires) and is a magnetic dipole positioned 15 mm away from a qubit. The field generated by the wire at the qubit will then be $B_q \simeq 0.25 r_0^3/0.015^3$ mG, where $r_0 \simeq 10$ mm is the distance at which the field is measured in the ZGC; thus, $B_q \simeq 0.075$ mG. Assuming an Xmon qubit with a superconducting quantum interference device (SQUID) of dimensions $40 \times 10\ \mu\text{m}^2$ (cf. Ref. [59]), the estimated magnetic flux due to the wire threading the SQUID is $\Phi_q \simeq 4 \times 10^{-18}$ Wb. This estimate is approximately 3 orders of magnitude smaller than a flux quantum $\Phi_0 \simeq 2.07 \times 10^{-15}$ Wb; typical flux values for the Xmon operation are on the order of $0.5\Phi_0$.

TABLE VI. Magnetic-field measurements of the materials used for the main components of the quantum socket. The tested samples are significantly larger than any component used in the actual implementation of the three-dimensional wires and microwave package. The margins of error indicated in parentheses are estimated from the fluctuation of the magnetic sensor.

Material	$\|\vec{B}\|$ (mG)
CW724R	0.21(5)
CW453K	0.25(5)
Al 5N5	0.02(5)

APPENDIX C: THERMAL CONDUCTANCE OF A THREE-DIMENSIONAL WIRE

In this appendix, we describe the method used to estimate the thermal performance of a three-dimensional wire and compare it to that of an Al-wire bond. Note that at very low temperatures, thermal conductivities can vary by orders of magnitude between two different alloys of the same material. The following estimate can thus only be considered correct to within approximately one order of magnitude. Thermal conductivity is a property intrinsic to a material. To characterize the cooling performance of a three-dimensional wire, we instead use the heat-transfer rate (power) per kelvin difference, which depends on the conductivity.

The power transferred across an object with its two extremities at different temperatures depends on the cross-sectional area of the object, its length, and the temperature difference between the extremities. Since the cross section of a three-dimensional wire is not uniform, we assume that the wire is made of two concentric hollow cylinders. The cross-sectional area of the two cylinders is calculated by using dimensions consistent with those of a three-dimensional wire. The inner and outer hollow cylinders are assumed to be made of phosphor bronze and brass alloys, respectively. The thermal conductivities of these materials at low temperatures are determined by extrapolating measured data to 25 mK [82].

The Al-wire bonds are assumed to be solid cylinders with a diameter of 50 μm. In the superconducting state, the thermal conductivity of Al can be estimated by extrapolating from values in the literature [83].

The heat-transfer rate per kelvin difference is calculated by multiplying the thermal conductivity k_t with the cross-sectional area A and dividing it by the length of the thermal conductor ℓ. The heat-transfer rate per kelvin difference of a three-dimensional wire is calculated by summing the heat-transfer rate per kelvin difference of the inner conductor to that of the outer conductor, and it is found to be $\Pi_t \simeq 6 \times 10^{-7}$ WK^{-1} at 25 mK. At the same temperature, the heat-transfer rate per kelvin difference of a typical Al-wire bond is estimated to be $\Pi_b \simeq 4 \times 10^{-12}$ WK^{-1} (see Table VII), much lower than for a single three-dimensional wire. Note that, instead of Al-wire bonds, gold-wire bonds can be used. These bonds are characterized by a higher thermal conductivity because they remain normal conductive also at very low temperatures. However, Al-wire bonds

TABLE VII. Parameters used in the estimate of the heat-transfer rate per kelvin difference for a three-dimensional wire and an Al-wire bond. In the table, we report the hollow cylinder's inner diameter d_i, the hollow cylinder's outer diameter and wire-bond diameter d_o, the hollow cylinder and wire-bond cross-sectional area A, and the thermal conductivity k_t. Conductor, Cond.; phosphor, phos.

	d_i (μm)	d_o (μm)	A (m^2)	k_t (m WK^{-1} m^{-1})
Inner cond. (phos. bronze)	290	380	4.74×10^{-8}	3.7
Outer cond. (brass)	870	1290	7.13×10^{-7}	24.1
Wire bond (Al)	···	50	1.96×10^{-9}	0.01

remain the most common choice because they are easier to use.

APPENDIX D: THERMOMECHANICAL TESTS

In this appendix, we first describe the test setup used to find the mean number of cycles before mechanical failure of a three-dimensional wire and show images of the wire after testing; then we discuss the performance of the springs used in three-dimensional wires at various temperatures.

In order to obtain the mean number of cycles before mechanical failure of a three-dimensional wire, we use an automated pneumatic system, which makes it possible to compress the wire a very large number of times. The wire under test is operated at a stroke of 2.0 mm; the test-cycle time is 120 strokes per minute; finally, the entire test takes place at a temperature of 20 °C. The test is run for approximately 28 h, for a total of 200 000 wire compressions. Both the inner and outer conductors of the wire are mechanically functioning properly at the end of the test; mechanical abrasion is visible, even though the overall wire condition is excellent, as shown by the two images in Fig. 18. From tests on wires with a similar form factor—but made from different materials—we are confident that the number of cycles before dc and microwave electrical failure of our wires also exceeds 200 000.

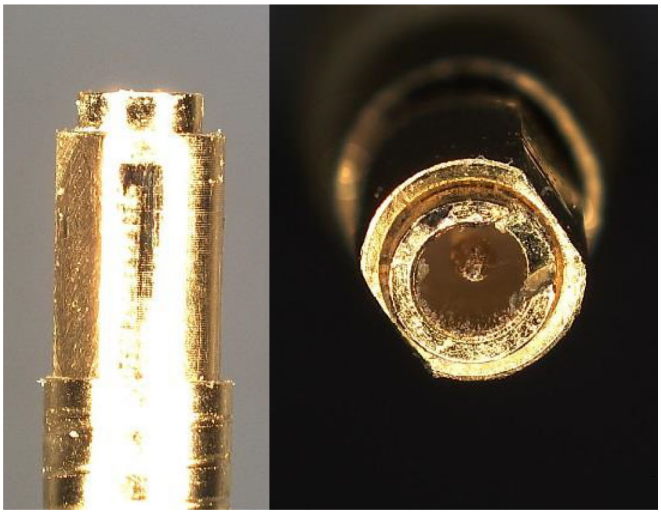

FIG. 18. Side- and top-view images of a three-dimensional wire after 200 000 compression cycles.

TABLE VIII. Thermomechanical tests on hardened BeCu springs. In the table, we report the outer diameter D of the coil forming the helix structure of the spring; the diameter d of the circular cross section of the spring (note that the smallest wire diameter is 150 μm); the spring free length L_f, i.e., the spring length at its relaxed position; the number of coils N_c; and the spring force F_c (estimated at all operating temperatures).

Spring type	D (mm)	d (mm)	L_f (mm)	N_c	F_c (N)
FE-113 225	2.30	0.26	11.55	11.25	approx. 1.0
FE-112 157	1.30	0.22	18.00	42.00	approx. 1.0
FE-50 15	0.60	0.15	31.75	150.00	approx. 0.5

The three types of tested springs are called FE-113 225, FE-112 157, and FE-50 15, and their geometric characteristics are reported in Table VIII. We run temperature cycle tests by dunking the springs repeatedly in liquid nitrogen and then in liquid helium without any load. At the end of each cycle, we attempt to compress them at room temperature. We find no noticeable changes in mechanical performance after many cooling cycles. Subsequently, the springs are tested mechanically by compressing them while submerged in liquid nitrogen or helium. The setup used for the compressive-loading test of the springs is shown in movie S4 in Sec. S6 of the Supplemental Material [47], which also shows a properly functioning spring immediately after being cooled in liquid helium. In these tests, we only study compression forces because, in the actual experiments, the three-dimensional wires are compressed and not elongated.

The compression force is assessed by means of loading the springs with a mass. The weight of the mass that fully compresses the spring determines the spring compression force F_c. The compression force of each spring is reported in Table VIII. We observe through these tests that the compression force is nearly independent of the spring temperature, increasing only slightly when submerged in liquid helium. Assuming an operating compression $\Delta L = 2.0$ mm, we expect a force between 0.5 and 2.0 N for the inner conductor and between 2.0 and 4.0 N for the outer conductor of a three-dimensional wire at a temperature of 10 mK. Note that we choose spring model FE-113 225 for use with the grounding washer.

APPENDIX E: ALIGNMENT ERRORS

In this appendix, we provide more details about alignment errors. Figure 19 shows a set of microimages for Au and Ag samples. The Au pads in Figs. 19(a) and 19(b) are mated two times at room temperature; the

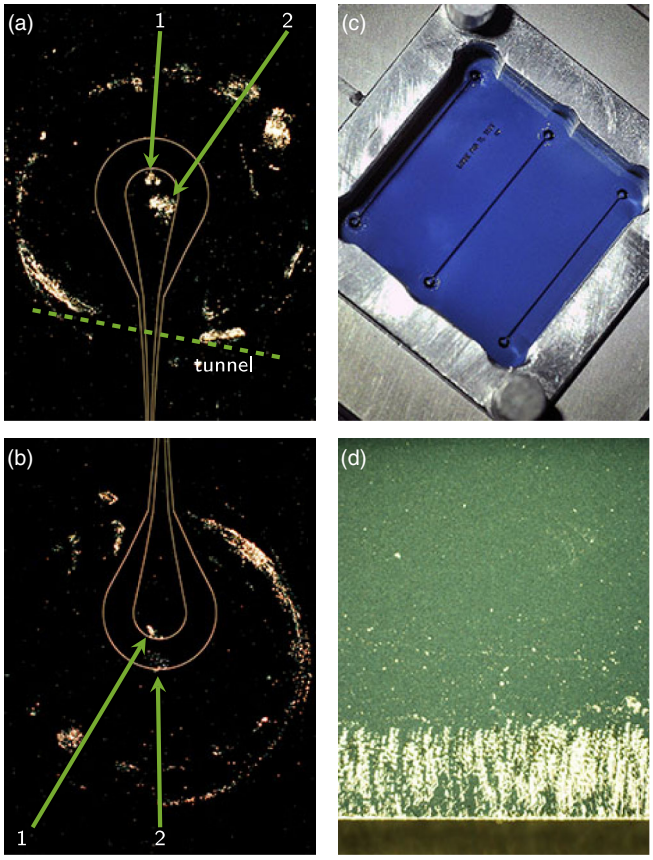

FIG. 19. Microimages showing three-dimensional wire alignment errors. (a),(b) Au pads. The pad displayed in (a) is connected to that in (b) by way of a CPW transmission line approximately 11.5 mm long. The die shifted upward between the first (arrow 1) and second (arrow 2) mating instance, resulting in a lateral misalignment for the bottom pad. The rotational misalignment for the pad in (a) is indicated by a dashed line. (c) Successful alignment for six Ag pads on the same chip. (d) Peripheral area of an Ag sample (ground plane). The marks are attributed to contact with the grounding washer.

three-dimensional wires used to mate these pads feature the smaller tunnel (500 μm width). The pad dimensions are $W_p = 230$ μm and $T_p = 1000$ μm. Noticeably, for the pad in Fig. 19(a), the wire bottom interface matches the contact pad in both mating instances, even though the matching is affected by a rotational misalignment of approximately 15° with respect to the transmission-line longitudinal axis. However, for the pad in Fig. 19(b), the lateral misalignment is significant enough that the inner conductor lands on the dielectric gap in the second mating instance.

In our initial design, a perfect match required that the die dimensions should be, at most, 1 thou smaller than the dimensions of the chip recess, as machined. In the case of the sample holder used to house the Au samples, the chip-recess side lengths are 15.028(5), 15.030(5), 15.013 (5), and 15.026(5) mm. The Au samples are diced from a Si wafer using a dicing saw from DISCO (model DAD-2H/6), set to obtain a (15×15)-mm^2 die. Owing to the saw inaccuracies, the actual die dimensions are $14.96(1) \times 14.96(1)$ mm^2, significantly smaller than the chip-recess dimensions. This size difference causes the die to shift randomly between different mating instances, generating significant alignment errors.

As described in the text, in order to minimize such errors, a superior DISCO saw is used, in combination with a DISCO electroformed bond-hub diamond-blade model ZH05-SD 2000-N1-50-F E; this blade corresponds to a nominal kerf between 35 and 40 μm. Additionally, we use rotational as well as lateral aligning markers; the latter are spaced with increments of 10 μm that allow us to cut dies with dimensions ranging from 14.97 to 15.03 mm, well within the machining tolerances of the sample holder. After machining, the actual inner dimensions of each sample holder are measured by means of a measuring microscope. The wafers are then cut by selecting the lateral dicing markers associated with the die dimensions that best fit the holder being used.

Figure 19(c) shows a successful alignment for six Ag pads on the same chip; the chip is mounted in a sample holder with a grounding washer. All three main steps for an ideal and repeatable alignment (see Sec. III D) are followed. Figure 19(d) shows the distinctive marks left by the grounding washer on an Ag film. The marks are localized towards the edge of the die; the washer covers approximately a width of 500 μm of Ag film. Such a width results in a good electrical contact at the washer-film interface.

In conclusion, it is worth commenting upon some of the features in Fig. 5(d). The figure clearly shows the dragging of a three-dimensional wire due to cooling contractions. In fact, for the Al chip recess, an estimate of the lateral contraction length from room temperature to approximately 4 K can be obtained as $\Delta L_{\mathrm{Al}} = \alpha(4) L_{\mathrm{Al}} \simeq (4.15 \times 10^{-3})$ $(15 \times 10^{-3}\ \mathrm{m}) \simeq 62$ μm, where $\alpha(4)$ is the integrated linear thermal-expansion coefficient for Al 6061-T6 [84] at 4 K from Ref. [61] and L_{Al} is the room-temperature length of the recess side [85]. Note that the sample holder is actually made from Al alloy 5N5; however, different Al alloys contract by approximately the same quantity. For the Si sample substrate, the lateral contraction length from room temperature to about 4 K is approximately given by $\Delta L_{\mathrm{Si}} \simeq 3.2$ μm, where the integrated linear thermal-expansion coefficient at 4 K is found in Table 2 of Ref. [86]. Below 4 K, the thermal expansion of both materials is negligible for our purposes, and thus the 4-K estimate can also be considered valid at approximately 10 mK.

APPENDIX F: SAMPLE FABRICATION

In this appendix, we outline the fabrication processes for the samples used to test the quantum socket. A set of samples is made by lift-off of a 3-μm Ag film, which is grown by means of EBPVD (a system from Intlvac Canada Inc., model Nanochrome II) on a 3-in. float-zone

(FZ) Si (100) wafer with a thickness of 500 μm. The superconducting Al-on-Si samples are made by etching a 120-nm Al film that is deposited by EBPVD on a 500-μm FZ Si wafer. The Al-on-sapphire sample is made by etching a 100-nm Al film that is deposited by an UHV EBPVD (a system from Plassys-Bestek SAS) on a 500-μm c-plane single-crystal sapphire wafer. Prior to deposition, the wafer is annealed *in vacuo* at approximately 850 °C, while being cleaned by way of molecular oxygen; a 1-nm germanium buffer layer is grown at room temperature before we deposit the Al film. Last, two sets of test samples are made by etching Au films with thicknesses of 100 and 200 nm, with a 10-nm Ti adhesion underlayer in both sets. The films are grown by EBPVD (Intlvac) on a 3-in. Czochralski undoped Si (100) wafer with a thickness of 500 μm.

The 3-μm Ag samples are required to reduce the series resistance of the CPW transmission lines (see Secs. IV B, IV C, and IV D). Fabricating such a relatively thick film necessitates a more complex process than that used for the Au and Al samples. The Ag samples are fabricated with a thick resist tone-reversal process. The wafer is spun with an AZ P4620 positive tone resist to create a resist thickness of approximately 14 μm, then soft baked for 4 min at 110 °C. Because the resist layer is so thick, a rehydration step of 30 min is necessary before exposure. Optical exposure is performed for 30 s in a mask aligner from SÜSS MicroTec AG (model MA6), in soft contact with a photomask. After exposure, the sample is left resting for at least 3 h so that any nitrogen created by the exposure can dissipate. The tone-reversal bake is done for 45 min in an oven set to 90 °C, filled with ammonia gas. The sample then undergoes a flood exposure for 60 s and is developed in AZ® 400 K for 15 min. Subsequently, 3 μm of Ag is deposited and lift-off of the resist is performed in acetone for 5 min with ultrasound.

APPENDIX G: MICROWAVE PARAMETERS

In this appendix, we present a set of microwave parameters that help further analyze the performance of the quantum socket. These parameters are obtained from the measured S-parameter data of Figs. 9 and 10(a) and are shown in Fig. 20. The complex input impedance can be obtained from the frequency-dependent impedance matrix $\mathbf{Z} = [Z_{mn}]$ as [87]

$$Z_{\text{in}} = Z_{11} - \frac{Z_{12}Z_{21}}{Z_{22} - Z_L}, \tag{G1}$$

where $Z_L = Z_c = 50\ \Omega$ is the load impedance. The impedance matrix is obtained using the measured complex S-parameter matrix $\mathbf{S} = [S_{mn}]$ from

$$\mathbf{Z} = \sqrt{Z_c}\left(\begin{bmatrix} 1 & 0 \\ 0 & 1 \end{bmatrix} + \mathbf{S}\right)\left(\begin{bmatrix} 1 & 0 \\ 0 & 1 \end{bmatrix} - \mathbf{S}\right)^{-1}\sqrt{Z_c}. \tag{G2}$$

The magnitude of Z_{in} is shown in Fig. 20(a).

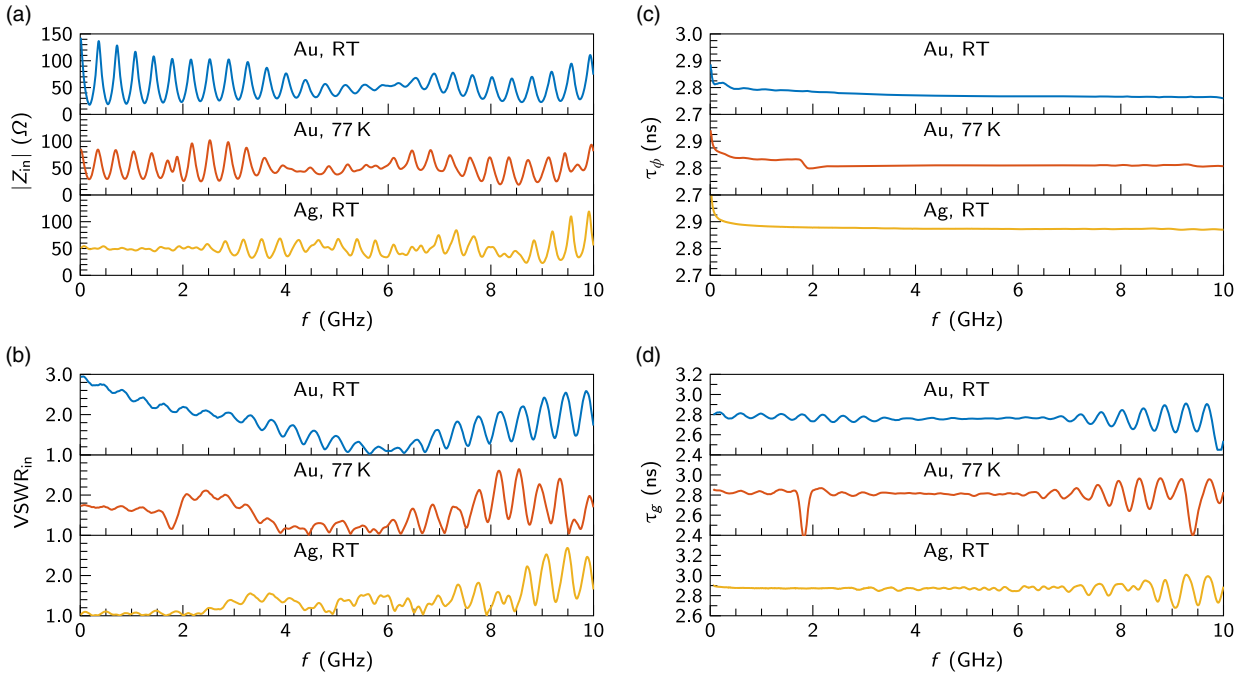

FIG. 20. Quantum-socket microwave parameters. (a) Input impedance magnitude $|Z_{\text{in}}|$. (b) Input VSWR, VSWR$_{\text{in}}$. (c) Phase delay τ_ϕ. (d) Group delay τ_g. Blue corresponds to the Au sample at room temperature (RT), red to the Au sample at 77 K, and orange to the Ag sample at RT.

The input voltage standing-wave ratio (VSWR) is obtained from [41]

$$\mathrm{VSWR}_{\mathrm{in}} = \frac{1+|S_{11}|}{1-|S_{11}|} \tag{G3}$$

and is displayed in Fig. 20(b).

The phase delay is calculated as [87]

$$\tau_{\phi} = -\frac{1}{2\pi}\frac{\angle S_{21}}{f} \tag{G4}$$

and is displayed in Fig. 20(c).

Finally, the group delay is obtained from [41]

$$\tau_{g} = -\frac{1}{2\pi}\frac{\partial}{\partial f}(\angle S_{21}) \tag{G5}$$

and is displayed in Fig. 20(d). The derivative in Eq. (G5) is evaluated numerically by means of central finite differences with sixth-order accuracy. The data in Fig. 20(d) are postprocessed using 1% smoothing. Note that the output impedance and the VSWR are also evaluated and resemble the corresponding input parameters.

The input and output impedances as well as the VSWRs indicate a good impedance matching up to approximately 8 GHz. The phase and group delays, which are directly related to the frequency dispersion associated with the quantum socket, indicate minimal dispersion. This result is expected for a combination of coaxial structures (the three-dimensional wires) and a CPW transmission line. Thus, we expect wideband control pulses to be transmitted without significant distortion in applications with superconducting qubits (see Sec. S8 of the Supplemental Material [47] for further details on microwave-pulse transmission).

[1] D. Deutsch, Quantum theory, the Church-Turing principle and the universal quantum computer, Proc. R. Soc. A **400**, 97 (1985).

[2] John Clarke and Frank K. Wilhelm, Superconducting quantum bits, Nature (London) **453**, 1031 (2008).

[3] Michel H. Devoret and Robert J. Schoelkopf, Superconducting circuits for quantum information: An outlook, Science **339**, 1169 (2013).

[4] John M. Martinis, Qubit metrology for building a fault-tolerant quantum computer, NPJ Quantum Inf. **1**, 15005 (2015).

[5] Timothy M. Miller, Christine A. Jhabvala, Edward Leong, Nicholas P. Costen, Elmer Sharp, Tomoko Adachi, and Dominic J. Benford, in *High Energy, Optical, and Infrared Detectors for Astronomy V*, edited by Andrew D. Holland and James W. Beletic, SPIE Proceedings Vol. 8453 (SPIE-International Society for Optical Engineering, Bellingham, WA, 2012), p. 84532H.

[6] David W. Abraham, Jerry M. Chow, Antonio D. Córcoles Gonzalez, George A. Keefe, Mary E. Rothwell, James R. Rozen, and Matthias Steffen, Removal of spurious microwave modes via flip-chip crossover, U.S. Patent No. 13/838,324 (22 December 2015).

[7] Teresa Brecht, Matthew Reagor, Yiwen Chu, Wolfgang Pfaff, Chen Wang, Luigi Frunzio, Michel H. Devoret, and Robert J. Schoelkopf, Demonstration of superconducting micromachined cavities, Appl. Phys. Lett. **107**, 192603 (2015).

[8] Danna Rosenberg, Donna-Ruth Yost, Rabindra Das, David Hover, Livia Racz, Steven Weber, Jonilyn Yoder, Andrew Kerman, and William Oliver, in *Proceedings of the APS March Meeting*, 2016.

[9] Pedram Roushan *et al.*, Chiral groundstate currents of interacting photons in a synthetic magnetic field, arXiv: 1606.00077.

[10] Alessandro Bruno, Stefano Poletto, Nadia Haider, and Leonardo DiCarlo, in *Proceedings of the APS March Meeting*, 2016.

[11] Jay M. Gambetta, Jerry M. Chow, and Matthias Steffen, Building logical qubits in a superconducting quantum computing system, arXiv:1510.04375.

[12] Teresa Brecht, Wolfgang Pfaff, Chen Wang, Yiwen Chu, Luigi Frunzio, Michel H. Devoret, and Robert J. Schoelkopf, Multilayer microwave integrated quantum circuits for scalable quantum computing, NPJ Quantum Inf. **2**, 16002 (2016).

[13] David P. DiVincenzo, Quantum computation, Science **270**, 255 (1995).

[14] Michael A. Nielsen and Isaac L. Chuang, *Quantum Computation and Quantum Information* (Cambridge University Press, Cambridge, England, 2000).

[15] David P. DiVincenzo, The physical implementation of quantum computation, Fortschr. Phys. **48**, 771 (2000).

[16] N. David Mermin, *Quantum Computer Science: An Introduction* (Cambridge University Press, Cambridge, England, 2007).

[17] Thaddeus D. Ladd, Fedor Jelezko, Raymond Laflamme, Yasunobu Nakamura, Christopher Monroe, and Jeremy L. O'Brien, Quantum computers, Nature (London) **464**, 45 (2010).

[18] Carlos A. Pérez-Delgado and Pieter Kok, Quantum computers: Definition and implementations, Phys. Rev. A **83**, 012303 (2011).

[19] Ashley Montanaro, Quantum algorithms: An overview, NPJ Quantum Inf. **2**, 15023 (2016).

[20] Daniel Gottesman, An introduction to quantum error correction and fault-tolerant quantum computation, Proc. Symp. Appl. Math. **68**, 13 (2010).

[21] Robert Raussendorf and Jim Harrington, Fault-Tolerant Quantum Computation with High Threshold in Two Dimensions, Phys. Rev. Lett. **98**, 190504 (2007).

[22] Austin G. Fowler, Matteo Mariantoni, John M. Martinis, and Andrew N. Cleland, Surface codes: Towards practical large-scale quantum computation, Phys. Rev. A **86**, 032324 (2012).

[23] Pieter Kok, William J. Munro, Kae Nemoto, Timothy C. Ralph, Jonathan P. Dowling, and Gerard J. Milburn, Linear optical quantum computing with photonic qubits, Rev. Mod. Phys. **79**, 135 (2007).

[24] Jeremy L. O'Brien, Akira Furusawa, and Jelena Vućković, Photonic quantum technologies, Nat. Photonics **3**, 687 (2009).
[25] Christopher Monroe and Jungsang Kim, Scaling the ion trap quantum processor, Science **339**, 1164 (2013).
[26] David Cory, in *Frontiers in Optics, OSA Technical Digest (CD)* (Optical Society of America, Washington, DC, 2006), p. LTuI3.
[27] N. Cody Jones, Rodney Van Meter, Austin G. Fowler, Peter L. McMahon, Jungsang Kim, Thaddeus D. Ladd, and Yoshihisa Yamamoto, Layered Architecture for Quantum Computing, Phys. Rev. X **2**, 031007 (2012).
[28] Ronald Hanson, Leo P. Kouwenhoven, Jason R. Petta, Seigo Tarucha, and Lieven M. K. Vandersypen, Spins in few-electron quantum dots, Rev. Mod. Phys. **79**, 1217 (2007).
[29] Brett M. Maune, Matthew G. Borselli, Biqin Huang, Thaddeus D. Ladd, Peter W. Deelman, Kevin S. Holabird, Andrey A. Kiselev, Ivan Alvarado-Rodriguez, Richard S. Ross, Adele E. Schmitz, Marko Sokolich, Christopher A. Watson, Mark F. Gyure, and Andrew T. Hunter, Coherent singlet-triplet oscillations in a silicon-based double quantum dot, Nature (London) **481**, 344 (2012).
[30] Floris A. Zwanenburg, Andrew S. Dzurak, Andrea Morello, Michelle Y. Simmons, Lloyd C. L. Hollenberg, Gerhard Klimeck, Sven Rogge, Susan N. Coppersmith, and Mark A. Eriksson, Silicon quantum electronics, Rev. Mod. Phys. **85**, 961 (2013).
[31] Andrew P. Higginbotham, Ferdinand Kuemmeth, Micah P. Hanson, Arthur C. Gossard, and Charles M. Marcus, Coherent Operations and Screening in Multielectron Spin Qubits, Phys. Rev. Lett. **112**, 026801 (2014).
[32] Joe O'Gorman, Naomi H. Nickerson, Philipp Ross, John J. L. Morton, and Simon C. Benjamin, A silicon-based surface code quantum computer, NPJ Quantum Inf. **2**, 15019 (2016).
[33] Rami Barends *et al.*, Superconducting quantum circuits at the surface code threshold for fault tolerance, Nature (London) **508**, 500 (2014).
[34] Antonio D. Córcoles, Easwar Magesan, Srikanth J. Srinivasan, Andrew W. Cross, Matthias Steffen, Jay M. Gambetta, and Jerry M. Chow, Demonstration of a quantum error detection code using a square lattice of four superconducting qubits, Nat. Commun. **6**, 6979 (2015).
[35] Diego Ristè, Stefano Poletto, M-Z. Huang, Alessandro Bruno, Visa Vesterinen, Olli-Pentti Saira, and Leonardo DiCarlo, Detecting bit-flip errors in a logical qubit using stabilizer measurements, Nat. Commun. **6**, 6983 (2015).
[36] Julian Kelly *et al.*, State preservation by repetitive error detection in a superconducting quantum circuit, Nature (London) **519**, 66 (2015).
[37] Josh Y. Mutus, Theodore C. White, Rami Barends, Yu Chen, Zijun Chen, Ben Chiaro, Andrew Dunsworth, Evan Jeffrey, Julian Kelly, Anthony Megrant, Charles Neill, Peter J. J. O'Malley, Pedram Roushan, Daniel Sank, Amit Vainsencher, James Wenner, Kyle M. Sundqvist, Andrew N. Cleland, and John M. Martinis, Strong environmental coupling in a Josephson parametric amplifier, Appl. Phys. Lett. **104**, 263513 (2014).
[38] A typical chip comprises a dielectric substrate (e.g., silicon or sapphire) and a metallic surface.
[39] Matthias Zapatka and Ralf Ziser, in *Proceedings of the 2009 74th ARFTG Microwave Measurement Conference, Broomfield, CO, 2009* (IEEE, New York, 2009), p. 1.
[40] Robert E. Collin, *Foundations for Microwave Engineering*, 2nd ed. (IEEE, New York, 2001).
[41] David M. Pozar, *Microwave Engineering*, 4th ed. (John Wiley & Sons, Hoboken, NJ, 2011).
[42] These errors can result in undesired short-circuit connections to the ground.
[43] James Wenner, Matthew Neeley, Radoslaw C. Bialczak, Michael Lenander, Erik Lucero, Aaron D. O'Connell, Daniel Sank, Haohua Wang, Martin Weides, Andrew N. Cleland, and John M. Martinis, Wirebond cross talk and cavity modes in large chip mounts for superconducting qubits, Supercond. Sci. Technol. **24**, 065001 (2011).
[44] The pillar is included in the design, as there is concern over potential damage to the large (15×15)-mm^2 substrates (particularly the Si ones) from mechanical strain due to the three-dimensional wires pushing on the top of the chip.
[45] The microconnector is necessary because the high temperatures generated by soldering a coaxial cable directly to the wire back end would damage some of the inner wire components. The breaking temperature of those components is even lower than the melting temperature of the available eutectic solders.
[46] The simulation software used is the high-frequency three-dimensional full-wave electromagnetic-field simulation software (also known as HFSS) by Ansys, Inc.
[47] See Supplemental Material at http://link.aps.org/supplemental/10.1103/PhysRevApplied.6.044010 for experimental setups and settings, animated electric field simulations, screw-in microconnector anomalies, superconducting resonator couplings and fits, spring tests, high- and low-tone qubit measurements, and microwave-pulse transmission details.
[48] Rainee N. Simons, *Coplanar Waveguide Circuits, Components, and Systems* (John Wiley & Sons, Hoboken, NJ, 2001).
[49] This is the case provided that the vacuum still constitutes the majority of the volume of the cavity.
[50] Luigi Frunzio, Andreas Wallraff, David Schuster, Johannes Majer, and Robert Schoelkopf, Fabrication and characterization of superconducting circuit QED devices for quantum computation, IEEE Trans. Appl. Supercond. **15**, 860 (2005).
[51] Chunhua Song, Thomas W. Heitmann, Michael P. DeFeo, Kang Yu, Robert McDermott, Matthew Neeley, John M. Martinis, and Britton L. T. Plourde, Microwave response of vortices in superconducting thin films of Re and Al, Phys. Rev. B **79**, 174512 (2009).
[52] Chunhua Song, Michael P. DeFeo, Kang Yu, and Britton L. T. Plourde, Reducing microwave loss in superconducting resonators due to trapped vortices, Appl. Phys. Lett. **95**, 232501 (2009).
[53] Anthony Megrant, Charles Neill, Rami Barends, Ben Chiaro, Yu Chen, Ludwig Feigl, Julian Kelly, Erik Lucero, Matteo Mariantoni, Peter J. J. O'Malley, Danial Sank, Amit Vainsencher, James Wenner, Theodor C. White, Yi Yin, Jian Zhao, Christopher J. Palmstrøm, John M. Martinis, and Andrew N. Cleland, Planar superconducting resonators with internal quality factors above one million, Appl. Phys. Lett. **100**, 113510 (2012).

[54] Alloy 430, grade ISO CuZn21Si3P, UNS C69300.
[55] Grade DIN 2.1030—CuSn8, UNS C52100.
[56] Rami Barends, James Wenner, Michael Lenander, Yu Chen, Radoslaw C. Bialczak, Julian Kelly, Erik Lucero, Peter O'Malley, Matteo Mariantoni, Daniel Sank, Haohua Wang, Theodor C. White, Yi Yin, Jian Zhao, Andrew N. Cleland, John M. Martinis, and J. J. A. Baselmans, Minimizing quasiparticle generation from stray infrared light in superconducting quantum circuits, Appl. Phys. Lett. **99**, 113507 (2011).
[57] Antonio D. Córcoles, Jerry M. Chow, Jay M. Gambetta, Chad Rigetti, James R. Rozen, George A. Keefe, Mary B. Rothwell, Mark B. Ketchen, and Matthias Steffen, Protecting superconducting qubits from radiation, Appl. Phys. Lett. **99**, 181906 (2011).
[58] Austin G. Fowler and John M. Martinis, Quantifying the effects of local many-qubit errors and nonlocal two-qubit errors on the surface code, Phys. Rev. A **89**, 032316 (2014).
[59] Rami Barends, Julian Kelly, Anthony Megrant, Daniel Sank, Evan Jeffrey, Yu Chen, Yi Yin, Ben Chiaro, Josh Mutus, Charles Neill, Peter O'Malley, Pedram Roushan, James Wenner, Theodor C. White, Andrew N. Cleland, and John M. Martinis, Coherent Josephson Qubit Suitable for Scalable Quantum Integrated Circuits, Phys. Rev. Lett. **111**, 080502 (2013).
[60] Alexander Teverovsky, in *Proceedings of the 42nd Annual IEEE International Reliability Physics Symposium, Phoenix, 2004* (IEEE, New York, 2004), p. 547.
[61] Eric D. Marquardt, J. P. Le, and Ray Radebaugh, in *Proceedings of the 11th International Cryocooler Conference, Keystone, CO, 2000* (Springer Science, New York, 2000), p. 681.
[62] Note that the DUT is a piecewise transmission line inhomogeneously filled with dielectric materials. Transforming the time t into distance is only possible with a detailed knowledge of geometries and materials for all regions of the DUT. Since this information is not known to a high degree of accuracy, we prefer to express all measured quantities as a function of t.
[63] Eric Bogatin, *Signal Integrity—Simplified*, 1st ed. (Prentice-Hall Professional Technical Reference, Upper Saddle River, NJ, 2003).
[64] John R. Rinehart *et al.*(to be published).
[65] David W. Abraham, George A. Keefe, Christian Lavoie, and Mary E. Rothwell, Chip mode isolation and cross-talk reduction through buried metal layers and through-vias, U.S. Patent No. 13/838,261 (19 July 2016).
[66] David W. Abraham, Jerry M. Chow, and Jay M. Gambetta, Symmetric placement of components on a chip to reduce cross talk induced by chip modes, U.S. Patent No. 8,972,921 (3 March 2015).
[67] Daniel T. Sank (private communication).
[68] Julie Tournet, Denise Gosselink, Guo-Xing Miao, Marc Jaikissoon, Deler Langenberg, Thomas G. McConkey, Matteo Mariantoni, and Zbigniew R. Wasilewski, Growth and characterization of epitaxial aluminum layers on gallium-arsenide substrates for superconducting quantum bits, Supercond. Sci. Technol. **29**, 064004 (2016).
[69] Patxi Duthil, Material properties at low temperature in *Proceedings of the CASCERN Accelerator School: Superconductivity for Accelerators, Erice, Italy, 2013* (CERN, Geneva, 2014), pp. 77–95.
[70] Matteo Mariantoni, Edwin P. Menzel, Frank Deppe, Miguel Á. Araque Caballero, Alexander Baust, Thomas Niemczyk, Elisabeth Hoffmann, Enrique Solano, Achim Marx, and Rudolf Gross, Planck Spectroscopy and Quantum Noise of Microwave Beam Splitters, Phys. Rev. Lett. **105**, 133601 (2010).
[71] Rami Barends, Ph.D. thesis, Delft University of Technology, 2009.
[72] Géraldine Haack, Ferdinand Helmer, Matteo Mariantoni, Florian Marquardt, and Enrique Solano, Resonant quantum gates in circuit quantum electrodynamics, Phys. Rev. B **82**, 024514 (2010).
[73] Matteo Mariantoni, Haohua Wang, Tsuyoshi Yamamoto, Matthew Neeley, Radoslaw C. Bialczak, Yu Chen, Michael Lenander, Erik Lucero, Aaron D. O'Connell, Daniel Sank, Martin Weides, James Wenner, Yi Yin, Jian Zhao, Alexander N. Korotkov, Andrew N. Cleland, and John M. Martinis, Implementing the quantum von Neumann architecture with superconducting circuits, Science **334**, 61 (2011).
[74] Matteo Mariantoni, Frank Deppe, Achim Marx, Rudolf Gross, Frank K. Wilhelm, and Enrique Solano, Two-resonator circuit quantum electrodynamics: A superconducting quantum switch, Phys. Rev. B **78**, 104508 (2008).
[75] Darren K. Brock, Elie K. Track, and John M. Rowell, Superconductor ICs: The 100-GHz second generation, IEEE Spectrum **37**, 40 (2000).
[76] Oleg A. Mukhanov, Energy-efficient single flux quantum technology, IEEE Trans. Appl. Supercond. **21**, 760 (2011).
[77] Deepnarayan Gupta, Dmitri E. Kirichenko, Vladimir V. Dotsenko, Robert Miller, Saad Sarwana, Andrei Talalaevskii, Jean Delmas, Robert J. Webber, Sergei Govorkov, Alexander F. Kirichenko, Igor V. Vernik, and Jia Tang, Modular, multi-function digital-RF receiver systems, IEEE Trans. Appl. Supercond. **21**, 883 (2011).
[78] See https://www.iarpa.gov/index.php/research-programs/c3.
[79] Note that we also perform magnetic tests by exposing all samples to a ultrahigh-pull neodymium rectangular magnet, with dimensions of $25.4 \times 25.4 \times 9.5$ mm^3 and a pull of 10.4 kg. We find magnetic fields with the same order of magnitude as in Table VI.
[80] http://www.diehl.com/en/diehl-metall/company/brands/diehl-metall-messing/ecomerica/alloys.html and http://www.otto-fuchs-duelken.de/fileadmin/user_upload/Downloads/OF2285_2014-02_EN.pdf.
[81] http://www.steelnumber.com/en/steel_alloy_composition_eu.php?name_id=1310.
[82] See http://www.lakeshore.com/Documents/LSTC_appendixI_l.pdf.
[83] R. M. Mueller, Christoph Buchal, T. Oversluizen, and Frank Pobell, Superconducting aluminum heat switch and plated press-contacts for use at ultralow temperatures, Rev. Sci. Instrum. **49**, 515 (1978).
[84] ISO AlMg1SiCu, UNS A96061.
[85] Note that $\alpha(4)$ can be accurately estimated from the data at http://www.cryogenics.nist.gov/MPropsMAY/6061%20Aluminum/6061_T6Aluminum_rev.htm.
[86] C. A. Swenson, Recommended values for the thermal expansivity of silicon from 0 to 1000 K, J. Phys. Chem. Ref. Data **12**, 179 (1983).
[87] See http://www.ece.rutgers.edu/~orfanidi/ewa/.