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Implementation of Natural Switching Surface Control for a Flyback Converter

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Implementation of Natural Switching Surface Control for a Flyback Converter

An Undergraduate Honors College Thesis

in the

Department of Electrical Engineering
College of Engineering
University of Arkansas
Fayetteville, AR

by

Ethan Williams

This thesis is approved.

Thesis Advisor:

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Abstract

The flyback converter is an extremely common topology used for DC/DC power conversion. Widely used methods to control the flyback converter include voltage mode and current mode controllers [1]-[5]. More recently, sliding mode control has been developed for the flyback converter [6]-[7]. While these control methods may be considered adequate, the Natural Switching Surface (NSS) sliding mode control method detailed in this thesis presents a more robust controller. NSS control eliminates the effects presented from variations in components and design as well as minimizes the effects from external disturbances [6]-[9].

This thesis steps through the complete design and implementation process of a NSS controller for a 100W flyback converter. The fundamental operational principals of the flyback converter will be described first. A detailed derivation of the NSS control for a flyback converter will follow. Simulations of the derived controller will be evaluated in MATLAB/Simulink[©]. The component level selection and design is detailed. Finally, the completed flyback with the NSS controller is fully tested in a laboratory setting and experimental results are analyzed.

Acknowledgments

Dedication

This thesis and all the work associated with it is dedicated to three people: God, my wife, and my parents. First, God has blessed me with the opportunity to come to University of Arkansas and have the rare opportunity to find my life's passion immediately out of high school. I've been so blessed over my college career and have felt the grace and presence of God though this whole project. Through my struggles, I've had the opportunity to grow stronger in my faith. Second, words cannot explain the appreciation I have for my wife, Kendra Williams. This senior year has challenged our first year of marriage, but I couldn't have asked for anyone better to go through life with. The understanding and comfort you provided me is beyond any expectation I could have set. All this hard work has been to advance our future, so this project is dedicated to her. Lastly, this project is also dedicated to my parents. Growing up, they have been nothing but encouraging and loving. I wouldn't be who I am or where I am with their help.

Table of Contents

List of Figures

List of Abbreviations

AC – Alternating Current

ADC – Analog-to-Digital Converter

BCM – Boundary Conduction Mode

CCM – Continuous Conduction Mode

DC – Direct Current

DCM – Discontinuous Conduction Mode

DSP – Digital Signal Processor

IC – Integrated Circuit

I/O – Input/Output Pins

MOSFET – Metal-Oxide-Semiconductor Field-Effect Transistor

NSS – Natural Switching Surface

PCB – Printed Circuit Board

RC – Resistor-Capacitor, in Reference to a Snubber Topology

RCD – Resistor-Capacitor-Diode, in reference to a Snubber Topology

Si – Silicon

SiC – Silicon-Carbide

SMC – Sliding Mode Control

SS – Sliding Surface

SSEES – Sustainable Smart Electrical Energy Systems (Research Group of University of

       Arkansas)

TI – Texas Instruments

V_{gs} – Voltage over Gate to Source of MOSFET

I. Introduction

1.1 Overview

Switch mode power converters are found everywhere in today's society. Power electronics are used in a wide range of applications including computers, cellphones, and power distribution and generation, to name a few. Through the use of switch mode power converters, voltage or current can be scaled or modified accordingly to fit the needs of an end application. Switch mode power converters can be used to convert power to or from DC/AC or be used to convert DC/DC or AC/AC. A prime example of this conversion need is a cellphone charger. A typical United State household wall receptacle is 120V AC. Typical cellphone batteries require between 5V to 12V DC to charge. A switch mode power converter can be implemented in the cellphone charger that will converter the input AC power to DC power then step the voltage down to the needed DC voltage level. Ideally, this conversion should be done in the most efficient way with the smallest packaging and as cheap as possible.

There are multiple different switch mode power converter topology options. Some common topologies include buck, boost, buck-boost, SEPIC, cûk, zeta, forward converter, push-pull, and flyback. Each topology has its benefits and limitations and selection is highly dependent upon the application. This thesis will focus on the design and control of a flyback converter. University of Arkansas' Sustainable Smart Electrical Energy Systems (SSEES) Research Group has previously analyzed multiple converter topologies for the use in renewal energy, specifically for the harnessing of solar power in microinverter applications. The flyback converter proved to be the most suitable candidate for this application based on their criteria [10]. Therefore, to assist SSEES further in their flyback microinverter applications, this research was performed.

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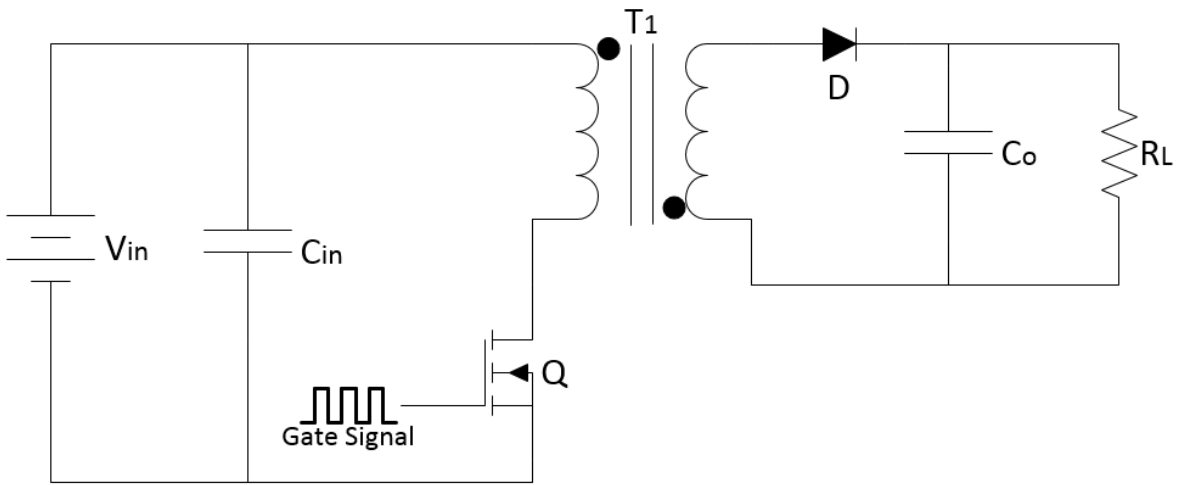
Figure 1: Basic Flyback Converter Topology

The flyback converter is an isolated DC/DC power converter. The use of a flyback transformer in the topology provides inherent isolation.
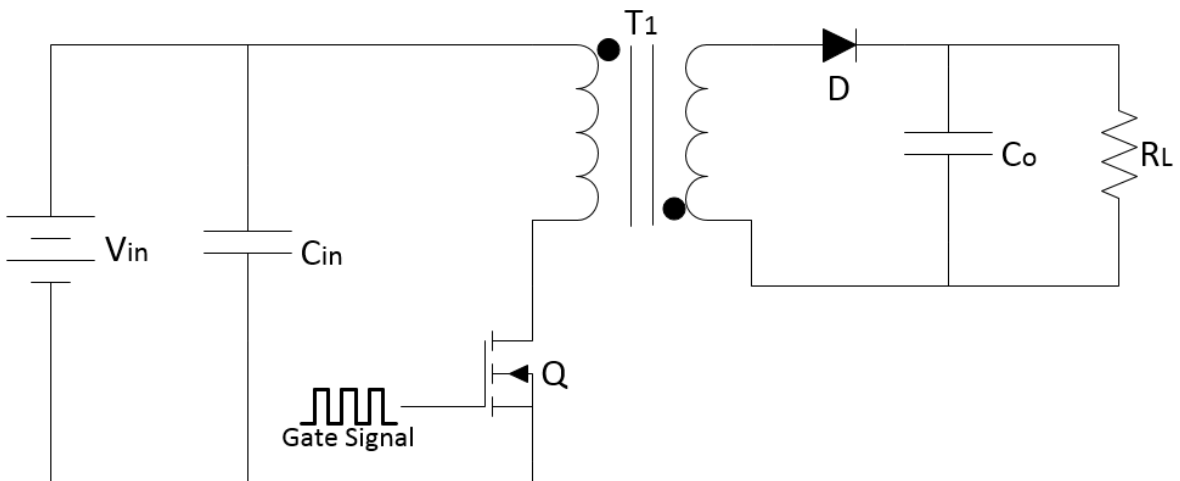
Figure 1 shows the basic flyback converter topology. The main components are the input and output capacitors, C_{in} and C_o respectively, the semiconductor switching device, Q, the flyback transformer, T_1, the output diode, D, and the load, R_L, represented here as purely resistive.

The most widely used method to control a traditional flyback converter is current mode control. Many industries, such as Linear Technologies, Texas Instruments (TI), and ON Semiconductor, provide integrated circuit (IC) chips that can perform the control function automatically, only requiring basic feedback signals [1][4][5]. While current mode control may be easy to implement, it does not necessarily mean that it is the most robust control method. The NSS control method detailed in this thesis provides many benefits over the traditional current mode control. NSS control utilizes natural trajectories intrinsically found in the operation of the flyback converter, making transient times minimal. NSS's operation is not hindered by component variations and reacts minimally to external disturbances [8] [9]. In addition, being a derivative of sliding mode control (SMC), the switching frequency can be ideally infinite if operating in Continuous Conduction Mode (CCM) to maintain the system on the sliding surface (SS), creating minimal ripple current in the output [6]. Realistically, infinite switching frequency is not possible, limited by sensory acquisition and processor calculation times, but nevertheless, actual NSS control implementation can minimize the current ripple generated.

The flyback converter presented in this thesis was designed for 100W maximum power conversion, taking an average input of 24V DC and stepping it up to 200V DC. 24V DC was considered to the normal output voltage of an individual solar panel. 200V DC was chosen to provided sufficiently high enough voltage for the input stage of a DC/AC inverter for 120V AC power grid tied microinverter applications. A Silicon (Si) metal-oxide-semiconductor field-effect transistor (MOSFET) was used as the switching semiconductor device. The flyback transformer was an off-the-shelf transformer available from Coilcraft, used to minimize

development costs. The digital signal processor (DSP) implemented was a Texas Instruments

TMS320F28335.

1.2 Organization of Thesis

This thesis is organized as follows: Chapter 2 details the basic operation of the flyback converter,

detailing governing equations and modes of operation. Chapter 3 provides a detailed derivation

of the Natural Switching Surface (NSS) controller for the flyback converter. Chapter 4 solves

the NSS control for Bound Conduction Mode (BCM) and analyzes the derived controller in

MATLAB/Simulink$^{©}$. Chapter 5 details the selection and justification of components for

discrete implementation of the flyback converter and controller. Chapter 6 details the code

developed in the DSP for NSS control implementation. Finally, Chapter 7 analyzes acquired

experimental data from laboratory testing of the NSS controlled flyback converter.

II. Flyback Converter Operation

2.1 Components and Operation Principle

Figure 2 shows a detailed version of the flyback converter topology. The main components are the input and output capacitors, C_{in} and C_o respectively, the semiconductor switching device, Q, the flyback transformer, T_1, the output diode, D, and the load, R_L, represented here as purely resistive. The flyback transformer's model, T_1, has been extended to explicitly show the magnetizing inductance, L_m, in parallel with an ideal transformer. Our variables of interest, or state variables, are the output voltage, v_0, and the transformer's magnetizing current, i_m.

Figure 3 and Figure 4 show the two states for the flyback converter from the switching of Q. Figure 3 shows the equivalent circuit for when Q is on. Figure 4 shows the equivalent circuit for when Q is off. In both instances, it is assumed that the on resistance and leakage current of Q and D is negligible. When Q is on, the input voltage, V_{in}, is connected in parallel to L_m and V_p and the primary current, i_p, rises linearly. Therefore, diode D is reverse biased, and no current flows through the secondary of the transformer. The required load energy is supplied from the output capacitor, C_o. During this on time, energy is stored in T_1's magnetic field. As Q turns off, the current stops flowing through the primary of T_1 and the voltages of V_p and V_s invert polarity due to Lenz and Faraday law [11]. The diode, D, now becomes forward biased and allows current to flow to the output, therefore decreasing the energy stored in the magnetic field of T_1. This current recharges the output capacitor, C_o, and supplies energy to the load. Since the output voltage is connected in parallel to the secondary of the transformer, the secondary current, i_s, will decrease linearly [12].
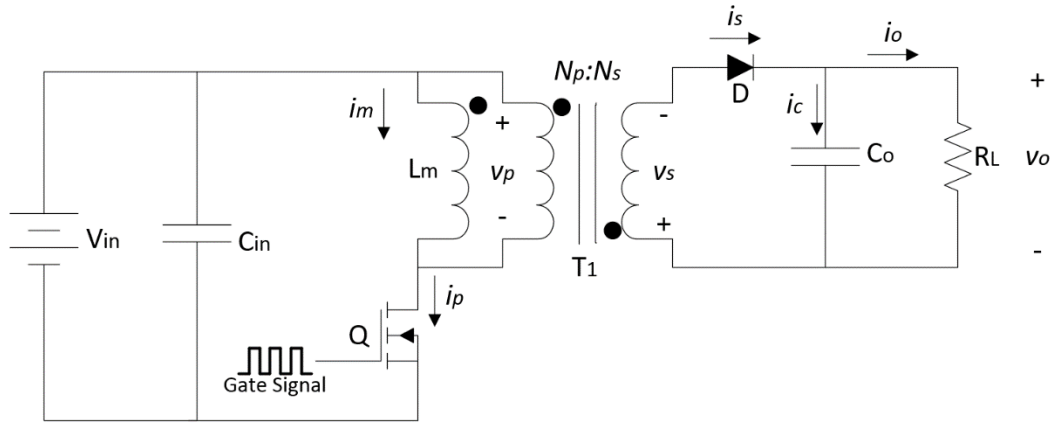
Figure 2: Detailed Flyback Converter
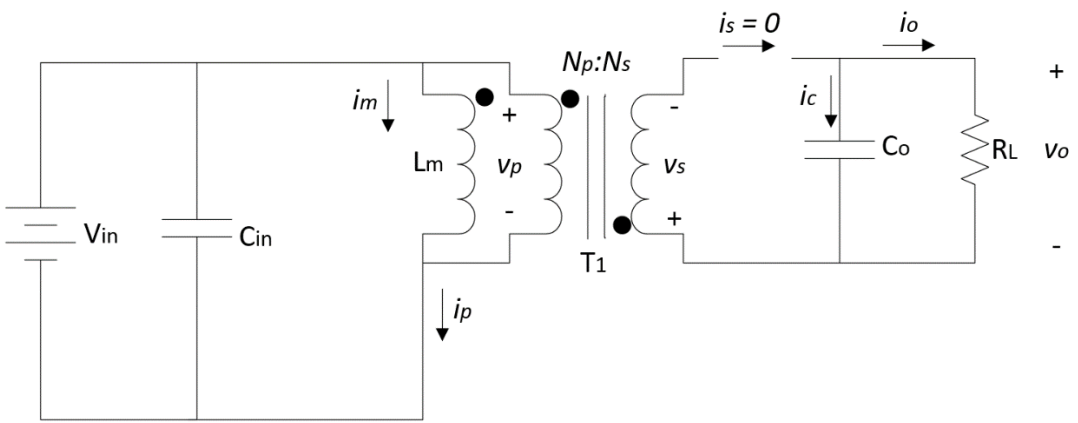
Figure 3: Q_{on} Equivalent Circuit
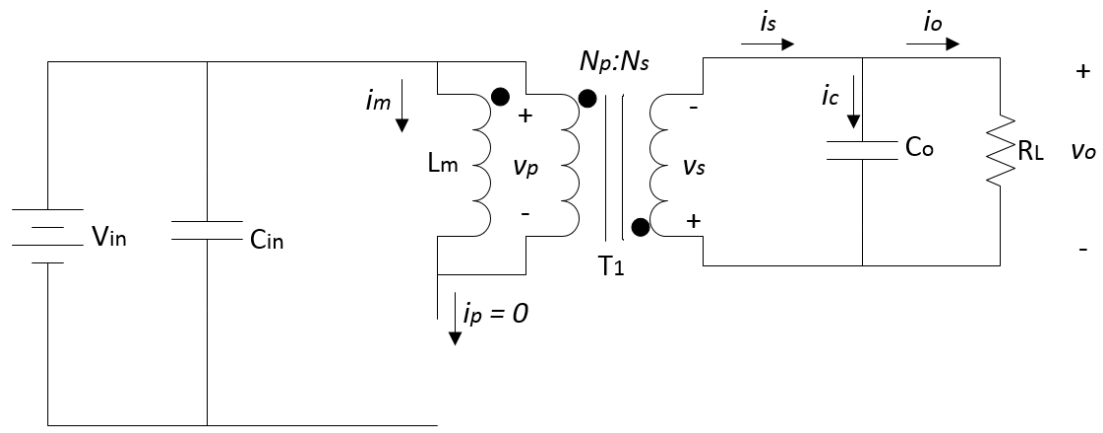
Figure 4: Q_{off} Equivalent Circuit

2.2 On-State Equations

During Q_{on}, the primary of the transformer, V_p, is connected in parallel with V_{in}. The primary current, i_p, is equal to the magnetizing current, i_m, and is described as

$$\frac{di_m}{dt} = \frac{V_{in}}{L_m} \tag{1}$$

This can be seen to cause a linear increase in i_m with an increase in time. The secondary current, i_s, is zero during the on time because the diode, D, is reversed biased. The secondary voltage is related to the primary voltage by the turns ratio.

$$v_s = \frac{N_s}{N_p} v_p \tag{2}$$

The output voltage can be determined by the output capacitor, C_o. The output current, i_o, is observed to be the negative of the output capacitor current, i_c, since i_s is equal to zero.

$$\frac{dv_o}{dt} = -\frac{i_o}{C_o} \tag{3}$$

2.3 Off-State Equations

During Q_{off}, the primary current, i_p, is equal to zero since Q blocks the current. The primary and secondary voltage will flip polarity due T_1's magnetic field decreasing, forcing D to become forward biased and the secondary current to conduct. The secondary current can be related to the magnetizing current flowing between the ideal transformer and L_m by the turns ratio.

$$i_s = \frac{N_p}{N_s} i_m \tag{4}$$

The output voltage will be reflected back to the primary by the turns ratio. Note that v_o is equal to $-v_s$.

$$v_p = -v_o \frac{N_p}{N_s} \tag{5}$$

Therefore, L_m's inductor equation can be written as

$$-v_o \frac{N_p}{N_s} = L_m \frac{di_m}{dt}$$

$$\frac{di_m}{dt} = \frac{-v_o \frac{N_p}{N_s}}{L_m} \tag{6}$$

The output voltage is again determined by the output capacitor.

$$i_s - i_o = C_o \frac{dv_o}{dt}$$

$$\frac{dv_o}{dt} = \frac{\left(\frac{N_p}{N_s} i_m\right) - i_o}{C_o} \tag{7}$$

2.2 Continuous, Boundary, and Discontinuous Modes of Operation

Depending upon the ending value the magnetizing current, i_m, each switching cycle, the flyback

converter can be classified into three different modes of operation: continuous conduction mode

(CCM), boundary conduction mode (BCM), and discontinuous conduction mode (DCM).

CCM occurs when the magnetic field in the transformer never completely depletes each

switching cycle and therefore the magnetizing current never reaches zero. BCM is classified as

when the magnetizing current reaches zero just as the switch is turned back on. BCM is the

transition between CCM and DCM. DCM occurs when the magnetizing current reaches zero

and stays at zero for the remainder of the switching cycle until Q is turned back on. Figure 5

shows the magnetizing current for all three modes of operation in steady-state.
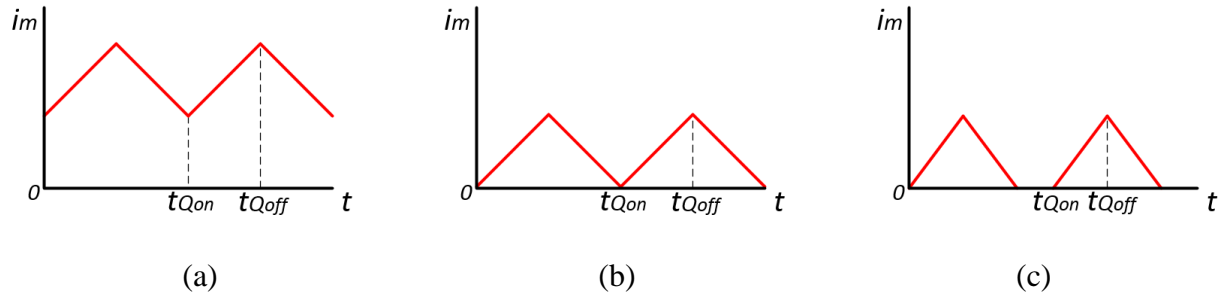
Figure 5: Flyback Modes of Operation; CCM (a), BCM (b), and CCM (c)

Comparing CCM and DCM applications for the flyback converter, CCM is more appropriate for constant output voltage situations while DCM is more desirable for constant output current situations. In DCM and BCM, the flyback converter can react to transients in output load changes and input voltage swiftly compared to CCM. One downfall of DCM and BCM is larger currents trough the transformer compared to CCM at the same operating conditions [12]. [13] performed a detailed analysis for CCM and BCM comparing four major areas of losses: conduction losses, switching losses, diode losses, and transformer losses. The conclusion was that a decision of operating mode based solely on losses was not clear due to each mode having significantly higher and lower losses in different areas. [13] continued with an operational comparison for CCM and BCM. Ultimately, it was concluded that the benefits of BCM outweighed CCM. One advantage of BCM was inherent short circuit output protection. Another significant benefit of BCM is zero current switching for Q at turn on and D at turn off. This minimizes current spikes associated from Q at turn on and EMI generated from D at turn off [13]. Therefore, the develop NSS controller will be designed to operate at BCM for all loading conditions.

2.3 Ideal Flyback Converter Waveforms for BCM

Figure 6 details the expected waveforms from an ideal flyback converter operating in BCM in steady-state operation [12]. These waveforms are a graphical representation of (1)-(7). The duty cycle is 50% in this representation. The output voltage is represented as a sinusoidal ripple, though realistically this waveform will differ significantly based off of the output capacitance, load, duty cycle, and switching frequency.
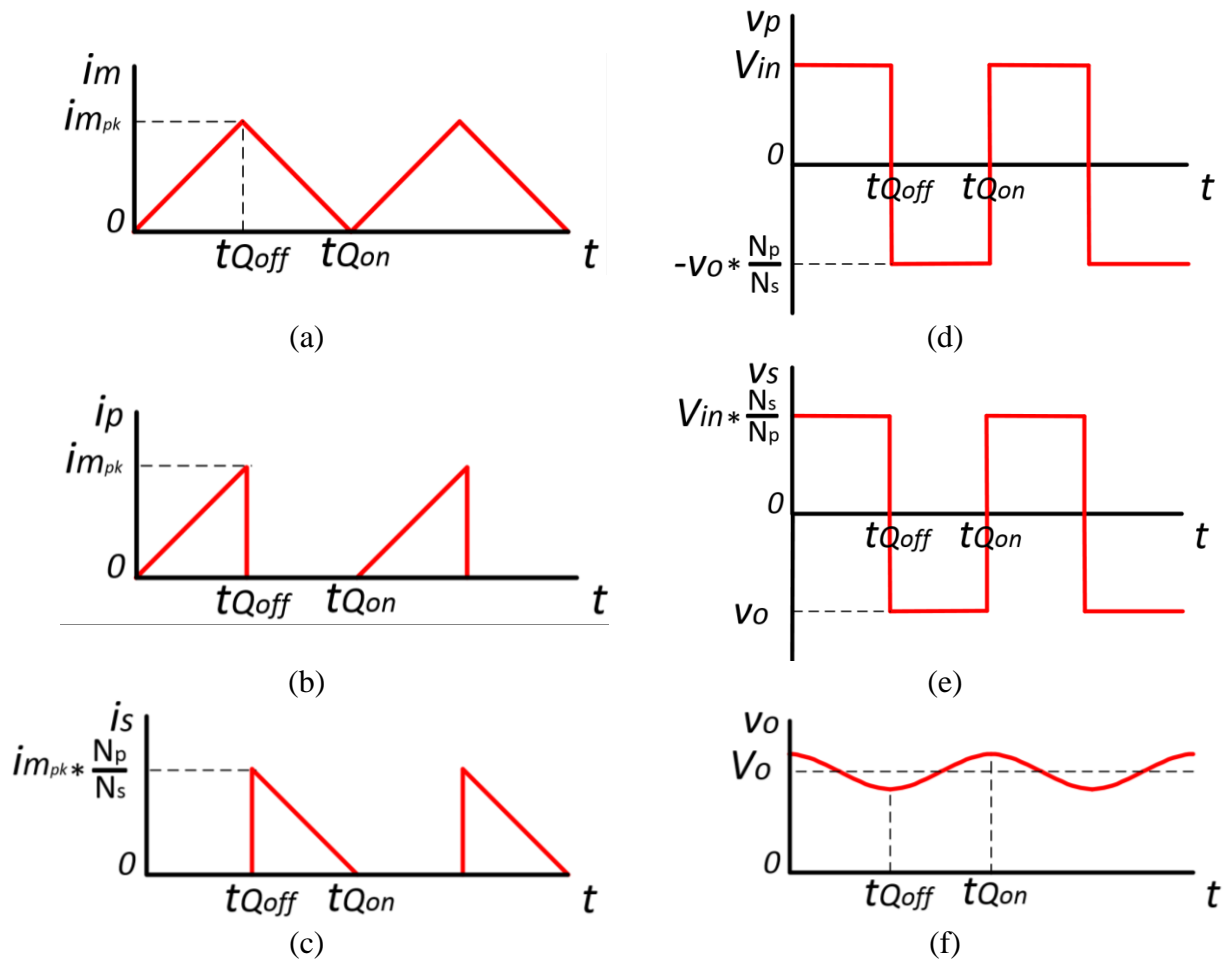
Figure 6: Ideal Flyback Converter Waveforms for BCM Operation

(a) Magnetizing Current, (b) Primary Current, (c) Secondary Current, (d) Primary Voltage, (e) Secondary Voltage, and (f) Output Voltage

III. Natural Switching Surface (NSS) Derivation

3.1 Normalization Equations

The first step in deriving the natural switching surface for a generic flyback converter is to normalize the equations that describe the operation of the flyback converter [8]. The trajectories derived later in the subsections of this chapter are in the v_{on} vs. i_{mn} plane. This eliminates the requirement for converter specific variables and operating conditions and allows for a general representation of the NSS for any flyback converter. Because the flyback converter involves a transformer, a reference side must be determined for the normalizing equations. The secondary side is selected as the reference side. Therefore, V_r, i_r, and Z_o are derived and considered secondary base variables. (8)(58)(10)(12) and their derivatives (9)(11)(13) detail the equations used to normalize the flyback converter's operating equations referred to the secondary side [8] [14].

$$v_{xn} = \frac{v_x}{V_r} \tag{8}$$

$$dv_{xn} = \frac{dv_x}{V_r} \tag{9}$$

$$i_{xn} = \frac{i_x}{\frac{V_r}{Z_o}} \tag{10}$$

$$di_{xn} = \frac{di_x}{\frac{V_r}{Z_o}} \tag{11}$$

$$t_n = \frac{t}{T_o} \tag{12}$$

$$dt_n = \frac{dt}{T_o} \tag{13}$$

where v_x, i_x, and t are the variables that are to be normalized. It can be observed that $\frac{V_r}{Z_o}$ create a reference current, i_r, which i_x is normalized against in (10)(11). To normalize a variable that is

referred to the primary side, the normalizing base variables must be referred to the primary side.

Reflecting the voltage base from the secondary to the primary requires V_r to be multiplied by $\frac{N_p}{N_s}$.

Reflecting the current base from the secondary to the primary requires i_r to be multiplied by $\frac{N_s}{N_p}$

[11] [14]. (14)-(17) detail the equations used to normalize the converter specific variables with the correct base reference.

$$V_{inn} = \frac{V_{in}}{V_r \frac{N_p}{N_s}} \tag{14}$$

$$i_{mn} = \frac{i_m}{\frac{V_r}{Z_o} \frac{N_s}{N_p}} \tag{15}$$

$$v_{on} = \frac{v_o}{V_r} \tag{16}$$

$$i_{on} = \frac{i_o}{\frac{V_r}{Z_o}} \tag{17}$$

Z_o is the characteristic equation of the output filter during the off state. Figure 7 shows the output filter during the off state, where the secondary inductance, L$_s$, is equal to L$_m$, referenced to the secondary side by the transformer turns ratio [11].

$$L_s = L_m \left(\frac{N_s}{N_p}\right)^2 \tag{18}$$

The characteristic impedance, Z_o, can be derived by determining the ratio of the amplitude of the voltage to the amplitude of the current [15]. Therefore, we must find the equations that describe the voltage and current. The inductor and capacitor equations are

$$-v_o = L_m \left(\frac{N_s}{N_p}\right)^2 \frac{di_s}{dt} \tag{19}$$
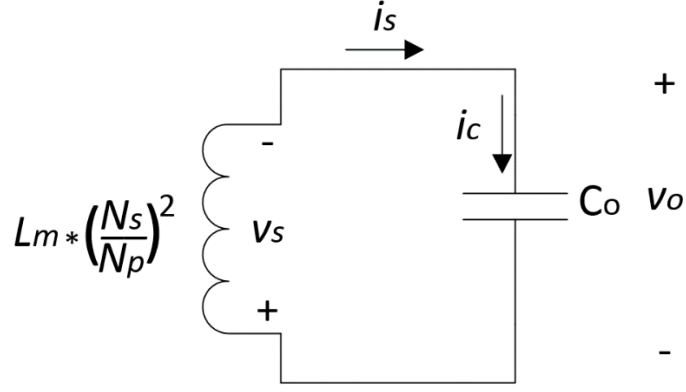
Figure 7: Output Filter During Off State

$$i_c = C_o \frac{dv_o}{dt} \tag{20}$$

It can be observed that $i_s = i_c$. Solving for the voltage equation first, we can take the derivative

of (20) and substitute the result into (19)

$$\frac{di_s}{dt} = C_o \frac{d^2 v_o}{dt^2} \tag{21}$$

$$-v_0 = L_m \left(\frac{N_s}{N_p}\right)^2 C_o \frac{d^2 v_o}{dt^2}$$

$$\frac{d^2 v_o}{dt^2} + \frac{v_o}{L_m C_o \left(\frac{N_s}{N_p}\right)^2} = 0 \tag{22}$$

Solving for this second order differential equation (22), it can be assumed that the general

solution has the form of [15]

$$v_0(t) = A * cos(\omega_o t + \varphi) \tag{23}$$

where the first and second derivative of (23) equals

$$\frac{dv_o}{dt} = -A\omega_o * \sin(\omega_o t + \varphi) \tag{24}$$

$$\frac{d^2 v_o}{dt^2} = -A\omega_o^2 * \cos(\omega_o t + \varphi) \tag{25}$$

Replacing (23) and (25) into (22) results in

13

$$-A\omega_o^2 * \cos(\omega_o t + \varphi) + \frac{A * \cos(\omega_o t + \varphi)}{L_m C_o \left(\frac{N_s}{N_p}\right)^2} = 0 \qquad (26)$$

Canceling like terms in both add-ins results in a simplified expression for ω_o, the natural frequency [15].

$$-\omega_o^2 + \frac{1}{L_m C_o \left(\frac{N_s}{N_p}\right)^2} = 0$$

$$\omega_o = \frac{1}{\frac{N_s}{N_p}\sqrt{L_m C_o}} \qquad (27)$$

The initial conditions of the circuit can be identified from the end of the on-state of the flyback converter. The secondary current, $i_s(0) = 0$, and the capacitor voltage can be assumed to be equal to an arbitrary voltage, $v_0(0) = V_a$. Plugging into (23), we see that

$$v_0(0) = A * \cos(\varphi) = V_a \qquad (28)$$

To eliminate φ, we can look at the initial conditions of (20) and plug in the derivative, (24).

$$i_c(0) = 0 = C_o \frac{dv_o}{dt}$$

$$0 = -C_o A \omega_o * \sin(\varphi) \qquad (29)$$

Observing both (28) and (29), we can solve for φ. $A \neq 0$ in (28). Therefore for (29) to be true

$$\varphi = 0 \qquad (30)$$

which allows (28) to simplify to

$$A = V_a \qquad (31)$$

Finally, (23) can be completely written as

$$v_0(t) = V_a \cos\left(\frac{1}{\frac{N_s}{N_p}\sqrt{L_m C_o}} * t\right) \qquad (32)$$

The current equation, (20), can be completed using the derivative of equation (32).

14

$$i_s(t) = -C_0 V_a \frac{1}{\frac{N_s}{N_p}\sqrt{L_m C_o}} * \sin\left(\frac{1}{\frac{N_s}{N_p}\sqrt{L_m C_o}} * t\right) \tag{33}$$

With both the voltage, (32), and current, (33), equations identified, the characteristic equation

can now be computed. Taking the magnitudes of (32) and (33) and plugging into the equation

for Z_o [15]

$$Z_o = \frac{\hat{v}_0}{\hat{\imath}_0}$$

$$Z_o = \frac{V_a}{C_0 V_a \frac{1}{\frac{N_s}{N_p}\sqrt{L_m C_o}}}$$

$$Z_o = \frac{N_s}{N_p}\sqrt{\frac{L_m}{C_0}} \tag{34}$$

To find T_o for the normalization of time t, equation (27) can be extended to find f_0 and therefore

T_o.

$$\omega_o = 2\pi f_o = \frac{1}{\frac{N_s}{N_p}\sqrt{L_m C_o}}$$

$$f_o = \frac{1}{2\pi \frac{N_s}{N_p}\sqrt{L_m C_o}} \tag{35}$$

$$T_o = 2\pi \frac{N_s}{N_p}\sqrt{L_m C_o} \tag{36}$$

To recap this subsection, the variable specific normalizing equations are

$$V_{inn} = \frac{V_{in}}{V_r \frac{N_p}{N_s}} \tag{14}$$

$$i_{mn} = \frac{i_m}{\frac{V_r}{Z_o}\frac{N_s}{N_p}} \tag{15}$$

$$v_{on} = \frac{v_o}{V_r} \tag{16}$$

$$i_{on} = \frac{i_o}{\frac{V_r}{Z_o}} \tag{17}$$

where v_x, i_x, and t are the variables that are to be normalized and

$$Z_o = \frac{N_s}{N_p}\sqrt{\frac{L_m}{C_0}} \tag{34}$$

$$T_o = 2\pi\frac{N_s}{N_p}\sqrt{L_m C_o} \tag{36}$$

3.2 Normalization and Trajectory of On-State Equations

The on-state equations were previously defined as

$$\frac{di_m}{dt} = \frac{V_{in}}{L_m} \tag{1}$$

$$\frac{dv_o}{dt} = -\frac{i_o}{C_o} \tag{3}$$

Using (14)(15)(16)(17), the on-state equations can be normalized [14]. Starting with (1)

$$\frac{\frac{V_r}{Z_o}\frac{N_s}{N_p}\left(\frac{di_m}{\frac{V_r}{Z_o}\frac{N_s}{N_p}}\right)}{T_o\left(\frac{dt}{T_o}\right)} = \frac{\left(\frac{V_{in}}{\frac{N_p}{V_r}\frac{N_p}{N_s}}\right)V_r\frac{N_p}{N_s}}{L_m}$$

$$\frac{\frac{V_r}{Z_o}\frac{N_s}{N_p}di_{mn}}{T_o\,dt_n} = \frac{V_{inn}V_r\frac{N_p}{N_s}}{L_m}$$

$$\frac{di_{mn}}{dt_n} = V_{inn}\frac{Z_o T_o}{L_m}\left(\frac{N_p}{N_s}\right)^2$$

16

$$\frac{di_{mn}}{dt_n} = V_{inn} \frac{\frac{N_s}{N_p}\sqrt{\frac{L_m}{C_0}} 2\pi \frac{N_s}{N_p}\sqrt{L_m C_o}}{L_m} \left(\frac{N_p}{N_s}\right)^2$$

$$\frac{di_{mn}}{dt_n} = V_{inn} 2\pi \tag{37}$$

Continuing with the normalization of (3)

$$\frac{V_r * \left(\frac{dv_o}{V_r}\right)}{T_o * \left(\frac{dt}{T_o}\right)} = \frac{-\left(\frac{i_o}{V_r} * Z_o\right) * \frac{V_r}{Z_o}}{C_o}$$

$$\frac{V_r * dv_{on}}{T_o * dt_n} = \frac{-i_{on} * \frac{V_r}{Z_o}}{C_o}$$

$$\frac{dv_{on}}{dt_n} = -i_{on} * \frac{T_o}{Z_o C_o}$$

$$\frac{dv_{on}}{dt_n} = -i_{on} * \frac{2\pi \frac{N_s}{N_p}\sqrt{L_m C_o}}{C_o \frac{N_s}{N_p}\sqrt{\frac{L_m}{C_0}}}$$

$$\frac{dv_{on}}{dt_n} = -i_{on} 2\pi \tag{38}$$

To relate (37) and (38) to the v_{on} vs. i_{mn} plane, it can be observed that dividing the two

equations will provide the slope of the line in the plane.

$$\frac{\frac{di_{mn}}{dt_n}}{\frac{dv_{on}}{dt_n}} = \frac{V_{inn} 2\pi}{-i_{on} 2\pi}$$

$$\frac{di_{mn}}{dv_{on}} = \frac{-V_{inn}}{i_{on}} \tag{39}$$

It is observable that the line has a constant slope for a constant load. As the load changes, the

slope of the line will also change. Also, since the slope of the line is negative, the line will be a

downward sloping line in the plane. Integrating equation (39)

$$\int di_{mn} = \int \frac{-V_{inn}}{i_{on}} dv_{on}$$

$$i_{mn} = -v_{on} \frac{V_{inn}}{i_{on}} + C \tag{40}$$

where C is a constant from integration. C is a design parameter that is used to shift the on-trajectory into a desired location, detailed in Chapter 4. Rearranging (40) to equal zero defines the normalized on-trajectory of the converter, λ_{on}.

$$\lambda_{on} = i_{mn} + v_{on} \frac{V_{inn}}{i_{on}} + C \tag{41}$$

3.3 Normalization and Trajectory of Off-State Equations

The off-state equations were previously defined as

$$\frac{di_m}{dt} = \frac{-v_o \frac{N_p}{N_s}}{L_m} \tag{6}$$

$$\frac{dv_o}{dt} = \frac{\left(\frac{N_p}{N_s} * i_m\right) - i_o}{C_o} \tag{7}$$

(14)(17) can be used to normalize (6) [14].

$$\frac{\frac{V_r}{Z_o} \frac{N_s}{N_p} \left(\frac{di_m}{\frac{V_r}{Z_o} \frac{N_s}{N_p}}\right)}{T_o * \left(\frac{dt}{T_0}\right)} = \frac{-\left(\frac{v_0}{V_r}\right) V_r \frac{N_p}{N_s}}{L_m}$$

$$\frac{\frac{V_r}{Z_o} \frac{N_s}{N_p} di_{mn}}{T_o * dt_n} = \frac{-v_{on} V_r \frac{N_p}{N_s}}{L_m}$$

$$\frac{di_{mn}}{dt_n} = -v_{on} \frac{Z_o T_o}{L_m} \left(\frac{N_p}{N_s}\right)^2$$

18

$$\frac{di_{mn}}{dt_n} = -v_{on}\frac{\frac{N_s}{N_p}\sqrt{\frac{L_m}{C_0}}2\pi\frac{N_s}{N_p}\sqrt{L_mC_o}}{L_m}\left(\frac{N_p}{N_s}\right)^2$$

$$\frac{di_{mn}}{dt_n} = -v_{on}2\pi \tag{42}$$

Continuing with normalizing (7)

$$\frac{V_r\left(\frac{dv_o}{V_r}\right)}{T_o\left(\frac{dt}{T_o}\right)} = \frac{\left(\frac{i_m}{\frac{V_r}{Z_o}\frac{N_s}{N_p}}\right)\frac{V_r}{Z_o}\frac{N_s}{N_p}\frac{N_p}{N_s}}{C_o} - \frac{\left(\frac{i_o}{\frac{V_r}{Z_o}}\right)\frac{V_r}{Z_o}}{C_o}$$

$$\frac{V_r dv_{on}}{T_o dt_n} = \frac{i_{mn}\frac{V_r}{Z_o}}{C_o} - \frac{i_{on}\frac{V_r}{Z_o}}{C_o}$$

$$\frac{dv_{on}}{dt_n} = \frac{T_0}{C_o Z_o}(i_{mn} - i_{on})$$

$$\frac{dv_{on}}{dt_n} = \frac{2\pi\frac{N_s}{N_p}\sqrt{L_mC_o}}{C_o\frac{N_s}{N_p}\sqrt{\frac{L_m}{C_0}}}(i_{mn} - i_{on})$$

$$\frac{dv_{on}}{dt_n} = 2\pi(i_{mn} - i_{on}) \tag{43}$$

To solve for the complete trajectory during the off state, (42) and (43) must be solved together.

Taking the derivative of (42) and substituting into (43) results in

$$\frac{d^2i_{mn}}{dt_n^2} = -2\pi\frac{dv_{on}}{dt_n}$$

$$\frac{dv_{on}}{dt_n} = \frac{-1}{2\pi}\frac{d^2i_{mn}}{dt_n^2} \tag{44}$$

$$2\pi(i_{mn} - i_{on}) = \frac{-1}{2\pi}\frac{d^2i_{mn}}{dt_n^2}$$

$$2\pi i_{mn} + \frac{1}{2\pi}\frac{d^2i_{mn}}{dt_n^2} - 2\pi i_{on} = 0 \tag{45}$$

Laplace transform can be used to solve (45) [14].

$$2\pi\, I_{mn}(s) + \frac{1}{2\pi}\left(s^2 I_{mn}(s) - si_{mn}(0) - \frac{di_{mn}(0)}{dt_n}\right) - 2\pi\frac{i_{on}}{s} = 0$$

$$I_{mn}(s)(s^2 + (2\pi)^2) = si_{mn}(0) + \frac{di_{mn}(0)}{dt_n} + (2\pi)^2\frac{i_{on}}{s}$$

$$I_{mn}(s) = i_{mn}(0)\frac{s}{(s^2 + (2\pi)^2)} + \frac{di_{mn}(0)}{dt_n}\frac{1}{(s^2 + (2\pi)^2)} + i_{on}\frac{(2\pi)^2}{s(s^2 + (2\pi)^2)} \qquad (46)$$

All of the add-ins are in a standard inverse Laplace format except the last add-in of (46). Using the method of partial fractions

$$i_{on}\frac{(2\pi)^2}{s(s^2 + (2\pi)^2)} = i_{on}\frac{1}{s} - i_{on}\frac{s}{(s^2 + (2\pi)^2)} \qquad (47)$$

Substituting (47) into (46) and inverse Laplace transforming, the result is

$$i_{mn}(t_n) = i_{mn}(0)\cos(2\pi t_n) + \frac{\dfrac{di_{mn}(0)}{dt_n}}{2\pi}\sin(2\pi t_n) + i_{on} - i_{on}\cos(2\pi t_n)$$

$$i_{mn}(t_n) = i_{on} + \cos(2\pi t_n)\left(i_{mn}(0) - i_{on}\right) + \frac{di_{mn}(0)}{dt_n}\frac{1}{2\pi}\sin(2\pi t_n) \qquad (48)$$

(48) can be seen to be dependent upon t_n which is not conductive for a normalization of the converter. Therefore, the next steps are performed with the goal of removing the dependence of t_n. Using the trigonometric identity $a * \sin(x) + b * \cos(x) = \sqrt{a^2 + b^2} * \sin\left(x + \tan^{-1}\left(\frac{b}{a}\right)\right)$ to (48) [16]

$$i_{mn}(t_n) = i_{on} + \sqrt{a^2 + b^2} * \sin\left(2\pi t_n + \tan^{-1}\left(\frac{b}{a}\right)\right) \qquad (49)$$

where

$$a = \frac{di_{mn}(0)}{dt_n}\frac{1}{2\pi} \qquad (50)$$

$$b = (i_{mn}(0) - i_{on}) \qquad (51)$$

taking the derivative of (49) and equating to (42) results in

$$-v_{on}2\pi = 2\pi\sqrt{a^2 + b^2} * \cos\left(2\pi t_n + \tan^{-1}\left(\frac{b}{a}\right)\right) \tag{52}$$

To remove the tragicomic function dependent upon t_n in (52), the tragicomic identity

$\cos(\sin^{-1}(x)) = \sqrt{1 - x^2}$ can be applied [17] [14]. Solving (49) for the arcsin

$$\sin\left(2\pi t_n + \tan^{-1}\left(\frac{b}{a}\right)\right) = \frac{i_{mn} - i_{on}}{\sqrt{a^2 + b^2}}$$

$$2\pi t_n + \tan^{-1}\left(\frac{b}{a}\right) = \sin^{-1}\left(\frac{i_{mn} - i_{on}}{\sqrt{a^2 + b^2}}\right) \tag{53}$$

(53) can now be substituted into the inside of the tragicomic function in (52) and simplified with

the tragicomic identity discussed above

$$-v_{on}2\pi = 2\pi\sqrt{a^2 + b^2} * \cos\left(\sin^{-1}\left(\frac{i_{mn} - i_{on}}{\sqrt{a^2 + b^2}}\right)\right)$$

$$-v_{on}2\pi = 2\pi\sqrt{a^2 + b^2}\sqrt{1 - \left(\frac{i_{mn} - i_{on}}{\sqrt{a^2 + b^2}}\right)^2}$$

$$v_{on}^2 = (a^2 + b^2)\left(1 - \left(\frac{i_{mn} - i_{on}}{\sqrt{a^2 + b^2}}\right)^2\right)$$

$$v_{on}^2 = (a^2 + b^2) + (i_{mn} - i_{on})^2$$

$$(a^2 + b^2) = v_{on}^2 + (i_{mn} - i_{on})^2 \tag{54}$$

where a and b are still

$$a = \frac{di_{mn}(0)}{dt_n}\frac{1}{2\pi} \tag{50}$$

$$b = (i_{mn}(0) - i_{on}) \tag{51}$$

Observing (54), the equation is in the format of a circle. In the v_{on} vs. i_{mn} plane, the center of

the circle would be $(0, i_{on})$ and the radius, r, would be

$$r = \sqrt{a^2 + b^2} \tag{55}$$

$$r = \sqrt{\left(\frac{di_{mn}(0)}{dt_n}\frac{1}{2\pi}\right)^2 + (i_{mn} - i_{on})^2} \tag{56}$$

which is completely dependent upon the operating conditions of the converter. Rearranging (54) to equal zero, the normalize off-state trajectory can be defined as

$$\lambda_{off} = v_{on}^2 + (i_{mn} - i_{on})^2 - (a^2 + b^2) \tag{57}$$

3.4 Summary of the Normalizing Equations and Normalized Trajectories

This subsection serves to summarize the three previous subsections in this chapter for the

normalizing equations and the normalized trajectories [14]. The converter specific normalizing

equations are

$$V_{inn} = \frac{V_{in}}{V_r \frac{N_p}{N_s}} \tag{14}$$

$$i_{mn} = \frac{i_m}{\frac{V_r}{Z_o}\frac{N_s}{N_p}} \tag{15}$$

$$v_{on} = \frac{v_o}{V_r} \tag{16}$$

$$i_{on} = \frac{i_o}{\frac{V_r}{Z_o}} \tag{17}$$

where v_x, i_x, and t are the variables that are to be normalized and

$$Z_o = \frac{N_s}{N_p}\sqrt{\frac{L_m}{C_0}} \tag{34}$$

$$T_o = 2\pi\frac{N_s}{N_p}\sqrt{L_m C_o} \tag{36}$$

The on-state normalized trajectory was derived as

$$\lambda_{on} = i_{mn} + v_{on}\frac{V_{inn}}{i_{on}} + C \tag{41}$$

22

where C is a design parameter selected to place the converter in the desired operating condition.

(41) is observed to be a downward sloping line in the v_{on} vs. i_{mn} plane. Finally, the off-state

trajectory was derived as

$$(a^2 + b^2) = v_{on}^2 + (i_{mn} - i_{on})^2 \tag{54}$$

where

$$a = \frac{di_{mn}(0)}{dt_n} \frac{1}{2\pi} \tag{50}$$

$$b = (i_{mn}(0) - i_{on}) \tag{51}$$

which in the v_{on} vs. i_{mn} plane is a circle with the center located at $(0, i_{on})$ and the radius, r,

equal to

$$r = \sqrt{\left(\frac{di_{mn}(0)}{dt_n} \frac{1}{2\pi}\right)^2 + (i_{mn} - i_{on})^2} \tag{56}$$

r is completely dependent upon the operating conditions of the converter. Rearranged to equal

zero, the off-state trajectory can be defined as

$$\lambda_{off} = v_{on}^2 + (i_{mn} - i_{on})^2 - (a^2 + b^2) \tag{57}$$

IV. Proposed Control Law and Simulations

4.1 Graphical Analysis of the NSS Trajectories

Figure 8 shows a graph of the NSS trajectories derived in Chapter 3 and summarized in Section

3.4. This graph is for a generic flyback converter, with arbitrary trajectory placement in the

v_{on} vs. i_{mn} plane. As previously described, the on-state trajectory is a downward sloping line

and the off-state trajectory is a circle, generically pictured here with a center at (0,0). This

section attempts to explain how the two trajectories interact with each other and how they relate

to the operation of the converter.

Looking at the v_{on} vs. i_{mn} plane and thinking of the flyback converter as a whole, immediately

quadrants of the plane can be identified as unobtainable or undesirable areas of operation based

off the variable's polarity [14]. i_{mn} can only be positive for the flyback converter to be

operating properly. Therefore, i_{mn} would not be obtainable in quadrants III or IV. v_{on} would

not be desired to be negative either. This would imply that the load was transferring power to
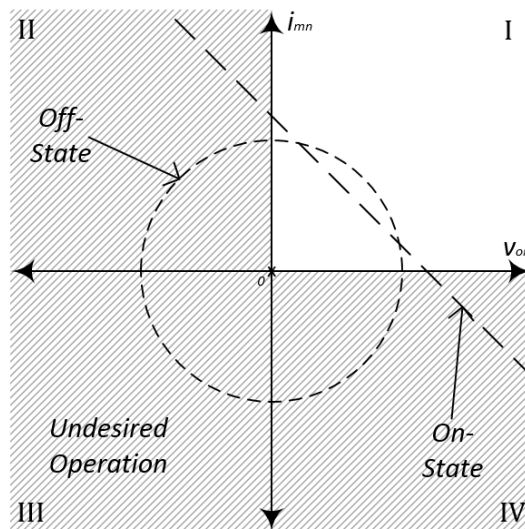
Figure 8: Generic NSS Graph

the input of the converter. Therefore, v_{on} should not operate in quadrants II or III. That leaves only quadrant I as the operational quadrant which satisfies both variables' conditions. In quadrant I, i_{mn} and v_{on} are both positive and the flyback converter would be transferring power to the load. The undesired quadrants have been grayed out in Figure 8.

Movement along the trajectories during steady-state can be determined by considering the flyback operation in each state [14]. As discussed in II. Flyback Converter Operation, during the on-state i_m is increasing, storing energy in the transformer's magnetic field from V_{in}, and v_o is decreasing, due to the load using up the energy stored in the output capacitor. Therefore, the converter operation would force the converter to slide up the trajectory during the on-state, as shown in Figure 9(a). During the off-state, i_m is decreasing, supplying the transformer's stored energy to the load and output capacitor, while v_o is increasing, due to the transformer's supplied energy. Therefore, operation would force the converter to slide down the trajectory during the off-state, as shown in Figure 9(b).

(a)   (b)
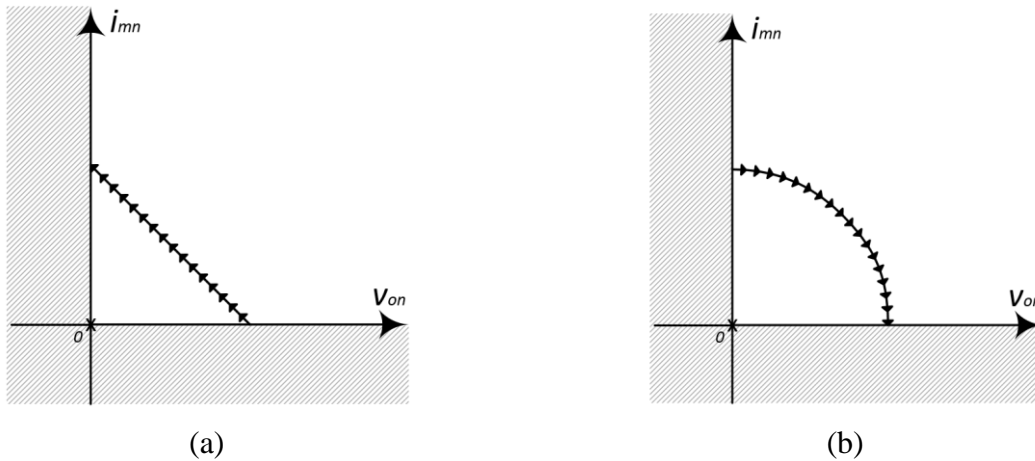
Figure 9: NSS Trajectory Sliding Direction: (a) on-state, (b) off-state

25

If the converter's trajectory was to reach an axis, the converter would then evolve on that axis. Therefore, reaching the i_{mn} axis, the converter would change i_{mn} while the output voltage remained at zero. Likewise, reaching the v_{on} axis, the converter would change v_{on} while keeping the magnetizing current zero. This is due to the unobtainable quadrants.

The interaction between these two trajectories determines how the flyback converter operates and in what mode it operates, whether CCM, BCM, or DCM as discussed in Chapter 2.2 Continuous, Boundary, and Discontinuous Modes of Operation [14]. From this knowledge, a control law to force the converter into BCM, as desired, can be designed. When the two trajectories intersect, the flyback converter switches from the on- to off-state or vice versa. Therefore, this intersection actually determines when the flyback converter's switch, Q, actually switches

There are three possibilities of where the trajectories can intersect, correlating to the three modes of operation. Figure 10 depicts the three choices. Figure 10(a) shows the converter trajectories in CCM. The converter never allows the magnetizing current to reach zero, therefore the converter is operating in CCM. Figure 10(b) allows the magnetizing current to just reach zero before turning on again, which correlates to BCM. Lastly, Figure 10(c) shows DCM operation, allowing the converter to evolve along the v_{on} axis with zero magnetizing current before changing back to the on-state. Figure 10(b) depicts the intended converter operation, since BCM operation is desired.

(a)

(b)

(c)
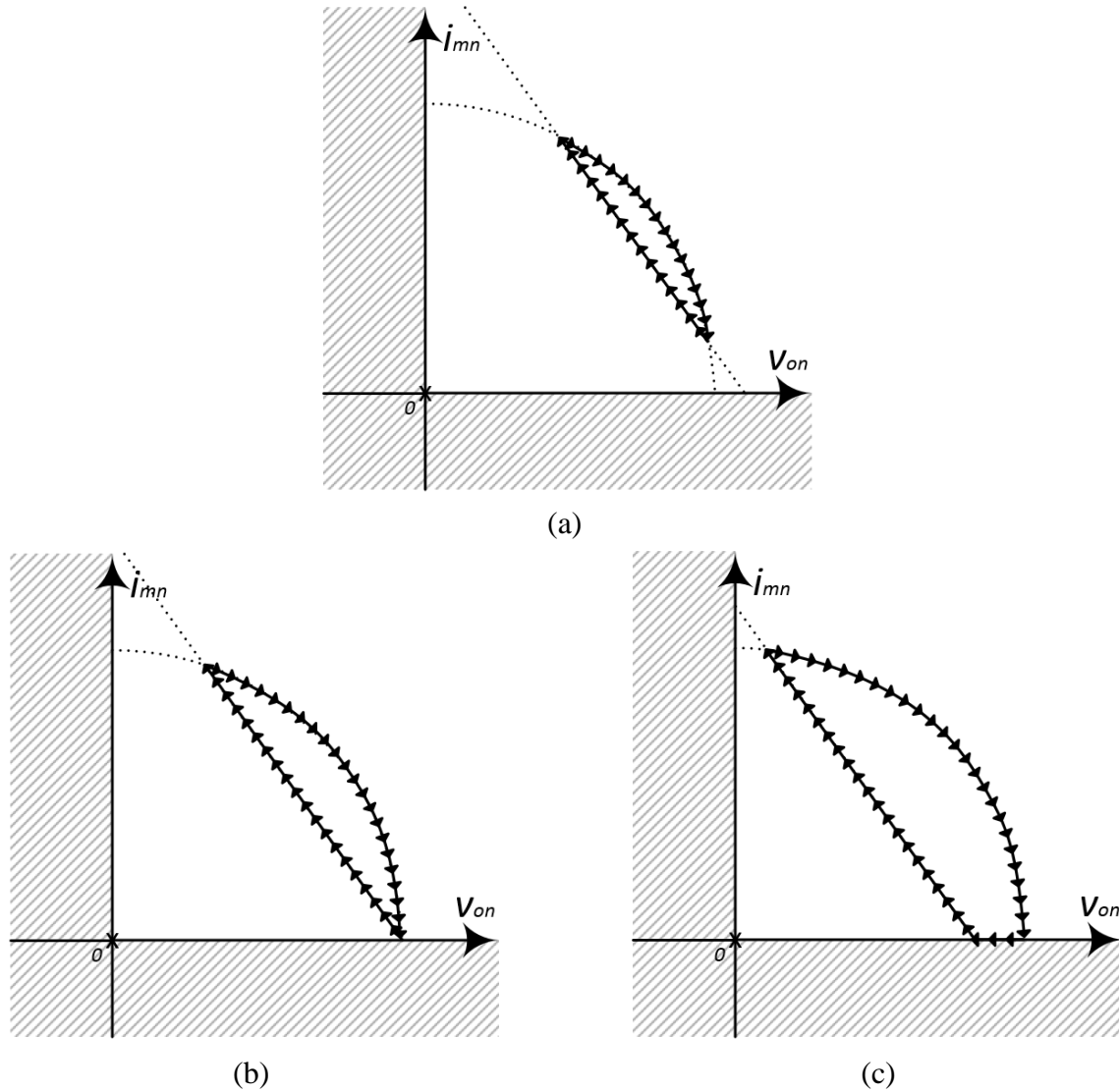
Figure 10: NSS Trajectories and Modes of Operation: (a) CCM, (b) BCM, and (c) DCM

4.2 BCM Trajectories

From the graphical analysis and the above discussion, a control law to keep the flyback converter in BCM operation can be achieved [14]. The goal of this section is to identify a known target operating point and define the trajectories' design parameters and unknowns to include this point. Therefore, a point in the form of (V_r, I_r) must be identified in the v_{on} vs. i_{mn} plane. Figure 10(b) can help with the identification of this point.

From Figure 10(b), we can identify a known point at the intersection of the on- and off-state trajectory on the v_{on} axis. Setting the reference voltage to the desired output voltage

$$V_r = V_o \tag{58}$$

$$v_{on} = \frac{v_o}{V_r} \tag{16}$$

$$v_{on} = \frac{v_o}{V_o} = 1 \tag{59}$$

As previously discussed, BCM is achieved by switching from the off- to on-state just as the magnetizing current reaches zero. Therefore, the desired current at turn-on is

$$i_{mn} = 0$$

A trajectory point is now known as

$$(V_r, I_r) = (1,0) \tag{60}$$

Using this known trajectory point, we can solve for the constant C in the on-state trajectory and the initial conditions of the off-state trajectory. Plugging in (60) into (42), C can be solved for.

$$0 = 0 + 1\frac{V_{inn}}{i_{on}} + C$$

$$C = -\frac{V_{inn}}{i_{on}} \tag{61}$$

Therefore, the complete BCM on-state trajectory is

$$\lambda_{on} = i_{mn} + v_{on}\frac{V_{inn}}{i_{on}} - \frac{V_{inn}}{i_{on}} \tag{62}$$

Moving on to the off-state trajectory, a and b can be simplified with the known trajectory point. Knowing $v_{on} = 1$, (42) can be simplified to

$$\frac{d_{imn}(0)}{dt_n} = -2\pi \tag{63}$$

Substituting (63) into (50), the equation for a can be reduced to

$$a = -1 \tag{64}$$

(51), the equation for *b,* can now also be simplified down to

$$b = -i_{on} \tag{65}$$

Substituting (64) and (65) into (57), the complete BCM off-state trajectory is defined as

$$\lambda_{off} = v_{on}^2 + (i_{mn} - i_{on})^2 - 1 - i_{on}^2 \tag{66}$$

(62) and (66) defined the on- and off-state trajectories for BCM operation [14].

4.3 Steady-State BCM Control Law

The goal of a control law is to force the converter to move to or stay on the identified BCM

trajectories. Knowing the movements along the trajectories for each state of Q and the above

conditions, a control law can be developed. The control law decides between two options: either

Q should be on or Q should be off. The decision is based off the current state of Q and the

relative location of the current operating point to the BCM trajectories.

Figure 11(a) depicts the control law and possible converter trajectories for when Q is on. As

previously discussed, while Q is on, the converter will move up the plane. If the converter is

currently operating below the off-trajectory, Q is kept on while the converter continues to move

up the plane until the off-state trajectory is reached. Once the off-state trajectory is reached, Q is

switched off.   If the converter is operating anywhere above the off-trajectory, then Q should be

turned off [14].

Figure 11(b) shows the control law and possible converter trajectories for when Q is off.

Remembering the desired to operate in BCM, the first part of the law is that Q is not allowed to

(a)   (b)
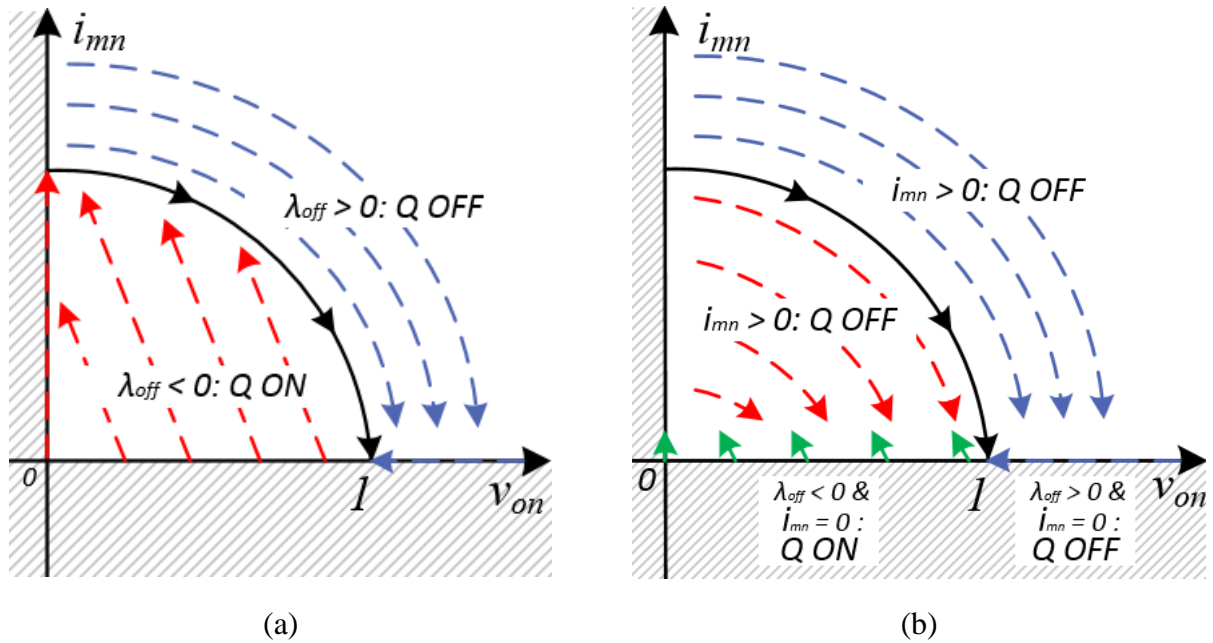
Figure 11: BCM Control Law Trajectories when: (a) Q is ON, (b) Q is OFF [14]

switch back on until $i_{mn} = 0$, once it has been switched off. Therefore, if the converter is

operating anywhere above the v_{on} axis ($i_{mn} > 0$), Q is kept off until the converter reaches the v_{on}

axis. Once the v_{on} axis is reached, the current operating point is compared to the off-state

trajectory. If the converter is operating greater than the off-state trajectory, Q is kept off,

allowing the converter to evolve down the v_{on} axis to the off-state trajectory. If the converter is

operating below or at the off-state trajectory, Q is switched on, allowing the converter to ride the

on-state trajectory back up to the off-state trajectory as previously described [14].
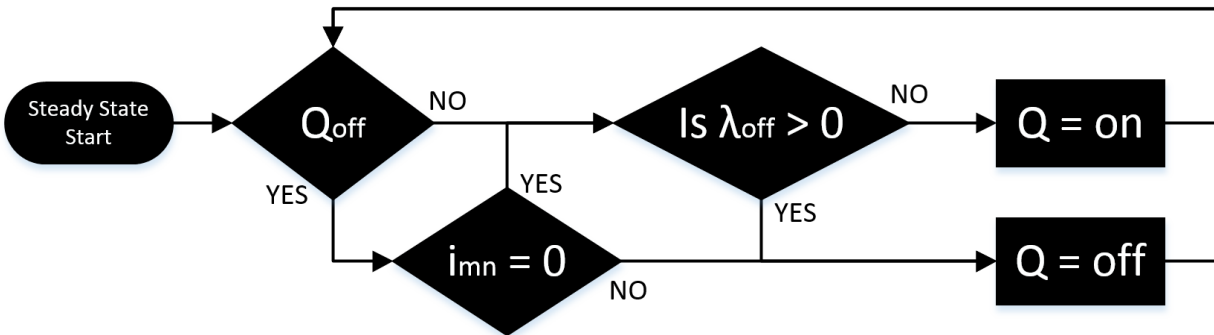
Figure 12: BCM Control Law Flow Diagram

Figure 12 shows a complete flow diagram for the developed BCM control law. The above control law forces the converter to move to and operate on the BCM trajectories, no matter where the converter is currently operating, in one switching cycle. This allows the flyback converter to operate in BCM continuously for any loading condition during steady-state. In a transient situation, where the input voltage or load changes, the worst case scenario would be that the converter recovers in one switching cycle. During that one transient switching cycle, a DCM of operation with a slight over voltage output or a BCM of operation with a slight under voltage output could be experienced. This is because the desired on- and off-state trajectories change with converter parameter changes. Taking only one switching cycle to recover provides remarkable stability and transient response time for all converter conditions.

Another significant benefit of keeping Q off, once switching off, until $i_{mn} = 0$ is that the effect of chattering is eliminated. Chattering is defined as a condition where Q is repeatedly turned on and off in quick succession to keep the actual converter trajectory infinitely close to the desired trajectory. Figure 13 shows a hypothetical chattering situation. This would be avoided with the proposed control law because only two definite switching locations are identified: at the intersection of the on- and off-state trajectory and on the v_{on} axis.
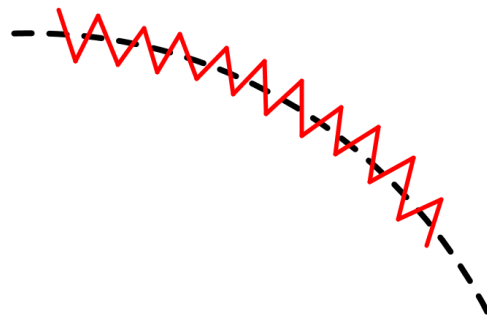
Figure 13: Hypothetical Chattering Situation

Ideal trajectory - Dotted Line, Actual Trajectory - Solid Line

4.4 Steady-State Switching Frequency Derivation

The switching frequency of a converter is very important in considerations for EMI and component selection including microcontroller or processor, semiconductor devices, current sensors, and analog-to-digital (ADC) converters. This section will derive an accurate approximation for the steady-state switching frequency using the proposed control laws. The switching frequency is found to be dependent upon the average input and output voltage, turns ratio of the transformer, and the transformer's magnetizing inductance.

The normalized switching period, T_n, can be described as

$$T_n = t_{on_n} + t_{off_n} \tag{67}$$

where t_{on_n} and t_{off_n} are the normalized values for the on and off time, respectively. t_{on_n} and t_{off_n} can be found by looking at the differential equations for i_{mn} in each state. For the on-state

$$\frac{di_{mn}}{dt_n} = V_{inn} 2\pi \tag{37}$$

$$t_{on_n} = \frac{\Delta i_{mn}}{V_{inn} 2\pi} \tag{68}$$

and for the off-state

$$\frac{di_{mn}}{dt_n} = -v_{on} 2\pi \tag{42}$$

$$t_{off_n} = \frac{\Delta i_{mn}}{V_{on} 2\pi} \tag{69}$$

where dt_n is replaced with the state's time length and di_{mn} is replaced with Δi_{mn}. Note that Δi_{mn} is equal for both on- and off-states. Substituting (68) and (69) into (67)

$$T_n = \frac{\Delta i_{mn}}{V_{inn} 2\pi} + \frac{\Delta i_{mn}}{V_{on} 2\pi}$$

$$T_n = \frac{\Delta i_{mn}}{2\pi} \left(\frac{1}{V_{on}} + \frac{1}{V_{inn}} \right) \tag{70}$$

Knowing that V_{on} is equal to approximately 1 on average, (70) can be simplified down to

$$T_n = \frac{\Delta i_{mn}}{2\pi}\left(1 + \frac{1}{V_{inn}}\right) \tag{71}$$

To convert the normalized period into the converter specific period, (12) can be used.

$$T = \frac{\Delta i_{mn}}{2\pi}\left(1 + \frac{1}{V_{inn}}\right)T_o \tag{72}$$

And therefore the switching frequency is

$$f_{sw} = \frac{2\pi}{\Delta i_{mn}T_o\left(1 + \frac{1}{V_{inn}}\right)} \tag{73}$$

This equation is only helpful if you know Δi_{mn}. Therefore, this will be the next step. As previously discussed, and as will be seen in more detail in the simulations to follow, in steady-state operation, Δi_{mn}'s extremes are at the intersection of the on- and off-state trajectory. One extreme is where $i_{mn} = 0$, which corresponds to $V_{on} = 1$. The other intersection defines Δi_{mn} and here it is found that V_{on} is close, but not equal to 1. To find this intersection and therefore Δi_{mn}, the on- an off-state trajectories will be solved for V_{on} then set equal to each other to eliminate V_{on}. Following that, Δi_{mn} can then be solved for. Starting with the on- and off-state trajectories, setting them equal to 0 since that is the objective of the control law, and substituting i_{mn} as Δi_{mn},

$$0 = v_{on}^2 + (\Delta i_{mn} - i_{on})^2 - 1 - i_{on}^2 \tag{66}$$

$$v_{on} = \sqrt{1 + i_{on}^2 - (\Delta i_{mn} - i_{on})^2}$$

$$v_{on} = \sqrt{1 - \Delta i_{mn}^2 + \Delta i_{mn}2i_{on}} \tag{74}$$

$$0 = \Delta i_{mn} + v_{on}\frac{V_{inn}}{i_{on}} - \frac{V_{inn}}{i_{on}} \tag{62}$$

$$v_{on} = 1 - \Delta i_{mn}\frac{i_{on}}{V_{inn}} \tag{75}$$

33

Equating together (74) and (75) and solving for Δi_{mn}

$$1 - \Delta i_{mn} \frac{i_{on}}{V_{inn}} = \sqrt{1 - \Delta i_{mn}^2 + \Delta i_{mn} 2 i_{on}}$$

$$\Delta i_{mn} = \frac{2 i_{on} \left(1 + \frac{1}{V_{inn}} \right)}{1 + \left(\frac{i_{on}}{V_{inn}} \right)^2} \tag{76}$$

It can be observed that the denominator is nearly 1, therefore it can be neglected.

$$\Delta i_{mn} = 2 i_{on} \left(1 + \frac{1}{V_{inn}} \right) \tag{77}$$

Substituting (77) into (73) and (36) for T_o, the switching frequency dependent upon normalized

values is

$$f_{sw} = \frac{N_p / N_s}{2 i_{on} \sqrt{L_m C_o} \left(1 + \frac{1}{V_{inn}} \right)^2} \tag{78}$$

Using equations (14), (17), (34), and substituting V_r and V_o, the switching frequency can be

described in non-normalized converter values as

$$f_{sw} = \frac{V_o * N_p / N_s}{2\, i_o Z_o \sqrt{L_m C_o} \left(1 + \frac{V_r \frac{N_p}{N_s}}{V_{in}} \right)^2}$$

$$f_{sw} = \frac{V_o * \left(\frac{N_p}{N_s} \right)^2}{2 i_o L_m \left(1 + \frac{V_r N_p}{V_{in} N_s} \right)^2} \tag{79}$$

4.5 Simulations of Steady-State BCM Control Law

The control law proposed above was implemented in MATLAB/Simulink[©]. Figure 14-16**Error!**

Reference source not found. shows the Simulink[©] implementation of the flyback converter and

proposed control law. Figure 14 shows the overall top level hierarchy of the flyback converter implementation. The *step* block is used to model an output load change condition, with initial and final values as variables *Io_1* and *Io_2*, and step time variable as *tstep*. The final and initial values represent the output current (non-normalized). The *clock* outputs the simulation time, which is scaled and stored in MATLAB as the non-normalized time value. The *Normalized Flyback Equations* block implements equations (37)(38) (42)(43), the normalized on- and off-state operating equations, as well as outputs variable data to the MATLAB workspace. This block is detailed in Figure 15. The *Control Law* block implements the proposed BCM control law, described above. The *Control Law* block is detailed in Figure 16. The flyback was simulated at 100W, with device parameters equivalent to chosen devices used in the experimental testing, detailed in Figure 17 and later in the thesis. Figure 18 details the source code used along with the Simulink models to test the proposed BCM control law in steady-state operation.
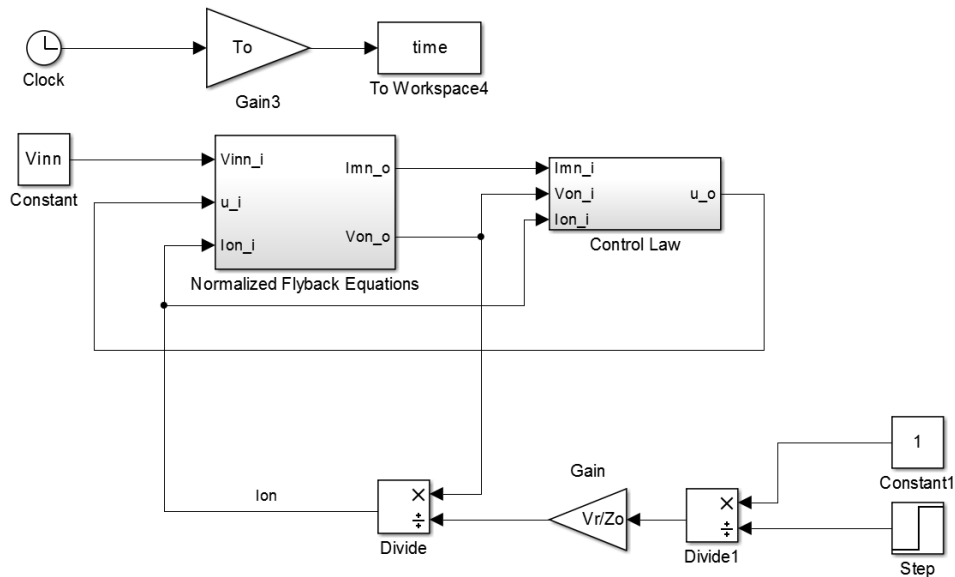
Figure 14: Top Level Hierarchy of Simulink© Flyback Implementation [14]
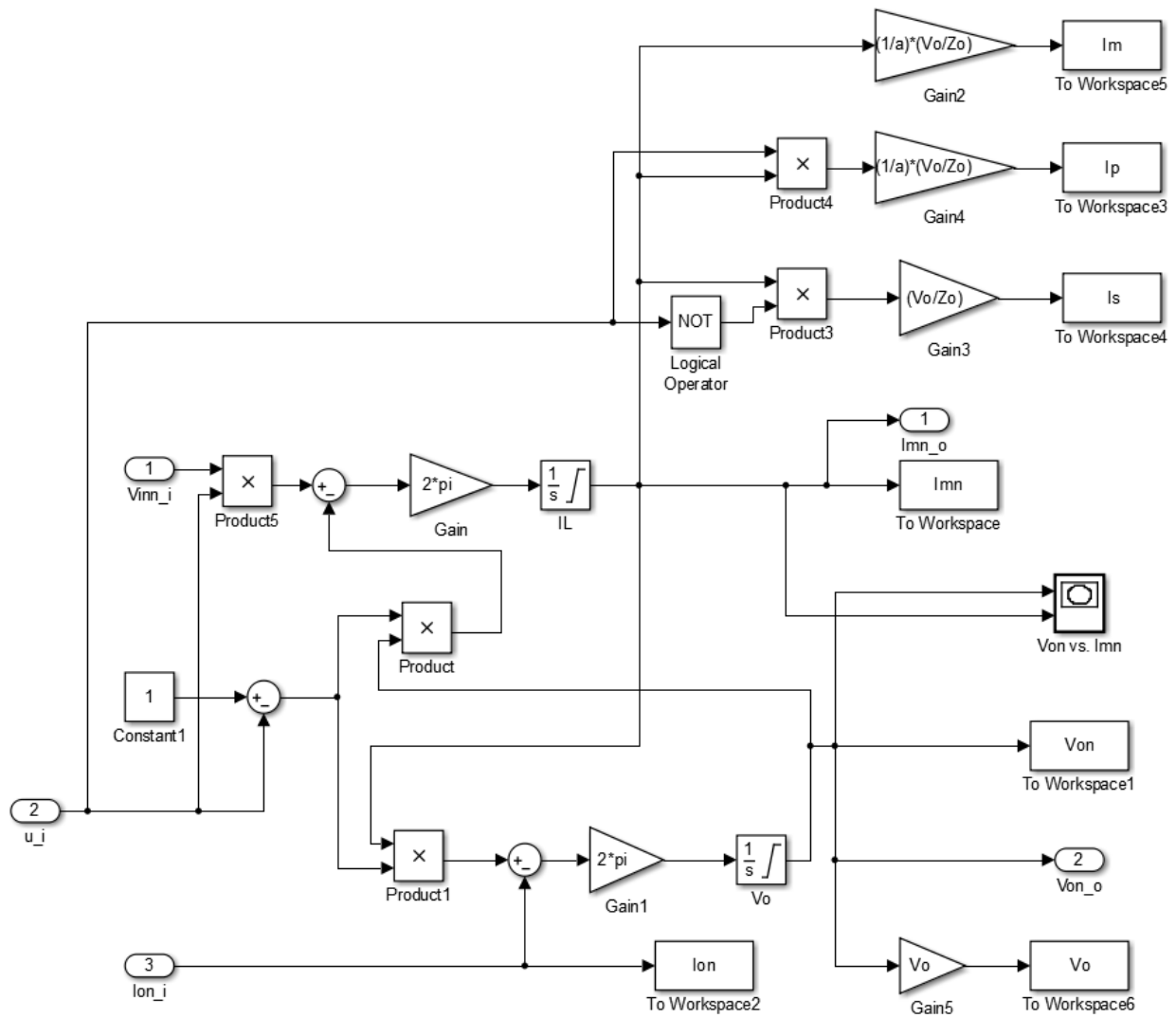
Figure 15: *Normalized Flyback Equations* Simulink© Block [14]
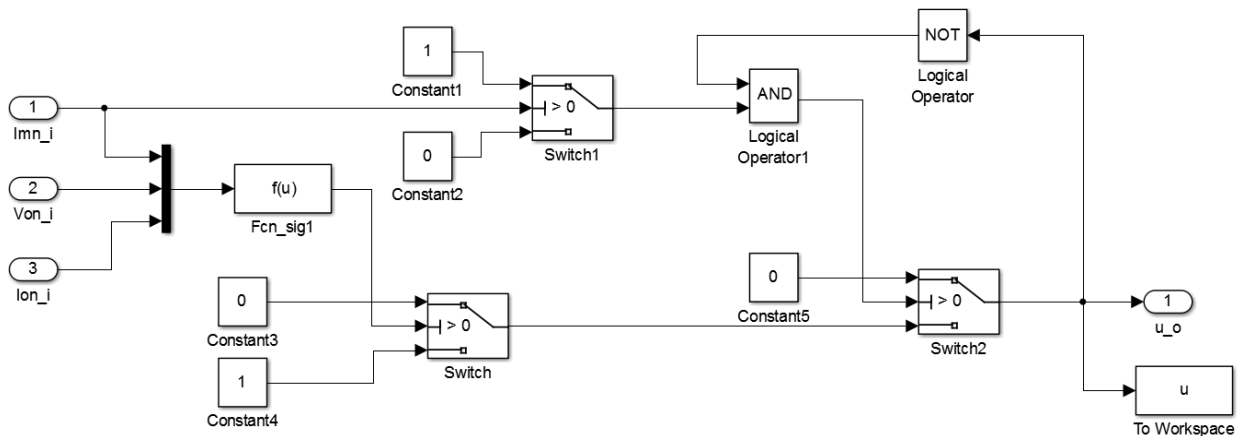
Figure 16: *Control Law* Simulink[(c)] Block [14]

Parameter	Value	Parameter	Value
V_o	200V	C_o	100uF
I_o	0.5A	V_{in}	24V
Power	100W	N_p/N_s	1/6
L_m	28uH		

Figure 17: Experimental and Simulation Device Parameters

MATLAB Source Code:
Steady-State Simulation

```
%% Parameters
Lm=28e-6;    %L for transformer http://www.coilcraft.com/ja4635.cfm
Co=100e-6;   %output capacitance
Vin=24;      %Voltage at MPP for  Kyocera KD205GX-LP
Vo=200;      %output voltage Reference
Io=0.5;      %output current for 100W
a=1/6;       %ratio for transformer http://www.coilcraft.com/ja4635.cfm
Io_1=0.5;    %output current before tstep
Io_2=0.5;    %output current after tstep
tstep = 0.5;%time to step


%% Calculations
To = 2*pi*sqrt(Lm*Co)/a;    %Period
Zo=(1/a)*sqrt(Lm/Co);       %Characteristic Impedance
Vinn=(1/a)*Vin/Vo;          %Normalized Input Voltage
Ion_const=Io/(Vo/Zo)        %Normalized Output Voltage
fsw=(Vo*a^2)/(2*Io*Lm*(1+(Vo*a/Vin))^2) %switching frequency
```

Figure 18: MATLAB Source Code for Steady-State Simulation [14]

Figure 19 shows the simulation results for the on- and off-state trajectories of the steady-state BCM control law implementation for one switching cycle. From this figure, it is notable that the on-state trajectory is a straight line and the off-state trajectory is an arc of a circle (the circle is distorted in the figure due to axis scaling). The converter changes from the off-state to the on-state once the converter reaches $i_{mn} = 0$, meaning the converter is operating in BCM as desired.

Figure 20 shows the steady-state primary and secondary current while Figure 21 shows the steady-state output voltage. The primary and secondary current are clearly operating in BCM; once the secondary current reaches zero, the primary current instantly starts increasing. The output voltage has a ripple less than 0.09V (also shown by Figure 19), which corresponds to less than 0.05%. The average value is equal to 199.97V, which is only a 0.015% error from the desired 200V reference. From equation (79), the switching frequency is approximated to be 34.77kHz for these operating conditions. The switching frequency is measured to be 34.81kHz from the simulations, which is an error of 0.12%.
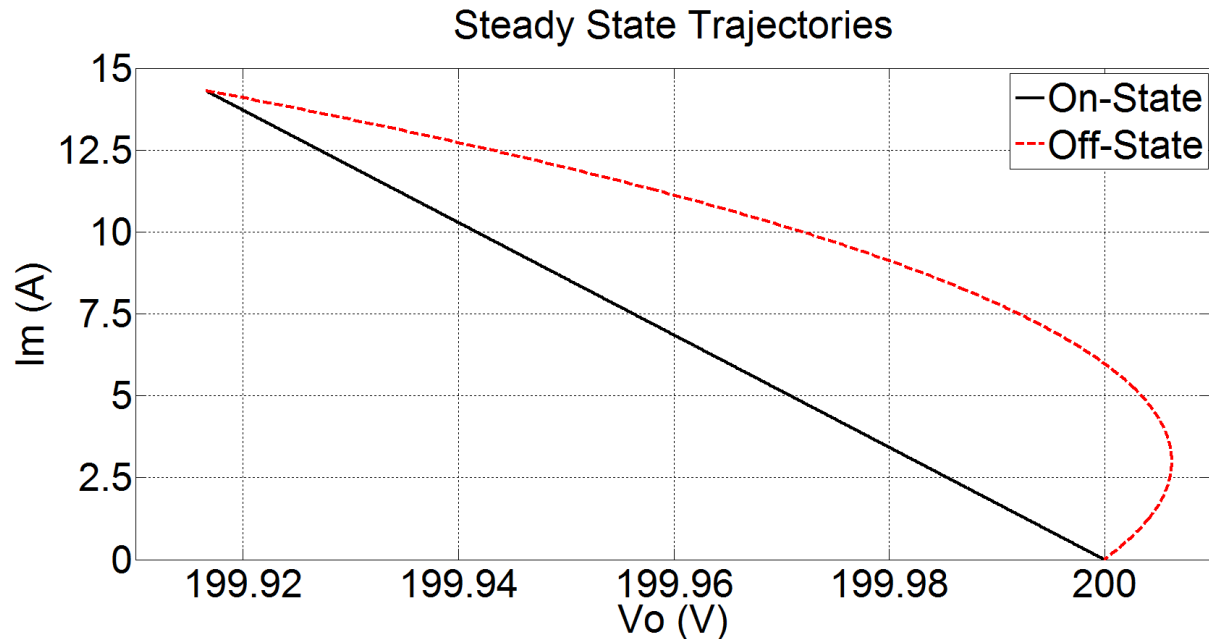
Figure 19: Simulink$^{©}$ Steady-State Simulation of Trajectories
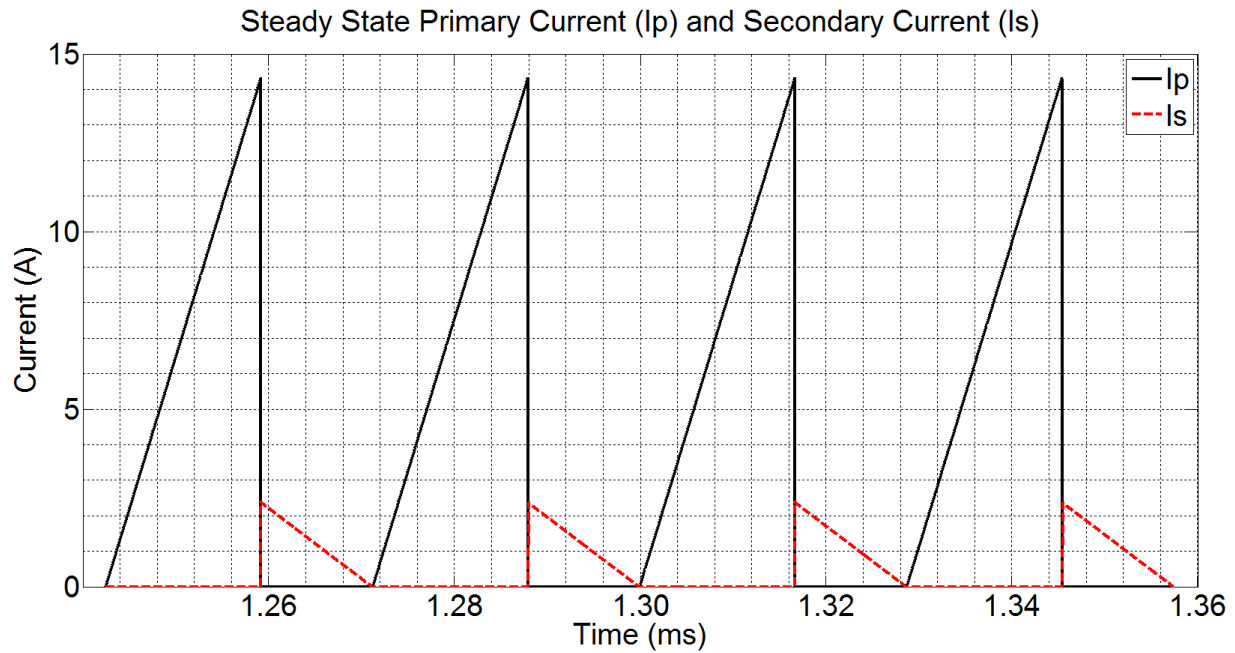
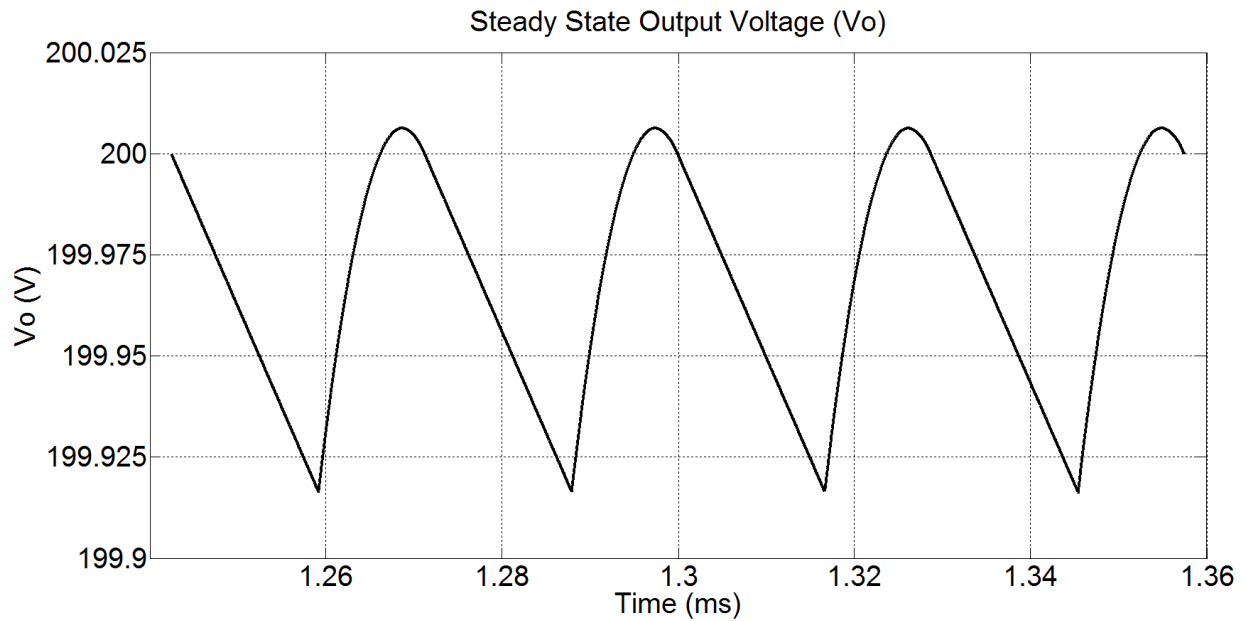Figure 20: Simulink$^{©}$ Steady-State Simulation: I_p and I_s

Figure 21: Simulink$^{©}$ Steady-State Simulation: V_o

4.6 Transient Response of BCM Control Law

A transient response happens when the input voltage or loading condition changes. The transient

lasts for only one switching cycle, assuming the change is completed in one switching cycle, due

to the proposed control law forcing the converter to the NSS. This allows for an extremely fast transient response. Depending on when the voltage or load changes constitutes how the converter will react. The only two options for the converter operation with the proposed control law is to continue in BCM or operate in DCM for one switching cycle.

If the off-trajectory radius is decreased (by a change in output current or input voltage) while the converter is operating past the new radius value, the converter will operate in DCM for one switching cycle. This is due to the fact that to get back to a lower radius trajectory, the converter must evolve down the v_{on} axis. This will result in a slightly larger overshoot of the output voltage compared to steady-state for one switching cycle. If the change occurs while the converter is operating below the new off-trajectory radius, no transient will occur. Figure 22 shows an example of a DCM transient. The key point of this figure is the transient trajectory which evolves down the v_{on} axis. This is not the only situation where a DCM operation could occur, but just one example.

In comparison, if the off-trajectory radius is extended, the converter will still operate in BCM. If the change is during the on-state, no transient will be experienced. If the change is during the off-state however, the converter will undershoot the new trajectory. In the next switching cycle, the converter will recover and operate back on the desired trajectories. This will result in a slightly lower output voltage and higher peak input current compared to steady-state for one switching cycle. Figure 23 shows an example of an undershooting BCM transient. The undershooting transient is observable with the larger peak current.
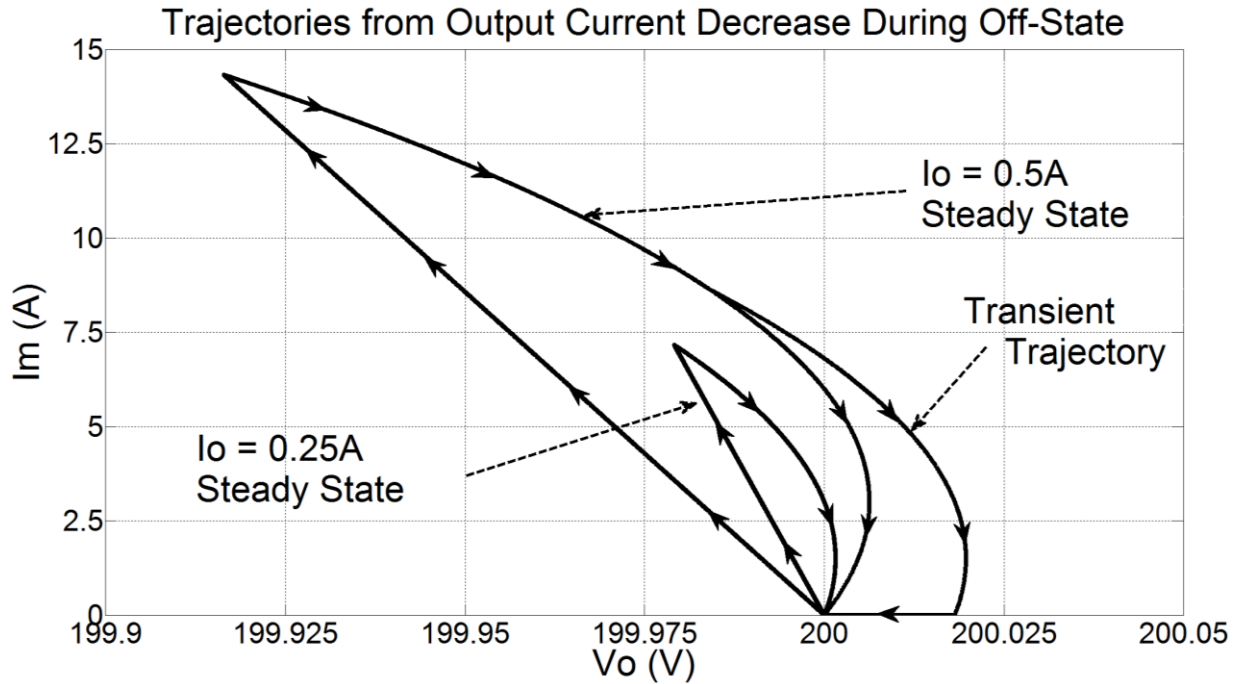
Figure 22: Transient Trajectory: DCM
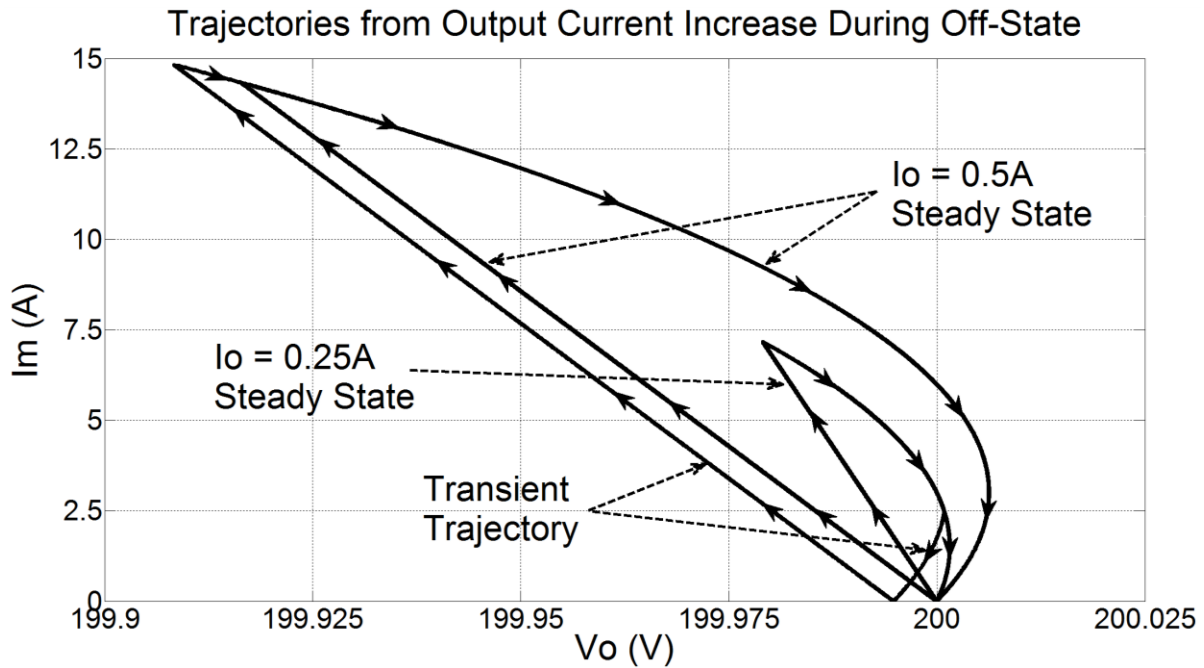
Figure 23: Transient Trajectory: BCM

Analyzing the undershooting BCM transient, a modification of the control law could be potentially be proposed. During the off trajectory, if Q was turned on the instant the off-

trajectory crossed the on-trajectory, the undershooting voltage and increase peak current would be avoided. This would force the converter to operate in CCM, never reaching 0A during the transient. While this is a viable solution to improve the transient, the modification was omitted due to creating potential chattering issues during steady-state and increasing control complexity.

Another note about Figure 22 and Figure 23 is that during steady-state, both loading conditions operated in BCM automatically. This was intended and one of the main points of the proposed control method.

4.7 Start-Up Operation and Max Input Current Protection

Now that the control law's steady-state and transient characteristics have been analyzed, one last unique situation is converter start-up. Using the proposed BCM control law during start up, the flyback converter would experience an extreme input and magnetizing current peak. This is due to the control law bringing the output voltage to the reference value in one switching cycle; this would obviously requires a large amount of energy since the converter is starting with 0V output. The start-up trajectory is shown in Figure 24. Here, the peak input current reaches 375A, which is obviously unacceptable for common devices. The settling time (defined here as the time for the output voltage to be bounded within 5% of its desired value) is only 0.841ms, shown in the output voltage waveform in Figure 25.
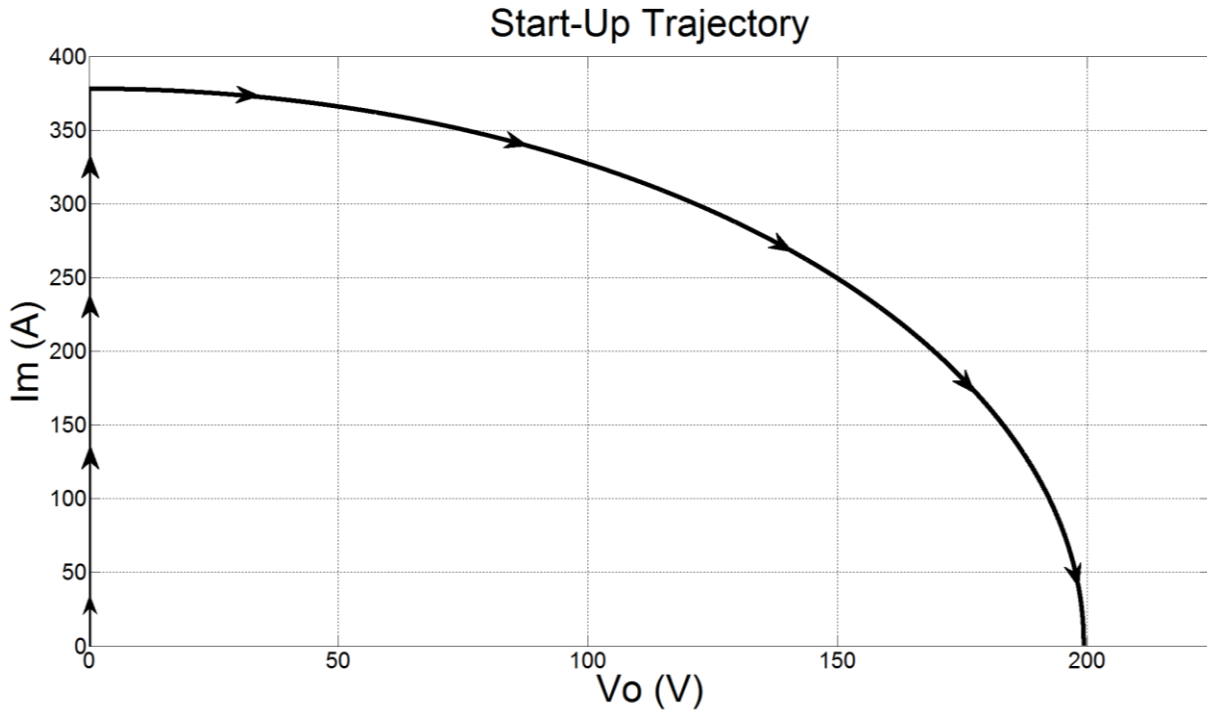
Figure 24: Start-Up Trajectory
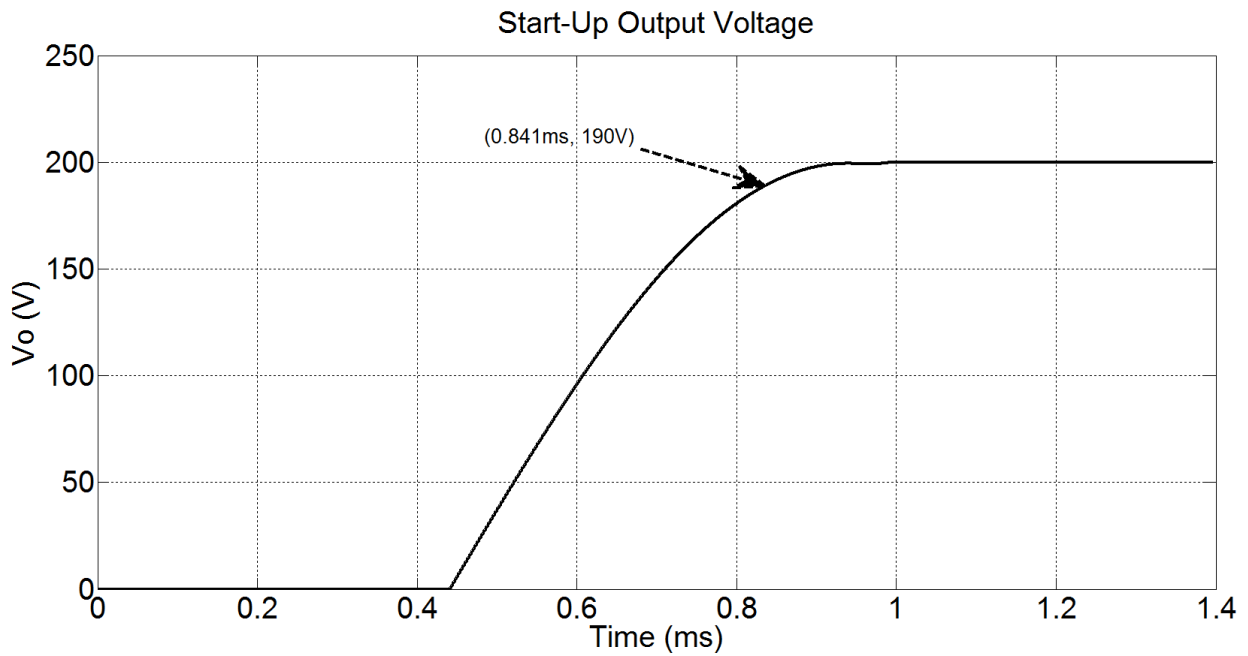
Figure 25: Start-Up Output Voltage

To fix the large start-up input current, a maximum input current level can be set. This is a

desirable addition to the control law because it protects the input devices (such as the

semiconductor switch and transformer) from exceeding the current ratings and damaging the

devices. Therefore, a peak input current value can be selected based off the device ratings. This

value could then be normalized based off (15) if desired.

For this specific controller design, the peak input current was set to a non-normalized value of

20A. Figure 26 shows the updated control law flow diagram with the peak limitation addition.

Figure 27 details the updated Simulink$^©$ control law block. Figure 28 shows the start-up

trajectory with the current maximum implemented. As expected, the current never exceeds 20A.

The converter now takes multiple switching cycles to reach the desired voltage reference. As

described before, the load of the converter is modeled as purely resistive; therefore, the output

current is actually a function of the output voltage. In the start-up situation, the output current is

increasing with the output voltage until the desired voltage reference is reached. Here, the

controller is still operating in BCM during the start-up, forcing the magnetizing current to zero

before turning Q back on. Figure 29 shows the effects of limiting the input current. The

converter's output voltage settling time drastically increased from 0.841ms to 30.1ms, which is

an undesirable effect.

Figure 26: BCM Control Law Flow Diagram with Input Current Limit, BCM Start-Up

Figure 27: *Control Law* Simulink© Block with Input Current Limit, BCM Start-Up

Figure 28: Start-Up Trajectory with Input Current Limit, BCM Start-Up
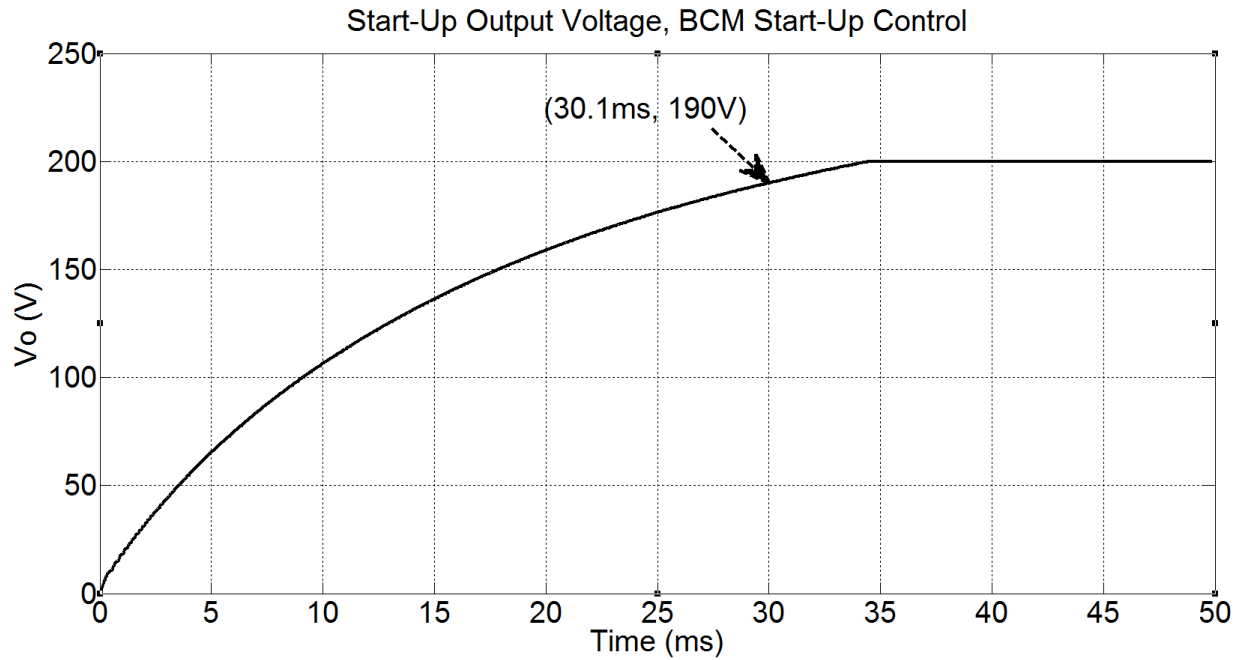
Figure 29: Start-Up Output Voltage with Input Current Limit, BCM Start-Up

To decrease the settling time, the start-up control was modified to operate in CCM, with a set Δi_{mn}, instead of operating in BCM. This allowed for a larger amount of energy to transfer faster, while still limiting the peak current. i_{mn} oscillated between the defined peak, $i_{mn_{pk}}$ and $i_{mn_{pk}} - \Delta i_{mn}$. This control was chosen to be implemented any time the converter is operating below the settling range (5% of V_r, which in this converter 190V). The transition location between the CCM and BCM control method was selected arbitrarily and could be changed for each application, depending on the expect peak current and settling times. The longer the CCM control method operates during start up (the closer the transition is to steady-state operation), the faster the settling time will be. A potential issue though is getting the transition too close to steady-state and causing a chattering situation in the converter where the control law is switching

from BCM to CCM operation from a small transient. Therefore, the 5% of V_r boundary was

selected.

For this converter design, $\Delta i_{mn} = 5A$. Again, this was an arbitrary selection. The smaller

the Δi_{mn}, the faster the settling time will be. The negative effects of a smaller Δi_{mn} is a higher

switching frequency, which could affect EMI, increase start-up losses, and cause higher average

power dissipation through the devices. 5A seemed to be an acceptable trade off in this

application based off the selected components and operating current.

Figure 30 shows the updated flow diagram for the CCM start-up method. Figure 31 shows the

updated *Control Law* block for the CCM start-up. Figure 32 and Figure 33 show the start-up

trajectory with the CCM start-up control. Figure 32 shows the first few switching cycles of start-

up. It is clear that the converter is now operating in CCM with a Δi_{mn} of 5A and peak of 20A.

Figure 33 highlights the transition from CCM to BCM at 190V (5% of V_r). From there, BCM

control continues to and during steady-state. The benefit of this modified control is shown in

Figure 34. The settling time decreased to 13.5ms, a 55.1% reduction compared to the BCM
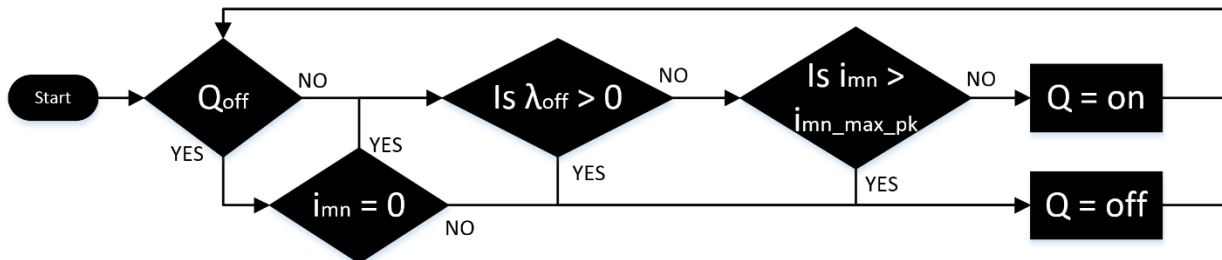
start-up of Figure 29.
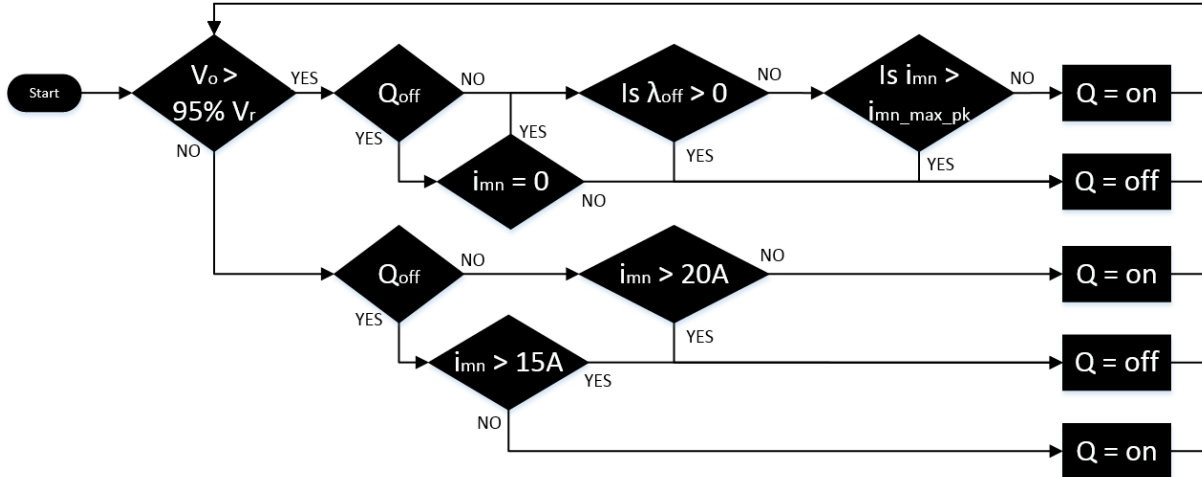
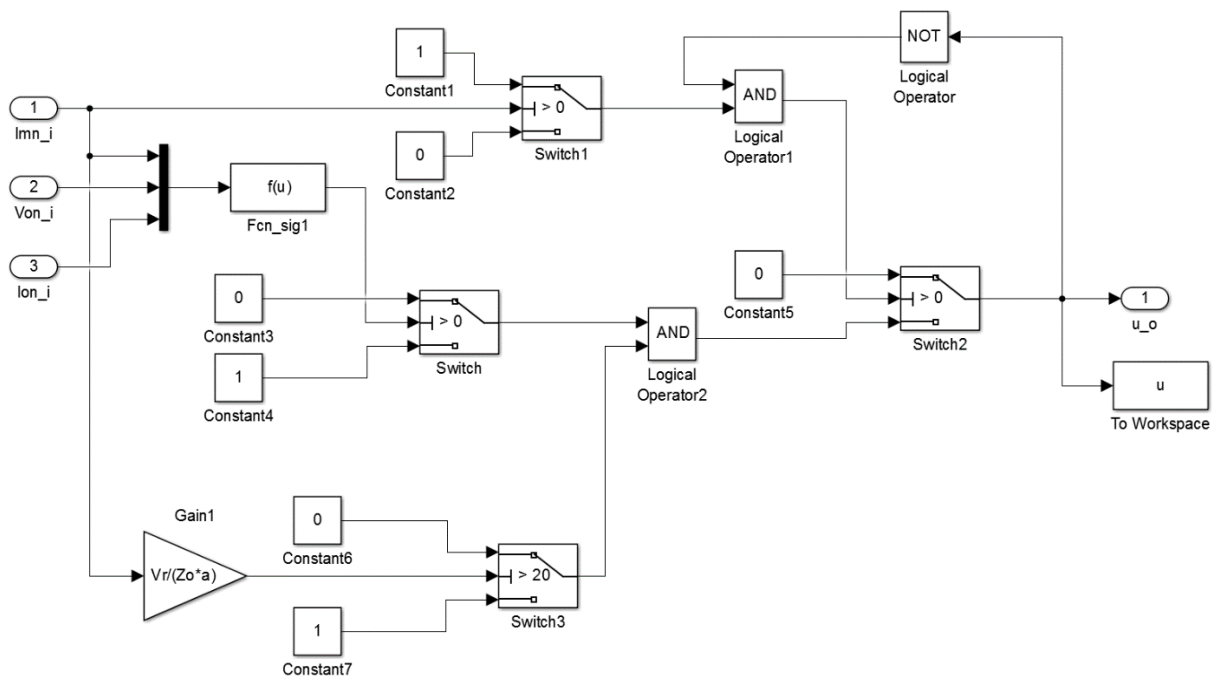Figure 30:BCM Control Law Flow Diagram with Input Current Limit, CCM Start-Up
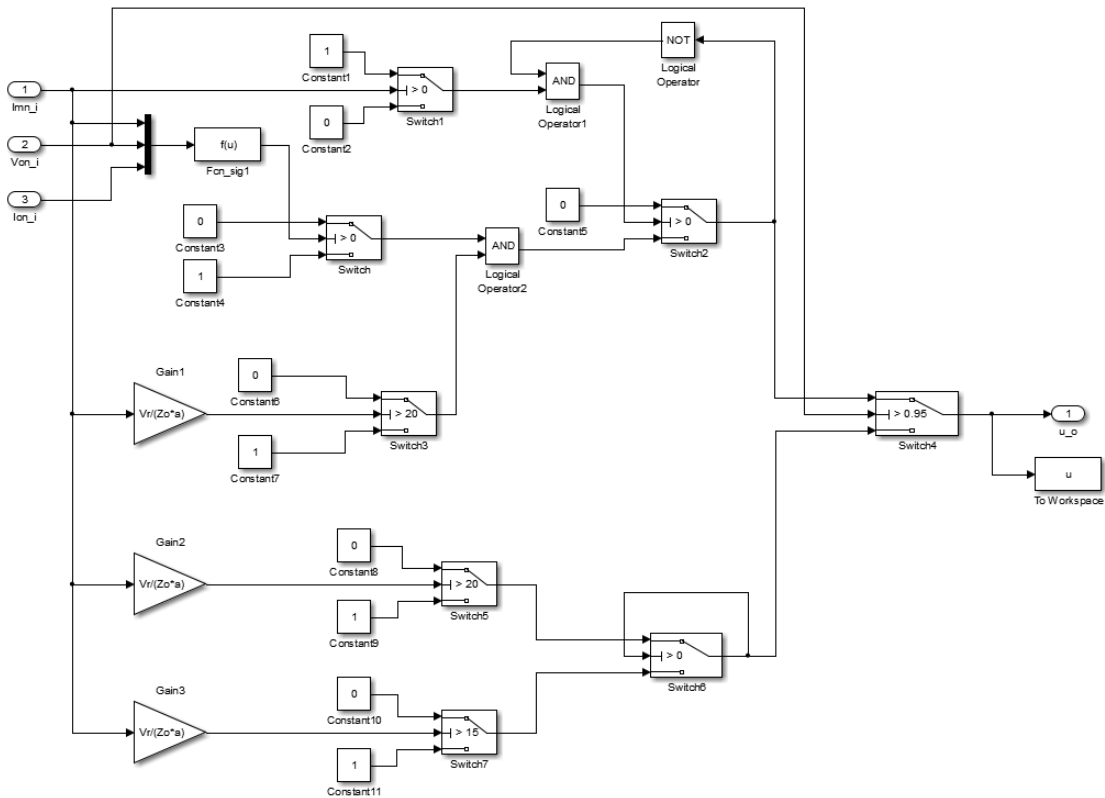
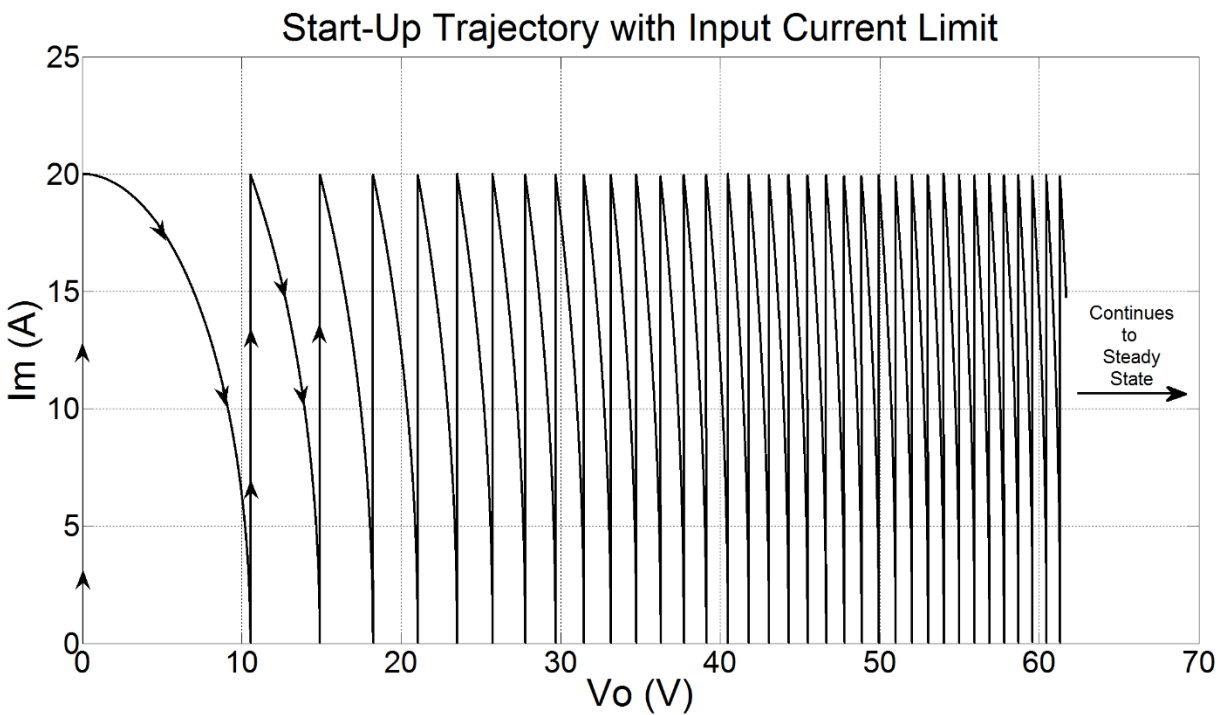Figure 31: Control Law Simulink© Block with Input Current Limit, CCM Start-Up
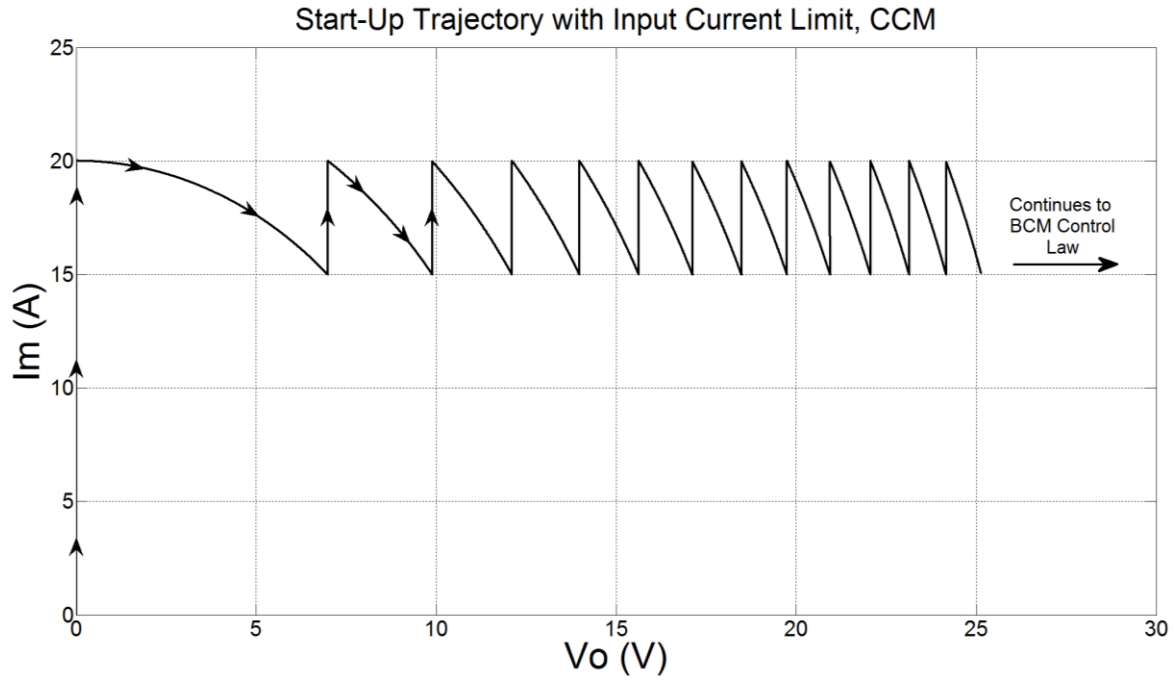
Figure 32: Start-Up Trajectory with Input Current Limit, CCM Start-Up
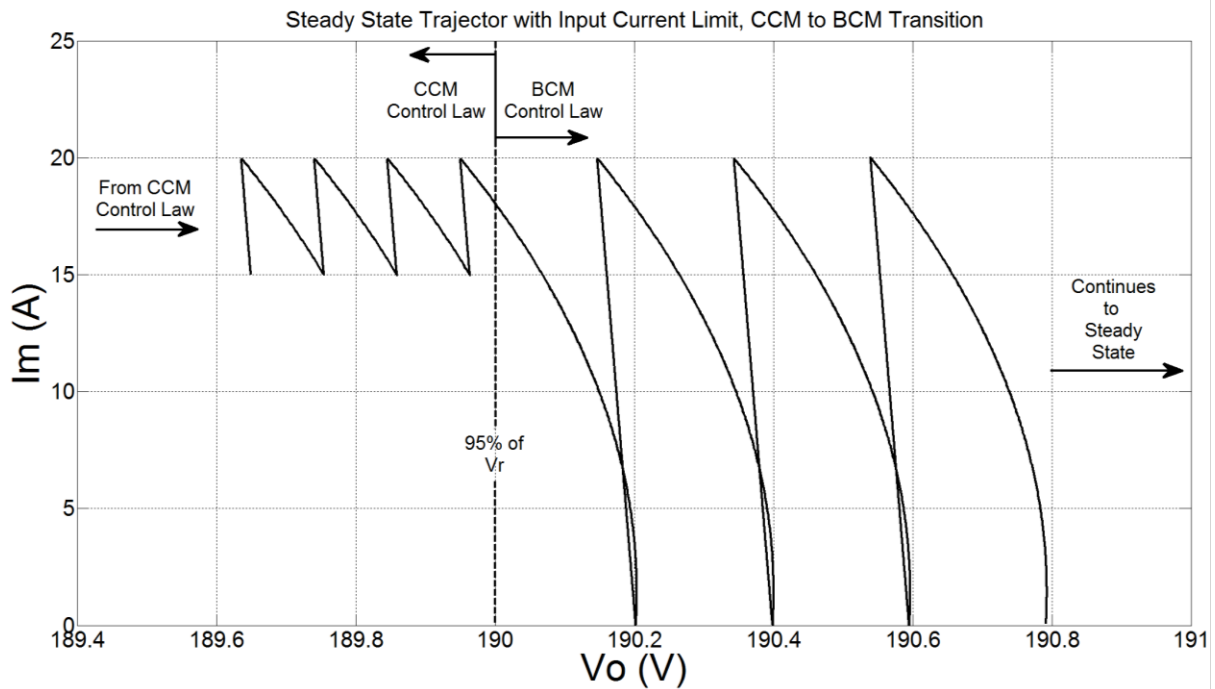
Figure 33: Start-Up Trajectory with Input Current Limit, CCM to BCM Transition
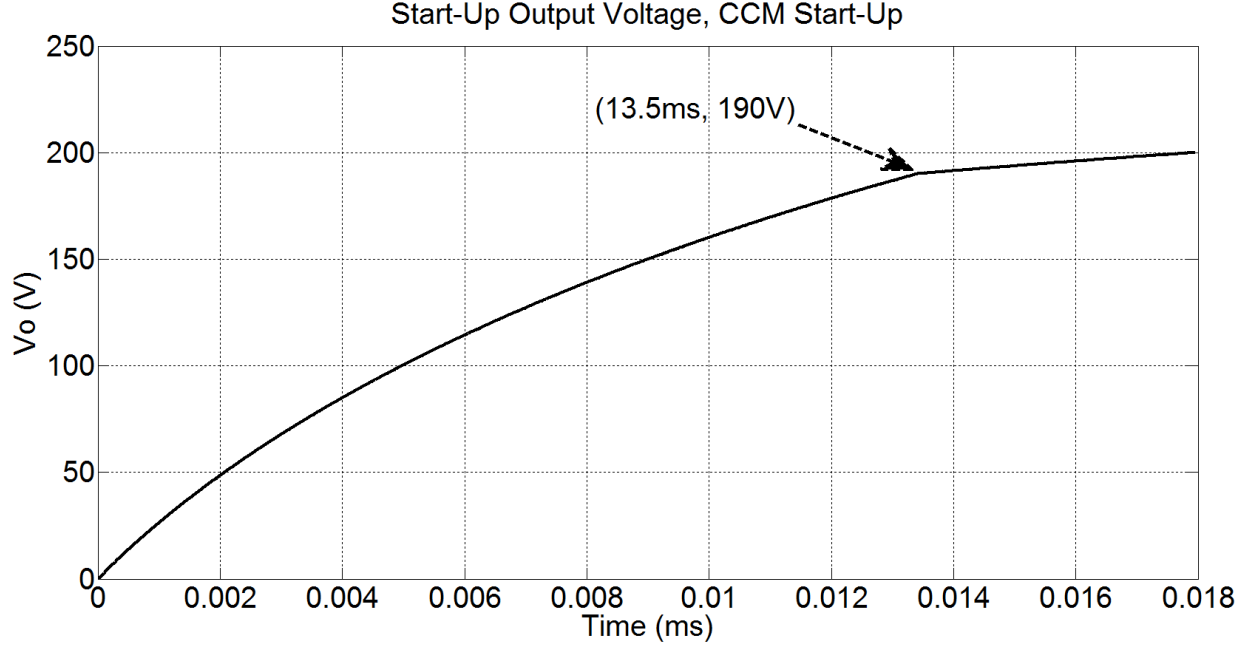
Figure 34: Start-Up Output Voltage with Input Current Limit, CCM Start-Up

4.8 Review of Proposed Control

This section has presented the proposed control law for operating the flyback converter in BCM control under any loading condition. The on-state trajectory was derived as

$$\lambda_{on} = i_{mn} + v_{on}\frac{V_{inn}}{i_{on}} - \frac{V_{inn}}{i_{on}} \tag{62}$$

while the off-state trajectory was derived as

$$\lambda_{off} = v_{on}^2 + (i_{mn} - i_{on})^2 - 1 - i_{on}^2 \tag{66}$$

With the known trajectories, the switching frequency was derived as

$$f_{sw} = \frac{V_o * \left(\frac{N_p}{N_s}\right)^2}{2i_oL_m\left(1 + \frac{V_rN_p}{V_{in}N_s}\right)^2} \tag{80}$$

The proposed law allowed for swift response to transients in just one switching cycle. This control was analyzed and modeled in Simulink[©]/MATLAB. In addition to steady-state and transient response, start-up was also analyzed. It was determined that the best method for

managing start-up input current peaks and settling time was to operate with a maximum input current limit as well as operating in CCM during start-up. Figure 30 shows the complete final flow diagram for the proposed control.

V. Hardware Design and Component Selection

5.1 Overview and Hardware Design Considerations

While the flyback itself presents a minimal component converter topology, combining all the required parts for control, power, and signal compensation can tally up quite quickly. This chapter will step through each major section of the hardware implementation and selection for an intended 100W flyback converter, implementing the NSS control detailed in Chapter 4. Realistically, the tested flyback converter was only capable of 90W due to saturating the transformer.

Implementation of the control law was performed in a Digital Signature Processor (DSP). The necessary feedback signal variables to implement the NSS control included the output voltage, primary current, secondary current, and output current. The input voltage was not required for the designed NSS control, but is a variable in the NSS trajectories. Therefore, feedback network to acquire the input voltage was include incase this signal was required in future research. The feedback signals were acquired through analog-to-digital conversion (ADC) in the DSP. To calculate the magnetizing current variable, the primary and secondary currents of the transformer were summed together. This is possible due to the flyback's current operation. Ideally, the magnetizing current is equal to the primary current when Q is on and equal to the secondary current times the turns ratio when Q is off.

This chapter is broken into detailed sections covering each hardware section: basic flyback components and snubbers, MOSFET and gate driver, power supplies, input voltage feedback,

output voltage feedback, and primary, secondary, and output current feedback. Appendix A details the complete schematic of the flyback converter.

5.2 Basic Flyback Components and Snubbers

Figure 54 found in Appendix A details the main hierarchical overview of the flyback converter. Detailed are the basic flyback components and snubbers as well as the connections for each hierarchical block of individual systems. The details of the hierarchical blocks are discussed in later sections of this chapter. Major components selected at this level include the transformer and associated snubber as well as the output diode and associated snubber.

The transformer selected was Coilcraft's JA4635-AL. This transformer was a readily available, off-the-shelf flyback transformer. In addition, SSEES already had this transformer on-hand and therefore was an added incentive to cut-down on development costs. The transformer has a turns ratio of 1 to 6 and minimal winding resistance and leakage inductance. Utilizing [18] as well as experimental testing, a resistor-capacitor-diode (RCD) snubber was employed in parallel to the primary of the transformer to cap the voltage spikes associated with the leakage inductance of the transformer that were generated at the turn-off of Q.

The output diode was selected based on reverse voltage ratings, on-resistance, reverse recovery time, and junction capacitance. The worst-case reverse voltage was during the on time of Q where the output diode experienced the output voltage (200V) plus the input voltage (35V max) reflected by the turns ratio. Therefore, the max reverse voltage would be around 410V during steady-state. The faster the recovery time and the lower the junction capacitance, the better

switching performance and lower ringing is experienced. With all this in mind, C3D06060A

manufactured by Cree Inc. was selected. This device is rated for 600V reverse voltage, has no

reverse recovery time, being Silicon-Carbide (SiC), and less than 30pF of capacitance at the

expected steady-state reverse voltage [19]. During experimental testing, large ringing was

generated by the switching of the output diode. To minimize this effect, a resistor-capacitor

(RC) snubber was employed in parallel with the diode. [20] was used to assist in the resistor and

capacitor value selection.

5.3 MOSFET and Gate Driver

Figure 57 in Appendix A details the MOSFET and gate-driver configuration. A Si MOSFET

was implemented for the semiconductor switch Q. This technology selection was based on cost

and ease of use, in comparison to JFETS, SiC MOSFETs, Gallium-Nitride MOSFETs or other

semiconductor transistors. Important characteristics for the MOSFET were the V_{ds} ratings,

current ratings (sustained and peak), on-resistance, and turn-on/off times. The max V_{ds},

neglecting any transients, would be experienced during the off-time when the output voltage is

reflect by the transformer to the primary (33V) in series with the input voltage (35V max).

Therefore, the V_{ds} rating must exceed 68V plus headroom for any transient or spike voltages.

The expected average current in steady-state with the implemented NSS control is approximately

7A, with a peak of approximately 15A, neglecting start up. The IRFP250MPBF manufactured

by International Rectifier was selected exceeding all the desired criteria.

A gate-driver was used to ensure adequate turn-on time to minimize switching losses and heating

of the MOSFET as well as provide an adequate V_{gs} based off an input signal from the DSP.

UCC27531DBVR from Texas Instruments (TI) was selected. This gate-driver is able to supply a max of 2.5A, guaranteeing a fast turn-on time with our selected MOSFET. The chip's voltage supply is the voltage level that is output to the MOSFET's gate. Therefore, proper selection of the power supply allowed a sufficient V_{gs} for the MOSFET. The input signal high level threshold is only 2.2V max. Our selected DSP, which is only capable of outputting 3.3V on its input/output (I/O) pins, was capable of triggering the gate-signal. A 100kΩ resistor was placed from the input signal pin to ground to prevent the gate signal from floating and eliminating the possibility of false activations. In addition, a 10Ω resistor was placed in series between the gate-driver's output and the MOSFET's gate to limit the inrush current and turn-on time to assist in switch ringing. A RC snubber was placed from drain to source of the MOSFET to help eliminate associated switching ringing. [20] and experimental testing help define the snubber component values.

5.4 Input Voltage Feedback

Figure 56 in Appendix A contains the schematic of the input voltage feedback. A basic voltage divider generated a 2.5V signal at a 35V input, the max input signal, which was fed into the non-inverting pin of an op-amp. An ADA4851 op-amp from TI was designed in a basic buffer configuration with a 3.3V zener on the output to protect the DSP from over voltage. The buffer, detailed in Figure 35, was necessary to minimize the error introduced to the voltage divider ratio once a connection was made to the divider. The ADA4851 op-amp selection is detailed in Section 5.6.
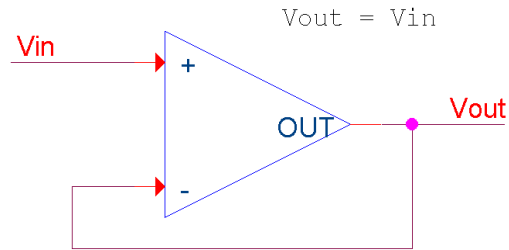
Figure 35: Buffer Op-Amp Configuration

5.5 Output Voltage Feedback

Since the output of the flyback is isolated, an isolated voltage sensor had to be implemented to acquire the output voltage feedback, as shown in Figure 55 in Appendix A. The ACPL-C87B from Allego was selected as the isolated voltage sensor. An input voltage signal was generated by a resistive voltage divider on the output voltage. At 205V output, the voltage divider was designed to be 2.0V. This ACPL-C87B had a gain of one and output the signal on two pins: the difference in voltage between the two outputs represented the input signal magnitude. Therefore, an ADA4851 op-amp configured in a differential (subtractor) configuration with a gain of one, detailed in Figure 36, was designed. The output of the op-amp had a basic RC low-pass filter set for a cut-off frequency of 70Hz and a 3.3V zener diode to protect the DSP from overvoltage. A downfall of the isolated voltage sensor was the requirement of an isolated power supply.
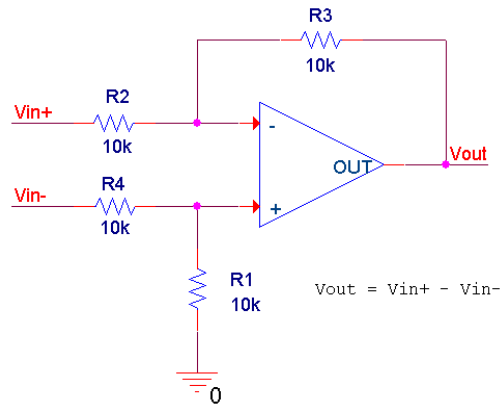
Figure 36: Differential (Subtractor) Op-Amp Configuration with Gain = 1

5.6 Primary, Secondary, and Output Current Feedback

The primary, secondary, and output current feedback signals were all designed in the same way, with a difference in gain. These schematics are detailed in Figure 58-59 of Appendix A. The current sensors used were the LTSR 15 for the primary current and the LTSR 6 for the secondary and output current, both manufactured by LEM. These sensors were isolated hall-effect, closed loop current sensors, containing all necessary sensing elements and amplification internally. In addition, these sensors can adequately measure current up to 100kHz with no phase shift, which is a necessity. The only difference between the LTSR 15 and 6 is the current rating and gain. The primary current required the LTSR 15 due to the higher average current rating experienced compared to the secondary or output current. At zero amps, the output of the current sensors were 2.5V. This value, plus the signal value during operation, would exceed the ADC voltage limits. Therefore a DC level shifter stage followed by a gain stage was designed. The ADA4851 was selected due to a wide input voltage range, rail-to-rail output, and zero output phase shift up to 10Mhz. The current will experience an "infinite frequency" step response during switching, therefore the frequency response played a big effect in op-amp selection.

57
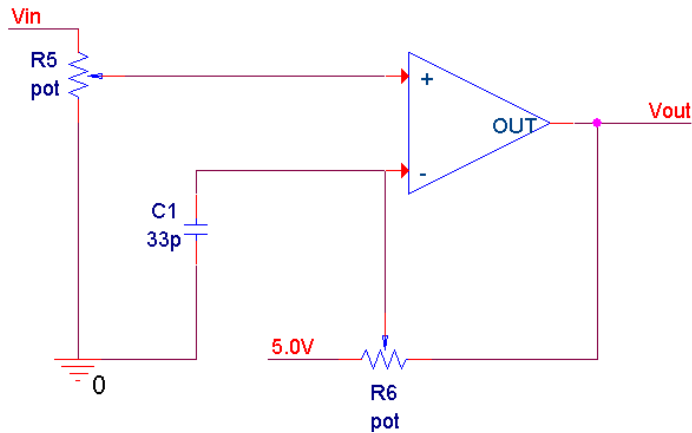
Figure 37: DC Level Shifter Op-amp Configuration

The output of the current sensor was first filtered by a low-pass RC filter set at a cut-off

frequency of approximately 1MHz before the DC level shifting op-amp . A potentiometer

created a voltage divider on the non-inverting pin of the op amp. On the inverting pin, another

potentiometer voltage divider fed off the 5.0V supply was tuned to match the non-inverting DC

value to create a 0V op-amp output at 0A.   The DC level shifter op-amp configuration is

detailed in Figure 37. The output was again filtered by a low-pass RC filter set at a cut-off

frequency of approximately 100kHz.

The gain stage was implemented as a basic non-inverting op-amp configuration, detailed in

Figure 38. A potentiometer controlled the gain and was set for maximum resolution during

experimental testing. The output of the op amp was again filtered by a RC low-pass filter and

had a 3.3V zener diode to protect the DSP from over voltage.
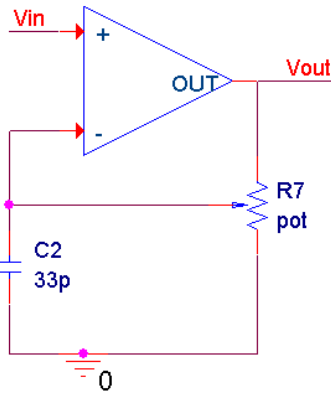
Figure 38: Non-Inverting Op-amp Configuration

5.7 Power Supplies

The power supplies were selected based off the input voltage range, current rating, and output voltage. Three different output voltage levels and power supplies were needed: non-isolated 5.0V supply for op-amps and current sensors, non-isolated 12.0V supply for the MOSFET gate-driver, and an isolated 5.0V supply for the isolated output voltage sensor. This design is detailed in Figure 60 in Appendix A.

Unintentionally, the isolated power supply's output voltage implemented varied greatly based off of output current drawn, inherent in the design of the supply. With minimal to no load, the output voltage could be as much as 6.0V which would damage or destroy the isolated voltage sensor. Therefore, a dummy load of 150Ω was added to ensure the output voltage was within our voltage sensor's supply range. While this worked for the design, it is recommended in future revisions that a non-load dependent power supply be selected.

5.8 Digital Signal Processor

The DSP selected was TI's TMS320F28335. The DSP was housed off board, using TI'S

development programmer and ControlCARD.   A major influence in the selection of the

TMS320F28335 was the fact that the SSEES lab already had the development interface and

ControlCARDs available, which significantly cut down on development costs. Nevertheless, the

DSP had the capabilities of implementing the NSS control. The TMS320F28335 is capable of

running at 150MHz, executing multiplication in a signal clock cycle, and contains 16 ADC

channels running at 25MHz.

5.9 Photo of Developed Board

Figure 39-40 show the completed flyback converter board. Figure 41 show the completed

flyback converter connected to the DSP ControlCARD. This was the implementation used for

experimental testing. The PCB was fabricated on a on-site milling machine using basic, 1oz.
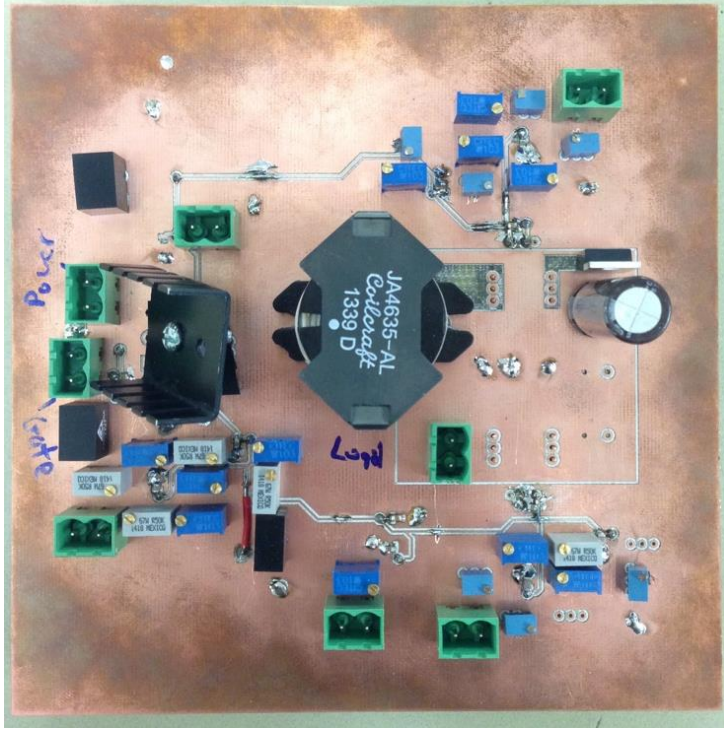
copper.

Figure 39: Top Side of Developed Flyback Converter
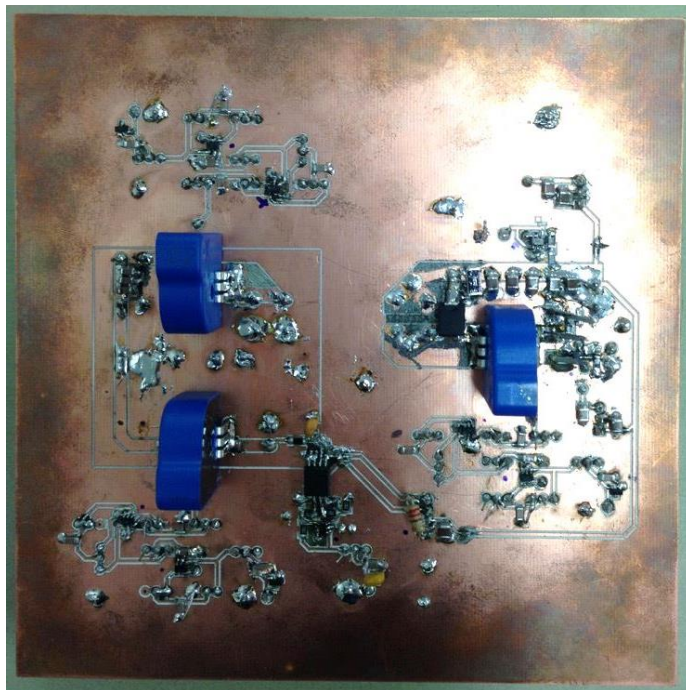
Figure 40: Bottom Side of Developed Flyback Converter
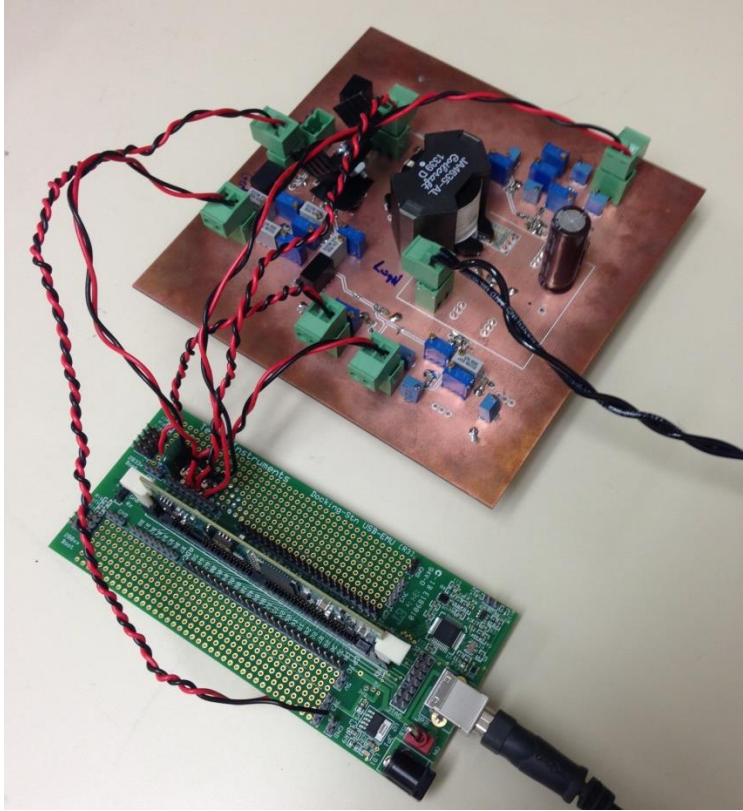
Figure 41: Flyback Converter with Connections to DSP

VI. DSP Software Design

6.1 Overview of Code Development

As discussed in Chapter 5, the selected DSP was TI's TMS320F28335 development

ControlCARD and programmer. All code was developed in the C programming language in TI's

Code Composer Studio IDE, V6.0.1. All information regarding specific peripheral operations

and registers for the TMS320F28335 came from TI's datasheets for the TMS320F28335 found at

TI's website. This chapter serves to detail the code developed to utilize the DSP in

implementation of the NSS Control derived in Chapter 4. The system inputs to the DSP are the

four needed system variables through ADC channels: primary current, secondary current, output

current, and output voltage. The output of the DSP is the gate-signal, fed to the gate-driver of

the flyback. Only two global variables were used to pass information between functions: the

current switch state Q, and a NEW_DATA flag, used to prevent calculation during noisy

switching instances.

Before the control code could be completely developed, the sensors must be calibrated and gain

equations calculated. Calibration was performed by feeding the flyback converter a known gate

signal from a function generator and adjusting the potentiometers to set gains and cut-off

frequencies while recording data to calculate the needed equations. This is detailed in Section

7.1, but the acquired gain equations will already be used and implemented in code in this

chapter.

6.2 Oscillator, Interrupt, and GPIO Setup

Figure 42 details the code to initialize the DSP's oscillator. The 'OscillatorSetup' function was the first task performed in the main program. The DSP was run at the maximum frequency, 150MHz, so that the fastest processing capabilities were achieved. As a protection, TI requires a "password" to allow the modification of operation sensitive registers. To gain access to locked register(s), 'EALLOW' must be stated before the register(s) can be modified. Which registers are 'EALLOW' protected is detailed in the datasheets. To re-lock the registers after modification, 'EDIS' must be passed.

Interrupts were used for Timer0 and ADC conversion when debugging. For the interrupts to function, the individual interrupt mask had to be cleared and global interrupts had to be enabled. In addition, the actual interrupt service routine (ISR) function vector had to be linked to its corresponding interrupt register. The interrupt configuration is detailed in Figure 43.

All unused general purpose input/output (GPIO) pins are recommended to be set to outputs and set low. Figure 44 shows the basic function to perform this task.

DSP Oscillator Configuration

```
//Disable WatchDog Timer, set SYSCLOCK to 150MHz
void OscillatorSetup()
{
    EALLOW;                             //Register is EALLOW protected
    SysCtrlRegs.PLLCR.bit.DIV = 10;     //OSCCLK * 10 = 30Mhz*10 = 300MHz
                                        //from PLL
    SysCtrlRegs.PLLSTS.bit.DIVSEL = 2;  //PLL/2 = 300Mhz/2 => CLKIN =
                                        //SYSCLKOUT = 150MHz
    SysCtrlRegs.WDCR = 0x0068;          //Disable watchdog timer
    EDIS;                               //Ends EALLOW
}
```

Figure 42: DSP Oscillator Configuration

DSP Interrupt Configuration

```
void InterruptSetup()
{
    DINT;                               //Disable global Interrupts
    EALLOW;                             //Pie Vector Table is EALLOW protected
    PieVectTable.TINT0 = &Timer0_ISR;//Link Timer0 to interrupt vector
    PieVectTable.SEQ1INT = &Adc_ISR;    //Link ADC to interrupt vector
    EDIS;                               //End EALLOW;
    PieCtrlRegs.PIECTRL.bit.ENPIE = 1;  //Enable Pie vector fetching
    PieCtrlRegs.PIEIER1.bit.INTx7 = 1;  //Enable Timer0 Interrupt into
                                        //PIE1 block
    PieCtrlRegs.PIEACK.all = 0xFFFF;    //Clear Acknowledgements
    IER = 0x01;        //Enable INT1 to CPU (timer0 in INT1)
    EINT;              //Enable Global Interrupts
}
```

Figure 43: DSP Interrupt Configuration

DSP GPIO Configuration

```
//Set all pins to low, outputs
void GpioSetup()
{
    EALLOW;        //Register is EALLOW protected

    //Configure GPIO pins: outputs, lows, no pull-up resistor
    GpioDataRegs.GPACLEAR.all = 0xFFFFFFFF;   //Low output
    GpioDataRegs.GPBCLEAR.all = 0xFFFFFFFF;   //Low output
    GpioDataRegs.GPCCLEAR.all = 0xFFFFFFFF;   //Low output
    GpioCtrlRegs.GPADIR.all = 0xFFFFFFFF;     //Configure as outputs
    GpioCtrlRegs.GPBDIR.all = 0xFFFFFFFF;     //Configure as outputs
    GpioCtrlRegs.GPCDIR.all = 0xFFFFFFFF;     //Configure as outputs

    EDIS;          //Ends EALLOW protection
}
```

Figure 44: DSP GPIO Configuration

6.3 Timer0 Setup

Timer0 was used for two purposes: to provide a delay upon startup and to delay the acquisition

of data after a switching action. Upon DSP power up, a delay was implemented after the basic

configuration and ADC circuitry was powered on. This was intended to ensure everything was

stable before performing the control. When the gate signal changed, noise was generated on all

feedback signals. Therefore, to neglect the noise and prevent inaccurate readings, a time delay

was implemented after the gate signal changed, preventing the control calculations. A flag was

cleared and Timer0 activated when the switch changed states. Once Timer0 overflowed and

interrupted, the flag was set and the control code was allowed to continue to calculate until the

next switch transition. Figure 45 details the Timer0 configuration and interrupt service routine.

DSP Timer0 Configuration and Interrupt

```
//Enable Timer0 Interrupt, Set to period of 5ms
void Timer0Setup()
{
      SysCtrlRegs.PCLKCR3.bit.CPUTIMER0ENCLK = 1;      //Activate Peripheral
                                                       //CPU1 Timer Clock
      CpuTimer0Regs.TCR.bit.TIE = 1;            //Enable Timer0
                                                //Interrupt at Peripheral Level
      CpuTimer0Regs.PRD.all = 0x000C;           //Main Counter
      CpuTimer0Regs.TPR.bit.TDDR = 0xFF;        //Prescale Value low
      CpuTimer0Regs.TPRH.bit.TDDRH = 0xFF;      //Prescale Value high
      CpuTimer0Regs.TCR.bit.TRB = 1;            //Reload the timer
      CpuTimer0Regs.TCR.bit.TSS = 0;            //Start the timer
}

//Reset Timer0, Turn off Timer0, disable timer0 interrupt, enable ADC
//interrupt, start ADC.  If past startup, set new_data flag to allow control
interrupt void Timer0_ISR()
{
      CpuTimer0Regs.TCR.bit.TIF = 1;    //Writing 1 clears the flag
      PieCtrlRegs.PIEACK.bit.ACK1 = 1; //Clears the acknowledgement for Int1
      if(STABILIZE == 1)
      {
            STABILIZE = 0;                      //signify end of start up delay
            CpuTimer0Regs.TCR.bit.TSS = 1;  //Stop the timer
            CpuTimer0Regs.PRD.all = 100;    //Main Counter
            CpuTimer0Regs.TPR.bit.TDDR = 0; //Prescale Value low
            CpuTimer0Regs.TPRH.bit.TDDRH = 0; //Prescale Value high
            CpuTimer0Regs.TCR.bit.TRB = 1;  //Reload the timer
      }
      else if(STARTUP == 0)  //used to prevent inaccurate data during noise
      {
            CpuTimer0Regs.TCR.bit.TSS = 1;      //Stop the timer
            CpuTimer0Regs.PRD.all = 700;        //Main Counter
            CpuTimer0Regs.TCR.bit.TRB = 1;      //Reload the timer
            NEW_DATA = 1;                       //set flag
      }
}
```

Figure 45: DSP Timer0 Configuration and Interupt

6.4 ADC Configuration and Interrupt

The ADC was configured to perform eight conversions in a sequence: output current once, secondary current once, primary current twice, and output voltage four times. The primary current and output current were oversampled to perform averaging on a sample basis. These two variables were selected to be averaged due to the sensitivity of the control to these variables compared to the secondary and output current. The ADC was configured in continuous sample mode meaning as soon as the 8 conversion sequence was completed, it restarted the sequence without needing to be told to do so. The ADC clock was also configured to the highest setting of 25MHz. TI programs each DSP with a unique calibration sequence as it comes off the assembly line when manufactured. This calibration is called by the 'ADC_cal()' function to ensure ADC accuracy. Figure 46 details the ADC configuration function.

The ADC interrupt was not used during normal operation but occasionally used for debugging purposes. Testing performed with the ADC interrupt included toggling a GPIO pin to see the conversion sequence period. Figure 46 details the ADC interrupt.

```c
void AdcSetup()
{
        //ADC Clock Setup
        EALLOW;                         //Registers are EALLOW protected
        SysCtrlRegs.HISPCP.bit.HSPCLK = 3;  //High Speed Clock,
                                        //HSPCLK, = SYSCLKOUT/6 = 150MHz/6 = 25MHz
        AdcRegs.ADCTRL1.bit.CPS = 0;            //ADC prescaler of 1
                                                //-> ADC Clock = 25MHz
        SysCtrlRegs.PCLKCR0.bit.ADCENCLK = 1; //Activate ADC Clock
        EDIS;

        //Calibration and General Startup
        AdcRegs.ADCTRL3.bit.ADCBGRFDN = 3;  //Power up ADC Bandgap reference
        AdcRegs.ADCTRL3.bit.ADCPWDN = 1;    //Power up ADC circuitry
        ADC_cal();                      //Calls factory calibration procedure
        AdcRegs.ADCMAXCONV.bit.MAX_CONV1 = 7;     //8 Conversions Take Place
        AdcRegs.ADCTRL1.bit.ACQ_PS = 20;    //S/H window 1 * 25Mhz period
        //Choose which channels to convert in which order
        AdcRegs.ADCCHSELSEQ1.bit.CONV00 = 4;      //Vo
        AdcRegs.ADCCHSELSEQ1.bit.CONV01 = 3;      //Ip
        AdcRegs.ADCCHSELSEQ1.bit.CONV02 = 4;      //Vo
        AdcRegs.ADCCHSELSEQ1.bit.CONV03 = 2;      //Io
        AdcRegs.ADCCHSELSEQ2.bit.CONV04 = 4;      //Vo
        AdcRegs.ADCCHSELSEQ2.bit.CONV05 = 5;      //Is
        AdcRegs.ADCCHSELSEQ2.bit.CONV06 = 4;      //Vo
        AdcRegs.ADCCHSELSEQ2.bit.CONV07 = 3;      //Ip

        //Adc Interrupt Setup
        AdcRegs.ADCTRL2.bit.INT_MOD_SEQ1 = 0;//Seq1 Interrupt at every EOC
        AdcRegs.ADCTRL2.bit.INT_ENA_SEQ1 = 1;//Seq1 Interrupts enabled

        AdcRegs.ADCTRL1.bit.SUSMOD = 2; //ADC stops after current conversion
                                        // when debugger hits breakpoint
        AdcRegs.ADCTRL1.bit.CONT_RUN = 1;   //allows continuous running
        AdcRegs.ADCTRL2.bit.RST_SEQ1 = 1;   //Reset Seq1
}

//used for sequence period measurement
interrupt void Adc_ISR()
{
        AdcRegs.ADCST.bit.INT_SEQ1_CLR = 1;             //Clear Interrupt Flag
        PieCtrlRegs.PIEACK.bit.ACK1 = 1;//Clears the acknowledgement for Int
        AdcRegs.ADCTRL2.bit.RST_SEQ1 = 1;       //Reset Seq1
        AdcRegs.ADCTRL2.bit.SOC_SEQ1 = 1;       //Start Seq1 conversion
        GpioDataRegs.GPATOGGLE.bit.GPIO20 = 1; //Set Pin if toggle desired
}
```

Figure 46: DSP ADC Configuration and Interrupt

6.5 Main Loop and NSS Control

The first tasks in the main loop are to call the described functions above to configure the system and peripherals. After the stabilization delay, the switch is turned on for the first time and the code enters an infinite loop. Figure 26 from Chatper 4 details the algorithm that is implemented in the loop. The startup method because turning off at a hard input peak current limit and waiting for the seoncdary current reaches zero, just as Figure 26 describes. The CCM start up discussed in Section 4.7 made the implementation more difficult with very little gained. Each main loop consists of calculating the average of the sampled ADC data and calculating the normalized off-trajectory to determine the desired switch status.

If the switch is on, the switch can be turned off once the converter's state is greater than the off-trajectory or the primary current has reached a maximum limit, here set at 22A. If the switch is off, it can only be turned on again after the secondary current has reached zero and the system is below the off-trajectory. The off trajectory can be simplified depending upon what state you are in. During the on-state, equation (66) can be expanded to (81) which simplifies the multiplication . During the off-state, we force the system to wait till the magnetizing current is zero before checking the off-trajectory. Therefore, we can simplify (66) to (82).

$$\lambda_{off} = v_{on}^2 + i_{mn}^2 - 2i_{mn}i_{on} - 1 \tag{81}$$

$$\lambda_{off} = v_{on}^2 - 1 \tag{82}$$

```
int main()
{
      OscillatorSetup(); //Clock Out is 150MHz, Watchdog Disabled
      InterruptSetup();  //Enable Global Interrupts and Timer0
      GpioSetup();       //Set all as low outputs
      AdcSetup();        //Setup ADC
      Timer0Setup();     //5ms Period, waiting for ADC to stabilize

      long vo_array[4] = {0, 0, 0, 0};    //vo average array
      int i = 0;                          //vo array index
      long long vo_total = 0;             //running vo average array total
      int vo_ave = 0;                     //vo average
      long seq_ave = 0;                   //vo conversion sequence average
      int ip_average = 0;                 //ip average

      //dummy loop for stabilization from timer0
      do
      {
      }while(STABILIZE);

      //switch on for first time
      EALLOW;      //allow registers to be modified continuously, no EDIS
      GpioDataRegs.GPASET.bit.GPIO28 = 1; //Set Pin, gate signal
      Q = 1;                              //Set flag
      CpuTimer0Regs.TCR.bit.TSS = 0;//Start the timer to block calculations
      AdcRegs.ADCTRL2.bit.SOC_SEQ1 = 1;   //Start Seq1 conversion

      //infinite main loop
      while(1)
      {
         if(NEW_DATA == 1)    //only calculates after switching noise gone
         {
                 //average vo in this sequence
                 seq_ave = AdcMirror.ADCRESULT0;
                 seq_ave = seq_ave + AdcMirror.ADCRESULT2;
                 seq_ave = seq_ave + AdcMirror.ADCRESULT4;
                 seq_ave = seq_ave + AdcMirror.ADCRESULT6;
                 vo_ave = seq_ave >> 2;  //store vo average

                 //calculate a running sequence average. Round robbin
                 vo_total  = vo_total + vo_ave;//add to total
                 vo_array[y] = vo_ave;         //add to array
                 y++;                          //index array
                 if(y > 3)                     //loop around if past size
                       y = 0;
                 vo_ave = vo_total >> 4;       //calculate the average
                 vo_total = vo_total - vo_array[y];  //remove last value

                 //average primary current for this sequence
                 ip_average = AdcMirror.ADCRESULT1;
                 ip_average = ip_average + AdcMirror.ADCRESULT7;
                 ip_average = ip_average >> 1;
         }
```

```c
if(Q == 1 && NEW_DATA == 1)    //Switch is on, calculate boundary
                                        //and compare if above or below
        {

    //off state trajectory
    if((vo_ave*0.000366211+0.08)*(vo_ave*0.000366211+0.08)+(ip_average*
        0.0000140477+0.00000211395)*(ip_average*0.0000140477+0.00000211395)-
        2*(ip_average*0.0000140477+0.00000211395)*(AdcMirror.ADCRESULT3*
        0.00000810274-0.0162190)-1 > 0.0)
        {
            GpioDataRegs.GPACLEAR.bit.GPIO28 = 1; //turn off switch
            Q = 0;                                //set switch  off flag
            NEW_DATA = 0;                         //prevent calculations
            CpuTimer0Regs.TCR.bit.TSS = 0;        //Start the timer
        }
        //turn off if past peak limit
        else if((ip_average*0.0058895) > 22.854)
        {
            GpioDataRegs.GPACLEAR.bit.GPIO28 = 1; //turn off switch
            Q = 0;                                //set switch  off
            NEW_DATA = 0;                         //prevent calculations
            CpuTimer0Regs.TCR.bit.TSS = 0;        //Start the timer
        }
        //else, Q stays on
        }

        else if (Q == 0 && NEW_DATA == 1) //switch is off
        {
        //check for zero secondary current
        if(AdcMirror.ADCRESULT5*0.000914063 - 0.6735 < 0.15018 )
        {
          //calculate simplified off trajectory
          if((vo_ave*0.000366211+0.08)*(vo_ave*0.000366211+0.08) < 1)
          {
              GpioDataRegs.GPASET.bit.GPIO28 = 1; //Turn on switch
              Q = 1;           //Set switch on
              NEW_DATA = 0;   //prevent calculation
              CpuTimer0Regs.TCR.bit.TSS = 0;      //Start the timer
          }
          //else, Q stays off
        }
      //else, Q stays off
      }
    }
    return 0;
}
```

Figure 47: DSP Main Program Loop

VII. Experimental Results

7.1 Sensor Calibration

Immediately upon testing, it was evident that the transformer was not capable of transferring the 100W it was designed for. The transformer saturated, decreasing the magnetizing inductance, and cause the input current to rise quickly. Therefore, the load on all testing was 500Ω, which is equivalent to 90W during steady state.

Figure 48 shows the primary and secondary feedback current signals at the input of the ADC. Each signal was simultaneously compared to its corresponding LEM sensor output to calculate the gain equation for each channel. For the output voltage, a digital multi-meter was attached to the output voltage while monitoring the output voltage feedback line. Data points were acquired and a line of best fit was established. Since the load was known and purely resistive, the output current was calibrated in the same way.
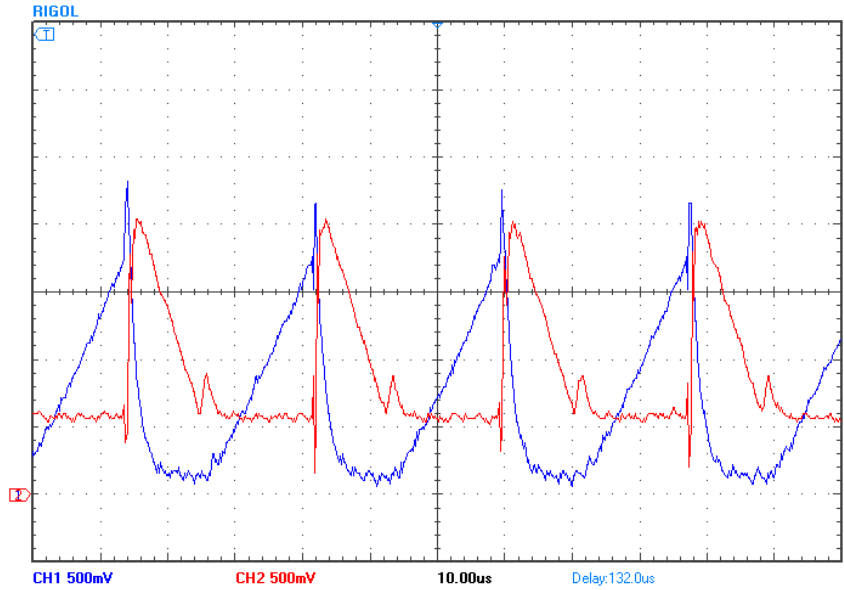
Figure 48: Primary and Secondary Feedback Signals using Function Generator

Blue-Secondary Current, Red-Primary Current

7.2 Main Loop Period

The main loop period was calculated by toggling a GPIO pin every cycle. Figure 49 shows this toggle overlaid on the primary current feedback signal for reference. During the switching transitions, the toggle frequency is greatly increased until Timer0 interrupts. This is due to the NEW_DATA flag intentionally preventing the DSP from performing calculations during noisy areas. It is also notable that the frequency of loops is faster during the off-state than the on-state. This is due to the fact the off-trajectory calculation is greatly simplified in comparison to the on-state. On average, the on-state period was approximately 1us and the off-state period was approximately 600ns.
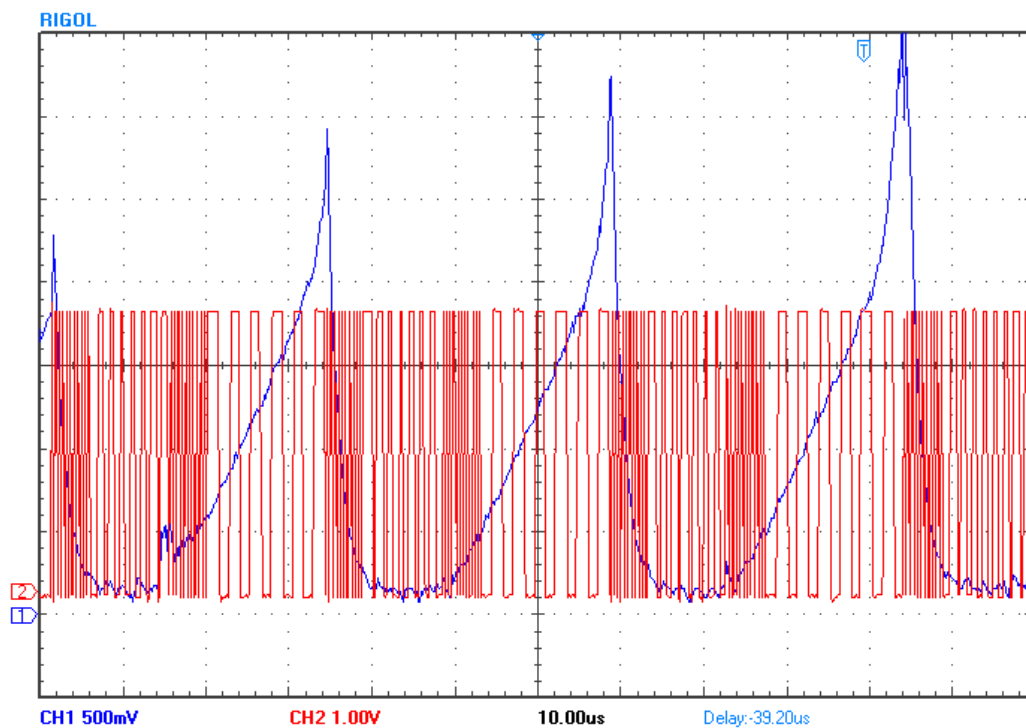
Figure 49: Main Loop Period Calculation

Red-GPIO Toggle, Blue-Primary Current

7.3 Steady State Primary and Secondary Feedback Signals

?? and ?? show two snap shots of what should be the steady state signals of the primary and secondary currents. There is a slight oscillation of the current peak at times, instead of the expected constant peak value. This could be coming from noise in the feedback lines or delays in the program execution. Another possibility could be form the time delay introduced from introducing a moving average on the output voltage. More research and debugging will need to be performed to find the root of the issue.
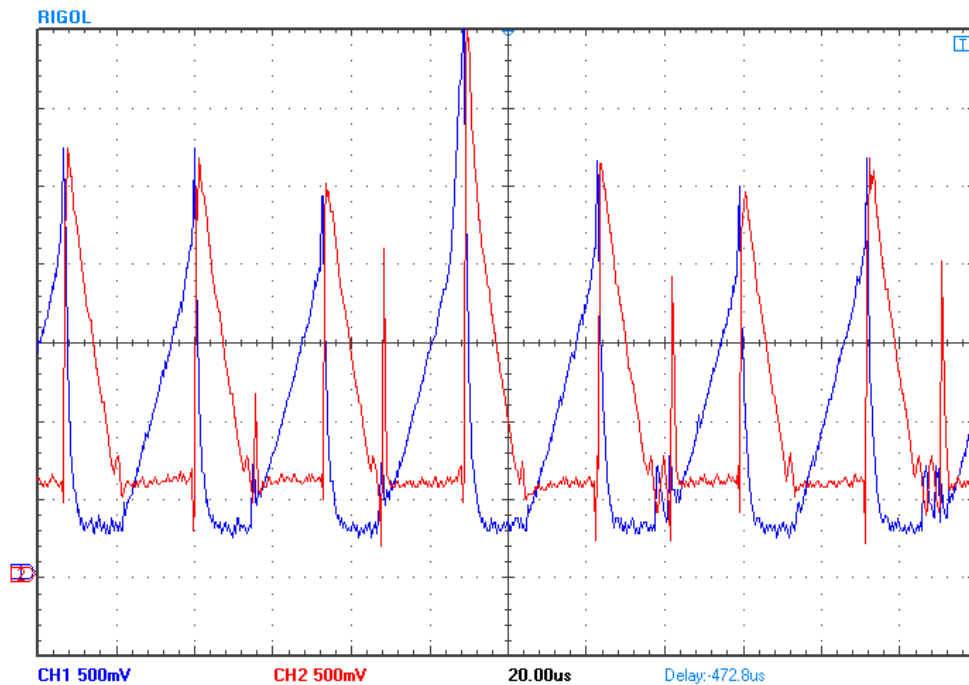
Figure 50: Steady State Primary and Secondary Current with DSP Control

Blue-Primary Current, Red-Secondary Current
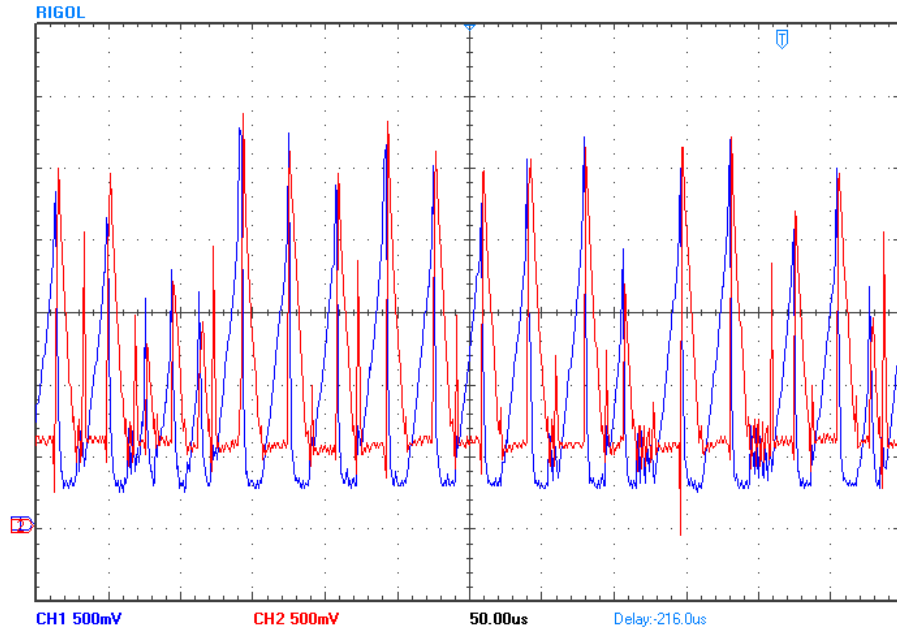
Figure 51: Steady State Currents Indicating Oscillation Error

Blue-Primary Current, Red-Secondary Current

7.4 Start Up Output Voltage

Figure 52 shows the output voltage during start up. To reach the steady state value of 200V it takes approximately 35ms. This is extremely comparable to the simulated result with the same startup method shown in Figure 24. Here, the simulated time to reach 200V was 34ms. The experimental results show a slight overshoot of output voltage equivalent to less than 10V, but no oscillation. During steady state, a digital multi metered connected to the output reads an AC voltage ripple of only 200mV.
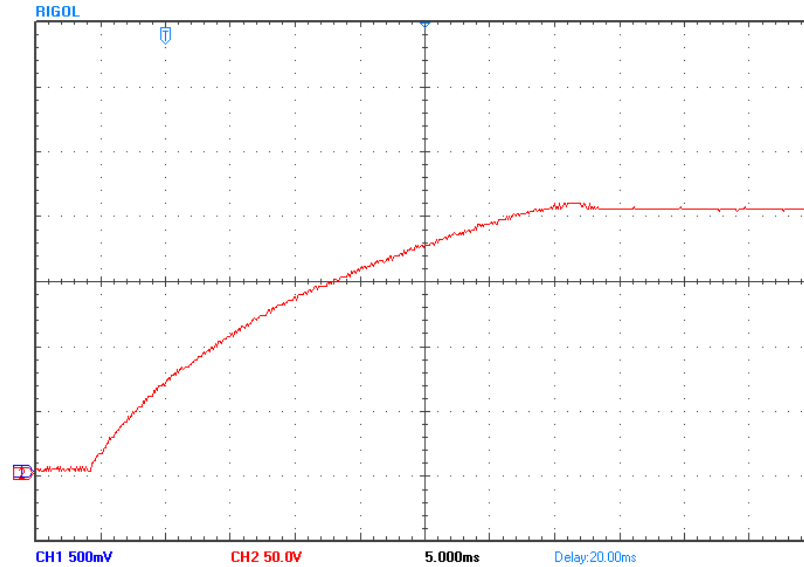
Figure 52: Start-up Output Voltage

7.5 Output Voltage Regulation to Input Voltage Drop

Figure 53 shows the stability of the NSS control. The input voltage was dropped 17V over 600ms. The output voltage is shifted 200V down the y-axis from the center grid so that the signal could have a high enough gain for the output voltage change to be noticeable. Therefore, the output voltage started at 200V before the input voltage change and ended at approximately 199V after the change. The NSS control successfully regulated the output voltage within an acceptable tolerance to a wide input swing.
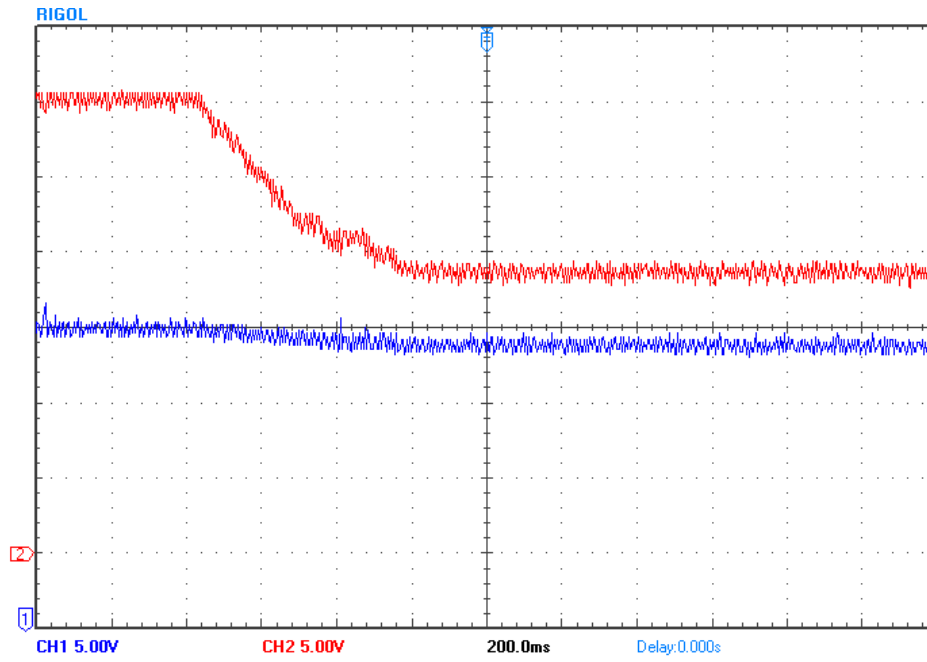
Figure 53: Input Voltage Drop

Red-Input Voltage, Blue-Output Voltage

Conclusion

This thesis covered from the derivation to the experimental testing of a flyback converter implementing the Natural Switching Surface control method. The normalized NSS derivations were detailed in Chapter 3 and the desired BCM control law was solved for in Chapter 4. Following the derivations, the control law was simulated and validated in MATLAB/Simulink$^©$. A 90W flyback converter prototype was designed and constructed, detailed in Chapter 5. The NSS control law was developed in a DSP, explained in Chapter 6, and experimental results were obtained and summarized in Chapter 7.

The NSS control adequately regulated the flyback converter. A steady state output voltage near 200V was reached and held. The flyback converter was able to recover from an input voltage swing of 17V with only a 1V change on the output. The steady state primary and secondary currents did have some errors. Where a constant peak current was expected on the currents during steady state, an oscillatory nature was noticed. This could be induced by noise on the feedback signals or delays in the DSP programming implementation. A downfall of this control technique is that the converter is operating under variable frequency, making EMI considerations more difficult.

Future research could include analyzing the effects of noise on the feedback signals and which signals are more sensitive. Each variable in the off-trajectory is not weighted equal. Therefore, a small change in a variable's signal due to noise could introduce large output errors. Other research could be an attempt to minimize needed sensors by using known state variables and operation of the flyback converter and predicting the unknown variables.

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Appendix A

Appendix A details the schematics used for the hardware implementation of the 90W flyback
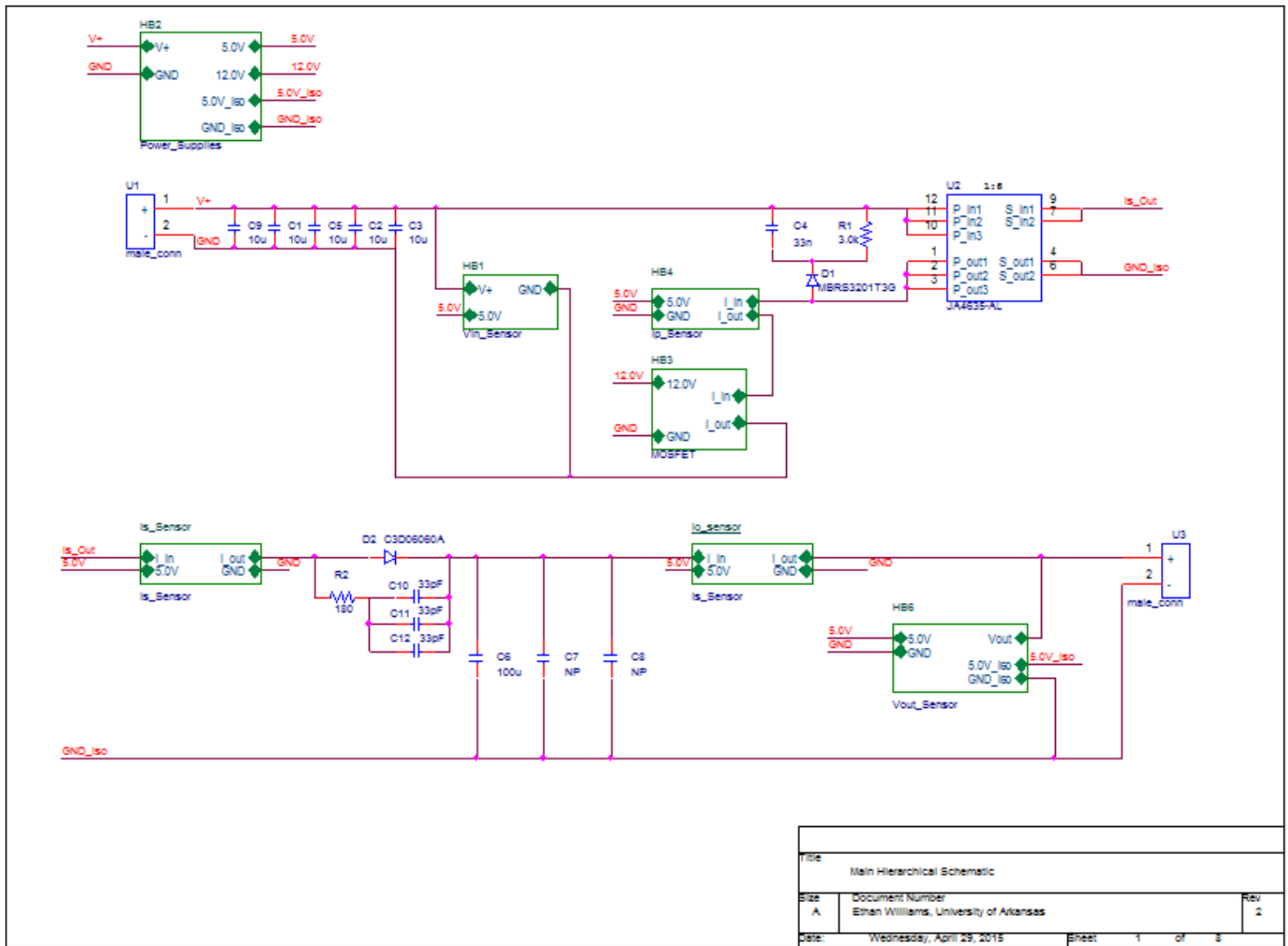
converter prototype. The board design is also included in this appendix.

Figure 54: Main Hierarchical Schematic
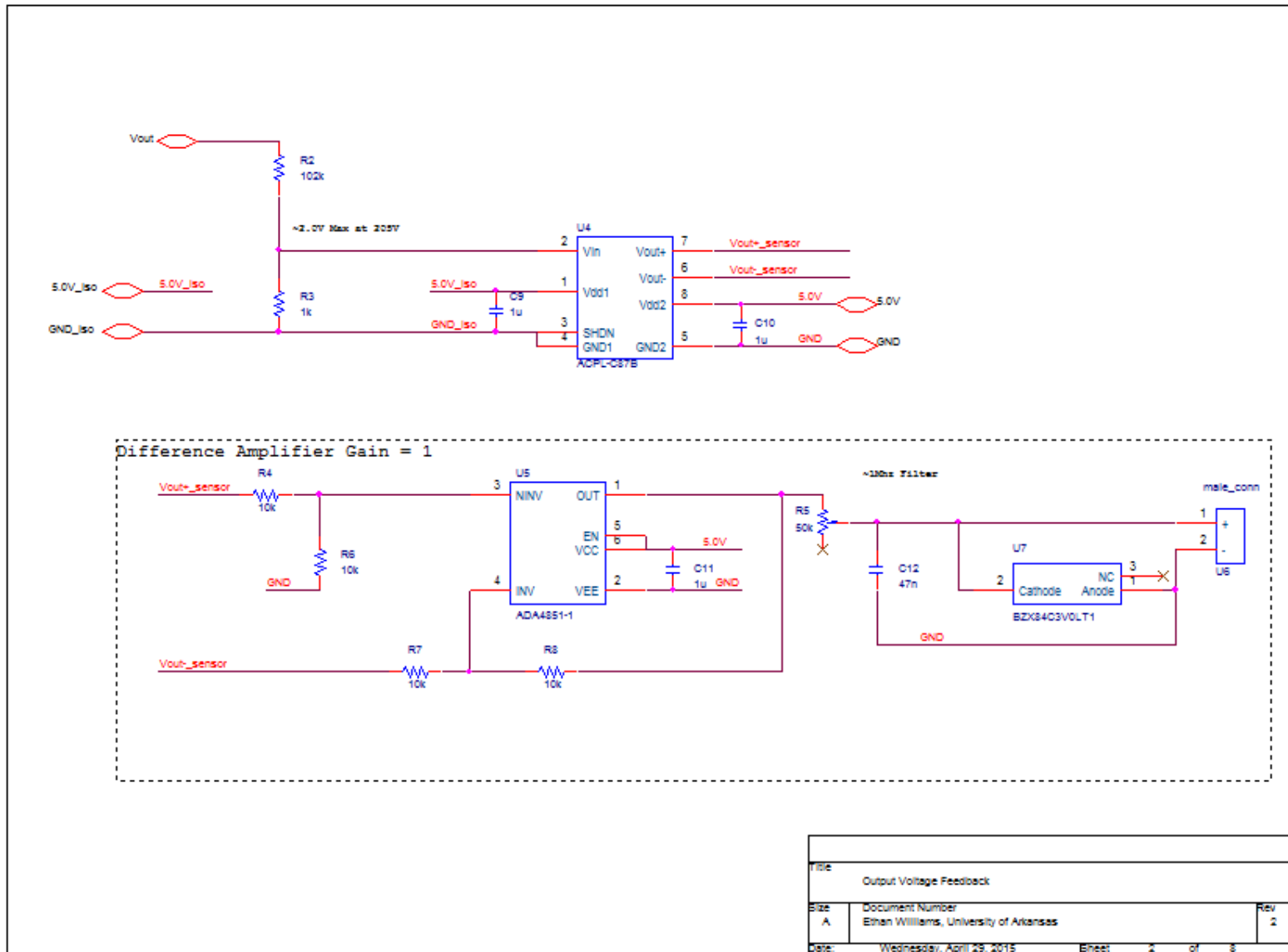
Figure 55: Output Voltage Schematic
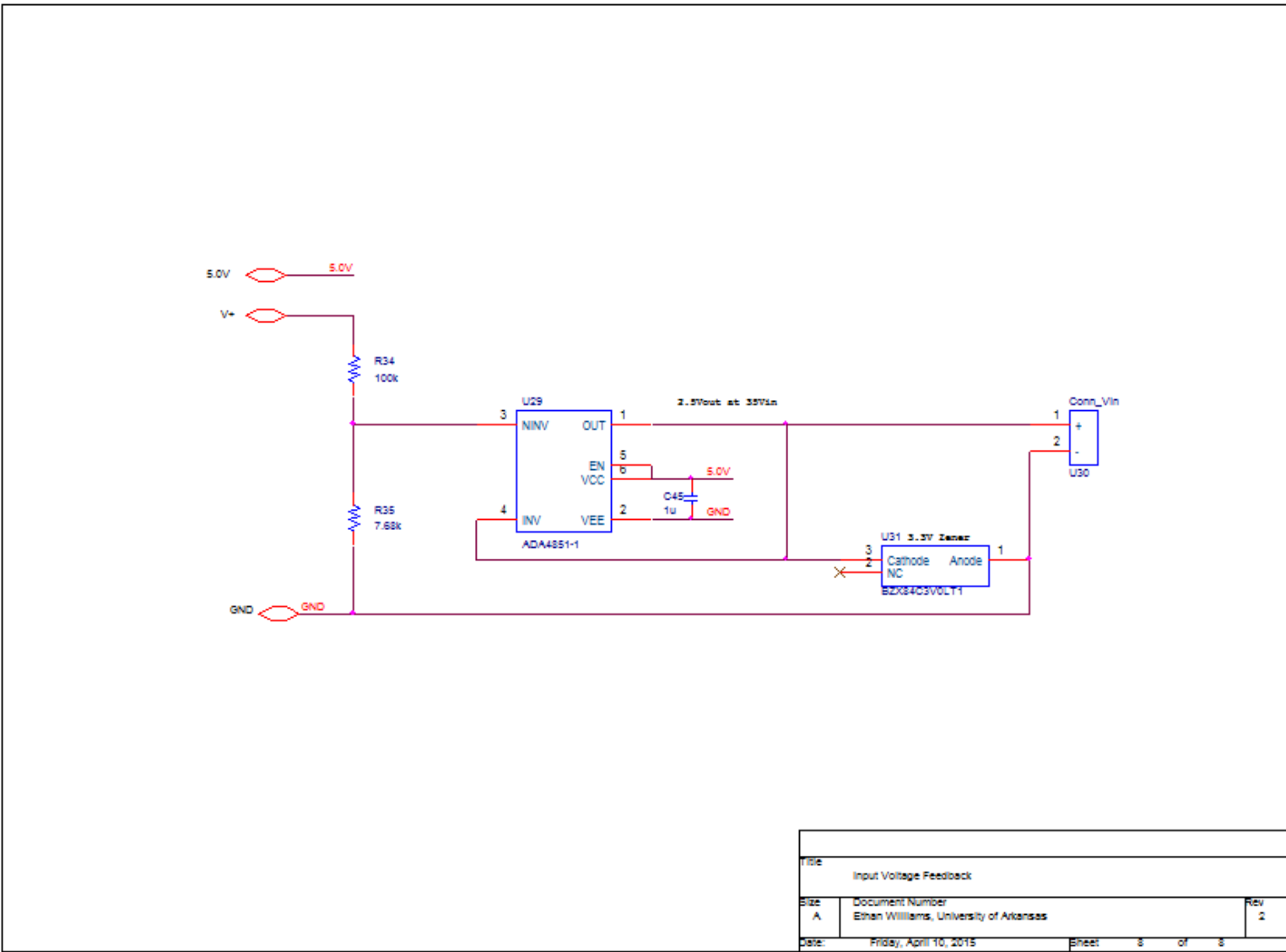
Figure 56: Input Voltage Schematic
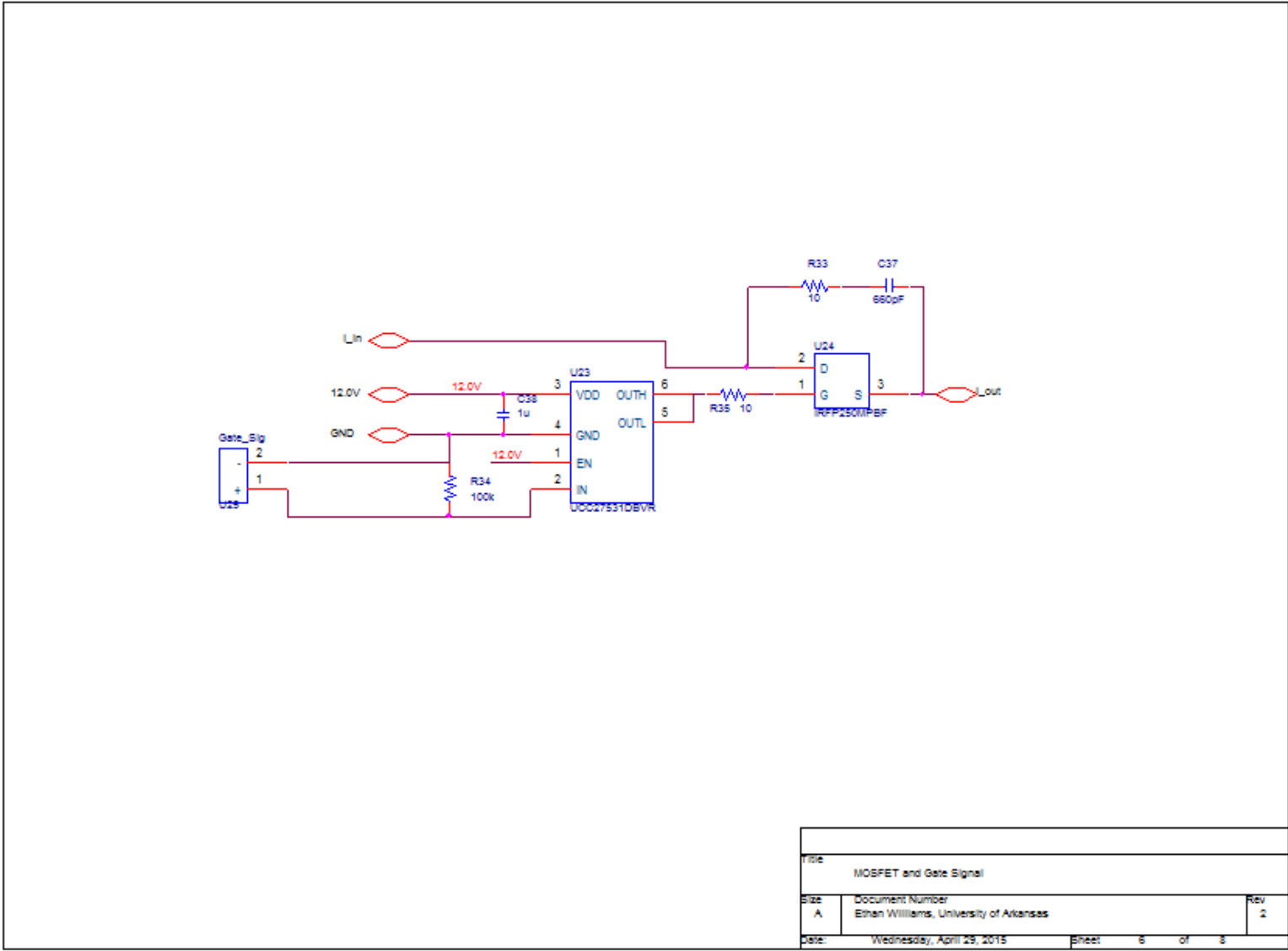
Figure 57: MOSFET and Gate-Driver Schematic
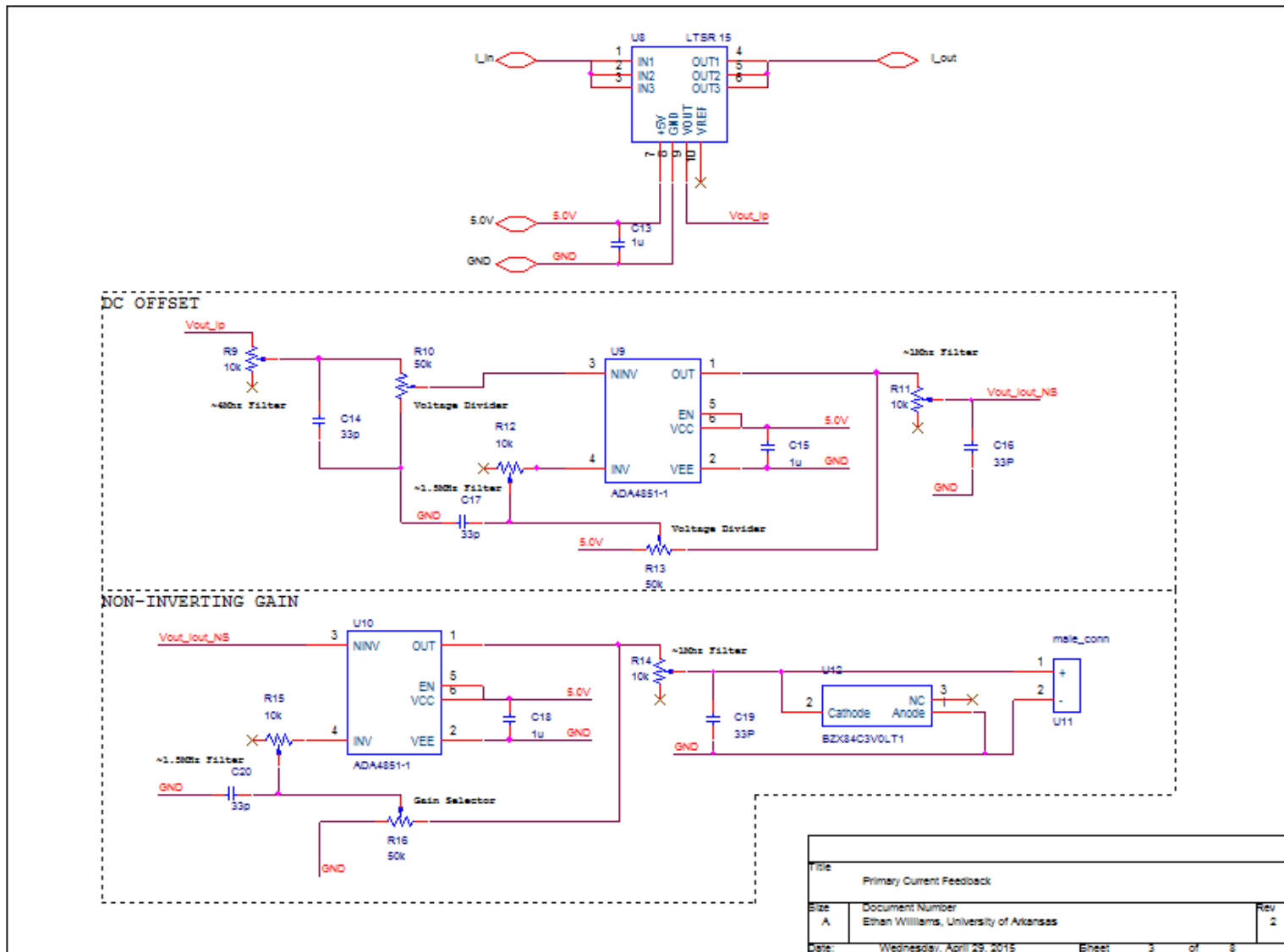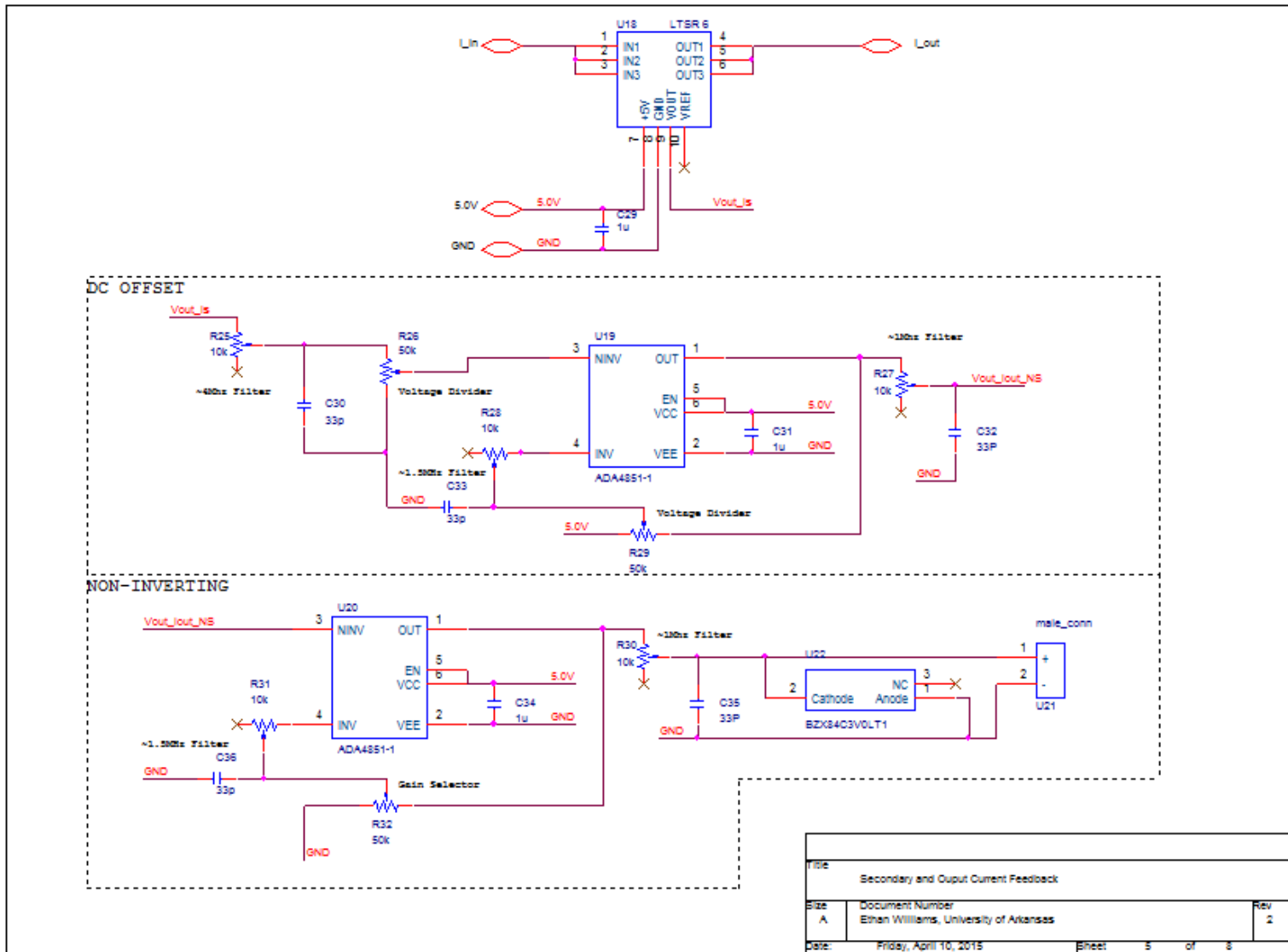
Figure 58: Primary Current Schematic
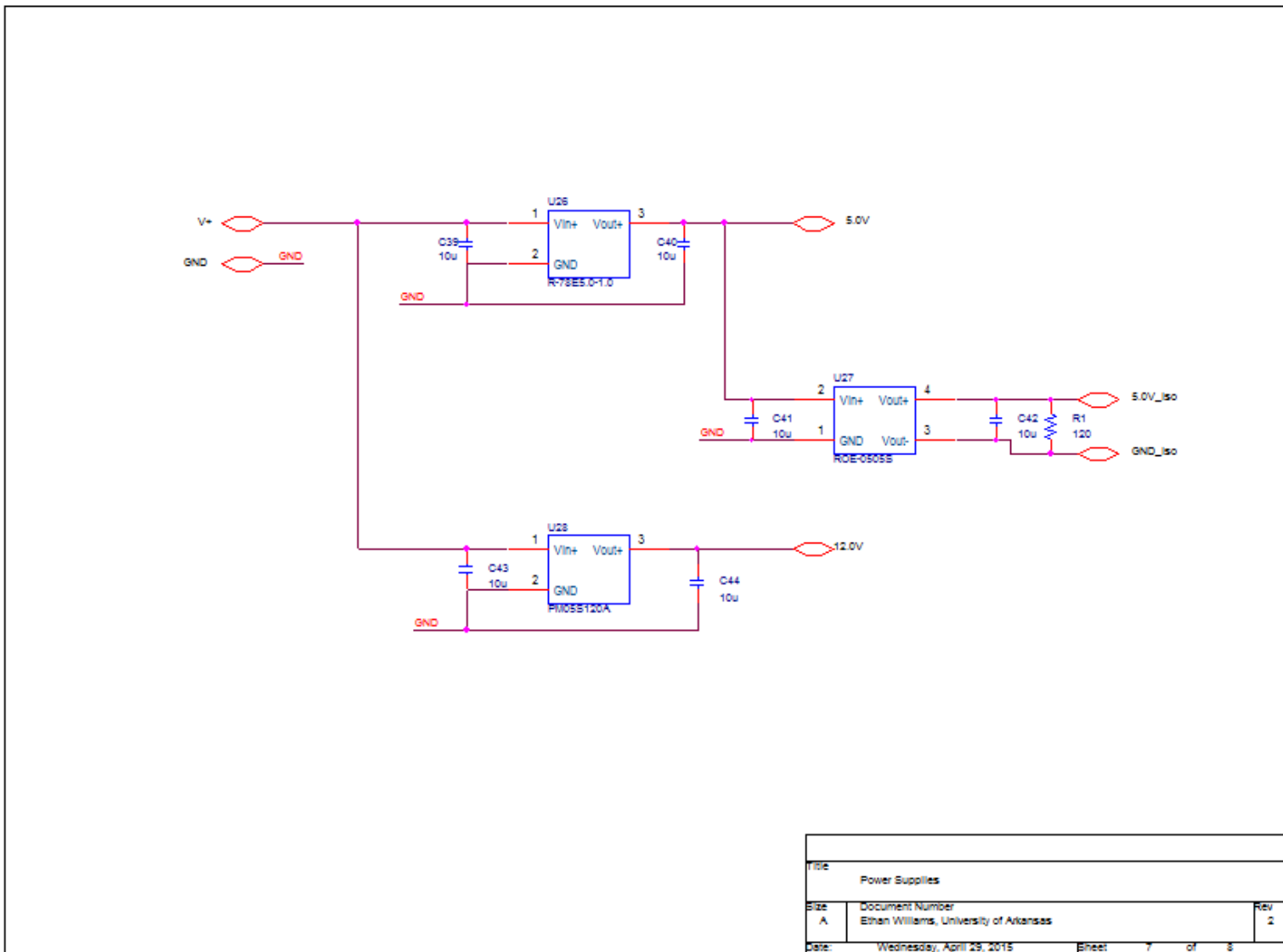
Figure 59: Secondary and Output Current Schematic
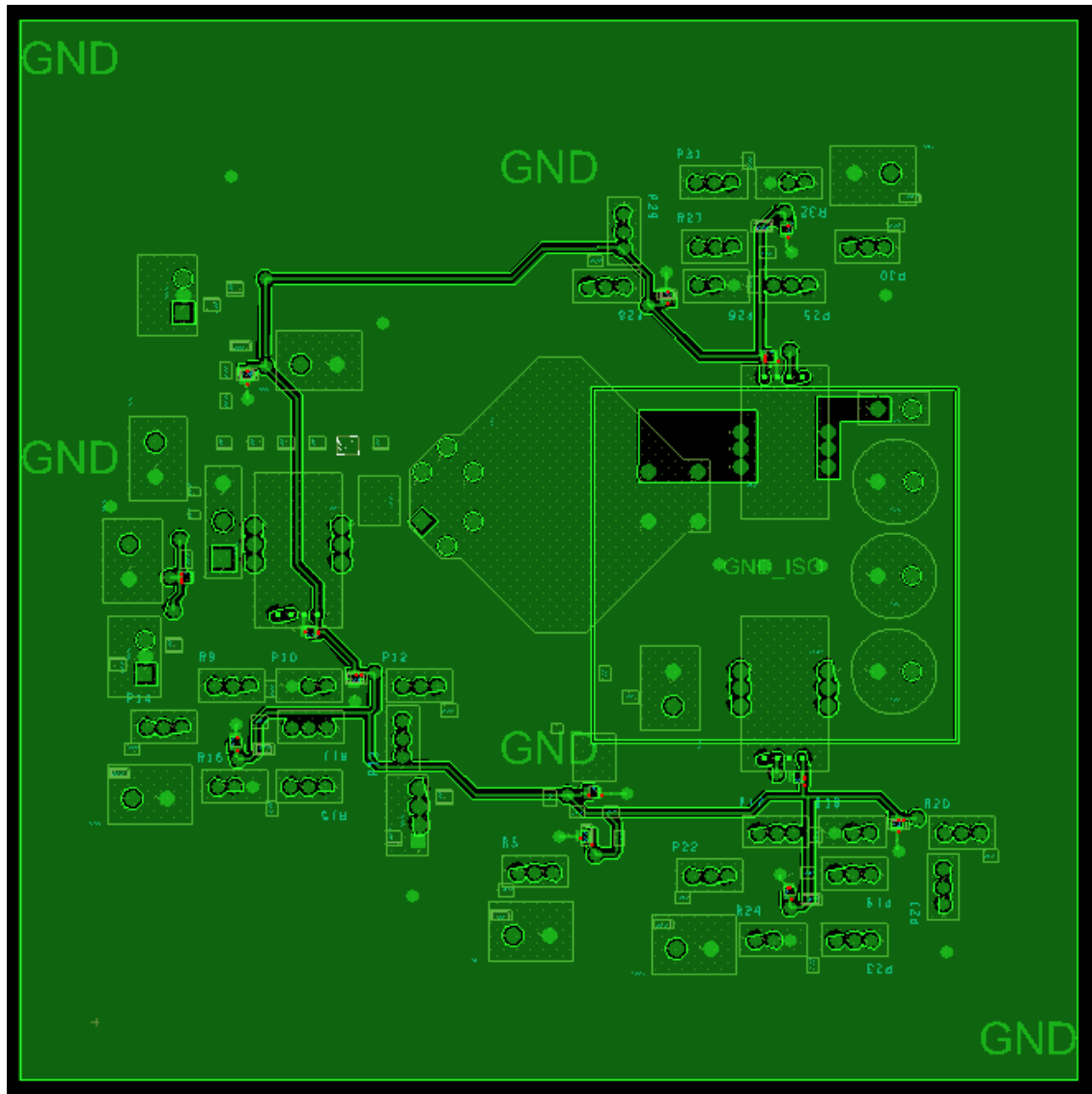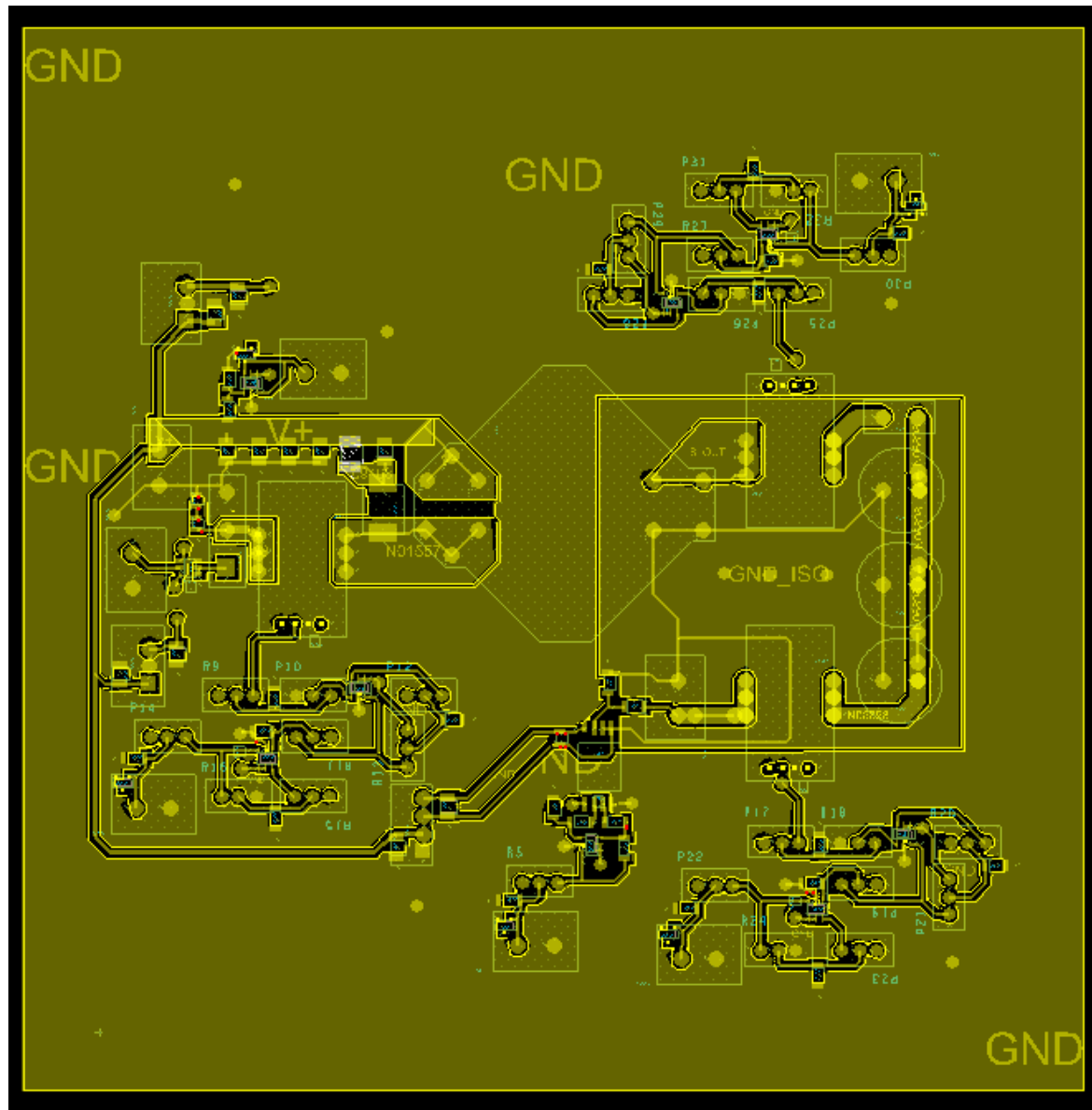
Figure 60: Power Supply Schematic

Figure 61: Top of Allegro Board Layout

Figure 62: Bottom of Allegro Board Layout