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Coreless Planar Transformer using Low-Temperature Co-fired Ceramics for Isolated Gate Driver Applications

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Coreless Planar Transformer using Low-Temperature Co-fired Ceramics for Isolated Gate Driver Applications

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by

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This thesis is approved

Thesis Advisor:

Thesis Committee

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Abstract

The aim of this thesis project is to design a signal isolation transformer for gate driver applications using coreless planar transformers (CPT) on a low-temperature co-fired ceramic (LTCC) substrate. To achieve this goal a modulator-demodulator circuit will be selected from several existing designs and an isolation transformer will be designed as a CPT to produce a high frequency high temperature signal isolation for gate driver applications in switching converters, audio drivers, and motor drives. Several designs for coreless planar transformers will be evaluated and tested, and the results will be compared to the theoretical performance obtained from SPICE models for each transformer design.

Acknowledgements

I would like to acknowledge John Fraley, Dr. Alex Lostetter, and the APEI team for making this thesis possible. I would like to express my sincere thanks to Kaoru Porter and Errol Porter for their tremendous help and guidance during the design and fabrication of this experiment.

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I. Introduction

The purpose of this thesis is to design a Coreless Planar Transformer (CPT) on Low-Temperature Co-fired Ceramic (LTCC) for electrical isolation of input signals. CPTs provide several advantages over traditional wound transformers or ferrite-core planar transformers. These include reduced manufacturing steps as the transformer is part of the PCB, decreased power losses at higher frequencies by eliminating core losses, and reduced overall system size and cost. Using this technology on LTCC provides further advantages of higher operating temperature and increased feature resolution for the transformer. Electrical isolation is important in many gate driver applications to protect the electronics driving the input from damage from noise or EMF spikes fed back to the input from the power stage output. The electrical characteristics of the CPT will be highly dependent on the manufacturing process however the design of these transformers gives the designer greater control in optimizing such as precise winding spacing and orientation when compared to traditional wire-wound magnetics. This design will have many benefits in applications, besides reduced cost by combining the transformer and the substrate into a single unit, for instance higher operating temperatures can allow for smaller thermal management systems, which reduces overall system size and further reduces system cost. Coreless transformers have the potential to increase system efficiency since they have no core loss and for higher frequencies the magnetization current is reduced, meaning less power is lost in the windings.

II. Background

The design of a CPT is highly dependent on geometry. The basic planar transformer consists of spiral traces on two or more layers of a multi-layered substrate. The transformer can be fully

characterized by the layout of each spiral inductor, specifically the outer radius, the trace width, the distance center to center between adjacent traces, and the number of turns, as well as the separation between the layers supporting the spirals [2]. An example of the three dimensional geometry of a Coreless Planar Transformer can be found in Figure 1. As shown in previous research [7] the number of turns, the outer radius, and the layer separation have the most significant impact on the inductive properties of the transformer. When the layer separation is much smaller than the spiral radius the magnetic coupling between inductors becomes significant and will result in mutual inductance without a ferromagnetic core present between the coils; hence the coreless term in CPT.

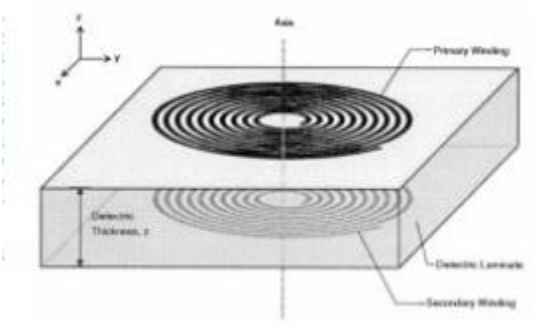

Figure 1. 3D geometry of CPT [7]

Several CPT designs were evaluated with varying winding size, spacing, and ratios. Design considerations for the transformer include sufficient breakdown voltage between windings and between coils based on dielectric strength of the LTCC and a gain that will result in the secondary output to be within the input range of the demodulator at the operating frequency which can be adjusted by changing the winding ratio. For use in high temperature gate driver

applications the transformer must be able to produce the expected performance at temperatures of at least 225C.

III. Design

A. Schematic Design

First, several modulator and demodulator pairs that are suitable for gate driver designs were evaluated for transitioning utilizing a CPT on LTCC. Utilizing one of the existing solutions that has previously been proven to function with traditional wire-wound transformers provided a baseline with which the LTCC CPT design could be compared. Once the modulation system had been decided upon the transformer portion of the isolation circuit was redesigned by replacing the original magnetic isolation components with a CPT. Several CPT designs were evaluated and the most suitable layout was used. The CPT designs selected to be tested were designed based on the requirements of the modulation system for drive current of the primary and the minimum voltage gain of the transformer. For the modulation system several available designs were evaluated. The target frequency of the transformers was between 10-20 MHz so the modulator and demodulator needed to be able to meet these frequencies as well as operate at temperatures up to 225 °C. Due to availability a custom High Temperature Silicon on Insulator (HTSOI) IC designed at APEI Inc. was selected for the modulator and demodulator pair. The modulator can operate between 5-50 MHz and has a drive strength of 8mA.

B. MATLAB code

The equivalent circuit model for the transformer can be found in Figure 2. The equivalent transformer model parameters for each transformer geometry was determined using MATLAB

code based off the equations derived in [8]. The series resistance of the spiral coils, R_p and R_s for the primary and secondary spirals respectively, was calculated by finding the total length of the spiral trace and dividing by the width of the trace to determine the number of squares that make up the spirals. The resistivity of the conductor used for the trace given by the manufacturer in units of Ohms per square can then be multiplied by the number of squares to find the resistance of a spiral inductor in Ohms. The capacitive elements $C1$ and $C2$ in the model represent the parasitic capacitance present between adjacent spiral windings within the same coil. These values were calculated by summing the capacitance from each turn of the spiral to the next turn approximated as closed circles and using the dielectric constant of the substrate. The capacitive element $C12$ in the model represent the parasitic capacitance between the primary and secondary coils. This was calculated by finding the total area of the traces for each spiral and using a parallel plate approximation with the dielectric constant of the substrate.

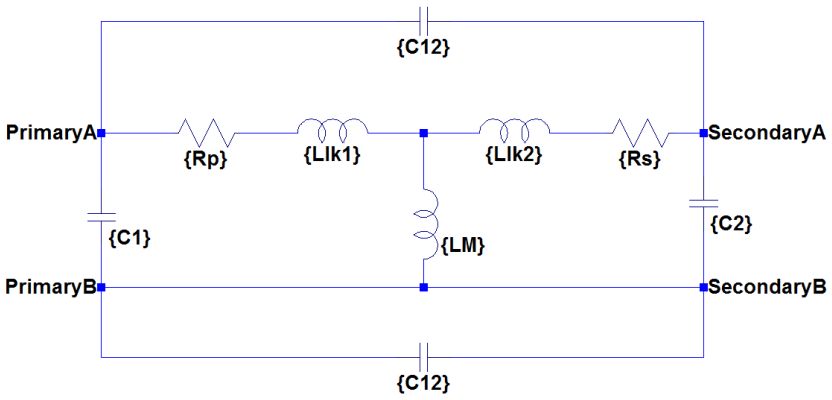

Figure 2. High Frequency Equivalent Circuit of CPT

The inductance values in the equivalent circuit model can be derived from Maxwell's equations for approximating the inductance of two circular filaments in air [8]. The equation used to calculate the mutual inductance of two circular filaments is given below.

$$M_{ij} = \frac{\mu_0 \pi}{h_1 \ln\frac{r_2}{r_1} h_2 \ln\frac{a_2}{a_1}} \int_0^\infty S(kr_2, kr_1) * S(ka_2, ka_1) * Q(kh_1, kh_2) e^{-k|z|} dk \quad (3.1)$$

$$S(kr_2, kr_1) = \frac{J_0(kr_2) - J_0(kr_1)}{k} \quad (3.2)$$

$$S(ka_2, ka_1) = \frac{J_0(ka_2) - J_0(ka_1)}{k} \quad (3.3)$$

$$Q(kh_1, kh_2) = \frac{2}{k^2}(\cosh k\frac{h_1+h_2}{2} - \cosh k\frac{h_1-h_2}{2}), when\ z > \frac{h_1+h_2}{2} \quad (3.4)$$

$$Q(kh_1, kh_2) = \frac{2}{k}\left(h - \frac{e^{-kh}-1}{k}\right), when\ z = 0, h = h1 - h2 \quad (3.5)$$

Where h_1 and h_2 are the inner and outer radii of one filament and a_1 and a_2 are the inner and outer radii of the other and z is the distance between filaments.

The two inductances labeled $Llk1$ and $Llk2$ are the leakage inductances of the primary and secondary coils respectively. They are calculated by first finding the self-inductance of the coil and subtracting from it the mutual inductance of the pair of coils which is discussed later. This represents the magnetic field that is generated each inductor in the transformer but does not get coupled to the other side. The self-inductance of a planar transformer can be calculated by approximating the spiral turns as a series of closed concentric circular filament and using Maxwell's equations to find the inductance between adjacent circles of the same spiral and summing across the entire coil. The self-inductance of a spiral coil is calculated with the following equation.

$$L_p = \sum_{j=1}^{N_p} \sum_{i=1}^{N_p} M_{ij} \quad (3.6)$$

Where Np is the number of turns of the coil.

Finding the mutual inductance, LM in the model, between two planar coils is done in a similar manner. The calculation involves two sums using Maxwell's equation on the same approximated concentric circles. One summation for circular filament in the primary side to each of the circular

filaments on the secondary side, and the second summation for the mutual inductance contributed by each turn of the primary coil. The equation for this is shown below.

$$M_{ps} = \sum_{j=1}^{N_p} \sum_{i=1}^{N_s} M_{ij} \tag{4.7}$$

Where Np is the primary turns and Ns is the secondary turns.

Notably absent from the model in Figure 2 but found in the traditional transformer model is a resistive element in parallel with the inductor, LM. This resistor in the traditional transformer model represents the eddy current losses dissipated as heat and hysteresis losses from reversing the magnetic fields in the transformer. Both of these losses are occur in the core of the transformer. With this being a coreless transformer these losses are eliminated from the model [1].

Table 1. SPICE Model Parameters

Parameter	TA	TB	TC	TD	TE
Rp (Ω)	1.1313E+01	1.1501E+01	2.8712E+00	3.4499E+01	3.8227E+01
Rs (Ω)	1.1313E+01	1.1501E+01	2.8712E+00	3.4499E+01	3.8227E+01
C1 (F)	8.7881E-13	1.2113E-12	2.9861E-13	2.7267E-12	3.0219E-12
C2 (F)	8.7881E-13	1.2113E-12	2.9861E-13	2.7267E-12	3.0219E-12
C12 (F)	6.5758E-11	6.8121E-11	5.6863E-11	6.7851E-11	2.2642E-10
LM (H)	2.9715E-06	3.4013E-06	8.7534E-07	7.6521E-06	1.8531E-05
Llk1 (H)	2.2428E-07	2.5495E-07	5.8301E-08	6.2392E-07	7.6598E-07
Llk2 (H)	2.2428E-07	2.5495E-07	5.8301E-08	6.2392E-07	7.6598E-07

C. LTCC Design

Previous research has shown that the parameters that have the most significant impact on the electrical properties of the CPT are the outer radius of the spiral, the number of turns, and the layer separation between the spiral coils. According to [7] the mutual inductance is inversely proportionate to the coil separation therefore for optimum gain between the primary and secondary coils the coils should be as close together as possible. The LTCC fabrication was performed using DuPont's Green Tape 951 system with 10 mil thick tape. This resulted in a minimum distance between conductive layers of approximately 215 μm after firing. Working with a fixed z variable in the MATLAB code discussed previously, the values of w, s, and N were adjusted to produce several different sets of values for the electrical parameters in the equivalent circuit model. These values were then simulated in SPICE and evaluated based on the current draw and voltage gain within the target operating frequency range of 5-20MHz. The transformer geometries that performed well in simulation were then designed and a layout produced to be fabricated in LTCC. Five designs were selected to be fabricated. The transformers were constructed on a four layer stack of 10 mil thick 951 ceramic tape and screen printed silver conductors. Four additional layers without conductors were added for mechanical strength and to alternate the directions of lateral stresses induced during tape manufacturing. The internal conductive layers were printed with DuPont's 6142D silver paste, vias were made with 6141 silver paste, and the top conductive layer was made with 6146 solderable silver paste. In order to have the spiral coils as close as possible they must be printed on consecutive layers in the stack. This means that at minimum at least one of the coils will be buried in the substrate. Vias were needed to bring the connections of any buried coil to one of the outer surfaces without crossing through the region between the primary and secondary coils as this would potentially shield a portion of the coils from coupling properly.

The transformer layouts were designed to meet the several specifications in order to perform properly with the selected modulation system. First the transformer must have an approximately one-to-one voltage gain at the desired operating frequency such that the input to the demodulator stage is within the voltage levels specified. Second the current draw from the primary side must be below the drive strength of the modulator. Thirdly the transformer must provide adequate blocking capabilities for large transient voltage spikes during switching events. Finally the transformer must be reasonably compact so as to be integrated into a full gate driver circuit board.

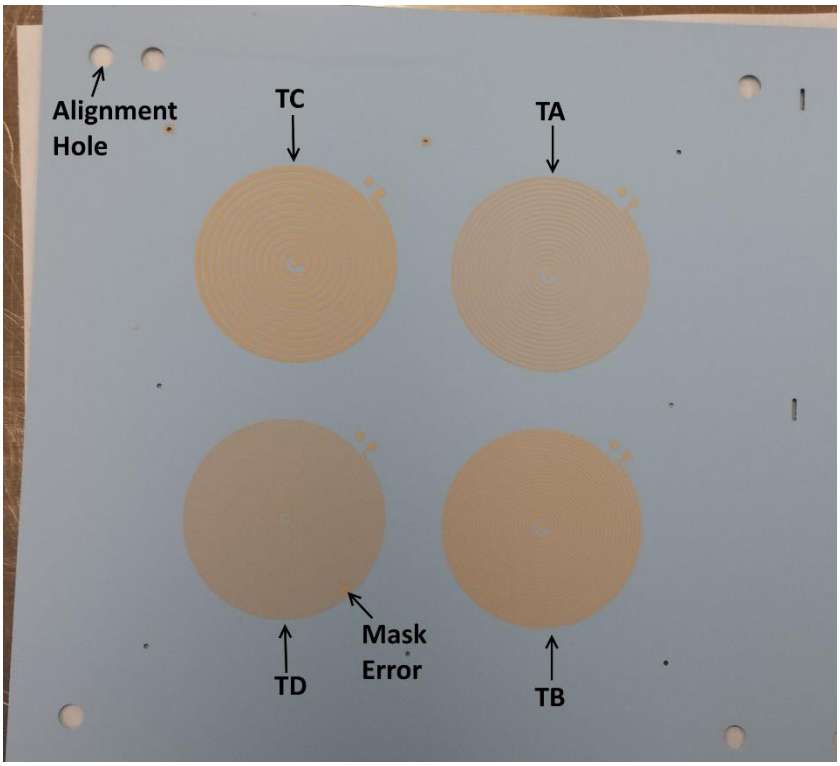

Figure 3. Four Transformer Designs on LTCC during Fabrication

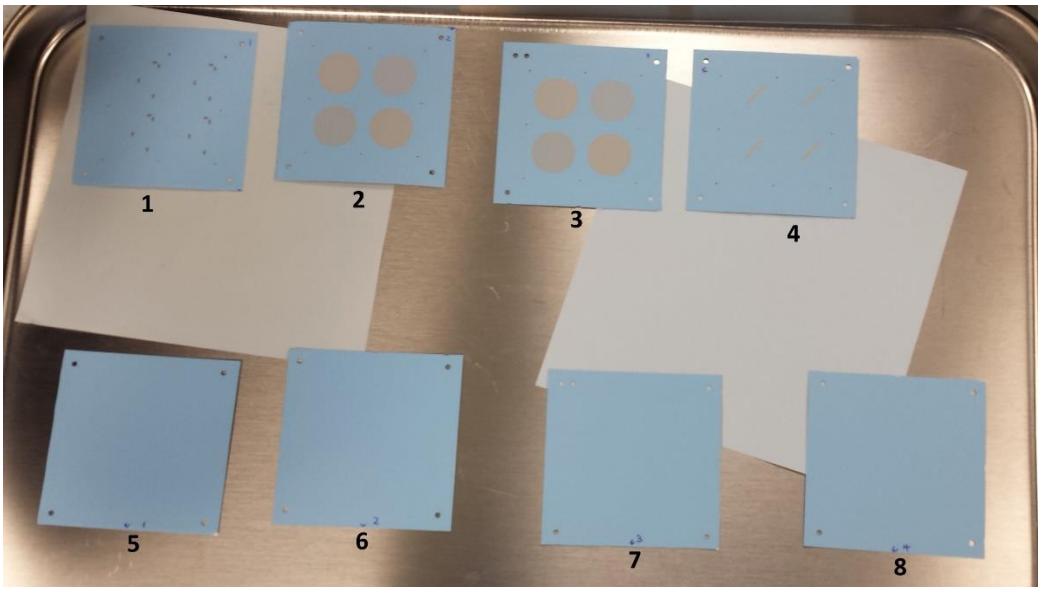

Figure 4. Four LTCC CPTs Showing Layer Order

Table 2. LTCC Layout Parameters*

Parameter	TA	TB	TC	TD	TE
r (m)	0.0095000	0.0095000	0.0095000	0.0095000	0.02000
w (m)	2.5400e-004	2.5400e-004	5.0800e-004	1.2700e-004	2.5400e-004
s (m)	5.0800e-004	3.8100e-004	7.6200e-004	2.5400e-004	5.0800e-004
z (m)	2.1590e-004	2.1590e-004	2.1590e-004	2.1590e-004	2.1590e-004
Np	18	25	12	37	39
Ns	18	25	12	37	39

* Note: Dimensions given in Table 2 are as drawn prior to firing. Horizontal and vertical dimensions will experience shrinkage during firing process. According to DuPont's datasheet for 951 Green Tape™ the percent shrinkage is 12.7% laterally and 15% vertically.

IV. Analysis

A. Simulation

The values obtained from the MATLAB code were automatically written to a SPICE parameter file. This parameter file contains a line for each parameter of the SPICE model and is brought into the simulation with an include statement. To simulate each transformer design, following steps were taken. First the transformer geometry was input into MATLAB. Next the code found in Appendix A was executed and the results written to a parameter file in the same directory as the SPICE model. Then the SPICE simulator was opened and the desire simulations performed with the model parameters corresponding to the CPT layout that was previously calculated. The voltage at the secondary terminal as well as the primary current, the current that must be supplied by the modulator output circuit, are recorded for each transformer in Figure 5 to Figure 9

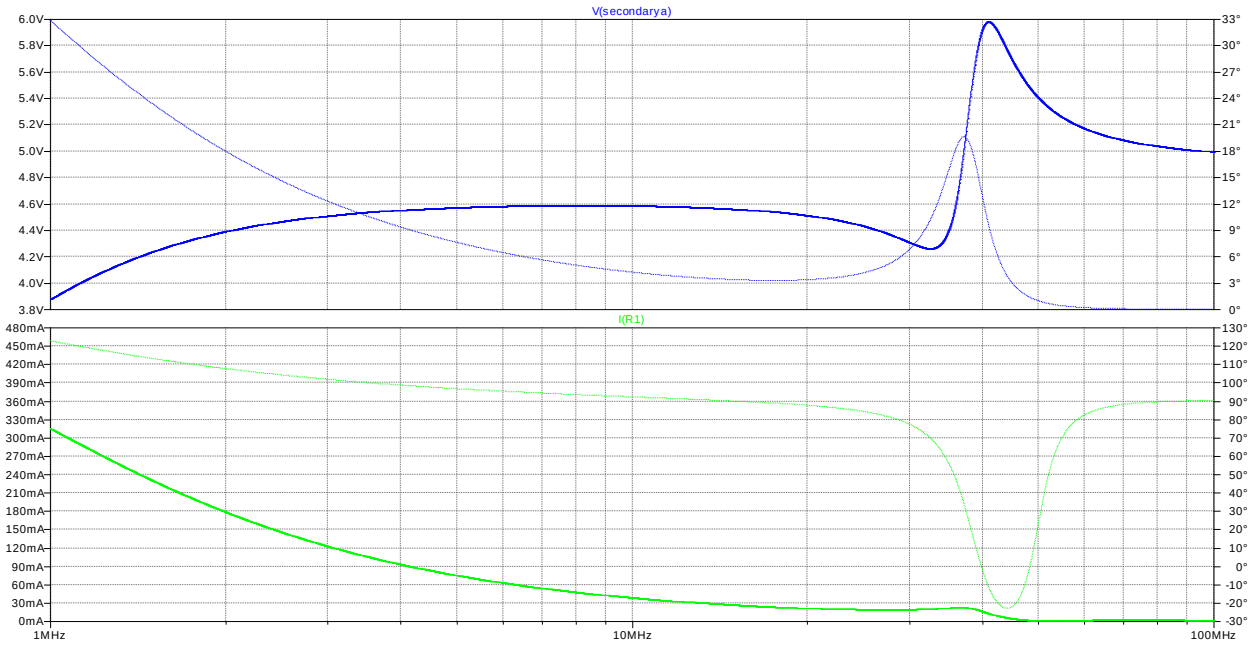

Figure 5. Transformer A Simulation Output Voltage and Primary Current

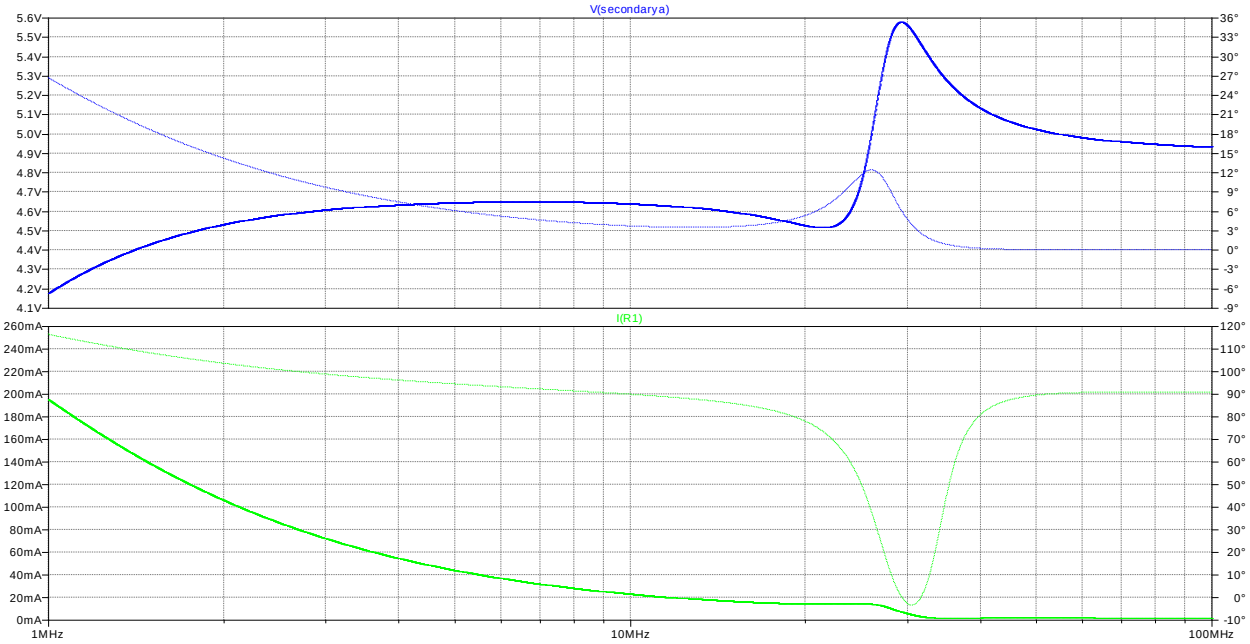

Figure 6. Transformer B Simulation Output Voltage and Primary Current

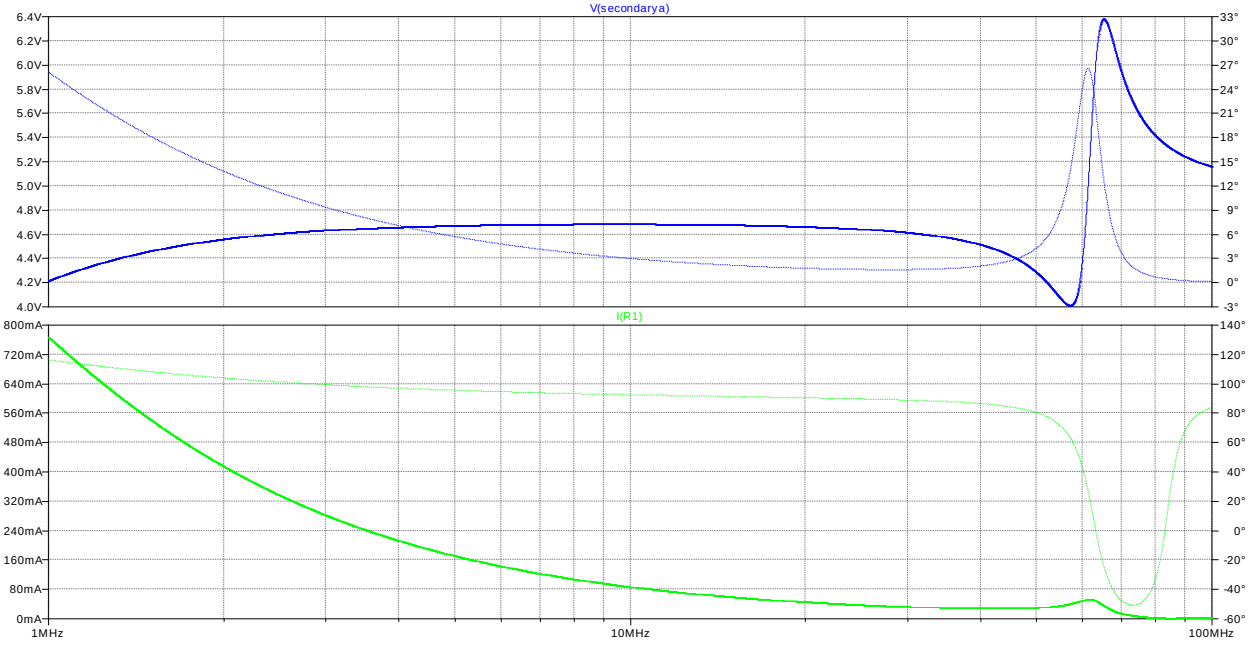

Figure 7. Transformer C Simulation Output Voltage and Primary Current

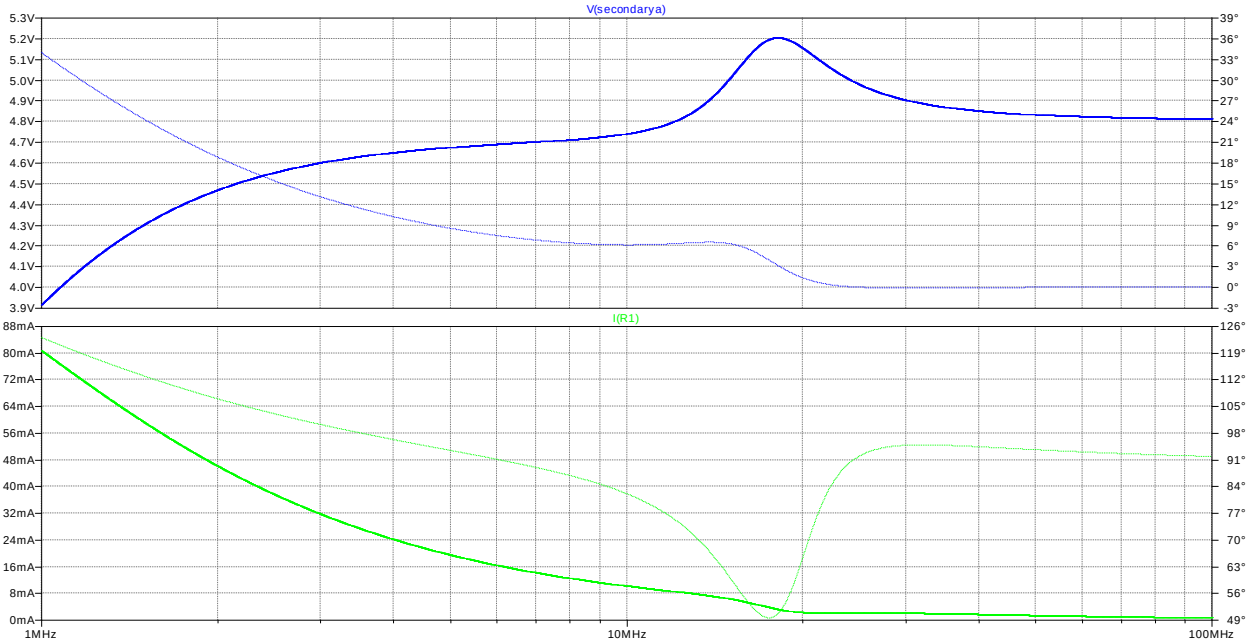

Figure 8. Transformer D Simulation Output Voltage and Primary Current

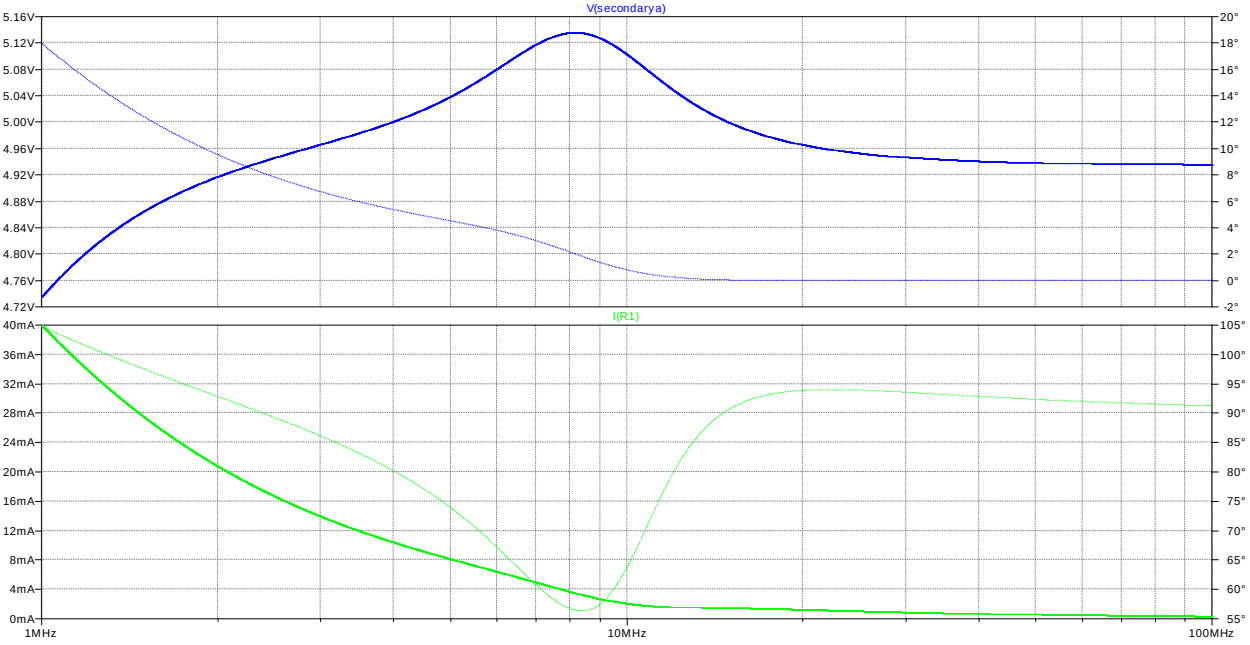

Figure 9. Transformer E Simulation Output Voltage and Primary Current

These results show that each transformer design will theoretically achieve a gain of greater than one within the frequency range of the modulator, 10-50MHz, as well as a current draw below the maximum source current of the modulator output, 8mA.

Table 3. SPICE Model Parameters

Parameter	TA	TB	TC	TD	TE
Rp (Ω)	1.1313E+01	1.1501E+01	2.8712E+00	3.4499E+01	3.8227E+01
Rs (Ω)	1.1313E+01	1.1501E+01	2.8712E+00	3.4499E+01	3.8227E+01
C1 (F)	8.7881E-13	1.2113E-12	2.9861E-13	2.7267E-12	3.0219E-12
C2 (F)	8.7881E-13	1.2113E-12	2.9861E-13	2.7267E-12	3.0219E-12
C12 (F)	6.5758E-11	6.8121E-11	5.6863E-11	6.7851E-11	2.2642E-10
LM (H)	2.9715E-06	3.4013E-06	8.7534E-07	7.6521E-06	1.8531E-05
Llk1 (H)	2.2428E-07	2.5495E-07	5.8301E-08	6.2392E-07	7.6598E-07
Llk2 (H)	2.2428E-07	2.5495E-07	5.8301E-08	6.2392E-07	7.6598E-07

B. Isolated Testing

Initial testing involved performing individual transformer designs in isolation to fully characterize the coil design that was used. These tests consisted of LTCC test cards with previously selected CPT designs and a benchtop test setup designed to test the frequency response of the transformer as well as performance of the device under simulated operating conditions up to 225C. First short lengths of Teflon coated wires were soldered to the pads for each transformer using high melting point solder. Next using a Network Analyzer the input impedance for each transformer was measured up to 30 MHz. The results from the Network Analyzer may be found in Figure 10 to Figure 14. Then the gain of each transformer was measured up to 30 MHz by connecting the primary side of each transformer to the output

Network Analyzer and the secondary side to the input. These results may be found in Figure 23 to Figure 27.

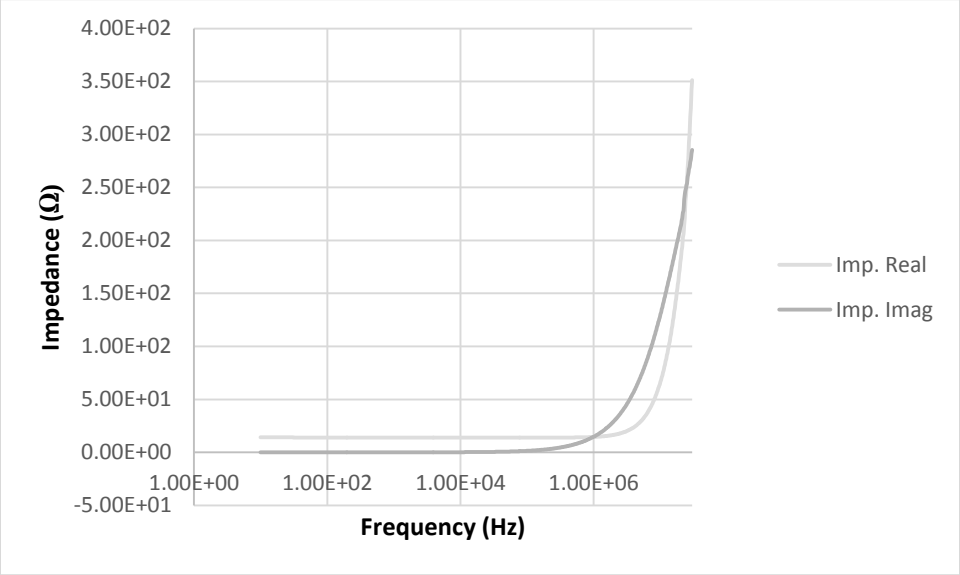

Figure 10. Input Impedance for Transformer A

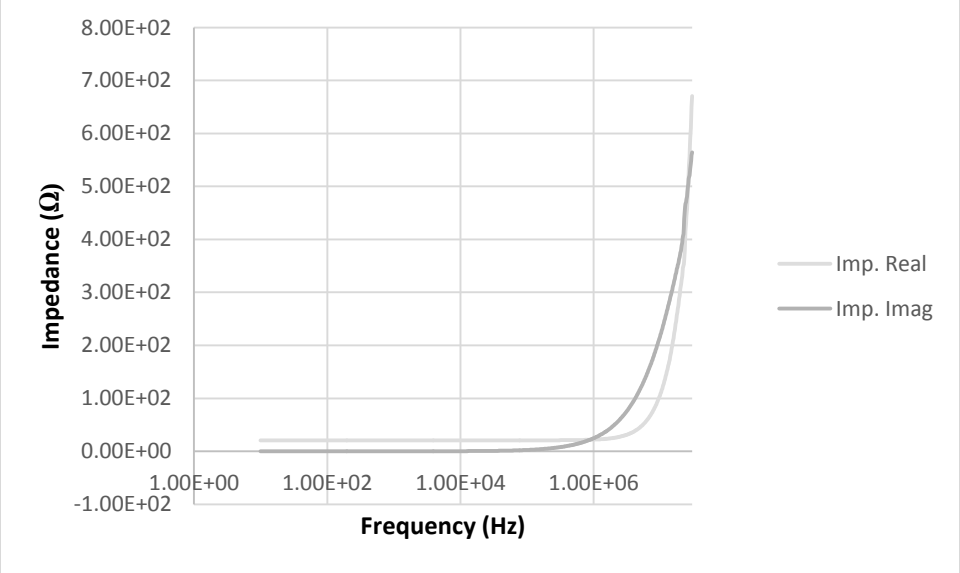

Figure 11. Input Impedance for Transformer B

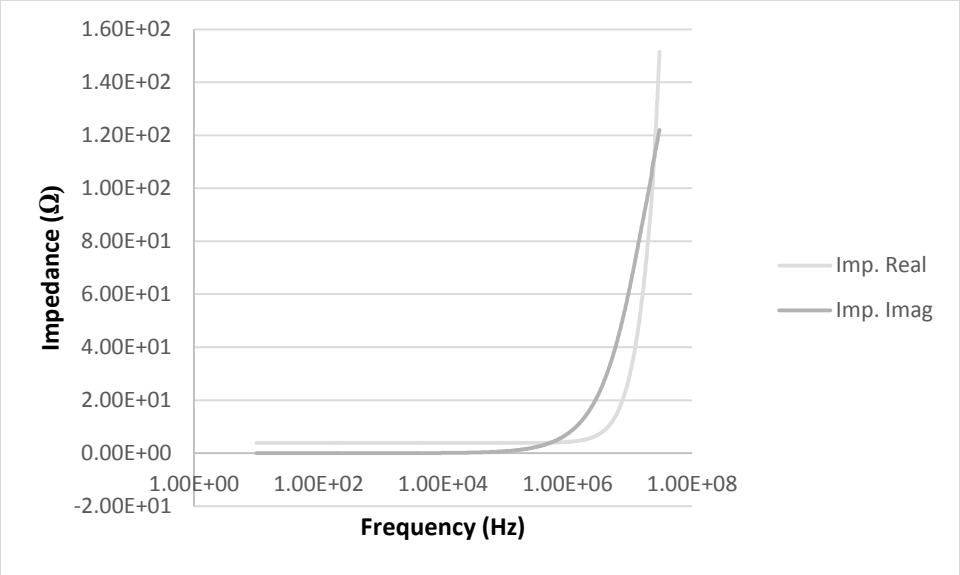

Figure 12. Input Impedance for Transformer C

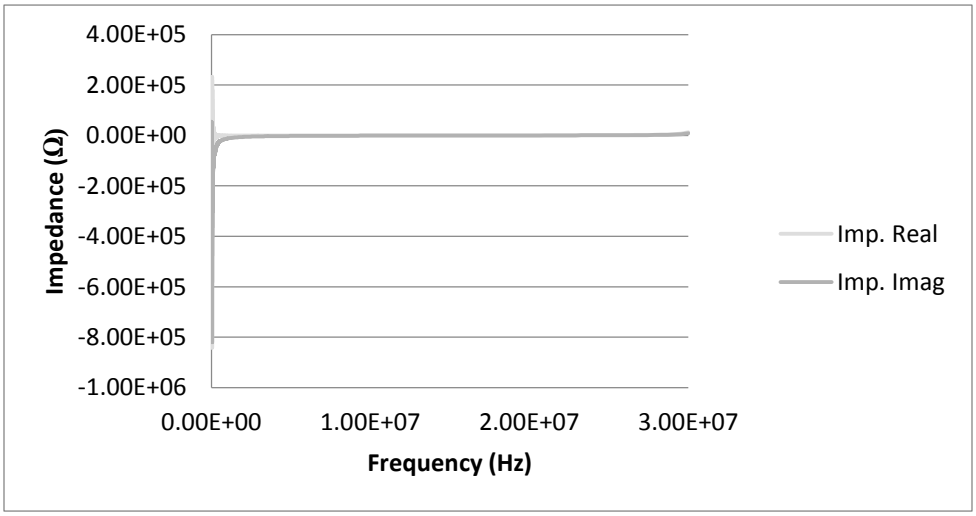

Figure 13. Input Impedance for Transformer D

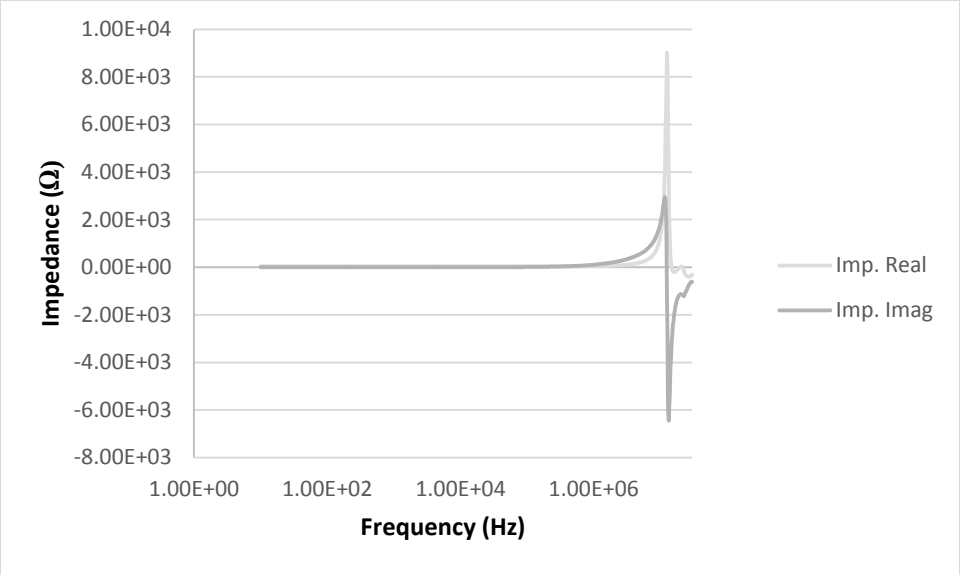

Figure 14. Input Impedance for Transformer E

C. Full System Testing

For full system testing the modulator and demodulator circuits were made of Direct Bond Copper (DBC) cards with screw terminal posts for all the connections. The output of the modulator was connected to the primary side and the secondary to the demodulator. Benchtop power supplies were connected to VCC and VSS of the modulator and demodulator as well as the bias supply of the modulator used to adjust its operating frequency. Oscilloscope probes were connected to the input of the modulator and the output of the demodulator and differential probes were connected to the primary and secondary sides of the transformer. The modulator input was connected to a function generator producing as square wave with a frequency of 20 KHz and a 50% duty cycle. This was repeated with each transformer at 25C, 125C, and 225C. The results from the full system testing may be found in Figure 16 to Figure 20. In these figures Channel 1 shows the input from the function generator and Channel 4 shows the output from the

demodulator. Channel 2 and Channel 3 are the primary and secondary voltage respectively. Unfortunately the demodulator circuit was non-functional likely due to handling or packaging. However the output from the secondary side demonstrates that the transformer performs correctly. The output from the secondary side shown by channel 3 in Figure 16 to Figure 20 as the same frequency as the input to the primary side of the transformer. The amplitude of the signal on channel 3 is within the input range acceptable for 5V CMOS integrated circuits. Any input below the negative voltage rating of the input circuit, such as present on in Figure 17 will be clamped to ground by input protection diodes.

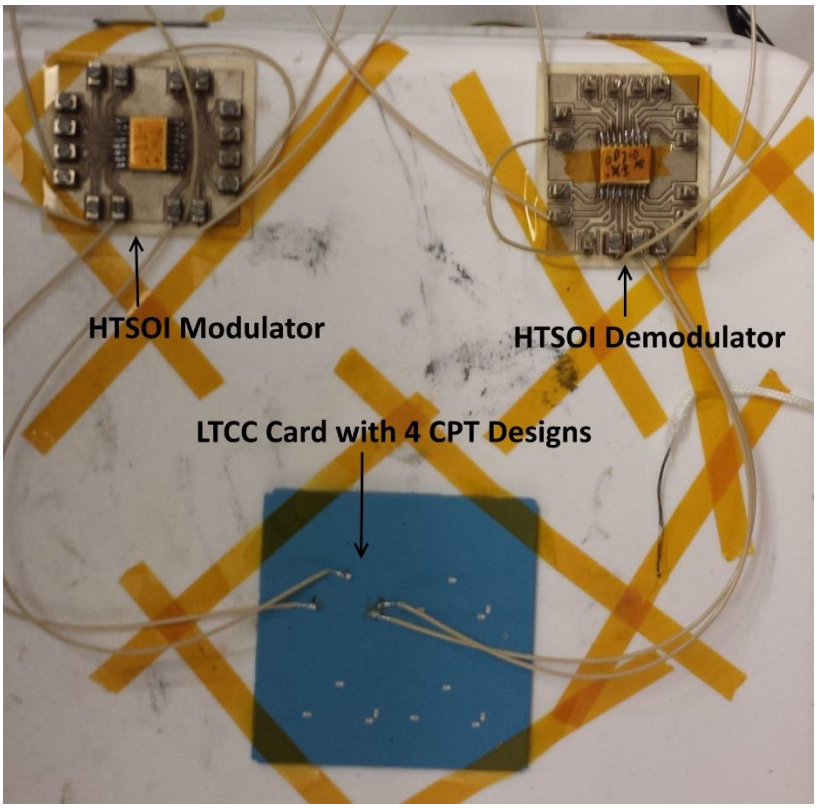

Figure 15. Experimental Setup

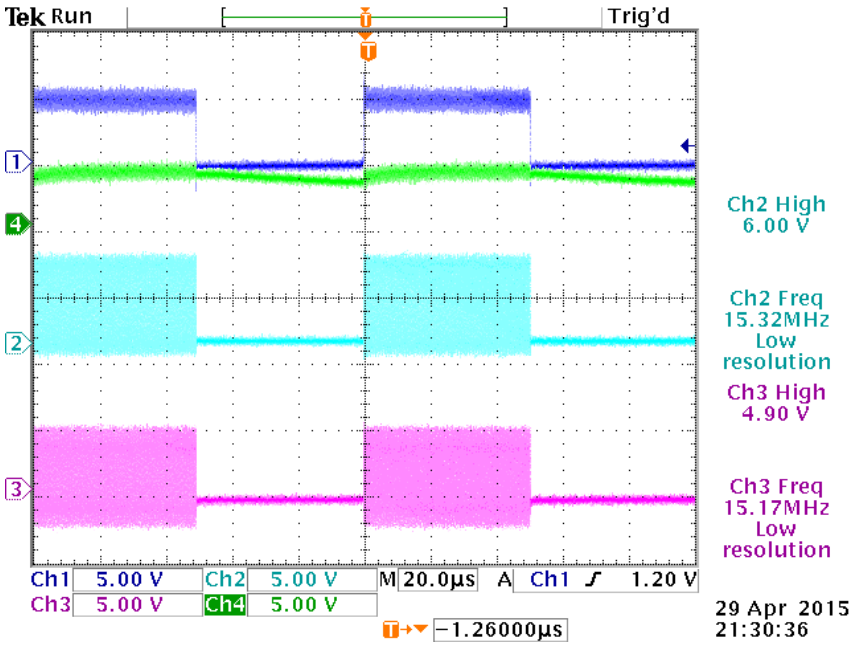

Figure 16. Transformer A Full System 15Mhz

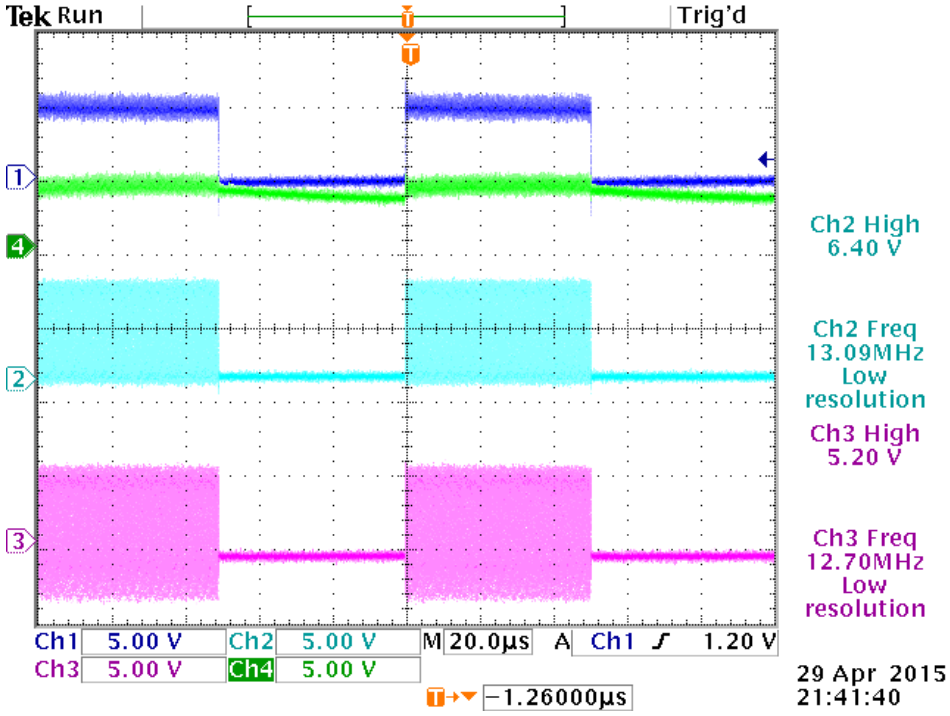

Figure 17. Transformer B Full System 13Mhz

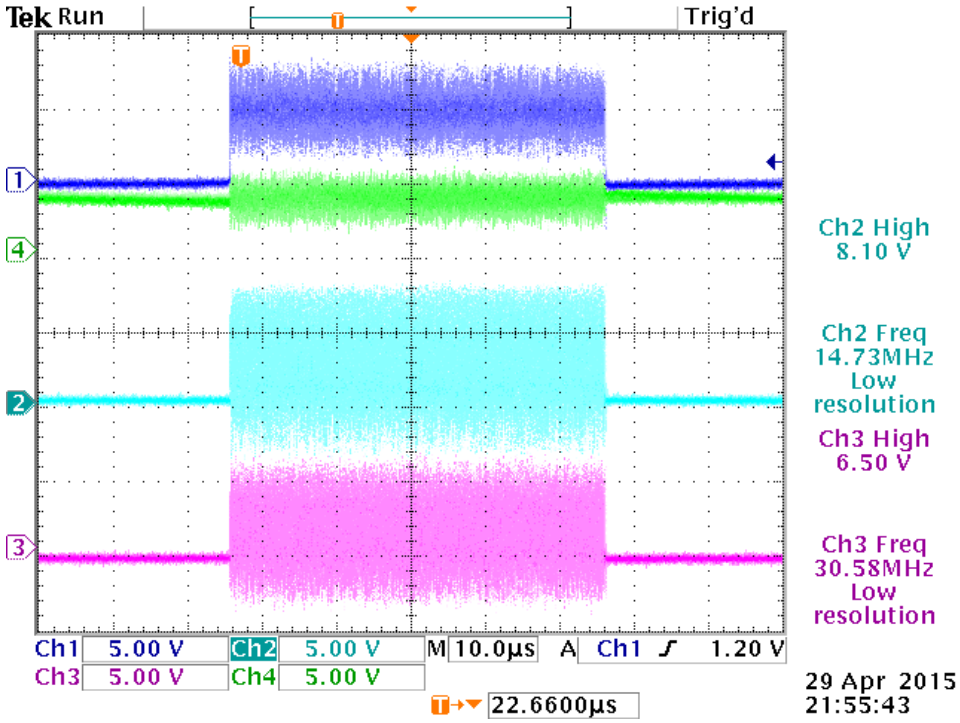

Figure 18. Transformer C Full System 15 MHz

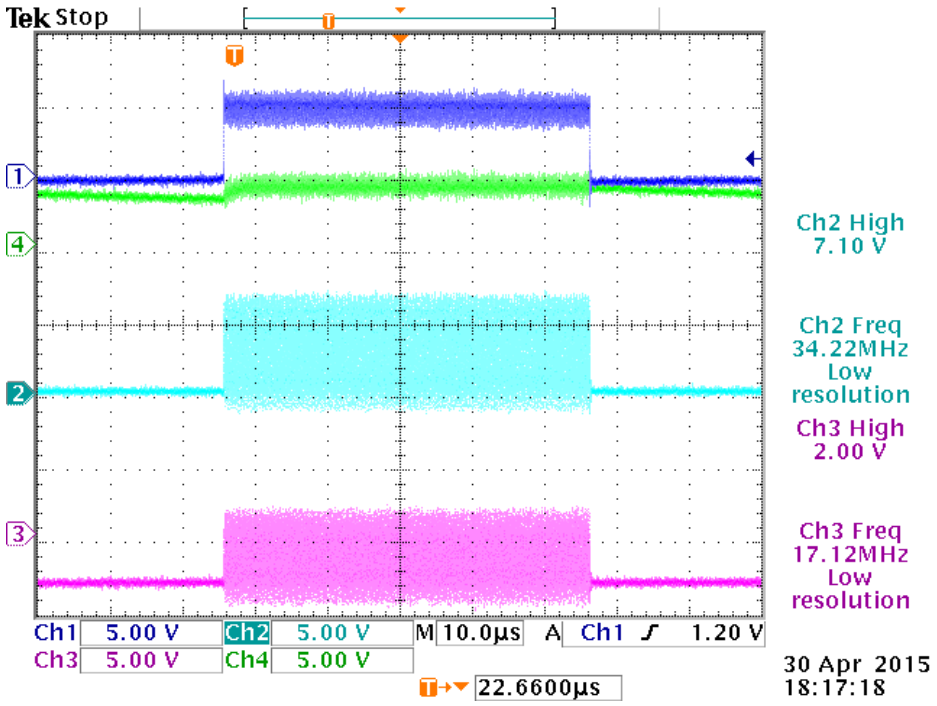

Figure 19. Transformer D Full System 34 MHz

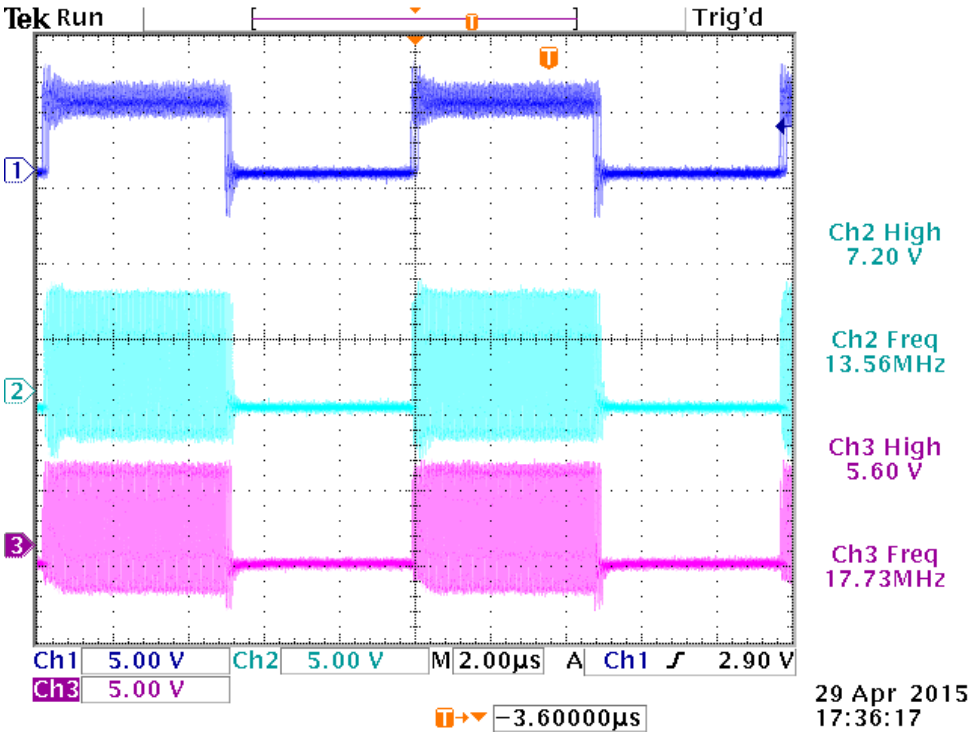

Figure 20. Transformer E Full System 14 MHz

D. Temperature Testing

Due to high 60Hz noise present on the transformer terminals that exceeded the input ratings of the HTSOI circuits used for the modulator and demodulator in depth testing at higher temperature was not possible. This noise came from heater of the hot plate regardless of if the hotplate is on or off. This indicates that a portion of the hotplate's heater was tied directly to the mains voltage. Adding a ground plane between the hotplate surface and the transformer reduced but did not eliminate the noise while adding further complications due to temperature gradients across the system. Therefore only a limited functionality test was performed on transformers A and E at increased operating temperature the results of which may be found in Figure 21 and Figure 22 respectively. These figures demonstrate that the modulation circuit operates properly

at 125 °C and 225 °C and that the transformers produce a voltage gain close to one at these temperatures when using the modulator. Further testing at temperature was performed using a network analyzer to confirm that each transformer produces the expected voltage gain within the desired frequency range at both 125 °C and 225 °C.

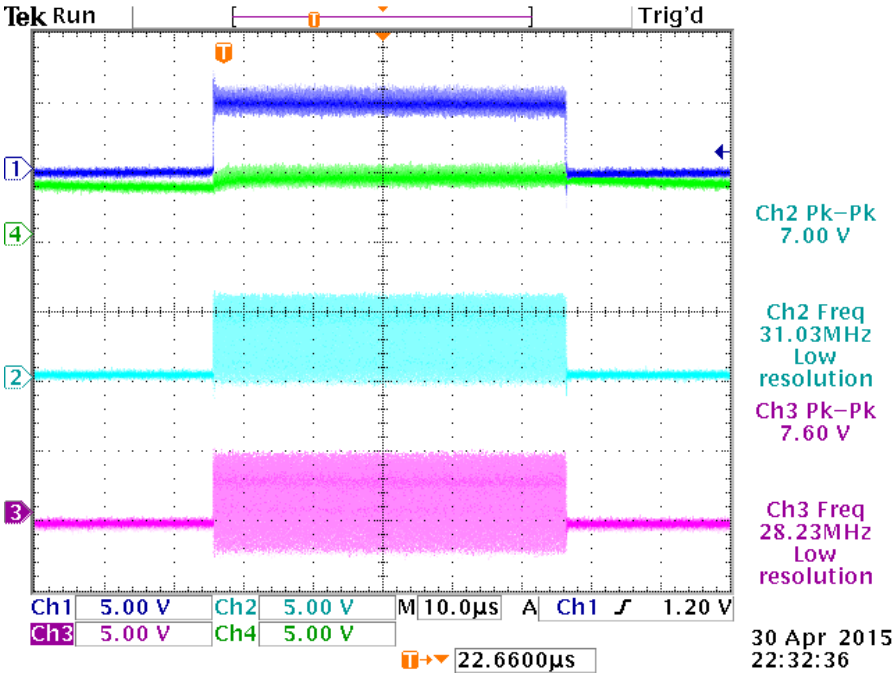

Figure 21. Transformer A at 125C, 30 MHz

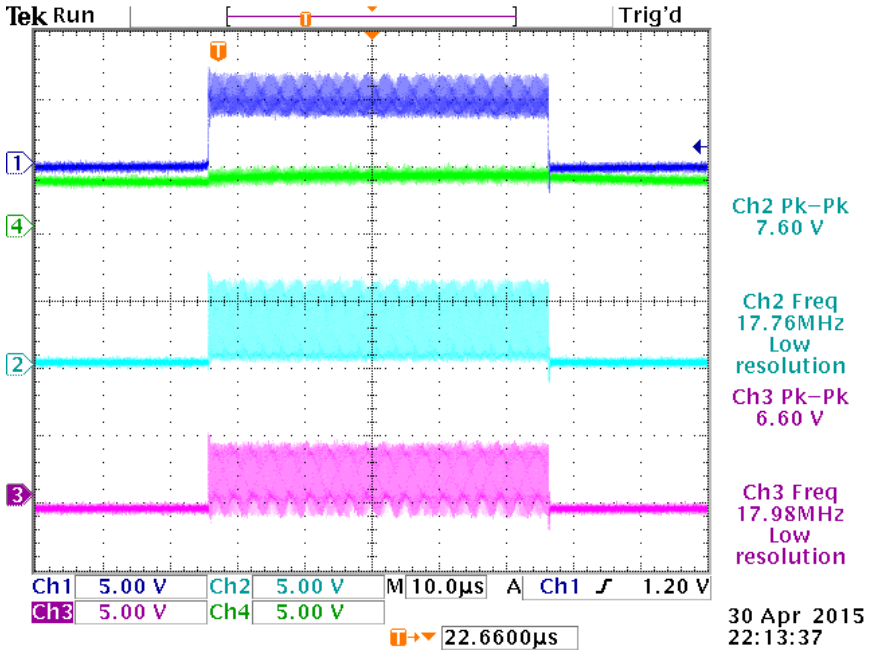

Figure 22. Transformer E at 225C, 18 MHz

The gain of each transformer was measured using a Network Analyzer by first heating the transformer to 125C separately then connecting the analyzer and running the test from 1MHz to 30 MHz. This was repeated at 225 °C as well for each transformer. The gain for each transformer at 25C, 125C, and 225C can be found in Figure 23 to Figure 27.

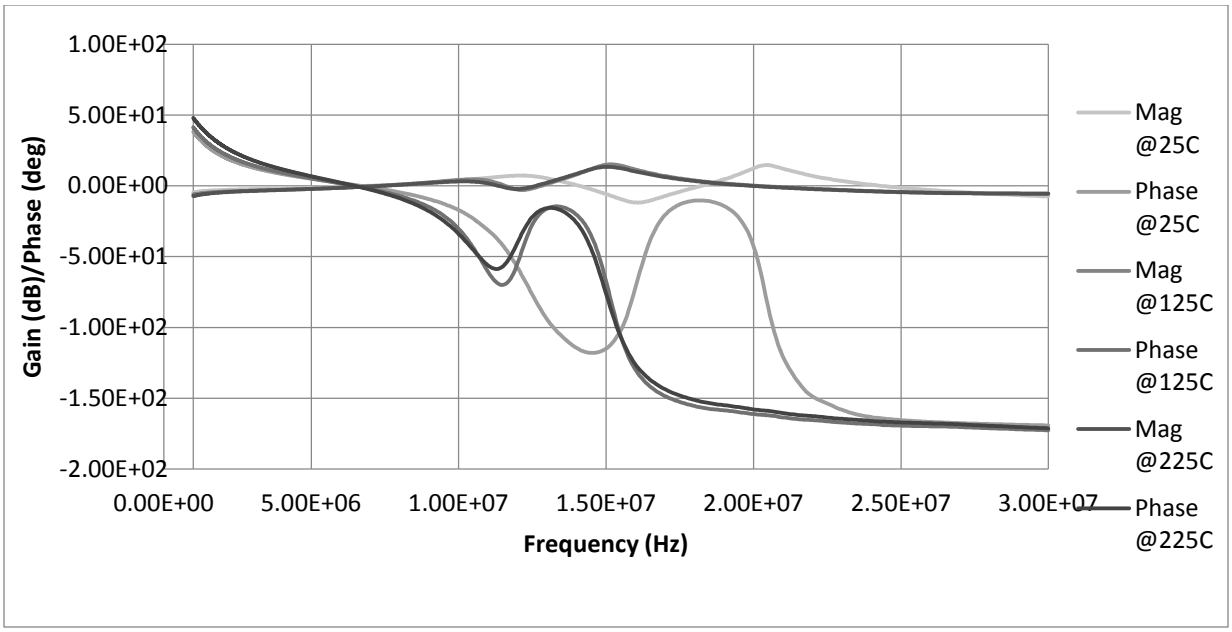

Figure 23. Transformer A Gain vs. Frequency

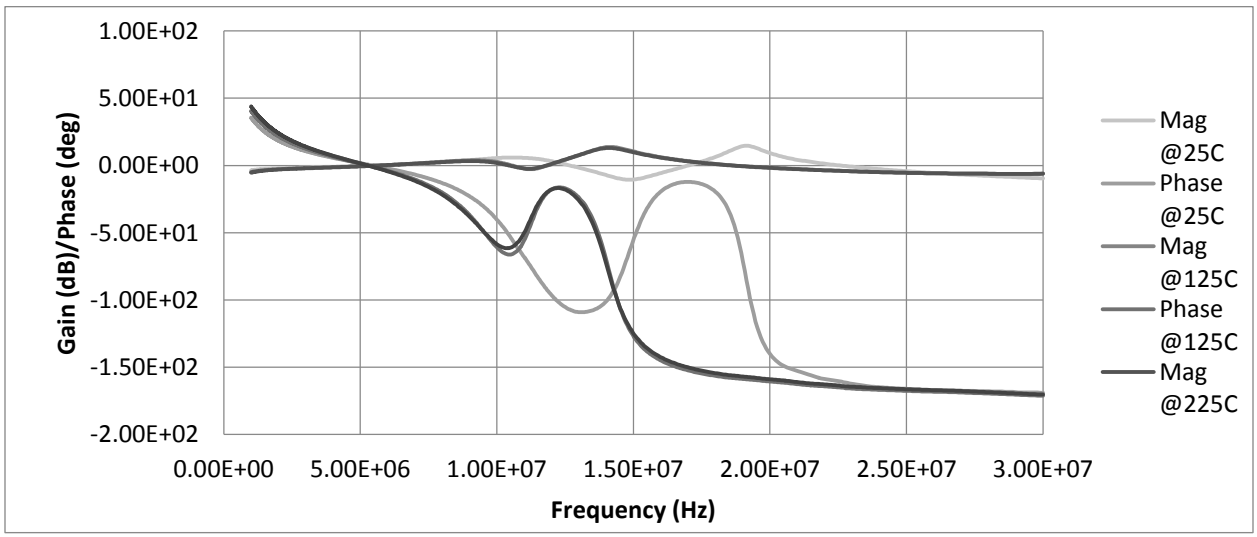

Figure 24. Transformer B Gain vs. Frequency

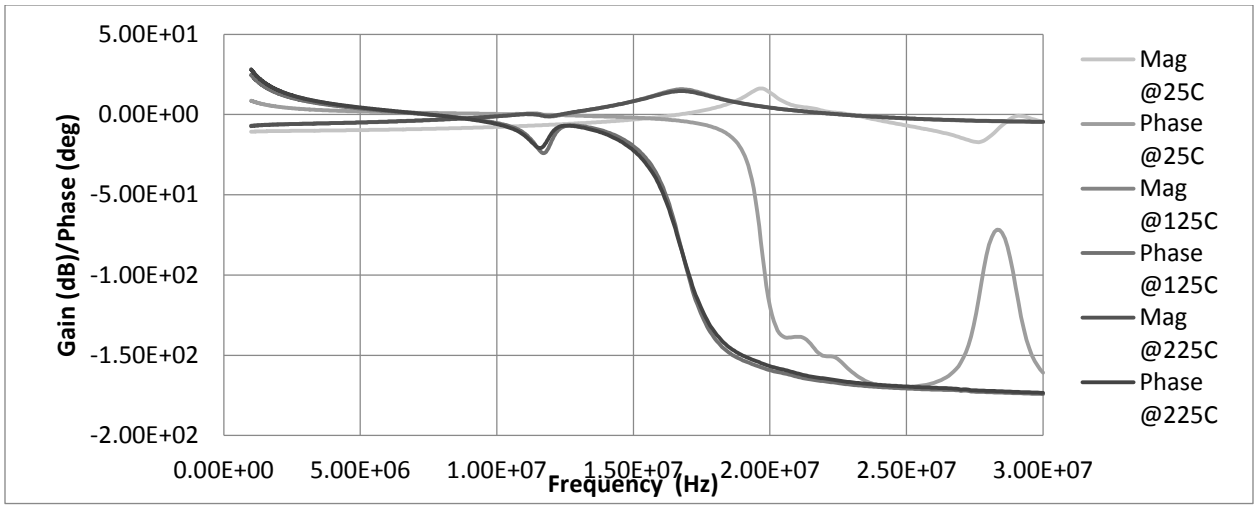

Figure 25. Transformer C Gain vs. Frequency

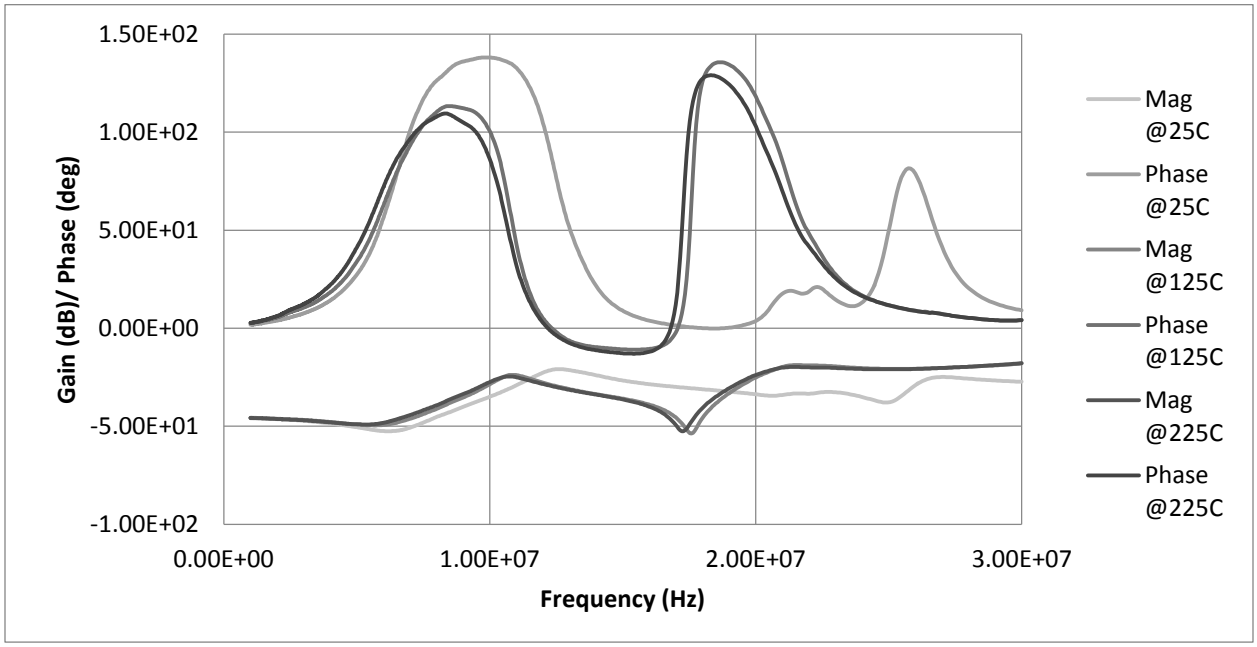

Figure 26. Transformer D Gain vs. Frequency

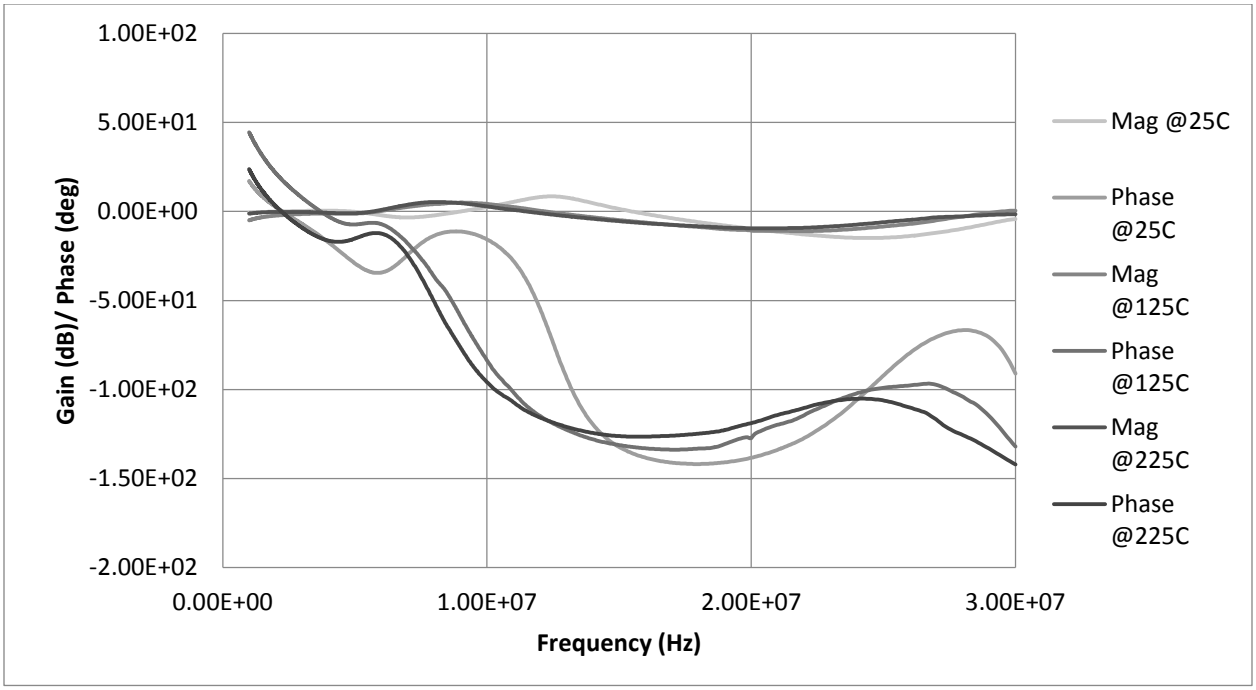

Figure 27. Transformer E Gain vs. Frequency

The results show that transformers A, B, C, and E all achieved a gain of approximately 1 within the target operating frequency range and a peak gain of greater than 1. There is a pronounced shift in the plots at 125C and 225C from the 25C plot. This is due to needing longer probes with different impedance in order to reach the temperature setup safely. The results demonstrated that the transformers will perform at high temperature. The peak gain frequencies compare favorably to the results obtained in section A. Simulation. Transformer D however only achieved a peak gain of -2dB. This in addition to the results for transformer D's impedance confirm the suspected fabrication error that was seen in the mask for this transformer, see Figure 3. This is likely due to the design from this transformer being at the limit of the resolution of the LTCC process used for fabrication.

V. Conclusion

In this thesis, a coreless planar transformer was designed on low-temperature co-fired ceramic that will produce a gain of at least one at frequencies above 10 MHz. It was shown that the model developed in MATLAB successfully approximates the CPT at these frequencies. It was shown that from the physical geometry of a spiral shaped CPT the electrical parameters may be obtained through several simple calculations for each parameter.

It was shown that several configurations of CPT were successfully able to operate at frequencies between 10MHz and 30 MHz. The transformers were also demonstrated to operate at high temperatures with little effect on their performance. The use of CPTs in high temperature applications such as gate drivers benefit from the reduced cost and manufacturing steps as well as increased performance when compared to traditional surface mount wire-wound magnetics. Further testing at higher temperatures and with a more complete modulation system would be needed before this design could be integrated into new circuit design.

The success of transformers A-C, and E to produce a gain of close to one within the target frequencies as well as at elevated temperature has numerous applications in both signal and power isolation systems. The ability to integrate the transformer into the substrate can provide cost savings and increased efficiencies.

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Appendix A: MATLAB Code

```
%Matthew Feurtado Honor Thesis
%CPT calculations for 951 LTCC
function calculations()
  h = 9e-6
  r = 0.0174
  w = 2.2098e-4
  s = 4.4196e-4
  z = 2.159e-4 %fired thickess(85% 0f 10mil)
  Np = 39
  Ns = 39
  f = 10e6
  T=300
  [Cp, Cs, Rac, Mps, Llk, Zin] = calc(h, w, s, Np, Ns, r, z, f, T);
  writeParams('../params.txt',Cp, Cs, Rac, Mps, Llk);

endfunction

function [Cp, Cs, Rac, Mps, Llk, Zin] = calc (h, w, s, Np, Ns, r, z, f, T)
  [Lp, Mps, Llk] = inductance (h, w, s, Np, Ns, r, z)
  [Cp, Cs]  = capacitance (h, w, s, Np, r, z)
  Rac = resistance (h, w, s, Np, r, f, T)
  [Mps, Llk] = InductanceS (h, w, s, Np, Ns, r, z)
  [Zin] = impedance(Rac, Rac, 10e6, Llk, Llk, Mps, Cs, Cs, Cp, f, Np)
endfunction

function writeParams(file,Cp, Cs, Rac, Mps, Llk)
  fileID = fopen(file, 'w');
  fprintf(fileID, '.param %s = %.4e\n', 'Rp', Rac);
  fprintf(fileID, '.param %s = %.4e\n', 'Rs', Rac);
  fprintf(fileID, '.param %s = %.4e\n', 'C1', Cs);
  fprintf(fileID, '.param %s = %.4e\n', 'C2', Cs);
  fprintf(fileID, '.param %s = %.4e\n', 'C12', Cp);
  fprintf(fileID, '.param %s = %.4e\n', 'LM', Mps);
  fprintf(fileID, '.param %s = %.4e\n', 'Llk1', Llk);
  fprintf(fileID, '.param %s = %.4e\n', 'Llk2', Llk);
  fclose(fileID);
endfunction

function [Cp, Cs]  = capacitance (h, w, s, N, r, d)
    lngth = 2*pi.*N.*(r-N.*s)+s.*pi.*N.^2;
    e0=8.8541878e-12;
    er=7.8;     %Dielectric constant for DuPont green tape is 7.8
    Cp = e0.*er.*(w+0.5.*d).*lngth./d;
    Cs=0;
    for i=1:(N-1)
        Cs+=2*pi*e0*er.*h./log((r-s.*(N-i-1))/(r-s.*(N-i)));
    endfor
endfunction

function Rac = resistance (h, w, s, N, r, f, T)
    p=2.44e-8.*(1+0.0034.*(T-293));
    u0=4*pi*10^-7;
```

```
    lngth = 2*pi.*N.*(r-N.*s)+s.*pi.*N.^2;
    squares = lngth./w;
    Rdc = 3.3e-3.*squares;  %Based on 6142D cofireable conductor
    s = 1./sqrt(pi*f*u0./p);
    Rac = Rdc.*h./(s.*(1-exp(-h./s)))
endfunction


function [Mps, Llk] = InductanceS (h, w, s, Np, Ns, r, z)
    % h = vertical height of conductor
    % w = width of conducting path
    % s = distance between two equivalent points in the conducting path
    % Np, Ns = primary and secondary number of turns. Must be integers for
this program.
    % r = outer radius of the transformer
    % z = distance between transformer coils
    Lp=0;
    rx=r;
    for i=1:Np
        ax=r;
        for j=1:Np
            if i==j
                z2=0.2235.*(w+h);    %GMD of a loop from itself.
            else
                z2=0;
            endif

            Lp+=Msimple(rx,rx-w,ax,ax-w,z2);
            #inc+=1
            ax-=s;
        endfor
        rx-=s;
    endfor

    Mps=0;
    rx=r;
    for i=1:Np
        ax=r;
        for j=1:Ns
            Mps+=Msimple(rx, rx-w, ax, ax-w, z);
            ax-=s;
        endfor
        rx-=s;
    endfors
    Llk=Lp-Mps;

endfunction

function L = Msimple(r1, r2, a1, a2, z) %calculates inductance between two
filaments
    a=sqrt(a1.*a2);  %geometric mean radius
    r=sqrt(r1.*r2);
    f=sqrt((4.*a.*r)/(z.^2+(a+r).^2));
    [K,E]=ellipke(f^2);
    u0=4*pi*10^-7;
    L = u0.*sqrt(a.*r).*(2/f).*((1-(f.^2)./2).*K-E);
Endfunction
```

```
function [Lp, Mps, Llk] = inductance (h, w, s, Np, Ns, r, z)
    % h = thickness (height) of the conductor
    % w = width of the conductor path
    % s = distance between conductor paths
    % Np = number of turns on the primary coil
    % Ns = number of turns on the secondary coil
    % r = outer radius of transformer
    % z = distance between the coils (dielectric thickness)
    %% Calculating Lp
    a1 = r;
    Lp=0;
    for i=1:Np
        r1=r;
        for j=1:Np
            if i==j
                zeff=0.2235.*(w+h);
            else
                zeff=0;
            endif
            Lp += Mij(h, h, r1, r1-w, a1, a1-w, zeff);
            r1 -= s;
        endfor
        a1 -= s;
    endfor
    %% calculating mutual inductance
    Mps = 0;
    a1=r;
    for i=1:Np
        r1=r;
        for j=1:Ns
            d = sqrt(z.^2+((i-j).*s).^2);
            Mps += Mij(h,h,r1,r1+w,a1,a1+w,sqrt(d.^2+((i-j).*s).^2));
            r1 -= s;
        endfor
        a1 -= s;
    endfor
    Llk = Lp-Mps;
endfunction

%%Calculates the induction between two circular strips i and j
function L = Mij (h1,h2,r1,r2,a1,a2,z)
    f=@(k)Sfunc(k,r2, r1).*Sfunc(k,a2,a1).*Qfunc(z,k,h1,h2).*exp(-k.*abs(z));
    placeholder=quadcc(f,0,10000);
    u0=4*pi*1e-7;
    L=((u0*pi)/(h1*log(r2/r1)*h2*log(a2/a1)))*placeholder;
    return
endfunction

%%Q function for Mij
function f = Qfunc (z,k,x1,x2)
    if(z==0)
        h=x1;
        f=(2./k).*(h-((exp((-k).*h)-1)./k));
    else
        f=(2./(k.^2)).*(cosh(k.*(x1+x2)./2)-cosh(k.*(x1-x2)/2));
    end
```

```
    return
endfunction

%%S function for Mij
function z = Sfunc (k, x1, x2)
    z=(besselj(0,k*x1)- besselj(0,k*x2))./k;
    return
endfunction

%%Impedance calculations
function [Zin] = impedance(R1, R2, RL, Llk1, Llk2, LM, C1, C2, C12, f, n )
  s = 2*pi*f*i; %s = jW
  R2p = n^2 * R2;
  Llk2p = n^2 * Llk2;
  C1p = C1 + ((n-1)/n)*C12;
  C2p = (1/n^2)*C2 + ((1-n)/n)*C12;
  C12p = (1/n)*C12;
  X1 = R1 + s*Llk1;
  X2 = R2p + s*Llk2p;
  Y1 = X2*((1/X1) + (1/(s*LM))) + 1;
  Y2 = (1/X2) + s*C12p + s*C2p + (1/n^2*RL);
  Y = -(1/X2) + Y1*Y2;
  A = ((s*C12p) + (X2/X1)*Y2) / Y;
  B = ((1/X1) + s*C12p*Y1) / (n*Y);
  Zin = 1 / ((s*C12p*(1-n*B)) + ((1-A)/X1) + s*C1p); %input impedance
endfunction
```