Analytical Switching Loss Model for SuperJunction MOSFET with Capacitive Non-Linearities and Displacement Currents for dc-dc Power Converters

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Abstract— A new analytical model is presented in this work to predict power losses and waveforms of high-voltage silicon SuperJunction (SJ) MOSFET during hard-switching operation. This model depends on datasheet parameters of the semiconductors, as well as, the parasitics obtained from the printed circuit board characterization. It is important to note that it also includes original features accounting for strong capacitive non-linearities and displacement currents. Moreover, these features demand unusual extraction of electrical characteristics from regular datasheets. A detailed analysis on how to obtain this electrical characteristics is included in this work.

Finally, the high accuracy of the model is validated with experimental measurements in a double-pulse buck converter setup by using commercial SJ MOSFET, as well as, advanced device prototypes under development.

I. Introduction

High-voltage Super-Junction (SJ) MOSFET in the range of 600 V have been in the market for around 20 years. As frequencies of operation increase to miniaturize passive components of the system, the prediction of switching losses in power converters is becoming more complex and necessary. A deep understanding of the transients is crucial to achieve proper models with realistic reproduction of the measured waveforms. Hence, the aim of this work to provide an accurate and physically meaningful analytical model to estimate switching losses in SJ MOSFET.

In prior literature a large number of piecewise analytical models address the dynamic behavior of the power switches [1]-[5]. All these models have in common the segmentation of a single operation cycle in different time intervals. In this sense, the turn-on and turn-off are constituted by multiple intervals. Each one of these intervals has an associated equivalent circuit in reference to the switch action within an inductive switching topology like the one plotted in Fig. 1a. Some of these models [3]-[5] are mainly focused on the low voltage range (<40V), thus being, specialized in emulating features related to high-speed switching rather than replicating the details related to the architecture of the device. Other works [1],[2] provide dedicated models for high voltage MOSFET (>500V). However, these models are actually designed for Planar technologies (see Fig. 1b) meaning some characteristics of SJ MOSFET (see Fig. 1c) are not taken into consideration.

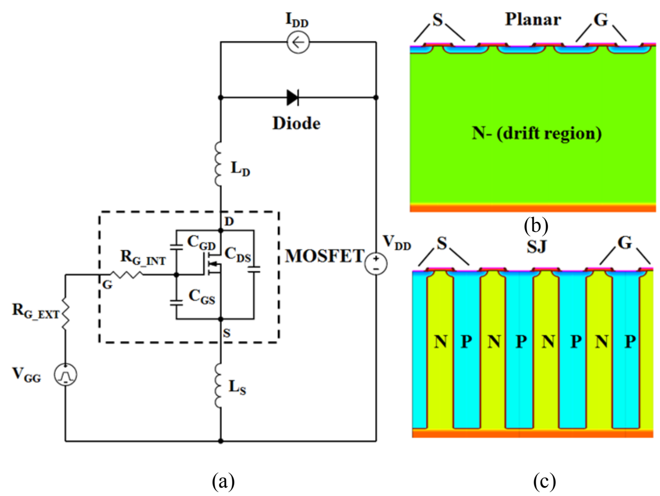

Fig. 1. (a) Circuit scheme to derive the analytical model and to perform Mixed-Mode simulations. (b) Cross section of Planar MOSFET. (c) Cross section of SuperJunction MOSFET built by using TCAD tools. In the performed simulations only a half of the basic cells in (b) or (c) are combined with the circuit in (a).

Among the peculiar features of the SJ MOSFET, the non-linear parasitic capacitances appear as a major hindrance in analytical models. As a matter of fact, C_{DS} and C_{GD} show a reduction of several orders of magnitude when sweeping V_{DS} from zero to more than a hundred volts (see Fig. 2b). Many works model this effect by an effective constant capacitance

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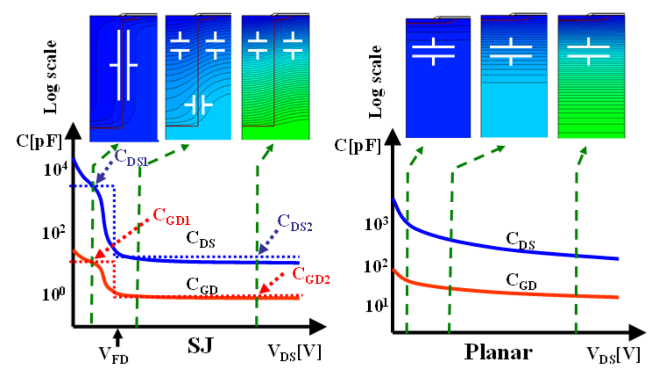
(C_{eff}) extracted by integrating the capacitance along the voltage range of interest [6]. This approach can be really inefficient in a piecewise model like the one presented in this work due to the consideration of several values of capacitance in order to obtain the analytical model. Other models propose a capacitive decay which is linear with V_{DS} [7] or proportional to $(1+V_{DS}/\Phi)^{-1/2}$, where Φ is an adjustment parameter [3],[4]. These two approaches increase the accuracy of the circuit analysis with respect to C_{eff} in the analysis of Planar MOSFET, however their precision could be insufficient for SJ MOSFET. Finally, recent work suggests the use of multiple constant capacitances for different intervals of time [1]. Nevertheless, the extraction of the different capacitances does not follow an established methodology neither a physical meaning is attributed.

Inspired by the model in [1] a new analytical model that defines two separated values of capacitance ($C_{DS1,2}$ and $C_{GD1,2}$), has been developed schematically defined by dotted lines in Fig. 2a. It should be noted that the model presented in this paper is a black-box and does not take into account the architecture of the MOSFET but the behaviour of its capacitances. The relation between C and V_{DS} has been studied in previous works [12]. The transition from one capacitive value to the other is determined by the relative value of V_{DS} with respect to a V_{FD}. The latter has the physical meaning of being the voltage at which the MOSFET drift region is fully-depleted. Aside from the non-linear capacitances, extensively described in Section II, the new model also includes a correction to the displacement currents inside the MOSFET. Despite a few papers mentioning the impact of the displacement current on the power dissipation [8]-[10], this effect has never been included before in an analytical model. The details for the current displacement modeling will be found in Section III. Further discussion on minor elements of the model and the deployment of the complete formulation are the contents of Section IV. Section V presents the experimental validation and discussion of the model and, eventually, Section VI is devoted to draw conclusions and to define future lines of work.

II. Non-Linear Capacitances

The dynamic effects caused by the non-linear capacitances need to be taken into account in order to have an accurate analytical model. In order to tackle these effects two different values of C_{DS} and C_{GD} are defined for voltages above and below a newly defined V_{FD} voltage. As shown in Fig. 2a, a step function sets C_{DS1} and C_{GD1} when $V_{DS} < V_{FD}$ whereas C_{DS2} and C_{GD2} are activated when $V_{DS} > V_{FD}$. The inset pictures in Fig. 2 display the equipotential line distribution in the cross section of a half-pitch cell in Planar and SJ MOSFET. Both structures are built using TCAD tools [11]. From them, it can be inferred that C_{DS1} represents the horizontal capacitance when the vertical PN pillar starts depleting charge to the lateral direction. The accumulation of potential lines in a relatively thin (<10µm per half pitch) and large capacitive area (>40µm per half pitch) result in a very high capacitance. Differently, C_{DS2} incarnate the vertical capacitance after the charge between pillars is completely depleted. In this case the potential lines are stacked vertically in a relatively thick (>40µm per half pitch) and small capacitive area (<10µm per half pitch), thus giving a very small capacitance. Since the MOS gates lay above the N pillars, the full depletion of these pillars enables the potential lines to be relieved from the gate oxide towards the silicon underneath. Subsequently, the transition from C_{GD1} to C_{GD2} will be correlated to the transition from C_{DS1} to C_{DS2}.

From a waveform perspective, the full depletion of the drift region in SJ MOSFET is translated into a steep variation of the dV_{DS}/dt when V_{DS} is equal to V_{FD}. As it will be further described in Section IV, V_{DS} reaches V_{FD} at the beginning of the Miller Plateau during the turn-on and, oppositely, at the end of the Miller Plateau during the turn-off. It is important to note that, in prior literature [1], the inflection point during the V_{DS} raise or fall was never related to V_{FD} but confused with the voltage drop during conduction. Furthermore, this phenomenology, genuine to SJ MOSFET, does not appear in Planar MOSFET. As shown in Fig. 2b, the depletion from the PN junction at the silicon surface is always extending vertically towards the bottom of the drift region. This implies that the capacitive area for C_{DS} and C_{GD} is always the same one and it only increases with the depth when a certain voltage is applied. It is this effect, the one that causes V_{DS} to rise and drop progressively during transients when working with Planar MOSFET.



(a) (b)

Fig. 2. Schematic dependence of C_{DS} and C_{GD} with V_{DS} in (a) SJ MOSFET and (b) Planar. Equipotential lines and equivalent capacitances are plotted in the MOSFET drift region for three V_{DS} values. Dotted lines in (a) indicate $C_{DS1,2}$ and $C_{GS1,2}$,as well as, the step function that is used to approximate non-linear capacitances in the new theoretical model.

The C_{DS} and C_{GD} transition from high to low values has been discussed above for an ideal SJ MOSFET structure. However this transition could be more or less abrupt depending on the charge balance between N and P pillars, the different cell pitch at the termination and many other technological factors. Consequently, sometimes it becomes difficult to define an effective V_{FD} that separates the two levels of capacitance. In this manuscript, we propose a methodology to extract V_{FD} based on the V_{DS} value at which Q_{RSS} reaches 90% of Q_{RRS} at V_{DD} (maximum reverse voltage). In a similar fashion as in other datasheet standards (e.g.; definition of reverse recovery charge or Q_{RR}), a percentage below 100% avoids issues related to large saturation tails for Q_{RSS}. In order to validate this method, four different SJ MOSFET have had V_{FD} calculated from datasheets and also extracted from V_{DS} waveforms, see Figs. 3 and 4. It is important to note, that samples #1, #2 and #3 are commercially available, whereas sample #4 is a prototype produced by ON Semiconductor. A comparison between the V_{FD} calculated from the datasheet capacitance graphs and the V_{FD} estimated from transient V_{DS} waveforms (inflection point) is shown in Table I proving the validity of this method. It is worth remarking that V_{FD} tends to lower values in ultimate SJ MOSFET generations. This fact, related to the smaller cell pitch, has interesting advantages to reduce the switching MOSFET power losses (P_{SW}), as it will be discussed in Section V.

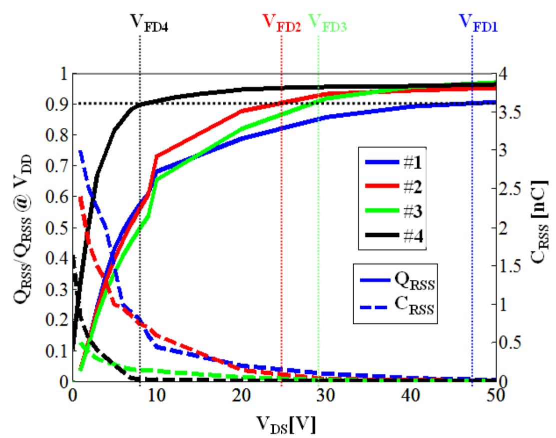


Fig. 3. Q_{RSS} and C_{RSS} vs. V_{DS} for four different SJ MOSFETs. Q_{RSS} is normalized to Q_{RSS}@V_{DD}.for illustrative purposes. Dotted lines indicate V_{FD} when Q_{RRS} reaches 90% of Q_{RSS}@V_{DD}.

TABLE I. TESTED SJ MOSFETS WITH THEIR RON AND V_{FD}

Sample	Device	R_{ON} (mΩ)	V_{FD} (V)	
			Measured	*Analytical*
#1	IPA60R190C6	170	46	47
#2	STF23NM60ND	150	23	24
#3	FCPF22N60NT	140	31	28
#4	ON Semi prototype	145	8	8

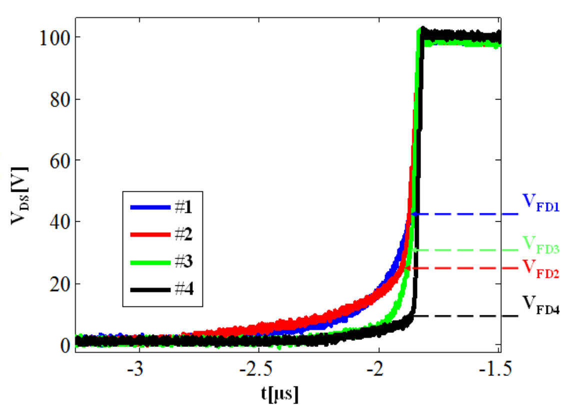


Fig. 4. Measured V_{DS} vs. time for four different SJ MOSFETs. The measurements are performed by using a double-pulse setup in a similar circuit as Fig. 1a (V_{DD} = 100 V, I_{DD} = 4 A). The V_{DS} inflection point is perfectly correlated to the V_{FD} definition in Fig. 3.

III. CURRENT DIVERSION

The current diversion phenomenon, triggered by the existence of displacement currents which internally charge and discharge the capacitances within the device, consists on the division of the MOSFET source current (I_S) into two components: the current that flows through the channel (I_{CH}) and the current that flows through the output capacitance (I_{COSS}).

This effect, experimentally proven in [10], only takes place during some specific periods of time within fast turn-on and turn-off events. An alternative method used in this manuscript to study the current diversion is the Mixed-Mode simulation. Mixed-Mode simulation combines the TCAD structures in Fig. 1b with the SPICE circuit depicted in Fig. 1a. Hence, the physical effects in the SJ MOSFETs are captured with more accuracy than using SPICE-based models. A direct consequence is the recognition of current due to hole or electron flow, corresponding to I_{COSS} and I_{CH}, respectively. For the specific case of SJ MOSFET #4 (ON Semiconductor prototype), the technological and geometrical parameters are perfectly detailed in the TCAD structure. This structure is therefore selected to exemplify the current diversion effect as well as to calibrate the same effect in the analytical model.

The simulated waveforms during the turn-off, calculated by SDEVICE from Sentaurus™ [11], are plotted in Fig. 6 for two different values of external gate resistance (R_{G_EXT}). The selection of 150 Ω and 10 Ω for R_{G_EXT} allows the analysis of slow and fast transitions. In both cases, an I_{CH} fall is observed at the start of the Miller plateau. The remaining current level after the current fall is defined as current plateau (I_P) and it becomes a fundamental piece of our analytical model. Interestingly, I_{CH} falls down to I_P due to the charging of C_{OSS} by I_{COSS}, as it can be seen in Fig. 5. Note that this occurs in parallel to V_{DS} rise. It is therefore deduced, for small R_{G_EXT}, the need to charge C_{OSS} in a short time demands high I_{COSS}, temporally diverted from I_{CH}. The reduction of I_P at small R_{G_EXT} is more prominent for values below 20 Ω, as it is observed in Fig. 6c. A similar phenomenology occurs in a lesser extent to charge C_{ISS} when part of I_S diverts to I_G. Such a second order current diversion, only noticeable in the case of 10 Ω for R_{G_EXT}, is neglected in this model for simplification.

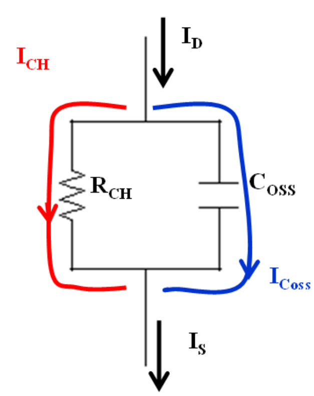


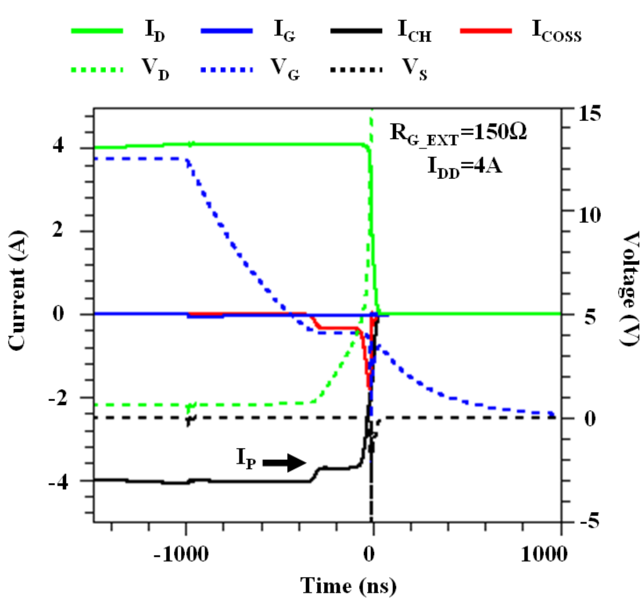
Fig. 5. Simplified model of the MOSFET to explain current diversion effect.

The key to obtain accurate I_{COSS} and I_{CH} waveforms in this analytical model is I_P value. In order to model I_P with accuracy, it needs to be taken into account, that there is a high dependency of this value with $R_{G\_EXT.}$ Therefore by taking that into account and relating I_P also with circuit behaviour and device data, a general analytical formula has been developed empirically by observing I_P patterns in the simulated waveforms. This analytical formula is provided in (1),

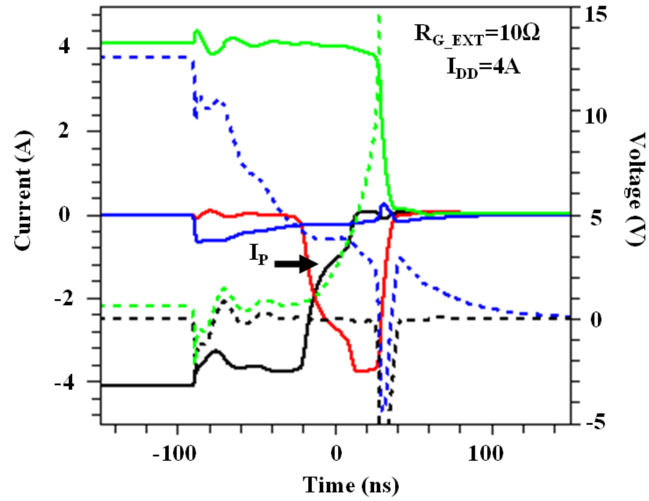
$$I_p = I_{DD} e^{-k\frac{Q_{DS}V_{GG}}{Q_{GD}I_{DD}R_G}} \quad (1)$$

where the dependencies with I_{DD} which is the current in the MOSFET when is turned on , R_G which is the sum of R_{G_EXT} and R_{G_INT}, V_{GG} which is the driving voltage of the MOSFET, Q_{GD} and Q_{GS} are taken into account and where k is a parameter of adjustment. The value of k is adjusted to 1.2 empirically to match the analytical and simulated I_P for SJ MOSFET #4. It is noteworthy that this value remains constant for different current (I_{DD}) conditions. A good correlation for I_P vs. R_{G_EXT} is demonstrated in Fig. 7 comparing analytical and simulated values for I_{DD} 4 and 10 A.

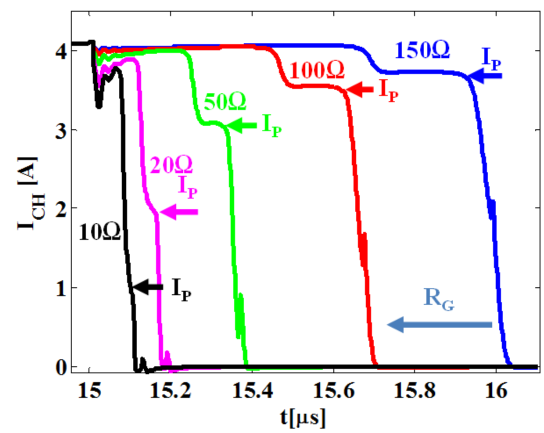
In the context of our piecewise model, I_P becomes relevant in the second and third stages of the turn-off as explained in the following section. During the turn-off plateau region, I_P calculated in (1) is subtracted from I_{CH}, which represents the unique current able to generate losses by Joule effect. Conversely, during the turn-on plateau region, I_P is added to I_{CH}. The latter, perfectly counterbalances the lower MOSFET power loss at the turn-off ($P_{SW,OFF}$) by a higher MOSFET power loss at the turn-on ($P_{SW,ON}$) [9]. Hereafter, for practical reasons, our model automatically adds the difference between $P_{SW,OFF}$ calculated by I_D and I_{CH} to $P_{SW,ON}$ calculated by I_D.



(a)



(b)



(c)

Fig. 6. Simulated current and voltage waveforms during the turn-off for (a) R_{G_EXT}=150Ω and (b) R_{G_EXT}=10Ω (I_{DD} = 4 A). The I_{CH} value during the Miller plateau, otherwise named I_P, is indicated in both cases. (c) Variation of I_{CH} with R_G, in order to show the effect over the current plateau (I_P).

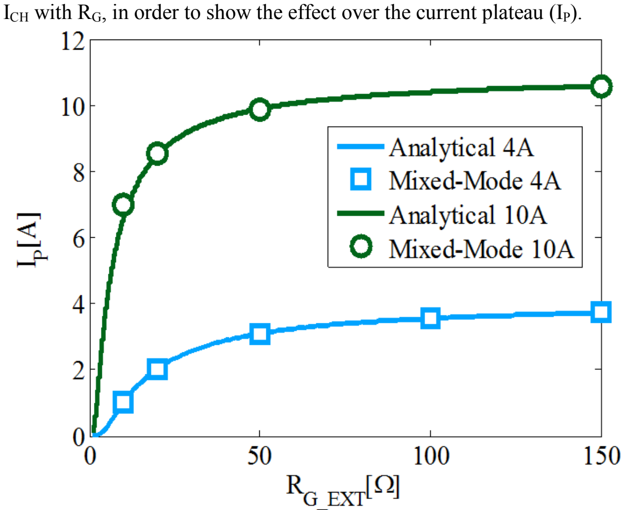


Fig. 7. I_P vs. R_{G_EXT} extracted from analytical model (lines) and simulations (symbols). I_{DD} is 4 and 10 A. $I_P = I_{CH} = I_{DD}$ for large R_{G_EXT}.

IV. Analytical Model Description

The proposed piecewise analytical model is divided in multiple stages in both the turn-on (see Fig 8a) and turn-off (see Fig. 8b). Each one of these total ten stages is defined by observing patterns in the measured waveforms of different SJ MOSFETs in a DC/DC converter. Hence, this model reliability has only been tested for DC/DC converter under normal operating conditions for the MOSFET. It should be noted that turn on and turn off are completely independent. In order to estimate the waveforms, the equations need to be used sequentially, always calculating all the parameters from the previous stage before proceeding to the next stage (e.g. stage 1 parameters need to be calculated before proceeding into stage 2).

A. Turn on (Stage 1-5)

Stage 1 (t_0-t_1): At the start of this stage the voltage applied between the gate and the source (V_{GS}) is zero. By increasing V_{GG}, both C_{GS} and C_{GD} will start being charged, thus increasing V_{GS} exponentially, as shown in (2) with $\tau_{iss} = R_G \cdot [C_{GS2} + C_{GD2}]$. At this stage the MOSFET is supporting high voltage, therefore C_{GS2} and C_{GD2} are going to be used.

$$V_{GS}(t) = V_{GG}\left[1 - e^{-(t-t_0)/\tau_{iss}}\right] \qquad (2)$$

During this stage the diode will still be conducting until V_{GS} reaches the threshold voltage value (V_{th}) that is reached by the end of this stage. Therefore, the MOSFET is not conducting and the voltage between drain and source (V_{DS}) is equal to V_{DD}.

Stage 2 (t_1-t_2): In this stage V_{GS} surpasses the threshold voltage which means that the current will start increasing from zero. Thus, making V_{DS} to start dropping. In this case $t_2 - t_1$ is defined as the time it takes the current to go from 0 A to I_{D_PEAK}, where I_{D_PEAK} is the peak current reached thanks to the reverse recovery of the diode. Therefore, it is important to be able to characterize the reverse recovery effect of the diode correctly. For this reason, an approximation similar to the one explained in [1] is going to be used, considering the Q_{RR} of the diode and the di/dts in order to obtain I_{D_PEAK}. V_{GS} also reaches a peak by the end of this stage that is defined by:

$$V_{GS\_PEAK} = \frac{I_{D\_PEAK}}{g_{fs}} + V_{th} \qquad (3)$$

where g_{fs} is the transconductance of the MOSFET.

It is important to take into account that during this stage the FET can either be working in the ohmic region or in the saturation region. In this analytical model only the saturation region is going to be considered, due to the characteristics of the application.

In the case under study the current starts increasing following V_{GS}. V_{GS} is obtained from the Laplace transformation of the equivalent circuit of the stage as done in previous works [1],[2].

$$V_{GS}(t) = V_{GS\_PEAK} - \left(V_{GS\_PEAK} - V_{th}\right)\left[e^{-(t-t_1)/\beta}\right] \qquad (4)$$

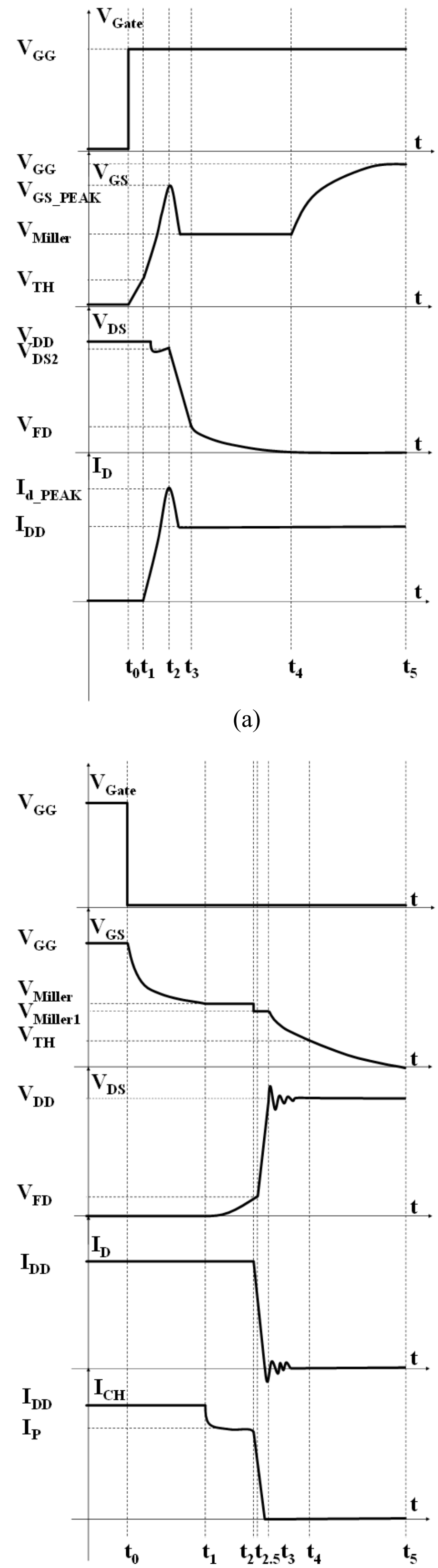


Fig. 8. Piecewise analysis of current and voltage waveforms for SJ MOSFETs during (a) turn-on and (b) turn-off.

$$I_D(t) = g_{fs}[V_{GG} - V_{th}]$$

$$\left\{1 - \frac{1}{\tau_a - \tau_b}\left(\tau_a\left(e^{-(t-t_1)/\tau_a}\right)^q - \tau_b\left(e^{-(t-t_1)/\tau_b}\right)^q\right)\right\} \quad (5)$$

$$V_{DS}(t) = V_{DD} - (L_s + L_d)\frac{dI_D}{dt} \quad (6)$$

where L_S and L_D are parasitic inductances that are depicted in the circuit of Fig. 1a. The following parameters are to be applied to (5).

$$\tau_n = R_G(C_{GS2} + C_{GD2}) + g_{fs} \cdot L_s \quad (7)$$

$$\tau_m = \sqrt{R_G \cdot C_{GS2} \cdot g_{fs}(L_s + L_d)} \quad (8)$$

$$\tau_a = \frac{2\tau_m^2}{\left(\tau_n - \sqrt{\tau_n^2 - 4\tau_m^2}\right)} \quad (9)$$

$$\tau_b = \frac{2\tau_m^2}{\left(\tau_n + \sqrt{\tau_n^2 - 4\tau_m^2}\right)} \quad (10)$$

It is important to note that in (5), q is a fixed value that was experimentally adjusted to fit SJ MOSFET di/dt and it has the same value for the four MOSFET under study. Also, g_{fs} is non-linear and it varies with I_D. g_{fs} will be considered constant for the value of I_{DD} under study, even though the current through the MOSFET changes during the switching stage.

Stage 3 (t_2-t_3): At this time, the MOSFET V_{DS} starts dropping until it reaches V_{FD} and the current drops to zero in the diode, meaning it is equal to I_{DD} in the MOSFET. Therefore, the amount of time required for this stage is not as simple to calculate as in other stages, mainly because t_3 can either be considered as the time V_{DS} reaches V_{FD} or the time it takes for I_D to reach I_{DD}. For this analysis both times will be calculated, and t_3 will be taken as the time it takes longer to achieve. This is the reason $t_{2.5}$ is defined in this stage, $t_{2.5}$ will always be considered as the time V_{DS} reaches V_{FD}. So in the case it takes longer for V_{DS} to reach V_{FD}, t_3 will be equal to $t_{2.5}$. During this stage I_D reaches I_{DD}, in order to model this slope, the frequency of oscillation of the ringing is going to be taken into account considering a sinusoidal waveform for the ringing of the current. Therefore, I_D is modelled as followed:

$$f_{osc} = \frac{1}{2\pi\sqrt{(L_d + L_s)(C_{GD2} + C_{DS2})}} \quad (11)$$

$$I_D(t) = \left[I_{d\_PEAK} - I_{DD}\right]\cos\left(\omega_{osc}(t - t_2)\right) + I_{DD} \quad (12)$$

If I_{DD} is reached before V_{FD}, I_D is kept constant at I_{DD} value and V_{FD} will eventually be reached in the next stage. Otherwise, V_{FD} will be defined by (13) until the time is $t_{2.5}$. From $t_{2.5}$ till t_3 V_{DS} will be defined by (14)

$$V_{DS}(t) = V_{DS2} - \left[\frac{V_{GG} - V_{miller}}{R_G \cdot C_{GD2}}\right](t - t_2) \quad (13)$$

where, $V_{miller} = \frac{I_{DD}}{g_{fs}} + V_{th}$.

$$V_{DS}(t) = V_{FD} \cdot \left[e^{-(t-t_{2.5})/\alpha}\right] \quad (14)$$

In (14), α is the value that allows V_{DS} to be equal to V_{ds_on} at t_4. The time t_4 can be defined as $t_4 = t_2 + t_{mp}$, where t_{mp} is the time of the Miller Plateau that is obtained as shown in (15).

$$t_{mp} = \frac{\left(V_{FD} - V_{ds\_on}\right) \cdot \left(R_{G\_ext} + R_{G\_int}\right) \cdot C_{GD1}}{\left(V_{GG} - V_{th}\right)} \quad (15)$$

Finally for this stage, V_{GS} is defined as shown in (16). When V_{miller} is reached V_{GS} is kept constant at that value.

$$V_{GS}(t) = V_{GS\_PEAK} + \frac{1}{g_{fs}} \cdot \frac{di}{dt} \cdot (t - t_2) \quad (16)$$

Stage 4 (t_3-t_4): The time this stage lasts is determined by (15) as explained before. V_{DS} is given by (14) and the current is kept constant at I_{DD} value. It should be noted that from this point onwards the model is no longer working in the high voltage range and C_{GD1} and C_{DS1} are going to be used.

Stage 5 (t_4-t_5): At this stage the MOSFET is in the on state, therefore $V_{DS}(t)$ is kept at V_{ds_on} and $I_D(t)$ is kept at I_{DD}. In terms of V_{GS}, it continues to charge up the output capacitance (C_{OSS}) following the next equation, where $\tau_{oss} = R_G \cdot (C_{GD1} + C_{DS1})$.

$$V_{GS}(t) = V_{miller} + (V_{GG} - V_{miller})\left(1 - \left(e^{-(t-t_4)/\tau_{oss}}\right)\right) \quad (17)$$

B. Turn off (Stage 6-10)

Stage 6 (t_0-t_1): During this stage V_{GS} starts at V_{GG} value. The moment V_{GG} is set to zero, V_{GS} starts decreasing steadily, due to the discharge of the parasitic capacitances of the MOSFET, as shown in (18) where $\tau_{iss} = R_G(C_{GS1} + C_{GD1})$. At this stage the MOSFET is supporting low voltage, therefore C_{GS1} and C_{GD1} are going to be used.

The MOSFET is still in conduction mode in this stage, therefore, I_D and V_{DS} are both kept at I_{DD} and V_{DD} respectively, and I_{CH} is kept at I_{DD}.

$$V_{GS}(t) = V_{GG} \cdot e^{-(t-t_0)/\tau_{iss}} \quad (18)$$

The end of this stage is set when V_{GS} reaches the level of the Miller Plateau, V_{miller}.

Stage 7 (t_1-t_2): In this stage, V_{DS} begins to increase, as stated by (19), not necessarily reaching V_{FD} by the end of this stage. The duration of this stage is defined by the Miller Plateau time. This duration can be calculated by using (20).

$$V_{DS}(t) = V_{ds\_on} \cdot e^{-(t-t_1)/\gamma} \quad (19)$$

$$t_{mp} = \frac{\left(R_{G\_ext} + R_{G\_int}\right)\left(V_{FD} - V_{ds\_on}\right)C_{GD1}}{V_{th}} \quad (20)$$

During this time I_D is still constant at I_{DD} level and V_{GS} is constant at V_{miller} voltage. Although, the drain current is constant, the current going through the channel (I_{CH}) starts to drop reaching the current plateau level (I_P) and keeping this current during the whole duration of this stage. I_P is calculated as shown in (1). As for the drop of I_{CH}, it is calculated as shown in (21), taking into account that it is C_{GD} the capacitance that needs to be discharged through the channel of the MOSFET at this stage.

$$I_{CH}(t) = (I_P - I_{DD})e^{-(t-t1)/(R_G C_{GD1})} - I_P \quad (21)$$

Stage 8 (t_2-t_3): During this stage V_{DS} will continue to increase until it reaches V_{DD}, meaning C_{DS2} and C_{GD2} are going to be used from this stage until the end of the turn off. I_D will start to drop and it should reach zero before V_{DD} is reached in a SJ MOSFET. I_{CH} will also drop and in this case with the same slope I_D drops until it reaches zero.

As it was done in stage 3, the moment in time when V_{DS} reaches V_{FD} will be defined as $t_{2.5}$. Thus, V_{DS} will be defined by (19) until this value is reached and then V_{DS} will follow (22) until it reaches V_{DD}.

$$V_{DS}(t) = V_{FD} + \frac{(V_{GG} - V_{FD})}{R_G C_{GD2}}(t - t_{2.5}) \quad (22)$$

$$I_D(t) = g_{fs}\left[\frac{V_{miller}}{(\tau_a - \tau_b)}\left(\tau_a\left(e^{-(t-t_1)/\tau_a}\right) - \tau_b\left(e^{-(t-t_1)/\tau_b}\right)\right) - V_{th}\right] \quad (23)$$

In this scenario V_{GS} is constant at a lower level than the Miller Plateau that can be defined as $V_{Miller1}$, that is dependent of the IP previously calculated.

$$V_{miller1} = \frac{I_P}{g_{fs}} + V_{th} \quad (24)$$

Stage 9 (t_3-t_4): In super-junction devices I_D should be zero by the start of this stage due to di/dts being much higher than in planar MOSFET, thus implying that the MOSFET will not enter this stage and could be considered as part of stage 8.

Stage 10 (t_4-t_5): In this final stage of the turn off, V_{GS} will drop from $V_{miller1}$ until it reaches zero while C_{OSS} is being discharged. As for V_{DS} and I_D both remain constant at V_{DD} and zero respectively. For the sake of completion parasitic effects of the circuit can be used in order to add overshoot and ringing to the waveforms, as it was done in previous works [1]. It is important to note that these effects are not going to have a dramatic influence over the losses and they will improve the matching of the experimental and analytical waveforms to an extent.

$$V_{DS}(t) = V_{DD} + V_{max} \cdot e^{-\alpha(t-t_4)} \quad (25)$$

$$V_{GS}(t) = \frac{V_{miller1}}{\tau_a - \tau_b}\left(\tau_a\left(e^{-(t-t_4)/\tau_a}\right) - \tau_b\left(e^{-(t-t_4)/\tau_b}\right)\right) \quad (26)$$

$$I_D(t) = -(C_{GD2} + C_{DS2}) \cdot V_{max} e^{-\alpha(t-t_4)} \cdot \omega \cdot sin(\omega(t - t_4)) + \alpha \cdot cos(\omega(t - t_4)) \quad (27)$$

$$\alpha = \frac{R_{G\_int}}{2 \cdot (L_s + L_d)} \quad (28)$$

$$\omega = \sqrt{\frac{1}{(C_{GD2} + C_{DS2})(L_d + L_s)} - \alpha^2} \quad (29)$$

V. Experimental Validation and Discussion

The experimental validation of the analytical model is carried out by means of a DC/DC buck converter where the Device Under Test (DUT) is switched by a double pulse (V_{DD} = 100 V and I_{DD} = 4A). In order to obtain the waveforms of the current though the DUT, a shunt resistor is placed in series to its source to measure the source current (I_S). Moreover, voltage probes are placed to sense V_{GS} and V_{DS}. Even though diverse operation conditions were tested, the set of conditions in Table II is selected for the validation of the model. This selection is optimal with respect to the reduction of the current ringing as well as identification of V_{FD}. There are also included in Table II the parasitic inductances of the PCB board, thus completing the dataset corresponding to the setup, that have been obtained by using finite element on the PCB design, as well as, adding the parasitic inductance from the TO-220 package. Aside from the data in Table II, a second group of data, summarized in Table III, is related to the electrical characteristics of the SJ MOSFET used as a DUT. These electrical characteristics are collected from the datasheet of SJ MOSFET for all the samples under analysis shown in Table III, Fig. 9 explains thoroughly the process it needs to be followed to extract the parameters correctly. Both datasets are the essential inputs that our analytical model requires. The model has been implemented in MatLAB® in order to generate waveforms and to compute the dissipated powers in a time range of a few seconds.

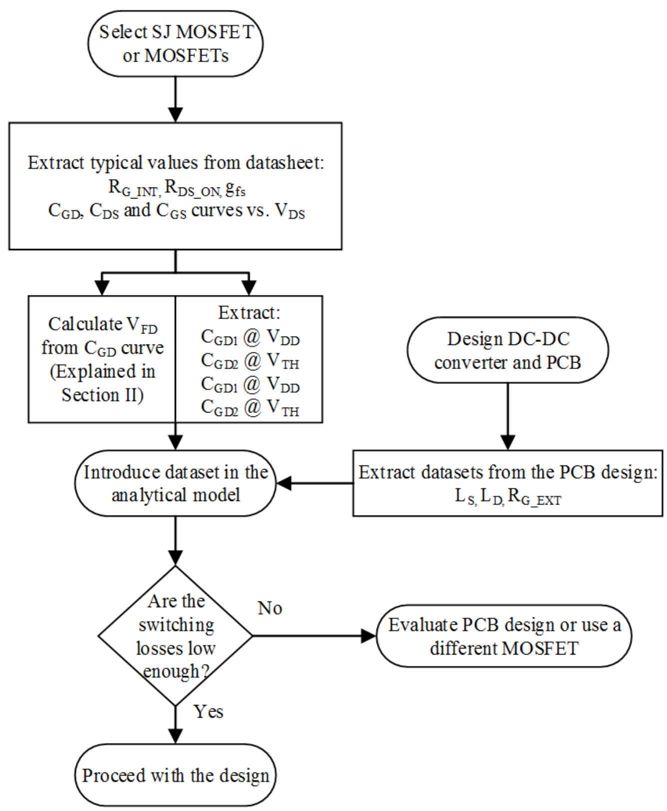


Fig. 9. Flowchart explaining the parameter extraction process for the analytical model.

The waveforms calculated with the analytical model and measured in the test setup are compared in Fig. 10 for samples #1 and #3 which are the samples with more different switching waveforms for both transients, since sample #2 has similar waveforms to sample #1 and sample #3 has similar waveforms to sample #4. These waveforms correspond to the dynamic evolution of V_{DS} (Fig. 10c), V_{GS} (Fig. 10a) and I_D (Fig. 10b) during turn-on and turn-off (considering the measured I_S equal to $-I_D$). Furthermore, the instantaneous dissipated power ($P_{SW,SP}$), defined as $V_{DS} \cdot I_D$, is represented in Fig. 10d to identify the position of the power peaks during the transients. It should be noted that the time scale differs in order to show the reliability of the analytical model during the transients.

By simple comparison of the waveforms, it can be seen that the analytical model is able to match the experimental waveforms with accuracy. The consideration of V_{FD}, helps greatly in this task in the case of V_{DS}, and especially in V_{GS}, improving the match between stage times and Miller plateau levels. In spite of this, I_D continues showing some discrepancies during the turn-on due to the modeling of the reverse recovery. In this sense, the value of di/dt matches but the reverse recovery peak introduces some error in the power loss calculation.

TABLE II. OPERATION CONDITIONS AND PCB INDUCTANCES

Parameter	***Value***
R_{G_EXT} [Ω]	150
L_S [nH]	16
L_D [nH]	12
V_{GG} [V]	12
V_{DD} [V]	100
I_{DD} [A]	3
f [kHz]	100

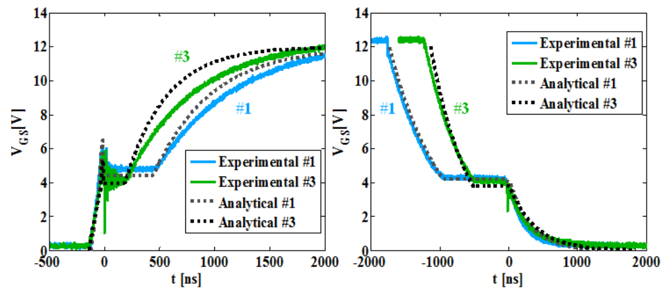
TABLE III. SJ MOSFET PARAMETERS IN THE ANALYTICAL MODEL

Parameter	**MOSFET Samples**			
	#1	***#2***	***#3***	***#4***
C_{GD1}[pF]	2000	2200	500	920
C_{GD2} [pF]	15	9.5	18	12
C_{GS} [pF]	1500	2000	2000	1720
C_{DS1} [pF]	7000	6700	6500	29000
C_{DS2} [pF]	70	60	70	65
V_{FD} [V]	47	24	28	8
R_{G_INT}[Ω]	8.5	4	4	6.5
gfs	3	5	6.5	3
R_{ds_on}[mΩ]	170	150	140	150

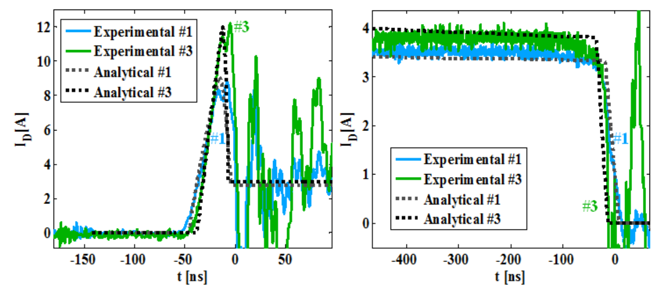
These waveforms are used in order to estimate the losses during the switching stage, formerly called P_{SW}. The P_{SW} calculation is done by integration of $P_{SW,SP}$ in Fig. 10d, or by using (30)

$$P_{sw} = f \int V_{DS}(t) I_D(t)\, dt \tag{30}$$

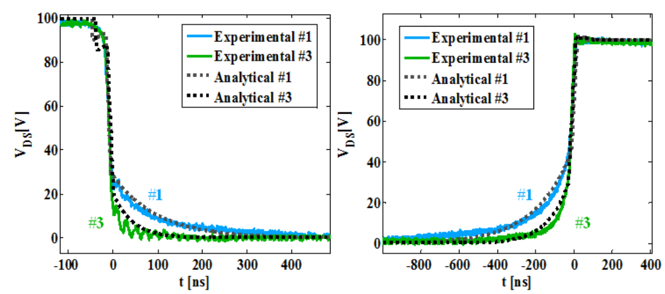
The intervals of integration are delimited by the start of V_{DS} fall and the end of V_{GS} raise, for $P_{SW,ON}$, and by the start of the V_{GS} fall and the end of the V_{DS} raise, for $P_{SW,OFF}$ (P_{SW}= $P_{SW,ON}$ + $P_{SW,OFF}$). Note that, at this point, the effect of the current diversion is not yet considered, due to the fact that it cannot be compared with experimental data.



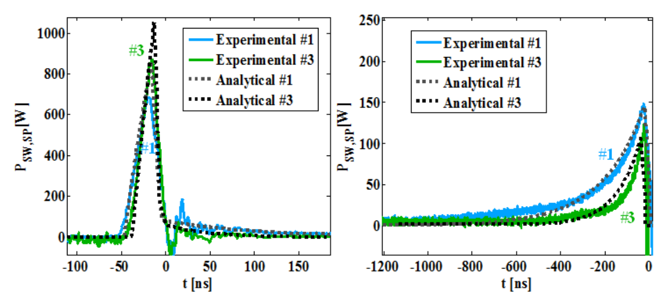
(a)



(b)



(c)



(d)

Fig. 10. Comparison between measured (solid lines) and analytical (dotted lines) waveforms for (a) V_{GS} (b) I_D, (c) V_{DS} and (d) the instantaneous dissipated power ($P_{SW,SP}$).

After applying (30), all the analytical and measured $P_{SW,ON}$ and $P_{SW,OFF}$ are summarized in Table IV for samples #1, #3 and #4. A maximum of 21% percent of error in a separated transient event is observed, which proves the good accuracy of the model. Even more, this percentage falls below the 20% when considering the error over P_{SW}.

TABLE IV. SWITCHING POWER LOSS COMPARISON (CURRENT DIVERSION NOT INCLUDED)

Sample		Method		Error
		Analytical	*Experimental*	
#1	$P_{SW,ON}$ [W]	2.96	2.46	+17%
	$P_{SW,OFF}$ [W]	2.99	3.42	-13%
	P_{SW} [W]	5.95	5.88	+3%
#2	$P_{SW,ON}$ [W]	3.01	2.65	+12%
	$P_{SW,OFF}$ [W]	2.91	3.04	-4%
	P_{SW} [W]	5.92	5.69	+4%
#3	$P_{SW,ON}$ [W]	2.29	1.99	+13%
	$P_{SW,OFF}$ [W]	1.38	1.09	+21%
	P_{SW} [W]	3.67	3.08	+16%
#4	$P_{SW,ON}$ [W]	2.82	2.32	+20%
	$P_{SW,OFF}$ [W]	0.91	0.82	+10%
	P_{SW} [W]	3.73	3.14	+15%

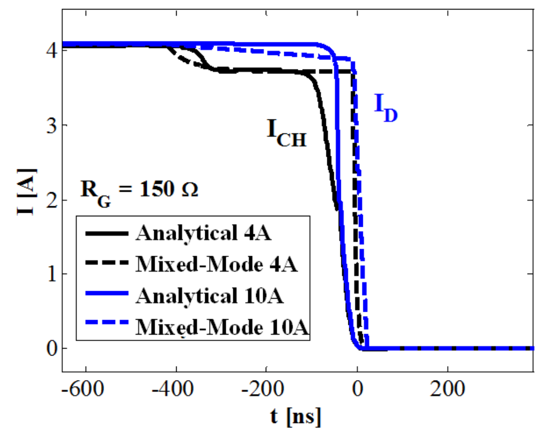
TABLE V. IMPACT OF CURRENT DIVERSION ON POWER LOSSES (SAMPLE #4, R_{G_EXT} = 150Ω)

	Without current diversion			With current diversion		
	$P_{SW,ON}$ [W]	*$P_{SW,OFF}$ [W]*	*P_{SW} [W]*	*$P_{SW,ON}$ [W]*	*$P_{SW,OFF}$ [W]*	*P_{SW} [W]*
Experimental	2.32	0.82	3.14	---	---	---
Mixed-Mode	2.53	1.03	3.56	3.27	0.29	3.56
Analytical	2.82	0.91	3.73	3.24	0.49	3.73

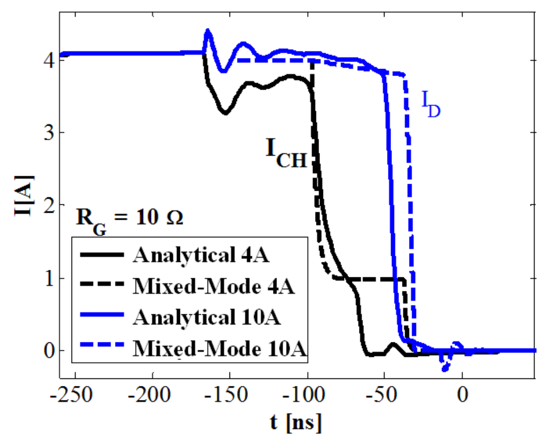
In a more advanced analysis of P_{SW}, the current diversion explained in Section III is considered by replacing (30) with (31) during the applicable time intervals.

$$P_{sw} = -f \int V_{DS}(t) I_{CH}(t)\, dt \tag{31}$$

This modification is not expected to vary P_{SW} but the distribution of power loss between $P_{SW,ON}$ and $P_{SW,OFF}$. Before calculating the new power losses, the precision of the model in reproducing I_{CH} is exemplified in Fig. 11 by comparing analytical with simulated waveforms. The simulated I_{CH} and I_D waveforms in Fig. 11 correspond to a zoom of the curves in Fig. 6 for sample #4 with an R_{G_EXT} of 10 Ω and 150 Ω. It is observed that, although I_P matches perfectly, the duration of the plateau is larger in the analytical curves. Subsequently, a second order overestimation of $P_{SW,OFF}$ is expected. A comparison of waveforms during the turn-on is not presented because of the intricate current identification. As a matter of fact, the reverse recovery current flows from the power diode to the MOSFET, thus masking the displacement current. For practical reasons, the model does not recalculate I_{CH} during the turn-on; it proceeds by directly adding the power loss reduction during the turn-off into the turn-off power loss.



(a)



(b)

Fig. 11. Comparison between simulated (solid lines) and analytical (dashed lines) current waveforms for I_{CH} (black) and I_D (blue). R_{G_EXT} is (a) 150Ω and (b) 10Ω whereas and I_{DD} is fixed to 4 A in all cases.

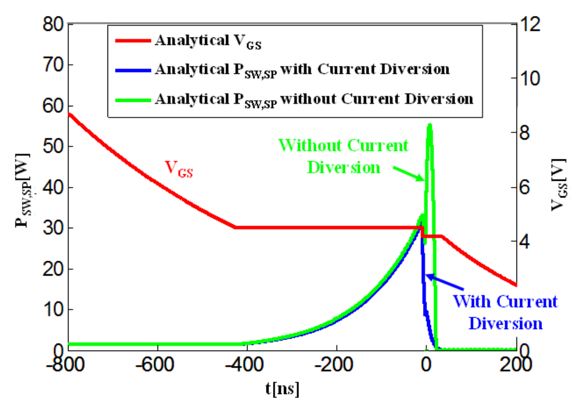


Fig. 12. Analytical $P_{SW,SP}$ vs. time for the cases with and without current diversion. Analytical V_{GS} is introduced as a reference to identify the Miller plateau. (Sample #4, R_{G_EXT} = 150 Ω)

The impact of the current diversion on the power losses is inferred from Table V for sample #4 with an R_{G_EXT} of 150 Ω. Even though P_{SW} is preserved, both analytical and simulated methods show dissimilar $P_{SW,ON}$ and $P_{SW,OFF}$. More precisely, the cases without current diversion underestimate $P_{SW,ON}$ by 25% and overestimate $P_{SW,OFF}$ by 200%. The origin of the new power distribution is understood by Fig. 12, where the analytical $P_{SW,SP}$ for the cases with and without current diversion are compared. In the case without current diversion, a 30% of $P_{SW,OFF}$ is added at the end of the Miller plateau during a short time (i.e., when the $I_D V_{DS}$ crossing takes place during less than 50ns). The fast plummeting of I_{CH} with respect to I_D avoids the additional power loss when considering current diversion. This effect, evidenced in Fig. 10, results in a sort of zero-current switching at the turn-off. Another observation is the utter importance of the power dissipated during the Miller plateau ($P_{SW,MP}$). For large R_{G_EXT}, $P_{SW,MP}$ constitutes the larger part of $P_{SW,OFF}$ and it is scarcely impacted by current diversion. Besides the well-known dependencies of $P_{SW,MP}$ with R_{G_EXT} and Q_{GD}, the effect of V_{FD} is also included in the new model. Effectively, among other electrical parameters, a low V_{FD} contributes in reducing $P_{SW,MP}$. The current diversion effect can be of utter importance when using soft switching techniques, such as zero-current switching (ZCS) or zero-voltage switching (ZVS) where only one transient is removed.

Finally, it is important to note that testing of the analytical model has been done for different values of R_{G_EXT} from a range of 10 to 150 Ω and compared to their respective experimental waveforms in order to validate the model. It was decided in the end to use the waveform comparison of 150 Ω in this work because they are more representative in order to visualize the different stages proposed in the analytical mode, even though a much smaller value is normally used in this kind of application.

VI. Conclusion

A major breakthrough towards an accurate analytical model for high-voltage SJ MOSFETs is reported and experimentally proven in this paper. The non-linear approximation of the capacitances, as well as, the newly defined V_{FD} contribute to the accuracy of this model, proving the importance and the need of a good characterization of non-linear parameters in analytical models. A first order approach to the calculation of I_{CH} by considering the current diversion effect is introduced for the first time in an analytical model. As forthcoming work, we expect to improve the compactness and precision of the model, as well as, to extend testing the predictability of our model to other commercial SJ MOSFET and other circuit topologies.

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