A novel adaptive synchronous rectification system for low output voltage isolated converters

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***Abstract*—The design of efficient, isolated low output voltage converters is a major concern due to their widespread use. One of the preferred methods used to maximize their efficiency is synchronous rectification, i.e. the replacement of the secondary side diodes with MOSFETs to decrease conduction losses. However, depending on the topology being used, synchronous rectification might not provide the required efficiency improvement or even be easily implemented. This paper presents a novel synchronous rectification system that can be applied to converters with symmetrically-driven transformers and to converters from the Flyback family; in both cases, the proposed system adaptively generates a control signal that controls a synchronous rectifier MOSFET placed in paralell with each diode, turning it on during the conduction intervals of the diodes. The proposed system uses only information from the secondary side, thus avoiding breaking the isolation barrier; it can be built using a few low cost analog components, it is reliable and simple, and could be easily implemented in an integrated circuit. Up to a 3 % improvement is demonstrated in a 3.3-5 V, 120 W Push-Pull converter and up to a 2.5 % improvement is obtained in a 5 V, 50 W Flyback converter, both of them designed for telecom applications.**

***Index Terms*—DC-DC power converters, Power conversion, Switching converters**

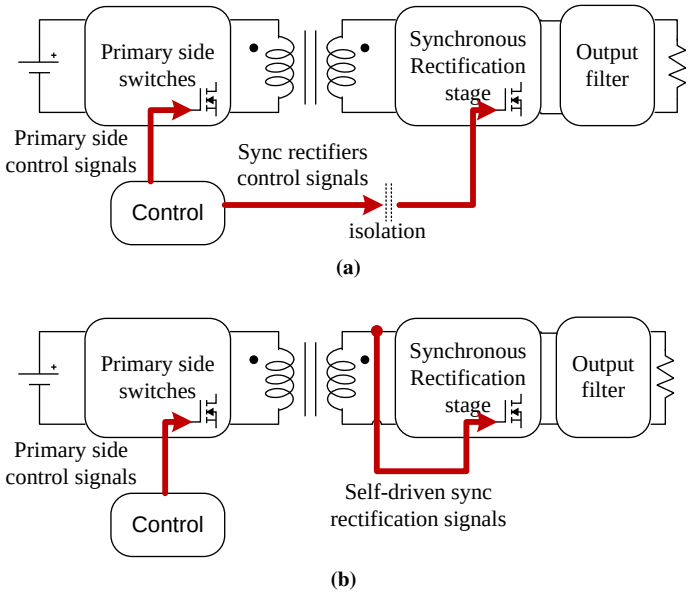

Figure 1. Isolated converter block diagram: (a) with EDSR; (b) with SDSR.

I. Introduction

LOW output voltage converters are widely used in many applications. The supply of integrated circuits, microprocessors and FPGAs is undoubtely one of the most important; said loads are usually supplied with voltages that can range from 1.2 V to 5 V, thus demanding high output currents from the converter. To increase the efficiency of these converters, transistors must replace diodes in the rectification stage, in a technique usually called Synchronous Rectification (SR). A detailed comparison between the use of diode rectifiers versus synchronous rectifiers can be found e.g. in [1].

In the majority of low output voltage applications, MOSFET transistors are used as synchronous rectifiers, mainly due to their low on-resistance that minimizes conduction losses. The major drawback regarding the use of synchronous rectifiers is the need for a control signal that has to turn on the transistor during the intervals when the diodes would be conducting, avoiding short circuits in the secondary side. Traditionally, two different techniques have been used to control the synchronous rectifiers [2]. The first one is called *External-driven Synchronous Rectification (EDSR)* and it is shown in Fig. 1a. In this technique, the control signals are generated by an auxiliar circuit that guarantees the appropriate timing, and thus the transistors can be activated during the whole rectification period and the efficiency can be maximized [3]. However, in isolated applications, the control signals that are usually generated in the primary side have to be transmitted to the secondary side, thus increasing complexity and cost.

Fig. 1b shows the second technique, called *Self-driven Synchronous Rectification* (SDSR). In SDSR the control signals are obtained directly from the power stage; therefore, the specific topology being used determines the conduction intervals of the rectifiers. SDSR is preferred in isolated applications because the control signals are usually obtained directly from the power transformer, thus yielding a very simple, efficient and reliable rectification stage [4]–[6]. Several modifications to the SDSR method have been proposed to improve its performance in certain applications [7]–[13], although the

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complexity of some of the solutions finally led to a hybrid scheme, as in [11], [12]. However, in many topologies the driving signals cause the synchronous rectifiers to be off during a certain part of the switching cycle, thus causing conduction of the parasitic diodes and decreasing efficiency. For instance, in topologies with symmetrically-driven transformers, as Half-bridge, Full-bridge and Push-Pull topologies, the synchronous rectifiers are not activated during the dead times of the transformer. This fact causes a noticeable decrease in the efficiency for high input voltages (i.e. low duty cycles). In telecom applications in which a wide input voltage range is common (18-36 V in rated 24 V converters and 36-72 V in rated 48 V converters), commercial products might suffer an efficiency drop as high as 4 % (see for instance the ASQ24 family [14]). Several solutions have already been proposed to solve this problem [15]–[17]. Reference [15] proposes a system based on additional windings to drive the synchronous rectifiers. It provides a very good performance but requires a very careful magnetic design, which can compromise the behavior of the system and increase the cost of the converter. References [16], [17] use an additional controlled voltage source to force the synchronous rectifiers to be on during the dead times. This system also performs well, but again requires a careful design of the voltage source, which in turn has to be regulated using extra circuitry that complicates the system.

This paper proposes a novel synchronous rectification scheme to be used in isolated converters that has been called Adaptive Off-Time Synchronous Rectification (AOTSR). The proposed system extends the time interval when the synchronous rectifiers are activated in topologies with symmetrically-driven transformers (Half and Full-bridges and Push-Pull) that implement SDSR. The system can also be used as a complete synchronous rectification system in converters from the Flyback family (Flyback, isolated SEPIC, Ćuk and Zeta). In this kind of applications the use of synchronous rectification has also been explored throughout custom circuitry: [18] uses very simple analog circuitry to control a synchronous rectifier in a low cost Flyback converter, but only when it operates in Discontinuous Conduction Mode (DCM). Several commercial ICs, as the IR11672 or the NCP4302, allow to control synchronous rectifiers using only information from the secondary side in Flyback and Half-Bridge converters, but the use of these ICs is currently not very widespread. Furthermore, those ICs turn on or off the rectifiers by measuring the instantaneous voltage across it, thus having relatively high noise-sensitivity. With the use of additional switches in converters with symmetrically-driven transformers with SDSR, and with a single switch in parallel with the diode in converters from the Flyback family, the AOTSR system provides a noticeable increase in the efficiency; it can be used with standard, primary-side control ICs, it can be implemented using very simple, low cost analog circuitry and it is suitable to be easily integrated. The proposed system is intended to work with fixed frequency converters that operate in Continous Conduction Mode (CCM). CCM operation is the usual design case for the target converters at full load, which is when synchronous rectification provides better results with respect to the use of diodes.

This paper is organized as follows: section II presents the AOTSR concept and its theoretical basics. Section III proposes a simple analog implementation of the AOTSR which can be used for both types of converters, while section IV presents several experimental results that show the efficiency improvement that can be achieved. Finally, section V states the conclusions.

II. The Adaptive Off-time Synchronous Rectification concept

For the sake of clarity, this section is divided in two parts: subsection II-A presents the AOTSR concept for converters with symmetrically-driven transformers, whereas subsection deals with converters from the Flyback family. Although the AOTSR concept is very similar in both cases, conceptually speaking the derivations of the main equations and the desired waveforms are slightly different, and therefore they are explained separately.

A. Converters with symmetrically-driven transformers

Fig. 2a shows a center-tapped SR stage typical of converters with symmetrically-driven transformers; only the output inductance of the filter stage is shown for simplicity. In the first half of the switching cycle, T_{sw}, $SR1$ is activated during the interval $[0, dT_{sw}]$, while during $t_{dead,1}$ its gate voltage falls to zero and the parasitic diodes carry the inductance current. During the second half of the switching cycle the same happens with $SR2$. The conversion ratio in this symmetrically-driven converters can be expressed as:

$$\frac{V_{out}}{V_{ct,peak}} = 2d \, , 0.5 \geq d \geq 0 \, , \tag{1}$$

$V_{ct,peak}$ depending on the topology; for instance, assuming a transformer turns ratio of $n:1:1$, in a Half-bridge converter $V_{ct,peak} = \frac{V_{in}}{2n}$, whereas in a Full-bridge and in a Push-Pull converter $V_{ct,peak} = \frac{V_{in}}{n}$.

Figure 2b shows a general block diagram of the proposed AOTSR and its corresponding operating waveforms. The idea is to connect an additional MOSFET in paralell with each main synchronous rectifier. These main synchronous rectifiers are still self-driven, as in a conventional SDSR design, thus having the advantages previously stated in Section I. The additional transistors, $AR1$ and $AR2$, which are placed in parallel with the main rectifiers $SR1$ and $SR2$, are controlled by the same signal, $v_{AR}(t)$. $AR1$ and $AR2$ are in charge of carrying the output current only during the main synchronous rectifiers off-time intervals, $t_{dead,1}$ and $t_{dead,2}$. Such arrangement, although requires additional transistors, keeps the advantages of SDSR and also eases thermal management. $t_{dead,1}$ and $t_{dead,2}$ can be easily found from Fig. 2:

$$\begin{aligned} &t_{dead,1} = t_{dead,2} = \\ &= \frac{T_{sw}}{2} - dT_{sw} = \frac{T_{sw}}{2}\left(1-2d\right) \, , 0 < D < 0.5 \, . \end{aligned} \tag{2}$$

As (2) shows, the dead times change with the duty cycle; therefore, the system has to adaptively change $v_{AR}(t)$ for

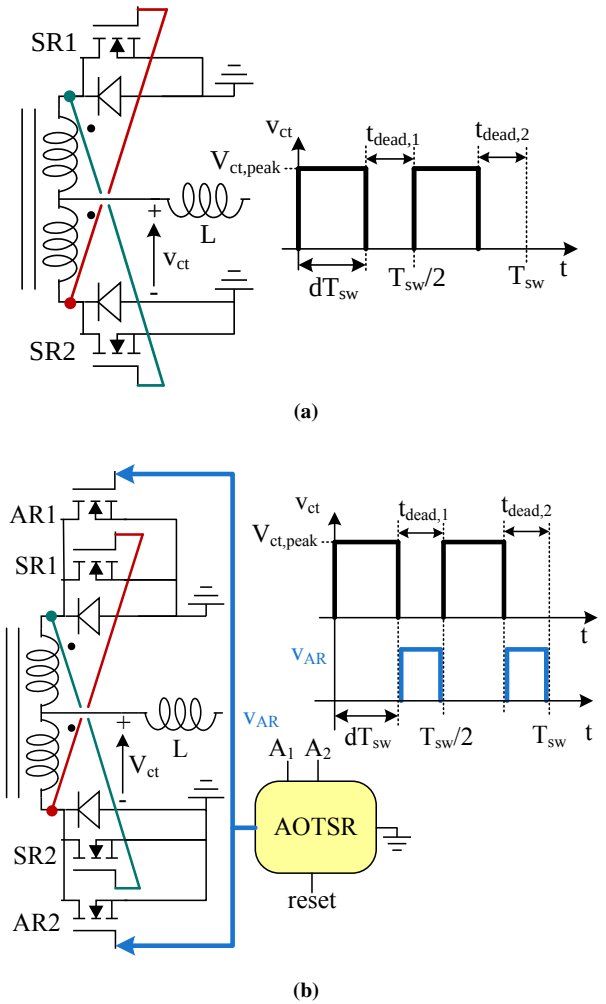


Figure 2. (a) Center-tapped rectifier with SDSR and corresponding waveforms in a converter with a symmetrically-driven transformer; (b) proposed AOTSR and desired control waveforms for the additional rectifiers AR1 and AR2.

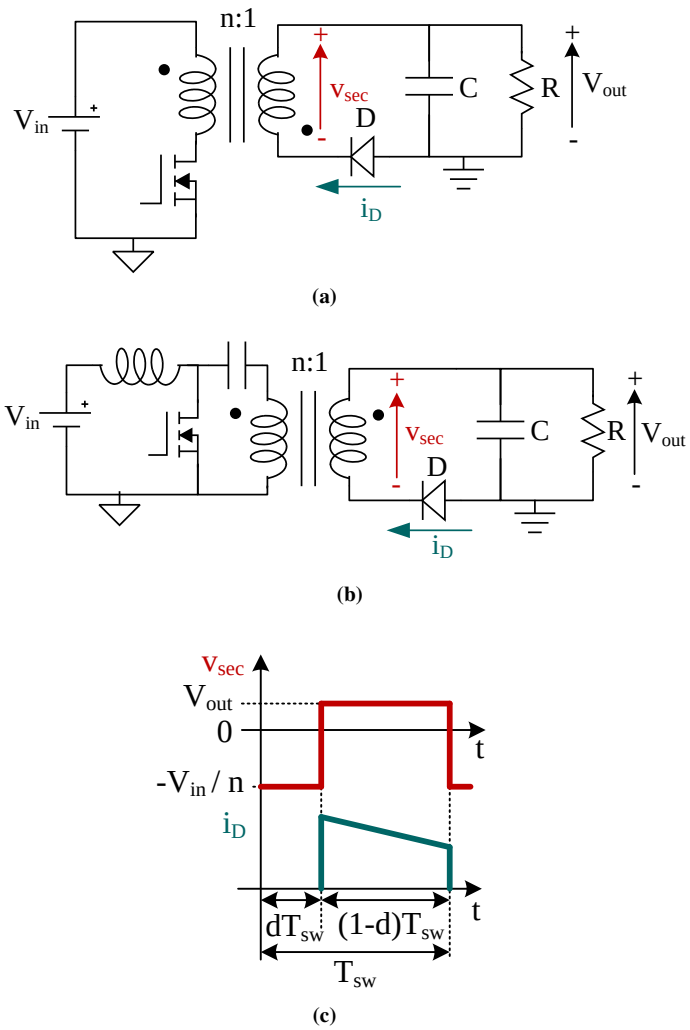


Figure 3. (a) Flyback converter; (b) isolated SEPIC converter; (c) ideal operating waveforms.

different operating conditions, avoiding an overlap with the control signals of the primary switches, situation that would cause a short-circuit in the secondary side. Furthermore, it has to generate $v_{AR}(t)$ using only information from the secondary side of the transformer to avoid breaking the isolation barrier; said information has been represented arbitrary in Fig. 2b by the input terminals A_1, A_2 and $reset$, that have to be connected to appropriate points of the secondary circuit to achieve the desired adaptive behavior.

B. Converters from the Flyback family

Figures 3 and 4 show the four isolated converters that arise from the buck-boost converter, i.e. the Flyback family of converters. Figs. 3a and 3b show a Flyback and an isolated SEPIC converter, respectively, while Fig. 3c shows their corresponding operating waveforms. Figs. 4a and 4b show the Zeta converter (inverse SEPIC converter) and the isolated Ćuk converter, respectively. Fig. 4c shows the corresponding waveforms. Note that in each group of figures a voltage that fulfills the volts-second balance is highlighted (V_{sec} in Fig. 3 and V_L in Fig. 4). The conversion ratio in these four isolated, buck-boost derived converters is:

$$\frac{V_{out}}{V_{in}} = \frac{1}{n}\frac{d}{1-d}\,. \tag{3}$$

In these four converters the output diode D carries the output current during $(1-d)\,T_{sw}$.

Figure 5 shows the proposed synchronous rectification scheme and its corresponding waveforms in the case of the Flyback converter. A MOSFET that acts as the synchronous rectifier, AR, must be added in paralell with D. The AOTSR system generates a control pulse, $v_{AR}(t)$, that turns AR on during $(1-d)\,T_{sw}$, avoiding an overlap with the control signal of the primary switch. Once again the system has to adaptively generate $v_{AR}(t)$ disregarding of the value of the duty cycle and using only information from the secondary side. The AOTSR block represented in Fig. 5 is the same as the one depicted in Fig. 2b; it is shown in the following section that the same implementation can be used for both cases, just connecting the corresponding terminals A_1, A_2 and $reset$ to appropriate points of the secondary side. Furthermore, the same implementation can also be directly applied to the isolated SEPIC, Ćuk and Zeta converters: a MOSFET must

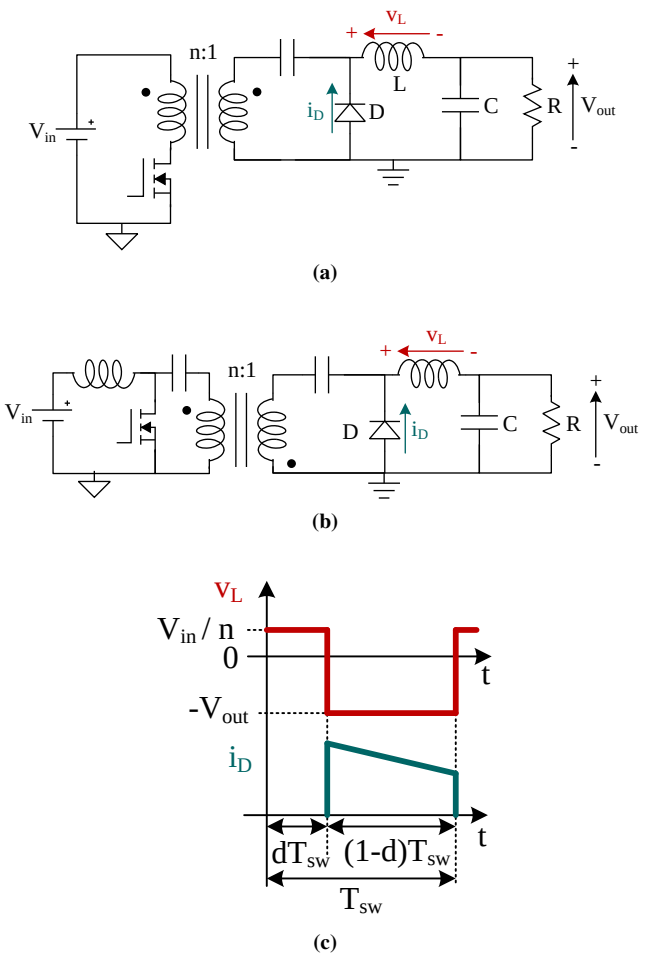


Figure 4. (a) Isolated Zeta converter (inverse SEPIC); (b) isolated Cuk converter; (c) ideal operating waveforms.

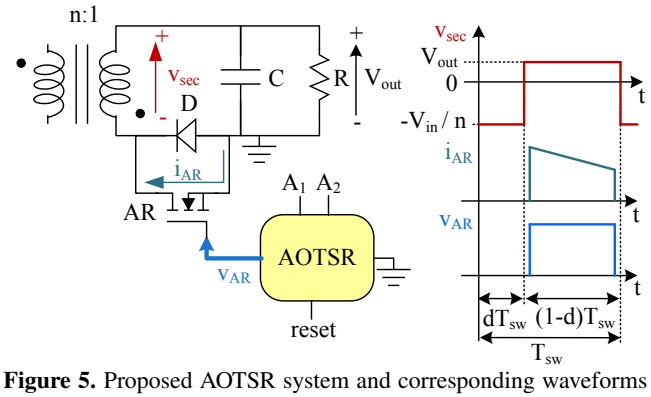


Figure 5. Proposed AOTSR system and corresponding waveforms in a Flyback converter.

be placed in paralell with D and activated during $(1-d)\,T_{sw}$. Note that in these four converters the auxiliary synchronous rectifier is ground-referenced.

III. Implementation of the Adaptive Off-time Synchronous Rectification

Fig. 6 shows the proposed implementation of the AOTSR system. It is comprised of a peak detector (D_{pd} and C_{pd}), two current mirrors (one made up of T_1 and T_2, and the second made up of T_3 and T_4) and a comparator. The key idea of the circuit is to charge C_{pd} to the peak voltage between A_1 and A_2 in each switching cycle:

$$V_{Cpd} = \max\left\{V_{A1}\left(t\right) - V_{A2}\left(t\right)\right\}_{T_{sw}\geq t\geq 0}\ . \tag{4}$$

Within a switching cycle, V_{Cpd} is assumed to remain constant. C_{pd} must be selected small enough to avoid any change in the operation of the converter, and at the same time it should be able to maintain its voltage approximately constant during a switching cycle, taking into account the current demand of the AOTSR circuitry. A capacitance in the range of a few hundreds of nanofarads is suitable for this application. Neglecting voltage drops in the transistor junctions, the current generated by the first current mirror, T_1 and T_2, is:

$$I_{T_1} = I_{T_2} = \frac{V_{Cpd}}{R_1}\ . \tag{5}$$

I_{T_1} generates a voltage at the positive input of the comparator equal to:

$$V_+ = R_2 \cdot \frac{V_{Cpd}}{R_1} = \frac{R_2}{R_1} V_{Cpd}\ . \tag{6}$$

Neglecting the voltage drop across D_{pd}, the current generated by the second current mirror (T_3 and T_4) is:

$$I_{T_3} = I_{T_4} = \frac{V_{A1}}{R_{ramp}}\ , \tag{7}$$

V_{A1} being the voltage at $A1$. Following Fig. 6, I_{T_4} charges C_{ramp} generating the following voltage waveform at the negative input of the comparator:

$$V_-\left(t\right) = \frac{V_{A1}}{R_{ramp}C_{ramp}} t\ . \tag{8}$$

The time when the voltage ramp V_- equals V_+ determines the lenght of the control pulse, t_{VAR}. Using (6) and (8):

$$\begin{aligned} &\frac{V_{A1}}{R_{ramp}C_{ramp}} t_{\text{VAR}} = \frac{R_2}{R_1} V_{Cpd} \Rightarrow \\ &\Rightarrow t_{\text{VAR}} = R_{ramp}C_{ramp}\frac{R_2}{R_1}\frac{V_{Cpd}}{V_{A1}}\ . \end{aligned} \tag{9}$$

Therefore, t_{VAR} depends on the values of R_1, R_2, C_{ramp} and R_{ramp}, as long as on the voltage at $A1$ and on the peak voltage between $A1$ and $A2$, i.e. the voltage V_{Cpd}.

From Figs. 2b and 5, it is apparent that the AOTSR must ensure that $v_{AR}\left(t\right)$ goes to zero during the conduction intervals of the primary side transistors (during $[0, dT_{sw}]$ and $[T_{sw}/2, T_{sw}/2 + dT_{sw}]$ in converters with symmetrically-driven transformers and during $[0, dT_{sw}]$ in converters from the Flyback family), to avoid overlapping. This is achieved through the reset transistor M_{reset}: assumming that the $reset$ terminal is connected to a voltage that goes high during the conduction intervals of the main transistors, both inputs of the comparator will be pulled low during such intervals. Note from Fig. 6 that the voltage at the negative input is slightly higher than the voltage at the positive input, due to the different forward voltage drop of each diode: V_- is pulled down to the forward voltage drop of the PN diode D_{reset-}, which is slightly higher than the forward voltage drop of the Schottky diode D_{reset+}, ensuring that $v_{AR}\left(t\right)$ is 0 whenever M_{reset} is

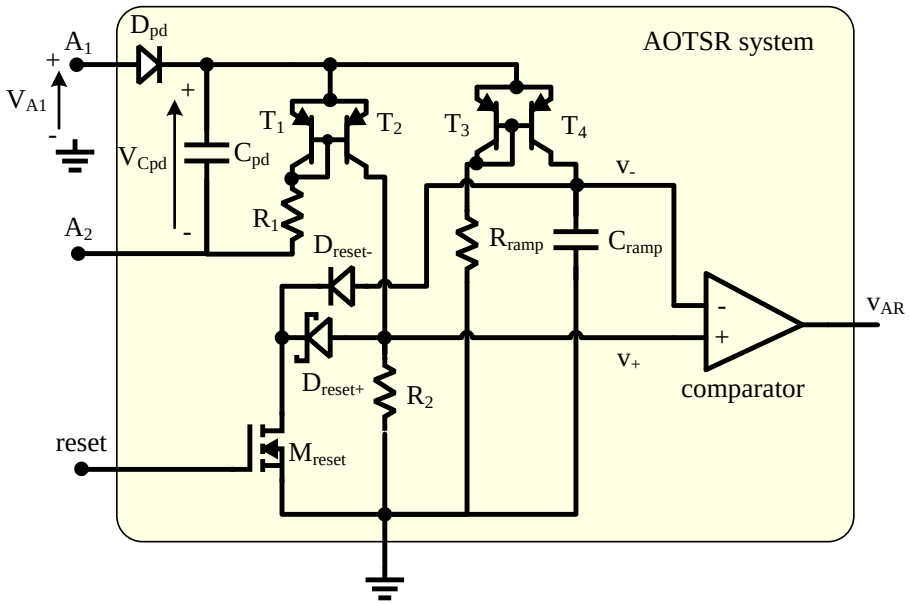


Figure 6. Circuit implementation of the AOTSR system.

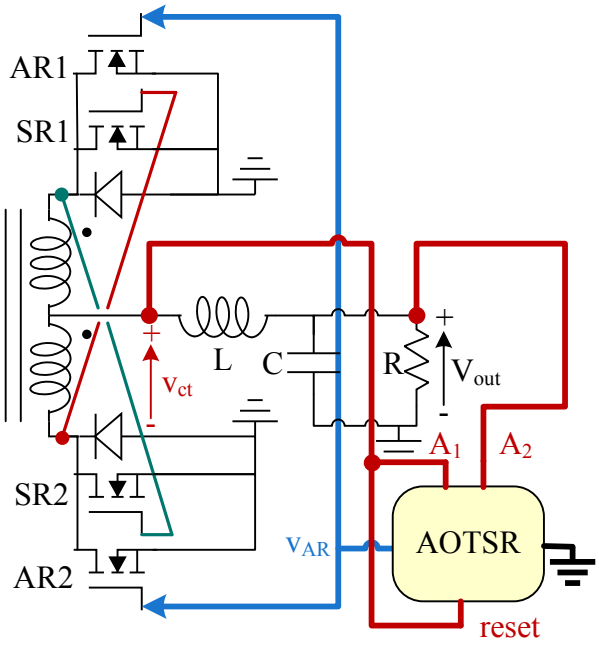


Figure 7. Connection of the proposed AOTSR system in a converter with a symmetrically-driven transformer.

activated. This reset mechanism guarantees that the proposed system causes no overlap, even in the presence of sudden changes of the duty cycle. Several alternatives are possible to avoid DCM operation of the proposed AOTSR; for instance, if the current through the rectifier becomes negative and at the same time V_{AR} is high, then V_{AR} can be immediately pulled low. This can be done using very few additional components.

A. Converters with symmetrically-driven transformers

Fig. 7 shows the proposed system in the case of converters with symmetrically driven transformers. A_1 and A_2 must be connected to the center tap of the transformer and to the output terminal, respectively. The $reset$ terminal is also connected to the center tap, thus reseting the AOTSR during the desired intervals. With the aforementioned connections, V_{Cpd} and V_{A1} are:

$$V_{Cpd} = V_{ct,peak} - V_{out} \tag{10}$$

$$V_{A1} = V_{ct,peak} \ . \tag{11}$$

Using (10), (11) and (1), (9) can be written as:

$$t_{\text{VAR}} = \frac{R_2}{R_1} R_{ramp} C_{ramp} \left(1 - 2d\right) \ . \tag{12}$$

Now choosing R_1, R_2, R_{ramp} and C_{ramp} as:

$$R_{ramp} C_{ramp} \frac{R_2}{R_1} = k \frac{T_{sw}}{2} \ , \tag{13}$$

k being a safety factor to ensure that no short circuits take place, (9) can be written as:

$$t_{\text{VAR}} = k \frac{T_{sw}}{2} \left(1 - 2d\right) \ . \tag{14}$$

Comparing (14) with (2), it is apparent that, with the aforementioned selection of the component values described by (13), the duration of the pulse can be made as close to the duration of the dead times as desired; in practice k will be chosen to be around 0.9 to avoid overlapping and at the same time maximize t_{VAR}. Furthermore, (14) yields the desired adaptive behavior: the higher the duty cycle, the shorter t_{VAR}. Fig. 8 shows the operating waveforms of the AOTSR for two different values of the duty cycle.

B. Converters from the Flyback family

Fig. 9 shows the proposed system in the case of a Flyback converter. In this case, A_1 and A_2 must be connected to the cathode of D and to the output, respectively. The $reset$ terminal is also connected to the cathode of D, again pulling

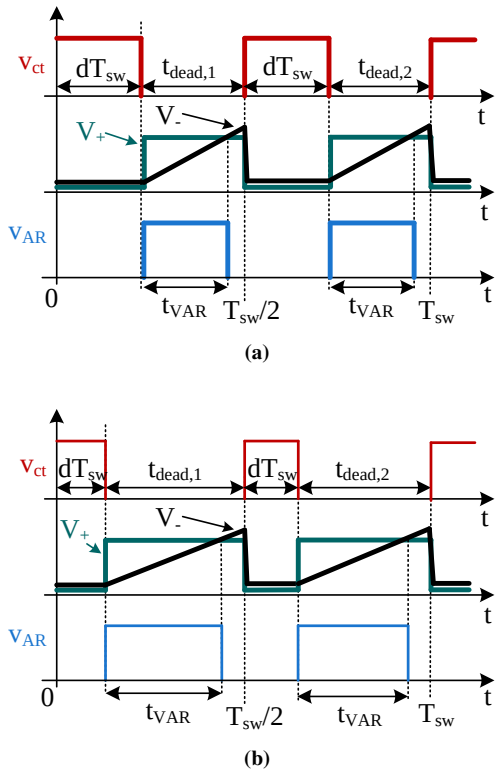


Figure 8. Operating waveforms of the AOTSR in a converter with a symmetrically driven transformer: (a) d ≈ 0.25; (b) d ≈ 0.15.

$v_{AR}(t)$ low during the desired intervals. With the aforementioned connections, V_{Cpd} and V_{A1} are:

$$V_{Cpd} = \frac{V_{in}}{n} \tag{15}$$

$$V_{A1} = \frac{V_{in}}{n} + V_{out} \ . \tag{16}$$

Using (15), (16) and (3), (9) can now be written as:

$$t_{\text{VAR}} = \frac{R_2}{R_1} R_{ramp} C_{ramp} (1-d) \ . \tag{17}$$

Now choosing R_1, R_2, R_{ramp} and C_{ramp} fulfilling:

$$\frac{R_2}{R_1} R_{ramp} C_{ramp} = k T_{sw} \ , \tag{18}$$

k being a safety factor to ensure that no short circuits take place, (9) can be written as:

$$t_{\text{VAR}} = k T_{sw} (1-d) \ . \tag{19}$$

Once again, it is apparent that, with the aforementioned selection of the component values, the duration of the pulse can be made as close to the duration of the diode conduction time as desired; in practice k will be chosen to be around 0.9 to avoid possible short circuits and at the same time maximize t_{VAR}. Equation (19) again yields the desired adaptive behavior: the higher the duty cycle, the shorter t_{VAR}. Fig. 10 shows the operating waveforms of the AOTSR for two different values of the duty cycle.

Figure 9 is also applicable to the isolated SEPIC converter, whereas the appropriate connections in the case of the isolated Zeta and Ćuk converters are shown in Fig. 11

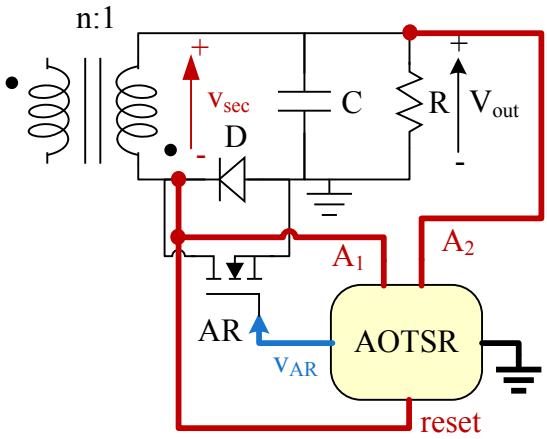


Figure 9. Connection of the proposed AOTSR system to a Flyback converter.

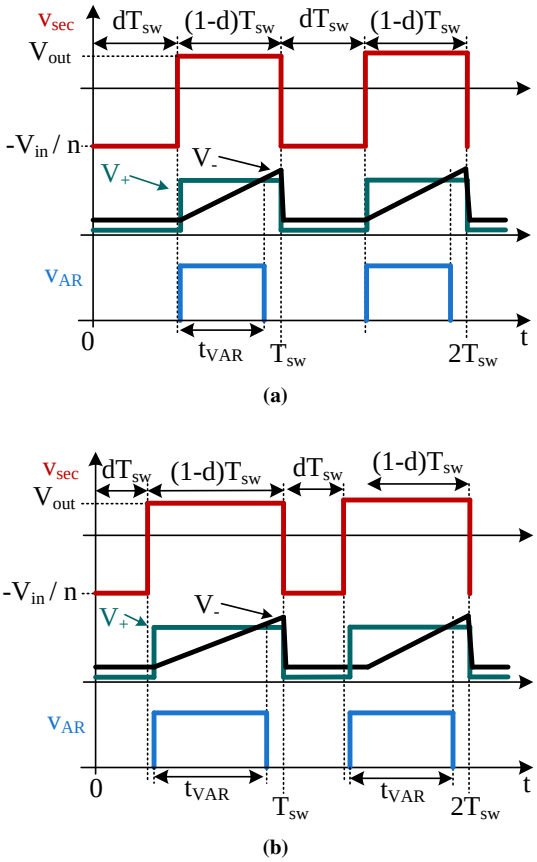


Figure 10. Operating waveforms of the AOTSR in the Flyback converter: (a) D ≈ 0.5; (b) D ≈ 0.3.

IV. Experimental Results

Two converters were used to test the proposed system. A 100 W Push-Pull converter was used to implement the AOTSR system in a converter with a symmetrically-driven transformer; a 50 W Flyback converter was selected to test the system in an isolated buck-boost derived topology. The results obtained are shown in the following sections.

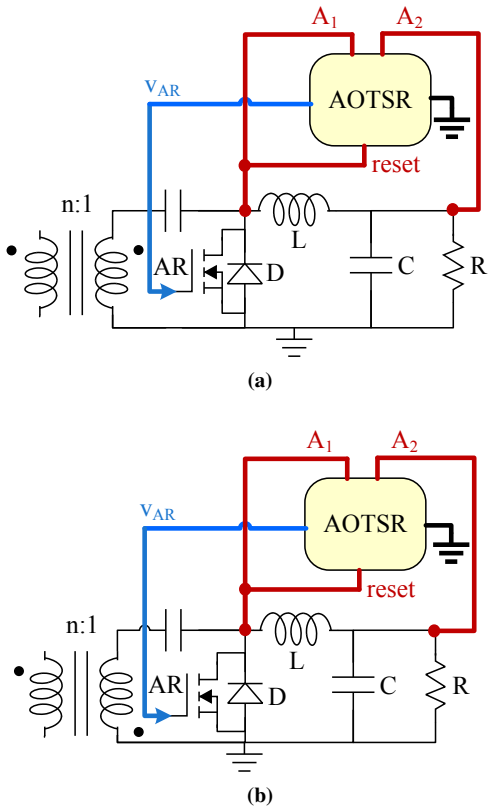


Figure 11. (a) AOTSR connections for an isolated Zeta converter; (b) AOTSR connections for an isolated Ćuk converter.

A. *100 W Push-Pull converter*

The main specifications of the Push-Pull converter are: $V_{in} = 18 - 36\ V$, $V_{out} = 3.3 - 5\ V$, $L = 3.3\ \mu H$ and $C = 120\ \mu F$. The transformer has three primary turns and one secondary turn in each winding, and the switching frequency is 115 kHz. IRL1404 MOSFETs are used as the main synchronous rectifiers $SR1$ and $SR2$; the same model is used for the auxiliar rectifiers $AR1$ and $AR2$. General purpose (but matched) transistors (BC557) are used as T_1, T_2, T_3 and T_4 in the AOTSR system. A fast response comparator (AD790) is also used: this is a high performance, expensive comparator, and much cheaper integrated circuits (as the TL3016 used in the following section) could be used. The auxiliar rectifiers are driven by an additional MOSFET driver, UCC27424, supplied from an unregulated voltage obtained from the transformer; according to the specifications of the converter, the supply voltage changed from 6 V ($V_{in} = 18\ V$) to 12 V ($V_{in} = 36\ V$). A higher drive voltage can be easily obtained from one of the secondary windings, whose peak voltage is equal to $2V_{ct}$, therefore providing a voltage ranging from 12 V to 24 V; a linear regulator is then required to avoid an excessive gate voltage. Table I summarizes the design of the AOTSR. To account for component tolerances, R_{ramp} has been replaced with a variable resistance to implement a conservative design ($k < 0.8$).

Fig. 12 shows the efficiency measured at different operating conditions, with and without the proposed system: it is apparent that the AOTSR noticeably increases the efficiency

Table I. Design parameters of the AOTSR for the Push-Pull converter.

$\frac{T_{sw}}{2}$ (μs)	k	R_1 (kΩ)	R_2 (kΩ)	R_{ramp} (kΩ)	C_{ramp} (nF)
4.35	0.8	5	5	3.9	1

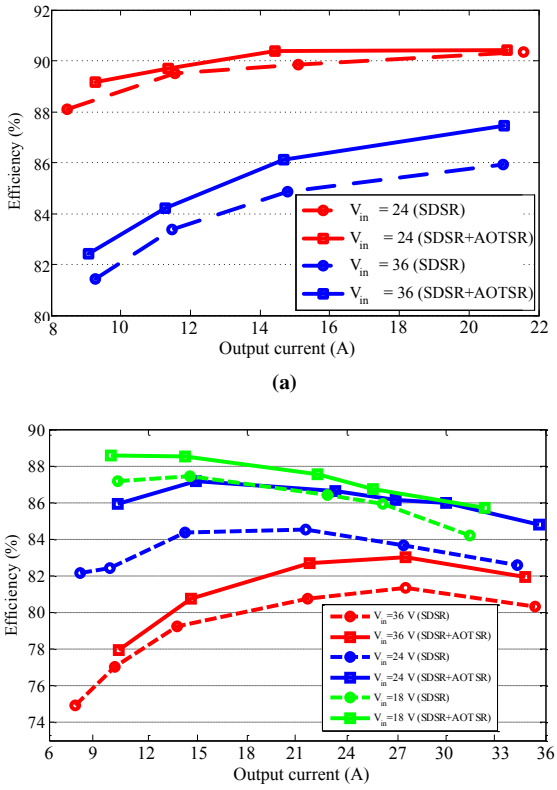
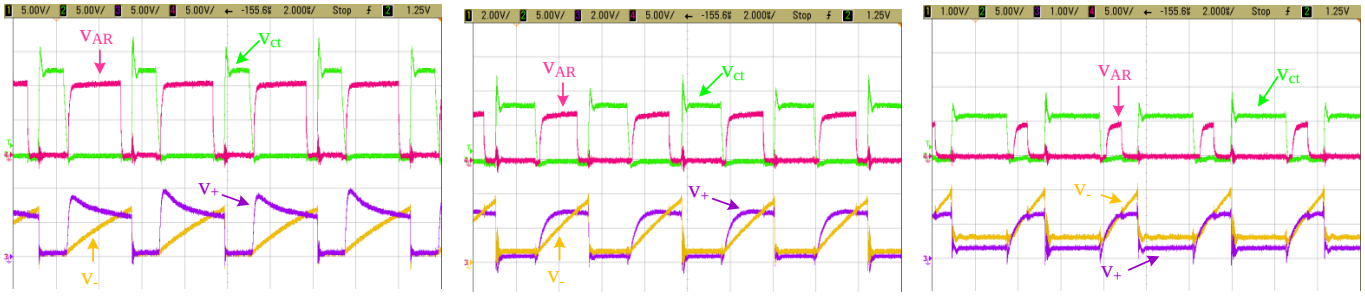


Figure 12. Measured efficiency with and without the proposed system: (a) $V_{out} = 5\ V$; (b) $V_{out} = 3.3\ V$.

regardless of the input and output voltages. The efficiency increase achieved is higher for $V_{in} = 36\ V$, i.e. when the conduction time of the auxiliar rectifier is longer. Fig. 13 shows several operating waveforms. It can be seen that the proposed system presents the expected adaptive behavior, changing t_{VAR} according to (14).

Figure 14 shows a sample operating waveform in detail, and Table II shows the values of the parameters highlighted in Fig. 14 for different operating conditions: t_{d1} and t_{d2} have to be long enough to guarantee that no overlapping takes place, disregarding of the operating conditions. t_{d1} is determined by the rising time of V_+ and by the delays introduced by the turn-off of M_{reset}, the comparator and the gate drive circuitry of the auxiliar rectifiers. The rising time of V_+ is in turn determined by R_1 and the equivalent capacitance at the positive input of the comparator. As overlapping is less likely to take place at the turn-on of the auxiliar rectifiers, the aforementioned delays and the rising time of V_+ should be minimized to maximize the efficiency improvement. Interval t_{d2} is determined by the value of k. The value of t_{VAR} is also shown in Table II, along with its relative lenght with respect to the dead times and the efficiency improvement achieved ($\Delta\eta$).



(a) (b) (c)

Figure 13. Experimental waveforms at $V_{out} = 3.3\ V$: (a) $V_{in} = 36\ V$; (b) $V_{in} = 24\ V$; (c) $V_{in} = 18\ V$.

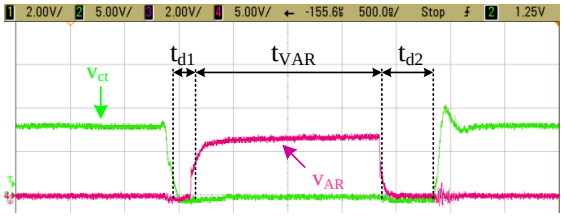


Figure 14. Detail of v_{AR} and v_{ct} in the Push-Pull converter and definition of several important paramenters.

Table II shows several interesting facts. Ideally, and according to (14), t_{VAR} should remain constant if the input and output voltages are fixed. However, due to nonidealities that have not been taken into account in the analysis (for instance, the voltage peak that appears in v_{ct}), the actual values of t_{VAR} might vary. The results shown in Table II demonstrate that t_{VAR} remains approximately constant for a given input voltage as expected, disregarding of the output power. Furthermore, both t_{d1} and t_{d2} change with the operating conditions, too. t_{d1} changes mainly because the rise time of V_+ depends on the input voltage. The higher t_{d1}, the lower the value of k with respect to the design value: if the variations of k were unacceptable in a certain design, a more accurate adjustment of the peak detector and the minimization of t_{d1} would be required. t_{d2} is one of the most important parameters, as it determines the appearance of overlap: it is apparent that it remains approximately constant in the whole operating range, which is the desired behavior. Finally, note that k remains slightly below its maximum design value.

Table II. Parameters highlighted in Fig. 14 for the Push-Pull converter ($V_{out} = 3.3\ V$).

V_{in} (V)	I_{out} (A)	t_{d1} (μs)	t_{VAR} (μs)	t_{d2} (μs)	$k = \frac{t_{\text{VAR}}}{(1-2d)\frac{T_{sw}}{2}}$ %	$\Delta\eta$ %
24	7.5	0.55	1.68	0.56	62.3	2.2
	15	0.55	1.7	0.52	65.3	2.8
	24	0.5	1.8	0.5	70.1	2.1
36	7.5	0.35	2.4	0.54	76	0.7
	15	0.35	2.2	0.7	70	1.1
	24	0.3	2.1	0.7	68.5	2.1

B. 50 W Flyback converter

The main specifications of the Flyback converter are: $V_{in} = 36 - 72\ V$, $V_{out} = 5\ V$ and $C = 470\ \mu F$. The transformer has 12 primary turns and 2 secondary turns; the switching frequency is 100 kHz. Two 12CWQ03 Schottky diodes are placed in paralell at the secondary side and an IRL1404 was used as the auxiliar rectifier, that is driven by an UCC27424. The supply voltage of the driver is obtained from V_{sec} using a peak detector and a simple, 5 V linear regulator. The same circuit described in section IV-A was used, except for the comparator. In this case a low cost, fast response TL3016 from Texas instruments is used. As the maximum supply voltage of the TL3016 is 5 V, slight modifications of the circuit in Fig. 6 are required: different values for the two resistors tied to T_1 and T_2 are selected to ensure that the voltage V_+ is never above 5 V, and the values of C_{ramp} and R_{ramp} are chosen to compensate this difference. Finally, to minimize the influence of the forward voltage drop of D_{reset-}, which can be noticeable when working with low voltage values, D_{reset-} is replaced by a Schottky diode and D_{reset+} is short-circuited. Table III summarizes the design of the AOTSR. Once again, a conservative design with $k < 0.8$ has been selected. In this case, the comparator cannot withstand more than 5 V at any of its inputs; thereby, the component values of the system have been selected to keep v_+ and v_- below such limit, as long as to fulfill (18). A small filter resistor was added to the peak detector to minimize the effect of the voltage spike that takes place in the Flyback converter.

Fig. 15 shows the efficiency of the converter measured with and without the proposed system. The Flyback converter achieved nearly 83 % efficiency using dissipative clamp and turn-off snubbers. With the AOTSR system the efficiency increased nearly 2.5 %, regardless of the input voltage. Note that the efficiency increase achieved is approximately constant in the whole input voltage range, unlike in the results presented in section IV-A; in this case the average current through the

Table III. Design parameters of the AOTSR for the Flyback converter.

T_{sw} (μs)	k	R_1 (kΩ)	R_2 (kΩ)	R_{ramp} (kΩ)	C_{ramp} (nF)
11.4	0.8	15	3.3	10	4.2

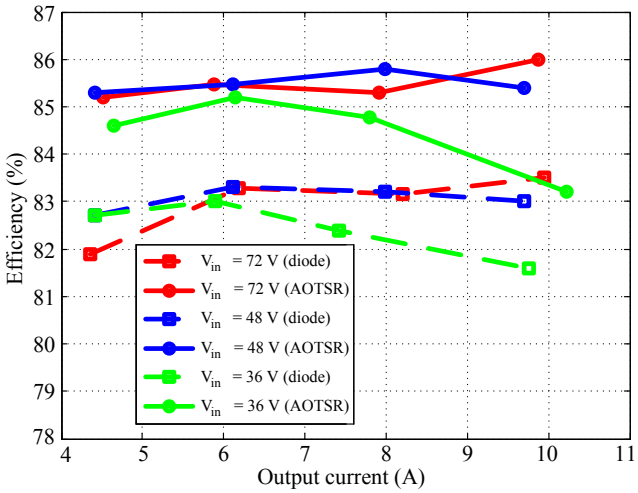


Figure 15. Measured efficiency with and without the proposed system at different operating conditions; the output voltage was $V_{out} = 5\ V$.

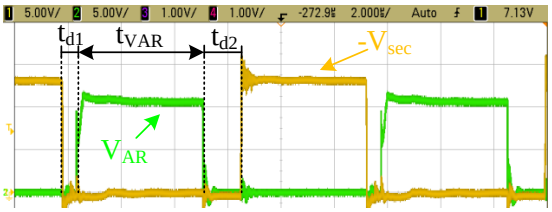


Figure 16. Detail of v_{AR} and v_{sec} in the Flyback converter and definition of several important parameters.

output diode only depends on the output power and does not change with the input voltage, causing the efficiency increase to remain approximately constant disregarding of the conduction time of the auxiliar rectifier.

Figure 16 shows a sample operating waveform in detail; the same parameters shown in Table II have been measured in the Flyback converter and are shown in Table IV, and the same considerations stated in Section IV-A over t_{d1} and t_{d2} can be applied here.

Similar conclusions to those obtained in the previous section can be stated according to the results shown in Table IV. Once again, variations of the actual values of t_{VAR} are small enough to be neglected for constant input and output voltages. t_{d1} varies due to the same reasons explained in the case of the Push-Pull converter. t_{d2} remains approximately constant in the whole operating range, ensuring that no overlap takes place. Finally, k remains slightly below its maximum design value, and changes according to the variations in t_{d1}.

V. Conclusions

A novel adaptive off-time synchronous rectification system has been presented in this paper. The system is especially suitable for isolated, low output voltage converters, as it uses only information from the secondary side of the transformer; this facts allows complex and sometimes unreliable pulse transmission systems required to transfer the control pulses to the secondary side when synchronous rectification is implemented. The proposed adaptive synchronous rectification system is applicable to converters with symmetrically-driven

Table IV. Parameters highlighted in Fig. 14 for the Flyback converter ($V_{out} = 5\ V$).

V_{in} (V)	I_{out} (A)	t_{d1} (μs)	t_{VAR} (μs)	t_{d2} (μs)	$k = \frac{t_{\text{VAR}}}{(1-d)\,T_{sw}}$ %	$\Delta\eta$ %
36	4	1	3.45	1.6	57.5	1.9
	6	1	3.45	1.6	58.2	2.2
	8	1	3.45	1.6	58.2	2.38
	10	0.9	3.5	1.65	59	2.2
48	4	0.64	4.9	1.5	71.6	2.3
	6	0.6	4.85	1.45	71	2.27
	8	0.56	4.85	1.4	71	2.5
	10	0.52	4.9	1.4	71.6	2.7
72	4	0.35	6.3	1.5	-	3.1
	6	0.3	6.25	1.55	78.3	2.19
	8	0.4	6.1	1.45	76.4	2.14
	10	0.45	6	1.5	76	2.5

transformers (Half and Full-bridges and Push-Pull) and to converters from the isolated buck-boost family (Flyback, isolated SEPIC, Ćuk and ZETA). The proposed system is simple, inexpensive and can easily be implemented in an integrated circuit. It has been demonstrated that the system is capable of increasing up to a 3 % the efficiency of a 100 W Push-Pull converter with SDSR, and nearly 2.5 % the efficiency of a 50 W Flyback converter with Schottky diodes. Furthermore, it can reliably work in a wide range of operating conditions due to its adaptive behavior.

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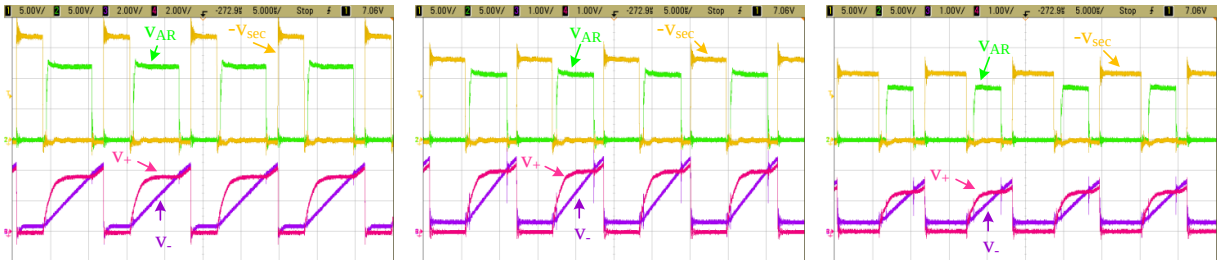

(a) **(b)** **(c)**

Figure 17. Experimental waveforms at $V_{out} = 5\ V$. V_t refers to the : (a) $V_{in} = 72\ V$; (b) $V_{in} = 48\ V$; (c) $V_{in} = 36\ V$.

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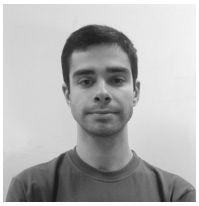

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