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Characterization of prototype LSST CCDs

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ABSTRACT

We present characterization methods and results on a number of new devices produced specifically to address LSST's performance goals, including flatness, QE, PSF, dark current, read noise, CTE, cosmetics, and crosstalk. The results indicate that commercially produced, thick n-channel over-depleted CCDs with excellent red response can achieve tight PSF at moderate applied substrate bias with no evidence of persistent image artifacts. We will also report ongoing studies of mosaic assembly techniques to achieve chip-to-chip co-planarity, high fill factor, and thermal stability.

Keywords: CCD, LSST, quantum efficiency, point spread function

1. INTRODUCTION

The ambitious science goals of the Large Synoptic Survey Telescope (LSST) will be achieved in part by a wide-field imager that will achieve a new level of performance in terms of area, speed, and sensitivity. The instrument performance is dominated by the focal plane sensors, which are now in development. These new-generation sensors will make use of advanced semiconductor technology and will be complemented by a highly integrated electronics package located inside the cryostat. A test laboratory has been set up at Brookhaven National Laboratory (BNL) to characterize prototype sensors and to develop test and assembly techniques for eventual integration of production sensors and electronics into modules that will form the final focal plane.

As described in [1], the key requirements for LSST sensors are wideband quantum efficiency (QE) extending beyond 1μ m in the red, control of point spread function (PSF), and fast readout using multiple amplifiers per chip operated in parallel. In addition, LSST's fast optical system (f/1.25) places severe constraints on focal plane flatness. At the chip level this involves packaging techniques to minimize warpage of the silicon die, and at the mosaic level careful assembly and metrology to achieve a high coplanarity of the sensor tiles.

In view of the long lead time to develop the needed sensor technology, LSST undertook a study program with several vendors to fabricate and test devices which address the most critical performance features [2]. The remainder of this paper presents key results of this study program. Section 2 summarizes the sensor requirements and the results of design optimization studies, and Section 3 presents the sensor development plan. In Section 4 we describe the test bench at BNL. Section 5 reports measurement results obtained to date on devices fabricated by several vendors. Section 6 presents a summary of the paper and an outlook for the future work.

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2. SENSOR REQUIREMENTS AND DESIGN OPTIMIZATION

2.1 Requirements

The technology advances needed for LSST sensors are listed in Table 1 below.

Table 1 LSST sensor requirements

Science driver	Technology Advance	Criterion		
Broadband, high QE	Thick silicon, fully depleted	QE(1000nm) > 30%		
	Transparent back contact	QE(400nm) > 40%		
Seeing-limited image quality	Low charge diffusion	< 3.2µm rms		
	Small pixel size	10µm (0.2")		
	Low read noise	< 5 e- rms		
	Low dark current	< 2 e-/pix/s		
	Low persistence	< 10 ⁻⁴		
	High full well	> 90,000 e-		
	Flat silicon surface	< 5µm p-v		
	TTP-controlled package	< 6.5µm over raft		
High throughput	Multiport output	$(4K)^2$, 16 output		
	High fill factor die & pkg	> 93%		

2.2 Optical

To balance the tradeoffs between red QE and charge diffusion, an optimization study was performed [1]. Increasing the silicon thickness improves the QE beyond 950nm, while it causes increased charge diffusion which broadens the PSF in the u.g.r.and I bands. An illustration of this tradeoff is shown in Figure 2, where the contribution to PSF at 550nm from charge diffusion is plotted versus averaged QE in the y-band. Note that temperature plays a role in this tradeoff - higher temperatures improve the red QE while having minimal effect on diffusion.



Figure 1 Effect of sensor thickness on point spread function and y-band QE at three temperatures: 140K (diamonds), 180K (triangles), and 220K (circles). Thickness range is 50µm (points at lower left) to 250µm (upper right) in 50µm steps.

2.3 Electrical

Another tradeoff involves the electrical performance of the focal plane. Survey speed is decreased by the time taken to read out the focal plane after each exposure, but increasing the pixel rate degrades read noise. To meet the goal of 2s readout time for the full focal plane while keeping the read noise below 5 electrons rms, the sensor is divided into segments read out in parallel. In the tradeoff analysis the detector size is assumed to be 4K X 4K, the readout time is

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constrained to be 2s, and we estimate the noise performance of the detector based on a simple noise model of the source follower transistor (Figure 2a). The choice of 16 segments (1Mpix per segment) and 250kpix/s provides the necessary performance. The arrangement of the segments can be chosen to provide a large contiguous imaging area, as shown in the CCD conceptual layout in Figure 2b.



Figure 2: (a)Estimated read noise for a 4K x 4K sensor constrained to 2s readout time. Increasing the segmentation allows the clock rate, and hence the read noise, to be reduced. Noise estimates are based on CCD output transistor properties with three values of sense node capacitance. (b) Proposed layout of a 16-fold segmented, 4K x 4K CCD for fast, low-noise readout.

2.4 Mechanical

A crude defocus model provides limits on the flatness tolerance. Figure 3 shows the normalized PSF as a function of displacement from best focus. The proposed allocation of flatness tolerance for the sensor surface, raft of nine sensors, and full focal plane of 189 sensors is shown.



Figure 3: Estimated defocus for 550nm light, with allocation to sensor, raft, and full focal plane. A 3.2µm rms Gaussian PSF at optimum focus is assumed.

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2.5 Reference design

A reference design for LSST sensors has been proposed based on the preceding design studies. As shown in Figure 4, it is a 4K x 4K CCD fabricated on 100 μ m-thick, p-type silicon with a resistivity in the range 5 – 10 k Ω -cm. The CCD imaging area is divided into sixteen, 512x2048 pixel, independently read out segments. Each segment has a low power, low noise source follower amplifier. An independent substrate bias voltage, applied from the front side of the device, biases the thin conductive window on the backside and results in a fully-depleted substrate under the imaging area with an average electric field of 5 – 10 kV/cm. Guard rings around the periphery provide a gradual lateral voltage gradient to the silicon die edge, which is at the same potential as the entrance window. Care must be taken to ensure that p-implanted regions on the frontside are narrow enough to avoid forming conductive channels to the backside. Bond pads are arranged on two sides of the die and connect to traces on the package, which may incorporate bussing of common clock and bias signals.



3. SENSOR DEVELOPMENT PLAN

The LSST camera collaboration is about halfway through a three-phase sensor technology development program. Starting in 2005, contracts were awarded to three vendors to address the most pressing technology challenges [2]. A matrix showing the goals of the study contracts is shown in Table 2. With the funding available, this program emphasized the demonstration of thick, high resistivity, fully-depleted sensors. Less emphasis was given to high fill factor die layout, packaging, and flatness.

Table 2: Vendor study program.

Vendor	Sensor	Thick hi-rho Si	10µm pixel	Large format	Segmented	Flat Silicon	Buttable Pkg	Sensors delivered
A	ССД	x						5
в	CCD	x	x	x	x			2
с	pin/CMOS	X	x	x	x		· · ·	1

Vendors A and B developed CCDs while Vendor C provided a large-format silicon p-i-n/CMOS hybrid. The p-in/CMOS hybrid sensor has been tested and results are reported in [3]. The interest in p-i-n/CMOS technology for LSST is now being focused on guide sensors, where fast window-mode readout is advantageous. The remainder of this paper will report the initial results of tests on the study program's CCD sensors.

Following the study program, a request for proposals for prototype sensors meeting all LSST specifications has been issued in early 2008. In addition to meeting performance goals, the prototype phase will emphasize yield and

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reproducibility to minimize risk of cost and schedule overruns in procurement. During prototype development the LSST collaborating institutions will prepare test facilities having throughput compatible with the expected production rate of 10-20 sensors per month. Development of the production-ready prototype is expected to take two years, after which procurement of the full complement of science sensors will begin.

4. TEST FACILITY

A CCD test facility has been constructed in the Instrumentation Division of Brookhaven National Laboratory. Its primary instrumentation consists of:

- Liquid nitrogen cooled Dewar with 4" window, temperature controlled stage for mounting CCDs in a variety of mechanical packages. A 10µCi ⁵⁵Fe source, in the form of a 3mm disk, is mounted on a stepper-motor actuated arm inside the Dewar which can position the source over the center of the CCD or behind a shield.
- Monochromatic flat field illumination provided by a Xe lamp, grating monochromator, and 12" integrating sphere with input, monitor, and output ports.
- Long working distance, high N.A. microscope objective mounted on a translation stage, which images a 4µmcore optical fiber onto the CCD [4]. For 650nm light the spot size on the CCD is about 1.2µm Gaussian rms.
- Non-contact flatness measurement system consisting of an optical confocal displacement sensor (Keyence LT-9030) mounted on a 200mm-travel xy translation stage. The accuracy of the flatness measurement is presently limited by the nonidealities of the stage to about 2µm.

All testbench apparatus can be controlled over RS-232 or GPIB.

Our CCD controller is based on the control and readout electronics developed for the MMT Megacam [5]. For our measurements the readout rate was fixed at 156 kpix/s. Communication with the Linux PC is by optical fiber interface [6].

We use the RTS-2 observatory manager software [7] to provide a framework by which the user can specify a sequence of measurement runs, using a flexible scripting language. Using RTS-2, we have developed scripts that perform a complete optical and electrical characterization of the CCD under test. The run set (for measurement at three temperatures) generates about 850 image files and runs unattended for about 6 - 8 hours, typically overnight. Automated analysis procedures perform data reduction and various data quality checks.

Quantum efficiency is determined by taking flat field exposures over a range of wavelengths from 300 - 1100nm and subtracting a mean dark frame from each. The QE is then defined as

$$QE(\lambda,T) = \frac{\langle S_{ADU}(\lambda,T) \rangle}{g(T)} * F_{ref}(\lambda) * R(\lambda)$$

Where $\langle S_{ADU} \rangle$ is the signal (in ADU per pixel) averaged over a large defect-free area of the CCD, g(T) is the electronic gain in ADU per electron, F_{ref} is the photon flux measured by the monitor photodiode in the integrating sphere, and R is the predetermined ratio of flux at the CCD location to flux at the monitor photodiode. The factor g is measured by finding the K_{α} and K_{β} peaks in the spectrum of xray hits from ⁵⁵Fe, or by the slope of the photon transfer curve (variance vs. mean). The ratio R is determined by placing a calibrated photodiode at the CCD location, scanning the monochromator over the wavelength range 300 – 1100nm, and recording the ratio of flux in the photodiode at the CCD position to that in the integrating sphere. Reproducibility of the QE measurement is below 1% in the wavelength range 400-900nm. Absolute accuracy is limited by the histogram-fitting procedure in determining g(T), and by uncertainty in the temperature dependence of the soft x-ray energy required to produce an electron-hole pair in silicon. We do not have a firm estimate of these systematic errors, but believe them to be good to better than 5%.

For PSF measurements, we use the virtual knife edge technique described in [8], [9]. The spot produced by the point projector is repeatedly imaged as it is scanned in 2µm steps in x or y. Integrating the flux in a fixed group of pixels through which the spot travels allows one to estimate the size and shape of the point spread function. We fit the VKE profile to a Gaussian, and subtract the predetermined optical spot size quadratically to get an estimate of the PSF due to charge diffusion effects in the CCD.

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Figure 5: (a) x-ray histogram from 55 Fe, with fit to K_{α} and K_{β} peaks at 470 and 520 ADU. (b) Virtual knife edge scan, showing integral and differential fits.

5. TEST RESULTS ON STUDY CONTRACT CCDS

5.1 Description of CCDs delivered

Five devices from vendor A have been received and tested at BNL. Devices received early in the study program received less rigorous testing than those received later, as test equipment and analysis routines underwent improvement. Vendor B delivered two devices, but these have not yet been tested at BNL. Both vendors supplied operating parameters and test data for their CCDs. Table 3 is a summary of the characteristics of each device.

Vendor	Device	Thickness	Pixel size	Format	Segmentation	Amplifier	Comment
A	106-03	100µm	13.5µm	2K x 512	1 or 2	1-stage	"setup" device
A	106-05	100µm	13.5µm	2K x 512	1 or 2	1-stage	
A	106-06	100µm	13.5µm	2K x 512	1 or 2	2-stage	
A	106-07	100µm	13.5µm	2K x 4.6K	1 or 2	2-stage	Testing incomplete
A	107-01	150µm	13.5µm	2K x 512	1 or 2	2-stage	Different process lot
В	108-01	100µm	10µm	4K x 4K	16	1-stage	
В	108-02	100µm	10 <u>µ</u> m	4K x 4K	16	1-stage	

5.2 Flatness

Four of the five devices from Vendor A have been measured for surface flatness, and the results are shown in Figures 6 and 7. The contour plots give the residuals from the best-fit plane to data taken on a 1×1 mm grid. Below each contour map is a graph showing the cumulative distribution of residuals (absolute values shown). These devices show a characteristic bowing, with the large device being center-high and the smaller devices center-low. The departure from flatness is within LSST specifications over more than 96% of the imaging area for these devices. One of Vendor B's devices has been measured and it exhibits a poorer flatness characteristic, with an rms deviation from plane about seven

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SPIE USE: DB Check, Prod Check, Notes:



Figure 8: Dark images ("setup" device 106-03) and dark current vs temperature (study contract deliverable device 106-06). Circles: mean dark current. Squares: fraction of pixels with > 2e-/pix/s. LSST spec is for less than .05% of pixels to have 2e-/pix/s.

5.4 Amplifier gain, linearity, and full well

Figure 9 shows the response of sensor 106-06 to flatfield illumination at increasing exposure times. The full well (Fig. 9(a)) is about 300,000 electrons. Fig. 9(b) shows that the response is linear to within 0.5% from zero to 90% of full well.



Figure 9 (a) Response to flatfield illumination. (b) Slope normalized to the value at 100s. Response is linear up to 90% of full well.





Figure 10. Quantum efficiency for 100µm-thick devices biased at full depletion. Triangles are LSST requirements. Measurements supplied by vendors.

In Figure 11 we show the quantum efficiency of 100 and 150µm-thick devices from Vendor A. For these devices we have also compared the measured QE to values predicted from a model that takes into account the absorption coefficient of silicon at -70C from [10], the properties of the antireflection coating determined by ellipsometry, and an assumed dead layer of 6nm at the entrance window.



Figure 11: Measured and modeled quantum efficiency for Vendor A devices 106-06 (100µm thick) and 107-01 (150µm thick). Measurements made at BNL.

5.6 Point spread function

The point spread function measured by the virtual knife edge technique is shown in Fig. 12 for two samples from Vendor A. Data for both samples was taken at 163K. By fitting the low-voltage portion of the curve the doping concentration, silicon thickness, and junction potential can be determined to be $4.1 \times 10^{12} \text{ cm}^{-3}$, $95 \mu \text{m}$, 18V for sample 106-05 and

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2.1x10¹²cm⁻³, 150µm, 18V for sample 107-01 respectively. As the voltage is made more negative the CCDs become fully depleted and the PSF is determined by the diffusion of electrons as

$$\frac{\sigma}{d} = \sqrt{2D_T t_{dr}} ,$$

where d is the silicon thickness, D_T is the transverse diffusion coefficient, and t_{dr} is the drift time. Fig. 12 shows two curves for the fully-depleted PSF based on the known velocity-field relation for electrons in high-purity silicon [11]. The smaller PSF values assume that the transverse diffusion coefficient is suppressed at high fields according to the model of [12]. We are investigating alternative measurements of PSF using x-ray cluster size and cosmic ray track profiles to help understand the discrepancy between the VKE results and theory. Initial results from these new techniques show somewhat smaller PSF, in better agreement with the theory.



Figure 12: Point spread function measured by the virtual knife edge technique for samples 106-05 (left) and 107-01 (right).

5.7 Image persistence

One device from Vendor A was tested for image persistence. A point source of red light was projected onto the surface of the CCD and the intensity and exposure time adjusted to produce about 1/3 of full well in the brightest pixel. The exposures were repeated sixteen times without moving the spot, then an image was taken immediately with the source turned off. As shown in Figure 13, image persistence was less than 0.03%, with the measurement limited by signal to noise.





5.8 Mosaic assembly

As discussed in Section 2, LSST's fast optics require exceptional flatness of the mosaic focal plane. We experimented with a method similar to that described in [13] to adjust the tilts of dummy sensors on a prototype raft baseplate. The dummy sensors were assembled onto the raft with 3-point spacers whose heights could be adjusted by machining or

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lapping. Each trial assembly was scanned with the confocal displacement sensor, tilts measured, and spacers adjusted to make all surfaces coplanar. Initial tests using this approach resulted in overall flatness of 11 microns peak-to-valley, somewhat less than the LSST requirement. Figure 14 shows the progress of one series of adjustment trial assemblies. Further tests and alternative methods of planarization are being investigated.



Figure 14: Flatness of dummy sensor mosaic adjusted using machined spacers. Solid points: peak-to-valley variation of height over support points. Triangles: flatness of full mosaic.

6. SUMMARY AND OUTLOOK

The LSST sensor study program has been an important step towards development of the advanced sensors needed to achieve the survey's ambitious science goals. Vendors participating in the study program have demonstrated viable approaches to producing devices having extended red response with 100µm-thick, fully-depleted silicon; transparent back window contact; low dark current; negligible image persistence; high full well; flat silicon surface; and multiport output for fast readout. A characterization laboratory at BNL with fully automated image acquisition and analysis has verified the performance characteristics of the devices. The collaboration now plans to work with vendors to develop a full prototype meeting all critical LSST specifications that will allow procurement to begin in 2011.

7. ACKNOWLEDGEMENTS

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