THESIS FOR THE DEGREE OF LICENTIATE OF ENGINEERING

Operation and control of cascaded H-bridge converter for STATCOM application

EHSAN BEHROUZIAN

Department of Energy and Environment
CHALMERS UNIVERSITY OF TECHNOLOGY
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EHSAN BEHROUZIAN

Division of Electric Power Engineering
Department of Energy and Environment
Chalmers University of Technology
SE–412 96 Gothenburg
Sweden
Telephone +46 (0)31–772 1000

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To my family

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EHSAN BEHROUZIAN
Department of Energy and Environment
Chalmers University of Technology

Abstract

In the last decade, particular attention has been paid to the use of Modular Multilevel Converters (MMC) for grid applications. In particular, for STATCOM applications the phase leg of the converter is constituted by a number of single-phase full-bridge converters connected in cascade (here named Cascaded H-Bridge, CHB, converter). This multilevel converter topology is today considered the industrial standard for STATCOM applications and has replaced other converter topologies, mainly due to its small footprint, high achievable voltage levels (allowing transformer-less operation), modularity and reduced losses. However, there are still areas of research that need to be investigated in order to improve the performance and the operational range of this converter topology for grid-applications. The aim of this thesis is to explore control and modulation schemes for the CHB-STATCOM, both under balanced and unbalanced conditions of the grid, highlighting the advantages but also the challenges and possible pitfalls that this kind of topology presents for this specific application.

The first part of the thesis is dedicated to the two main modulation techniques for the CHB-STATCOM: the Phase-Shifted Pulse Width Modulation (PS-PWM) and the Level-Shifted PWM (LS-PWM) with cells sorting. In particular, the focus is on the impact of the adopted modulation on the active power distribution on the individual cells of the converter. When using PS-PWM, it is shown that non-ideal cancellation of the switching harmonics leads to a non-uniform active power distribution among the cells and thereby to the need for an additional control loop for individual DC-link voltage balancing. Theoretical analysis proves that a proper selection of the frequency modulation ratio leads to a more even power distribution over time, which in turns alleviates the role of the individual balancing control. Both PS-PWM and cells sorting schemes fail in cell voltage balancing when the converter is not exchanging reactive power with the grid (converter in zero-current mode). To overcome this problem, two methods for individual DC-link voltage balancing at zero-current mode are proposed and verified.

Then, the thesis focuses on the operation of the CHB-STATCOM under unbalanced conditions. It is shown analytically that regardless of the configuration utilized for the CHB-STATCOM (star or in delta configuration), a singularity exists when trying to guarantee balancing in the DC-link capacitor voltages. In particular, it is shown that the star configuration is sensitive to the level of unbalance in the current exchanged with the grid, with a singularity in the solution when positive- and negative-sequence currents have the same magnitude. Similar results are found for the delta configuration where, in a pure duality with the star configuration, the system is found to be sensitive to the level of unbalance in the applied voltage. The presence of these singularities represents an important limit of this topology for STATCOM applications.

Index Terms: Modular Multilevel Converters (MMC), cascaded H-bridge converters, STATCOM, FACTS.

Acknowledgments

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Ehsan Behrouzian
Gothenburg, Sweden
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List of Acronyms

HVDC	High Voltage DC
FACTS	Flexible AC Transmission System
DG	Distributed Generation
SVC	Static Var Compensator
VSC	Voltage Source Converter
STATCOM	STATic synchronous COMpensator
NPC	Neutral Point Clamped
ANPC	Active Neutral Point Clamped
CCC	Capacitor Clamp Converter
MMC	Modular Multilevel Converter
CHB	Cascaded H-Bridge
PWM	Pulse Width Modulation
PS-PWM	Phase shifted PWM
THD	Total Harmonic Distortion
LS-PWM	Level Shifted PWM
PD-PWM	Phase Disposition PWM
POD-PWM	Phase Opposition Disposition PWM
APOD-PWM	Alternate Phase Opposition Disposition PWM
SVM	Space Vector Modulation
SHE	Selective Harmonic Elimination
SHM	Selective Harmonic Mitigation
NVC	Nearest Vector Control
NLC	Nearest level Control

H-PWM	Hybrid PWM
MPC	Model Predictive Control
SRF	Synchronous Reference Frame
PR	Proportional Resonant
TSO	Transmission System Operators
DSP	Digital Signal Processing
FPGA	Field Programmable Gate Array
PLL	Phase Locked Loop
LPF	Low Pass Filter
MAF	Moving Average Filter
DCM	Distributed Commutations pulse-width Modulation
DSC	Delayed Signal Cancellation
DVCC	Dual Vector Current Control
CC	Current Controller
PCC	Point of Common Coupling
KVL	Kirchhoff’s Voltage Law

Contents

Chapter 1

Introduction

1.1 Background and motivation

Interconnected transmission systems are complex and require careful planning, design and operation. The continuous growth of the electrical power system, as well as the increasing electric power demand, has put a lot of emphasis on system operation and control. These topics are becoming more and more of interest, in particular due to the recent trend towards restructuring and deregulating of the power supplies [1][2]. It is under this scenario that the use of High Voltage Direct Current (HVDC) and Flexible AC Transmission Systems (FACTS) controllers represents important opportunities and challenges for optimum utilization of existing facilities and to prevent outages [2][3].

Typically, FACTS devices are divided into two main categories: series-connected and shunt-connected configurations [2][3]. At the actual stage, shunt-connected FACTS devices are dominating the market for controllable devices, mainly due to the inherited reactive characteristic of series capacitors and to the complications in the protection system. Shunt-connected reactive power compensators are available both based on mature thyristor-based technology (named Static Var Compensator, SVC) and on Voltage Source Converter (VSC) technology, also known under the name of STATic COMpensator (STATCOM). The thyristor-based technology is today the preferred option for installations having high-power ratings (typically above a few hundreds of MVar) [2]. On the other hand, the VSC technology is the most suitable choice when high speed of response or small footprint is needed. Furthermore, the use of VSC technology allows low harmonic pollution in the injected/absorbed current as compared with the SVC. These items, together with a higher operational flexibility and good dynamic characteristics under various operating conditions (for example, large variations in the short-circuit strength of the grid at the connecting point), indicate that the VSC technology is qualitatively superior relative to the thyristor-based SVC for static shunt compensator. Although today the STATCOM is more expensive than the SVC, its technical benefits together with the advancements in the technology are slowly leading to a shift from the thyristor-based to the VSC-based technology, similarly to the ongoing process in the HVDC area.

STATCOMs have been widely applied both in regional and distribution grids, mainly to miti-

gate power quality phenomena [4], and at transmission and sub-transmission level for voltage control, load shedding and power oscillations damping [2–4]. Furthermore, the STATCOM can be utilized in renewable-based power plants, mainly for grid-codes fulfillment and to allow fast reactive power compensation [5]. In case of renewable-based power plants, an interesting feature of the STATCOM is the possibility of incorporating an energy storage to the DC side of the VSC, thus allowing temporary active power exchange (for example, to limit power fluctuations).

The use of high-performance and cost-effective high power VSCs is a prerequisite for the realization of a STATCOM. Up to some years ago, the implementation of VSCs for high-power applications was difficult due to the limitations in the semiconductor devices. Typical voltage ratings for semiconductors are between 3 kV and 6 kV, which represent only a small fraction of the system rated voltage. For this reason, series-connection of static switches was needed in the VSC design for FACTS applications. Furthermore, the need to keep down the power losses has severely limited the level of the switching frequency that could be used in actual installations, leading to relatively large filtering stages. For these reasons, in the last decades multilevel converters for high-power application have gained more and more attention [6]. Among the multilevel VSCs family, the modular configurations such as Cascaded H-Bridge (CHB) converters seems as one of the most interesting solutions for high-power grid-connected converter [7].

Although CHB converter is an attractive solution for the implementation of FACTS devices, challenges still exist both from a control and from a design point of view. In the recent years, both manufacturers and researches have paid high effort to improve the control and the modulation of this converter topology. For the latter, Phase-Shifted Pulse Width Modulation (PS-PWM) [8] and the cells sorting algorithm [9, 10] has been extensively investigated in the literature. However, not sufficient attention has been given to the investigation of the different harmonic components that are generated when using PS-PWM and their impact on the system performance, in particular in case of non-ideal conditions of the system.

In [11], the use of a non-integer frequency modulation ratio (defined as the ratio between the frequency of the carrier and the grid frequency) is investigated. This work mainly focuses on the interaction between the cell voltage carrier harmonics and the fundamental component of the arm current. However, in case of CHB converters with reduced number of cells (such as for STATCOM applications), carrier harmonics in the current must also be taken into account. Furthermore, [11] does not provide any guideline for the reader on the selection of the frequency modulation ratio when trying to minimize the DC voltage divergence.

Another challenge regarding the CHB-STATCOMs is their control under unbalanced conditions. In particular, in case of star-connected CHB-STATCOM, when the system is exchanging negative-sequence current with the grid a zero-sequence voltage must be introduced in the output phase voltage of the converter to guarantee capacitor balancing [12–15]. On the other hand, the delta configuration allows negative-sequence compensation by letting a zero-sequence current circulate inside the delta [16–18].

In the work presented in [19][20], the star-connected CHB is considered as the most suitable configuration for positive-sequence reactive power control, typically for voltage regulation purpose and, more in general, for utility applications; on the other hand, delta configuration is considered to be the best solution for applications where negative-sequence is required, as it is

the case for industrial applications (for example, flicker mitigation).

However, requirements from Transmission System Operators (TSOs) are changing and start to demand negative-sequence injection capability for the converters connected to their grid [21]. Furthermore, the delta configuration can present limitations in injecting negative-sequence current in case of weak grids, where both load current and voltage are unbalanced, or under unbalanced fault conditions [20]. For this reason, it is of high importance to investigate the limits in terms of negative-sequence compensation for this kind of configurations.

1.2 Purpose of the thesis and main contributions

The aim of this thesis is to explore control and modulation schemes for the CHB-STATCOM, both under balanced and unbalanced conditions of the grid, highlighting the advantages but also the challenges and possible pitfalls that this kind of topology presents for this specific application.

Based on the described purpose, the following specific contributions can be identified:

- Control of CHB-STATCOMs at zero-current mode: It is shown that although existing approaches for individual DC-link voltage control are able to provide an appropriate voltage control, they are not able to provide a proper DC-link voltage control when the converter is operated at zero-current mode. Two methods for individual DC-link voltage balancing at zero-current mode are proposed and analyzed. The first method is based on a modified sorting algorithm and the second method is based on DC-link voltage modulation. Using the proposed methods, proper individual DC-link voltage balancing is achieved at zero-current mode.

- Investigation of Phase-Shifted PWM: It is shown that poor cancellation of harmonics of Phase-Shifted PWM (PS-PWM) leads to non-uniform power distribution among cells. Theoretical analysis shows that by proper selection of the frequency modulation ratio, a more even power distribution among the different cells of the same phase leg can be achieved, which alleviates the roll of the individual DC-link voltage control.

- Control in case of unbalanced conditions: Zero-sequence voltage/current injection is utilized for the control of CHB-STATCOMs under unbalanced condition. It is shown that a singularity in the solution of the zero-sequence component exists, which in turn limits the operational range of these converters under unbalanced conditions. The singularity in the delta configuration occurs when the positive- and negative-sequence components of the voltage at the converter terminals are equal, while for the star it is governed by the equality between the positive- and the negative-sequence component of the injected current. In addition to the amplitudes, the phase angles of currents in star and voltage in delta will highly impact the sensitivity of the converter. For the star configuration, the highest demand on the zero-sequence voltage occurs when the three-phase positive-sequence currents are aligned with the negative-sequence tern; on the contrary, the lowest demand on

the zero-sequence component occurs when the two terns are in phase opposition. Analogue results hold for the delta case.

The theoretical outcomes and control algorithms are verified both analytically and through dynamic simulations. The obtained theoretical results are also verified experimentally.

1.3 Structure of the thesis

The thesis is organized into seven chapters with the first chapter describing the background information, motivation and contribution of the thesis. Since the focus of the thesis is on multilevel converters, Chapter 2 gives an overview of the main multilevel converter topologies and their modulation techniques. Chapter 3 provides the basic control structure for star and delta configurations, under balanced conditions. Chapter 4 investigates the harmonic performances of the two CHB configurations and focuses on the individual DC-link voltage balancing. Chapter 5 is dealing with unbalanced conditions. Zero-sequence voltage/current injection is utilized in this chapter to deal with the unbalanced conditions. Verification of the control methods using experimental tests is made in Chapter 6. Finally, the thesis concludes with the summary of the results achieved and plans for future work in Chapter 7.

1.4 List of publications

The Ph.D project has resulted in the following publications, which constitute the majority of the thesis.

I. E. Behrouzian, M. Bongiorno and H. Zelaya De La Parra, ”An overview of multilevel converter topologies for grid connected applications,” in *Proc. of Power Electronics and Applications (EPE 2013-ECCE Europe), in proceedings of the 2013-15th European Conference on*, pp. 1-10, 2-6 Sept. 2013.

II. E. Behrouzian, M. Bongiorno and R. Teodorescu, ”Impact of frequency modulation ratio on capacitor cells balancing in phase-shifted PWM based chain-link STATCOM,” in *Proc. of Energy Conversion Congress and Exposition (ECCE), 2014 IEEE*, pp. 1931-1938, 14-18 Sept. 2014.

III. E. Behrouzian, M. Bongiorno, R. Teodorescu and J.P. Hasler, ”Individual capacitor voltage balancing in H-bridge cascaded multilevel STATCOM at zero current operating mode,” in *Proc. of Power Electronics and Applications (EPE 2015-ECCE Europe), in proceedings of the 2015-17th European Conference on*, pp. 1-10, 8-10 Sept. 2015.

IV. E. Behrouzian, M. Bongiorno and R. Teodorescu, ”Impact of switching harmonics on capacitor cells balancing in phase-shifted PWM based cascaded H-Bridge STATCOM,” accepted for publication in *IEEE Transactions on Power Electronics*.

V. E. Behrouzian, M. Bongiorno and H. Zelaya De La Parra, ”Investigation of negative sequence injection capability in H-bridge multilevel STATCOM,” in *Proc. of Power Electronics and Applications (EPE 2014-ECCE Europe), in proceedings of the 2014-16th European Conference on*, pp. 1-10, 26-28 Aug. 2014.

VI. E. Behrouzian and M. Bongiorno, ”Investigation of negative-sequence injection capability of cascaded H-Bridge converters in Star and Delta configuration,” submitted to *IEEE Transactions on Power Electronics*.

The author has also contributed to the following publications.

I. E. Behrouzian, A. Tabesh, F. Bahrainian and A. Zamani, ”Power electronics for photovoltaic energy system of an Oceanographic buoy,” in *Proc. of Applied Power Electronics Colloquium (IAPEC-2011)*, pp. 1-4, 18-19 April 2011.

II. E. Behrouzin, A. Tabesh, A. Zamani, ”A reliable and efficient circuitry for photovoltaic energy harvesting for powering marine instrumentations,” in *Proc. of Renewable Power Generation (RPG-2011), IET Conference on*, pp. 1-4, 6-8 Sept. 2011.

III. E. Behrouzian, K.D. Papastergiou, ”A hybrid photovoltaic and battery energy storage system for high power grid-connected applications,” in *Proc. of Power Electronics and Applications (EPE-2013), in proceedings of the 2013-15th European Conference on*, pp. 1-10, 2-6 Sept. 2013.

Chapter 2

Multilevel converter topologies and modulation techniques overview

2.1 Introduction

The concept of multilevel converters was first introduced in 1975 [22]. Multilevel converters are power conversion systems composed by an array of power semiconductors and several DC voltage sources. In the last decades, several multilevel converter topologies have been developed [23–27]. The elementary concept of a multilevel converter is to build up a high output voltage through several lower DC voltage sources. The voltage rating of each power semiconductor is kept at only a fraction of the output voltage. The output voltage waveform of a multilevel converter is then synthesized by selecting different voltage levels obtained from the DC voltage sources.

Depending on the selected topology, the number of levels of a multilevel converter can be defined as the number of constant voltage values that can be generated by the converter between the output terminal and a reference node within the converter. Generally, different voltage steps are equidistant from each other. Each phase of the converter has to generate at least three voltage levels in order to be included in the multilevel converter family.

A multilevel converter presents several advantages and disadvantages over a traditional two-level converter. Some of the advantages can be summarized as follows [23–27].

- A multilevel converter generates an output voltage with lower distortion and reduced $\frac{dv}{dt}$.
- For the same harmonic spectrum of the converter output voltage, the switching frequency of the power semiconductors can be much lower. This leads to lower switching losses and thereby higher efficiency.
- Since the voltage rating of each power semiconductor can be kept at only a fraction of the output voltage, the stress across power semiconductors reduces and consequently lower ratings for power semiconductors are required.

- It allows transformer-less installations for grid connected applications.

On the other hand, some of the disadvantages are [23–27]:

- A multilevel converter comprises a greater number of power semiconductors. This leads to a more complex system, which negatively impacts the system reliability. Control and modulation of such a converter is also a difficult challenge.

- There is a limit in the number of achievable levels for some of the multilevel converter topologies. The complexity in the control is one the most important determining factors in the number of achievable levels.

Many papers discussed about multilevel converter topologies, comparison between them [28–30] and their modulation techniques [27],[31]. The aim of this chapter is to provide an overview of different multilevel converter topologies and modulation techniques with focus on STATCOM applications. Advantages and disadvantages of three basic multilevel converters, the Neutral Point Clamped Converter (NPC), Capacitor Clamp Converter (CCC) and modular configurations will be discussed. In particular, different topologies will be compared in terms of number of components, DC-link capacitor dimensioning, modularity and controllability.

2.2 Main multilevel converter topologies

2.2.1 Neutral Point Clamped converter (NPC)

NPC was first introduced by Nabae et al., in 1981 [32]. Figure 2.1(b) shows a three phase three-level NPC. This converter is based on the modification of the two-level converter (shown in Fig. 2.1(a)) adding two additional power semiconductors per phase. Using this configuration, each power semiconductor can be rated at half voltage as compared with a two-level converter having the same DC bus voltage. In another words, with the same power semiconductor rating as two-level converter, the voltage can be doubled in NPC. In addition, NPC allows to generate a zero-voltage level, obtaining a total of three different voltage levels. Figure 2.1(c) [33] shows another configuration of NPC called Active Neutral Point Clamped (ANPC), which will be discussed later.

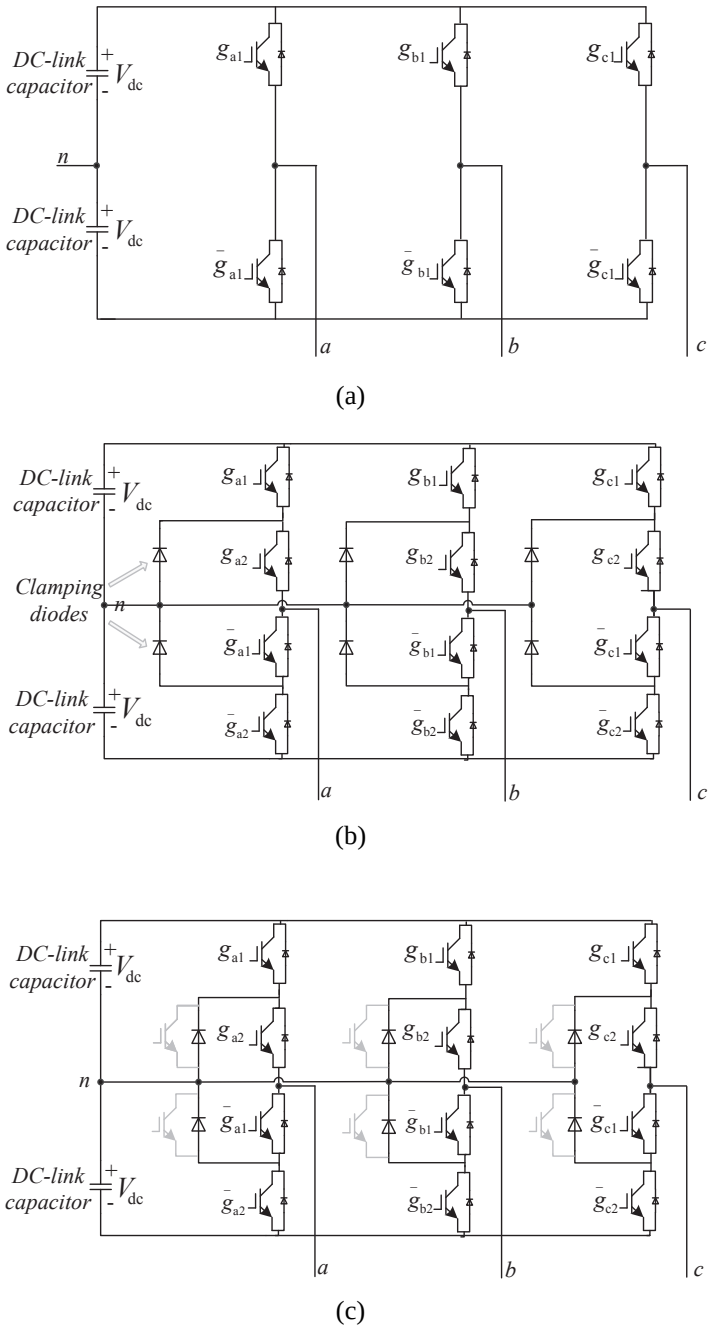


Fig. 2.1 (a) Classic two-level converter, (b) Three-phase three-level NPC, (c) ANPC.

Figure 2.2 shows the different switching states for one phase leg of the three-level NPC and their corresponding output voltage levels. Current path for each set of gate control signals are highlighted. Note that there are only two control gate signals per phase. The other two gate signals are inverted to avoid to short circuit the DC-link. In Fig. 2.2, ON state of each power semiconductor is represented by 1 and OFF state is represented by 0. Gate signals $(g_{a1}, g_{a2}) = (1,0)$ is not used since this switching state does not provide any current path at the output. The

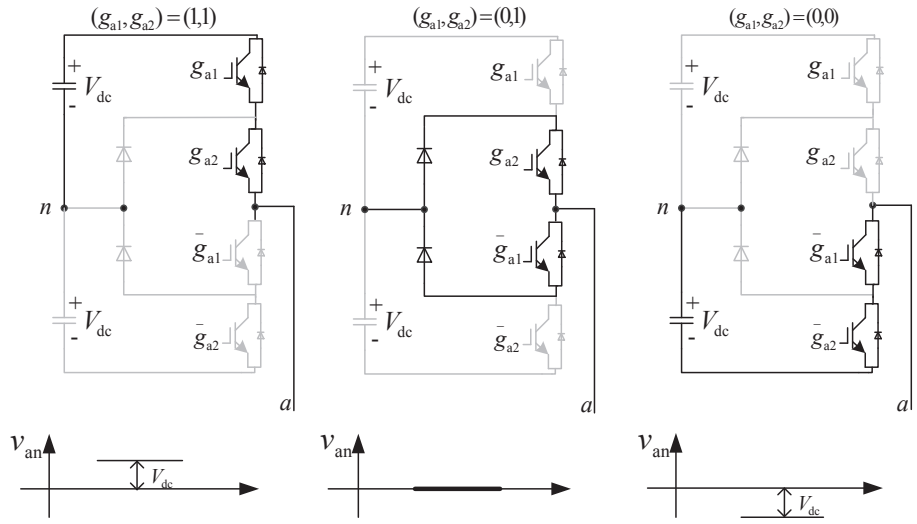


Fig. 2.2 Three-level NPC switching states and corresponding output voltage levels.

same switching states are also valid for the other two phases.

The NPC can be extended to higher number of output levels. For example Fig. 2.3 shows the phase leg of a five-level NPC. Although each power semiconductor device is rated at the voltage level of V_{dc}, the clamping diodes require different ratings for reverse voltage blocking. For this reason, series connection of diodes, each rated for a voltage level of V_{dc} are needed as in Fig. 2.3

NPC takes its name from the use of diodes to limit the collector-emitter voltages of the switching device to the voltage across one capacitor. Although it is theoretically possible to increase the number of levels, NPC finds its realistic limit to five-level due to the complexity of the system, complexity of the control and large number of components required [24]. Another limiting factor for the number of levels in NPC is represented by the uneven distribution of semiconductor losses among the semiconductors, which limits the switching frequency and the output power. The latter can be overcome by installing additional power semiconductors in parallel with the clamping diodes forming the so-called Active Neutral Point Clamped (ANPC) showed in Fig. 2.1(c) [33]. It is important to stress that although the power loss is more even in an ANPC, the need for more power electronic components leads to an increase in complexity of the overall system. In addition, the diode reverse recovery becomes an important design challenge. It is also of importance to mention that NPC does not present a modular configuration. Therefore series connection of power semiconductor is needed to achieve the desired voltage level for grid-connected applications. Thanks to the common DC link for all phases, the requirements on the DC-link capacitor are only to provide the temporary energy storage during switching operations, to distribute reactive power among the phases and to support the system losses. Despite the mentioned limitations, the NPC has been successfully implemented in STATCOM applications in its three-level topology with power level up to $\pm$120MVA [34].

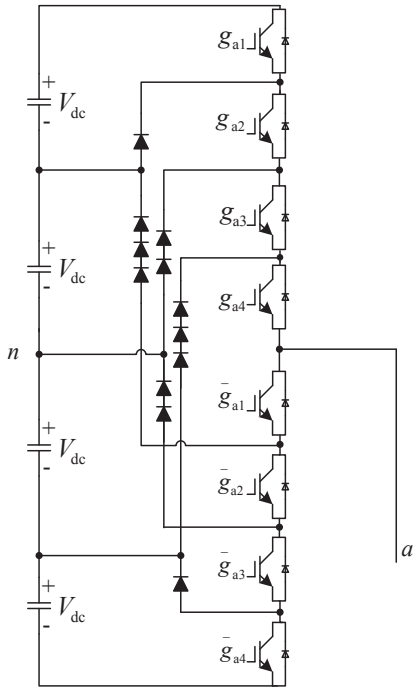


Fig. 2.3 Phase *a* of a five-level NPC.

2.2.2 Capacitor Clamp Converter (CCC)

The CCC was first introduced by Meynard et al., in 1992 [35]. Figure 2.4(a) shows a three phase three-level CCC. CCC can be considered as an alternative to overcome some of the NPC drawbacks. The main difference between this topology and the NPC is that the clamping diodes are replaced by clamping capacitors.

Figure 2.4(b) shows the different switching states for one phase leg of the three-level CCC and their corresponding output voltage levels. Current path for each set of gate control signals are highlighted. Similar to the NPC, only two control gate signals per phase leg are needed in order to avoid to short circuit the DC-link. However, in the CCC the inverted gating signals are related to different power semiconductors as compared with NPC and shown in Fig. 2.4(b). The output voltage levels of the converter are generated by adding or subtracting the clamping capacitor voltage with the DC bus voltage; for example, zero-voltage level in this topology is obtained by connecting the output of the converter to the neutral point (*n* in Fig. 2.4(b)) through clamping capacitor with opposite polarity with respect to the DC bus voltage. It should be noted that all four combinations of (g_{a1}, g_{a2}) can be used in the CCC. Only three are shown in Fig. 2.4(b). Both gate signals of $(g_{a1}, g_{a2}) = (1, 0)$ and $(g_{a1}, g_{a2}) = (0, 1)$ generate zero-voltage level at the output.

Being able to generate the same voltage level with different switching states is known as voltage level redundancy. This redundancy plays an important role in the capacitor voltage balancing in a CCC. For example, in a five-level CCC there are six combinations of capacitor selection and switching states that generate zero-voltage level. By proper selection of the switching states and

capacitor combinations, it is possible to control the capacitor charging state. This can improve the complexity of the capacitor voltage controller for higher levels [23]. Common DC source is also another advantage of this topology.

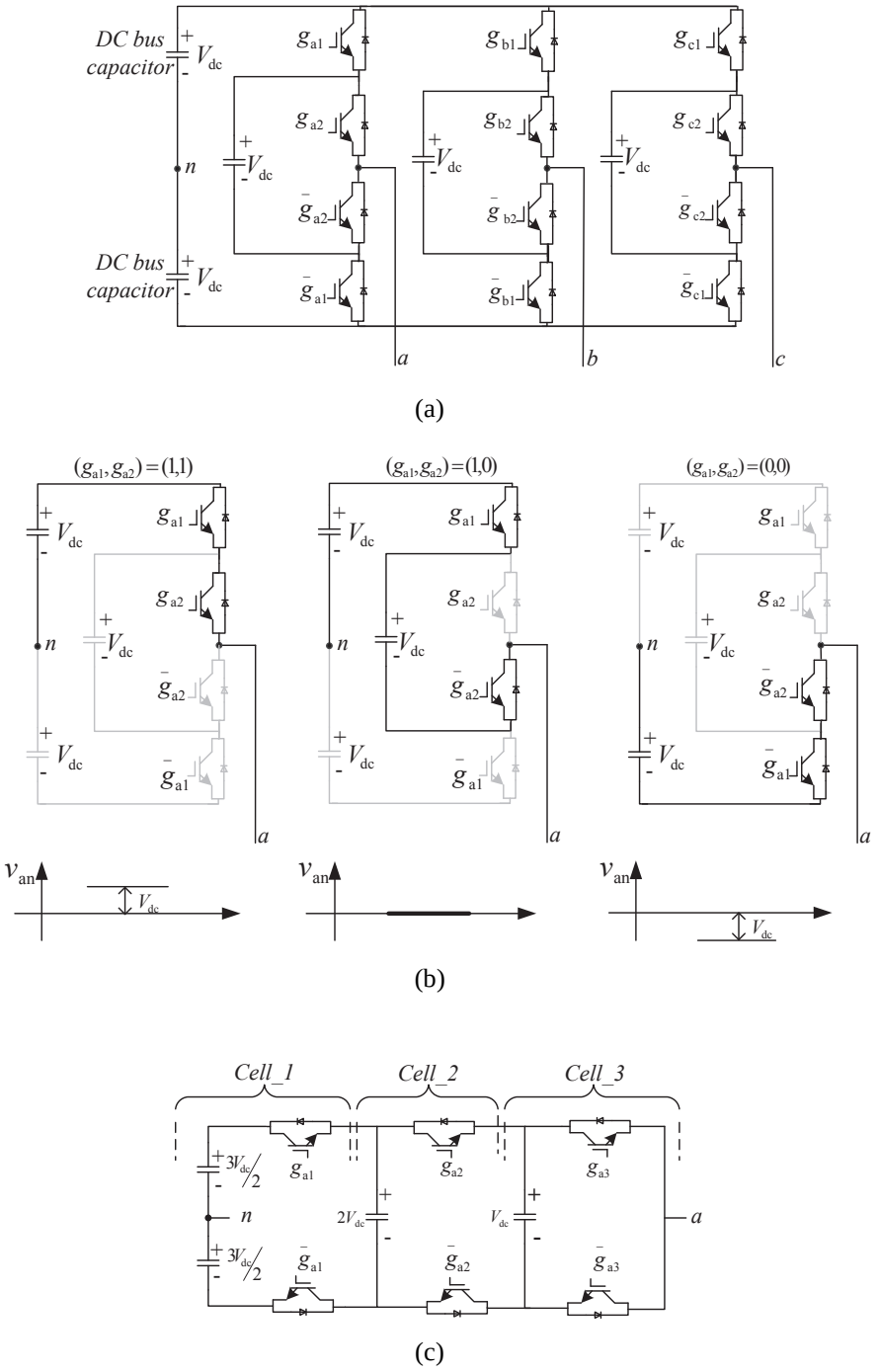


Fig. 2.4 (a) Three-phase three-level CCC, (b) Three-level CCC switching states and their corresponding output voltage level, (c) Phase *a* of a four-level CCC.

The CCC can be extended to higher number of output levels. This can be observed by redrawing the CCC as illustrated in Fig. 2.4(c) for phase *a* of a four-level CCC. In Fig. 2.4(c), cell is refer to a pair of power semiconductor devices together with one capacitor. These cells (or modules) can be connected in cascaded form and each one provides one additional voltage level to the output. This property of the CCC has led to the idea that the CCC can be seen as a modular topology. However, the capacitors within each cell of CCC are charged to different voltage levels and this is in contrast with the modularity concept.

High number of voltage levels requires a relatively high number of capacitors in this topology. A *m*-level CCC requires a total of $(m-1)(m-2)/2$ clamping capacitors per phase in addition to the $m-1$ main DC-link capacitors. Lack of modularity and the high number of capacitors for high number of voltage levels can reduce the reliability of this converter. The size of the capacitors can also become large when using low switching frequency (typically, for switching frequencies below 800-1000 Hz), due to the fact that the output current flows through clamping capacitor as long as the switching state does not change. However, being able to overcome the complexity in the control and hardware, a five-level CCC is implemented in STATCOM applications with voltage level up to 6.6kV [36].

2.2.3 Modular configurations

Modularity, in industrial design, refers to an engineering technique that builds large systems by combining smaller and identical subsystems. Designing power converter using the modularity concept was first introduced by Marchesoni et al., in 1990 [37]. The modular configurations consist of many identical cells connected in series. These cells can be either half- or full-bridge (H-bridge) converter. Figure 2.5 shows the half- and full-bridge cells with switching states and corresponding output voltage levels.

Different modular configurations will be shown in Section 2.3 but for illustration purpose, a single-line diagram of a five-level star configuration is shown in Fig. 2.6. This topology is capable of reaching high output voltage levels using only standard low-voltage technology components. Due to the modularity, in case of a fault in one cell, it is possible to replace it quickly and easily. Moreover, it is possible to bypass the faulty module without stopping the load, bringing an almost continuous overall availability.

Although modular configurations presents a fairly simple structure, they suffer from requirement of large number of cells (more isolated capacitors) to decrease the harmonics and switching frequency. This leads to a more complex DC-voltage regulation loop. However various control algorithms exist to control high number of capacitors voltage [8]. Moreover, due to the lack of a common DC link, the output power will be affected by an oscillatory component having characteristic frequency equal to twice the grid frequency; these oscillations will be reflected on the DC-link voltage and therefore each cell necessitates over-sizing of the DC link capacitors to provide filtering effect.

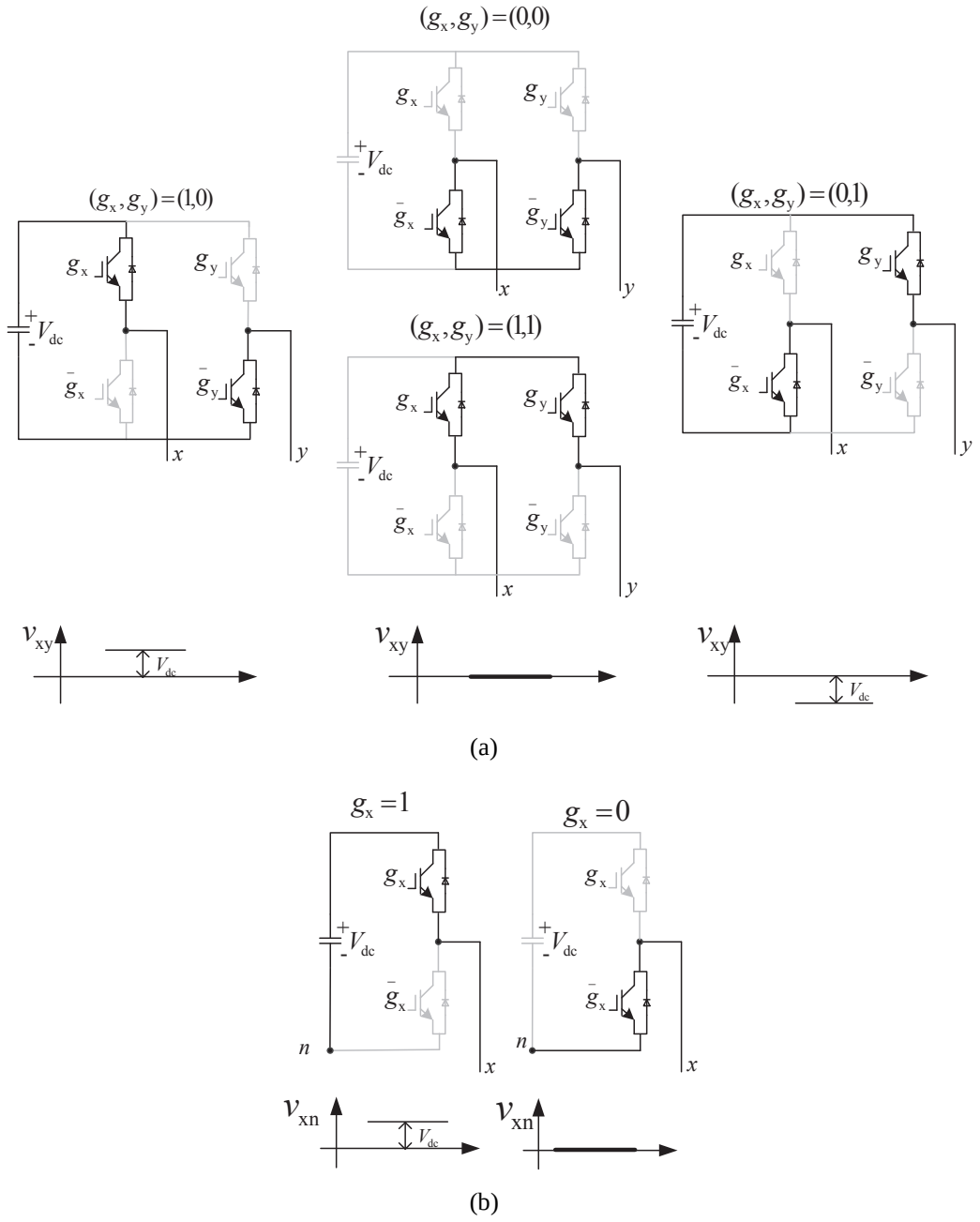


Fig. 2.5 Cell with switching states and corresponding output voltage level; (a): H-bridge; (b): half-bridge.

It is also possible to use cells with unequal DC source voltages in modular configurations and form an alternative configuration called hybrid or asymmetric configuration [38]. The hybrid configuration can produce higher voltage level with fewer power electronic requirements. This reduces the size and cost when compared to the traditional modular configuration with equal DC-links, since fewer semiconductors and capacitors are employed. The main disadvantage of

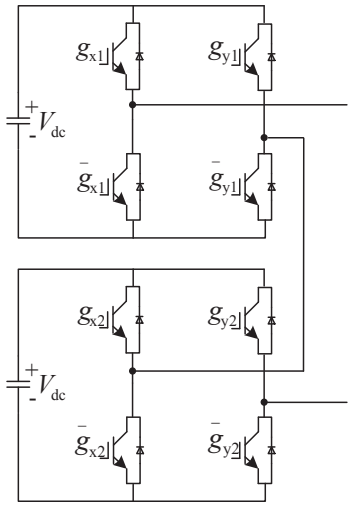


Fig. 2.6 Single-line diagram of a five-level star configuration.

this approach is that the converter is no longer modular.

2.2.4 Multilevel converter topologies comparison for STATCOM applications

In recent years, the demand for high-voltage conversion applications has drastically increased. Reliability, availability, controllability, modularity, number of components and losses are the main features for high power STATCOM applications.

In STATCOM applications the converter voltage is increased through a step-up transformer before connecting to the grid. Consequently, the current will be high in the low voltage side which leads to higher power loss and thus reduced efficiency. This is the driving force that has led the research community to focus on transform-less solutions, in order to directly connect the converter to the grid. In addition, a transformer-less topology allows a reduced footprint for the system and a reduction in losses. Since in high-voltage applications the voltage rating usually ranges several tens to hundreds of kVs, the power processing cannot be accomplished with any single IGBT or similar switch. One way to reach high voltage rating is to connect several switches in series and operate them simultaneously. However, the series operation of switches is very difficult because of tolerances in their characteristics and/or the unavoidable mismatch between the driving circuits. The main problem is to ensure an equal voltage sharing among the components during static and dynamic transient states. Furthermore, special arrangements are needed to guarantee a continuous operation of the device in case of faulty switch.

A simpler method to increase the voltage rating is to use modular configurations. In these configurations the total output voltage of the converter can be increased by increasing the number of cells, each operated at low voltage. As mentioned before it is possible to raise the voltage in modular configurations only by increasing the number of voltage levels. The ability of these configurations to increase the number of levels also results in better harmonic performance and

lower switching losses. These configurations also have the ability to successfully balance the capacitor voltages for high number of levels. It is for these reasons that the modular configurations are often considered as the most suitable solution to implement high-power STATCOM, while NPC and CCC are more suitable for medium-voltage and low-power applications. Table 2.1 summarizes different characteristics of multilevel converter topologies discussed in this section.

The main modular configurations are the star, delta and double star. In this thesis, the modular multilevel converters that are based on the use of H-bridge converters will be denoted as Cascaded H-Bridge (CHB) converters, while the converter based on half-bridge cells will be simply denoted as Modular Multilevel Converters (MMCs). Therefore, the star and delta configurations will be CHB converters, while the double start can be either CHB or MMC depending of the adopted cell topology. Each of these configurations has specific characteristics, advantages and disadvantages. A detailed review of these configurations is provided in the next section.

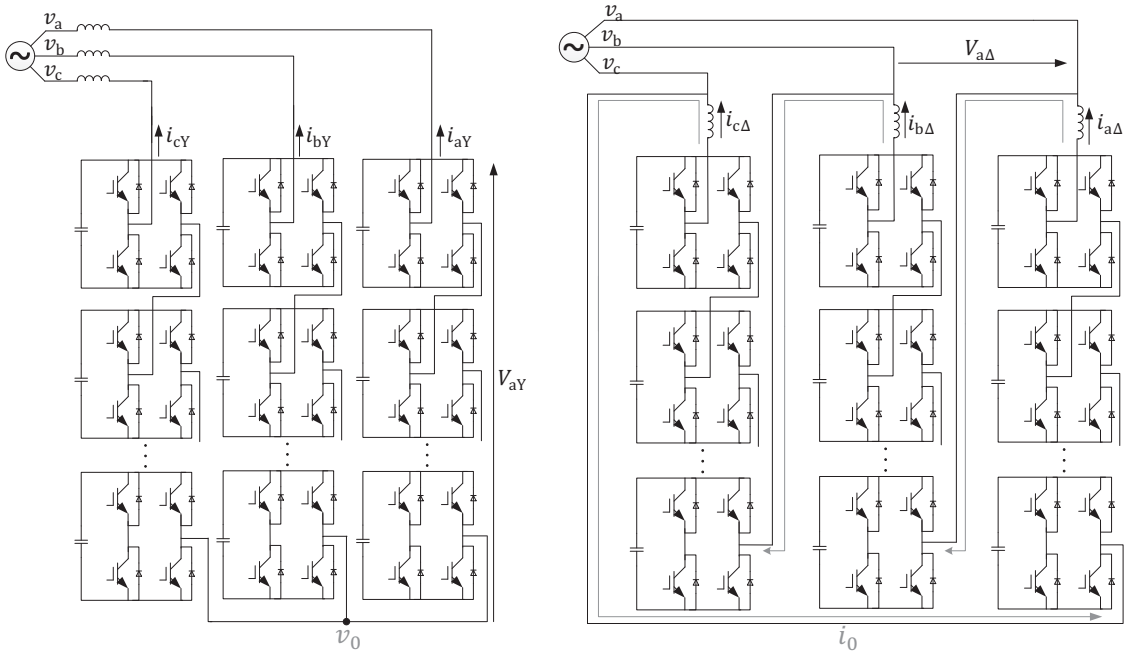
TABLE 2.1. SUMMERY OF MULTILEVEL CONVERTERS CHARACTERISTICS

structure	NPC	CCC	CHB
Switches per phase (Converter with m- level)	$2(m-1)$	$2(m-1)$	$2(m-1)$
Clamping diodes per phase (Converter with m-level)	$(m-1)(m-2)$	0	0
Capacitors per phase (Converter with m-level)	$(m-1)$	$(m-1)(m-2)/2$ $+(m-1)$	$(m-1)/2$
Loss distribution	Uniform with ANPC	Uniform	Uniform
Maximum practical levels	3-5 levels	5-7 levels	No theoretical limit
Availability	Low	Low	High
Modularity	No	No	Yes
Capacitor sizing	low	high	high
Common DC source	Yes	Yes	No
Low switching	Capable	Capable with large capacitors	Capable with large capacitors

2.3 Modular subset configurations and comparison

The main modular configurations: star, delta and double star configurations [19] are investigated in this section and their application for STATCOM is addressed.

Star and delta configurations are shown in Fig. 2.7 for the application of three-phase STATCOM. Each phase consists of several H-bridge converters connected in series. Three phases can be connected in either star (Y, Fig. 2.7(a)) or delta (Δ, Fig. 2.7(b)). A prototype of star and delta configurations as three-phase STATCOM was first demonstrated by Peng et al., in 1996 [39]. In less than two years, in 1998, GEC ALSTHOM T&D (now ALSTOM T&D) proposed to use



(a) (b)

Fig. 2.7 CHB configurations; (a): star configuration; (b): delta configuration.

these configurations as a main power converter in their STATCOMs. Robicon Corporation also commercialized their medium voltage drives utilizing these configurations in 1999. Currently these devices offer a power range of 10-250 MVAr [40, Chapter 2].

Another modular configuration that is receiving increased research focus is the MMC, which was first introduced by Marquardt and Lesincar in 2003 [9]. This configuration is shown in Fig. 2.8. Each phase of the converter, also called converter leg, consists of two arms. Each arm contains equal number of cells and a coupling inductor to limit the current under AC fault and also to limit the $^{di}/_{dt}$ due to switching. The AC output is connected in the middle of the two arms. It is also possible to use H-bridge instead of half-bridge as illustrated in Fig. 2.9.

Comparing the star and delta configurations, the first difference is in their voltage and current rating. Under balanced grid voltage condition with equal number of cells per phase and similar power electronic equipment, star has $\sqrt{3}$ time higher current rating compared to the delta, while delta has $\sqrt{3}$ time higher voltage rating compared to the star in each phase. In case of unbalanced grid voltage, delta has the ability to exchange negative-sequence current with the grid by controlling a zero-sequence current that circulates inside the Δ. Although it leads to a slight increase in losses, the circulating current can exchange power between phases, which can be used to balance capacitor voltages especially when negative-sequence reactive power is needed.This also results in an increased current rating as compared to balance condition (and consequently higher current rating compared to the star). Higher current rating not only affects the rating of the semiconductors in the bridges, but more importantly affects the current ripple, and thereby the rating of the capacitors in each bridge. With the same reasoning, the star configuration needs to be over-rated in terms of voltage when operated under unbalanced grids, due to the needed

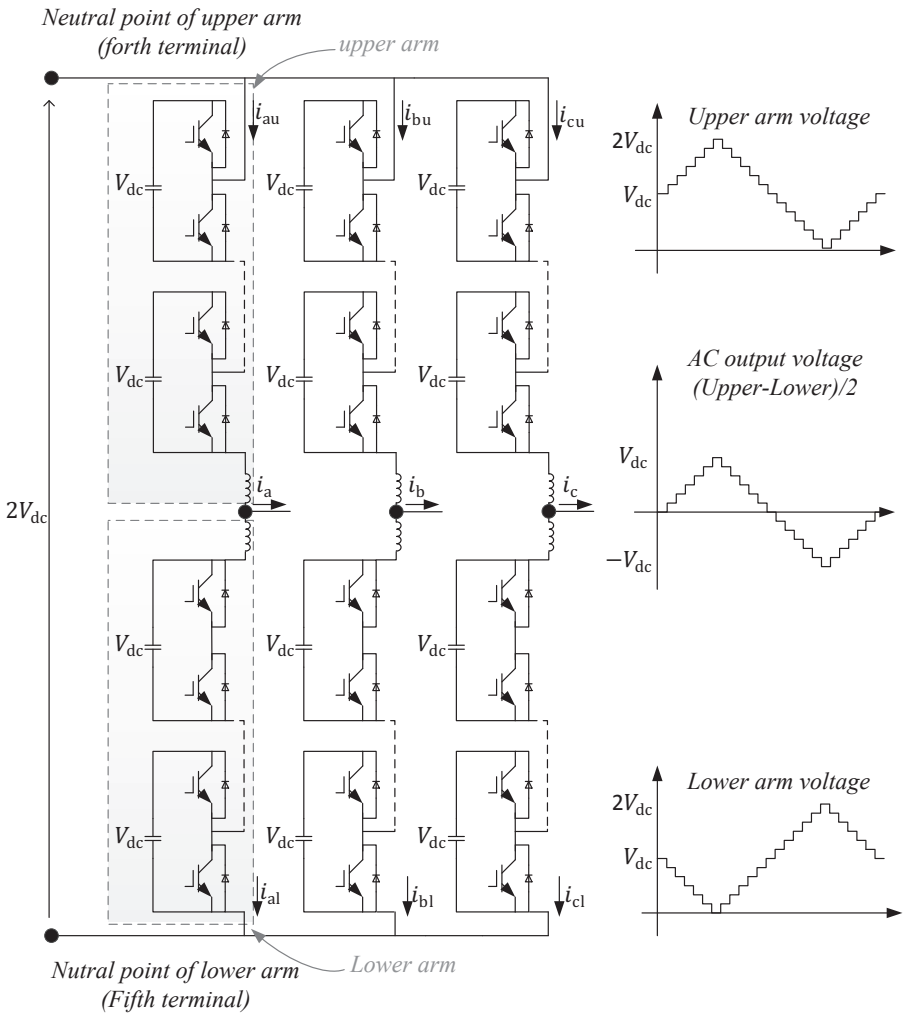


Fig. 2.8 Double star configuration with half-bridge cells (known as MMC).

zero-sequence voltage (which will lead to a movement of the floating Y-point of the converter) to guarantee capacitor voltage balancing.

Regarding the double-star configurations, CHB and MMC are ”five-terminal circuits” because two neutral points of upper and lower arms are used as the two DC terminals. This is the main advantage of these configurations over star and delta since they can manipulate active power without the need of isolated DC sources in each cell. This is particularly important in High Voltage DC (HVDC) and motor drive applications, where large amount of active power is transfer. However, being the focus of this thesis on STATCOM applications only, a common DC-link between the three phases is not needed.

In STATCOM application the converter must be able to provide reactive power under unbalanced condition. Double star configurations, similar to the delta, have the ability to exchange negative-sequence current with the grid by controlling the circulating current.

One of the other important feature of the double-star configuration is the lower device current rating of the individual cells, due to the AC current sharing between the two converter arms.

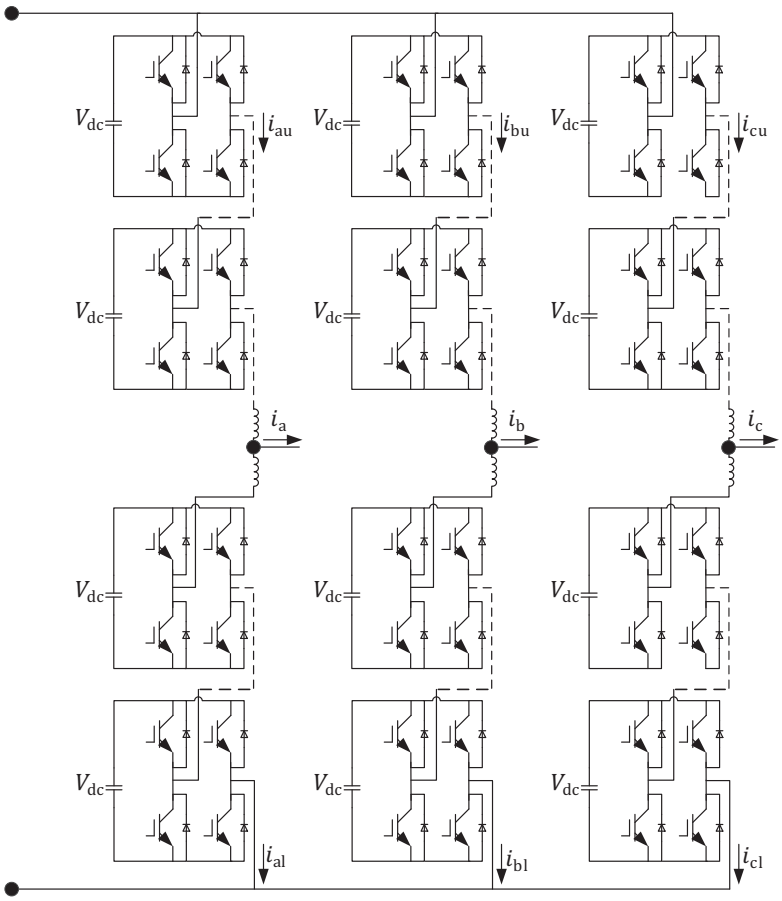


Fig. 2.9 Double star with CHB configuration.

However, the voltage rating of these devices is higher compare with the star and delta. As it is shown in Fig. 2.8 each converter arm generates an AC voltage with a DC offset equal to half of the total DC-link voltage in MMC. This results in a higher converter arm voltage rating (two times the AC voltage). If H-bridge cells are used instead of half-bridge cells, each arm is needed to generate only the AC voltage with the same amplitude of the output voltage. Therefore the number of cells reduces to half as compare with the double star with half-bridge while the number of power semiconductor in each cell is now doubled. As an example if half- and H-bridge cells with 1pu voltage rating are available, in order to generate an AC voltage with 1pu peak under balanced conditions, only one cell per phase is needed if star configuration is chosen while $\sqrt{3}$ cells are needed for delta. Double star configuration with half-bridge cells needs 4 half-bridge cells and double star configuration with H-bridge cells needs 2 H-bridge cells to satisfy the requirements.

The interaction between DC offset voltage at each arm and fundamental current in double star configuration results in a large fundamental frequency component in the arm capacitor voltages. This increases the capacitor voltage ripple as compared with the star and delta configurations. Thus the size of the capacitors and hence cost and footprints increase significantly in the double star configuration.

Double star configuration with H-bridge cells is superior to the one with half-bridge cells since it has additional buck and boost functions of the DC-link voltage. Having H-bridge cells enables this configuration to tolerate a broad range of variation in the DC-link voltage.This feature makes it suitable for renewable resources such as wind and solar power since the DC-link voltage varies with weather variations. Moreover, this configuration has the ability to suppress fault currents arising from DC-side short circuit events [41].

In STATCOM applications, where only reactive power is exchanged with the grid, star and delta configurations have superior performances. Besides having a less complex controller they have higher efficiency, need less number of cells [42] and have better dynamic performance [28]. Table 2.2 summarizes different characteristics of all modular subset configurations discussed in this chapter.

This section introduces the main modular configurations. Several alternative modular configurations can be found in literature [43, 44].

TABLE 2.2. SUMMERY OF MODULAR SUBSET CONFIGURATIONS CHARACTERISTICS

	star	delta	double star MMC	double star CHB
Cell numbers balanced condition	v_{ac}/V_{dc}	$\sqrt{3}v_{ac}/V_{dc}$	$4v_{ac}/V_{dc}$	$2v_{ac}/V_{dc}$
current rating balanced condition	$\sqrt{3}$/phase	1/phase	0.5/phase	0.5/phase
Negative-sequence compensation	capable (v_0)	Capable(i_0)	Capable(i_0)	Capable(i_0)
Circulating current	No	Yes	Yes	Yes
Voltage rating unbalanced condition	Balanced voltage+v_0	No change	No change	No change
Current rating unbalanced condition	No change	Balanced current+i_0	Balanced current+i_0	Balanced current+i_0
Capacitor size balanced condition	Higher than delta	-	Higher than star&delta	Higher than star&delta
Capacitor size unbalanced condition	Lower than delta	-	Higher than star&delta	Higher than star&delta
Hardware complexity	Lowest	-	-	-
Controller complexity	Medium	Medium	High	High
Cost	capacitor & switch trade off			

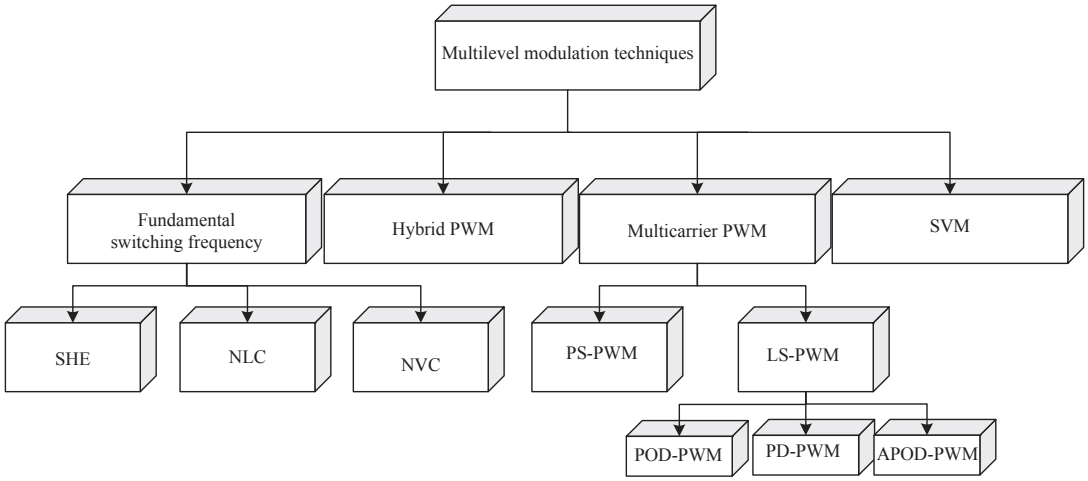


Fig. 2.10 Multilevel converter modulation techniques.

2.4 Multilevel converter modulation techniques

A modulation technique determines the switching function of a converter. The modulation technique must guarantee that the generated voltage at the output of the converter is similar to the desired voltage as much as possible. The challenge is to extend traditional modulation techniques to the multilevel case, where the large number of cells gives different alternatives to modulate the converter. Each modulation approach focuses on the optimization of some converter features such as switching loss reduction, uniform switching loss distribution, improving harmonic performances, common-mode voltage minimization, minimum computational cost, etc. The most common modulation techniques for multilevel converters are summarized in Fig. 2.10.

The fundamental switching modulators, provide a switching function such that each cell has only one commutation per fundamental cycle. The switching function with multicarrier PWM are determined based on comparison between carriers and a reference signal. Hybrid PWM is a mixture of fundamental and carrier-based modulation. Space Vector Modulation (SVM) considers all the possible switching states and select the best combinations in each control cycle to generate an output voltage with equal volt/second as the reference value. Detail description of each modulator is provided in this section.

It is also worth mentioning that the switching commands for the converter are not always determined by a dedicated modulation stage; instead, they can be determined by a direct consequence of the overall converter controller. Hysteresis current controller and Model Predictive Control (MPC) are typical examples of these type of controllers.

2.4.1 Multicarrier PWM

1. $Phase-Shifted\ PWM\ (PS-PWM)$: This method is a natural extension of the traditional bipolar and unipolar PWM techniques. This modulation technique is one of the most commonly used modulation techniques for multilevel converters with half or H-bridge

cells, such as CCC and all the modular configurations.

The hardware implementation and operating principle of the PS-PWM for one phase of a five-level star configuration are illustrated in Fig. 2.11 and Fig. 2.12, respectively. Each cell is modulated independently through a comparison between a modulation and a carrier signal. The modulation signal is the same for all the cells that constitutes a phase leg while a phase shift is introduced between the carrier signals of each cell. It is proven that the lowest distortion at the total output can be achieved when the phase shifts between carriers are $360^0/n$ (where n is the number of cells per phase).

Since the modulation signals and carrier frequency are the same for all the cells, the switching pattern and thereby the active power are evenly distributed among all the cells [31]. The advantage of the even power distribution is that, in case of CHB-STATCOM as an example, once the DC-link capacitors are properly charged, no unbalance will be produced among the DC-link voltages. Moreover, due to the proper selection of the phase shift angle between carriers, the total output waveform has a switching pattern with n times the switching pattern of each cell. Hence, better Total Harmonic Distortion (THD) is obtained at the output, using n times lower carrier frequency.

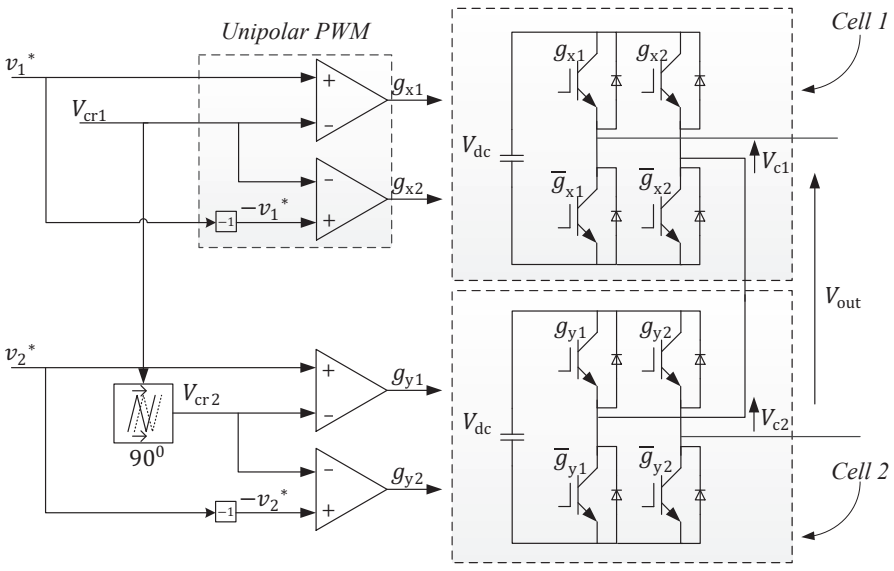


Fig. 2.11 Hardware implementation of PS-PWM for one phase of a five-level star based on unipolar PWM.

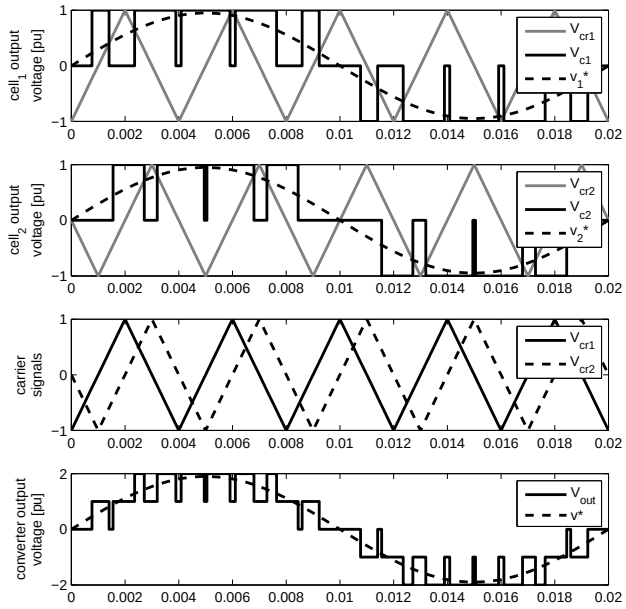


Fig. 2.12 Operating principle and switching pattern of the PS-PWM based on unipolar PWM.

2. *Level – Shifted PWM* $(LS-PWM)$: This method is a natural extension of traditional bipolar PWM techniques. In traditional bipolar PWM, a carrier signal is compared with the reference to decide between two different voltage levels. If the reference voltage is greater than the carrier then a switching command that generates the positive voltage level is sent to the converter. In another case, if the reference is less than the carrier, a switching command that generates the negative voltage level is sent to the converter.

   By extending this idea for a multilevel converter with m levels, $m-1$ carriers are needed. Each carrier is set between two voltage levels and the same principle of bipolar PWM is applied. Required carriers can be arranged in vertical shifts. If all the carriers are in phase with each other (only vertical shift), the modulation technique is named Phase Disposition PWM (PD-PWM). If all the positive carriers in phase with each other and in opposite phase of the negative carriers, we talk about Phase Opposition Disposition PWM (POD-PWM). By alternating the phase between adjacent carriers, Alternate Phase Opposition Disposition PWM (APOD-PWM) is obtained. Different arrangement of carriers provides different THD. For example POD-PWM at the expense of having more complicated structure than PD-PWM has less THD than PD-PWM [45],[46]. An example of these arrangements for a five-level (thus four carriers) star configuration is given in Fig. 2.13. The switching command must be wisely directed to the appropriate power semiconductor in order to generate the corresponding levels. The hardware implementation and cell output voltage by using LS-PWM for a five-level star configuration is illustrated in Fig. 2.14.

   This modulation technique can be adapted to any multilevel converter. However, as it can be observed from Fig. 2.15, it is clear that the switching pattern is not uniform between two cells when LS-PWM is used. This causes an uneven power distribution among the different cells.

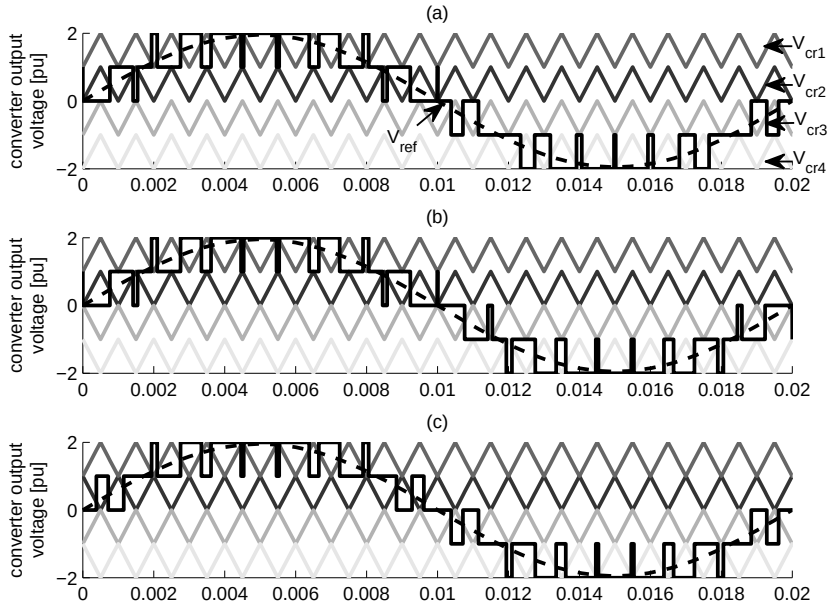


Fig. 2.13 LS-PWM arrangement; (a): PD; (b): POD; (c): APOD.

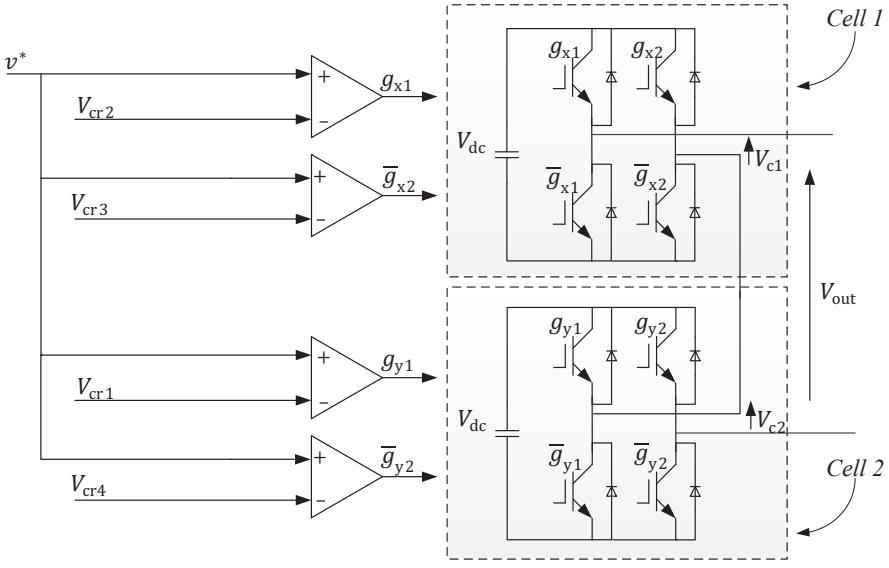


Fig. 2.14 Hardware implementation of LS-PWM.

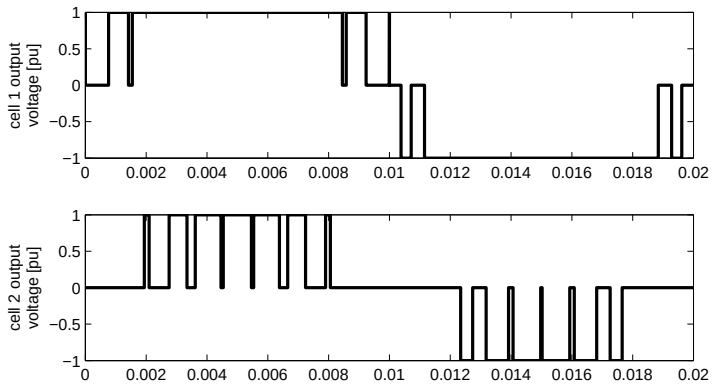


Fig. 2.15 Cell output voltages by using LS-PWM.

2.4.2 Space Vector Modulation (SVM)

Using Fig. 2.16 (a) different steps of SVM can be summarized as follow. First step is to determine all the switching states and their corresponding state-space vector in $\alpha\beta$-reference frame. Fig. 2.16 (a) shows all the eight switching space vectors with black circles for a traditional two level converter. + and - signs in parentheses are to show which switch in each phase is on. For example $(-,+,+)$ shows that in phase *a* lower switch and in the other two phases upper switches are on.

Second step is to determine the reference voltage state-space vector in $\alpha\beta$-reference frame. Third step is to find the three closest switching combination to the reference (v_1, v_2, v_3 in Fig. 2.16 (a)). The final step is to calculate the time duration of each switching state (t_1, t_2) so that the time average of the generated voltage equals the reference space vector.

Figure 2.16 (b) shows the extension of SVM for a three level star (one cell per phase). Each cell can produce positive ($+V_{\mathrm{dc}}$), negative ($-V_{\mathrm{dc}}$) and zero (0) voltage levels. Having 3 levels, results in 3^3 possible combinations, shown with black circles. It can be observed that for some vectors more than one switching state is possible.

Following the same steps as explained before v_1, v_2, v_3 and their corresponding time t_1, t_2, t_3 should be determined in order to make the switching commands.

It should be noted that SVM explained here is valid only for a balanced system with purely sinusoidal reference voltages. In case of an unbalanced system, existence of harmonics or zero-sequence component this algorithm must be modified [47, 48].

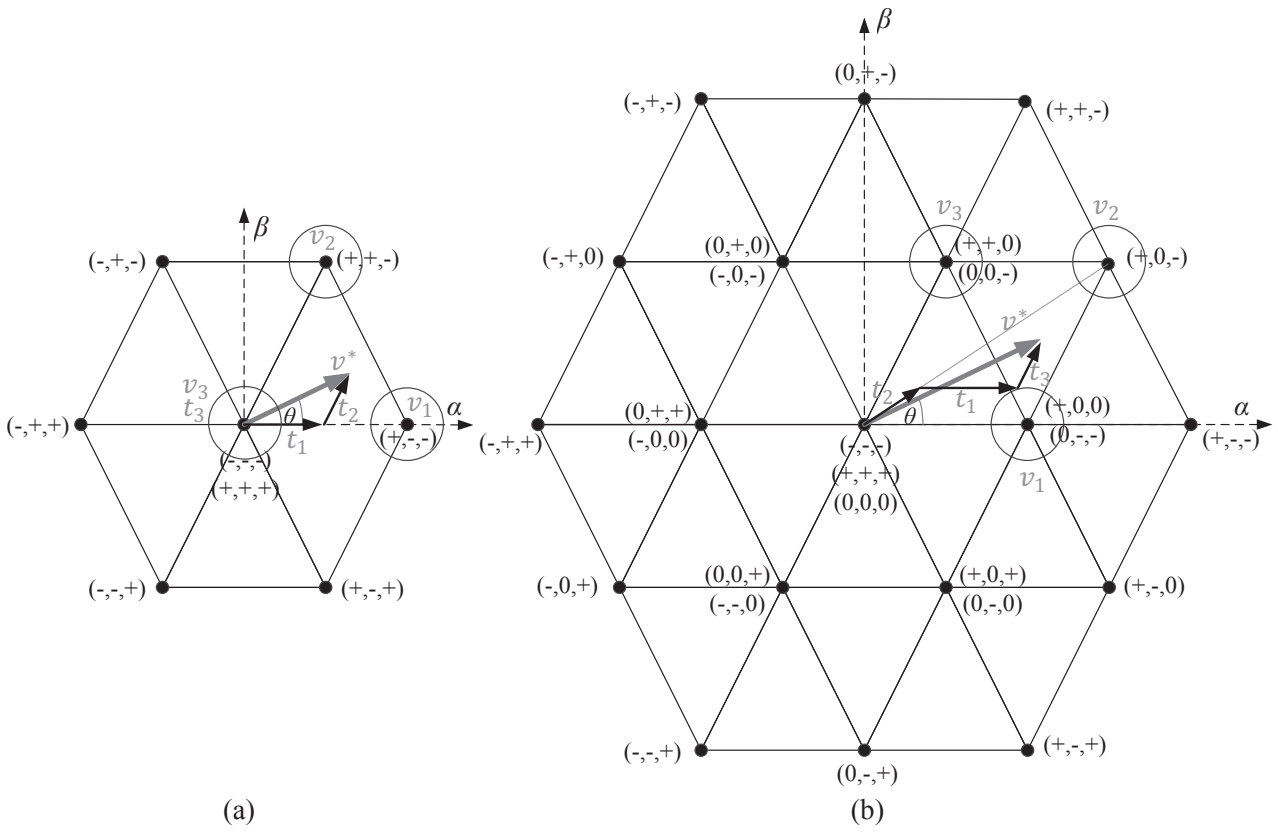


Fig. 2.16 SVM principle for; (a): traditional two level converter; (b): three-phase three-level star configuration.

2.4.3 Fundamental switching modulators

1. *Selective Harmonic Elimination* (*SHE*): The basic idea of SHE is predefining and precalculating switching angles per quarter-fundamental cycle via Fourier analysis to ensure the elimination of undesired low-order harmonics. The first step is to find the Fourier series of the multilevel waveform based on unknown switching angles. Next step is to set the undesired Fourier coefficient to zero, while the fundamental component is made equal to the desired reference value. The obtained equations are solved offline using numerical methods, finding solution for the angles.

   As an example for phase *a* of the star configuration with three H-bridges per phase, a typical waveform considering three switching angles $(\alpha_1, \alpha_2, \alpha_3)$ is given in Fig. 2.17. Each angle is associated to a particular cell. Consequently each cell of the converter produces positive or negative voltage levels at a specific angle only once in a fundamental cycle. SHE is also known as staircase modulation because of the stair-like shape of the voltage waveform.

   Note that there is no control over non eliminated harmonics and if non eliminated harmonic amplitude are not suitable for a particular application, additional cells and angles can be introduced. It is also possible to limit the harmonic content to acceptable values

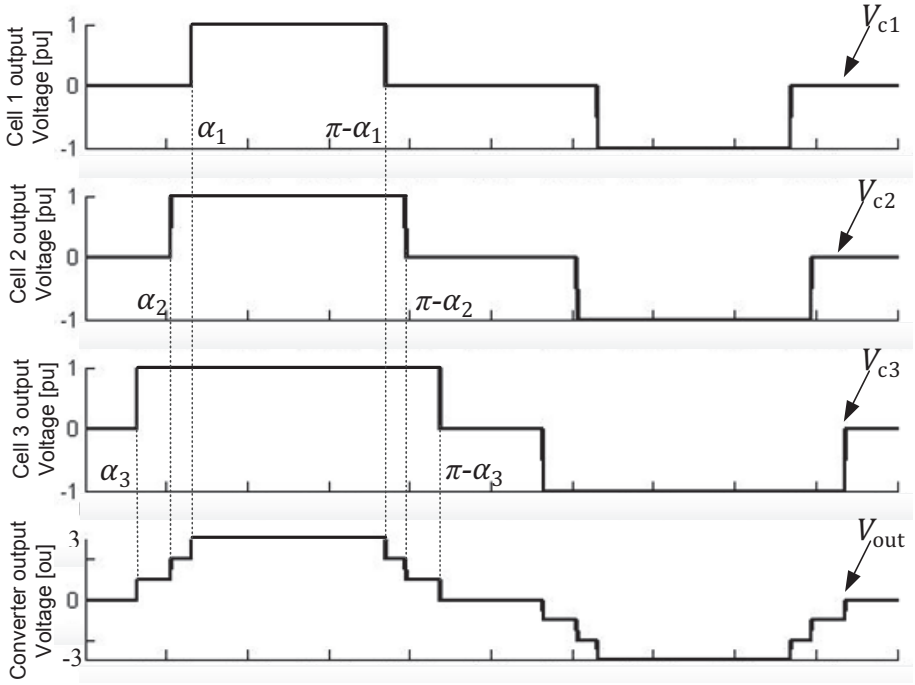


Fig. 2.17 SHE technique for phase *a* of the star configuration with 3 cells per phase.

instead of completely eliminating them. This method is called Selective Harmonic Mitigation (SHM).

The main advantage of SHE is the reduction of the switching frequency and consequently the switching losses. It also eliminates the low order harmonics, facilitating the reduction of output filter size. However, this method requires numerical algorithms to solve the equations for different modulation indexes. With current technology of microprocessors it is not possible to do the calculations in real time. Therefore, the solutions are stored in a look-up table, and interpolation is used for those unsolved modulation indexes. This makes SHE method not suitable for applications where high dynamic performance is needed.

2. *Nearest Vector Control* (NVC): NVC also known as State Vector Control is the alternative method to SHE to provide a low switching frequency, with no numerical calculation and poor dynamic performance. The basic idea is to simply approximating the reference voltage to the closest voltage vectors that can be generated in the $\alpha\beta$ frame.

   The dots in Fig. 2.18 shows all the possible voltage vectors generated by the converter, surrounded by the hexagons. Each converter vector is considered as the closest vector to the reference, as long as the reference voltage is located inside the hexagon surrounded that vector. Hence, when the reference voltage falls into a certain hexagon, the corresponding vector is generated by the converter.

   Unlike SHE, this technique does not eliminate low-order harmonics. However, this problem can be avoided by using multilevel converters with a high number of levels. High

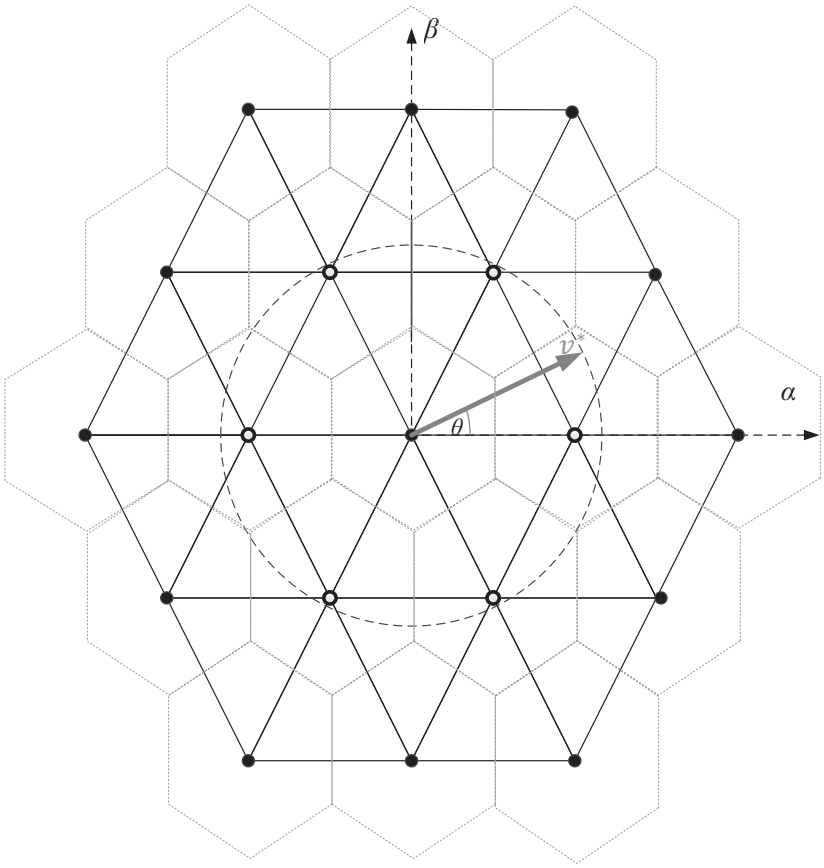


Fig. 2.18 All the possible voltage vector for a three-level star configuration and their corresponding hexagon.

number of levels provides more available voltage vectors and thereby smaller error. Despite the simple operating principle, its practical implementation is not trivial.

3. *Nearest level Control* (*NLC*): NLC, also known as round method, is somehow the per-phase time domain counterpart of the NVC. The basic principle in both methods is the same but instead of choosing the closest vector, when using NLC the voltage level closest to the reference voltage is selected. Also unlike NVC, where three phases are controlled simultaneously with the vector selection, here three phases are controlled independently with 120^0 phase shifted references. The main advantage of this method over NVC is that since finding the closest level is much easier than finding the closest vector to the reference, NLC is greatly simplified in relation to NVC.

   The output voltage using NLC is shown in Fig. 2.19 for the first quarter cycle of the reference voltage, where V_{dc} is the voltage difference between two voltage levels (usually the DC-link voltage in modular configurations), v^* is the reference voltage and V_{out} is the output voltage. As can be seen from Fig. 2.19 the maximum error in approximation of the closest voltage level is $V_{\text{dc}}/2$.

   Similar to NVC, NLC does not eliminate specific low-order harmonics. Therefore, both

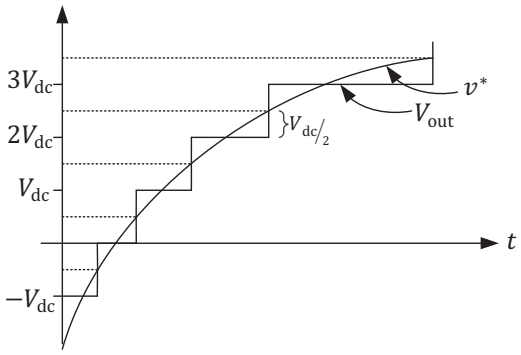


Fig. 2.19 The output voltage waveform using NLC.

NVC and NLC are not recommended for multilevel converters with reduced number of levels. Hence these methods are more suitable for converters with higher number of levels to avoid important low-order harmonics. The main advantages of NLC over other switching techniques is its simplicity in both implementation and concept, and efficiency improvement due to the low switching frequency.

2.4.4 Hybrid PWM (H-PWM)

This modulation technique is an extension of PWM for hybrid or asymmetric configuration (modular configurations with unequal DC sources). The basic idea of this modulation technique is to reduce the switching losses and improve the converter efficiency by reducing the switching frequency of the higher power cells. To do this, instead of using high-frequency carrier-base PWM for all cells, high power cells can be controlled at a fundamental switching frequency, while the low-power cells are controlled by using unipolar PWM. Detail description of this modulation technique can be found in [31].

The modulation techniques introduced in this chapter are based on having fixed DC sources as DC-links in multilevel converters. In the field of STATCOM, DC sources are replaced by capacitors. This is an important parameter that has to be taken into account when using any of the modulation techniques introduced in this chapter. More details about modification of the modulation techniques considering having capacitors as DC sources will be provided in Chapter 4.

2.5 Conclusion

Multilevel converters have become an attractive solution for high power applications. The most common multilevel converter topologies have been described in this chapter. Complexity both in control and hardware structure, reliability, modularity and efficiency as the most important parameters for high power applications are addressed for the described topologies. Several modulation techniques for multilevel converters were also briefly reviewed.

Chapter 3

Overall control of CHB-STATCOM

3.1 Introduction

CHB configurations (star and delta) present outstanding advantages as modularity, high power and high voltage capability using low rated components as compare with the other multilevel topologies. Nevertheless, these salient features require elaborated and not trivial control strategies due to the complexity of these configurations.

Control objectives of CHB-STATCOMs can be classified into two main categories: controlling the exchanging current and thereby the exchanging power between the converter and the grid, and ensure the capacitor voltage balancing among all cells. Several linear and non-linear approaches have been proposed for modular configuration based STATCOMs [49]. The simplest control strategy is based on linear PI controller implemented in the rotating dq-reference frame [8]. This method requires a robust synchronization method to transform AC quantities to DC.

It is also possible to directly control the AC quantities with a fast dynamic. This controller is based on instantaneous power theory in $\alpha\beta$- or three-phase system. The main advantage of this control strategy is that no synchronous transformation is needed. The simplest linear approach to implement this control strategy is the Proportional Resonant (PR) controller [50]. However, this controller has the restriction of constant frequency operation. Two main non-linear approaches to implement the controller for CHB-STATCOMs are hysteresis control [51] and MPC [52]. The main drawback of MPC when applied to CHBs with high number of levels is the high number of switching states that must be evaluated.

It is not easy to define which one of the control strategies achieves the best results. But it must be noted that computational burden is as important factor as the dynamic and steady state behaviors of the control strategy. Considering the actual devices for control purposes such as Digital Signal Processing (DSP) and Field Programmable Gate Array (FPGA), to implement an advanced control algorithm put a heavy restriction in choosing the control algorithm.

In this chapter the overall control of CHB-STATCOMs implemented in the rotating dq-reference frame is provided. Due to its uniform switching pattern and thus uniform power distribution among cells, PS-PWM is here considered as the modulator stage.

3.2 CHB-STATCOM modeling and control

3.2.1 System modeling

In order to be able to derive an adequate control algorithm, first the dynamic and steady-state modeling equations of the CHB-STATCOM should be defined. Through steady-state analysis, it is possible to calculate the reference voltages required to reach an arbitrary operating condition. This is especially useful to determine the capabilities of CHB-STATCOM through an open loop control. The CHB-STATCOMs with an arbitrary number of cells n per phase is shown in Fig. 3.1 and Fig. 3.2 in its star and delta configurations, respectively.

The voltage difference between grid and converter output voltages is supported by a passive filter in each phase, used to filter the harmonics in the injected current. For the delta configuration the filter is typically connected inside the delta; in this way the filter can handle the voltage difference between converter phases and limit the circulating current inside the delta.

The dynamic model of the system in Fig. 3.1 can be obtained using Kirchhoff's circuit law. In this analysis it is assumed that all the cells have equal DC-link capacitor, charged at the same voltage level; also, it is assumed that the AC voltage is equally shared among all the cells. The set of voltage-current equations on the AC side can be obtained as

$$\begin{aligned} L_{\mathrm{f}}\frac{di_{\mathrm{aY}}}{dt}+R_{\mathrm{f}}i_{\mathrm{aY}}+e_{\mathrm{a}} &= ns_{\mathrm{c}}^{\mathrm{a}}v_{\mathrm{dc}} \\ L_{\mathrm{f}}\frac{di_{\mathrm{bY}}}{dt}+R_{\mathrm{f}}i_{\mathrm{bY}}+e_{\mathrm{b}} &= ns_{\mathrm{c}}^{\mathrm{b}}v_{\mathrm{dc}} \\ L_{\mathrm{f}}\frac{di_{\mathrm{cY}}}{dt}+R_{\mathrm{f}}i_{\mathrm{cY}}+e_{\mathrm{c}} &= ns_{\mathrm{c}}^{\mathrm{c}}v_{\mathrm{dc}} \end{aligned} \tag{3.1}$$

where, $s_{\mathrm{c}}^{\mathrm{a}}$,$s_{\mathrm{c}}^{\mathrm{b}}$ and $s_{\mathrm{c}}^{\mathrm{c}}$ are the switching functions of the different cells in phase a,b and c (which can be $+1,-1$ and 0). R_{f} and L_{f} are the resistance and inductance of the filter reactor, respectively. n is the number of cells per phase and v_{dc} is the DC-link voltage of the cells. Using the exchanging active power between the grid and the converter, the dynamic equation of the DC side for one cell (for example in phase a) is obtained as

$$p=\frac{dw}{dt}=\frac{1}{2}C_{\mathrm{dc}}\frac{d(v_{\mathrm{dc}}^2)}{dt}=\frac{p_{\mathrm{a}}-\frac{R_{\mathrm{f}}|i_{\mathrm{aY}}|^2}{2}}{n}-\frac{v_{\mathrm{dc}}^2}{R_{\mathrm{dc}}} \tag{3.2}$$

where w and p are the energy stored in the DC-link capacitor and the active power flows in the cells respectively. C_{dc} is cell capacitor and R_{dc} is an additional resistor connected in parallel to the capacitor (not displayed in Fig. 3.1 and 3.2 for clarity of the figures) and represents the overall losses in the DC side; p_{a} is the active power absorbed from the grid in phase leg a. It is important to remark that (3.2) can be easily extended to the other two phases.

In order to simplify the dynamic equations, the switching functions are replaced with their fundamental component. The fundamental component is called modulation signal. For example for phase a

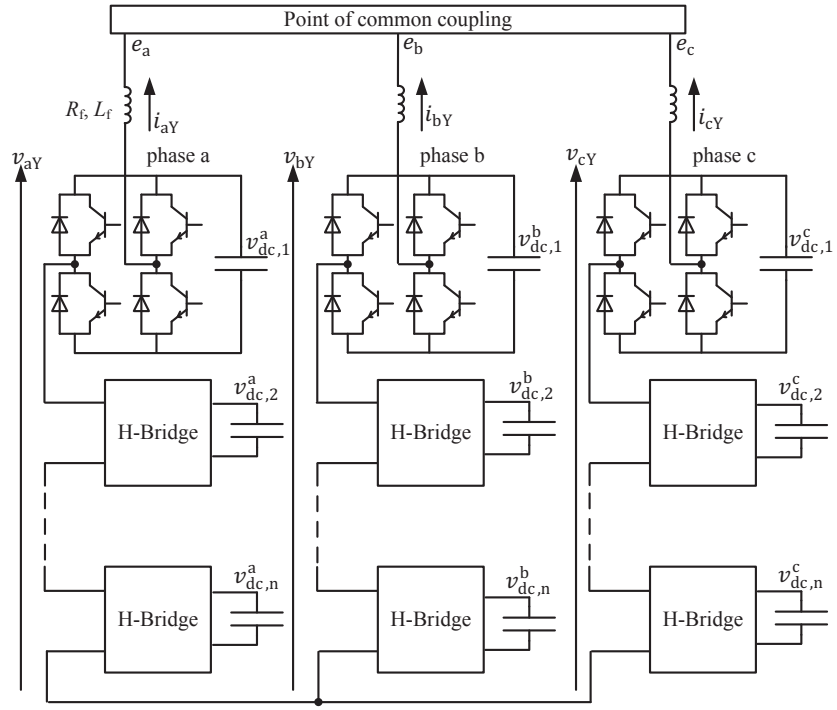


Fig. 3.1 Star configuration.

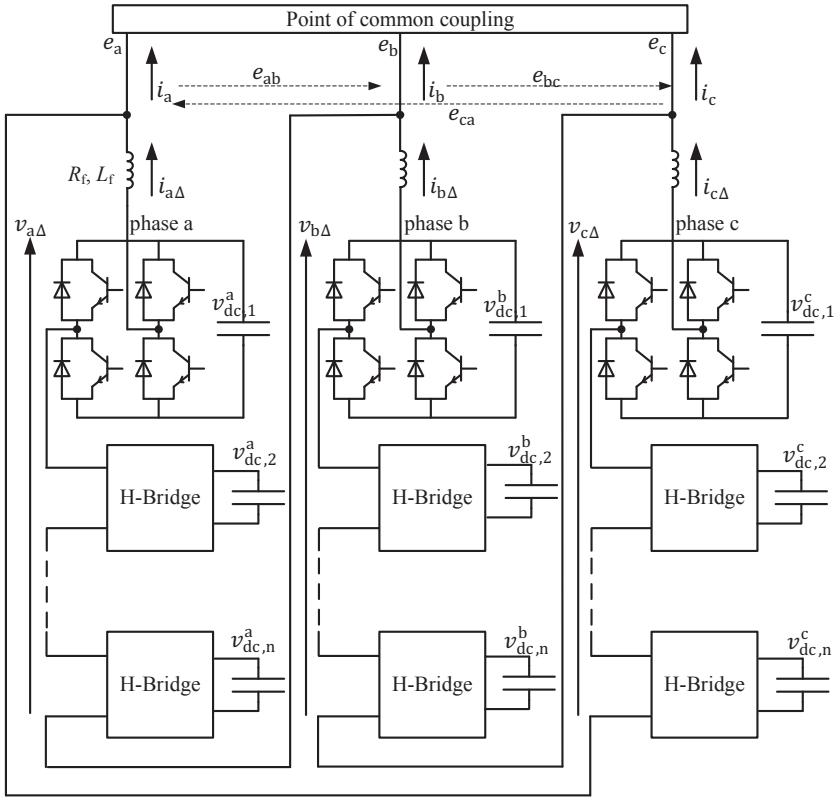


Fig. 3.2 Delta configuration.

$$s_{\mathrm{c}}^{\mathrm{a}} \cong m_{\mathrm{c}}^{\mathrm{a}} \tag{3.3}$$

where $m_{\mathrm{c}}^{\mathrm{a}}$ is the modulation signal for one cell in phase a.

Replacing (3.3) into (3.1) and applying Clarke transformation (described in the Appendix), the dynamic equation in the fixed $\alpha\beta$-frame can be written as

$$n\underline{m}_{\alpha\beta}(t)v_{\mathrm{dc}} - \underline{e}_{\alpha\beta}(t) - R_{\mathrm{f}}\underline{i}^{Y}_{\alpha\beta}(t) - L_{\mathrm{f}}\frac{d}{dt}\underline{i}^{Y}_{\alpha\beta}(t) = 0 \tag{3.4}$$

Having the transformation angle θ (the angle of the grid voltage vector) and using Park transformation (in Appendix) as

$$\begin{aligned}
\underline{m}_{\mathrm{dq}}(t) &= \underline{m}_{\alpha\beta}(t)e^{-\mathrm{j}\theta(\mathrm{t})} \\
\underline{e}_{\mathrm{dq}}(t) &= \underline{e}_{\alpha\beta}(t)e^{-\mathrm{j}\theta(\mathrm{t})} \\
\underline{i}^{Y}_{\mathrm{dq}}(t) &= \underline{i}^{Y}_{\alpha\beta}(t)e^{-\mathrm{j}\theta(\mathrm{t})}
\end{aligned} \tag{3.5}$$

(3.4) can be re-written in the rotating dq-reference frame as

$$n\underline{m}_{\mathrm{dq}}(t)v_{\mathrm{dc}} - \underline{e}_{\mathrm{dq}}(t) - R_{\mathrm{f}}\underline{i}^{Y}_{\mathrm{dq}}(t) - L_{\mathrm{f}}\frac{d}{dt}\underline{i}^{Y}_{\mathrm{dq}}(t) - L_{\mathrm{f}}j\omega\underline{i}^{Y}_{\mathrm{dq}}(t) = 0 \tag{3.6}$$

Re-arranging (3.2), the resulting dynamic equations in dq-frame are given by

$$\begin{aligned}
&L_{\mathrm{f}}\tfrac{d}{dt}\underline{i}_{\mathrm{dq}}(t) + R_{\mathrm{f}}\underline{i}_{\mathrm{dq}}(t) + \underline{e}_{\mathrm{dq}}(t) + j\omega L_{\mathrm{f}}\underline{i}_{\mathrm{dq}}(t) = n\underline{m}_{\mathrm{dq}}(t)v_{\mathrm{dc}} \\
&\tfrac{1}{2}C_{\mathrm{dc}}\tfrac{d(v_{\mathrm{dc}}^2)}{dt} = \tfrac{e_{\mathrm{d}}i_{\mathrm{d}} + e_{\mathrm{q}}i_{\mathrm{q}} - R_{\mathrm{f}}(i_{\mathrm{d}}^2 + i_{\mathrm{q}}^2)}{3n} - \tfrac{v_{\mathrm{dc}}^2}{R_{\mathrm{dc}}}
\end{aligned} \tag{3.7}$$

where ω is the angular frequency of the rotating vectors.

3.2.2 Steady-state analysis

In steady-state condition, the derivative terms are equal to zero. By setting the derivative terms in (3.7) to zero, the steady-state equations are calculated as

$$\begin{aligned}
\underline{M}_{\mathrm{dq}} &= \tfrac{R_{\mathrm{f}}\underline{I}_{\mathrm{dq}} + \underline{E}_{\mathrm{dq}} + j\omega L_{\mathrm{f}}\underline{I}_{\mathrm{dq}}}{nV_{\mathrm{dc}}} \\
0 &= \tfrac{E_{\mathrm{d}}I_{\mathrm{d}} - R_{\mathrm{f}}I_{\mathrm{d}}^2}{3n} + \tfrac{E_{\mathrm{q}}I_{\mathrm{q}} - R_{\mathrm{f}}I_{\mathrm{q}}^2}{3n} - \tfrac{V_{\mathrm{dc}}^2}{R_{\mathrm{dc}}}
\end{aligned} \tag{3.8}$$

where the use of capital letters denote the steady-state condition of the different quantities. In order to solve this equation, I_{q} and V_{dc} should be determined first. Usually, the desired value

for I_q is determined based on the required reactive power to be exchanged with the grid. If the dq-reference frame is synchronized with the grid voltage vector, the q component of the voltage ($E_q = 0$) can be considered equal to zero in steady-state. Thus, the desired value for I_q can be calculated as

$$Q^* = \mathrm{Im}\{\underline{E}_{dq}\underline{I}^*_{dq}\} = -E_d I_q + E_q I_d \Rightarrow I_q = -\frac{Q^*}{E_d} \tag{3.9}$$

where Q^* is the required reactive power. The DC voltage V_{dc} must be selected to a value that ensures the summation of all cells DC voltages at each phase is higher than the amplitude of the grid phase voltage, i.e.,

$$nV_{DC} > \frac{\sqrt{2}}{\sqrt{3}}\sqrt{E_d^2 + E_q^2} \Rightarrow V_{DC}|_{E_q=0} = k\frac{\sqrt{2}E_d}{\sqrt{3}n} \tag{3.10}$$

where k is a safety margin to guarantee proper operation of the converter, also in case of grid voltage transient; typically, k ranges between 1.1 and 1.15 [40].

Replacing V_{dc} and I_q in (3.8), the needed modulation signal corresponding to the specific operating condition can be calculated.

Just for illustration purposes, the following desired steady-state values in per unit and security margin of 15% for the DC-link voltage are here considered. The resulting modulation signals can be calculated as

$$\left.\begin{array}{l} n = 3 \\ E_d = 1\text{pu} \Rightarrow V_{DC} = 0.313\text{pu} \\ I_q = -1\text{pu} \\ L_f\omega = 0.15\text{pu} \\ R_f = 0.03\text{pu} \\ R_{dc} = 30\text{pu} \end{array}\right\rangle\left\langle\begin{array}{l} M_d = 0.9 \\ M_q = -0.03\text{pu} \\ I_d \cong 0\text{pu} \end{array}\right. \tag{3.11}$$

According to the calculated modulation signals, the safety margin of 15% ensures the proper operation of the converter without any over-modulation.

3.2.3 Control design and algorithm

The control method used for the CHB-STATCOMs consists of an inner current control loop, which is used to control the converter output current, and an outer cluster controller, used to control the DC capacitor voltages in each phase. Figure 3.3 shows the block diagram of the

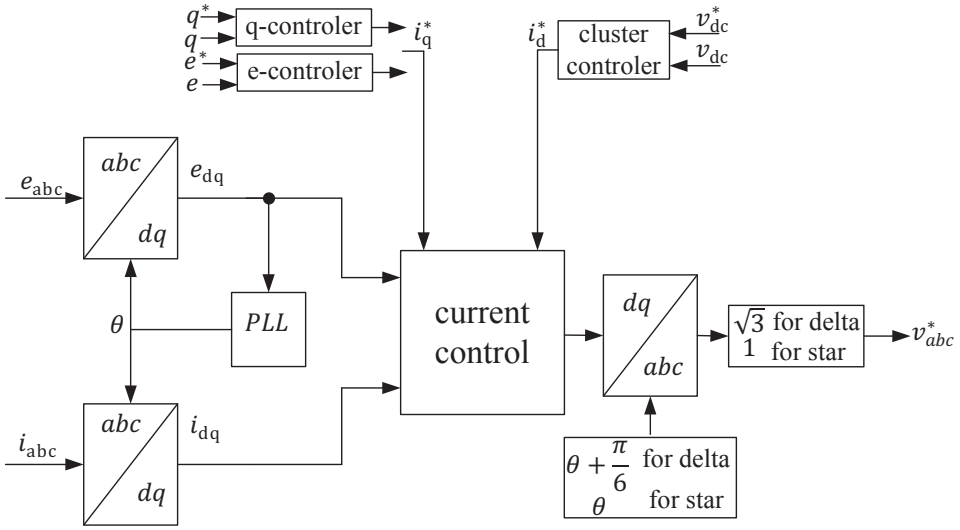


Fig. 3.3 Overall control block diagram of CHB-STATCOMs.

implemented control system. A Phase-Locked Loop (PLL) estimates the grid-voltage angle θ needed for the coordinate transformations. The cluster controller determines a reference value for the direct component of the current based on the selected DC-link voltage reference (v^*_{dc}). Reference value for the quadrature component of the current is determined either by the reactive power controller or voltage controller. Note that for the delta configuration the line-to-line reference quantities are required. Therefore, the outputs of the controller are transferred to three-phase using a transformation angle of $\theta + \frac{\pi}{6}$ and an amplification factor of $\sqrt{3}$. The main control blocks are described in the following.

Current control loop

To derive the control law, (3.7) can be written in the Laplace domain as

$$n\underline{m}_{\mathrm{dq}} v_{\mathrm{dc}} = \underline{e}_{\mathrm{dq}} + j\omega L_{\mathrm{f}} \underline{i}_{\mathrm{dq}} + (L_{\mathrm{f}} s + R_{\mathrm{f}}) \underline{i}_{\mathrm{dq}} \tag{3.12}$$

and therefore the law governing the current control is [8]

$$n\underline{m}_{\mathrm{dq}} v_{\mathrm{DC}} = (k_{\mathrm{p}} + \frac{k_{\mathrm{i}}}{\mathrm{s}})(\underline{i}^*_{\mathrm{dq}} - \underline{i}_{\mathrm{dq}}) + \underline{e}_{\mathrm{dq}} + j\omega L_{\mathrm{f}} \underline{i}_{\mathrm{dq}} \tag{3.13}$$

where i^*_{d} and i^*_{q} are the reference direct and quadrature currents, k_{p} is the proportional and k_{i} is the integral gain. Figure 3.4 shows the detailed current controller block diagram. The full control block diagram of the current controller together with the converter model is shown in Fig. 3.4(a). Simplified current controller block diagram and block diagram of the modulation signals calculation are shown in Fig. 3.4(b), top figure and Fig. 3.4(b), bottom figure respectively.

The proportional and integral gains of the implemented controller can be easily found shaping the closed-loop transfer function to have the same response as a first-order low-pass filter of bandwidth α_i, i.e.

$$G_i = \frac{i^*_{dq}}{i_{dq}} = \frac{sk_p + k_i}{L_f s^2 + s(R_f + k_p) + k_i} = \frac{\alpha_i}{s + \alpha_i} \tag{3.14}$$

Therefore, the proportional and integral gains can be found as

$$\begin{aligned} k_p &= \alpha_i L_f \\ k_i &= \alpha_i R_f \end{aligned} \tag{3.15}$$

Note that (3.12), (3.13), (3.14) and (3.15) are obtained for the star configuration. Considering the same filter impedances in each phase leg, the same equations can be written for the delta configuration except that one third of the actual value of the L_f and R_f should be considered. The ratio of one third is the delta to star impedance transformation.

Outputs of the current controller are direct and quadrature components of the reference voltage vector. In order to provide the modulation signal for each cell, the reference-voltage vector should be transferred to three-phase and normalized by the DC-link voltages. This is shown in Fig. 3.4(b) (bottom) where v^a_{dc1},...,v^a_{dcn} are the DC-link voltage values and m^a_{c1} ,..., m^a_{cn} are the modulation signals of the cells in phase *a*. With the same algorithm, modulation signals for the cells in other two phases can be obtained. These modulation signals are then sent to the modulator (for example, PS-PWM) to determine the switching patterns for the cells.

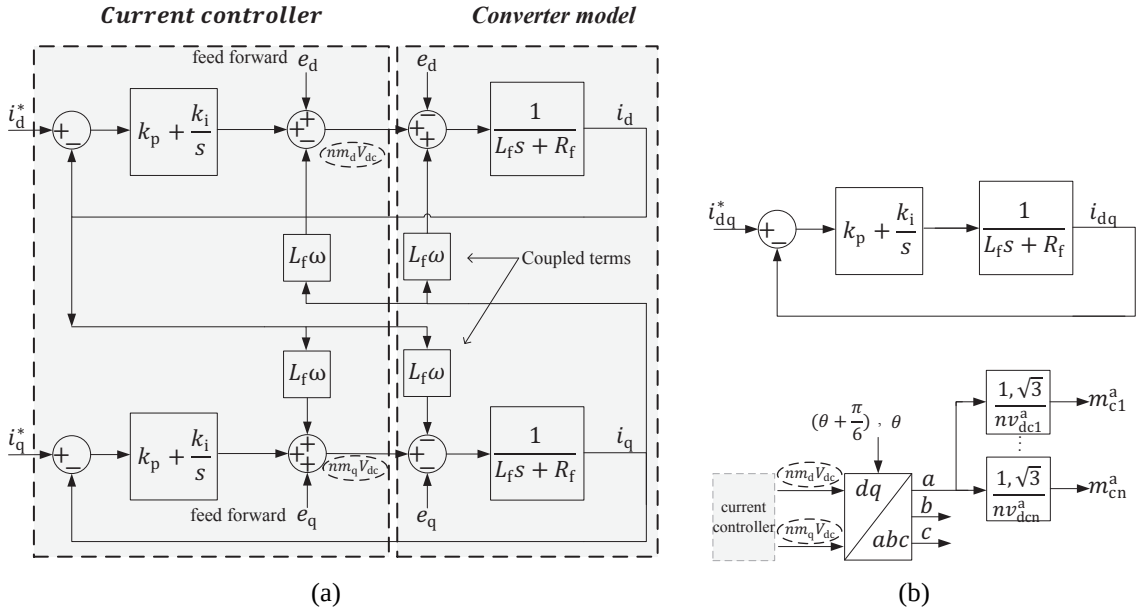


Fig. 3.4 Current control block diagram; (a): full-controller; (b-top): simplified controller; (b-bottom): cells modulation signal.

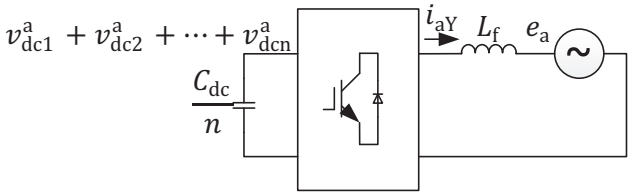


Fig. 3.5 Equivalent circuit of the star configuration for phase *a*.

Cluster control

The aim of the cluster controller is to generate the required reference direct-component of the current.

The equivalent circuit of the star configuration is shown in Fig. 3.5 for phase *a*. The DC capacitors are considered to be all in series. Assuming a loss-less system, the active power on the AC and on the DC side of the converter can be written as

$$p_{dc} = \frac{dw}{dt} = \frac{1}{2}\frac{C_{dc}}{n}\frac{d}{dt}(v^a_{dc1} + v^a_{dc2} + ... + v^a_{dcn})^2 = \frac{n}{2}C_{dc}\frac{d}{dt}(\frac{v^a_{dc1} + v^a_{dc2} + ... + v^a_{dcn}}{n})^2 =$$

$$= \frac{n}{2}C_{dc}\frac{d}{dt}(v_{cla})^2 \tag{3.16}$$

$$p_{ac} = \frac{|e_a||i_{aYd}|}{2}$$

where v_{cla} is called *cluster voltage* of phase *a* and is the average voltage of all the DC-link voltages in phase *a*. The active component of the three-phase current denoted by i_{aYd} for phase *a*, has the same phase angle of the grid voltage. Being the AC and DC side active powers equal, (3.16) can be written in Laplace domain as

$$nC_{dc}sv^2_{cla} = |e_a||i_{aYd}| \tag{3.17}$$

The term i_{aYd} is determined based on the desired DC-link voltage. Using a proportional controller having a gain of k_{clY}, all three phase direct currents can be written as

$$\begin{aligned} i_{aYd} &= k_{clY}(v^{*2}_{dc} - v^2_{cla})\cos(\theta) \\ i_{bYd} &= k_{clY}(v^{*2}_{dc} - v^2_{clb})\cos(\theta - 2\tfrac{\pi}{3}) \\ i_{cYd} &= k_{clY}(v^{*2}_{dc} - v^2_{clc})\cos(\theta + 2\tfrac{\pi}{3}) \end{aligned} \tag{3.18}$$

where $\cos(\theta)$ is used to generate AC currents that are in phase with the grid voltage; v^*_{dc} is the DC-link reference voltage and v_{cla},v_{clb},v_{clc} are the cluster voltages in phase *a*,*b*,*c*. The amplitude

of the active current component of phase *a* from (3.18) can be replaced into (3.17). Simplifying the results, the transfer function of the cluster controller for phase *a* can be calculated as

$$G_{\mathrm{cla}} = \frac{v_{\mathrm{cla}}^2}{v_{\mathrm{dc}}^{*2}} = \frac{k_{\mathrm{clY}}|e_{\mathrm{a}}|/nC_{\mathrm{dc}}}{s + k_{\mathrm{clY}}|e_{\mathrm{a}}|/nC_{\mathrm{dc}}} = \frac{\alpha_{\mathrm{cl}}}{s+\alpha_{\mathrm{cl}}} \tag{3.19}$$

which has the same response as a first-order low pass filter of bandwidth α_{cl}. The gain k_{clY} can then be designed for a desired bandwidth α_{cl} as

$$k_{\mathrm{clY}} = \frac{nC_{\mathrm{dc}}\alpha_{\mathrm{cl}}}{|e_{\mathrm{a}}|} \tag{3.20}$$

The resulting three-phase currents can then be transferred to the rotating *dq*-frame to generate the *d*-component of the reference current.

Following the same procedure, in order to generate the desired direct component of the current for delta configuration, the branch direct currents $i_{\mathrm{a\Delta d}}$,$i_{\mathrm{b\Delta d}}$ and $i_{\mathrm{c\Delta d}}$ must be in phase with their corresponding line-to-line voltage. Using a proportional controller with gain $k_{\mathrm{cl\Delta}}$three branch direct current can be written as

$$\begin{aligned} i_{\mathrm{a\Delta d}} &= k_{\mathrm{cl\Delta}}(v_{\mathrm{dc}}^{*2} - v_{\mathrm{cla\Delta}}^2)\cos(\theta + \tfrac{\pi}{6}) \\ i_{\mathrm{b\Delta d}} &= k_{\mathrm{cl\Delta}}(v_{\mathrm{dc}}^{*2} - v_{\mathrm{clb\Delta}}^2)\cos(\theta + \tfrac{\pi}{6} - 2\tfrac{\pi}{3}) \\ i_{\mathrm{c\Delta d}} &= k_{\mathrm{cl\Delta}}(v_{\mathrm{dc}}^{*2} - v_{\mathrm{clc\Delta}}^2)\cos(\theta + \tfrac{\pi}{6} + 2\tfrac{\pi}{3}) \end{aligned} \tag{3.21}$$

where $\cos(\theta + \frac{\pi}{6})$ is to make the branch direct currents in phase with the grid line to line voltage. The gain $k_{\mathrm{cla\Delta}}$ can be designed for a desired bandwidth α_{cl} as

$$k_{\mathrm{cla\Delta}} = \frac{nC_{\mathrm{dc}}\alpha_{\mathrm{cl}}}{|e_{\mathrm{ab}}|} \tag{3.22}$$

The line direct current i_{ad},i_{bd},i_{cd} are then calculated from the branch direct currents and the results are transferred to *dq*-reference frame to generate the desired reference direct current. The block diagram of the cluster controller is shown in Fig. 3.6.

It should be noted that only a proportional controller is chosen for the purpose of capacitor balancing. This is due to the fact that the DC-link voltages are not necessarily needed to be regulated at a certain voltage and a steady state error in DC-link voltage is acceptable as long as this voltage satisfies the security margin.

3.2.4 Phase-Locked Loop (PLL)

The objective of the PLL is to estimate the angle of the grid-voltage vector to perform the coordinate transformation. The PLL considered in this thesis is the one proposed in [53],[54].

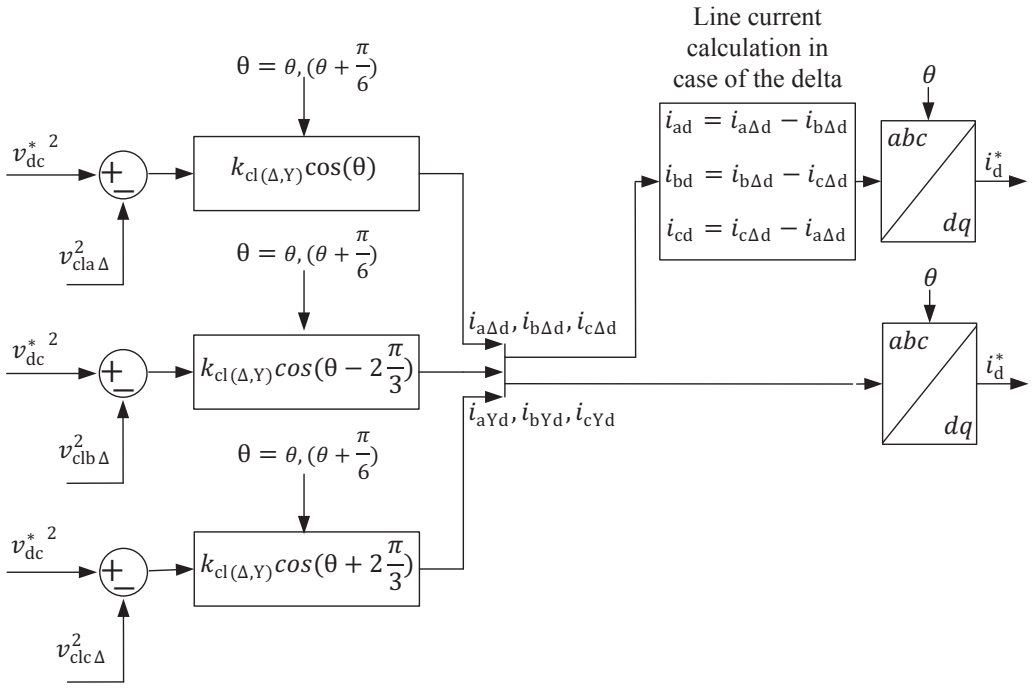


Fig. 3.6 Cluster controller block diagram.

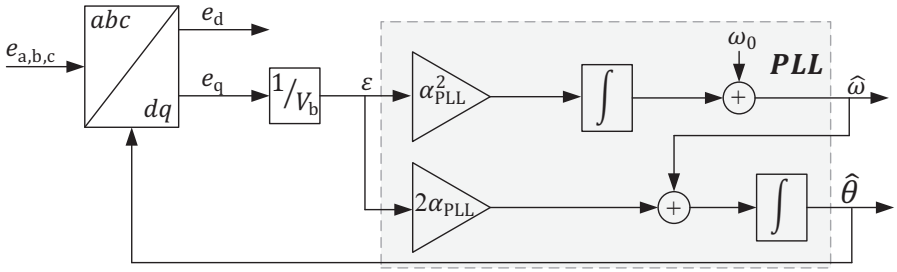


Fig. 3.7 Block diagram of PLL.

The law governing the PLL is given by

$$\begin{aligned} \frac{d\hat{\omega}}{dt} &= \alpha_{\mathrm{PLL}}^2 \varepsilon \\ \frac{d\hat{\theta}}{dt} &= \hat{\omega} + 2\alpha_{\mathrm{PLL}} \varepsilon \end{aligned} \tag{3.23}$$

where α_{PLL} is the closed-loop PLL bandwidth. The PLL should be robust against harmonics, grid voltage unbalances and faults. When fast synchronization is not needed, good harmonic rejection can be achieved by choosing a low bandwidth. The signal ε is the error input for the PLL (expressed in per-unit of the grid voltage amplitude V_{b}). A feed forward term with the fundamental AC frequency of $\omega_0 = 2\pi \times 50\ rad/s$ is added to achieve a faster tracking of the phase angle. Figure 3.7 shows the block diagram of the adopted PLL.

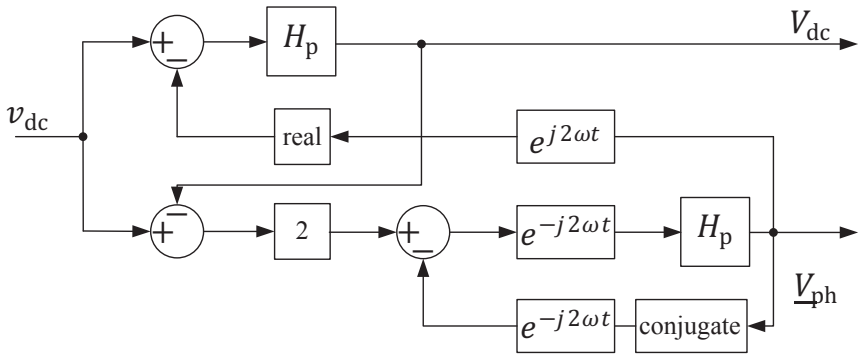


Fig. 3.8 Block diagram of single phase estimation algorithm.

3.2.5 DC-link filter design

In CHB-STATCOMs, the DC-link voltage of each cell contains a DC and a 100 Hz oscillatory components. The oscillatory component can produce harmful effects on the performance of the controller. Traditional methods to remove the 100 Hz component are Low-Pass Filter (LPF) and Moving-Average Filter (MAF), which are investigated and applied in [12]. An alternative way to separate the two frequency components in the measured DC voltage is to combine a LPF and a resonant filter with characteristic frequency centered at 100 Hz, as described in [55]. The advantage of this approach over the mentioned methods is that since the estimate of the oscillatory component is removed from the input signal to the LPF, higher bandwidth for the estimator can be used without jeopardizing its selectivity. To understand the principle of the implemented filter, let us assume that the input DC voltage v_{dc} comprises of an offset component (having amplitude of V_{dc}) and a sinusoidal contribution (having amplitude of V_{ph}) as

$$v_{dc} = V_{dc} + V_{ph}\cos(2\omega t) \tag{3.24}$$

Equation (3.24) can be rewritten as

$$v_{dc} = V_{dc} + \mathrm{Re}[\underline{V}_{ph}e^{j2\omega t}] = V_{dc} + \frac{\underline{V}_{ph}}{2}e^{j2\omega t} + \frac{\underline{V}^*_{ph}}{2}e^{-j2\omega t} \tag{3.25}$$

In order to extract the different components from the input signal, (3.25) can be re-arranged so that the phasors V_{dc} and V_{ph} become isolated and the LPF can be applied to the resulting signal as

$$\begin{aligned} V_{dc} &= H_p\{v_{dc} - \mathrm{Re}[\underline{V}_{ph}e^{j2\omega t}]\} \\ \underline{V}_{ph} &= H_p\{[2v_{dc} - 2V_{dc} - \underline{V}^*_{ph}e^{-j2\omega t}]e^{-j2\omega t}\} \end{aligned} \tag{3.26}$$

where H_p is a low pass filter of bandwidth α_{dc}. The block diagram of the single-phase estimation algorithm is depicted in Fig. 3.8

3.3 Digital control and main practical problems

The control algorithm described in this chapter has been derived in the frequency domain. However, the implemented control in the simulations is a digital control, where the control action is activated at each interrupt.

In order to improve the controller derived for ideal conditions, it is necessary to take into account some problems that occur in an actual system. One of the main problems in digital control is the delay due to the computational time of the control computer that affects the system performance. Moreover, it is important to consider that the amplitude of the output voltage is not infinite, but limited and proportional to the DC-link voltage level. For these reasons, some improvements are done to the described current controller. These improvements are the Smith predictor using a state observer for the computational time delay compensation and limitation of the reference voltage vector and anti-windup function to prevent integrator windup [56].

3.3.1 One-sample delay compensation

In the digital control the reference voltages from the controller is delayed one sampling period due to the computational time in the control computer. This delay will affect the performance of the system and cause overshoots and high oscillations during transients. To avoid this problem it is necessary to compensate for this delay.

In this work, a Smith predictor is used for this purpose. The main advantage of using Smith predictor is that the current controller can be treated as in the ideal case without any time delay. The basic idea of the Smith predictor is to predict the output current one sample a head by using a state observer and feed the predicted current back into the current controller. Thus, the delay of one sample has been eliminated. In order to feedback the real current to the current controller, the predicted current one sample delayed is subtracted from the feedback signal. The block scheme of the current controller with the computational time delay, the Smith predictor and the converter model (shown in Fig. 3.4(a)) is displayed in Fig. 3.9. The output of the Smith predictor is the difference between the estimated filter current at sample r, $\hat{\underline{i}}_{(\mathrm{dq})}(r)$ and the same signal at sample $r-1$,$\hat{\underline{i}}_{(\mathrm{dq})}(r-1)$. If at sample r a step in the reference current is applied, at sample $r+1$ the reference voltage $\underline{v}^{*}_{(\mathrm{dq})}$ output of the current controller will vary. Therefore, the output signal of the Smith predictor will not be equal to zero and will adjust the current error. At sample $r+2$ the difference between the predicted current and the delayed one will be zero again. Thus, the Smith predictor will affect the performance of the controller only during transients, but not during steady states.

For a correct estimation of the grid current, the state observer has to be designed in order to reproduce the converter model. Applying Kirchhoff's Voltage Law (KVL) to the circuit shown in Fig. 3.10, the following equation in the $\alpha\beta$-coordinate system can be written

$$\underline{v}_{\mathrm{c}}^{(\alpha\beta)}(t)-\underline{e}_{\mathrm{g}}^{(\alpha\beta)}(t)=R_{\mathrm{f}}\hat{\underline{i}}_{(\alpha\beta)}(t)+L_{\mathrm{f}}\frac{d}{dt}\hat{\underline{i}}_{(\alpha\beta)}(t) \tag{3.27}$$

In the dq-coordinate system, (3.27) becomes

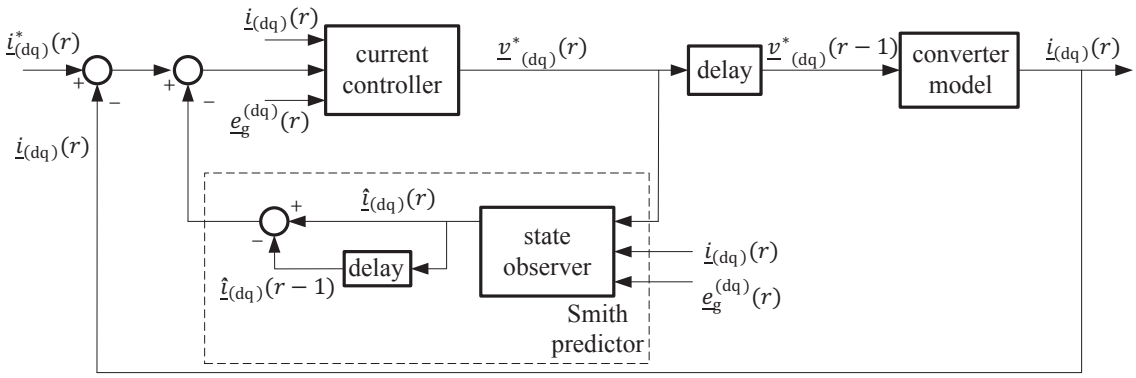


Fig. 3.9 Block scheme of the current controller with Smith predictor.

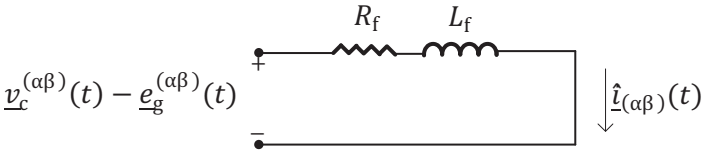


Fig. 3.10 Single-line diagram of circuit representation of state observer in time domain.

$$\underline{v}_c^{(dq)}(t) - \underline{e}_g^{(dq)}(t) = R_f \underline{\hat{i}}_{(dq)}(t) + L_f \frac{d}{dt}\underline{\hat{i}}_{(dq)}(t) + j\omega L_f \underline{\hat{i}}_{(dq)}(t) \tag{3.28}$$

which can be discretized using the forward Euler method. The grid voltage changes slowly compared with the sampling time, so it can be considered constant over one sampling period. The average value of the converter voltages over one sample period are equal to the reference values. Equation (3.28) can therefore be rewritten in the discrete time domain as

$$\begin{aligned}\underline{\hat{i}}_{(dq)}(r+1) = &\left(1 - \frac{R_f T_s}{L_f} - j\omega T_s\right)\underline{\hat{i}}_{(dq)}(r) + \frac{T_s}{L_f}\left(\underline{v}_c^{(dq)}(r) - \underline{e}_g^{(dq)}(r)\right) \\ &+ k_{psp}\left(\underline{i}_{(dq)}(r) - \underline{\hat{i}}_{(dq)}(r)\right)\end{aligned} \tag{3.29}$$

where k_{psp} is the observer gain. Thus, if k_{psp} is large, the observer does not trust the process model. If k_{psp} is small, the observer believes in the converter model.

To obtain the reference phase voltages, the reference voltage vector $\underline{v}^*_{(dq)}$ in the dq-coordinate system is transformed in the fixed $\alpha\beta$-coordinate system by using transformation angle $\theta(r) + \Delta\theta$, where $\Delta\theta = \omega T_s + 0.5\omega T_s$. $\Delta\theta$ is a compensation angle that takes into account the delay introduced by the discretization of the measured quantities ($0.5\omega T_s$), and the one sample delay due to the computational time (ωT_s). The reference voltage vector in the $\alpha\beta$-coordinate system is then given by

$$\underline{v}^*_{(\alpha\beta)} = \underline{v}^*_{(dq)} e^{j(\theta+\Delta\theta)} = \underline{v}^*_{(dq)} e^{j(\theta+\frac{3}{2}\omega T_s)} \tag{3.30}$$

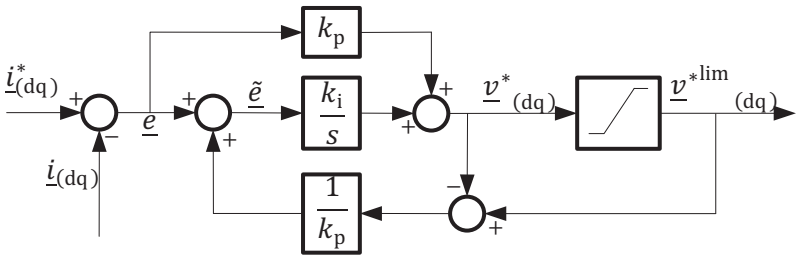


Fig. 3.11 Block scheme of the current controller with anti-windup.

3.3.2 Saturation and Integrator Anti-windup

Due to the limited attainable output voltage of the converter, a hard limiter must be used to limit the the reference voltage. If the controller limits the reference voltage then the input error to the integrator can not be set to zero. This leads to integrator windup. In order to avoid integrator windup, the integration should be inhibited whenever the reference voltage exceeds the maximum level. Alternatively, it is possible to use back-calculation of the current error in order to limit the demanded current during saturation [57]. In this case, if saturation occurs, the integrated current error will be modified in order to take into account the limited output voltage of the converter. The block scheme of the current controller with anti-windup is shown in Fig. 3.11. The input error to the integrator ($\tilde{\underline{e}}$) is modified as

$$\tilde{\underline{e}} = \underline{e} + \frac{1}{k_p}\left(\underline{v}^*_{(dq)} - \underline{v}^{*lim}_{(dq)}\right) \tag{3.31}$$

where $\underline{v}^{*lim}_{(dq)}$ is the limited reference voltage.

3.4 Simulation results

The CHB-STATCOMs with the system and control parameters of Table 3.1 are simulated in PSCAD in order to verify the implemented control strategy.

The highest bandwidth is assigned to the closed-loop current controller. This bandwidth is chosen based on the sampling frequency. Sampling points are located on the top and the bottom of each carrier and since there are three carriers and each carrier frequency is 1000 Hz then the sampling frequency will be 6000 Hz. For stability reasons, the rule-of-thumb is to select the bandwidth of the inner current controller at least a decay lower than the sampling frequency. Here, the closed-loop current control bandwidth is set to $(2\pi 500)^{\text{red}}/_{\text{sec}}$. In order to avoid any interaction between the current and cluster controller; the closed loop cluster controller bandwidth is chosen to be much slower than the closed loop current control bandwidth. For the PLL a low bandwidth of $(2\pi 5)^{\text{red}}/_{\text{sec}}$ is chosen to achieve a good harmonic rejection. Bandwidth of $(2\pi 50)^{\text{red}}/_{\text{sec}}$ is chosen for the DC-link filter to remove the 100 Hz oscillatory component and finally the observer gain of 0.1 is chosen.

TABLE 3.1. SYSTEM AND CONTROL PARAMETERS

Parameters	values
Rated power S_b	120 MVA,1 pu
Rated voltage V_b	33 kV,1 pu
System frequency f_g	50 Hz
Filter inductor L_f	4.33 mH,0.15 pu
Filter resistor R_f	0.136 Ω,0.015 pu
Cells capacitor C	4 mF,0.09 pu
DC-link voltage for star V_{dc}	10 kV,0.3 pu
DC-link voltage for delta V_{dc}	$10\sqrt{3}$ kV,0.525 pu
Cell numbers n	3
Carrier frequency f_{cr}	1000 Hz
Closed loop current control bandwidth α_i	$2\pi \times 500$ rad/sec
Closed loop cluster control bandwidth α_{cl}	$2\pi \times 5$ rad/sec
PLL bandwidth α_{PLL}	$2\pi \times 5$ rad/sec
Closed loop DC-link filter bandwidth α_{DC}	$2\pi \times 50$ rad/sec
Observer gain k_{psp}	0.1

Figure 3.12 shows the step performance of the CHB-STATCOMs. The figure on the left side shows the results for the star, while the right side figure shows the results for the delta. Top plots show the DC-link voltages (all cells) while middle plots show the reference (black) and the actual (gray) reactive current in the rotating dq-reference frame; bottom plots shows a detail of the step performance. This figure shows the ability of the controller to follow the desired DC-link voltage and reactive current values.

The simulation results in Fig. 3.12 are without considering the one-sample delay. As it mentioned earlier in digital implementation of the controller there will be one inevitable sample delay. Two digital implementation technique called synchronous and asynchronous reference voltage updating have been proposed in the literature [58, 59]. In the asynchronous technique the reference voltages for each cell is updated at each top and bottom of its own carrier while in the synchronous technique the reference voltages of all the cells are synchronously update at each interrupt. The advantage of the asynchronous technique is its simplicity in the implementation compare with the synchronous technique. However, the asynchronous technique can cause bigger overshoot at each transient as it will be shown in the next simulation results.

Figure 3.13 shows the transient performance of the CHB-STATCOMs with and without Smith predictor and by considering the one-sample delay in the implementation of the controller. The figures on the left side show the results for the star, while the right side figure show the results for the delta. Top plots shows the results with asynchronous technique and bottom plots show the results with synchronous technique. The overshoot and oscillation in the transient responses are due to the delay in the implementation of the controller. As it was expected, the overshoots are bigger when asynchronous technique is applied. It can also be observed that in both cases and for both configurations the Smith predictor improves the transient response. However, the Smith predictor is not so effective when asynchronous technique is applied. The reason is that in asynchronous technique the reference voltages for each cell is updated at each top and bottom

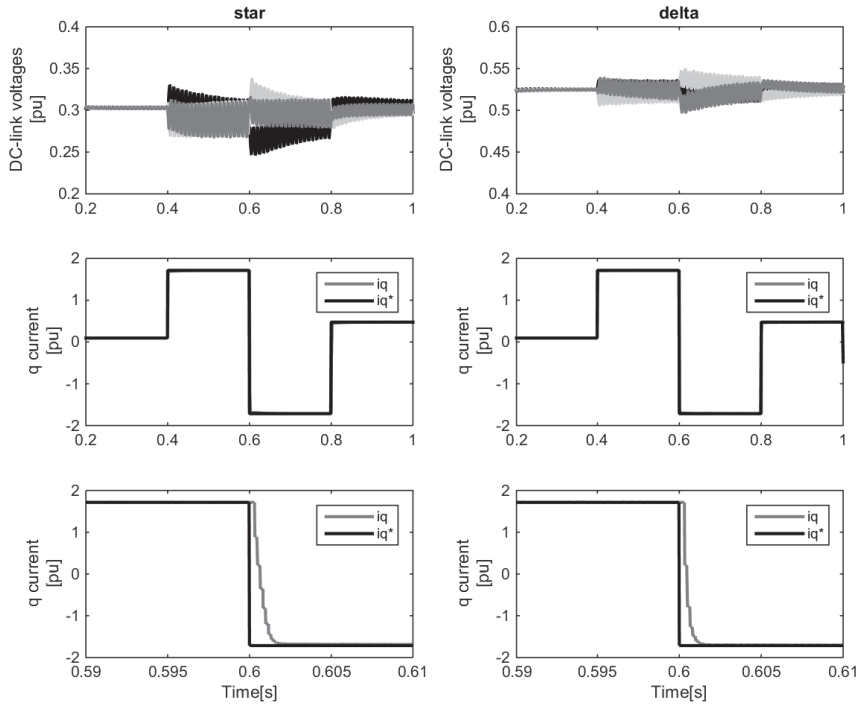


Fig. 3.12 Step performance of the CHB-STATCOMs; Top: capacitor cells voltages; middle: reference and actual injected reactive current; bottom: detail of the step performance.

of its own carrier. In consequence, once a step change is applied only one cell voltage reference is going to be updated in the next control period, while the other cells should wait until their carriers reach to the top or the bottom. This means that once a step change is applied only one cell reference voltage gets the advantage of the Smith predictor in the next control period. Therefore, asynchronous references update in PS-PWM does not allow the full benefit of the Smith predictor. For the synchronous technique, thanks to the synchronously updating the cell reference voltages, the Smith predictor can provide better improvement in the transient response as it can be observed from bottom plots.

For the simulation results shown so far, the DC voltage of the different cells in the CHB-STATCOM has been regulated by only using the cluster controller described in Section 3.2.3. This control loop would be sufficient in guaranteeing equal charge of the different capacitors of the converter if and only if the active power is equally distributed between the different cells. However, when using PS-PWM in actual implementations this cannot be guaranteed, due to different components characteristic, non-uniform switching pattern among the cells etc. Even in a simple simulation model, the time-step of the simulation will impact the active power distribution and thereby the charge of the different DC capacitors. As an illustrative example, consider the simulation results depicted in Fig. 3.14. For this simulation, the reference reactive power is set to 0.3 pu and is kept constant. From the figure, it is possible to observe that the DC-link voltages in the same phase leg will start to diverge from the reference value, while the cluster voltage (i.e., the average of the three DC-link voltages) is constant and properly controlled to its reference. This confirms that the active power is not distributed uniformly among the different cells, while the cluster controller properly manages to accomplish its duty. The

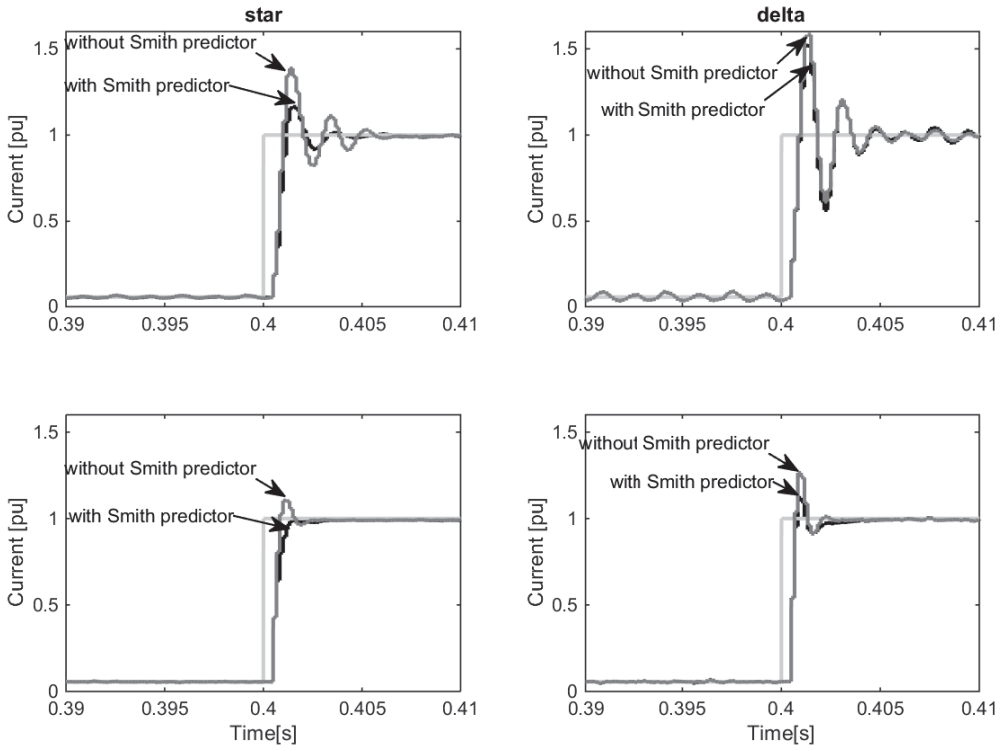


Fig. 3.13 Transient performance of CHB-STATCOMs with and without Smith predictor and with asynchronous (top plots) and synchronous (bottom plots) techniques.

reasons for this phenomenon together with the derivation of specific control loops to guarantee proper operation of the system will be investigated in the next chapter.

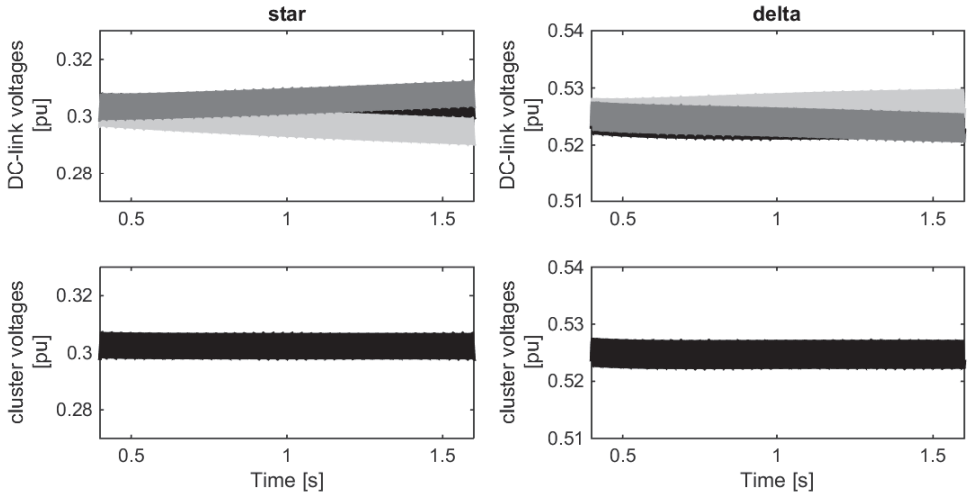


Fig. 3.14 Cluster and individual DC-link voltages of phase *a* for CHB-STATCOMs after 1.6 seconds; top: DC-link voltages; bottom: cluster voltages.

3.5 Conclusion

This chapter provides the overall controller for the CHB-STATCOMs. The controller consists of an inner current controller used to track the reference current and an outer cluster controller to control the DC-link voltages. Simulation results show the ability of the controller in tracking the reference current as well as DC-link voltage balancing. However, simulation results after 1.6 seconds show that the DC-link voltages inside one phase leg are diverging from the reference value due to the non-uniform active power distribution among different cells of the corresponding phase.

Chapter 4

CHB-STATCOM modulation and individual DC-link voltage balancing

4.1 Introduction

in case of non-uniform active power distribution among the cells that constitute the phase leg, the DC-link voltages diverge from the reference value. This non-uniform power distribution is mainly due to different characteristics of the components of the individual cells and, more in general, any condition that leads to a deviation from ideal conditions [60].

In the recent years, both manufacturers and researches have paid high effort to improve the control and the modulation of MMC. For the latter, Phase-Shifted Pulse Width Modulation (PS-PWM) has been extensively investigated in the literature [8]. It is shown in [60] that deviation from ideal condition affects the harmonic performance of the PS-PWM. This can negatively impact the active power distribution among the cells. However, not sufficient attention has been given to the investigation of the different harmonic components that are generated when using PS-PWM and their impact on the system performance, in particular in case of non-ideal conditions of the system.

The aim of this chapter is to extend the investigation of the impact of switching harmonics and the selection of a non-integer frequency modulation ratio on the voltage capacitor balancing when using PS-PWM. Theoretical analysis shows that by proper selection of the frequency modulation ratio, a more even power distribution among the different cells of the same phase leg can be achieved.

Although non-integer frequency modulation ratio improves the harmonic performances and provide more uniform active power distribution among cells, a completely uniform power distribution among cells is practically impossible. As a result, specific stabilization control loops (typically denoted as individual balancing control loop) are needed to guarantee a proper operation of the system.

The existing capacitor voltage-balancing strategies can be divided to two groups. First group consists of those strategies that need a dedicated individual balancing control algorithm [8].

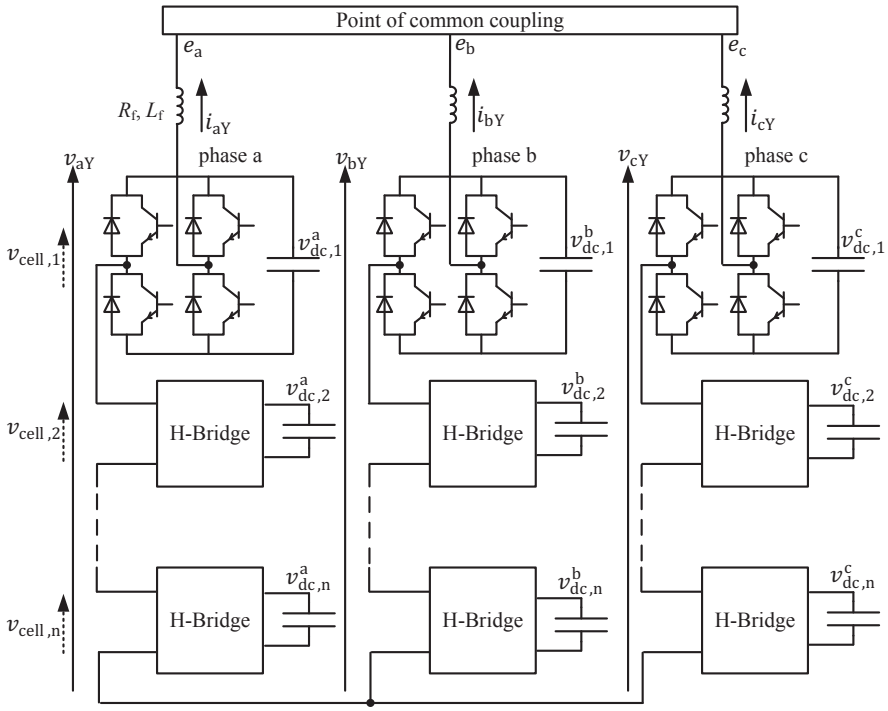


Fig. 4.1 Star configuration.

The second group is based on the technique called sorting algorithm [61].

In continuation of this chapter design process for individual DC-link voltage controller using both a dedicated controller and sorting algorithm is provided. It is shown that although both methods are successfully able to control the DC-link voltages when the converter is exchanging reactive power with the grid, they are not able to provide a proper DC-link voltage control when the converter is operating at zero-current mode. This chapter proposes two methods for capacitor voltage balancing at zero-current mode. First method is based on a modified sorting algorithm and second method is based on DC-link voltage modulation. Using the proposed methods, proper individual DC-link voltage balancing is achieved at zero-current mode.

4.2 Phase-shifted PWM harmonic analysis

The principle of PS-PWM has been explained in Section 2.4. Deviation from ideal condition affects the harmonic performance of the PS-PWM. This can negatively impact the active power distribution among the cells. Therefore the harmonic performance of PS-PWM is investigated in this section. The analysis is focused on the star configuration but is also valid for the delta. CHB-STATCOMs with an arbitrary number of cells *n* per phase is shown in Fig. 4.1 and Fig. 4.2 in its star and delta configurations, respectively.

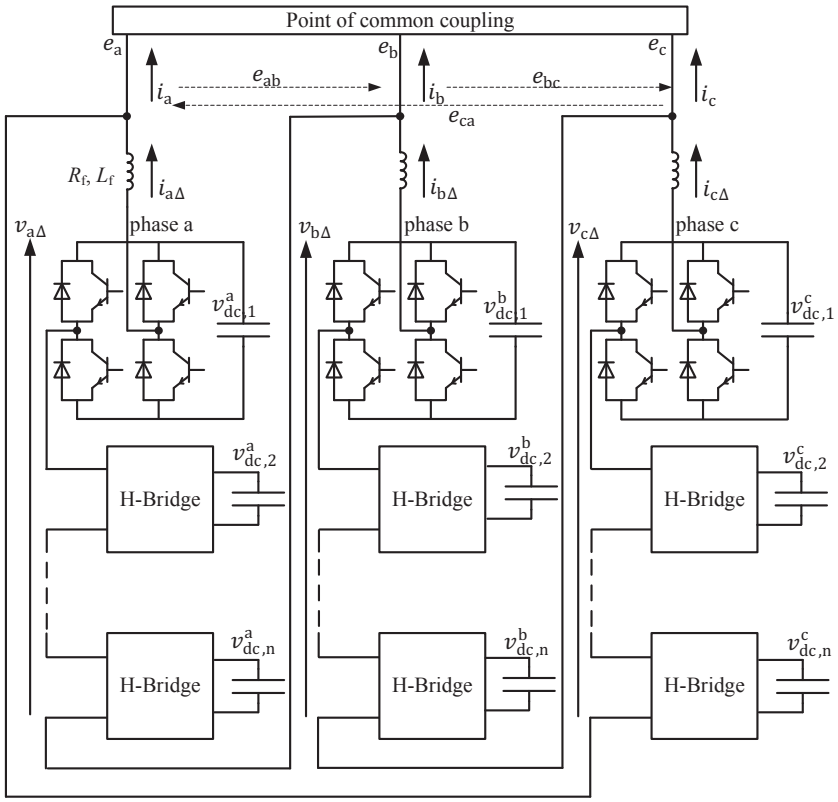


Fig. 4.2 Delta configuration.

The PS-PWM harmonic analysis here is focused on phase *a* of the star configuration (Fig. 3.1). Analogous considerations can be drawn for the other two phases. The switching pattern for the valves in the cells of the converter is here obtained using unipolar switching. As mentioned earlier, the basic principle of PS-PWM is to phase-shift the carriers for each cell in the same phase leg in order to cancel a specific set of harmonics in the total output voltage. Optimum harmonic cancellation is achieved by phase-shifting each cell carrier by $(k-1)\pi/N$, where N is the total number of cells in each phase and k refers to the cell number. Denoting with f_{cr} the carrier frequency, the selected phase-shift between the carriers allows cancellation of the harmonic components up to $2 f_{\mathrm{cr}} N$ in the total output phase voltage. Using asymmetrical regular sampled reference and double-edge carrier, the harmonic components of each cell in phase *a* can be found as [62]

$$\begin{aligned} V_{\mathrm{cell},k} = {} & \frac{4V_{\mathrm{dc}}}{\pi}\sum_{\mathrm{h}=1}^{\infty}\frac{M_{\mathrm{f}}}{h}J_{\mathrm{h}}\left(\frac{h\pi M_a}{2M_{\mathrm{f}}}\right)\sin\left(h\frac{\pi}{2}\right)\cos(h\omega_0 t)+ \\ & +\frac{4V_{\mathrm{dc}}}{\pi}\sum_{\mathrm{h}=1}^{\infty}\sum_{\mathrm{l}=-\infty}^{\infty}\frac{1}{q}J_{(2\mathrm{l}-1)}\left(q\frac{\pi}{2}M_a\right)\cos[(h+l-1)\pi]\times \\ & \times\cos\{[2h\omega_{\mathrm{cr}}+(2l-1)\omega_0]t+2h\frac{(k-1)\pi}{N}+(2l-1)\theta_0\} \end{aligned} \tag{4.1}$$

where V_{dc} is the DC-link voltage of the considered cell (all DC-link voltages are here assumed to be equal), ω_0 and ω_{cr} are the grid and carriers angular frequency, respectively, and θ_0 is the angle of the reference waveform. $M_f = {\omega_{cr}}/{\omega_0}$ is the frequency modulation ratio, M_a is the amplitude of modulation index in phase a, J is the Bessel function and $q = 2h + {(2l-1)}/{M_f}$. The term h represents the carrier index, while l is the side-band index. The overall output voltage of phase a is obtained by adding output voltage of all cells

$$V_{aY} = \sum_{k=1}^{n} V_{cell,k} \tag{4.2}$$

From (4.1) and (4.2) and considering, without loss of generality, $\theta_0 = 0$, yields

$$\begin{aligned} V_{aY} = {} & \frac{4NV_{dc}}{\pi} \sum_{h=1}^{\infty} \frac{M_f}{h} J_h\left(\frac{h\pi M_a}{2M_f}\right) \sin\left(h\frac{\pi}{2}\right) \cos(h\omega_0 t) + \\ & + \frac{4V_{dc}}{\pi} \sum_{h=1}^{\infty} \sum_{l=-\infty}^{\infty} \{\frac{1}{q} J_{(2l-1)}\left(q\frac{\pi}{2}M_a\right) \cos[(h+l-1)\pi] \times \\ & \times \sum_{k=1}^{n} \cos\{[2h\omega_{cr} + (2l-1)\omega_0]t + 2h\frac{(k-1)\pi}{N}\}\} \end{aligned} \tag{4.3}$$

Since

$$\sum_{k=1}^{n} \cos\{[2h\omega_{cr} + (2l-1)\omega_0]t + 2h\frac{(k-1)\pi}{N}\} = 0 \tag{4.4}$$

for all $h \neq N, 2N, 3N, \ldots$, the only harmonics remaining in the overall output voltage of phase a will be the side-band harmonic components centered around $2f_{cr}N$, or

$$\begin{aligned} V_{aY} = {} & \frac{4NV_{dc}}{\pi} \sum_{h=1}^{\infty} \frac{M_f}{h} J_h\left(\frac{h\pi M_a}{2M_f}\right) \sin\left(h\frac{\pi}{2}\right) \cos(h\omega_0 t) + \\ & + \frac{4V_{dc}}{\pi} \sum_{h=1}^{\infty} \sum_{l=-\infty}^{\infty} \frac{1}{q} J_{(2l-1)}\left(Nq\frac{\pi}{2}M_a\right) \cos[(Nh+l-1)\pi] \times \\ & \times \cos\{[2Nh\omega_{cr} + (2l-1)\omega_0]t\} \end{aligned} \tag{4.5}$$

Assuming for example that each phase leg of the star is constituted by three cascaded cells $(N = 3)$, the carriers will be relatively phase-shifted by $\pi/3$ and harmonic cancellation up to the side-bands around $2hf_{cr}N = 6f_{cr}, 12f_{cr}, \ldots$ will be achieved. Figure 4.3 illustrates the theoretical voltage-harmonic spectra of each cell output voltage (top) and of the total output phase voltage (bottom). The successive harmonic cancellation is evident.

Considering a perfectly balanced grid and under the assumption that the converter is not exchanging any negative-sequence current in steady state, the current harmonics for phase a can

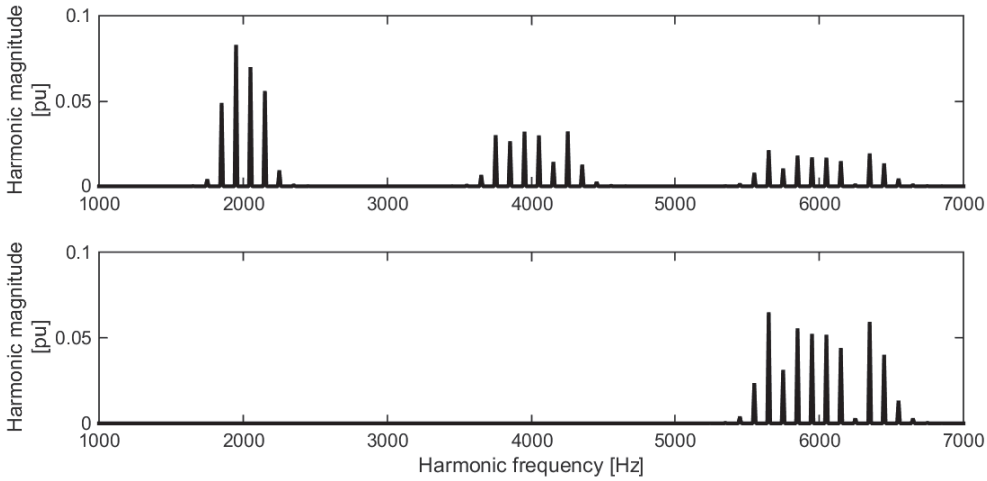


Fig. 4.3 Theoretical harmonic spectra; Top: cell output voltage; bottom: total phase leg *a* voltage. $N = 3$, $M_a = 0.9$, $M_f = 20$, $V_{dc} = 0.3$ *pu*

be calculated as[1]

$$I_{aY} = \frac{V_{aY} - E_a}{Z} \tag{4.6}$$

with Z the impedance of the filtering stage between the grid and the converter (calculated at the frequency of interest) and E_a the grid-voltage phasor for phase *a*. Observe that (4.6) considers the phase-to-neutral voltage V_{aY} for the computation of the line current and is therefore valid for single-phase systems only. In a three-phase CHB-STATCOM, the harmonic spectra in the current is determined by the phase-to-phase voltage; in the phase-to-phase voltage of the converter, some harmonics will be canceled [62] and therefore will not appear in the current waveform. However, this harmonic cancellation will not affect the analysis carried out in this thesis.

According with (4.6), the line current and phase voltage will present the same harmonic spectra, with the harmonic attenuation and phase change provided by the filter impedance. Observe that similar investigation can be performed for the delta configuration, where the grid phase voltage E_a in (4.6) must be replaced with the grid line-to-line voltage and V_{aY} must be replaced by $V_{a\Delta}$ in order to obtain the branch current $I_{a\Delta}$ (see Fig. 4.2).

4.2.1 Effect of side-band harmonics on the active power

The harmonic components in (4.1) can be divided into two main groups: fundamental component and side-band harmonics around it (first term in (4.1)), and carrier harmonics and their corresponding side-band harmonics (second term in (4.1)). In order to simplify the descrip-

[1] If the converter exchanges both positive- and negative-sequence current with the grid, the common-mode voltage of the converter must be controlled to a non-zero value to guarantee DC-voltage balancing. In this case, following the same approach described in this section, the contribution of positive- and negative-sequence components to the active power distribution between the cells can be evaluated using Fortescue Theory and superposition effect. Similar consideration holds for the delta configuration of the CHB-STATCOM.

tion, both the fundamental component and side-band harmonics around it are here denoted as base-band harmonics.

According to (4.1) and considering $N = 3$, the phase angle of the carrier side-band harmonics around $2hf_{cr}$ for each cell is equal to $2h(k-1)\pi/3$. These phase angles at $6f_{cr}$ $(h = 3)$ are equal to $0, 2\pi, 4\pi$ for each cell. Therefore, the harmonic components at $6f_{cr}$ are in phase with each other. Their amplitudes are also equal. On the other hand, the harmonic phase angles at $2f_{cr}$ $(h = 1)$ are equal to $0, 2\pi/3, 4\pi/3$ and at $4f_{cr}$ $(h = 2)$ are equal to $0, 4\pi/3, 2\pi/3$ for each cell. This means that the side-band harmonics for each cell around $2f_{cr}$ and $4f_{cr}$ have different phase angle.

Interaction between current and voltages harmonics with the same frequency can lead to active power, depending on their relative phase displacement. If this interaction occurs at carrier side-band harmonics around $2f_{cr}$ $(h = 1)$ or $4f_{cr}$ $(h = 2)$, the result will be a different active power flowing in the DC-link capacitor of the different cells, due to the difference in carrier phase angle described above. Both base-band and carrier harmonics of the current can interact with cell voltage harmonics. However, the interaction between cells voltage carrier harmonics and current base-band harmonics can only occur when low switching frequency for the cell is used, due to the essence of the Bessel function as it will be shown later in this section.

To investigate this interaction and its impact on active power distribution among cells, two case studies are here considered: low switching frequency for the cell (500 Hz and below, typical in systems with a high number of cells per phase leg) and high switching frequency (above 500 Hz, typical in systems with reduced number of cascaded cells per phase leg). Note that this distinction between low and high switching frequency is here intended as the possibility or not of interaction between voltage side-band harmonics and current base-band harmonics; this is dictated by the shape of the Bessel function in (4.1): practically, the Bessel function can be considered zero when $|l| > 10$, meaning that for frequencies above 500 Hz interaction between these group of harmonics can be neglected. Figure 4.4 shows a schematic representation of the different harmonic components and their location for both low (top) and high switching frequencies (bottom).

Case study #1, Low switching frequency

Considering 50 Hz grid frequency and, for example, 100 Hz switching frequency, it can be realized from the top plot in Fig. 4.4 that the voltage cell side-band harmonics correspond to $h = 1$ and $h = 2$; the base-band harmonics for the current are located at the same harmonic orders. This would indicate that for low switching frequency there are interactions between the cell voltage side-band harmonics and the base-band current harmonics. Since the phase angle of the cell voltage side-band harmonics corresponding to $h = 1$ and $h = 2$ are not equal, their interaction with the current base-band harmonics lead to different active power at each cell.

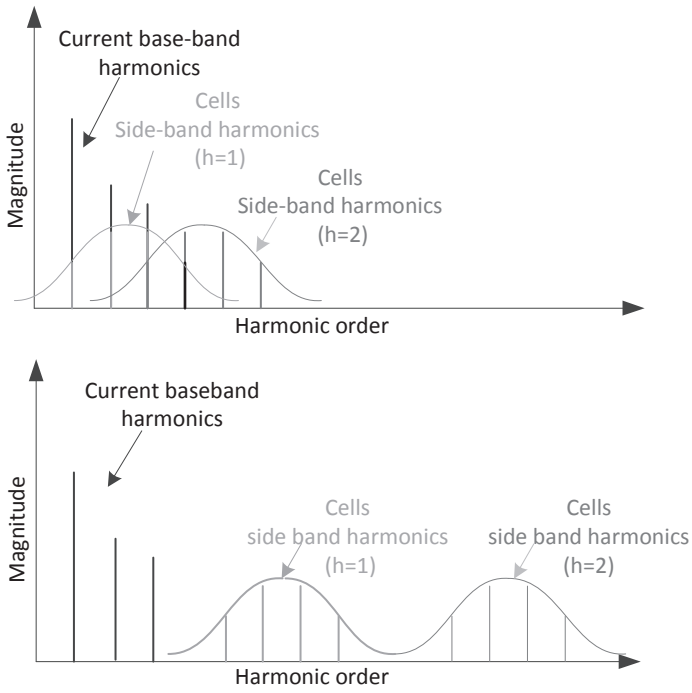


Fig. 4.4 Voltage and current harmonic spectra; Top: low switching frequency; bottom: high switching frequency.

Case study #2, High switching frequency

According to the bottom figure, for high switching frequency (here considered 1 kHz), no interaction occurs between the voltage cells side-band harmonics and the base-band current harmonics. This is because the interaction occurs in the side-band harmonics correspond to $h = 1$ and $l = -19$, and $h = 2$ and $l = -39$, where (as mentioned earlier) the Bessel function in (4.1) can be considered zero. This would indicate that for high switching frequency there is no interaction between voltage and current harmonics, thus the active power should be uniformly distributed between the different cells. However, interaction might still occur at carrier harmonics level.

To understand this, the star configuration is simulated in PSCAD with the system parameters reported in Table 3.1. Ideal DC sources are used instead of actual capacitors in the cells and a carrier frequency of 1 kHz for the high switching case and 100 Hz for the low switching case are considered. An illustrative example of the uneven active power distribution among the cells of the same phase leg is given in Fig. 4.5 for both low and high switching frequency case.

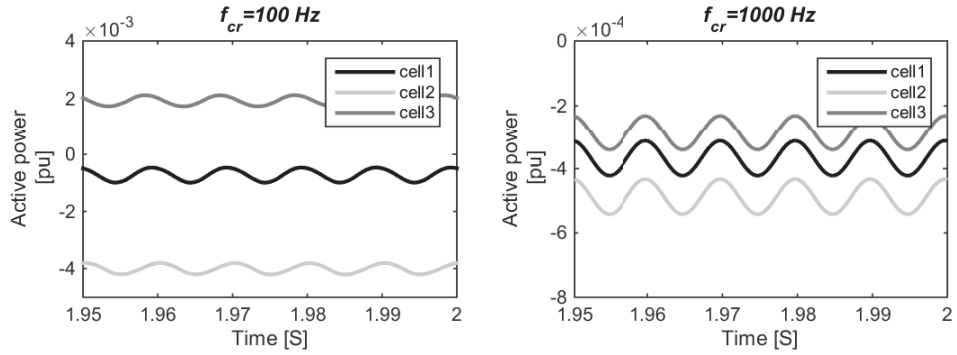


Fig. 4.5 Active power of each cells output after low pass filtering with cut off frequency of 20 Hz; Left: $M_\mathrm{f} = 2$; right: $M_\mathrm{f} = 20$.

Observe that the number of cells is kept equal for the two cases. When the switching frequency is low, there is always an interaction between cell voltage carrier harmonics and current base-band harmonics. If the switching frequency is high, the interaction is between the carrier harmonics only. As a result, the active power in the three cells is not equal. Observe that the total active power of one phase is not zero due to the losses in filter reactor and semiconductors elements.

In case of high switching frequency, the interaction occurs between voltage and current side-band harmonics. It has been shown that current carrier harmonics corresponding to $h = 1$ and $h = 2$ are canceled due to the phase-shift between carriers. However, the theoretical analysis presented earlier in this section is based on the assumption of a perfectly ideal converter. In such condition, the converter can be considered as a linear amplifier where the DC-link voltages in the different cells are equal, ideal carrier phase-shift is provided for each cell and no delays. Any deviation from ideal condition, such as diverge in DC-link voltages or non-ideal phase-shift in the carriers, will lead to non-ideal cancellation of the harmonic components in the total output voltage and consequently in the current. This can be seen from the voltage/current harmonic spectra in Fig. 4.6.

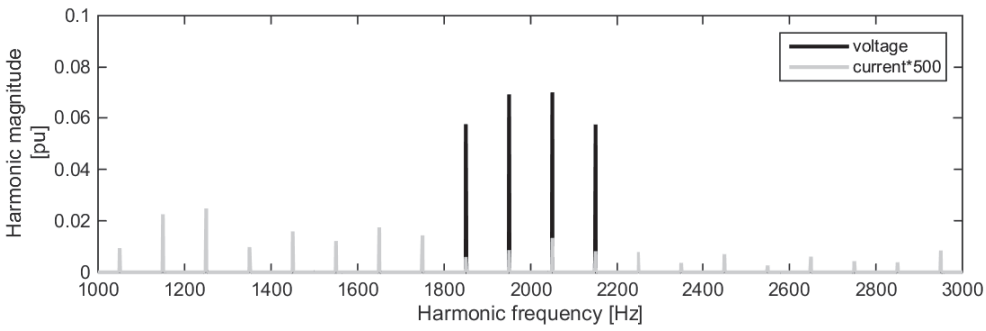


Fig. 4.6 Current and voltage carrier side-band harmonics at $h = 1$ in case of high switching frequency ($M_\mathrm{f} = 20$).

To quantify the effect of the harmonic interactions on the active power, the degree of unbalance

in the power is defined as

$$\Delta P = \frac{P_{\max} - P_{\min}}{P_{\text{ave}}} \tag{4.7}$$

with $P_{\max}$ and $P_{\min}$ the maximum and minimum active power among the cells and P_{ave} the average power. The degree of unbalance in Fig. 4.5 with $M_{\text{f}} = 20$ is 1.9, and with $M_{\text{f}} = 2$ is 8.32. Observe that the degree of unbalance at high switching frequency is much lower than the one at the low switching frequency, but still not zero. This indicates that in practical applications, where the DC sources are substituted with actual capacitors, in both cases the DC-link voltage of the cells will diverge. The DC-capacitor voltages will drift faster when low switching frequency is selected. This effect can be clearly seen in Fig. 4.7, where the same simulation has been performed when the ideal DC sources have been replaced with actual capacitors. For this simulation, the converter is exchanging 0.05 pu current with the grid and the needed control loop to guarantee the convergence of the voltage across the individual cells (see Section 4.3) has been intentionally disabled. The left and the right figure shows the capacitor voltages when using $f_{\text{cr}} = 250$ Hz and $f_{\text{cr}} = 1000$ Hz, respectively. Observe that, for clarity of the figure, a post-processing low-pass filter has been utilized to remove the oscillations in the measured capacitor voltage and thereby highlight the voltage divergence.

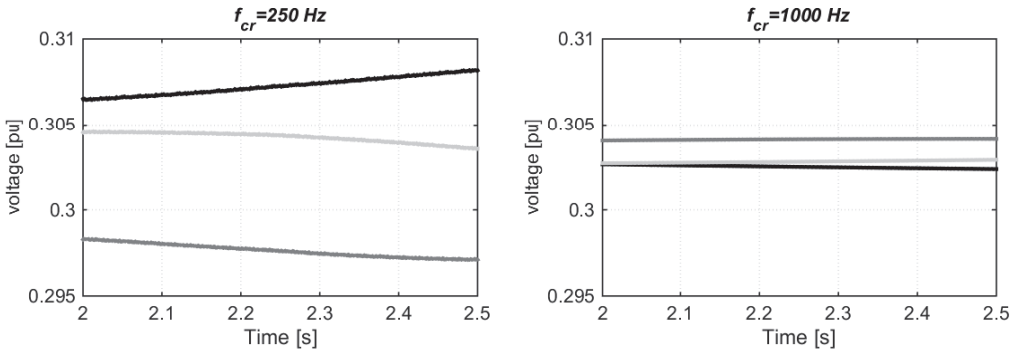


Fig. 4.7 Simulation results of capacitor voltages in phase *a* of the star configuration. Left: $f_{\text{cr}} = 250$ Hz; right: $f_{\text{cr}} = 1000$ Hz.

4.2.2 Selection of frequency modulation ratio

In case of low switching frequency and according to (4.1), base-band harmonics are located at $h\omega_0$ and carrier harmonics are located at $2h\omega_{\text{cr}} + (2l-1)\omega_0$. If the carrier frequency ω_{cr} is chosen to be non-integer multiple of fundamental frequency ω_0, the carrier harmonics will not be located at base-band harmonics and consequently the interaction between these two sets of harmonics will be removed. More details for this case can be found in [11]. Although the non-integer ratio effectively reduces the interaction between base-band and carrier harmonics (main problem with low switching frequencies), it can also provide an improvement for the carrier harmonic interactions (main problem with high switching frequencies). However, the case of high switching frequencies is more complicated and is investigated in the next section.

4.2.3 Impact of non-integer frequency modulation ratio for high switching frequencies

In case of high switching frequencies, the problem lies on the non-ideal cancellation of current carrier harmonics. As briefly mentioned earlier, the main reasons are: different modulation ratio among cells, different capacitors size tolerance, different DC-link voltage among cells, errors in carriers phase-shift that lead to different pulse width among cells [63]. Any kind of mismatch between the modulation of the single cells (for example, sampling delay, blanking time etc.) can also be the reason of failure in ideal carrier harmonics cancellation.

In practice there will be some non-zero error associated with the phase angle of the carrier waveforms. In order to show the impact of non-integer M_f in dealing with this error, the analysis here will be focused on one carrier harmonic component and the number of cells will be considered to be $N = 3$. The analysis can be extended to any other harmonic component and for any number of cells.

Considering $h = 1, l = 1$, $\theta_0 = 0$ and using (4.1) and (4.6), the output cell voltage and line current for phase a are

$$\begin{aligned} V_{\mathrm{cell},1} &= \underbrace{\frac{4V_\mathrm{dc}}{\pi}\frac{-M_\mathrm{f}}{2M_\mathrm{f}+1}J_{(1)}\left(\frac{2M_\mathrm{f}+1}{M_\mathrm{f}}\frac{\pi}{2}M_a\right)}_{V}\times \\ &\quad \times\cos[\underbrace{(2\omega_\mathrm{cr}+\omega_0)}_{\omega}t+2\theta_{\mathrm{cr}1}] = V\cos(\omega t+2\theta_{\mathrm{cr}1}) \\ V_{\mathrm{cell},2} &= V\cos(\omega t+2\theta_{\mathrm{cr}2}) \\ V_{\mathrm{cell},3} &= V\cos(\omega t+2\theta_{\mathrm{cr}3}) \end{aligned} \tag{4.8}$$

$$\begin{aligned} i_\mathrm{aY} = \frac{\sum_{\mathrm{i}=1}^{3} V_{\mathrm{cell,i}}}{Z_\omega} = \frac{V}{Z_\omega}[&\cos(\omega t+2\theta_{\mathrm{cr}1}-\angle Z_\omega)+ \\ &+\cos(\omega t+2\theta_{\mathrm{cr}2}-\angle Z_\omega)+ \\ &+\cos(\omega t+2\theta_{\mathrm{cr}3}-\angle Z_\omega)] \end{aligned} \tag{4.9}$$

where $\theta_{\mathrm{cr}1}, \theta_{\mathrm{cr}2}, \theta_{\mathrm{cr}3}$ are the initial phase angles of the carriers for each cell and $\angle Z_\omega$ is the filter impedance angle, here considered equal to $\pi/2$ (pure inductive filter).

Before proceeding in the calculation of the active power for each cell, the initial phase angle of the carriers $\theta_{\mathrm{cr}1}$, $\theta_{\mathrm{cr}2}$, $\theta_{\mathrm{cr}3}$ should be determined. Figure 4.8 shows as an example a comparison between a carrier with integer carrier frequency ratio of $M_\mathrm{f} = 2$ ($f_\mathrm{cr} = 100$ Hz with solid line) and non-integer carrier frequency ratio of $M_\mathrm{f} = 1.8$ ($f_\mathrm{cr} = 90$ Hz with dashed line). Observe that for this figure M_f is set small for clarity of the illustration. It can be seen from the figure that unlike the integer case, the initial phase of the carrier at the beginning of each fundamental period ($t = 0.02$ s, $t = 0.04$ s, ...) is not fixed when non-integer frequency modulation ratio is applied.

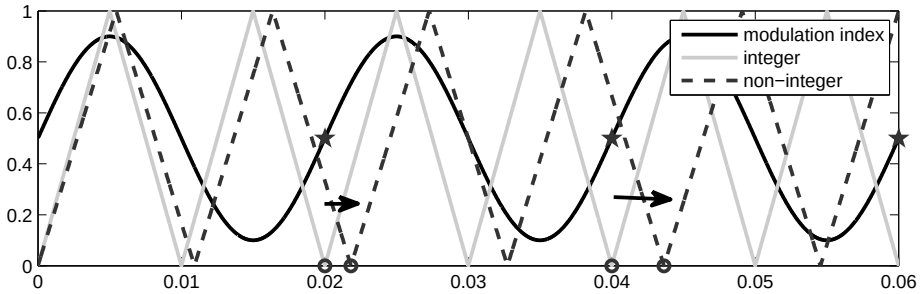


Fig. 4.8 Comparison between modulation index and carrier with integer ($f_{\text{cr}} = 100Hz$) and non-integer ($f_{\text{cr}} = 90Hz$) ratio.

Assume that the carrier initial phase angle in the first fundamental cycle is equal to zero and let us denote with f_{cri} the carrier frequency in case of an integer M_{f}, while f_0 is the system fundamental frequency. For a non-integer M_{f}, the corresponding carrier frequency, f_{crn}, can be represented as

$$f_{\text{crn}} = f_{\text{cri}} \pm \frac{\theta f_0}{2\pi} \tag{4.10}$$

with θ the relative phase-shift between two carriers after one fundamental cycle. Alternatively, after half of a fundamental cycle we get

$$f_{\text{crn}} = f_{\text{cri}} \pm \frac{\theta f_0}{\pi} \tag{4.11}$$

Therefore, for analysis purpose the carrier frequency for the non-integer case can be represented as the sum of the frequency f_{cri} and an additional term that takes into account the relative phase-shift between the two carriers. Considering, as an example, 1 kHz and 100 Hz as high and low switching frequencies, the corresponding non-integer frequency that provides $\pi/3$ initial phase angle after one fundamental period for this example can be 1008.3 Hz or 991.7 Hz for the high and 108.3 Hz or 91.7 Hz for the low switching frequency.

Using (4.11), the initial carrier phase angles after each half of a fundamental period is

$$\begin{aligned}
\theta_{\text{cr1}} &= \underbrace{\frac{\pi(f_{\text{crn}} - f_{\text{cri}})}{f_0}(h_{\text{f}} - 1)}_{\theta_1} + \varepsilon_{\text{n}}(\theta_1) \\
\theta_{\text{cr2}} &= \underbrace{\frac{\pi}{3} + \frac{\pi(f_{\text{crn}} - f_{\text{cri}})}{f_0}(h_{\text{f}} - 1)}_{\theta_2} + \varepsilon_{\text{n}}(\theta_2) \\
\theta_{\text{cr3}} &= \underbrace{\frac{2\pi}{3} + \frac{\pi(f_{\text{crn}} - f_{\text{cri}})}{f_0}(h_{\text{f}} - 1)}_{\theta 3} + \varepsilon_{\text{n}}(\theta_3)
\end{aligned} \tag{4.12}$$

where h_{f} refers to the half period number. For example, to find the phase angle of each carrier after three half period, h_{f} should be set to 3. The term ε_{n} in (4.12) is introduced to model any phase-shift error between the carriers, which is unavoidable in practical implementations. This error function is difficult to quantify but a function that provides a unique error for each initial phase angle can be considered as

$$\varepsilon_{\mathrm{n}}(\theta) = k_{\mathrm{n}}\theta \tag{4.13}$$

with k_{n} a constant coefficient. It should be noted that the selection of this error function does not affect the final result.

The active power for each cell calculated over a given number of half-cycles ($h_{\mathrm{f}} = h_{\mathrm{fd}}$) for a given non-integer carrier frequency can be obtained by multiplying the current and voltage in (4.8) and extracting the constant terms, as

$$\begin{aligned}
P_{\mathrm{cell},1} &= \tfrac{V^2}{2Z\omega h_{\mathrm{fd}}} \sum_{h_{\mathrm{f}}=1}^{h_{\mathrm{fd}}} [-\sin(2\theta_{\mathrm{cr1}} - 2\theta_{\mathrm{cr2}}) - \sin(2\theta_{\mathrm{cr1}} - 2\theta_{\mathrm{cr3}})] \\
P_{\mathrm{cell},2} &= \tfrac{V^2}{2Z\omega h_{\mathrm{fd}}} \sum_{h_{\mathrm{f}}=1}^{h_{\mathrm{fd}}} [-\sin(2\theta_{\mathrm{cr2}} - 2\theta_{\mathrm{cr3}}) - \sin(2\theta_{\mathrm{cr2}} - 2\theta_{\mathrm{cr1}}))] \\
P_{\mathrm{cell},3} &= \tfrac{V^2}{2Z\omega h_{\mathrm{fd}}} \sum_{h_{\mathrm{f}}=1}^{h_{\mathrm{fd}}} [-\sin(2\theta_{\mathrm{cr3}} - 2\theta_{\mathrm{cr2}}) - \sin(2\theta_{\mathrm{cr3}} - 2\theta_{\mathrm{cr1}}))
\end{aligned} \tag{4.14}$$

and in general, for N number of cells is

$$\begin{aligned}
P_{\mathrm{cell},k} &= \tfrac{V^2}{2Z\omega h_{\mathrm{fd}}} \sum_{h_{\mathrm{f}}=1}^{h_{\mathrm{fd}}} \sum_{\substack{\mathrm{n_n}=1 \\ \mathrm{n_n}\neq \mathrm{k}}}^{\mathrm{N}} -\sin(2\theta_{\mathrm{crk}} - 2\theta_{\mathrm{crn_n}}) \\
\theta_{\mathrm{cri}} &= \underbrace{\frac{\pi(i-1)}{N} + \frac{2\pi(f_{\mathrm{crn}} - f_{\mathrm{cri}})}{2f_0}(h_{\mathrm{f}} - 1)}_{\theta_i} + \varepsilon_n(\theta_i)
\end{aligned} \tag{4.15}$$

The final goal is to find a value for $f_{\mathrm{crn}} - f_{\mathrm{cri}}$ that provides an equal active power in all cells in the minimum time, i.e. in the minimum possible number of h_{fd}, in order to minimize the deviation in the capacitor voltages.

According to (4.14) the term $\frac{V^2}{2Z\omega h_{\mathrm{fd}}}$ is the same for each cell and thus it can be ignored in the calculation of the power since it has the same effect on each cell. Considering $N = 3$, $k_{\mathrm{n}} = 0.01$, $f_0 = 50$ Hz, Fig. 4.9 shows the active power of each cell as a function of the term $f_{\mathrm{crn}} - f_{\mathrm{cri}}$. The top plot shows the active power over one half period, second plot shows the active power over two half periods, third plot shows the active power over three half periods. As it can be observed, only when selecting $h_{\mathrm{fd}} = 3$ equal active power can be achieved (with $f_{\mathrm{crn}} - f_{\mathrm{cri}} = 16.67$ Hz). Close up picture of this case is shown in the bottom plot.

The same process is implemented for different number of cells (i.e. $N = 4, 5, \ldots$) and the results are shown in Fig. 4.10. The top plot shows the minimum number of half periods needed to achieve equal active power among cells, while bottom plot shows the corresponding $f_{\mathrm{crn}} - f_{\mathrm{cri}}$ value (lowest value).

By curve fitting the obtained results, the optimum solution for $f_{\mathrm{crn}} - f_{\mathrm{cri}}$ that provides equal active power among cells in the minimum number of half cycle period is

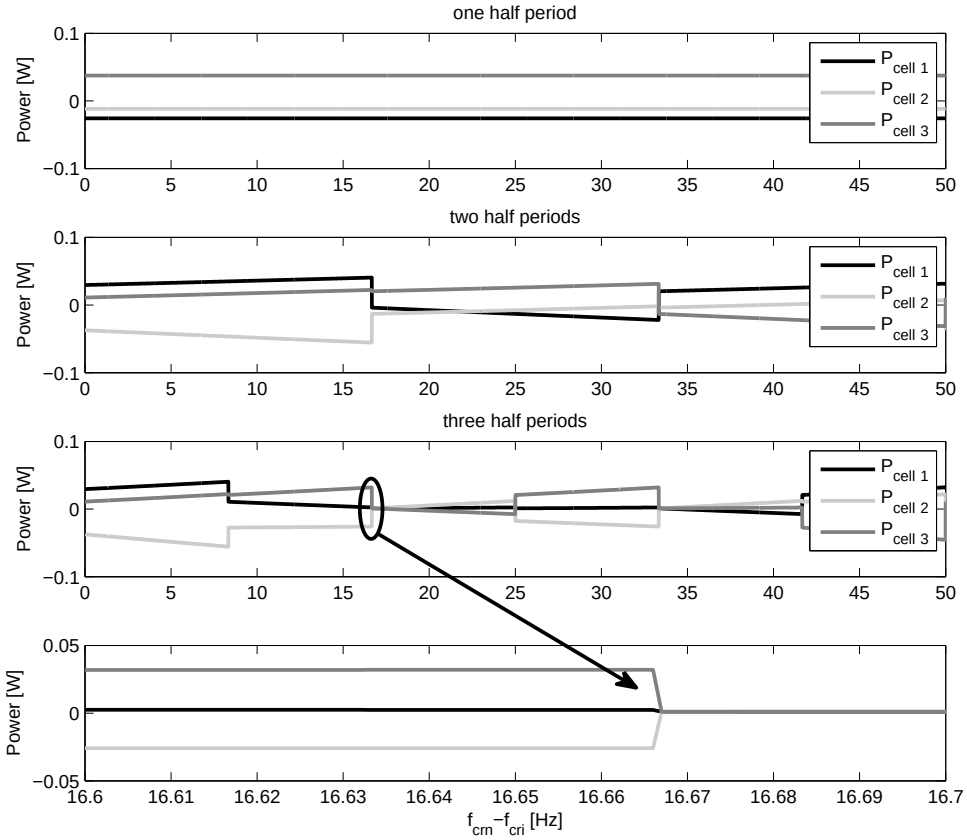


Fig. 4.9 Active power of each cell for $N = 3$; First on top: after one half period; second: after two half periods; third: after three half periods; forth: close up picture for three half periods.

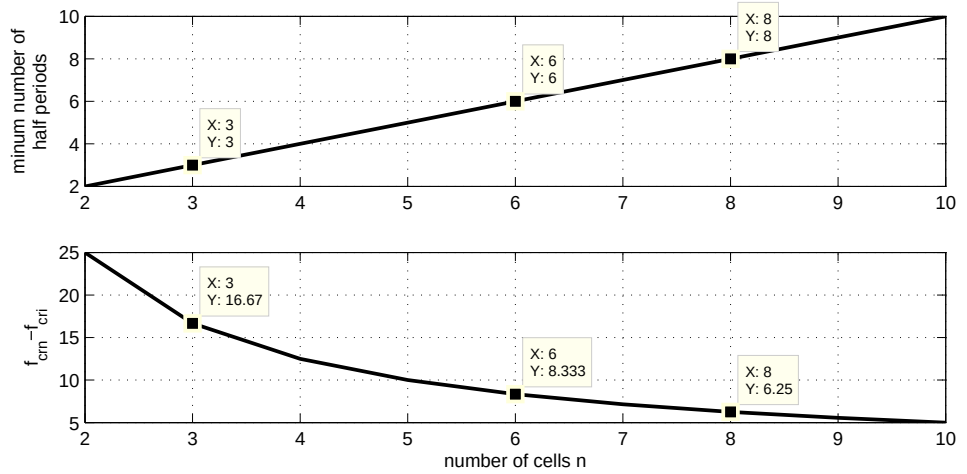


Fig. 4.10 Active power and minimum number of half period for different number of cells; top: minimum number of half period; bottom: $f_{\text{crn}} - f_{\text{cri}}$ value.

$$f_{\text{crn}} - f_{\text{cri}} = \pm\frac{f_0}{N} \tag{4.16}$$

For example, choosing the integer carrier frequency of 1 kHz and for a fundamental frequency of 50 Hz, the corresponding non-integer frequency for $N = 3$ is 1016.66 Hz or 983.33 Hz. Following the same procedure, the optimum solution for $f_{\text{crn}} - f_{\text{cri}}$ that provides equal active power among cells but in minimum number of full fundamental cycles (instead of half cycles) is

$$f_{\text{crn}} - f_{\text{cri}} = \pm\frac{f_0}{2N} \tag{4.17}$$

Similar to the previous example, choosing the integer carrier frequency of 1 kHz, the corresponding non-integer frequency for $N = 3$ is 1008.33 Hz or 991.66 Hz. Both of these frequencies provide the same results. In the following simulation results the higher switching frequency is chosen.

4.2.4 Simulation results

The star configuration with system parameters in Table 3.1 and using DC sources instead of actual capacitors is simulated in PSCAD with integer and non-integer frequency modulation ratio for both low and high switching frequencies. Figure 4.11 shows the output active power of each cell in phase *a* for different carrier frequencies. Low-pass filtering with cut off frequency of 20 Hz is applied to enhance the difference in the cells active power.

As discussed earlier, using integer carrier frequencies of 100 Hz and 1 kHz leads to different active power among the cells. As described in Section 4.2.3, optimum non-integer carrier frequencies that provides equal active power in minimum number of half-fundamental cycle are 116.66 Hz and 1016.66 Hz; similarly, optimum non-integer carrier frequencies which provides equal active power in minimum number of full-fundamental cycle are 108.33 Hz and 1008.33 Hz. It can be seen that although both 116.66 Hz, 1016.66 Hz and 108.33 Hz, 1008.33 Hz provide equal active power among cells, the selection of 116.66 Hz or 1016.66 Hz leads to less deviation in the cell active powers. Carrier frequencies of 125 Hz and 1025 Hz are examples of non-optimal non-integer carrier frequency. It can be seen from Fig. 4.11 (bottom) that, regardless the use of a non-integer M_f, the active powers are not equal in this case.

In order to show the effect of the frequency modulation ratio on voltage balancing of the capacitors, the ideal DC sources in the cells are replaced with actual capacitors. For these simulations, the star configuration is controlled to inject 0.052 pu reactive power into the grid. Figure 4.12 shows the capacitors voltages in phase *a* when using carrier frequencies of $f_{\text{cr}} = 1000$ Hz, 1008.3 Hz, 1016.6 Hz and 1025 Hz. Observe that while with $f_{\text{cr}} = 1000$ Hz the capacitor voltages will deviate from the desired value, the use of a non-integer carrier frequency of $f_{\text{cr}} = 1016.6$ Hz or $f_{\text{cr}} = 1008.3$ Hz will assist in keeping the voltages close to the reference. It can also be observed that the capacitor voltages are still slowly diverging when using $f_{\text{cr}} = 1025$ Hz, due to the non-optimal selection of this ratio. Similar results can be obtained when using low switching frequency for the converter cells, as shown in Fig. 4.13, where $f_{\text{cr}} = 250$ Hz is used for the integer case and around it for the non-integer cases. Again, a

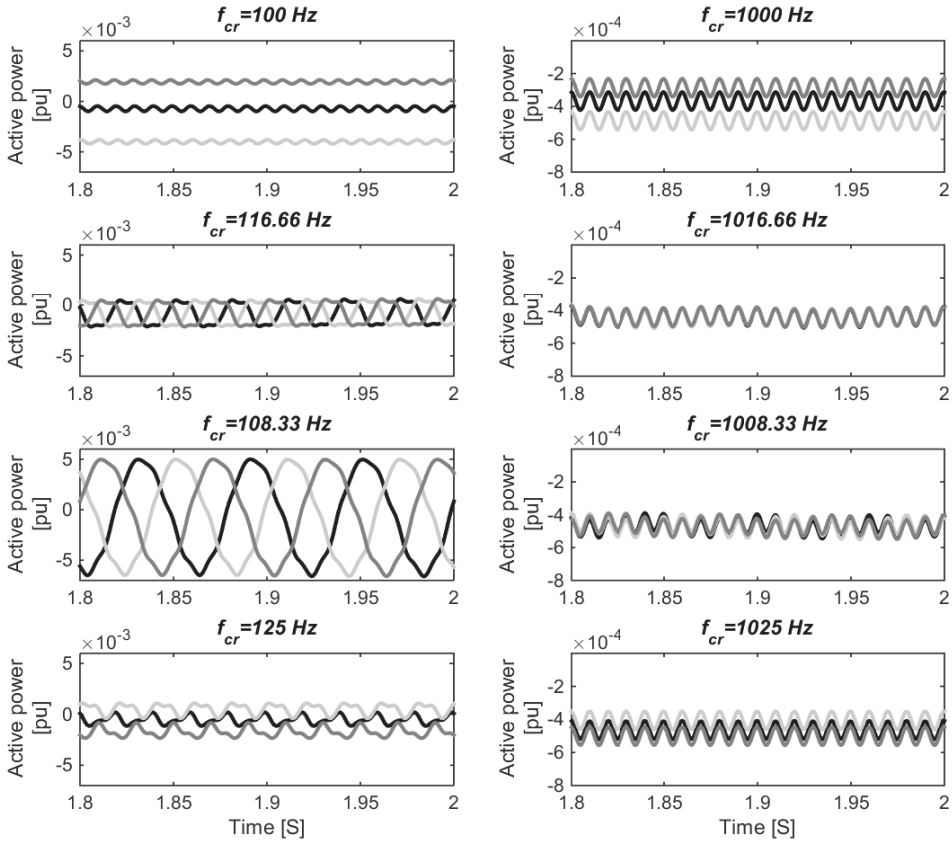


Fig. 4.11 Active power of each cell in phase *a* after low pass filtering for different carrier frequencies.

more uniform distribution of the active power in the different cells is obtained when selecting the carrier frequency according with (4.16) or (4.17).

The analysis carried out until now only focuses on the error in the phase shift between the different carriers and the presented results consider only this as a deviation from the ideal conditions. However, as mentioned earlier, in practical applications any kind of mismatch between ideal and actual conditions will have an impact on the distribution of the active power between the converter cells. As an example, Fig. 4.14 shows the capacitor voltages in phase *a* with $f_{\mathrm{cr}} = 1000$ Hz, 1008.3 Hz, 1016.6 Hz and 1025 Hz when a tolerance of 10% is considered for the DC-capacitor sizes in the simulation model. It can be observed that although non-integer M_f helps in keeping the voltages close to the reference, still for the simulated case it is not possible to provide a perfectly even active power distribution among the cells. As it can be understood from the analysis carried out in the previous sections, the impact of this kind of deviations will be more significant when lowering the switching frequency. Therefore, it is of importance to stress that an individual balancing controller must be implemented in actual installations, regardless the selection of M_{f}. Individual balancing control can be implemented by either a closed loop controller or by the sorting algorithm. Both of these methods and their implementation are provided in the next chapters.

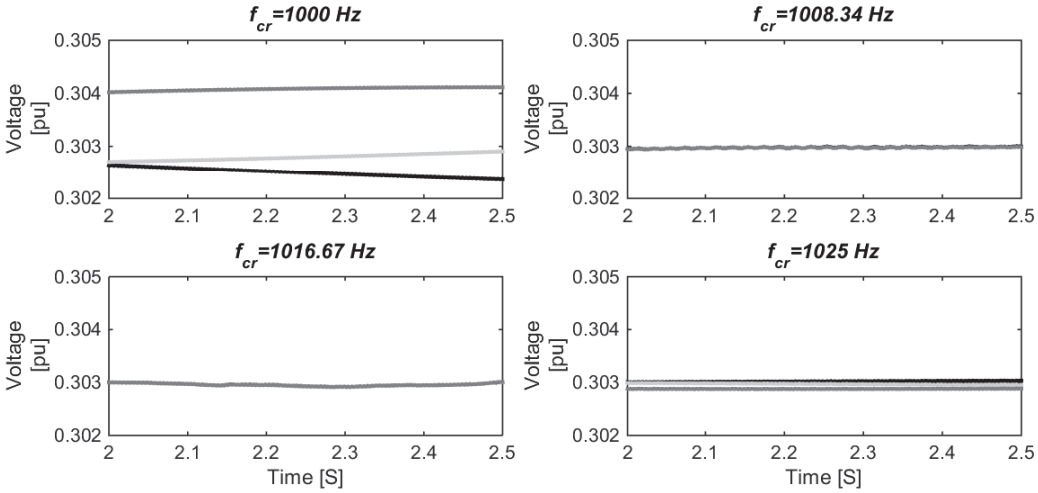


Fig. 4.12 Capacitors voltages in phase *a* with $f_{\mathrm{cr}} = 1000$ Hz, 1008.3 Hz, 1016.6 Hz and 1025 Hz.

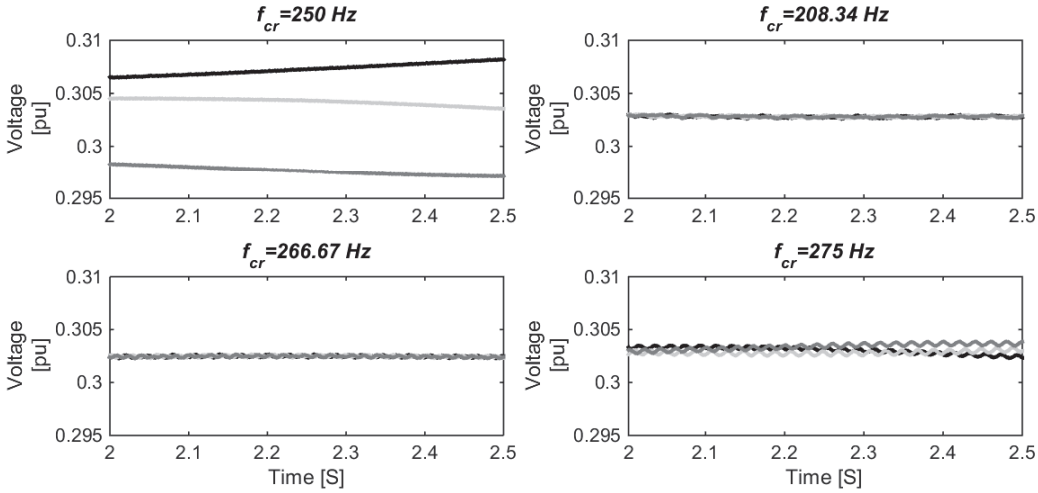


Fig. 4.13 Capacitors voltages in phase *a* with $f_{\mathrm{cr}} = 250$ Hz, 258.3 Hz, 266.6 Hz and 275 Hz.

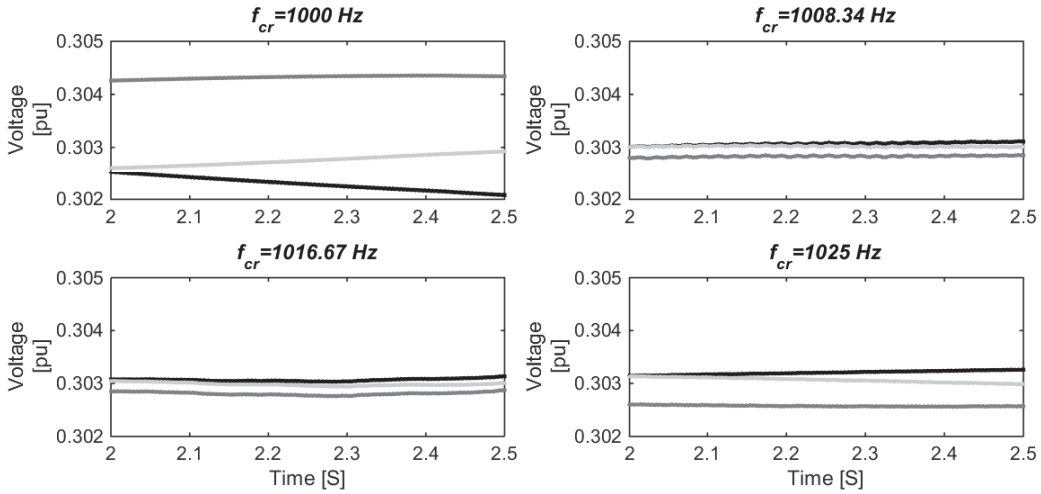


Fig. 4.14 Capacitors voltages in phase a with $f_{\mathrm{cr}} = 1000$ Hz, 1008.3 Hz, 1016.6 Hz and 1025 Hz and with tolerance of $\pm 10\%$ in DC capacitor sizes.

4.3 Individual DC-link voltage controller

The control system described in Chapter 3 provides identical modulation index for each cell. The basic idea of the individual DC-link voltage controller is to include an extra control loop in order to modify the modulation index for each cell and thus provide the required active power for individual DC-link voltage balancing.

Each modulation index is characterized by an amplitude and a phase angle. The method proposed in [64–66] modifies the amplitude and phase angle of each modulation index individually to provide the required active power for each cell. Modifying the modulation index by voltage vector superposition method is proposed in [8, 67–69].

Among the proposed methods, active voltage vector superposition method is more robust [69]. Therefore, the method used in [8] is used here for the individual DC-link voltage controller.

For STATCOM applications, the reactive component of the current is typically much larger than the active component ($i_{\mathrm{q}} >> i_{\mathrm{d}}$). Due to this fact and also considering to have a fast and precise current controller ($i_{\mathrm{qref}} \approx i_{\mathrm{q}}$) it is possible to estimate the current in each phase of the star as

$$\begin{aligned} \hat{i}_{\mathrm{aY}} &= \tfrac{\sqrt{2}}{\sqrt{3}} i_{\mathrm{qref}} \sin(\theta) \\ \hat{i}_{\mathrm{bY}} &= \tfrac{\sqrt{2}}{\sqrt{3}} i_{\mathrm{qref}} \sin(\theta - \tfrac{2\pi}{3}) \\ \hat{i}_{\mathrm{cY}} &= \tfrac{\sqrt{2}}{\sqrt{3}} i_{\mathrm{qref}} \sin(\theta + \tfrac{2\pi}{3}) \end{aligned} \tag{4.18}$$

where $\frac{\sqrt{2}}{\sqrt{3}}$ is the coefficient used for power invariant transformation from dq-reference frame to three-phase system and " $\hat{}$ " is to indicate the estimated quantities. Since the current is

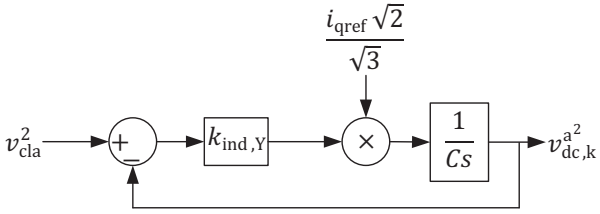


Fig. 4.15 Closed loop block diagram of the individual DC-link voltage controller.

leading/lagging by 90^0 with voltage, the current amplitudes are multiplied by $\sin(\theta)$.

The voltage components that are superposed to the reference voltage of each cell at each phase are

$$\begin{aligned} v_{\text{i,Y}}^{\text{a,k}} &= k_{\text{ind,Y}}(v_{\text{dc,k}}^{\text{a}^2} - v_{\text{cla}}^2)\sin(\theta) \\ v_{\text{i,Y}}^{\text{b,k}} &= k_{\text{ind,Y}}(v_{\text{dc,k}}^{\text{b}^2} - v_{\text{clb}}^2)\sin(\theta - \tfrac{2\pi}{3}) \\ v_{\text{i,Y}}^{\text{c,k}} &= k_{\text{ind,Y}}(v_{\text{dc,k}}^{\text{c}^2} - v_{\text{clc}}^2)\sin(\theta + \tfrac{2\pi}{3}) \end{aligned} \tag{4.19}$$

where $k_{\text{ind,Y}}$ is a proportional gain, $v_{\text{cla}}, v_{\text{clb}}, v_{\text{clc}}$ are the cluster voltages (average of DC-link voltage in each phase) in phase a, b, c and $v_{\text{dc,k}}^{\text{a}}, v_{\text{dc,k}}^{\text{b}}, v_{\text{dc,k}}^{\text{c}}$ are the DC-link voltage of k_{th} cell in phase a, b, c. The voltage components that are superposed to the reference voltage of each cell are AC signals in phase with the currents, which thus form an active power component to balance the DC-link voltages.

It should be mentioned that the difference between the cluster control loop explained in Chapter 3 and the individual DC-link voltage controller is that the cluster control loop takes care of the cluster voltage and controls it to the reference voltage while the individual DC-link voltage controller takes care of the DC-link voltage in each cell. The purpose of the individual DC-link voltage controller is to not allow the DC-link voltage to diverge from the cluster voltage.

The active power for the DC-link voltage balancing of the k_{th} cell in phase a can be written as

$$\frac{1}{2}Cs(v_{\text{dc,k}}^{\text{a}^2}) = \frac{\left|v_{\text{i,Y}}^{\text{a,k}}\right|\left|\hat{\text{i}}_{\text{aY}}\right|}{2} \tag{4.20}$$

Replacing the variable $\left|v_{\text{i,Y}}^{\text{a,k}}\right|$ and $\left|\hat{\text{i}}_{\text{aY}}\right|$ from (4.18) and (4.19) into (4.20), the closed loop block diagram of the individual DC-link voltage controller can be shown as Fig. 4.15. The closed-loop transfer function from v_{cla}^2 to $v_{\text{dc,k}}^{\text{a}^2}$ is given by

$$G_{\text{ind,Y}} = \frac{v_{\text{dc,k}}^{\text{a}^2}}{v_{\text{cla}}^2} = \frac{\frac{k_{\text{ind,Y}} i_{\text{qref}}\sqrt{2}}{C\sqrt{3}}}{s + \frac{k_{\text{ind,Y}} i_{\text{qref}}\sqrt{2}}{C\sqrt{3}}} = \frac{\alpha_{\text{ind}}}{\text{s}+\alpha_{\text{ind}}} \tag{4.21}$$

where α_{ind} is the closed-loop bandwidth of the individual DC-link voltage controller. From (4.21), the proportional gain of the individual DC-link voltage controller is given by

$$k_{\text{ind,Y}} = \frac{\sqrt{3}C\alpha_{\text{ind}}}{\sqrt{2}i_{\text{qref}}} \tag{4.22}$$

It can be observed from (4.22) that the individual balancing control does not work when i_{qref} is zero. Therefore this method is unable to provide the individual DC-link voltage control at zero-current mode. This problem and its solutions will be discussed in the next part of this chapter.

Following the same design process for the delta configuration, three phase estimated branch currents of the delta are

$$\begin{aligned}
\hat{i}_{\text{a}\Delta} &= \tfrac{\sqrt{2}}{3} i_{\text{qref}} \sin(\theta + \tfrac{\pi}{6}) \\
\hat{i}_{\text{b}\Delta} &= \tfrac{\sqrt{2}}{3} i_{\text{qref}} \sin(\theta + \tfrac{\pi}{6} - \tfrac{2\pi}{3}) \\
\hat{i}_{\text{c}\Delta} &= \tfrac{\sqrt{2}}{3} i_{\text{qref}} \sin(\theta + \tfrac{\pi}{6} + \tfrac{2\pi}{3})
\end{aligned} \tag{4.23}$$

where $\frac{\pi}{6}$ is the phase shift between the line and the branch currents. The voltage components which are superposed to the reference voltage of each cell at each phase are

$$\begin{aligned}
v_{\text{i},\Delta}^{\text{a,k}} &= k_{\text{ind},\Delta}(v_{\text{dc,k}}^{\text{a}^2} - v_{\text{cla}}^2) \sin(\theta + \tfrac{\pi}{6}) \\
v_{\text{i},\Delta}^{\text{b,k}} &= k_{\text{ind},\Delta}(v_{\text{dc,k}}^{\text{b}^2} - v_{\text{clb}}^2) \sin(\theta + \tfrac{\pi}{6} - \tfrac{2\pi}{3}) \\
v_{\text{i},\Delta}^{\text{c,k}} &= k_{\text{ind},\Delta}(v_{\text{dc,k}}^{\text{c}^2} - v_{\text{clc}}^2) \sin(\theta + \tfrac{\pi}{6} + \tfrac{2\pi}{3})
\end{aligned} \tag{4.24}$$

The proportional gain is then given by

$$k_{\text{ind},\Delta} = \frac{3C\alpha_{\text{ind}}}{\sqrt{2}i_{\text{qref}}} \tag{4.25}$$

Figure. 4.16 shows the overall control block diagram of CHB-STATCOMs including individual DC-link voltage controller.

4.3.1 Simulation results

The CHB-STATCOMs with system parameters of Table 3.1 are simulated in PSCAD including the individual DC-link voltage controller. In order to avoid the interaction between the cluster and individual DC-link voltage controller, the individual controller is intentionally designed to be slower than the cluster control loop. The closed loop bandwidth of the individual DC-link

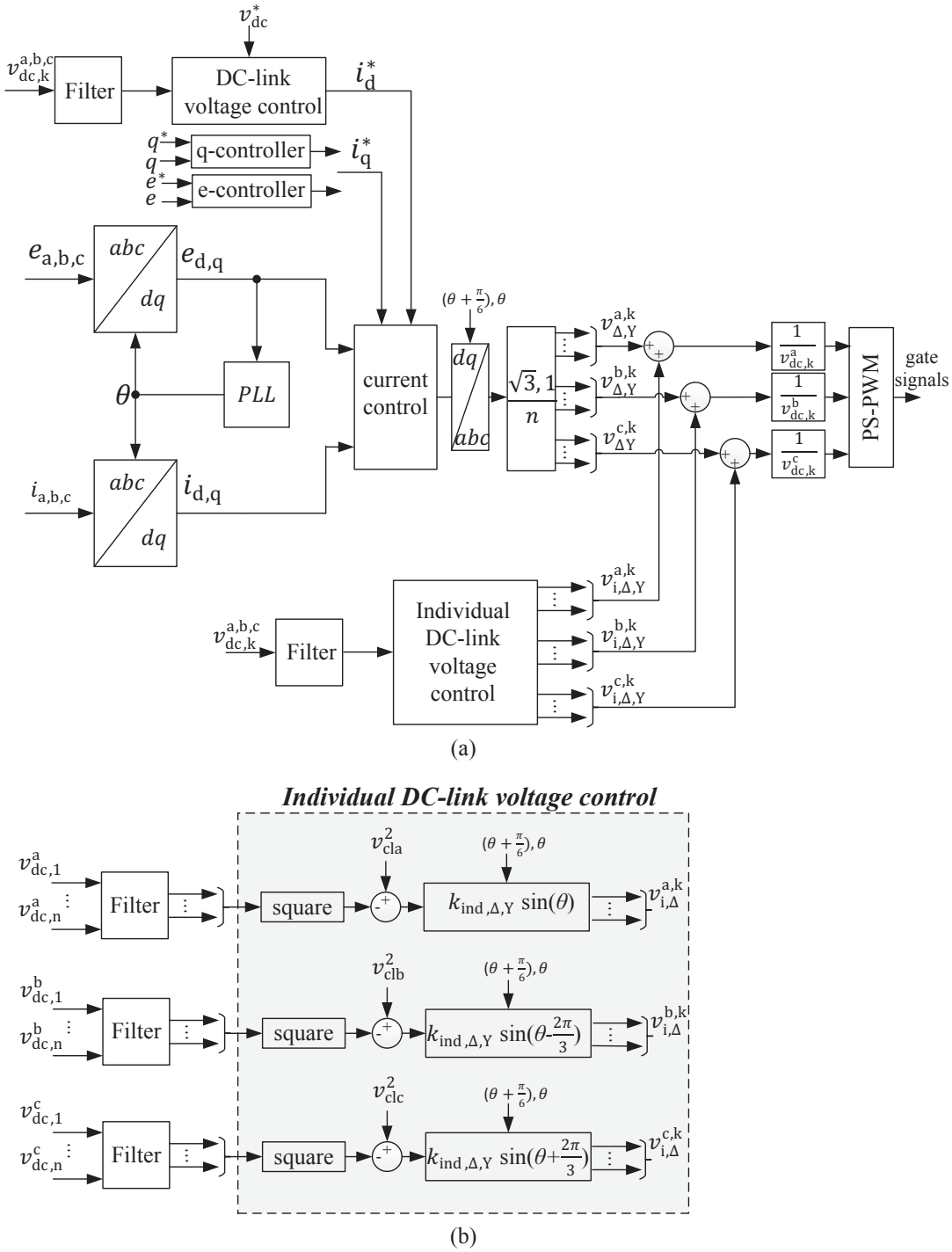


Fig. 4.16 Overall control block diagram CHB-STATCOMs with individual DC-link voltage controller; (a): Overall control; (b): individual DC-link voltage controller.

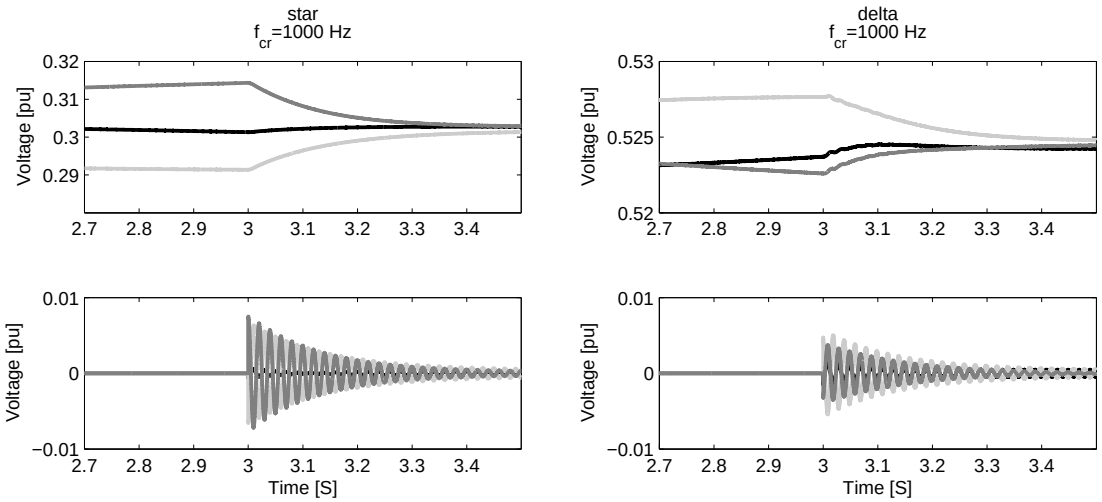


Fig. 4.17 DC-link voltage results of CHB-STATCOMs; top: filtered DC-link voltages; bottom: outputs of the individual DC-link voltage controller. (with carrier frequency of 1 kHz)

voltage controller is set to 1 Hz, i.e. 5 time below the bandwidth of the cluster control loop bandwidth.

Figure 4.17 shows the filtered DC-link voltages and the output of the individual DC-link voltage controller of each cell in phase *a* for both star and delta when integer carrier frequency of 1 kHz is used. The reference reactive current is set to 0.3 pu. The individual DC-link voltage controller is not activated in the beginning of the simulation and activated at $t = 3$ S. Figure 4.17 (top) shows the ability of the individual DC-link voltage controller to control the DC-link voltages.

Figure 4.18 shows the obtained simulation results when non-integer carrier frequency of 1016.67 Hz is used instead. It can be observed from Fig. 4.18 that by using non-integer frequency modulation ratio, the individual DC-link voltage controller puts much less effort in controlling the DC-link voltages. This shows the advantage of using non-integer frequency modulation ratio instead of the integer one.

4.4 Individual DC-link voltage control using sorting algorithm

Individual DC-link voltage control presented in the previous section is based on the superposition of a voltage component to the reference voltage. This modification of the reference voltage for each cell can degrade the harmonic performance of the PS-PWM [60]. This is due to the fact that the perfect harmonic cancellation will be achieved when all the modulation indexes are identical. Another problem caused by the individual DC-link voltage control using the control loop method is the interaction between the individual DC-link voltage controller and the cluster control loop. Due to these problems, another technique for controlling the DC-link voltages has been introduced, based on the sorting algorithm. The sorting algorithm allows the modulation scheme to inherently balance the DC-link voltages, thus removing the need for any control loop.

In sorting algorithm when the converter absorbs active power (charging mode) the cells with the

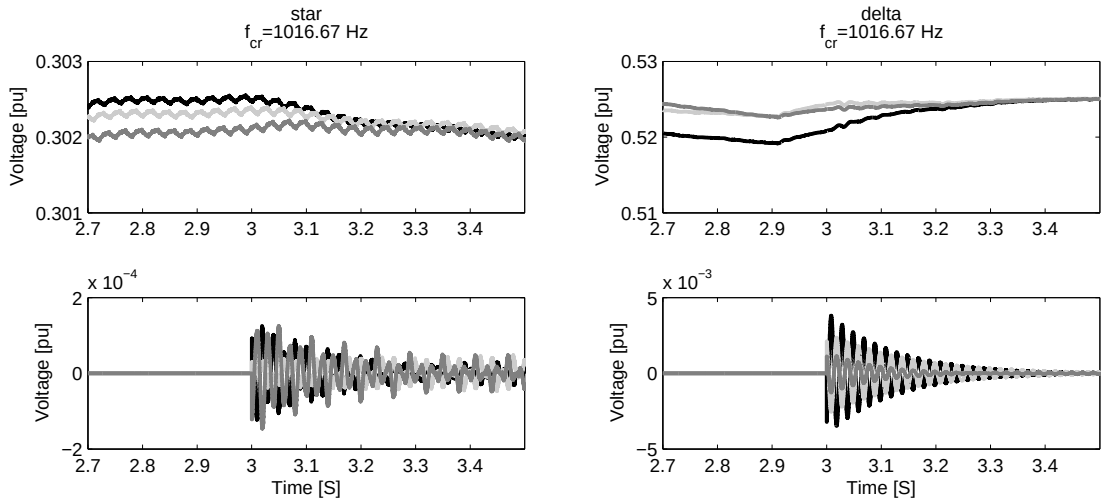


Fig. 4.18 DC-link voltage results of CHB-STATCOMs; top: filtered DC-link voltages; bottom: outputs of the individual DC-link voltage controller. (with carrier frequency of 1016.67 kHz)

lowest DC-link voltage are directly inserted to synthesize the reference voltage, while when the converter inject active power (discharging mode) it is vice verse and the cells with highest DC-link voltage will be used instead. This method gradually charges and discharges the capacitors with lower and higher voltage value without the need for an extra outer control loop [9, 10].

The main problem associated with the aforementioned sorting algorithm is the resulting high switching frequency as the balancing algorithm switches the cells according to their DC-link voltage at every control period. Another drawback of this technique is the required processing time for sorting the DC-link voltages. Many papers propose different methods to decrease the needed processing time for sorting the DC-link voltages [70–73] and the switching frequency [74–77]. References [78, 78] proposes a modified LS-PWM to evenly distribute the switching pulses among the cells using the sorting technique. References [79–81] proposes a modified PS-PWM using the sorting technique to improve the harmonic performances. Sorting algorithm for configuration with high number of cells per phase leg is proposed in [82] by using NLM. Sorting algorithm using predictive control is proposed in [83, 84] in order to reduce the switching frequency as well as ripples of the capacitor voltages.

4.4.1 Sorting algorithm and modulation technique

The current controller calculates the three-phase voltage references to be sent to the modulator. At the beginning of each control cycle, the minimum number of cells to be inserted (direct or reverse), and the fractional part of the voltage references are determined. The fractional part is then properly scaled and compared with a carrier.

If the state of the phase leg is in charging mode (considering the direction of the current to be toward the converter, charging mode is when reference voltage and current have the same sign), then the cells are sorted in ascending order. The required numbers of cells that are supposed to be inserted are chosen from the capacitors with the lowest voltage. For the remaining capacitors,

the one with the lowest voltage is chosen to be modulated by the fractional part of the voltage reference. The rest of the cells are fully bypassed.

The same process can be used for discharging mode (voltage and current at each phase are in opposite sign), where the cells are sorted in descending order.

For practical implementation, $floor$ and *rem* commands can be used for the sorting PWM. $floor(x)$ returns the nearest positive integer lower or equal to *x*. $rem(a/b)$ returns the fractional part of *a* divided *b*. For example, if the reference voltage in one phase is -19 *kV* and each cell voltage is $V_{dc} = 3.33$ *kV*, then $floor(-19/3.33)$=5 and $rem(-19/3.33)$=-2.35. The fractional part of the reference voltage is normalized with the cell voltage and will be used to modulate a cell. In this example eventually 5 cells must be reversed inserted and one cell must be modulated with the fractional part.

4.4.2 Zero-current operating mode

Although sorting algorithm is an effective solution for voltage balancing when the converter is exchanging current with the grid, less attention has been paid for zero-current operating mode (STATCOM in standby mode) in the literature. Sorting algorithm needs current sign information to provide a correct sorting pattern. As a consequence, when the exchanging current that flows in the cells is zero, the sorting algorithm is unable to take the correct insertion decision for proper balancing of the DC-link voltages. In practical applications, this is even more problematic when noise is also added in the measured current signal. The problem of system operation at zero-current mode also exists when using individual DC-link voltage control loop, as described in Section 4.3.

Here, two methods for capacitor voltage balancing at zero-current mode are proposed. The first method is based on a modified sorting algorithm, while the second method is based on DC-link voltage modulation. It is of importance to stress that the investigated methods are for zero-current mode only, since when a current circulates in the phase leg the classical or advanced sorting techniques can be adopted.

The proposed methods are meant for the star configuration. Although the same methods can be used for the delta configuration, it is of importance to consider that in this case, it is possible to force a current that circulates inside the delta and thereby allow a uniform distribution of the active power among the different cells. This solution cannot be implemented in practice in the star case. For this reason, capacitor cells balancing is more challenging in star configuration, especially in case of zero (or more in general, very small) current exchange between the compensator and the grid.

Figure 4.19 shows the principle of operation of unipolar PWM when the reference voltage is positive. The reference value in Fig. 4.19 is the fractional part of the reference voltage.

As shown in the right figure, if the RMS value of the current becomes zero, the sign of the instantaneous current will change in the middle of two sampling points. This implies a discharging following by a charging state during one control cycle. The same sign change is observable when reference voltage is negative: in this case, the instantaneous current is positive in the first

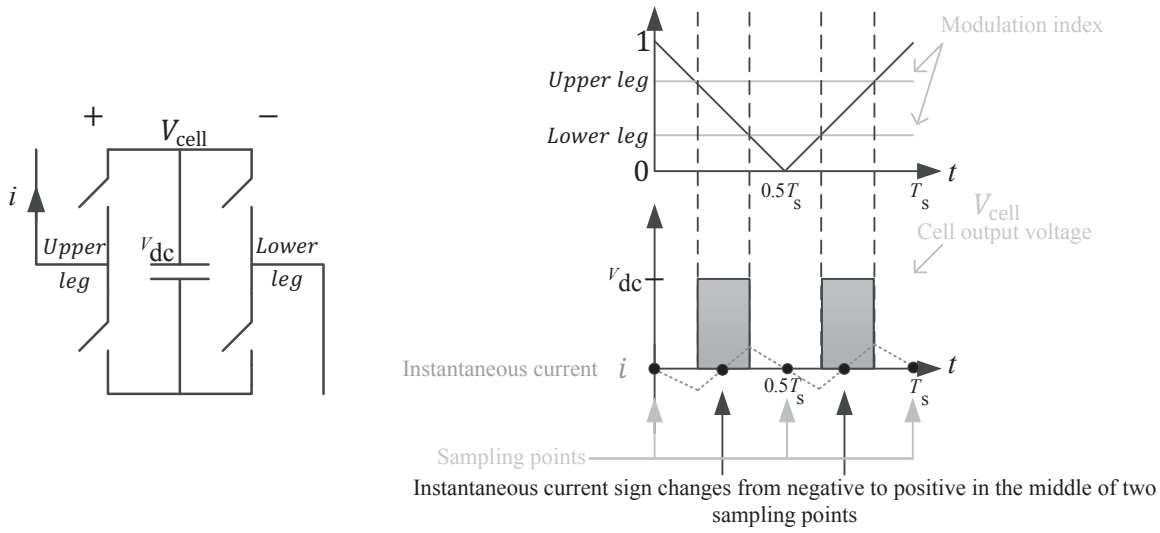


Fig. 4.19 Zero-current mode operation in unipolar PWM and positive reference voltage; left: H-bridge converter; right: unipolar PWM principle.

half cycle and is negative in the second half. This implies again a discharging followed by a charging state during one control cycle.

The sorting algorithm determines the switching pattern during one control cycle based on the charging or discharging mode; however the sign of the instantaneous current at zero-current mode shows that a single detection in the beginning of each control cycle is not sufficient to determine the sorting pattern. Therefore, the detection of charging or discharging, and consequently the sorting pattern, must be updated in the middle of two sampling points.

The conventional sorting algorithm is applied to a 19-level star configuration in PSCAD. Table 4.1 shows the system parameters selected for the simulation study.

TABLE 4.1. SYSTEM AND CONTROL PARAMETERS

Parameters	values
Rated power S_b	120 MVA , 1 pu
Nominal line to line rms voltage V_b	33 kV , 1 pu
Filter inductance L_f	4.33 mH , 0.15 pu
Filter resistor R_f	0.136 Ω , 0.015 pu
Capacitors C	4 mF , 0.088 pu
DC-link voltage of each cell V_{dc}	3.33 kV , 0.1 pu
Number of cells per phase N	9
Carrier frequency for PWM f_{cr}	500 Hz
Grid frequency f_o	50 Hz
Current control closed loop band width α_i	$2\pi \times 100$ rad/sec
Cluster control closed loop band width α_{cl}	$2\pi \times 5$ rad/sec

In order to provide a more realistic model, the capacitors in each cell are paralleled with a resistor. This resistor is to model the internal losses in the cell and is chosen to be different from

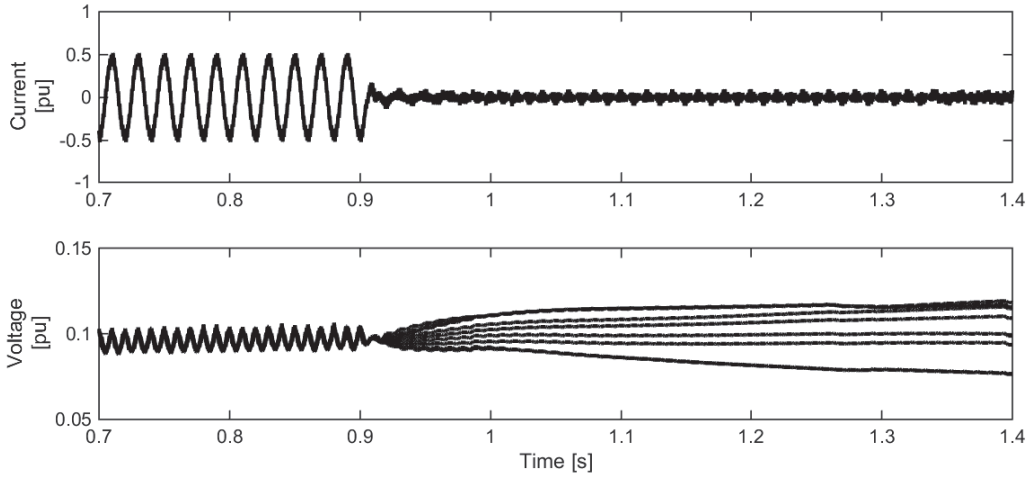


Fig. 4.20 DC-link voltages and line current in phase *a* without the proposed methods; top: line current; bottom: capacitor voltages.

cell to cell. In addition to the resistors, a ±20% tolerance band is chosen for the capacitors sizes (3.2 to 4.8 mF). Note that the deviation here considered is large in order to stress the system and accelerate the voltage deviation.

Figure 4.20 shows the simulation results when using the conventional sorting algorithm. Top plot shows the line current in phase *a* while the lower figure shows the DC-link voltages in phase *a*. Similar behavior can be observed for the other phases. All figures are showing the measured quantities in pu. At t=0.9 s, the reactive current is changed from 0.35 pu to zero. Figure. 4.20 shows that conventional sorting algorithm is not able to provide proper individual cell balancing at zero-current mode.

Figure 4.21 shows a detail of a cell output voltage, line current between two sampling points together with the interrupt signal. It can be observed from this figure that the sign of the current is negative in the first half of the control period and changes to positive after almost half of the period, as anticipated earlier in this section. Theoretically, at zero-current operating mode, the current sign changes exactly in the middle of the control period. This provides equal positive and negative areas, leading to equal charging and discharging. Consequently, the DC-link voltage should remain constant. However in practical applications this symmetry will not be achieved, leading to slightly more charging or discharging area (as in this specific example). Therefore the DC-link voltages will not remain constant and diverge from their reference values.

4.4.3 Modified sorting algorithm

The first proposed method takes advantage of the knowledge of the sign of the current ripple as zero-current mode. In STATCOM applications even if the reactive current is zero, there is always a small active current flowing in order to keep the charge of all capacitors and compensate for the losses. In this case the RMS value of the current is not zero. This is beneficial for the sorting since a small flowing current with small ripple amplitudes can be used for the cells

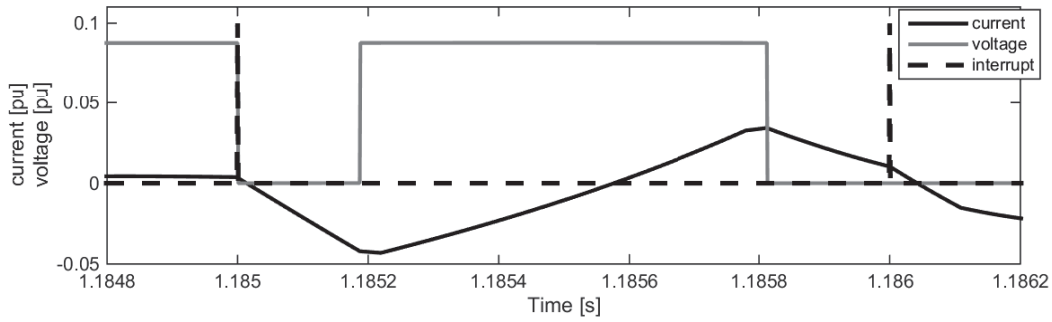


Fig. 4.21 Cell output voltage and line current together with main interrupts.

sorting. However, measurement noise can affect the detection of charging or discharging mode. The noise amplitudes can become bigger than the actual current.

In this section a solution is proposed, which is independent from the current measurements. The proposed method assumes that the ripple current is bigger than the RMS value when the exchanging current is small and therefore the actual current can be approximated with its ripple only.

As explained in the previous section, at zero-current mode the control cycles always start in a discharging mode and in the middle of the control cycle it should change to charging mode. Therefore, current and voltage measurements are not needed anymore to detect the charging or discharging modes. In the proposed method, two sets of interrupts are used. The main interrupt is synchronized with the top and bottom of the main carrier; this interrupt is used for sampling of the measured quantities. The second interrupt, located between the two sampling points is introduced in order to indicate the point where the discharging mode should change to charging mode. Whenever this interrupt is enabled, the sorting algorithm must change the sorting pattern according to the new mode. It is of importance to stress that the modified sorting algorithm proposed here should be used for zero-current mode only. The threshold for the activation of the proposed controller is here set to 0.03 pu current.

The flowchart of the proposed algorithm is shown in Fig. 4.22. In the beginning of each main interrupt, first the reference voltage is determined. Then, the number of cells that must be inserted (direct or reverse) and fractional part of the reference voltage are determined. Whenever the RMS value of the current is below the predefined threshold (0.03 pu in this case), the proposed method is activated. According to the sign of the current ripple discussed in the previous section, every control cycle starts with the discharging mode regardless of the polarity of the voltage. Thus, the first sorting pattern is determined based on the discharging mode. After this step, the controller waits to receive the second interrupt. From the middle of the control cycle to the end, the phase leg is in the charging mode and the sorting pattern is determined accordingly. Finally, the controller waits for the main interrupt to continue the same process.

It is worth mentioning that charging and discharging pattern explained here (discharging first charging second) is based on the assumption that there is no delay in the digital controller. Considering for example the one-sample delay in the digital controller, the charging and discharging pattern must be reversed (charging first discharging second). The reason is that due to

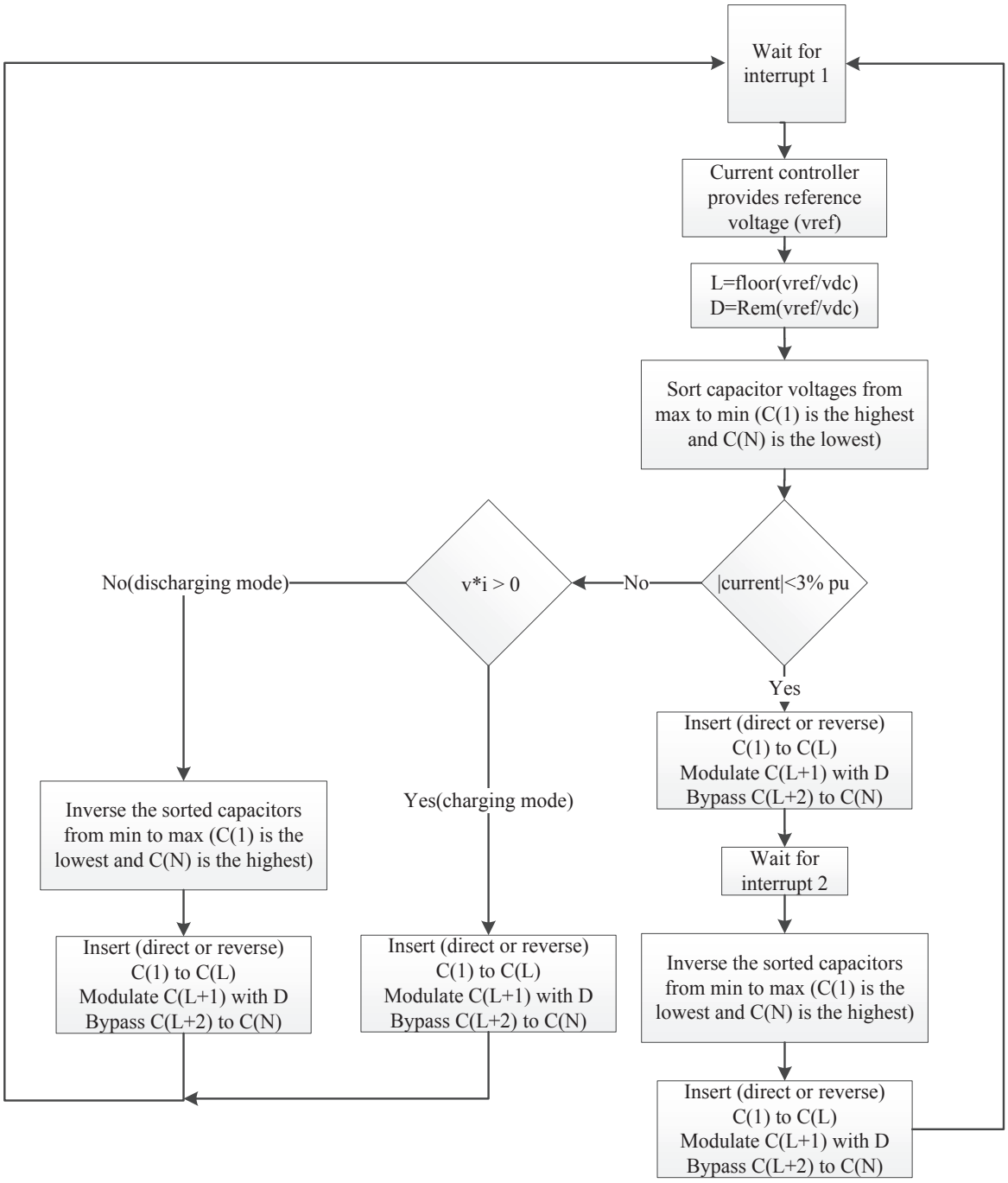


Fig. 4.22 flowchart of the proposed controller.

the one-sample delay, in each interrupt the controller decides about the next control period.

Since the modified sorting algorithm relies on the current ripple, the operating range of this method is limited by current ripple amplitude. The proposed method is valid as long as the RMS value of the current is less than the current ripple amplitude and must be avoided beyond this region. In order to provide wider control region at zero-current modes, an alternative method called DC-link voltage modulation is here proposed in the following section.

4.4.4 DC-link voltage modulation

The basic idea behind the DC-link voltage modulation method is to vary the amplitude of the current at zero-current mode by exchanging a small amount of active current with the grid.

Active current exchange can be achieved by allowing the capacitor voltages to increase and decrease gently around the desired reference value. A low-amplitude/low-frequency sinusoidal component can be added to the reference DC voltage once the converter operates at zero-current mode, thus forcing a small current exchange between the converter and the grid.

The amplitude of the sinusoidal component should not increase the DC-link voltage beyond the safety margin of the converter. According to (4.6) and considering only the fundamental component, the converter maximum and minimum voltages are calculated as

$$V_{\mathrm{aY}} = E_{\mathrm{a}} \pm ZI_{\mathrm{aY,rated}} \tag{4.26}$$

where $I_{\mathrm{aY,rated}}$ is the rated current of the converter. According to (4.26) the DC-link voltage band for each cell of the star configuration with N number of cells per phase leg is located between a minimum and maximum value as

$$V_{\mathrm{dc}} = \frac{E_{\mathrm{a}} \pm ZI_{\mathrm{aY,rated}}}{N} \tag{4.27}$$

The DC-link voltage reference can then be written as

$$v^*_{\mathrm{dc}} = \begin{cases} v^*_{\mathrm{dc,0}} + v\cos(2\pi f_{\mathrm{d}} t) & i^*_{\mathrm{q}} = 0 \\ v^*_{\mathrm{dc,n}} & i^*_{\mathrm{q}} \neq 0 \end{cases} \tag{4.28}$$

where $v\cos(2\pi f_{\mathrm{d}} t)$ is the sinusoidal component with amplitude of v and frequency of f_{d}; the zero-current mode is activated when $i^*_{\mathrm{q}} = 0$. The required DC-link voltage at zero-current mode is equal to the middle of the DC-link voltage band calculated in (4.27). Therefore, $v^*_{\mathrm{dc,0}}$ and v in (4.28) should be selected so that the DC-link voltage oscillates between the maximum and the middle of the DC-link voltage band. The voltage $v^*_{\mathrm{dc,n}}$ in (4.28) can be either designed to the maximum DC-link voltage level or it can be programmed to vary according to (4.27) [8].

The resulting current must be low in order to avoid to impact the grid voltage. However, the noise and ripple can affect the proper sorting algorithm. Therefore an estimate of the line current should be used instead of the measured signal. Since the reactive current is very small ($i_{\mathrm{d}} >> i_{\mathrm{q}}$)

and assuming a fast and precise current controller ($i_{\mathrm{d}}^{*} \approx i_{\mathrm{d}}$), it is possible to estimate the current in each phase of the star as

$$\begin{aligned} \hat{i}_{\mathrm{aY}} &= \tfrac{\sqrt{2}}{\sqrt{3}} i_{\mathrm{d}}^{*} \cos(\theta) \\ \hat{i}_{\mathrm{bY}} &= \tfrac{\sqrt{2}}{\sqrt{3}} i_{\mathrm{d}}^{*} \cos(\theta - \tfrac{2\pi}{3}) \\ \hat{i}_{\mathrm{cY}} &= \tfrac{\sqrt{2}}{\sqrt{3}} i_{\mathrm{d}}^{*} \cos(\theta + \tfrac{2\pi}{3}) \end{aligned} \tag{4.29}$$

where $\frac{\sqrt{2}}{\sqrt{3}}$ is the coefficient used for power invariant transformation from dq-reference frame to three-phase system and $\cos(\theta)$ is to make the current in phase with the grid (since the current is mainly active current). Note that i_{d}^{*} is determined by the cluster control loop described in Section 3.2.3. The current information required for the sorting algorithm can then be written as

$$i = \begin{cases} \text{estimated current from } (4.29) & i_{\mathrm{q}}^{*} = 0 \\ \text{measured current} & i_{\mathrm{q}}^{*} \neq 0 \end{cases} \tag{4.30}$$

According to (4.30), once the converter starts to operate under zero-current mode, the estimated currents of (4.29) instead are used in the sorting algorithm. For any other operating mode, the measured currents are used. It is of importance to stress that the estimated currents are only used in the sorting algorithm under zero-current mode. The current control will still use the measured currents in the feedback loop.

4.4.5 Simulation results

In this section, simulation results for the two proposed methods for DC-link voltage balancing under zero-current mode will be presented.

Modified sorting algorithm

The proposed modified sorting algorithm method is applied to the same simulation case study presented in the previous section (see Figure 4.20). Figure 4.23 shows the simulation results when using the proposed method. Top plot shows the three-phase line currents and bottom plot shows the capacitor voltages in phase *a*,*b* and *c*. At t=0.9 s, the reactive current is changed from 0.35 pu to zero. Figure 4.23 shows that the proposed algorithm is able to provide proper individual cell balancing at zero-current mode.

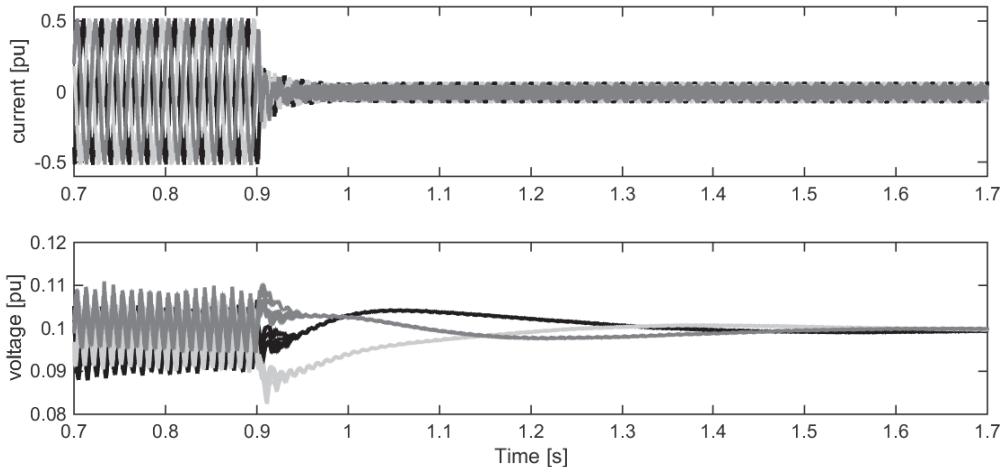


Fig. 4.23 Capacitor voltages and line current by using the proposed method; top: Three-phase line currents; bottom: all capacitor voltages in each phase.

Figure 4.24 shows a zoom view of the output voltage of two cells belonging to the same phase leg, the line current between two sampling points together with main and secondary interrupts. This figure shows that unlike the conventional sorting algorithm (Fig. 4.21), the output voltage is not generated by only one cell. According with the proposed method, the pulse is first generated by a cell that is chosen based on discharging mode and after half a period (at the secondary interrupt) the pulse is completed by a cell chosen based on the charging mode.

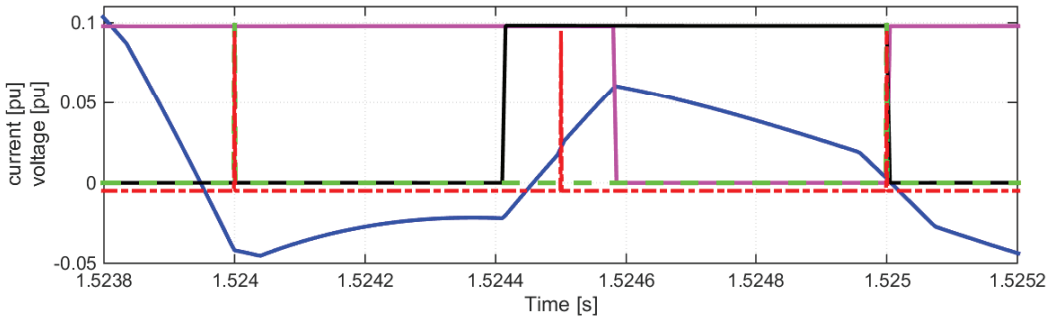


Fig. 4.24 Two cells output voltages and line current together with the main and secondary interrupts.

Figure 4.25 shows the simulated line current and DC-link voltages when the reference current varies from 0.03 pu inductive to 0.03 pu capacitive. From $t = 0.7$ s to $t = 0.8$ s, the reactive power is set to zero, from $t = 0.8$ s to $t = 1$ s to 0.03 pu inductive and from $t = 1$ s to $t = 1.2$ s to 0.03 pu capacitive. The current ripple amplitude from Fig. 4.20 (top) is 0.07 pu (i.e., above the threshold level). Again, as it is shown in Fig. 4.25 (bottom), the proposed method is able to provide proper individual cell balancing.

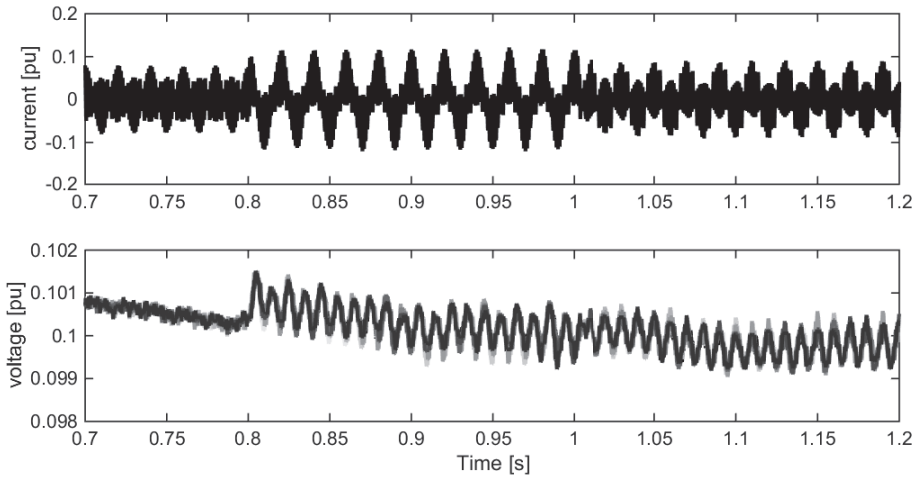


Fig. 4.25 DC-link voltages (top) and line current (bottom) with the proposed method in the current range of -0.03 pu to +0.03 pu.

To evaluate the robustness of the proposed method, a 0.05 pu white noise is added to the current and voltage measurements. Furthermore, a one-sample delay is considered in the controller. In order to provide a more realistic model, deadtime of 5 μs for the switches and 2 V forward voltage drop over the valves are considered. The amount of noise, deadtime and capacitor size variations chosen here are exaggerated quantities in order to verify the robustness of the proposed method under extreme cases.

Figure. 4.26 shows the obtained simulation results. Top plot shows the reactive component of the current and its reference. The reference reactive current is set to -1 pu in the beginning and changes to zero and 1 pu at $t = 0.5$ s and $t = 1.5$ s respectively. Bottom plot shows the successful operation of the controller in balancing the DC-link voltages.

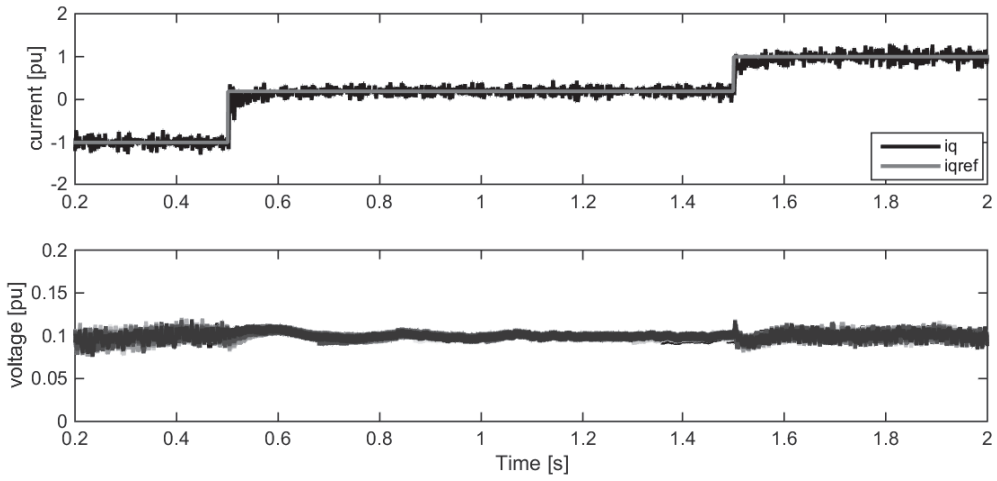


Fig. 4.26 Simulation results by considering noise, delay, deadtime and valves voltage drop; top: Reactive component of current and its reference; bottom: DC-link voltages in phase *a*.

Finally in order to evaluate the proposed method in presence of grid voltage harmonics, a 5th

harmonic of 0.016 pu amplitude and a 7th harmonic of 0.011 pu amplitude are added to the grid voltage. Figure 4.27 shows that also under this condition the proposed algorithm allows to keep the capacitor voltage balanced.

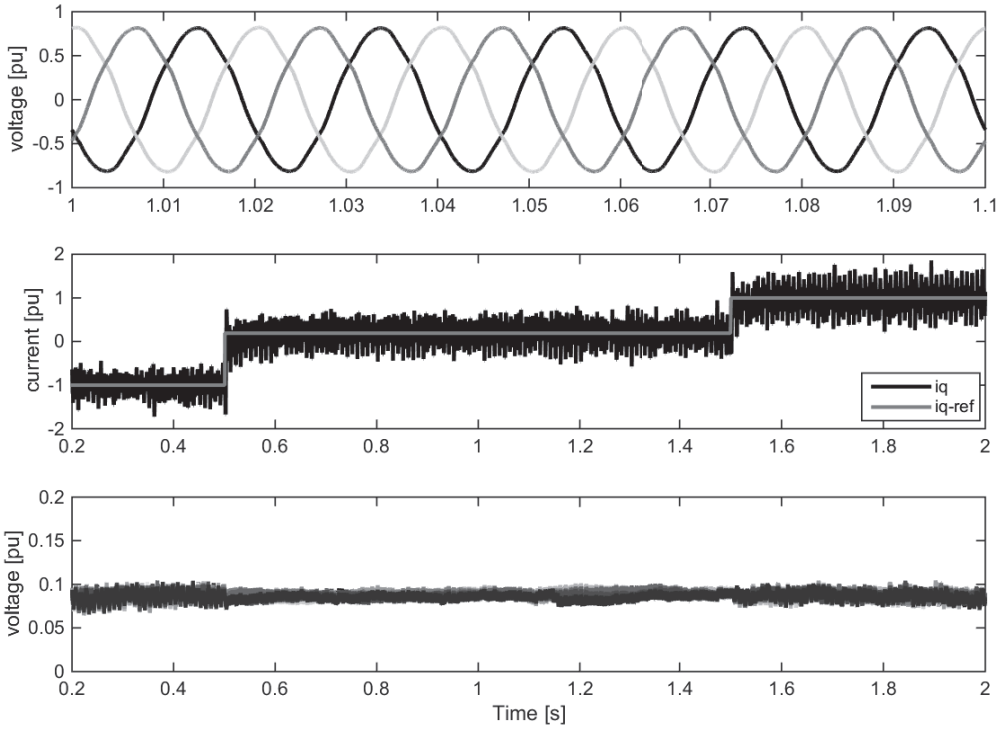


Fig. 4.27 Effect of grid voltage harmonics on the proposed method; top: Grid voltages; middle: reactive component of the current and its reference; bottom: capacitor voltages in phase *a*.

It should be noted that the extra interrupt only changes the sorting pattern and switching states of the converter between two sampling points. The proposed method does not affect the main current controller or reference voltages. Therefore this method does not imply any transient when the converter moves into or back from standby mode.

DC-link voltage modulation

The proposed DC-link voltage modulation method is applied to the same simulation case study presented in the previous section. Based on the system parameter in Table 4.1 and on (4.28), the DC-link voltage reference is defined as

$$v_{\mathrm{dc}}^{*}[\mathrm{pu}] = \begin{cases} 0.095 + 0.005\cos(2\pi 5t) & i_{\mathrm{q}}^{*} = 0 \\ 0.1 & i_{\mathrm{q}}^{*} \neq 0 \end{cases} \tag{4.31}$$

Note that the required DC-link voltage for the zero-current mode is equal to 0.09 pu. Therefore, to keep the oscillations of the DC-link voltage between 0.09 and 0.1 pu, $v_{\mathrm{dc},0}^{*}$ and v in (4.28)

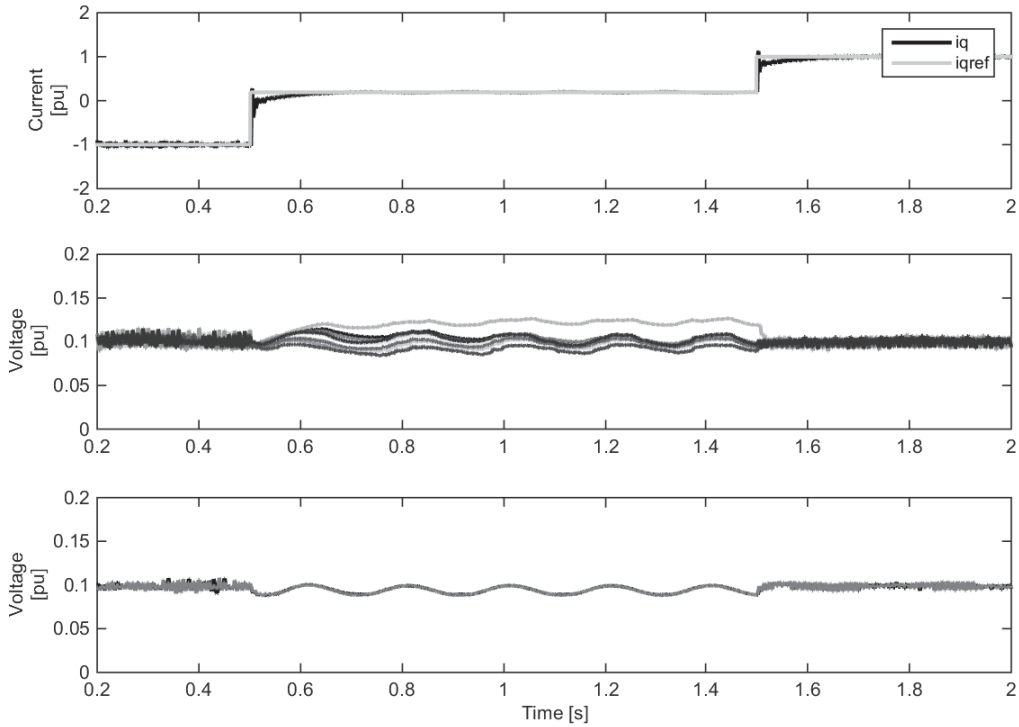


Fig. 4.28 DC-link voltages result with the DC-link voltage modulation method; top: Reactive component of the current and its reference; middle: capacitor voltages in phase *a* by using measured current in the sorting algorithm; bottom: capacitor voltages in phase *a* by using estimated current in the sorting algorithm.

are chosen to be 0.095 and 0.005 pu. 5 Hz is selected for the frequency of the DC-link voltage oscillations.

Figure. 4.28 shows the reactive current (top plot) and capacitor voltages (middle and bottom plots) when using the DC-link voltage modulation technique. The reference reactive current is set to -1 pu and then it is changed to zero and 1 pu at $t = 0.5$ s and $t = 1.5$ s respectively. Middle plot shows the capacitor voltages when the measured currents are used in the sorting algorithm, while the bottom plot shows the capacitor voltages when using the estimated currents. It can be observed that using the measured current in the sorting algorithm does not result in a perfect individual balancing while using the estimated currents leads to a proper balancing among the DC-link voltages.

As for the previous case, forward voltage drop over diodes, dead time, delay in the digital controller and noise are included in simulation model in order to evaluate the robustness of the proposed method. The same simulation as in Fig. 4.28 is implemented and the results are shown in Fig. 4.29. It can be observed that proposed method is still able to provide the correct balancing.

The resulting capacitor voltages in presence of grid voltage harmonics are shown in Fig. 4.30. The reference reactive current is the same as in the top plot of Fig. 4.28. It can be observed that in this case the individual balancing fails.

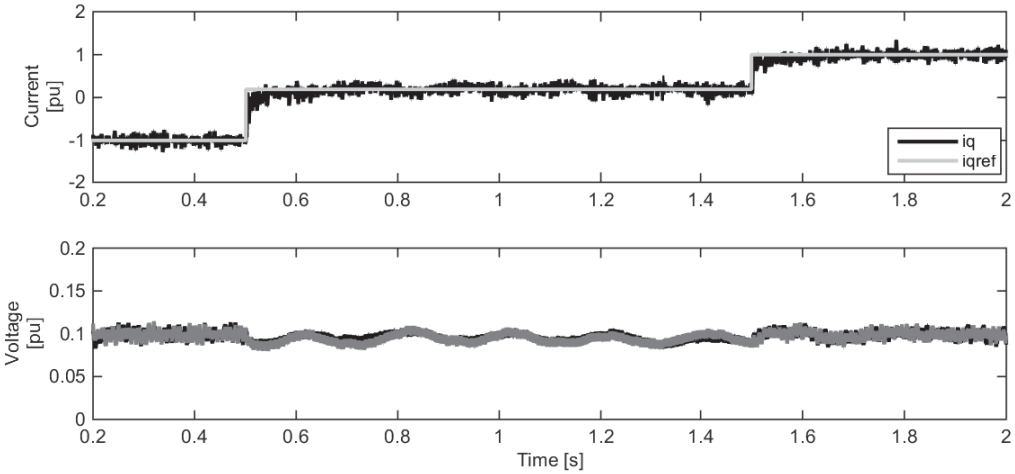


Fig. 4.29 DC-link voltages result with the DC-link voltage modulation method in presence of noise, delay, dead-time and voltage drop; top: Reactive component of the current and its reference; bottom: capacitor voltages in phase *a*.

As described in Section 3.2.3, in order to enhance the dynamic performance of the system, grid voltage feed-forward is used in the inner current controller. Although the feed-forward term allows a perfect voltage compensation under ideal conditions, problems might arise in case of distorted voltage at the connection point. As the controller is implemented in discrete time, delays due to discretization and computational time in the control computer result in a phase shift between the actual and feed-forwarded grid voltage. These phase shifts are typically compensated for the fundamental voltage component only, leading to a harmonic current flow between the VSC and the grid if additional countermeasures are not taken when implementing the current controller [85].

The presence of the harmonic currents has an impact on the decision taken by the sorting algorithm. This is due to the fact that the harmonics have an amplitude that is higher than the fundamental component. In order to avoid this effect and at the same time increase the system performance, when the converter is operated under distorted grids the current controller can be improved as suggested in [85], in order to reduce the amplitude of the current harmonics that flow in the converter phase legs. An alternative way to handle the problem is to simply increase the amplitude of the oscillations introduced in the DC-link voltage and, thereby, increase the amplitude of the fundamental current component. For the considered case, the DC-link voltage reference can be set as

$$v^*_{\mathrm{dc}}[\mathrm{pu}] = \begin{cases} 0.1 + 0.01\cos(2\pi 5t) & i^*_{\mathrm{q}} = 0 \\ 0.1 & i^*_{\mathrm{q}} \neq 0 \end{cases} \tag{4.32}$$

This indicates that carefulness must be taken in selecting the amplitude of the oscillations when the converter has to be operated under distorted conditions, in order to avoid that the DC-link voltage exceeds the ratings of the cell. Figure 4.31 shows the simulation results with the new DC-link voltage reference. It can be observed that under this condition the proposed algorithm allows to keep the capacitor voltage balanced.

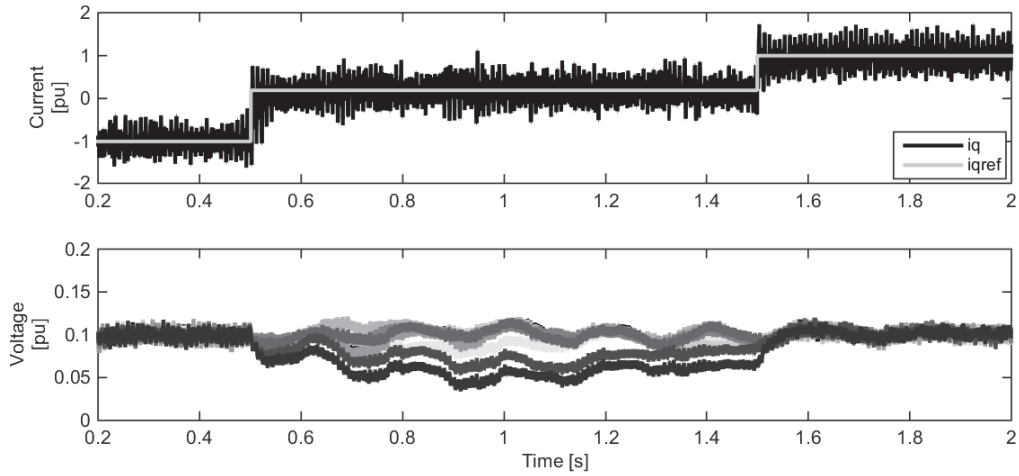


Fig. 4.30 DC-link voltages result with the DC-link voltage modulation technique in presence of grid voltage harmonics and DC-link voltage reference of (4.31).

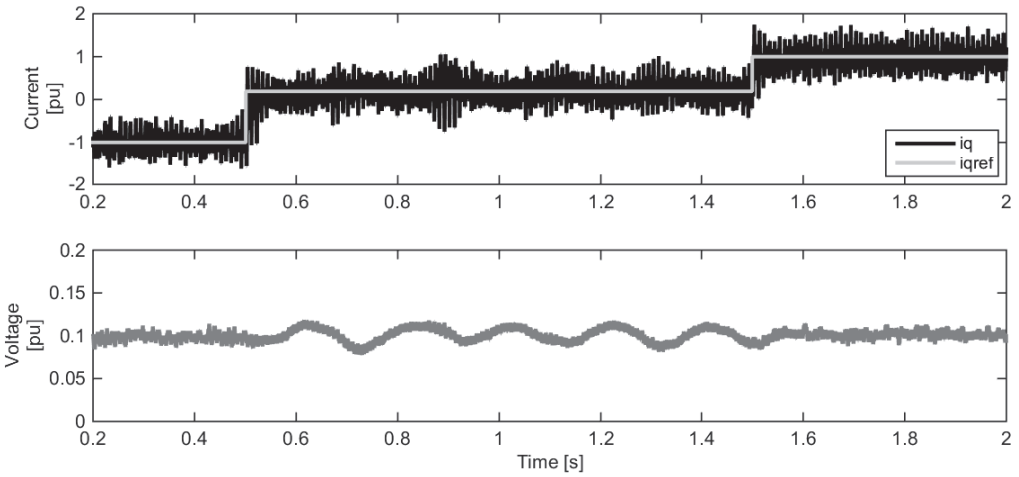


Fig. 4.31 DC-link voltages result with the DC-link voltage modulation technique in presence of grid voltage harmonics and DC-link voltage reference of (4.32).

4.5 Conclusion

In this chapter, the impact of the switching harmonics on the power distribution among the different cells of the star configuration with PS-PWM is investigated. A solution to improve the power distribution among the different cells is to select a non-integer frequency modulation ratio. The theoretical analysis gives indication on the optimal selection of the frequency modulation ratio, based on the number of cells that constitute the converter phase leg. It is of importance to stress that in practical implementations the individual DC-link voltage balancing controller is still needed, due to the unavoidable mismatch between the different harmonic components in the cells.

Two different individual DC-link voltage balancing techniques are described in this chapter: individual balancing control using extra outer control loop and sorting algorithm. Although both methods are well investigated in the literature, they are not able to provide proper balancing at zero-current mode. This chapter proposes two solutions for individual DC-link voltage balancing at zero-current operating mode: the modified sorting algorithm and the DC-link modulation technique.

Since the modified sorting algorithm uses the current ripple, the operating range of this method is limited by current ripple amplitudes. The proposed method is valid as long as the RMS value of the current is less than the current ripple amplitude and must be avoided beyond this region. Grid voltage harmonics can affect this method if the current that cause by harmonics exceed the amplitude of ripples.

The DC-link modulation technique provides easier control algorithm without the limitation of the previous method. However, if the increase in the capacitor voltages reference exceeds the safety margin of the converter, then higher safety margin for the DC-link voltage should be considered in the hardware design of the converter.

Chapter 5

Operation of CHB-STATCOM under unbalanced conditions

5.1 Introduction

The control system for the CHB-STATCOM presented in the previous chapters has been derived under the assumption that the connecting grid is perfectly balanced and that the compensator is only exchanging positive-sequence current with the grid. However, the STATCOM is often utilized for balancing purposes, both in terms of voltage and current balancing, and therefore needs to be able to properly and independently control both positive- and negative-sequence current. One of the main disadvantages of the CHB-STATCOM (in its star and delta configuration) as compared with the more traditional NPC and CCC is the lack of a common DC link and thereby the inability to exchange energy between the phase legs to guarantee an uniform active power distribution between the phase legs. For the unbalanced operation, as it will be shown later in this chapter, the cluster controller described in Section 3.2.3 is not sufficient and additional countermeasures must be taken to avoid capacitor voltage drifting.

In particular, in case of star configuration, when the system is exchanging negative-sequence current with the grid, a zero-sequence voltage must be introduced in the output phase voltage of the converter to guarantee capacitor balancing, resulting in a movement of the floating Y-point of the converter [12–15]. This leads to the need for an increased number of series-connected cells in order to realize the required phase voltage. On the other hand, the delta configuration allows negative-sequence compensation by letting a zero-sequence current circulate inside the delta, which increases the required current rating for the compensator [16–18]. Using zero-sequence voltage and current for hybrid star and hybrid delta configuration are presented in [86] and [87], respectively.

In the work presented in [19][20], the star configuration is considered as the most suitable configuration for positive-sequence reactive power control, typically for voltage regulation purpose and, more in general, for utility applications; on the other hand, delta configuration is considered to be the best solution for applications where negative sequence is required, as it is the case for industrial applications (for example, flicker mitigation).

However, requirements from Transmission System Operators (TSOs) are changing and start to demand negative-sequence injection capability for the converters connected to their grid [21]. Furthermore, the delta configuration can present limitations in injecting negative-sequence current in case of weak grids, where both load current and voltage are unbalanced, or under unbalanced fault conditions [20]. For this reason, it is of high importance to investigate the limits in terms of negative-sequence compensation for this kind of controllers.

In this chapter, the ability of CHB-STATCOMs to exchange negative-sequence current with the grid is investigated. A general solution for the required zero-sequence voltage and current under any unbalanced condition will be derived. It will be shown that both configurations exhibit a singularity in the solution of the zero-sequence component, which in turn limits the operational range of the compensator under unbalanced conditions.

5.2 Impact of unbalanced conditions on active power distribution

Figure 5.1 shows the line-diagram of a CHB-STATCOM, both in star and delta configurations. With reference to Fig. 5.1, assuming an unbalanced condition, the converter voltage and current for each phase in case of star can be written as

$$\begin{aligned}
\overline{V}_{\mathrm{a}} &= \overline{V}_{\mathrm{a}}^{+} + \overline{V}_{\mathrm{a}}^{-} = V^{+} e^{\mathrm{j}\theta_{\mathrm{v}}^{+}} + V^{-} e^{\mathrm{j}\theta_{\mathrm{v}}^{-}} \\
\overline{V}_{\mathrm{b}} &= \overline{V}_{\mathrm{b}}^{+} + \overline{V}_{\mathrm{b}}^{-} = V^{+} e^{\mathrm{j}(\theta_{\mathrm{v}}^{+} - \frac{2\pi}{3})} + V^{-} e^{\mathrm{j}(\theta_{\mathrm{v}}^{-} + \frac{2\pi}{3})} \\
\overline{V}_{\mathrm{c}} &= \overline{V}_{\mathrm{c}}^{+} + \overline{V}_{\mathrm{c}}^{-} = V^{+} e^{\mathrm{j}(\theta_{\mathrm{v}}^{+} + \frac{2\pi}{3})} + V^{-} e^{\mathrm{j}(\theta_{\mathrm{v}}^{-} - \frac{2\pi}{3})} \\
\\
\overline{I}_{\mathrm{g,a}} &= \overline{I}_{\mathrm{g,a}}^{+} + \overline{I}_{\mathrm{g,a}}^{-} = I^{+} e^{\mathrm{j}\delta_{\mathrm{i}}^{+}} + I^{-} e^{\mathrm{j}\delta_{\mathrm{i}}^{-}} \\
\overline{I}_{\mathrm{g,b}} &= \overline{I}_{\mathrm{g,b}}^{+} + \overline{I}_{\mathrm{g,b}}^{-} = I^{+} e^{\mathrm{j}(\delta_{\mathrm{i}}^{+} - \frac{2\pi}{3})} + I^{-} e^{\mathrm{j}(\delta_{\mathrm{i}}^{-} + \frac{2\pi}{3})} \\
\overline{I}_{\mathrm{g,c}} &= \overline{I}_{\mathrm{g,c}}^{+} + \overline{I}_{\mathrm{g,c}}^{-} = I^{+} e^{\mathrm{j}(\delta_{\mathrm{i}}^{+} + \frac{2\pi}{3})} + I^{-} e^{\mathrm{j}(\delta_{\mathrm{i}}^{-} - \frac{2\pi}{3})}
\end{aligned} \tag{5.1}$$

with

- V^{-},V^{+}: negative- and positive-sequence voltage phasor amplitude
- θ_{v}^{-},θ_{v}^{+}: negative- and positive-sequence voltage phasor angle
- I^{-},I^{+}: negative- and positive-sequence current phasor amplitude
- δ_{i}^{-},δ_{i}^{+}: negative- and positive-sequence current phasor angle

The active power in each phase (P_{ava}, P_{avb}, P_{avc}) can be calculated by the inner product of the phase current and voltage for each phase as

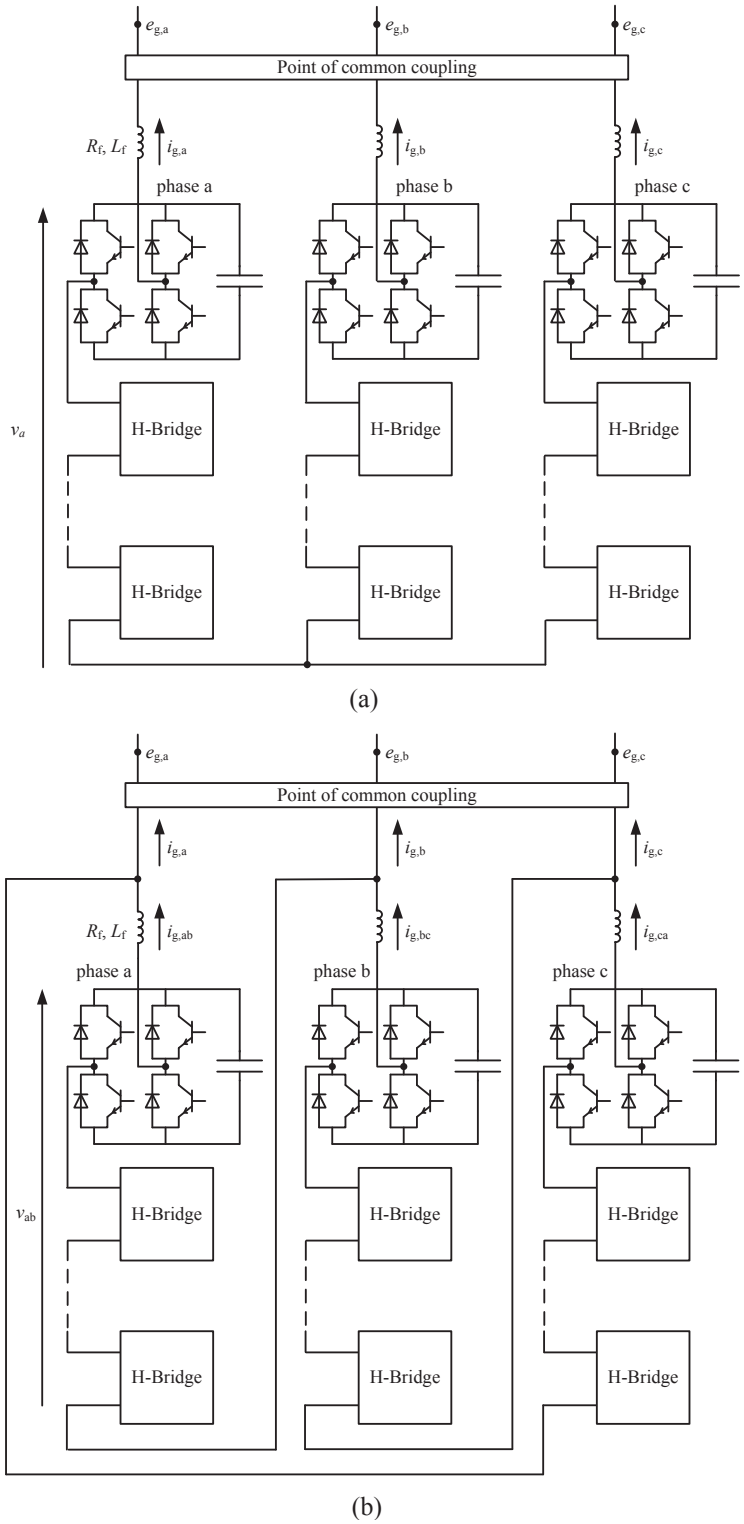


Fig. 5.1 Cascaded H-bridge multilevel converter. (a) star configuration, (b) delta configuration.

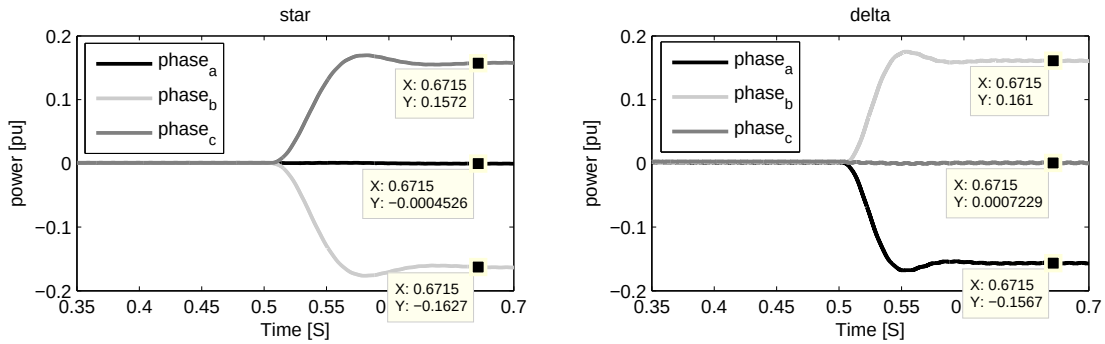


Fig. 5.2 Effect of unbalanced condition on average active power at each phase for CHB-STATCOMs.

$$
\begin{aligned}
P_{\text{ava}} &= \frac{V^+I^+}{2}\cos(\theta_{\text{v}}^+ - \delta_{\text{i}}^+) + \frac{V^-I^-}{2}\cos(\theta_{\text{v}}^- - \delta_{\text{i}}^-) \\
&\quad + \frac{V^+I^-}{2}\cos(\theta_{\text{v}}^+ - \delta_{\text{i}}^-) + \frac{V^-I^+}{2}\cos(\theta_{\text{v}}^- - \delta_{\text{i}}^+) \\
P_{\text{avb}} &= \frac{V^+I^+}{2}\cos(\theta_{\text{v}}^+ - \delta_{\text{i}}^+) + \frac{V^-I^-}{2}\cos(\theta_{\text{v}}^- - \delta_{\text{i}}^-) \\
&\quad + \frac{V^+I^-}{2}\cos(\theta_{\text{v}}^+ - \delta_{\text{i}}^- - \frac{4\pi}{3}) + \frac{V^-I^+}{2}\cos(\theta_{\text{v}}^- - \delta_{\text{i}}^+ + \frac{4\pi}{3}) \\
P_{\text{avc}} &= \frac{V^+I^+}{2}\cos(\theta_{\text{v}}^+ - \delta_{\text{i}}^+) + \frac{V^-I^-}{2}\cos(\theta_{\text{v}}^- - \delta_{\text{i}}^-) \\
&\quad + \frac{V^+I^-}{2}\cos(\theta_{\text{v}}^+ - \delta_{\text{i}}^- + \frac{4\pi}{3}) + \frac{V^-I^+}{2}\cos(\theta_{\text{v}}^- - \delta_{\text{i}}^+ - \frac{4\pi}{3})
\end{aligned}
\tag{5.2}
$$

It can be observed from (5.2) that each phase of the converter is characterized by a different active power, due to the interaction between the sequence components. Similar result is also valid for delta structure.

In order to show the effect of an unbalanced condition on the phase active powers, the CHB-STATCOMs are here simulated when injecting a negative-sequence current in the grid. For this simulation, the DC-link capacitors are replaced by fixed DC sources. Figure 5.2 shows the active power flowing in each phase of the star and delta configurations. For clarity of the illustration, the powers are low-pass filtered in order to remove the double-frequency component. The grid is balanced and the STATCOM is injecting 0.9 pu positive-sequence current in the grid. At $t = 0.5$ s the negative-sequence current is stepped from 0 pu to 0.4 pu. It is clearly possible to observe from the figure that under this condition, different active powers will flow in each phase leg; this would lead to diverging DC-capacitor voltages in the phase legs.

5.3 Control solution under unbalanced conditions

The control system of the CHB-STATCOM must guarantee that the active power is equally distributed among the phase legs, in order to compensate for the system losses and keep the charge of the DC capacitors. Considering the star configuration, a zero-sequence voltage can be added to all phases to fulfill this requirement. Assuming an unbalanced condition of the system and with reference to Fig. 5.1(a), the phasors of the converter phase voltage and current for phase *a* can be written as

$$\begin{aligned} \overline{V}_{\mathrm{a}} &= V^{+}e^{\mathrm{j}\theta_{\mathrm{v}}^{+}} + V^{-}e^{\mathrm{j}\theta_{\mathrm{v}}^{-}} + V_0 e^{\mathrm{j}\theta_{\mathrm{v}_0}} \\ \overline{I}_{\mathrm{g,a}} &= I^{+}e^{\mathrm{j}\delta_{\mathrm{i}}^{+}} + I^{-}e^{\mathrm{j}\delta_{\mathrm{i}}^{-}} \end{aligned} \tag{5.3}$$

with

- V^{-},V^{+}: negative- and positive-sequence voltage phasor amplitude
- θ_{v}^{-},θ_{v}^{+}: negative- and positive-sequence voltage phasor angle
- I^{-},I^{+}: negative- and positive-sequence current phasor amplitude
- δ_{i}^{-},δ_{i}^{+}: negative- and positive-sequence current phasor angle

Analogous relations hold for the other two phases of the converter.

The introduction of a zero-sequence voltage allows two degrees of freedom, in terms of amplitude (V_0) and angle ($\theta_{\mathrm{v}0}$). The goal is to find a suitable value for V_0 and $\theta_{\mathrm{v}0}$ to remove the interaction between the sequence components and thus provide an uniform active power distribution among phases. Considering phases *a* and *b* and considering zero-sequence voltage injection, the total active power can be written as

$$\begin{aligned} P_{\mathrm{a}} = {} & \frac{V^{+}I^{+}}{2}\cos(\theta_{\mathrm{v}}^{+} - \delta_{\mathrm{i}}^{+}) + \frac{V^{-}I^{-}}{2}\cos(\theta_{\mathrm{v}}^{-} - \delta_{\mathrm{i}}^{-}) + \\ & + \frac{V^{+}I^{-}}{2}\cos(\theta_{\mathrm{v}}^{+} - \delta_{\mathrm{i}}^{-}) + \frac{V^{-}I^{+}}{2}\cos(\theta_{\mathrm{v}}^{-} - \delta_{\mathrm{i}}^{+}) + \\ & + \frac{V_0 I^{-}}{2}\cos(\theta_{\mathrm{v}_0} - \delta_{\mathrm{i}}^{-}) + \frac{V_0 I^{+}}{2}\cos(\theta_{\mathrm{v}_0} - \delta_{\mathrm{i}}^{+}) \\ P_{\mathrm{b}} = {} & \frac{V^{+}I^{+}}{2}\cos(\theta_{\mathrm{v}}^{+} - \delta_{\mathrm{i}}^{+}) + \frac{V^{-}I^{-}}{2}\cos(\theta_{\mathrm{v}}^{-} - \delta_{\mathrm{i}}^{-}) + \\ & + \frac{V^{+}I^{-}}{2}\cos(\theta_{\mathrm{v}}^{+} - \delta_{\mathrm{i}}^{-} - \frac{4\pi}{3}) + \frac{V^{-}I^{+}}{2}\cos(\theta_{\mathrm{v}}^{-} - \delta_{\mathrm{i}}^{+} + \frac{4\pi}{3}) + \\ & + \frac{V_0 I^{-}}{2}\cos(\theta_{\mathrm{v}_0} - \delta_{\mathrm{i}}^{-} - \frac{2\pi}{3}) + \frac{V_0 I^{+}}{2}\cos(\theta_{\mathrm{v}_0} - \delta_{\mathrm{i}}^{+} + \frac{2\pi}{3}) \end{aligned} \tag{5.4}$$

The first two terms in (5.4) indicate the active power expressions associated to the positive- and negative-sequence components. These terms are equal in all phases and can be controlled through the overall DC-link voltage controller, as it will be shown in Section 5.4.2. The 3$^{\text{rd}}$ and 4$^{\text{th}}$ term denote the active power generated by the interaction between positive- and negative-sequence components; this interaction is responsible for the uneven power distribution between the phases. Finally, the last two terms in (5.4) are the active power terms generated by the zero-sequence voltage injection. Two main components can be identified in (5.4), an active power component that is common among the phases (P_{com}) and a component caused by the interaction between the different sequences (P_{dis}):

$$\begin{aligned}
P_{\text{com}} &= \frac{V^+I^+}{2}\cos(\theta_{\text{v}}^+ - \delta_{\text{i}}^+) + \frac{V^-I^-}{2}\cos(\theta_{\text{v}}^- - \delta_{\text{i}}^-) \\
P_{\text{disa}} &= \frac{V^+I^-}{2}\cos(\theta_{\text{v}}^+ - \delta_{\text{i}}^-) + \frac{V^-I^+}{2}\cos(\theta_{\text{v}}^- - \delta_{\text{i}}^+) + \\
&\quad + \frac{V_0I^-}{2}\cos(\theta_{\text{v}_0} - \delta_{\text{i}}^-) + \frac{V_0I^+}{2}\cos(\theta_{\text{v}_0} - \delta_{\text{i}}^+) \\
P_{\text{disb}} &= \frac{V^+I^-}{2}\cos(\theta_{\text{v}}^+ - \delta_{\text{i}}^- - \frac{4\pi}{3}) + \frac{V^-I^+}{2}\cos(\theta_{\text{v}}^- - \delta_{\text{i}}^+ + \frac{4\pi}{3}) + \\
&\quad + \frac{V_0I^-}{2}\cos(\theta_{\text{v}_0} - \delta_{\text{i}}^- - \frac{2\pi}{3}) + \frac{V_0I^+}{2}\cos(\theta_{\text{v}_0} - \delta_{\text{i}}^+ + \frac{2\pi}{3})
\end{aligned} \tag{5.5}$$

Under ideal conditions, the interaction between sequences is the only disturbing factor that leads to the uneven power distribution between the different phases. Therefore, calculating an appropriate zero-sequence voltage amplitude and phase that makes $P_{\text{disa}} = P_{\text{disb}} = 0$ will be sufficient to guarantee the balancing of the DC capacitors voltages. However, in practical applications other factors (such as different components characteristics) will impact the active power flowing in the phase legs. Therefore, (5.5) can be solved for a general case to find the appropriate zero-sequence voltage to compensate any kind of power disturbance as well as interaction between negative- and positive-sequences. Let us introduce two new variables K_1 and K_2, defined as:

$$\begin{aligned}
K_1 &= \frac{V^+I^-}{2}\cos(\theta_{\text{v}}^+ - \delta_{\text{i}}^-) + \frac{V^-I^+}{2}\cos(\theta_{\text{v}}^- - \delta_{\text{i}}^+) \\
K_2 &= \frac{V^+I^-}{2}\cos(\theta_{\text{v}}^+ - \delta_{\text{i}}^- - \frac{4\pi}{3}) + \frac{V^-I^+}{2}\cos(\theta_{\text{v}}^- - \delta_{\text{i}}^+ + \frac{4\pi}{3})
\end{aligned} \tag{5.6}$$

Expanding the cosine terms in (5.4), P_{disa} and P_{disb} can be rewritten as

$$
\begin{aligned}
P_{\text{disa}} &= K_1 + V_0\cos(\theta_{\text{v}_0})[\underbrace{\frac{I^-}{2}\cos(\delta_{\text{i}}^-) + \frac{I^+}{2}\cos(\delta_{\text{i}}^+)}_{K_3=\frac{1}{2}\text{Re}[\overline{I}_{\text{g,a}}]}] + \\
&\quad + V_0\sin(\theta_{\text{v}_0})[\underbrace{\frac{I^-}{2}\sin(\delta_{\text{i}}^-) + \frac{I^+}{2}\sin(\delta_{\text{i}}^+)}_{K_4=\frac{1}{2}\text{Im}[\overline{I}_{\text{g,a}}]}] \\
P_{\text{disb}} &= K_2 + V_0\cos(\theta_{\text{v}_0})[\underbrace{\frac{I^-}{2}\cos(\delta_{\text{i}}^- + \frac{2\pi}{3}) + \frac{I^+}{2}\cos(\delta_{\text{i}}^+ - \frac{2\pi}{3})}_{K_5=\frac{1}{2}\text{Re}[\overline{I}_{\text{g,b}}]}] + \\
&\quad + V_0\sin(\theta_{\text{v}_0})[\underbrace{\frac{I^-}{2}\sin(\delta_{\text{i}}^- + \frac{2\pi}{3}) + \frac{I^+}{2}\sin(\delta_{\text{i}}^+ - \frac{2\pi}{3})}_{K_6=\frac{1}{2}\text{Im}[\overline{I}_{\text{g,b}}]}]
\end{aligned}
\tag{5.7}
$$

The set of equations above can be simplified in order to isolate the terms that involves the zero-sequence voltage as:

$$
\begin{aligned}
P_{\text{disa}} - K_1 &= K_3 V_0\cos(\theta_{\text{v}_0}) + K_4 V_0\sin(\theta_{\text{v}_0}) \\
P_{\text{disb}} - K_2 &= K_5 V_0\cos(\theta_{\text{v}_0}) + K_6 V_0\sin(\theta_{\text{v}_0})
\end{aligned}
\tag{5.8}
$$

where the different terms have the meaning as indicated in (5.7). Solving (5.8), the phase angle and amplitude of the zero-sequence voltage are [88]

$$
\begin{aligned}
\tan\theta_{\text{v}_0} &= \frac{(P_{\text{disb}} - K_2)K_3 - (P_{\text{disa}} - K_1)K_5}{(P_{\text{disa}} - K_1)K_6 - (P_{\text{disb}} - K_2)K_4} \\
V_0 &= \frac{P_{\text{disa}} - K_1}{K_3\cos(\theta_{\text{v}_0}) + K_4\sin(\theta_{\text{v}_0})} = \frac{P_{\text{disb}} - K_2}{K_5\cos(\theta_{\text{v}_0}) + K_6\sin(\theta_{\text{v}_0})}
\end{aligned}
\tag{5.9}
$$

As mentioned earlier, for the delta configuration a circulating current ($I_0 e^{\text{j}\delta_{\text{i}_0}}$) can be used to guarantee capacitor balancing. The circulating current flows only inside the delta, allowing power exchange between the phases without affecting the grid. Similar to the star configuration, the zero-sequence current allows two degrees of freedom in terms of its amplitude and phase. Assuming an unbalanced condition and with reference to Fig. 5.1(b), the converter phase voltage and current for phase *a* can be written as

$$
\begin{aligned}
\overline{V}_{\text{ab}} &= V^+ e^{\text{j}\theta_{\text{v}}^+} + V^- e^{\text{j}\theta_{\text{v}}^-} \\
\overline{I}_{\text{g,ab}} &= I^+ e^{\text{j}\delta_{\text{i}}^+} + I^- e^{\text{j}\delta_{\text{i}}^-} + I_0 e^{\text{j}\delta_{\text{i}_0}}
\end{aligned}
\tag{5.10}
$$

Following the same criteria adopted for the star case, the amplitude and phase of the zero-sequence current can be calculated as [88]

$$\begin{aligned} \tan\delta_{i_0} &= \frac{(P_{disa}-K_{11})K_{15}-(P_{disb}-K_{12})K_{13}}{(P_{disb}-K_{12})K_{14}-(P_{disa}-K_{11})K_{16}} \\ I_0 &= \frac{P_{disa}-K_{11}}{K_{13}\cos(\delta_{i_0})+K_{14}\sin(\delta_{i_0})} = \frac{P_{disb}-K_{12}}{K_{15}\cos(\delta_{i_0})+K_{16}\sin(\delta_{i_0})} \end{aligned} \tag{5.11}$$

where the different constant terms are defined as

$$\begin{aligned} K_{11} &= \frac{V^+I^-}{2}\cos(\theta_v^+-\delta_i^-)+\frac{V^-I^+}{2}\cos(\theta_v^--\delta_i^+) \\ K_{12} &= \frac{V^+I^-}{2}\cos(\theta_v^+-\delta_i^--\frac{4\pi}{3})+\frac{V^-I^+}{2}\cos(\theta_v^--\delta_i^++\frac{4\pi}{3}) \\ K_{13} &= \frac{1}{2}\mathrm{Re}[\overline{V}_{ab}], K_{14} = \frac{1}{2}\mathrm{Im}[\overline{V}_{ab}] \\ K_{15} &= \frac{1}{2}\mathrm{Re}[\overline{V}_{bc}], K_{16} = \frac{1}{2}\mathrm{Im}[\overline{V}_{bc}] \end{aligned} \tag{5.12}$$

5.4 Control design

The aim of the implemented controller is to track both positive- and negative-sequence reference currents while at the same time control the DC-link voltages at a desired reference value. The overall control block diagram is shown in Fig. 5.3. Three phase quantities are transferred to the rotating dq-reference frame using a transformation angle θ, provided by the PLL. Positive- and negative-sequence components of the measured signals are estimated using Delayed Signal Cancellation (DSC) technique [89] and are independently controlled using a Dual Vector Current Control (DVCC). A detailed description of each part of the controller is provided in following.

5.4.1 Dual Vector Current-controller (DVCC)

The DVCC is constituted by two separate PI-based Current Controllers (CCs) implemented in the positive- and in the negative-synchronous reference frame, as shown in Fig. 5.4. Both grid voltage and filter current are separated into positive- and negative-sequence components and the controller tracks the corresponding reference currents. The CC outputs are the positive- and negative-sequence components of the reference output voltages in the corresponding dq-

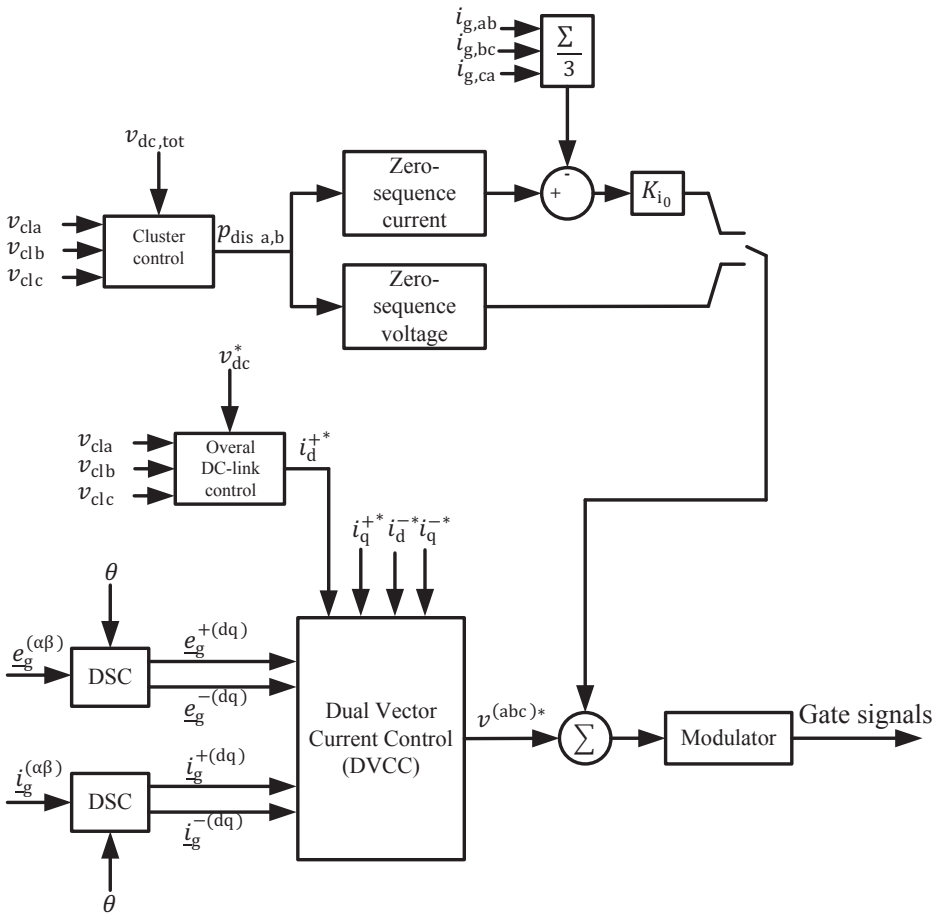


Fig. 5.3 Overall control block diagram.

reference frame, given by:

$$\begin{aligned}\underline{v}^{+(dq)*} &= \underline{e}_g^{+(dq)} + j\omega L_f \underline{i}_g^{+(dq)} + \left(K_p + \frac{K_i}{s}\right)\left(\underline{i}^{+(dq)*} - \underline{i}_g^{+(dq)}\right)\\ \underline{v}^{-(dq)*} &= \underline{e}_g^{-(dq)} - j\omega L_f \underline{i}_g^{-(dq)} + \left(K_p + \frac{K_i}{s}\right)\left(\underline{i}^{-(dq)*} - \underline{i}_g^{-(dq)}\right)\end{aligned} \tag{5.13}$$

where $\underline{v}^{+(dq)*}$,$\underline{v}^{-(dq)*}$ and $\underline{e}_g^{+(dq)}$,$\underline{e}_g^{-(dq)}$ are the reference and grid dq positive- and negative -sequence voltages, respectively, while $\underline{i}^{+(dq)*}$,$\underline{i}^{-(dq)*}$ and $\underline{i}_g^{+(dq)}$,$\underline{i}_g^{-(dq)}$ are the positive- and negative-sequence components of the reference and actual grid currents, respectively. L_f is the filter inductance, ω is the angular frequency of the grid voltage and K_p and K_i are the controller proportional and integral gain, tuned as suggested in [90]. It should be noted that in (5.13) L_f should be replaced by $L_f/3$ for the delta configuration. (see also Section 3.2.3).

The obtained reference voltages are then transformed back to three-phase quantities and the converter switching pattern is obtained in the modulator block in Fig. 5.3 using sorting approach.

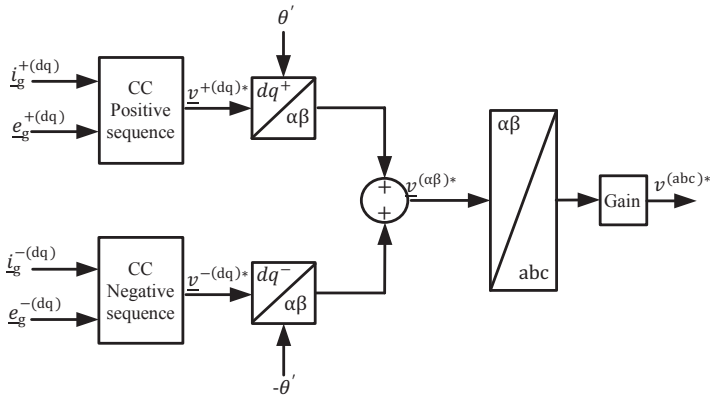


Fig. 5.4 Block diagram of dual vector current-controller (DVCC). $\theta' = \theta$ and Gain=1 for star case or $\theta' = \theta + \frac{\pi}{6}$ and Gain=$\sqrt{3}$ for delta case.

5.4.2 DC-link voltage control

The DC-link voltage control comprises of two stages:

1. Overall DC-link voltage control.
2. Cluster voltage (defined as the average DC-link voltage in each phase) control.

The overall DC-link voltage control is responsible to provide sufficient power to maintain the charge of all DC capacitors in the three phases. Using a voltage-oriented dq transformation (d-axis aligned with the grid-voltage vector) and setting the negative-sequence active power to zero ($e_{gd}^{-} i_{gd}^{-} + e_{gq}^{-} i_{gq}^{-} = 0$), the total three phase power on the AC side is equal to

$$p_{tot} = e_{gd}^{+} i_{gd}^{+} \tag{5.14}$$

The active power balance equation from the AC and DC side can be written as

$$\begin{aligned} p_{tot} = e_{gd}^{+} i_{gd}^{+} &= \frac{1}{2}\frac{C_{dc}}{n}\left[\frac{d}{dt}(\sum_{k=1}^{n} v_{dc,k}^{a})^2 + \frac{d}{dt}(\sum_{k=1}^{n} v_{dc,k}^{b})^2 + \frac{d}{dt}(\sum_{k=1}^{n} v_{dc,k}^{c})^2\right] \\ &= \frac{1}{2} n C_{dc} \frac{d}{dt}\left[(\frac{\sum_{k=1}^{n} v_{dc,k}^{a}}{n})^2 + (\frac{\sum_{k=1}^{n} v_{dc,k}^{b}}{n})^2 + (\frac{\sum_{k=1}^{n} v_{dc,k}^{c}}{n})^2\right] \\ &= \frac{3nC_{dc}}{2}\frac{d}{dt}\left[\frac{(v_{cla})^2 + (v_{clb})^2 + (v_{clc})^2}{3}\right] \end{aligned} \tag{5.15}$$

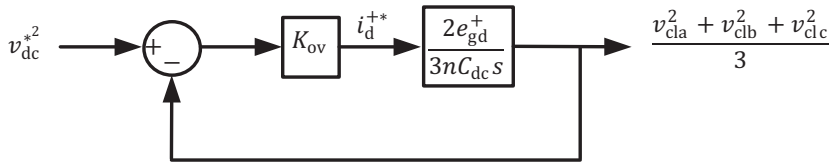


Fig. 5.5 Closed-loop block diagram of the overall DC-link voltage controller.

where n is the number of cells per phase and C_{dc} is the DC-link capacitor. Equation (5.15) can be written in Laplace domain as

$$e_{gd}^+ i_{gd}^+ = \frac{3n}{2} C_{dc} s \left[\frac{(v_{cla})^2 + (v_{clb})^2 + (v_{clc})^2}{3} \right] \tag{5.16}$$

The active power flow is controlled through the direct component of the positive-sequence current, as [90]

$$i_d^{+*} = K_{ov} \left\{ v_{dc}^{*2} - \left[\frac{(v_{cla})^2 + (v_{clb})^2 + (v_{clc})^2}{3} \right] \right\} \tag{5.17}$$

where K_{ov} is the controller gain and v_{dc}^* is the reference value for the DC-link voltage. Using (5.16) and (5.17) and considering an ideal current regulation ($i_{gd}^+ = i_d^{+*}$), the closed-loop block diagram of the overall DC-link voltage controller is displayed in Fig. 5.5.

The closed-loop transfer function of the overall DC-link voltage controller is

$$G_{ov} = \frac{\frac{2K_{ov}e_{gd}^+}{3nC_{dc}}}{s + \frac{2K_{ov}e_{gd}^+}{3nC_{dc}}} \tag{5.18}$$

which is a low pass filter with bandwidth of α_{ov}. The gain of the proportional controller can be design based on the desired bandwidth as

$$\alpha_{ov} = \frac{2K_{ov}e_{gd}^+}{3nC_{dc}} \Rightarrow K_{ov} = \frac{\alpha_{ov} 3nC_{dc}}{2e_{gd}^+} \tag{5.19}$$

The same overall DC-link controller can be used for both star and delta.

The cluster voltage control calculates the amount of zero-sequence voltage from (5.9) for the star configuration or zero-sequence current from (5.11) for the delta. This is here achieved through the control of the disturbance power p_{disa} and p_{disb} as

$$\begin{aligned} p_{disa} &= k_z \left(\frac{(v_{cla})^2 + (v_{clb})^2 + (v_{clc})^2}{3} - v_{cla}^2 \right) \\ p_{disb} &= k_z \left(\frac{(v_{cla})^2 + (v_{clb})^2 + (v_{clc})^2}{3} - v_{clb}^2 \right) \end{aligned} \tag{5.20}$$

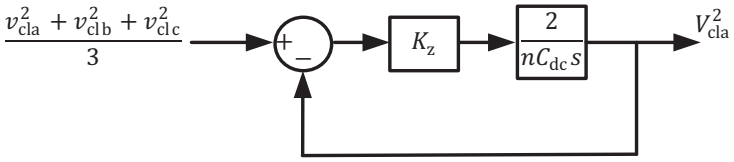


Fig. 5.6 Closed-loop block diagram of the cluster voltage controller.

where k_z is a proportional gain and v_{cla} and v_{clb} are the cluster voltages of phase *a* and *b*, respectively. The active power equation for the cluster voltages can then be written as

$$\frac{1}{2}nC_{dc}s(v_{cla}^2) = p_{disa} \tag{5.21}$$

where p_{disa} represents any disturbance that causes the cluster voltages to deviate. Replacing (5.20) into (5.21), the closed-loop block diagram of the cluster controller can be shown as Fig. 5.6. The closed-loop transfer function of the cluster voltage controller is

$$G_z = \frac{\frac{2K_z}{nC_{dc}}}{s + \frac{2K_z}{nC_{dc}}} = \frac{\alpha_z}{s+\alpha_z} \tag{5.22}$$

where α_z is the bandwidth of the cluster controller. From (5.22) the proportional gain of the cluster voltage control is given by

$$K_z = \frac{nC_{dc}\alpha_z}{2} \tag{5.23}$$

which can be used for both star and delta.

Note that the zero-sequence voltage calculated for the star configuration can be directly added to the reference voltages output from the DVCC(see Fig. 5.3); for the delta configuration, instead, the zero-sequence voltage that leads to the desired current circulation is obtained through a proportional controller of gain K_{io} as

$$v_{i0} = K_{io}\left(i_0\cos(\theta + \delta_{i0}) - \frac{(i_{a\Delta} + i_{b\Delta} + i_{c\Delta})}{3}\right) \tag{5.24}$$

5.4.3 Simulation results

The control method is verified for both star and delta with the system and control parameters reported in Table 5.1. Note that, in order to preserve the number of levels between the two configurations, the DC-link voltage is doubled for the star case, in order to provide enough margin for the zero-sequence voltage under unbalanced condition.

The overall DC-link voltage control is designed based on a fast current controller assumption.

TABLE 5.1. SYSTEM AND CONTROL PARAMETERS FOR UNBALANCED CONDITIONS

Parameters	values
Rated power S_b	120 MVA,1 pu
Rated voltage V_b	33 kV,1 pu
System frequency f_g	50 Hz
Filter inductor L_f	4.33 mH,0.15 pu
Filter resistor R_f	0.136 Ω,0.015 pu
Cells capacitor C_{dc}	4 mF,0.09 pu
DC-link voltage for star V_{dc}	20 kV,0.6 pu
DC-link voltage for delta V_{dc}	$10\sqrt{3}$ kV,0.525 pu
Carrier frequency f_{cr}	3000 Hz
Cell numbers n	3
Closed loop current control bandwidth α_i	$2\pi \times 500$ rad/sec
Closed-loop DVCC control band width α_i	$2\pi \times 500$ rad/sec
Closed-loop overall DC-link control band width α_{ov}	$2\pi \times 10$ rad/sec
Closed-loop cluster control band width α_z,α_{zd},α_{zs}	$2\pi \times 10$ rad/sec
Zero-sequence current gain K_{io}	10
PLL bandwidth α_{PLL}	$2\pi \times 5$ rad/sec
Observer gain k_{psp}	0.1

Therefore the bandwidth of the overall and cluster DC-link voltage control is intentionally chosen to be much lower than the DVCC bandwidth.

Figure 5.7 shows the simulation results for both star and delta configurations under unbalanced condition. Top figures show the DC-link voltages. Zero-sequence voltage and current are shown in the middle plot. Bottom plots show the reference and the actual negative- and positive-sequence q-component of the current. All parameters are in pu. From $t = 0.5$ s to $t = 0.7$ s, the grid voltage is balanced and only positive-sequence currents are exchanged with the grid. It can be observed that under this balanced condition, the zero-sequence voltage and current are equal to zero. At $t = 0.7$ s a step change is applied only in the positive-sequence current. Since the system is still under balanced conditions the required zero-sequence voltage or current is zero.

From $t = 0.8$ s to $t = 1.2$ s, the converters are exchanging both positive- and negative-sequence current with the grid while the grid voltage is still balanced. It can be seen that under this unbalanced condition the cluster controller sets a zero-sequence voltage or current in order to guarantee capacitor voltage balancing.

From $t = 1$ s to $t = 1.1$ s the cluster controller for both converters is intentionally disabled. This means that the zero-sequence voltage and current under this unbalanced condition are set to zero. It can be seen from the simulated capacitor voltages that without this controller the cluster voltages start to deviate from their average value, due to the non-uniform active power distribution among the phases. At $t = 1.1$ s the cluster controller is reactivated and cluster voltages are controlled back to the desired value.

From $t = 1.2$ s to $t = 1.4$ s, a 13% degree of unbalanced ($e_g^- / e_g^+ = 0.13$) is set for the grid vol-

tage. DC-link voltage results show the ability of the cluster controller to provide an appropriate zero-sequence voltage and current to control the cluster voltages under this new unbalanced condition.

Simulation results for the reactive component of the current are also showing the proper operation of the DVCC in providing an independent negative- and positive-sequence current control; only a small cross-coupling between the sequence components, due to the dynamic performance of the implemented DSC for sequence separation, can be observed during the simulated current steps.

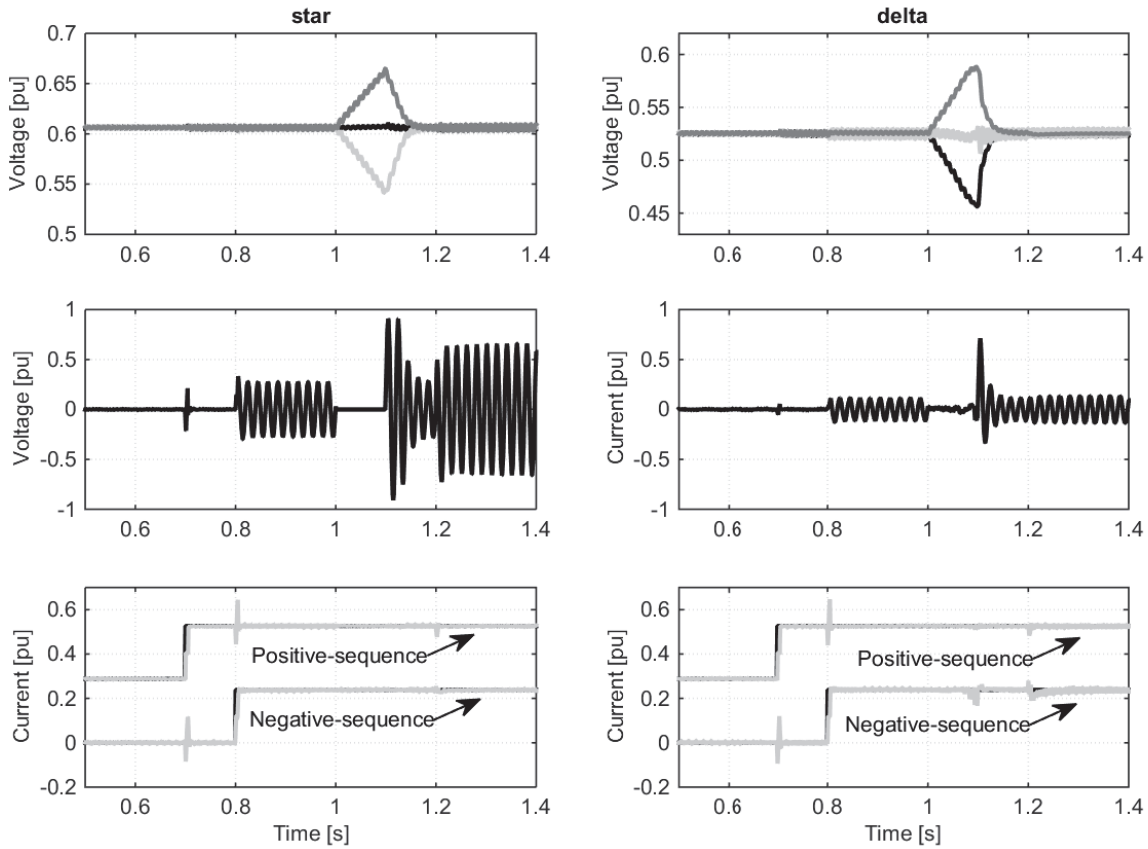


Fig. 5.7 Transient responses of star and delta configurations under unbalanced condition; top: DC-link voltages in three phases; middle: zero-sequence voltage and current; bottom: negative- and positive-sequence *q*-component of the current.

Figure 5.8 shows the grid three-phase voltage and current from the previous simulation. For clarity purpose, the grid three-phase voltages are shown only from $t = 1.16$ s to $t = 1.24$ s. As it mentioned earlier, at $t = 1.2$ s 13% degree of unbalanced is applied to the grid voltage. The grid three-phase currents are shown from $t = 0.76$ s to $t = 0.84$ s. It was shown that until $t = 0.8$ s, only positive-sequence current is exchanging between the grid and the converters. At $t = 0.8$ s a step change is applied to the negative-sequence current. This leads to three-phase unbalanced currents as can be seen in this figure.

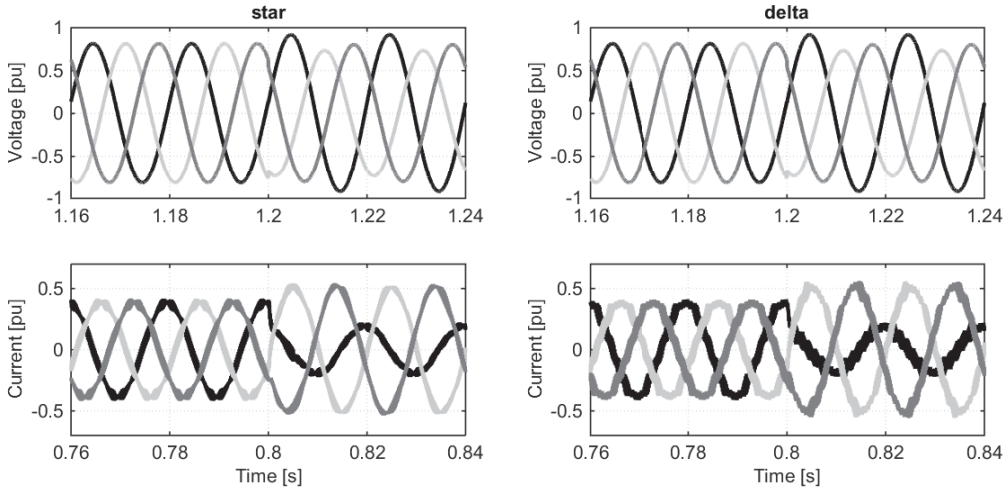


Fig. 5.8 The grid three-phase voltage and current. (Same case study as Fig. 5.7).

5.5 Operating range of CHB-STATCOMs under unbalanced conditions

5.5.1 General comparison

The comparison between the CHB-STATCOMs operating range is based on the required zero-sequence current and voltage to guarantee capacitor balancing under unbalanced conditions. According with (5.9) and based on the variables K_3 to K_6 in (5.7), it is possible to conclude that the star configuration is mainly sensitive to the amount of positive- and negative-sequence currents that the converter exchanges with the grid. Similarly, according with (5.11) and based on K_{13} to K_{16} defined in (5.12), the delta configuration is sensitive to the amplitude of the positive- and negative-sequence components of the voltage applied at the converter terminals.

To analyse the sensitivity for these two configurations, two case studies are here investigated; for the star configuration, it is assumed that the grid is balanced (thus, the grid voltage is only constituted by a positive-sequence component) while the converter is exchanging both positive- and negative-sequence current with the grid. For simplicity of the analysis, two operating conditions for the converter are here considered: the two current sequences have the same phase angle (for example, both positive- and negative-sequence currents are injected into the grid) or the current sequences are opposite in phase (for example, positive-sequence current is injected into the grid while the negative-sequence is absorbed by the compensator). In a dual situation, for the delta configuration it is assumed that the grid is unbalanced and the converter exchanges only positive-sequence current with the grid. The phase shift between the two sequence components of the voltage depends on a number of factors, for example the grid impedance and, in case of unbalance due to fault conditions, on the fault location; here it is assumed that the phase shift between positive- and negative-sequence voltage is either equal to zero or to π, in order to highlight the duality between the two configurations. It is also assumed that the filter impedance between the grid and converter is purely inductive and losses are neglected ($\delta^+ = \theta^+ \pm \frac{\pi}{2}$).

TABLE 5.2. NEGATIVE- AND POSITIVE-SEQUENCE QUANTITIES WITH THEIR CORRESPONDING ZERO-SEQUENCE VOLTAGE OR CURRENT

	v^+,θ_v^+	v^-,θ_v^-	i^+,δ_i^+	i^-,δ_i^-	v_0 or i_0
star	V^+,0	0,0	$I^+,\pm\frac{\pi}{2}$	$I^-,\pm\frac{\pi}{2}$	$\frac{A}{\sqrt{3}(I^{-2}-I^{+2})}$
star	V^+,0	0,0	$I^+,\mp\frac{\pi}{2}$	$I^-,\pm\frac{\pi}{2}$	$\frac{A'}{\sqrt{3}(I^{-2}-I^{+2})}$
delta	V^+,0	V^-,0	$I^+,\pm\frac{\pi}{2}$	0,0	$\frac{B}{\sqrt{3}(V^{-2}-V^{+2})}$
delta	V^+,0	V^-,π	$I^+,\pm\frac{\pi}{2}$	0,0	$\frac{B'}{\sqrt{3}(V^{-2}-V^{+2})}$

Table 5.2 summarizes the different sequence components for the considered cases. The corresponding zero-sequence voltage and current are calculated using (5.9) and (5.11). Other parameters in Table 5.2 are defined as follow

$$\begin{aligned} A &= \sqrt{C^2(I^- + I^+)^2 + 12(I^- - I^+)^2 P_{\text{disa}}^2} \\ A' &= \sqrt{C^2(I^- - I^+)^2 + 12(I^- + I^+)^2 P_{\text{disa}}^2} \\ B &= \sqrt{D^2(V^- + V^+)^2 + 12(V^- - V^+)^2 P_{\text{disa}}^2} \\ B' &= \sqrt{D^2(V^- - V^+)^2 + 12(V^- + V^+)^2 P_{\text{disa}}^2} \end{aligned} \tag{5.25}$$

with

$$\begin{aligned} C &= 2P_{\text{disa}} + 4P_{\text{disb}} - \sqrt{3}V^+ I^- \\ D &= 2P_{\text{disa}} + 4P_{\text{disb}} - \sqrt{3}V^- I^+ \end{aligned}$$

The solution for the zero-sequence voltage/current shows that a practical limitation exists in both configurations, with an infinite zero-sequence requirement needed under specific operating conditions. In the specific, the operating range of the star configuration is limited by the degree of unbalance (I^-/I^+). From Table 5.2, it can be observed that V_0 tends to infinity when the ratio I^-/I^+ approaches 1, i.e. a theoretically infinite voltage for the Y-point to allow power distribution among phases when the amplitude of the exchanged negative-sequence current equals the amplitude of the positive-sequence. In practical applications, the maximum attainable output voltage of the converter leg will determine the maximum degree of unbalance that the converter can cope with before losing the controllability of the DC-link voltages. Similar phenomena will appear for the delta configuration, where the operating range is limited by the degree of voltage unbalance (V^-/V^+). From Table 5.2, it can be observed that the zero-sequence current I_0 tends to infinity when the ratio (V^-/V^+) tends to 1. It is of importance to stress that the singularity is independent from the assumptions in Table 5.2 and will occur in any unbalanced condition if the voltage ratio for the delta and the current ratio for the star tends to 1.

Figure 5.9 (a),(c) shows the relation between positive- and negative-sequence currents and zero-sequence voltage amplitude for the star configuration when $\delta^+ = \delta^- = \frac{\pi}{2}$ (a) and $\delta^+ = -\delta^- = \frac{\pi}{2}$ (c). For the simulated case, V^+ is equal to 1 pu, while P_{disa} and P_{disb} are set to 0.02 pu and 0.01 pu, respectively. Observe that P_{disa}, P_{disb} are intentionally chosen to be very small, since

they are just to model the small disturbances caused by non-idealities. It can be observed that in both operating conditions, the singularity occurs when $I^+ = I^-$. It is of interest to observe that more effort is needed from a balancing point of view (i.e., more zero-sequence voltage injection for the same amount of current unbalance) when the current positive- and negative-sequence components have the same phase angle ($\delta^+ = \delta^- = \frac{\pi}{2}$ in Fig. 5.9(a)).

Figure 5.9 (b),(d) shows the relation between positive- and negative-sequence voltages and zero-sequence current amplitude for the delta case when $\theta_v^+ = \theta_v^- = 0$ (b) and when $\theta_v^+ = 0, \theta_v^- = \pi$ (d). For the simulated case, I^+ is equal to 1 pu, while P_{disa}, P_{disb} are 0.02 pu and 0.01 pu, respectively. It can be observed that in both cases the singularity occurs when $V^+ = V^-$. Similar to the star case, more balancing effort is required when $\theta_v^+ = \theta_v^- = 0$.

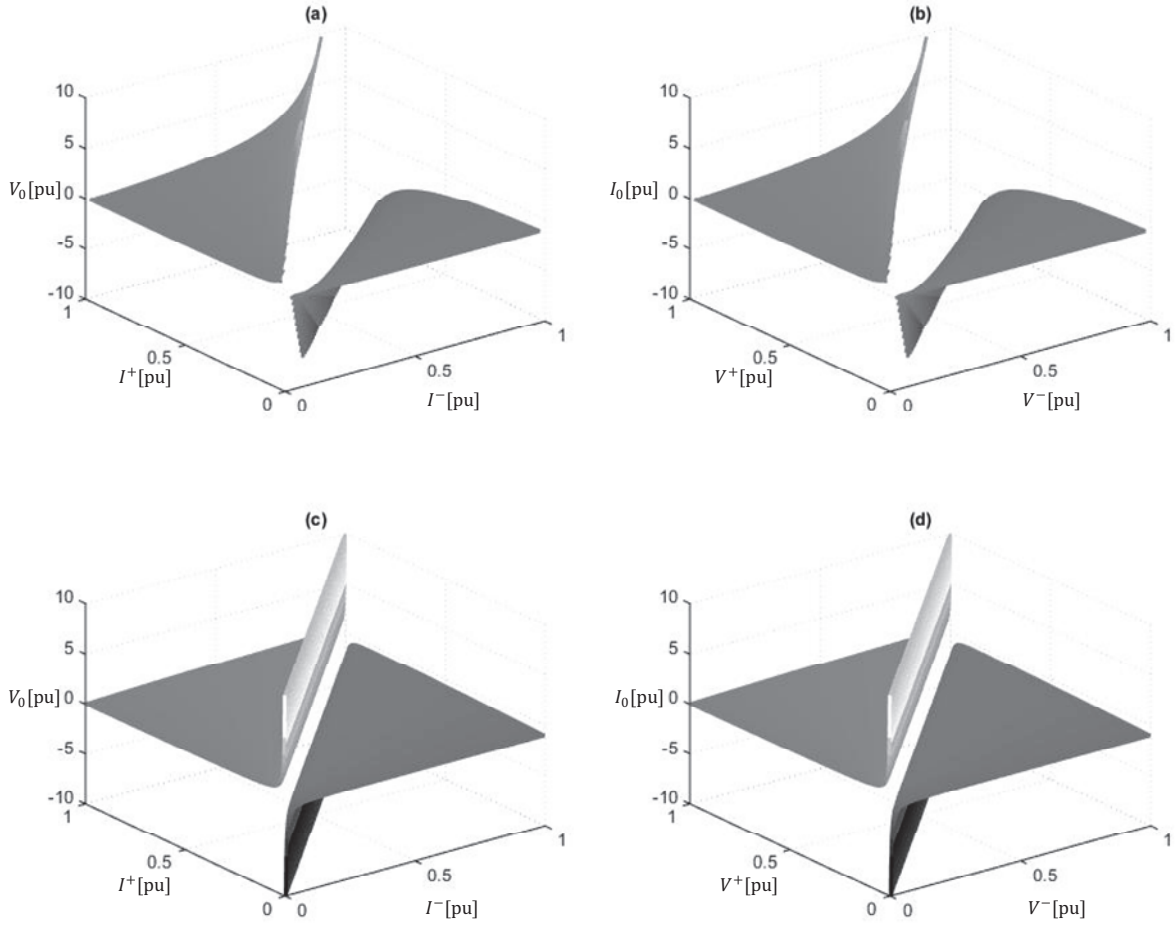


Fig. 5.9 Relationship between zero-sequence voltage/current and negative- and positive-sequence currents/voltages for star/delta configurations; (a): $\delta^+ = \delta^- = \frac{\pi}{2}$; (c): $\delta^+ = -\delta^- = \frac{\pi}{2}$; (b): $\theta_v^+ = \theta_v^- = 0$; (d): $\theta_v^+ = 0, \theta_v^- = \pi$.

It is possible to observe from Fig. 5.9 that although star and delta CHB-STATCOMs are sensitive to the degree of unbalanced in the current and voltage, respectively, the required amount of zero-sequence component needed for capacitor balancing also highly depends on the relative phase shift between the sequence components. For this reason, for the star configuration it is of interest

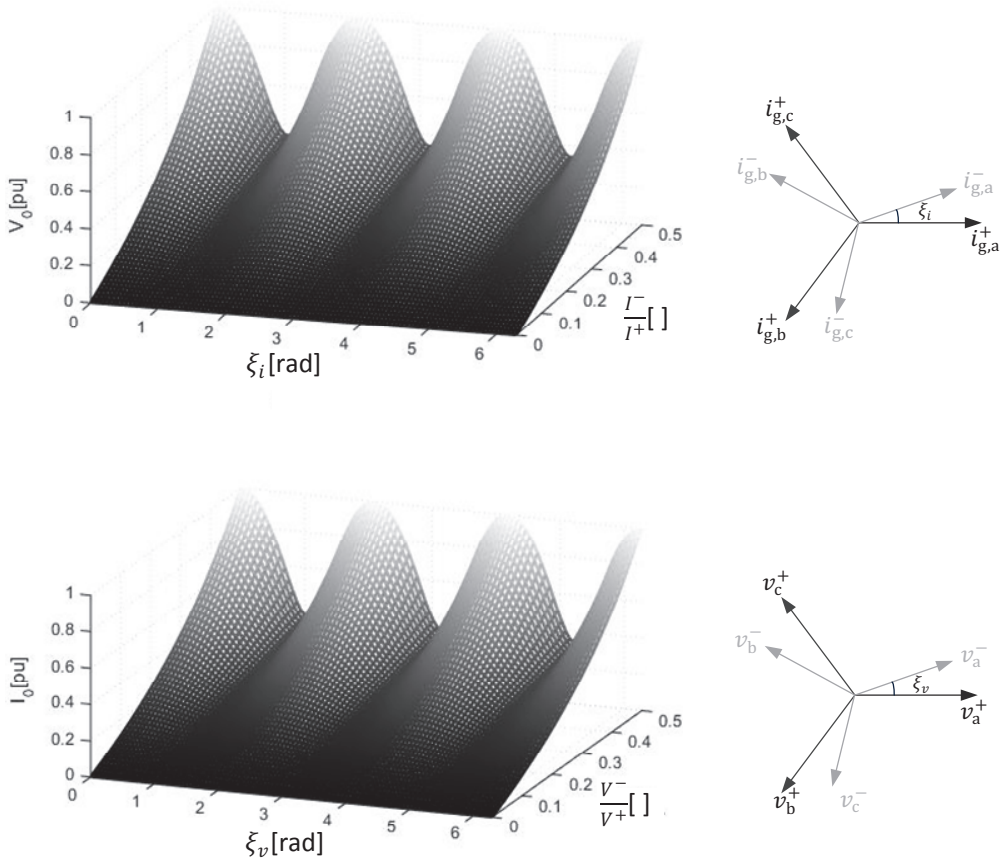


Fig. 5.10 Impact of phase shift between positive- and negative-sequence component on required zero-sequence component. Top: star configuration; bottom: delta configuration.

to investigate the impact of the relative phase shift between the current sequence components on the required amount of zero-sequence voltage. Analogous investigation can be performed for the delta configuration, where the impact of the relative phase shift between positive- and negative-sequence voltage on the required zero-sequence current is investigated.

Figure 5.10, top figure, shows the required zero-sequence voltage as a function of the phase shift between the current sequence components, denoted as ξ_i, and the degree of unbalance in the exchanged current. It is here assumed that the positive-sequence voltage V^+ is equal to 1pu. Similar analysis is performed for the delta configuration (see Fig. 5.10, bottom figure), where the impact of the phase shift between the negative- and the positive-sequence voltage is investigated under the assumption that the converter is injecting 1pu positive-sequence current into the grid. Note that the level of unbalance is limited to 0.5pu for clarity of the figure. As shown, the worst case (i.e., highest demand on the zero-sequence component) occurs when the positive-sequence tern is aligned with the negative-sequence tern (corresponding to $\xi_{i,v} = 0,\ 2\pi/3,\ 4\pi/3$); on the contrary, the lowest demand on the zero-sequence component occurs when the two terns are in phase opposition, i.e. for $\xi_{i,v} = \pi/3,\ \pi,\ 5\pi/3$. Therefore, it can be concluded that the case studies indicated in Table I where both current sequences are in phase for the star configuration (i.e., $\delta^+ = \delta^- = \pm\frac{\pi}{2}$) or when the voltage sequences are in phase for the delta configuration

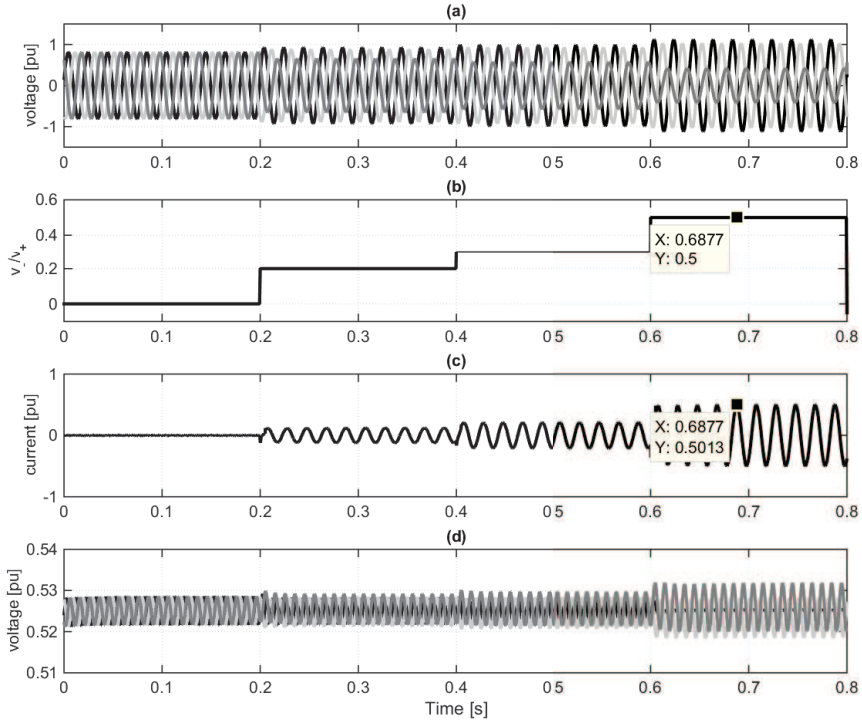


Fig. 5.11 Simulation results of delta configuration; (a): grid voltage; (b): $\frac{v^-}{v^+}$; (c): zero-sequence current; (d): capacitor voltages.

($\theta_v^+ = \theta_v^- = 0$) can be seen as the worst case scenarios under the given assumptions.

In order to verify the theoretical results, simulations are performed for the worst case scenario mentioned in Table 5.2 for both configurations, i.e. $\delta^+ = \delta^- = \pm\frac{\pi}{2}$ for the star and $\theta_{\mathrm{v}}^+ = \theta_{\mathrm{v}}^- = 0$ for the delta.

Figure 5.11 shows the obtained simulation results for the delta configuration. Figure 5.11 (a) shows the grid voltage, figure (b) shows the degree of unbalance in the converter terminal voltage (V^-/V^+), figure (c) shows the zero-sequence current and figure (d) shows the capacitor voltages in all three phases. The positive-sequence current is set to 0.5 pu.

As shown in the figure, an increase in the degree of voltage unbalance (V^-/V^+) leads to an increase of the zero-sequence current amplitude, as expected from the investigation carried out in this section. ($V^-/V^+ = 1$) is the critical point. If the terms P_{disa} and P_{disb} are neglected, the amplitude of the zero-sequence current in Table 5.2 can be simplified to $\frac{I^+V^-}{V^--V^+}$. It can be observed from Fig. 5.11 that, in agreement with the theoretical analysis, for ($V^-/V^+ = 0.5$) the zero-sequence current is about 0.5 pu and equals the amplitude of the positive-sequence current. Observe that an increase in the exchanged positive-sequence current will result in an increase of the zero-sequence current. For example, for the considered level of voltage unbalance, a 1 pu positive-sequence current would lead to a 1 pu circulating current to guarantee capacitor balancing, meaning that the converter must have a current rating equal to 2 pu. The required current rating for the converter will further increase if the voltage unbalance is increased. Finally,

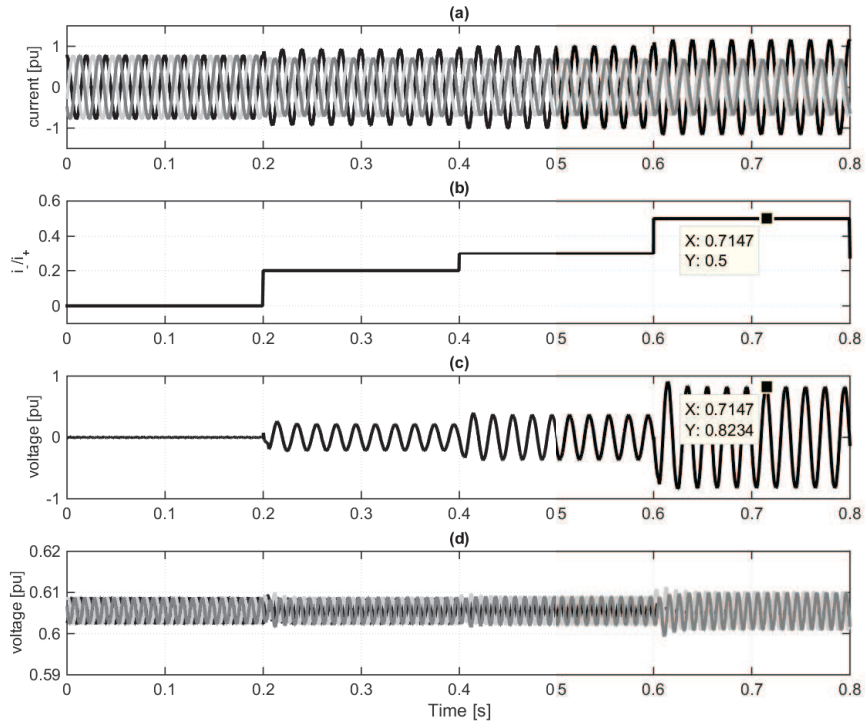


Fig. 5.12 Simulation results of star configuration; (a): line currents; (b): $\frac{I^-}{I^+}$; (c): zero-sequence voltage; (d): capacitor voltages.

Fig. 5.11 (d) clearly shows that the implemented control strategy allows proper DC-capacitor voltage balancing.

Figure 5.12 shows the obtained simulation results for the star configuration. Figure 5.12 (a) shows the line current, figure (b) shows the degree of unbalance in the current injected by the converter ($^{I^-}/_{I^+}$), figure (c) shows the zero-sequence voltage and figure (d) shows the capacitor voltages in all three phases. For this simulation study, the line-to-line grid voltage is set to 1 pu (corresponding to a peak value of 0.8 pu for the line-to-ground voltage) and is perfectly balanced. As expected, an increase in the degree of unbalance in the injected current ($^{I^-}/_{I^+}$) leads to an increase in amplitude of the zero-sequence voltage V_0, with a singularity when ($^{I^-}/_{I^+} = 1$). Note that the implemented controller works properly and is able to keep the capacitor voltages close to the reference value. As for the delta case, neglecting the terms P_{disa} and P_{disb}, from Table 5.2 the amplitude of the zero-sequence voltage can be simplified to $\frac{I^- V^+}{I^- - I^+}$. As it can be observed from Fig. 5.12, in agreement with the theoretical calculations at ($^{I^-}/_{I^+} = 0.5$) a 0.8 pu zero-sequence voltage peak is needed to guarantee capacitor balancing, i.e. a voltage that is equal to the grid voltage. Therefore, for the considered case a 2 pu rating in the converter voltage is needed to cope with the considered case. The required voltage rating will further increase if the current unbalance is increased.

5.6 Discussion

Both theoretical and simulation results provided in this chapter show that under unbalanced conditions there is a limit in the operating range of the CHB-STATCOM, both in star and delta configuration. The star configuration is sensitive to the degree of unbalance in the injected current, while the delta is sensitive to the degree of unbalance in the voltage at the converter terminals. This, together with the specific application, will dictate the selection of the suitable configuration for the CHB-STATCOM and its ratings.

The CHB-STATCOM is mainly used either for utility or industrial applications. Typically, the role of the compensator in utility applications is to regulate the grid voltage at the connection point by aim of positive-sequence current injection. Therefore, for this kind of applications the degree of unbalance in the injected current can be typically considered low, making the star configuration a suitable choice, especially when considering its reduced voltage ratings (thus, reduced number of required cascaded cells) as compared with the delta configuration.

When a STATCOM is employed for industrial applications, instead, its aim is mainly to improve the power quality at the end-user interface, for example to mitigate flicker caused by arc-furnace load. Under this scenario the compensator must be able to exchange both negative- and positive-sequence currents with the grid and the delta configuration appears as the most preferable choice, especially for systems connected to relatively strong grids. However, it is of importance to stress that this configuration would still suffer from high zero-sequence current requirements in case of asymmetrical faults located in the vicinity of the grid connection point.

5.7 Conclusions

In this chapter, the effect of unbalanced voltage and current on CHB-STATCOM has been investigated, both in case of star and delta configuration of the converter phase legs. Zero-sequence voltage (for the star configuration) or current (delta) allows to maintain the DC-link voltage of the different cells balanced in case of unbalanced operation. However, it has been shown that there are special operating conditions for both the star and the delta configuration where the zero-sequence component is unable to control the active power in each phase to zero. This is due to a singularity that exists in the solution for the calculation of the zero-sequence components. The singularity in the delta configuration occurs when the positive- and negative-sequence components of the voltage at the converter terminals are equal, while for the star case it is governed by the equality between the positive- and the negative-sequence component of the injected current. In addition to the amplitudes, the phase angles of currents in star and voltage in delta will highly impact the sensitivity of the converter. For the star configuration, the highest demand on the zero-sequence voltage occurs when the three-phase positive-sequence currents are aligned with the negative-sequence tern; on the contrary, the lowest demand on the zero-sequence component occurs when the two terns are in phase opposition. Analogue results hold for the delta case. In utility applications, where the priority is on voltage regulation, the converter aims to prioritize positive-sequence current injection to boost the voltage at the connection point and at the same time improve the degree of unbalance. Therefore, the star configuration can be utilized

for this purpose. In industrial application, such as arc furnaces, the converter aims to exchange both positive- and negative-sequence current; being this kind of loads typically connected to relatively strong grids, the delta configuration appears the most preferable choice for this kind of applications.

Chapter 6

Laboratory setup

6.1 Introduction

To validate the results obtained via simulation for the CHB-STATCOMs, the controllers have been tested experimentally in the Power System Laboratory at the Division of Electric Power Engineering of Chalmers University of Technology. In this chapter, a description of the laboratory setup and of the components used will be given. Then, obtained experimental results will be presented.

6.2 Laboratory setup

The block diagram of the experimental setup is given in Fig. 6.1. Each phase of the converter consists of three H-bridge cells and a filter. All three phases are connected to a delta/star switch, used to easily connect the phases either in star or in delta configuration. The converter is connected to an electronic AC-source that acts as the grid.

A measurement box measures the line currents and grid phase voltages and sends the signals to the analogue input of the controller. The DC-link voltage of each cell is measured within the corresponding cell as a digital signal and is sent to the digital input of the controller via optical fibers. The controller provides the appropriated pulses for each cell and sends the pulses to the corresponding cell via optical fibers. A figure of the actual laboratory setup is reported in Fig. 6.2.

In this laboratory setup the converter is connected to a California Instrument 4500LX programmable AC power source/analyzer. With this device it is possible to provide a three-phase voltage with controllable amplitude and frequency. Control ability over the voltage amplitude makes the start-up process much simpler since no start-up resistors and relays are needed to limit the inrush current. All DC capacitors can be precharged slowly by gently increasing the amplitude of the AC-source voltage.

The cell boards used for this laboratory setup have been built in cooperation with Aalborg Uni-

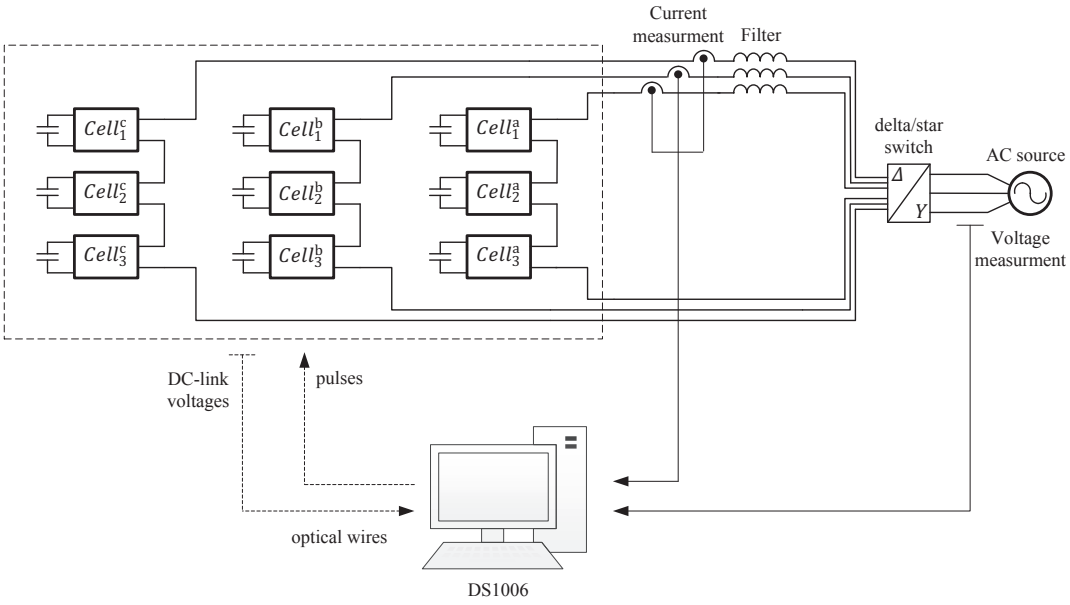


Fig. 6.1 Block diagram of the laboratory setup.

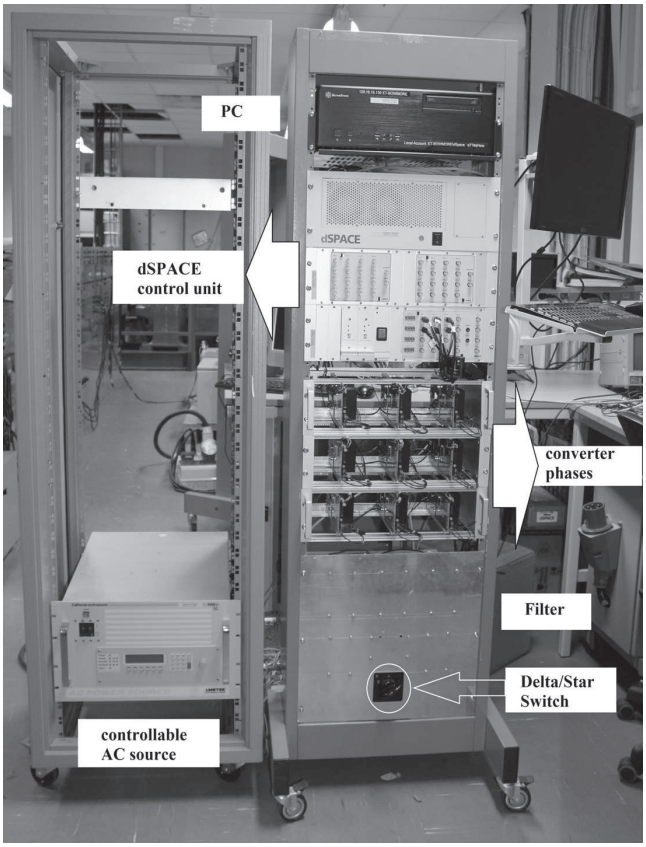


Fig. 6.2 Picture of the laboratory setup.

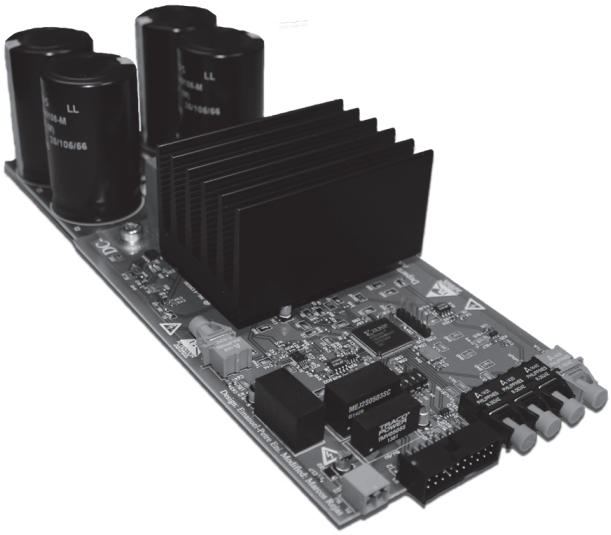


Fig. 6.3 Picture of the cell board with DC-link capacitors.

versity, Denmark. These cells are constituted by a three-phase two-level converter PSS15S92F6-AG/PSS15S92E6-AG [91], of which only two legs are used. The DC-link consists of four 1 mF capacitors connected in parallel. The DC-link voltage is measured within the cell board and sent to the controller via optical fibers. These boards have over/under voltage and over current protections. Moreover, these boards provides a 2μs hardware blanking time for the switching signals. The boards are also equipped with a thermal sensors for the semiconductors temperature. The data of the cell boards are reported in Table 6.1. Figure 6.3 shows one cell board as an example.

TABLE 6.1. DATA FOR CELLS.

rated voltage	400 V
rated current	8 A
DC-link capacitor	4 mF

The control computer system consists of a PC with a DS1006 processor board. The DS1006 can be programmed using C-code or using Matlab/Simulink. Together with the processor board, a DS2004 analogue to digital board for the analog input signals and a DS4004 for digital input signals are used. To generate pulse patterns, a DS5101 Digital Waveform Output Board is used. The DS5101 autonomously generates any TTL pulse patterns on up to 16 channels with high accuracy. Since the required number of channels for this laboratory setup is more than 16, two DS5101 boards are used and synchronized. The outputs of these boards are the firing pulses which are sent to each cell via optical fibers. Interrupts signals as well as board synchronization are generated through DWO programming.

6.3 Experimental results under balanced conditions

6.3.1 Dynamic performances of CHB-STATCOMs

A downscale version of the same model as described in Table 3.1 has been verified by experimental results. The system and control parameters for these experimental results are summarized in Table 6.2.

TABLE 6.2. SYSTEM AND CONTROL PARAMETERS FOR THE EXPERIMENTAL SET-UP

Parameters	values
Rated power S_b	1.5 kVA,1 pu
Rated voltage V_b	173.2 V,1 pu
System frequency f_s	50 Hz
Filter inductor L_f	15 mH,0.23 pu
Filter resistor R_f	1.4 Ω,0.07 pu
Cells capacitor C	4 mF,0.04 pu
DC-link voltage for star V_{DC}	62 V,0.36 pu
DC-link voltage for delta V_{DC}	106 V,0.61 pu
Cell numbers n	3
Carrier frequency f_{cr}	1000 Hz for PS-PWM and 3000 Hz for sorting algorithm
Inner loop control band width α_i	$2\pi \times 500$ rad/sec
Outer loop control band width α_{cl}	$2\pi \times 5$ rad/sec
Individual DC-link loop control band width α_{ind}	$2\pi \times 1$ rad/sec (only for PS-PWM)
PLL band width α_{PLL}	$2\pi \times 5$ rad/sec
DC-link filter band width α_{DC}	$2\pi \times 50$ rad/sec

Figure 6.4 shows the experimental results for the star connected CHB-STATCOM. The figures on the left side are the experimental results when sorting algorithm is used and the figures on the right side are the experimental results when PS-PWM is used. Figure 6.4 (a),(e) show the DC-link voltages in all three phases, Fig. 6.4 (b),(f) show the reference and actual q-component of the current, Fig. 6.4 (c),(g) show three phase currents and Fig. 6.4 (d),(h) show the phase a voltage at the converter terminals. It can be observed from these experimental results that the controller is able to track the reference current and at the same time control all the DC-link voltages at the reference value.

One practical issue regarding the CHB-STATCOMs is the forward voltage drop over diodes and switches. The effect of this voltage drop can be seen in Fig. 6.4 (d),(h). It can be observed that there is an asymmetry in both positive and negative peak of the voltage waveform. The reason is that at both positive and negative peak of the voltage, the current sign is changed from positive to negative or vice versa, due to 90^0 phase shift between the voltage and current in each phase. At this point the current path is changed from diodes to IGBTs or vice versa. Figure 6.5 shows the current path and cell output voltage for positive and negative currents and when the voltage reference is positive. V_D is the diode forward voltage drop, V_S is the switch forward voltage

drop, V_{dc} is the DC-link voltage and V_{out} is the cell output voltage. It can be seen that the output voltage of the cell is changed once the current direction changes.

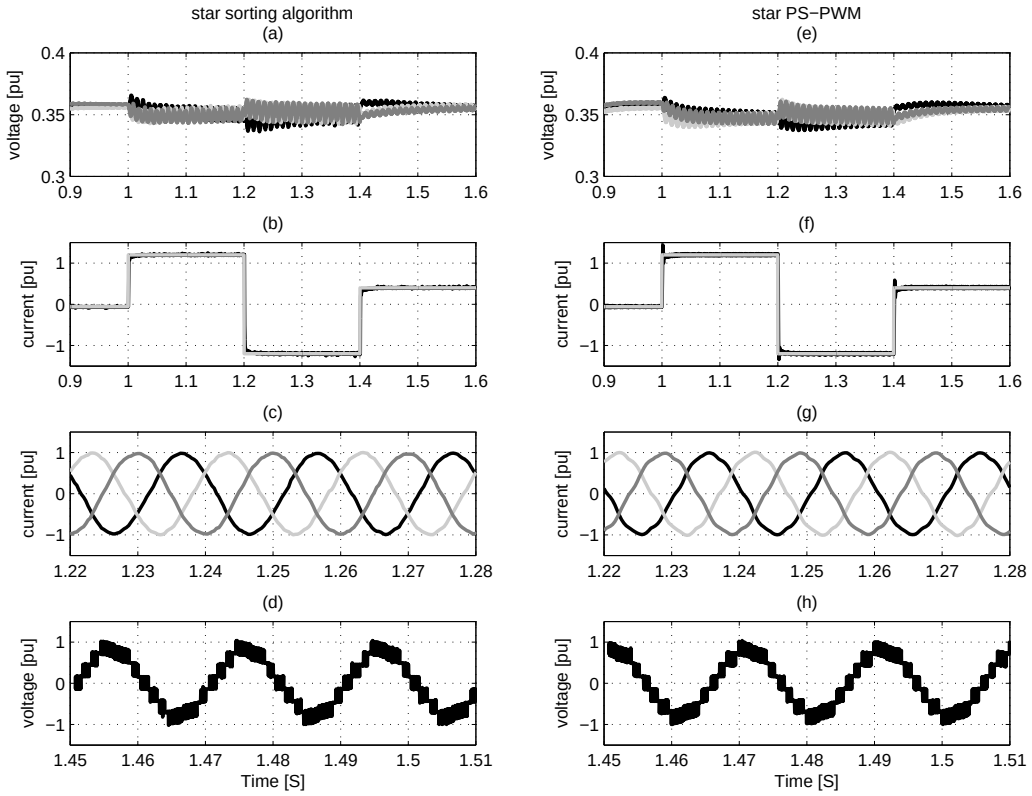


Fig. 6.4 Experimental results of the star configuration. (a,e) DC-link voltage of all the cells, (b,f) reference and actual q-current, (c,g) three-phase line currents, (d,h) converter output voltage of phase a. Figures on the left side are with sorting algorithm and figures on the right side are with PS-PWM.

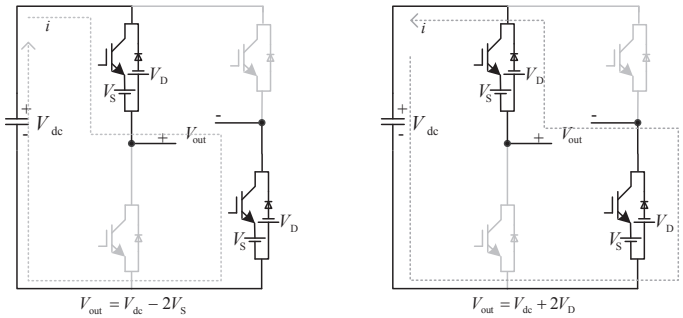


Fig. 6.5 Current path and cell output voltage.

Figure 6.6 shows the transient performance of the star configuration with and without Smith predictor for both simulation and experimental results including the forward voltage drop of semiconductors in the simulation model. The figures on the left side shows the results when

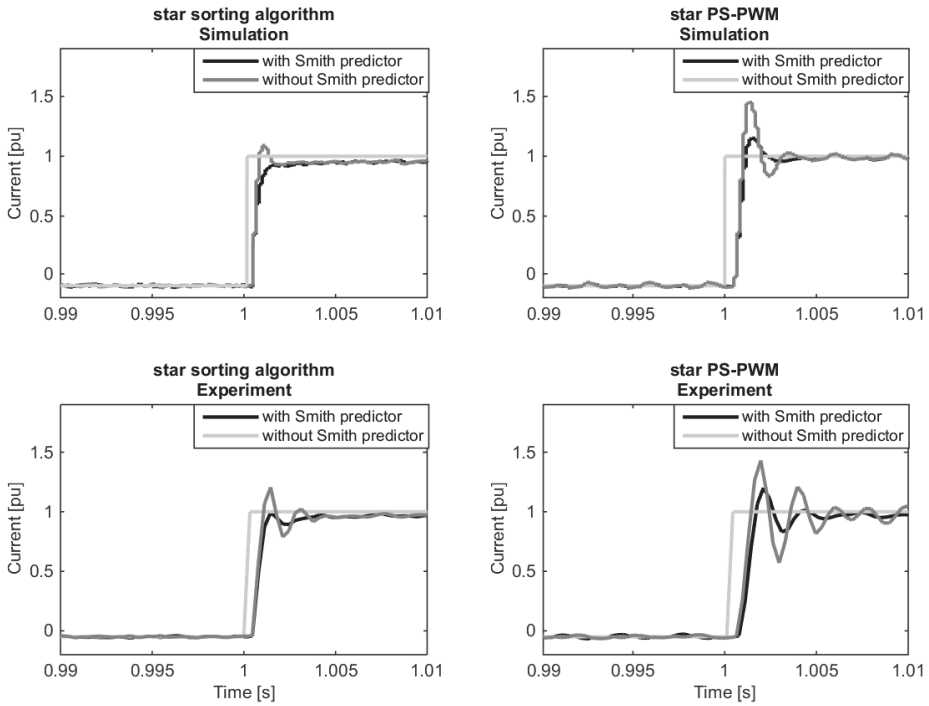


Fig. 6.6 Transient performance of the star configuration (left side are with sorting and right side are with PS-PWM) with and without Smith predictor. Figures on top are simulation and on bottom are experimental results.

sorting algorithm is used (simulations are on top and experimental are on bottom) the figures on the right side shows the results when PS-PWM is used (simulations are on top and experimental are on bottom). It can be observed that in all cases Smith predictor improves the transient performance of the converter. Note that the asynchronous technique has been used in the implementation of the PS-PWM for updating the modulation indexes of each cell. It can also be observed that there is a close similarity between the simulation and experimental results from the rise time and overshoot points of view. However, the experimental results show less damping in the oscillations during the transient. This mismatch between simulation and experimental results is mainly due to the dynamic behavior of the programmable AC power supply utilized in the laboratory setup; the voltage controller of the supply together with its filtering stage that has not been taken into account in the simulation model, where the CHB-STATCOM is assumed to be connected to an infinite bus.

In order to further investigate the effect of semiconductors voltage drop on the CHB-STATCOMs performance, star configuration with the sorting algorithm is chosen as the case study. Figure 6.7 shows the simulation results of the converter output voltage for phase *a* and its corresponding harmonic spectra. The top plot shows the results when the voltage drop over the semiconductors is set to zero. It can be observed that the voltage waveform is symmetrical and no low-order harmonic is generated in the output voltage. The bottom plot shows the results when the forward voltage drop of diodes and switches are set to 2 V. The asymmetrical shapes at the positive and negative peak of the voltage introduces low-order harmonics in the output voltage.

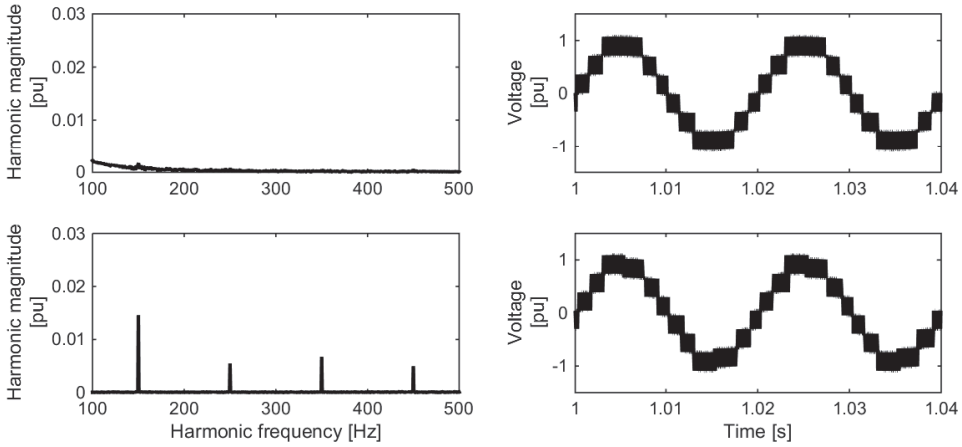


Fig. 6.7 Converter phase voltage and its corresponding harmonic spectra; (top):without forward voltage drop; (bottom):with voltage drop over semiconductors.

The third-order harmonic, which is the largest harmonic generated, does not affect the current in the star configuration since the third order harmonic is eliminated in the line-to-line voltage. However, in the delta configuration, the third-order voltage harmonic causes a third-order current harmonic that circulates inside the delta and negatively impacts the active power distribution among phases. This can be considered as a large disturbance for the cluster controller in balancing the cluster voltages.

In order to show the effect of the forward voltage drop on the cluster voltage in case of delta, the delta configuration is simulated with and without considering the forward voltage drop and the results are shown in Fig. 6.8. The figures on the left side are the simulation results of the cluster voltages (a), circulating current inside delta (b) and three-phase line currents (c) when 2 V forward voltage drop over the semiconductors is considered. The figures on the right side show the same simulation results without considering any forward voltage drop. It can be observed from the obtained results that the forward voltage drop can have a severe effect on the cluster voltages.

To overcome this problem, the circulating current resulting from the forward voltage drop should be controlled to zero. A simple P controller is chosen in this laboratory setup to control this circulating current to zero. This controller superposes a zero-sequence voltage to the reference voltages of each phase to produce a circulating current in opposite direction of the actual circulating current. This will eventually bring the total circulating current to zero. Following equation describes the circulating current controller:

$$V_{\mathrm{o}\Delta\mathrm{d}} = k_{\mathrm{o}\Delta\mathrm{d}} \left(\frac{i_{\mathrm{a}\Delta} + i_{\mathrm{b}\Delta} + i_{\mathrm{c}\Delta}}{3} \right) \tag{6.1}$$

where $V_{\mathrm{o}\Delta\mathrm{d}}$ is the zero-sequence voltage correspond to the required zero sequence current, $k_{\mathrm{o}\Delta\mathrm{d}}$ is the proportional gain and $i_{\mathrm{a}\Delta}$,$i_{\mathrm{b}\Delta}$,$i_{\mathrm{c}\Delta}$ are the three phase branch currents inside the delta.

Figure 6.9 shows the obtained experimental results of the delta configuration. Note that the only difference between the controller here and the controller explained in Chapter 3 is the extra

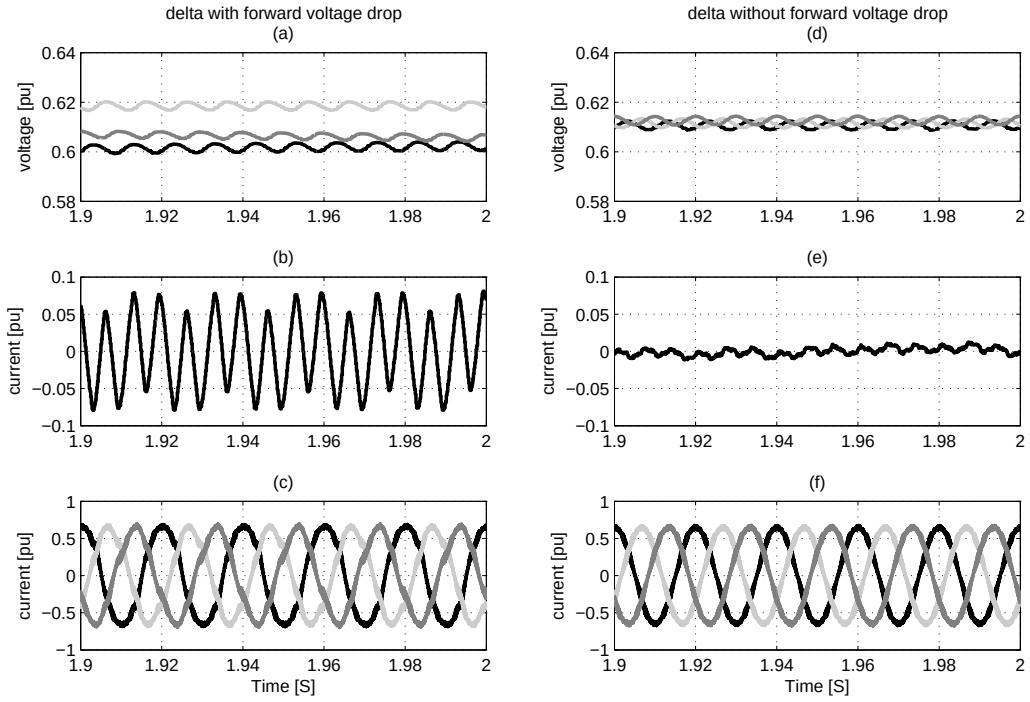


Fig. 6.8 Simulation results of the delta configuration with and without forward voltage drop over semiconductors; (top): cluster voltages; (middle): circulating current; (bottom) three-phase line currents.

circulating current controller in (6.1). The figures on the left side are the experimental results when sorting algorithm is used and the figures on the right side are the experimental results when PS-PWM is used. Figure 6.9 (a),(f) show the DC-link voltages in all three phases, Fig. 6.4 (b),(g) show the reference and actual q-component of the current, Fig. 6.9 (c),(h) show three phase currents, Fig. 6.9 (d),(i) show the phase a voltage of the converter and Fig. 6.9 (e),(j) show the circulating current inside delta. It can be seen that the circulating current controller is able to keep the circulating current close to zero and thus the converter is able to provide appropriate operation. Observe from Fig. 6.9 (a) and (f) that the cluster voltages are not exactly equal; this is due to the fact that the circulating current controller is based on a proportional controller only and therefore it is unable to set the steady-state error to zero. However, the controller will avoid the drifting of the DC-link voltages and keep the clusters close to their reference values, thus allowing proper operation of the system.

Figure 6.10 shows the transient performance of the delta configuration with and without Smith predictor for both simulation and experimental results. The figures on the left side shows the results when sorting algorithm is used (simulations are on top and experimental are on bottom) the figures on the right side shows the results when PS-PWM is used (simulations are on top and experimental are on bottom). Again, asynchronous technique has been used for the implementation of the PS-PWM. It can be observed that there is a close similarity between the simulation and experimental results from the rise time and overshoot points of view. However, the Smith predictor seems to be more effective in the experimental than the simulation results for the delta configuration. This can be due to fact the experimental set-up has more damping terms than the

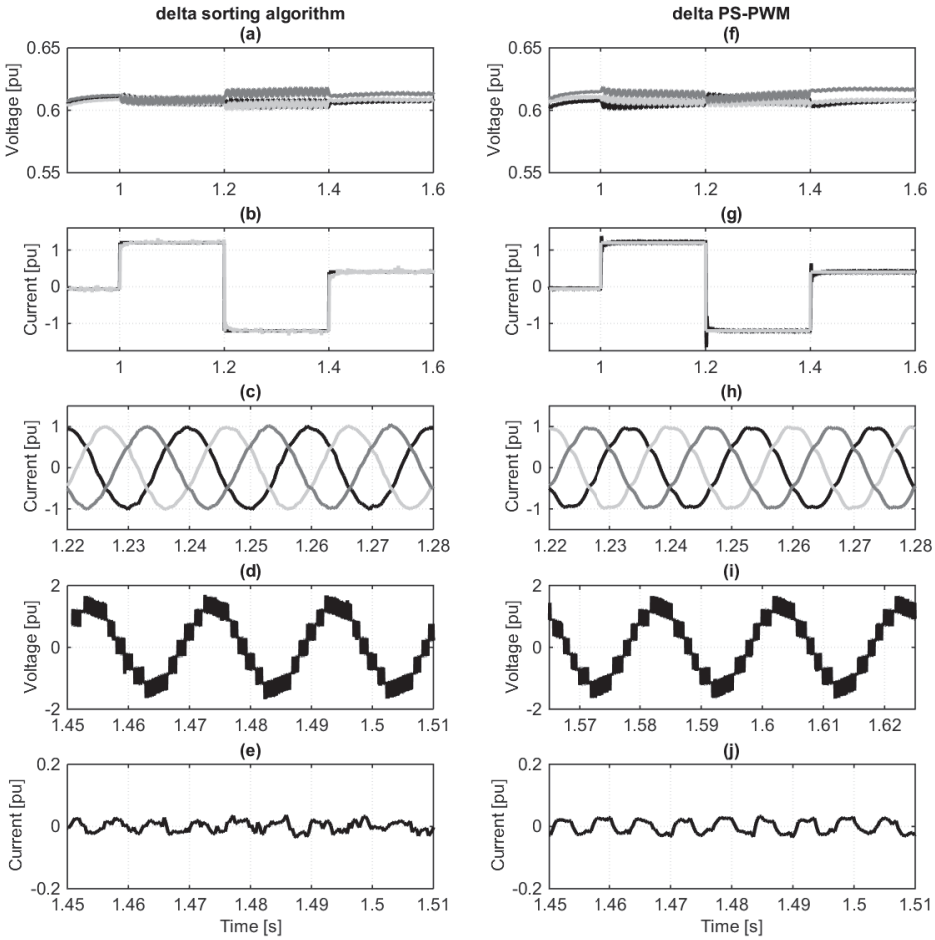


Fig. 6.9 Experimental results of the delta configuration. (a,f) DC-link voltage of all the cells, (b,g) reference and actual *q*-current, (c,h) three-phase line currents, (d,i) converter output voltage of phase *a*, (e,j) circulating current. Figures on the left side are with sorting algorithm and figures on the right side are with PS-PWM.

simulation model, which in turn provides better control over the circulating current specially during the transients.

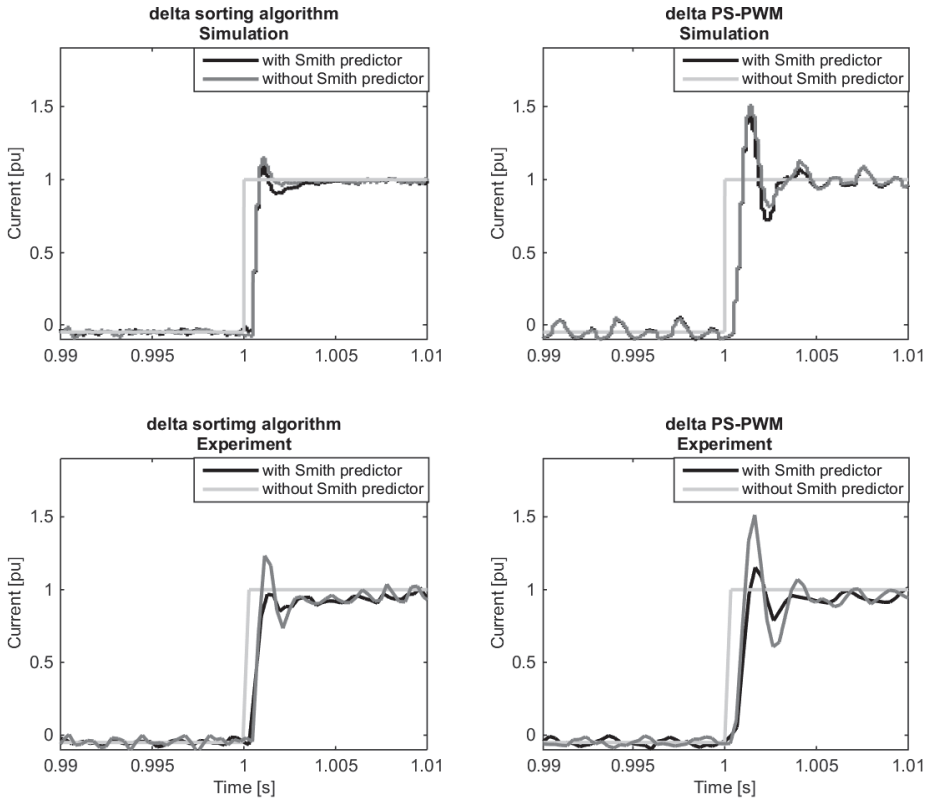


Fig. 6.10 Transient performance of the delta configuration (left side are with sorting and right side are with PS-PWM) with and without Smith predictor. Figures on top are simulation and on bottom are experimental results.

6.3.2 Integer versus non-integer carrier frequency modulation ratio

In order to validate the results regarding the use of a non-integer frequency modulation ratio, the star configuration with PS-PWM is experimentally tested with the same frequency modulation ratios used in Section 4.2.4. As shown in Section 4.2.3, the optimum carrier frequency that leads to the least divergence in the DC-link voltages with three cells per phase is 1016.6 Hz when using 1000 Hz as the integer carrier frequency. Figure 6.11 shows the filtered DC-link voltages for the cells in phase a with different carrier frequencies of 1000 Hz (a), 1008.3 Hz (b), 1016.6 Hz (c) and 1025 Hz (d). At $t = 0.5$ s the individual voltage controller is inhibited and at $t = 4.5$ s it is activated again. It can be observed that the least divergence occurs when carrier frequency of 1016.6 Hz is chosen, confirming the theoretical investigation.

Figure 6.12 shows the output of the individual DC-link voltage controllers for phase a when different carrier frequencies are employed. Note that the individual DC-link voltage control puts less effort in balancing the DC-link voltages in case of non-integer carrier frequency ratio, with minimum action when carrier frequency of 1016.6 is selected. This figure shows how

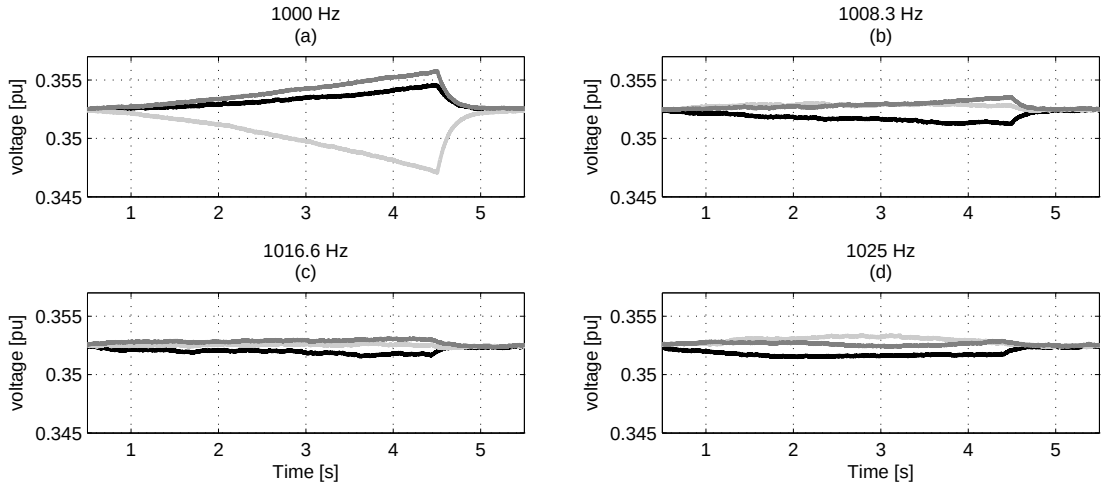


Fig. 6.11 Filtered DC-link voltages of phase *a* with different carrier frequencies and inhibited individual voltage balancing.

the non-integer carrier frequency ratio can alleviate the role of individual balancing controller, although this control loop is still necessary when this kind of modulation strategy is adopted.

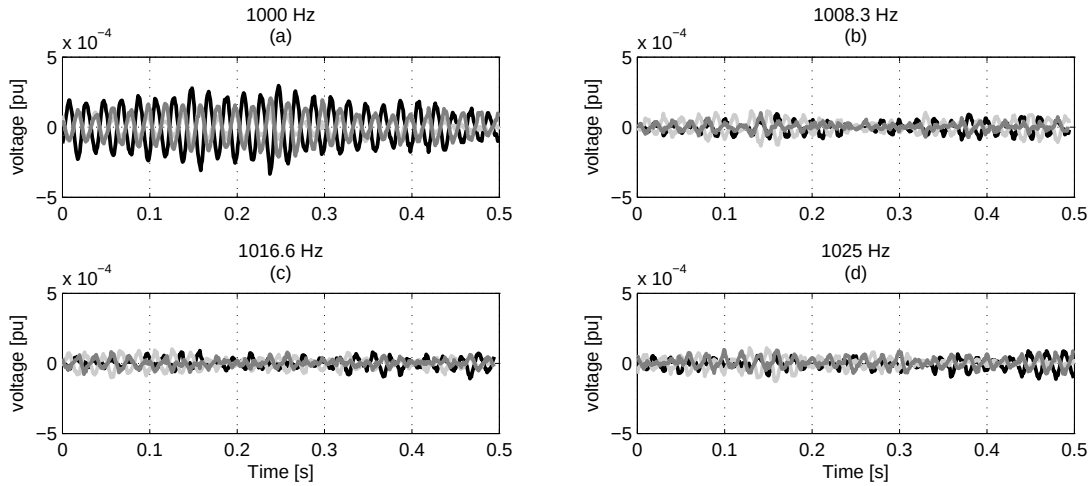


Fig. 6.12 Output of the individual DC-link voltage control for the DC-links in phase *a* of the star configuration at different carrier frequencies.

6.3.3 DC-link voltage modulation technique and zero-current mode

In Chapter 4, two methods for the individual capacitor balancing when the CHB-STATCOM is operated at zero-current mode have been presented and investigated: the first method is based on a modified sorting algorithm, while the second is based on the application of a modulation signal to the DC voltage reference. However, as mentioned in the chapter, the first method presents some limitations and can only be adopted when the RMS current is lower than the

current ripple. For this reason, only the experimental results for the DC-link voltage modulation technique will be presented.

This technique has been implimented in the laboratory for the star configuration with the system parameters reported in Table 6.2. Based on the system parameters, the maximum required DC-link voltage is equal as 0.354 pu. The required DC-link voltage for the zero-current mode is equal to 0.271 pu. Therefore, to keep the oscillations of the DC-link voltage between 0.271 and 0.354 pu, $v^*_{\mathrm{dc},0}$ and v in (4.28) are chosen to be 0.312 and 0.0006 pu. 5 Hz is selected for the frequency of the DC-link voltage oscillations.

$$v^*_{\mathrm{dc}}[\mathrm{pu}] = \begin{cases} 0.312 + 0.0006\cos(2\pi 5t) & i^*_{\mathrm{q}} = 0 \\ 0.354 & i^*_{\mathrm{q}} \neq 0 \end{cases} \tag{6.2}$$

Figure 6.13 shows the obtained experimental results. The top plot shows the reference and actual reactive component of the current. The plot in the middle shows the DC-link voltages in phase *a* when the measured currents are used in the sorting algorithm and bottom plot shows the experimental results when the estimated currents are used instead. The reactive current is set to 1 pu until $t = 1.5$ s and is then set to zero from $t = 1.5$ s to $t = 7.5$ s and to -1 pu from $t = 7.5$ s to $t = 8.5$ s. It can be observed that when the converter starts to operate at zero-current mode, the DC-link voltage modulation technique is activated. It can also be observed that the sorting algorithm provides a proper balancing when estimated current are used while it fails when using the measured currents, confirming the simulation results in Section 4.4.5.

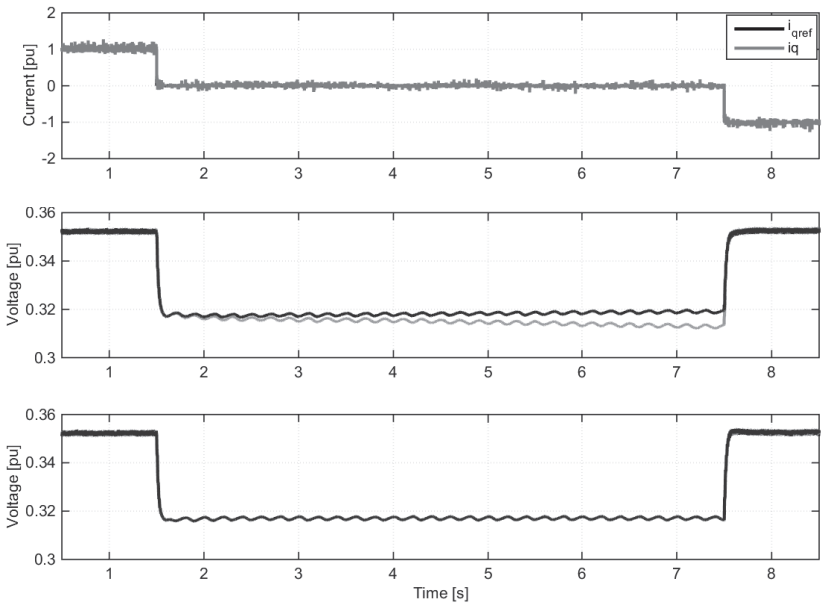


Fig. 6.13 Experimental results of the DC-link voltages at zero-current mode using DC-link modulation technique; top: Reactive component of the current; middle: DC-link voltages in phase *a* by using the measured currents in the sorting algorithm; bottom: DC-link voltages in phase *a* by using the estimated currents in the sorting algorithm.

Observe that individual balancing is obtained with a very small value of the amplitude of the oscillations. These oscillations will have no impact on the grid voltage.

6.4 Experimental results under unbalanced conditions

The control method presented in Chapter 5 is verified for both star and delta configurations with the control parameters of Table 6.3. System and other control parameters are the same as in Table 6.2.

TABLE 6.3. CONTROL PARAMETERS FOR UNBALANCED CONDITIONS (EXPERIMENTAL SET UP).

Parameters	values
Closed loop DVCC control band width α_{i}	$2\pi \times 500$ rad/sec
Closed loop overall DC-link control band width α_{ov}	$2\pi \times 10$ rad/sec
Closed loop cluster control band width α_{z},α_{zd},α_{zs}	$2\pi \times 10$ rad/sec
Zero-sequence current gain K_{io}	30

Figure 6.14 shows the experimental results of star and delta under unbalanced conditions. The grid voltage is balanced and the converter exchanges both positive- and negative-sequence reactive current with the grid. The figures on the left side are the results for the star and the figures on the right side are the results for the delta. All figures shows the results in per unit. Figures (a),(e) show the cluster voltages, figures (b),(f) show the positive-sequence and (c),(g) show negative-sequence currents and figures (d),(h) show the zero-sequence voltage and zero-sequence currents respectively.

Until $t = 1$ s both positive- and negative-sequence currents are set to zero. At $t = 1$ s a step change to one per unit in positive-sequence current is applied and at $t = 1.2$ s a step change to 0.1 per unit is applied in negative-sequence current. It can be observed that before applying the negative-sequence current very small zero-sequence voltage or current is needed to keep the cluster voltage balanced, since the different active power between the phases is small. After applying the negative-sequence current, more zero-sequence voltage or current is required to cancel out the effect of the different average active power between the phases.

It was shown previously under balanced condition that forward voltage drop over semiconductors produces a third order current harmonic inside the delta that impact the active power distribution. The same problem still exists for the unbalanced conditions, but since the controller for the unbalanced conditions already controls the circulating current, it automatically covers the third harmonic cancellation. Perfect cluster voltage balancing shows the ability of both zero-sequence voltage and current in providing an even power distribution between the phases. In order to highlight this ability at $t = 1.4$ s to $t = 1.6$ s both zero-sequence voltage and current controller are disabled. It can be observed that once these controllers are disabled the cluster voltages diverge, which the reactivation of the controllers brings back the cluster voltages to the set point.

Following the simulation results obtained in Fig. 5.11 in Chapter 5, Fig. 6.15 shows the obtained experimental results for the delta configuration. Figure 6.15 (a) shows the grid voltage, figure (b) shows the degree of unbalance in the converter terminal voltage (V^-/V^+), figure (c) shows the zero-sequence current and figure (d) shows the capacitor voltages in all three phases. All quantities are plotted in per unit. The positive-sequence current is set to 0.5 pu. It can be observed that the experimental results well match to the obtained simulation results in Chapter 5

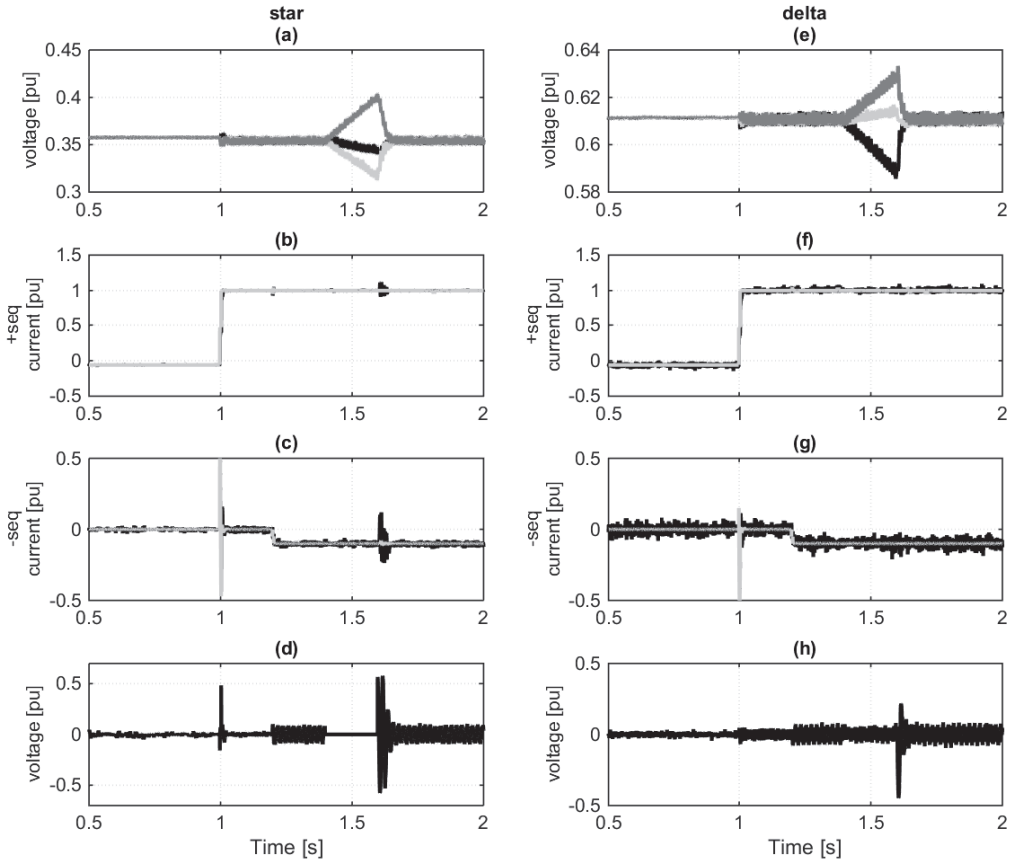


Fig. 6.14 Experimental results of the star (left side) and the delta (right side) configurations. (a,e) DC-link voltage of all the cells, (b,f) reference and actual positive-sequence *q*-current, (c,g) reference and actual negative-sequence *q*-current, (d) zero-sequence voltage, (h) zero-sequence current.

for the delta configuration.

Following the simulation results obtained in Fig. 5.12 in Chapter 5, Fig. 6.16 shows the obtained experimental results for the star configuration. Figure 6.16 (a) shows the line current, figure (b) shows the degree of unbalance in the current injected by the converter (I^-/I^+), figure (c) shows the zero-sequence voltage and figure (d) shows the capacitor voltages in all three phases. For this experimental study, the grid voltage is set to 1 pu (corresponding to a peak value of 0.8 pu for the line-to-ground voltage). Again, good match between simulation and experimental results is obtained.

6.5 Conclusions

This chapter is dedicated to the experimental results that covers the major part of the theoretical and simulation studies of the thesis. The laboratory setup used for this experiment is introduced. The effect of different practical issues such as one-sample intrinsic delay in the digital

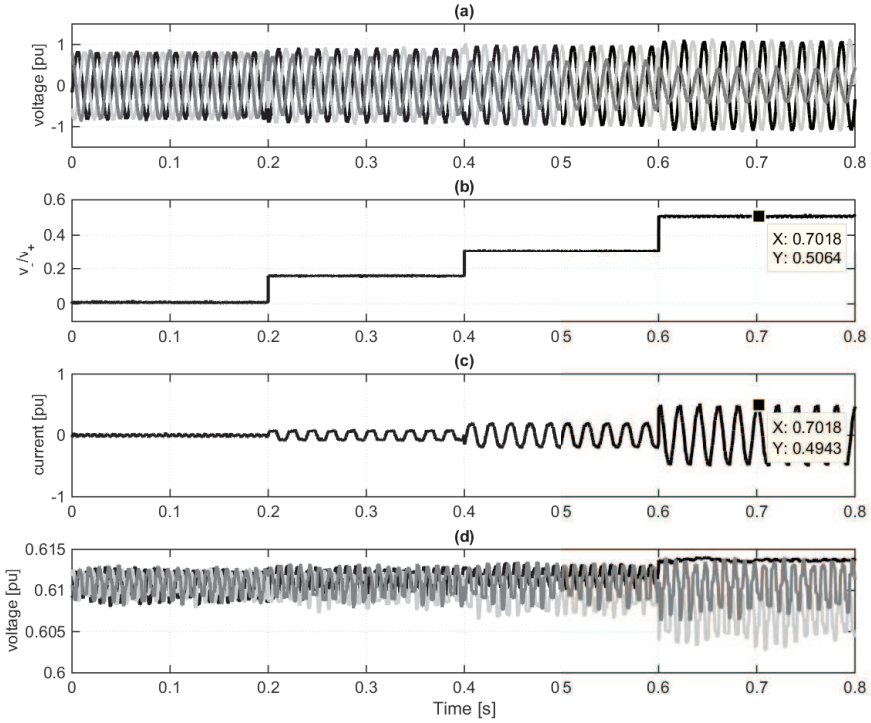


Fig. 6.15 Experimental results of the delta configuration; (a): grid voltage; (b): $\frac{V^-}{V^+}$; (c): zero-sequence current; (d): capacitor voltages.

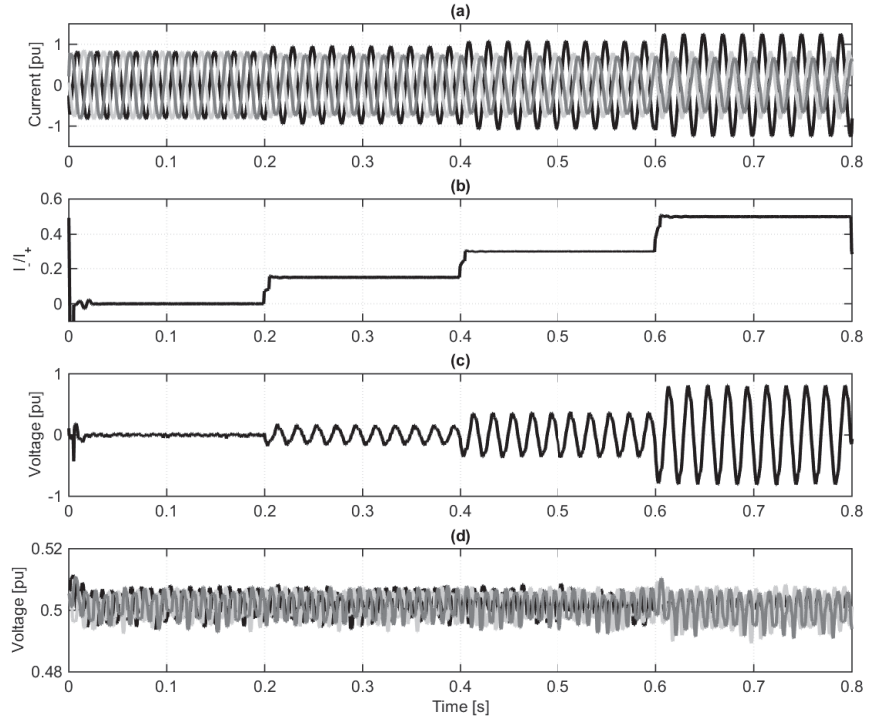


Fig. 6.16 Experimental results of the star configuration; (a): line currents; (b): $\frac{I^-}{I^+}$; (c): zero-sequence voltage; (d): capacitor voltages.

controller and forward voltage drop over semiconductor are shown. The close similarity between the experimental results in this chapter and theoretical and simulation studies of previous chapters proves the validity of the theoretical studies in this thesis.

Chapter 7

Conclusions and future work

7.1 Conclusions

This thesis has dealt with the control and modulation of Cascaded H-Bridge (CHB) converters for STATCOM applications. With focus on the star and delta connection of the phase legs that constitute the converter, the system performance under balanced and unbalanced operation have been investigated, trying to highlight the advantages but also the challenges and possible pitfalls that this kind of topology presents for STATCOM applications.

After an introductory overview of the main multilevel converter topologies that are available in today's market, the overall control structure for the CHB-STATCOM has been described in Chapter 3. Guidelines for tuning of the different control loops have been presented and the dynamic performance of the system has been tested through simulations. It has been highlighted that in actual implementations, due to the unavoidable deviations from ideal conditions, the Phase-Shifted Pulse Width Modulation (PS-PWM) technique suffers from a non-uniform power distribution among the different cells that constitute the phase legs of the converter, leading to the need for additional control loops to guarantee that the different DC-capacitor voltages do not diverge from the reference value. The analysis of this phenomenon is carried out in Chapter 4, where it has been shown that the non-uniform active power distribution is due to the interaction between the carrier side-band harmonics of the cell voltage and the base-band harmonics of the current (when low-switching frequency for the individual cells is selected), as well as poor cancellation of the carrier side-band harmonics (mainly in case of high-switching frequency selection). Theoretical analysis shows that by proper selection of the frequency modulation ratio, a more even power distribution among the different cells of the same phase leg can be achieved. This selection allows to alleviate the stabilization action required from the individual balancing controller and thereby to enhance the overall system stability. Another technique for the individual DC-link voltage balancing discussed in Chapter 4 is the cells sorting algorithm. However, it has been shown that both methods are not able to provide proper individual balancing when the CHB-STATCOM is not exchanging current with the grid (here denoted as zero-current mode). This condition is especially critical for the star-connected CHB-STATCOM, due to the lack of a closed path for the current (such as in the delta configuration) to exchange energy between

the three phases. Two methods for individual DC-link voltage balancing at zero-current mode have been proposed and discussed. The first method is based on a modified sorting algorithm, which takes advantage of the knowledge of the current ripple during zero-current operations, while the second method consists in superimposing a slow modulation signal to the DC-link voltage reference. The effectiveness of the two methods has been verified via simulation results. However, it is of importance to stress that the modified sorting approach can only be adopted when the RMS current is lower than the current ripple. Furthermore, the method is sensitive to harmonic distortion in the measured signals. This limits the applicability of the method to CHB-STATCOMs with low number of cascaded cells. On the other hand, the DC-link modulation technique provides a simple solution, without the main limitations present in the previous method. Furthermore, it is of importance to stress that the introduced oscillations in the DC voltage lead to a small active (not reactive) power flow between the converter and the grid, thus they will not have an impact on the grid voltage. However, carefulness must be adopted when the converter is meant to be operated in highly distorted grids.

Chapter 5 focuses on the operation of the CHB-STATCOM under unbalanced conditions. The needed control modifications to allow an independent control of positive- and negative-sequence components of the injected current have been discussed. Furthermore, a modification in the cluster controller to allow an uniform active power distribution between the phase legs of the converter has been described. This includes the use of a zero-sequence voltage (for the star configuration) or current (delta) to control the DC-link voltages to their reference value. Theoretical analysis has shown that regardless of the configuration utilized for the CHB-STATCOM, a singularity exists when trying to guarantee balancing in the DC-link capacitor voltages. In particular, it has been shown that when the phase legs of the converter are connected in star, the CHB-STATCOM is sensitive to the level of unbalance in the current exchanged with the grid, with a singularity in the solution when positive- and negative-sequence currents have the same magnitude. Similar results have been obtained for the delta configuration, where the system is found to be sensitive to the level of unbalance in the applied voltage. Furthermore, these singularities as well as the zero-sequence voltage/current demands around the singularity points highly depend on the relative phase shift between the sequence components (current for the star and voltage for the delta configuration). The presence of these singularities represents an important limit of this topology for STATCOM applications and suggests that the star configuration is most suitable for utility applications, where the converter is mainly employed for voltage regulation (mainly through positive-sequence current injection); for industrial applications or, more in general, when the CHB-STATCOM is used for balancing purposes, the delta configuration is the most preferable choice. However, the converter must be over-rated in terms of current in order to accommodate the needed circulating current. Furthermore, the dependency of the singularity on the level of voltage unbalance can lead to difficulties in the capacitor balancing in case of unsymmetrical faults that occur in the vicinity of the point of common coupling. All theoretical findings have also been validated through experimental tests.

7.2 Future work

The CHB converter and more in general the modular multilevel concept is still rather new and offers both opportunities and challenges for the researchers to improve its efficiency and performance. One important aspect that still needs research effort is the control and modulation of the converter; today, the research community is mainly divided into two main streams: the classical control and modulation approach, mainly based on linear control theory combined with various PWM techniques, and Model Predictive Control (MPC) approach. Both directions are of high interest and need further investigation in order to preserve (or even increase) the performance of the system and at the same time reduce to the minimum the number of switching events.

Also, the operation of the CHB-STATCOM in case of connection to weak grids is a challenge, especially when utilized for balancing purpose. Under this scenario, an interesting field of research is to investigate alternative control strategies for positive- and negative-sequence current injection, especially when the CHB-STATCOM is stressed and operated close to its limits.

It has been shown in this thesis that the two main configurations for the CHB-STATCOM available in today's market (i.e., the star and the delta configuration) present severe limitations when operated under unbalanced conditions. Recent standards require more and more participation from grid-connected converters to reduce the level of unbalance in the grid; if this is not a problem for those multilevel converters that present a common DC link (such as the NPC or the CCC topologies), the limitations in the star and delta CHB-STATCOM can be crucial and limit the applicability of this converter topology. For this reason, it can be of high interest to investigate alternative configurations for modular multilevel STATCOMs, in order to extend its operational range under unbalanced conditions.

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Appendix A

Transformations for three-phase systems

A.1 Introduction

This appendix describes transformations to calculate voltage vectors from three-phase quantities and vice versa. Moreover, expressions of the voltage vector both in the fixed ($\alpha\beta$-) and rotating (dq-) reference frame are given in the general case of unbalanced three-phase quantities.

A.2 Transformations of three-phase quantities into vector

A three phase positive system constituted by the three quantities $v_{\mathrm{a}}(t)$,$v_{\mathrm{b}}(t)$ and $v_{\mathrm{c}}(t)$ can be transformed into a vector in a complex reference frame, usually called $\alpha\beta$-reference frame by applying the following transformation

$$\underline{v}(t) = v_\alpha + \mathrm{j}v_\beta = K_{\mathrm{ab}}\left(v_{\mathrm{a}}(t) + v_{\mathrm{b}}(t)e^{\mathrm{j}\frac{2}{3}\pi} + v_{\mathrm{c}}(t)e^{\mathrm{j}\frac{4}{3}\pi}\right) \tag{A.1}$$

where the factor K_{ab} is equal to $\sqrt{3/2}$ or $2/3$ to ensure power or amplitude invariant transformation, respectively, between the two systems. Equation (A.1) can be shown in matrix form as

$$\begin{bmatrix} v_\alpha(t) \\ v_\beta(t) \end{bmatrix} = C_{23}\begin{bmatrix} v_{\mathrm{a}}(t) \\ v_{\mathrm{b}}(t) \\ v_{\mathrm{c}}(t) \end{bmatrix} \tag{A.2}$$

where the matrix C_{32} is equal to

$$C_{32} = K_{\mathrm{ab}}\begin{bmatrix} 1 & -\frac{1}{2} & -\frac{1}{2} \\ 0 & \frac{\sqrt{3}}{2} & -\frac{\sqrt{3}}{2} \end{bmatrix} \tag{A.3}$$

The inverse transformation, assuming no zero-sequence, i.e. $v_{\mathrm{a}}(t)+v_{\mathrm{b}}(t)+v_{\mathrm{c}}(t)=0$, is given by

$$\begin{bmatrix} v_{\mathrm{a}}(t) \\ v_{\mathrm{b}}(t) \\ v_{\mathrm{c}}(t) \end{bmatrix} = C_{23} \begin{bmatrix} v_{\alpha}(t) \\ v_{\beta}(t) \end{bmatrix} \tag{A.4}$$

where C_{23} is equal to

$$C_{23} = \frac{1}{K_{\mathrm{ab}}} \begin{bmatrix} \frac{2}{3} & 0 \\ -\frac{1}{3} & \frac{1}{\sqrt{3}} \\ -\frac{1}{3} & -\frac{1}{\sqrt{3}} \end{bmatrix} \tag{A.5}$$

A.2.1 Transformations between fixed and rotating coordinate systems

Let the vector $\underline{v}(t)$ rotates in the $\alpha\beta$-reference frame with the angular frequency of $\omega(t)$ in the positive (counter-clockwise) direction. Let also a dq-frame rotates in the same direction with the same angular frequency. In such a case, the vector $\underline{v}(t)$ appears as a fixed vector in the dq-frame. The components of $\underline{v}(t)$ in the dq-frame are thus given by the projections of the vector $\underline{v}(t)$ on the d-axis and q-axis of the dq-frame as shown in Fig. A.1.

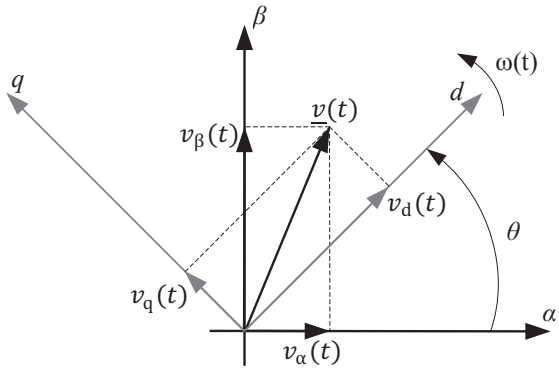

Fig. A.1 Relation between $\alpha\beta$-frame and dq-frame.

The transformation can be written in vector form as

$$\underline{v}_{(\mathrm{dq})}(t) = \underline{v}_{(\alpha\beta)}(t)e^{-\mathrm{j}\theta(t)} \tag{A.6}$$

with the angle $\theta(t)$ in Fig. A.1 given by

$$\theta(t) = \theta_0 + \int_0^t \omega(\tau)d\tau \tag{A.7}$$

The inverse transformation, from the rotating dq-frame to the fixed $\alpha\beta$-frame is defined by

$$\underline{v}_{(\alpha\beta)}(t) = \underline{v}_{(\mathrm{dq})}(t)e^{\mathrm{j}\theta(\mathrm{t})} \tag{A.8}$$

The transformation between the dq- and $\alpha\beta$-frames can be written in matrix form as

$$\begin{bmatrix} v_{\mathrm{d}}(t) \\ v_{\mathrm{q}}(t) \end{bmatrix} = R(-\theta(t)) \begin{bmatrix} v_{\alpha}(t) \\ v_{\beta}(t) \end{bmatrix} \tag{A.9}$$

which is the transformation from the fixed $\alpha\beta$-frame to the dq-frame and

$$\begin{bmatrix} v_{\alpha}(t) \\ v_{\beta}(t) \end{bmatrix} = R(\theta(t)) \begin{bmatrix} v_{\mathrm{d}}(t) \\ v_{\mathrm{q}}(t) \end{bmatrix} \tag{A.10}$$

which is the transformation from the the dq-frame to the fixed $\alpha\beta$-frame. The projection matrix $R(\theta(t))$ is

$$R(\theta(t)) = \begin{bmatrix} \cos(\theta(t)) & -\sin(\theta(t)) \\ \sin(\theta(t)) & \cos(\theta(t)) \end{bmatrix} \tag{A.11}$$

A.3 Voltage vectors for unbalanced conditions

Let consider the following phase voltages for a three-phase system

$$\begin{aligned} v_{\mathrm{a}}(t) &= \hat{v}_{\mathrm{a}}(t)\cos(\omega t - \varphi_{\mathrm{a}}) \\ v_{\mathrm{b}}(t) &= \hat{v}_{\mathrm{b}}(t)\cos(\omega t - \varphi_{\mathrm{b}} - \tfrac{2}{3}\pi) \\ v_{\mathrm{c}}(t) &= \hat{v}_{\mathrm{c}}(t)\cos(\omega t - \varphi_{\mathrm{c}} - \tfrac{4}{3}\pi) \end{aligned} \tag{A.12}$$

where $\hat{v}_{\mathrm{a}}(t)$ and φ_{a} are the amplitude and phase angle of phase voltage $v_{\mathrm{a}}(t)$, $\hat{v}_{\mathrm{b}}(t)$ and φ_{b} are the amplitude and phase angle of phase voltage $v_{\mathrm{b}}(t)$, $\hat{v}_{\mathrm{c}}(t)$ and φ_{c} are the amplitude and phase angle of phase voltage $v_{\mathrm{c}}(t)$, while ω is the angular frequency of the system.

Any unbalanced condition leads to unequal voltage amplitude or phase angle of the three phases. In such condition, the resulting voltage vector $\underline{v}_{\alpha\beta}(t)$ in the fixed $\alpha\beta$-frame can be expressed as the sum of two vectors rotating in opposite directions and interpreted as positive- and negative-sequence component vectors.

$$\underline{v}_{\alpha\beta}(t) = E^{+}e^{\mathrm{j}(\omega\mathrm{t}+\varphi^{+})} + E^{-}e^{-\mathrm{j}(\omega\mathrm{t}+\varphi^{-})} \tag{A.13}$$

where E^{+} and E^{-} are the amplitude of the positive and negative voltage vectors, respectively, and the corresponding phase angles are denoted by φ^{+} and φ^{-}.

When transforming the voltage vector $\underline{v}_{\alpha\beta}$ from the fixed $\alpha\beta$-frame to the rotating dq-frame, two rotating frame can be used, accordingly. These two frames are called positive and negative synchronous reference frames (SRFs) and are denoted as $dqp-$ and $dqn-$frame: the positive SRF rotates counterclockwise with the angular frequency of ω, while the negative SRF rotates clockwise with the same frequency. These two frames can be defined by the following transformations

$$\begin{aligned} \underline{v}_{\mathrm{dqp}}(t) &= e^{-\mathrm{j}\theta(\mathrm{t})}\underline{v}_{\alpha\beta}(t) \\ \underline{v}_{\mathrm{dqn}}(t) &= e^{\mathrm{j}\theta(\mathrm{t})}\underline{v}_{\alpha\beta}(t) \end{aligned} \tag{A.14}$$

Dividing the two equations in Eq. (A.14) leads to

$$\frac{\underline{v}_{\mathrm{dqp}}(t)}{\underline{v}_{\mathrm{dqn}}(t)} = e^{-\mathrm{j}2\theta(\mathrm{t})} \Rightarrow \underline{v}_{\mathrm{dqp}}(t) = \underline{v}_{\mathrm{dqn}}(t)e^{-\mathrm{j}2\theta(\mathrm{t})} \tag{A.15}$$

According to Eq. (A.15), considering the positive-sequence component as a DC-component (zero frequency) in the positive SRF, the negative-sequence component will be a vector that rotates with 100 Hz clockwise in the positive SRF. An analogues relation can be derived for a positive-sequence component in the negative SRF.

Appendix B

Symmetrical component basics

B.1 Introduction

This appendix describes the symmetrical component basics and shows how to extract the positive and negative and zero sequences from a set of three-phase unbalanced voltage and vice versa.

B.2 Positive, negative and zero sequence extraction

Figure B.1 shows three sets of phase vectors. The positive sequence is defined by

$$\begin{aligned} v_{\mathrm{a}}^{+} &= V^{+}\cos(\omega t) \\ v_{\mathrm{b}}^{+} &= V^{+}\cos(\omega t - \tfrac{2}{3}\pi) \\ v_{\mathrm{c}}^{+} &= V^{+}\cos(\omega t - \tfrac{4}{3}\pi) \end{aligned} \tag{B.1}$$

The negative sequence is defined as follow:

$$\begin{aligned} v_{\mathrm{a}}^{-} &= V^{-}\cos(\omega t + \theta^{-}) \\ v_{\mathrm{b}}^{-} &= V^{-}\cos(\omega t + \theta^{-} - \tfrac{4}{3}\pi) \\ v_{\mathrm{c}}^{-} &= V^{-}\cos(\omega t + \theta^{-} - \tfrac{2}{3}\pi) \end{aligned} \tag{B.2}$$

and the zero sequence is defined as:

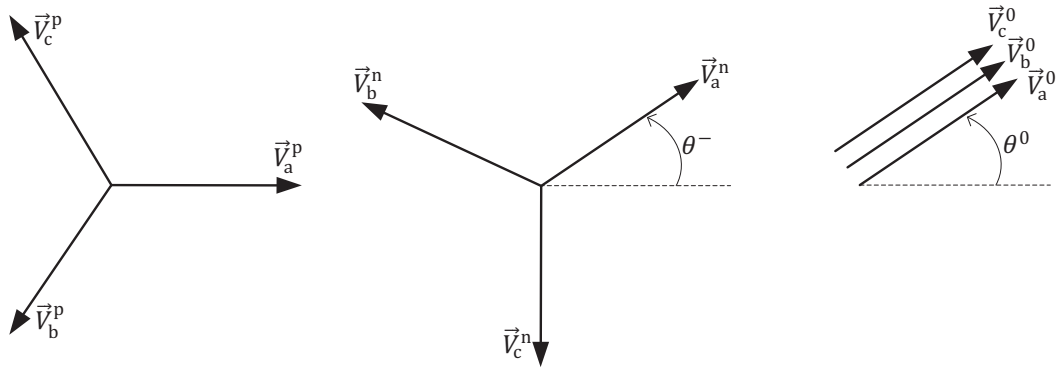

Fig. B.1 Positive, Negative and zero sequence components for a three phase unbalanced system.

$$\begin{aligned} v_a^0 &= V^0 \cos(\omega t + \theta^0) \\ v_b^0 &= V^0 \cos(\omega t + \theta^0) \\ v_c^0 &= V^0 \cos(\omega t + \theta^0) \end{aligned} \tag{B.3}$$

The time domain expressions can also be expressed in phasors form. Positive sequence phasors are

$$\begin{aligned} \vec{V}_a^+ &= V^+ e^{j0} \\ \vec{V}_b^+ &= V^+ e^{-j\frac{2}{3}\pi} \\ \vec{V}_c^+ &= V^+ e^{-j\frac{4}{3}\pi} \end{aligned} \tag{B.4}$$

the negative sequence phasors are

$$\begin{aligned} \vec{V}_a^- &= V^- e^{j\theta_n} \\ \vec{V}_b^- &= V^- e^{(\theta_n - j\frac{4}{3}\pi)} \\ \vec{V}_c^- &= V^- e^{(\theta_n - j\frac{2}{3}\pi)} \end{aligned} \tag{B.5}$$

and finally the zero sequence phasors are

$$\begin{aligned} \vec{V}_a^0 &= V^0 e^{j\theta_0} \\ \vec{V}_b^0 &= V^0 e^{\theta_0} \\ \vec{V}_c^0 &= V^0 e^{\theta_0} \end{aligned} \tag{B.6}$$

Concerning now a set of unbalanced three-phase voltage phasor as $\vec{V}_{\mathrm{a}}$,$\vec{V}_{\mathrm{b}}$ and $\vec{V}_{\mathrm{c}}$, according to symmetrical component theory these phasors can be written as:

$$\begin{aligned}\vec{V}_{\mathrm{a}} &= \vec{V}_{\mathrm{a}}^{+} + \vec{V}_{\mathrm{a}}^{-} + \vec{V}_{\mathrm{a}}^{0} \\ \vec{V}_{\mathrm{b}} &= \vec{V}_{\mathrm{b}}^{+} + \vec{V}_{\mathrm{b}}^{-} + \vec{V}_{\mathrm{b}}^{0} \\ \vec{V}_{\mathrm{c}} &= \vec{V}_{\mathrm{c}}^{+} + \vec{V}_{\mathrm{c}}^{-} + \vec{V}_{\mathrm{c}}^{0}\end{aligned} \tag{B.7}$$

In order to extract the positive, negative and zero sequence component phasor operator a is defined as

$$a = e^{\mathrm{j}\frac{2}{3}\pi} \tag{B.8}$$

operations on the a phasor are shown in Fig. B.2.

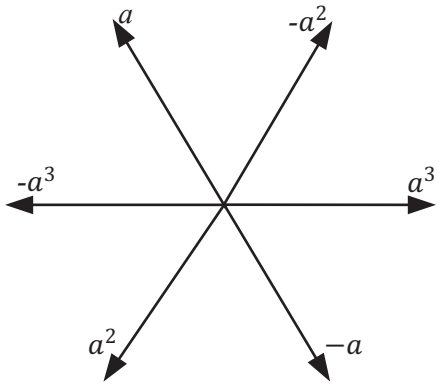

Fig. B.2 Operations on the a operator.

Using the phasor operator a defined in Eq. (B.8), the positive, negative and zero sequence phasor defined in Eq. (B.4)-(B.6) can be written as

$$\begin{aligned}V_{\mathrm{b}}^{+} &= a^2 V_{\mathrm{a}}^{+} \\ V_{\mathrm{c}}^{+} &= a V_{\mathrm{a}}^{+} \\ V_{\mathrm{b}}^{-} &= a V_{\mathrm{a}}^{-} \\ V_{\mathrm{c}}^{-} &= a^2 V_{\mathrm{a}}^{-} \\ V_{\mathrm{b}}^{0} &= V_{\mathrm{a}}^{0} \\ V_{\mathrm{c}}^{0} &= V_{\mathrm{a}}^{0}\end{aligned} \tag{B.9}$$

Substituting Eq. (B.9) into Eq. (B.7) yields

$$\begin{aligned}
\vec{V}_{\mathrm{a}} &= \vec{V}_{\mathrm{a}}^{+} + \vec{V}_{\mathrm{a}}^{-} + \vec{V}_{\mathrm{a}}^{0} \\
\vec{V}_{\mathrm{b}} &= \vec{V}_{\mathrm{b}}^{+} + \vec{V}_{\mathrm{b}}^{-} + \vec{V}_{\mathrm{b}}^{0} = a^2 V_{\mathrm{a}}^{+} + a V_{\mathrm{a}}^{-} + V_{\mathrm{a}}^{0} \\
\vec{V}_{\mathrm{c}} &= \vec{V}_{\mathrm{c}}^{+} + \vec{V}_{\mathrm{c}}^{-} + \vec{V}_{\mathrm{c}}^{0} = a V_{\mathrm{a}}^{+} + a^2 V_{\mathrm{a}}^{-} + V_{\mathrm{a}}^{0}
\end{aligned} \tag{B.10}$$

The expression can be shown in matrix form as

$$\begin{bmatrix} \vec{V}_{\mathrm{a}} \\ \vec{V}_{\mathrm{b}} \\ \vec{V}_{\mathrm{c}} \end{bmatrix} = \begin{bmatrix} 1 & 1 & 1 \\ 1 & a^2 & a \\ 1 & a & a^2 \end{bmatrix} \begin{bmatrix} \vec{V}_{\mathrm{a}}^{0} \\ \vec{V}_{\mathrm{a}}^{+} \\ \vec{V}_{\mathrm{a}}^{-} \end{bmatrix} \tag{B.11}$$

denoting:

$$B = \begin{bmatrix} 1 & 1 & 1 \\ 1 & a^2 & a \\ 1 & a & a^2 \end{bmatrix} \tag{B.12}$$

Inverse matrix of B can be shown as

$$B^{-1} = \frac{1}{3} \begin{bmatrix} 1 & 1 & 1 \\ 1 & a & a^2 \\ 1 & a^2 & a \end{bmatrix} \tag{B.13}$$

Using the inverse matrix of B the symmetrical positive,negative and zero sequence components in terms of the phase voltages can be written as follow

$$\begin{bmatrix} \vec{V}_{\mathrm{a}}^{0} \\ \vec{V}_{\mathrm{a}}^{+} \\ \vec{V}_{\mathrm{a}}^{-} \end{bmatrix} = \frac{1}{3} \begin{bmatrix} 1 & 1 & 1 \\ 1 & a & a^2 \\ 1 & a^2 & a \end{bmatrix} \begin{bmatrix} \vec{V}_{\mathrm{a}} \\ \vec{V}_{\mathrm{b}} \\ \vec{V}_{\mathrm{c}} \end{bmatrix} \tag{B.14}$$

substituting Eq. (B.14) into Eq. (B.9) and after some manipulation the following expressions can be obtained for all the symmetrical component sequences from the unbalanced phase voltages. The positive sequence can be expressed as

$$\begin{bmatrix} \vec{V}_{\mathrm{a}}^{+} \\ \vec{V}_{\mathrm{b}}^{+} \\ \vec{V}_{\mathrm{c}}^{+} \end{bmatrix} = \frac{1}{3} \begin{bmatrix} 1 & a & a^2 \\ a^2 & 1 & a \\ a & a^2 & 1 \end{bmatrix} \begin{bmatrix} \vec{V}_{\mathrm{a}} \\ \vec{V}_{\mathrm{b}} \\ \vec{V}_{\mathrm{c}} \end{bmatrix} \tag{B.15}$$

The negative sequence can be expressed as

$$\begin{bmatrix} \vec{V}_{\mathrm{a}}^{-} \\ \vec{V}_{\mathrm{b}}^{-} \\ \vec{V}_{\mathrm{c}}^{-} \end{bmatrix} = \frac{1}{3} \begin{bmatrix} 1 & a^2 & a \\ a & 1 & a^2 \\ a^2 & a & 1 \end{bmatrix} \begin{bmatrix} \vec{V}_{\mathrm{a}} \\ \vec{V}_{\mathrm{b}} \\ \vec{V}_{\mathrm{c}} \end{bmatrix} \tag{B.16}$$

The zero sequence can be expressed as

$$\begin{bmatrix} \vec{V}_a^0 \\ \vec{V}_b^0 \\ \vec{V}_c^0 \end{bmatrix} = \frac{1}{3} \begin{bmatrix} 1 & 1 & 1 \\ 1 & 1 & 1 \\ 1 & 1 & 1 \end{bmatrix} \begin{bmatrix} \vec{V}_a \\ \vec{V}_b \\ \vec{V}_c \end{bmatrix} \tag{B.17}$$

It should be noted that the theory explained in this appendix is based on phase voltage. However, the same theory is also valid for line-to-line voltages without any modification.