Thermo-Mechanical Simulations of SiC Power Modules with Single and Double Sided Cooling

Klas Brinkfeldt[1], Michael Edwards[2], Jonas Ottosson[3], Klaus Neumaier[4], Olaf Zschieschang[4], Alexander Otto[5], Eberhard Kaulfersch[6], Dag Andersson[1]

[1]Swerea IVF, Argongatan 30, SE-431 53 Mölndal, Sweden
[2]Chalmers University of Technology, SE-412 96 Göteborg, Sweden
[3]Volvo Group Truck Technology, Sven Hultins gata 9D, SE-412 88 Göteborg, Sweden
[4]Fairchild Semiconductor GmbH, Einsteinring 28, D-85609 Aschheim, Germany
[5]Fraunhofer ENAS, Technologie-Campus 3, D-09126 Chemnitz, Germany
[6]Berliner Nanotest und Design GmbH, Volmerstr. 9B, D-12489 Berlin, Germany

Abstract

Effectively removing dissipated heat from the switching devices enables a higher current carrying capability per chip area ratio, thus leading to smaller or fewer devices for a given power requirement specification. Further, the use of SiC based devices has proven to increase the efficiency of the system thereby reducing the dissipated heat. Thermal models have been used to compare SiC power modules. Single and double sided cooling have been simulated. The simulated maximum temperatures were 141 °C for the single sided version and 119.7 °C for the double sided version. In addition, the reliability of a single sided module and thermally induced plastic strains of a double sided module have been investigated. A local model of the wire bond interface to the transistor metallization shows a 3‰ maximum increase in plastic strain during the power cycle. Simulations of the creep strain rates in the die attach solder layer for a power cycling loads also shows a 3‰ increase in creep strain per cycle.

1. Introduction

The trends in power electronics devices point to higher power densities and switching frequencies combined with smaller system volumes. Generally these factors all lead to higher losses and/or higher operational temperatures, the main driver of package related failure mechanisms, which influences the reliability of the systems. Efficient thermal design of the modules is important to reduce temperature in the modules.

Common failure modes in power devices arise from temperature driven fatigue mechanisms in the packaging and interconnection materials and include bond wire lift-off and heel cracking, solder layer delamination and delamination of the DBC copper layers [1-3].

The power modules in this work are based on SiC power semiconductor devices, which have proven to increase the efficiency of the electronics system [4-5]. Since SiC-based devices allow higher device junction temperatures and enable a higher current carrying capability per chip area ratio, this is leading to smaller or fewer devices for a given power requirement specification. However, since lower operational and cycling temperatures are expected to increase the life time and enlarge reliability margins of the devices and their packages regardless of the semiconductor material, it is essential to remove dissipated heat effectively from the switching devices. Thus, improvements to the thermal management become important.

One way to achieve larger heat exchange area, and thereby a reduction in thermal resistance and operational temperature, is to cool both sides of the module. This is expected to enable an increase in the current carrying capability and a possibility to reduce the chip area and the required system volume even further. Since double-sided cooling requires new interconnection methods for the top side contacts on the devices, the removal of wire bond also has other benefits. These include removal of failure mechanisms and reliability issues associated with wire bonds and it has been demonstrated to significantly reduce the switching cell inductance, which allows for high speed switching and lower switching losses [6].

Sintered silver has been introduced as a die attach material in the field of power electronics [7]. The material consists of nano-scale, alternatively a mixture of nano- and micro-scale particles in an organic solvent/binder. The small particle sizes enable a sintering temperature in the order of 200-300 °C depending on if the surface material is Ag or Au, while the resulting joint is pure Ag with a melting temperature, T_m = 961 °C. The sintering process typically involves screen or stencil printing, a drying step, placement of the device chip followed by a rapid heating to above 250 °C, during which it is recommended to apply a pressure load of typically > 5 MPa. The high thermal and electrical conductivity of silver combined with a low processing temperature and high melting temperature makes the material very attractive to power electronics die attach applications.

In this work, the temperature response to power cycles are investigated using thermal models of single and double sided SiC-based power modules. Comparative simulations with single and double sided cooling of the devices are presented. Sintered silver is used as the die attach for the double sided versions.

In addition, creep and plastic strain from thermally induced stresses in the device layer are investigated using an FE-model.

978-1-4799-9950-7/15/$31.00 ©2015 IEEE

2015 16th International Conference on Thermal, Mechanical and Multi-Physics Simulation and Experiments in Microelectronics and Microsystems

2. Thermal Models

A thermal model was set up, in which a power module containing SiC switching devices sandwiched between two DBC substrates were subjected to three power pulses with a cycle time of 3 s and an on-time of 1.5 s. The simulated power dissipation was 70 W per chip, set up as an internal heat source in the model.

Two thermal simulations were run on the model. One had convection boundary conditions on the top surface of the top DBC substrate and the bottom layer of the bottom DBC substrate set to 3000 W/(m^{2}K), simulating water based heat sinks attached to the top and bottom of the power module.

The other simulation had only convection assigned to the bottom DBC, while the top was set to adiabatic boundary condition without heat transfer to the ambient.

The results of the simulations are shown in Figures 1 and 2. The simulated maximum temperatures of the devices are 133.8 °C and 119.7 °C for the simulation run with single and double sided cooling respectively. It should be pointed out that the geometrical model was identical for the two models.

In addition to the large, full-scale model, a local sub-model containing a slice through all layers over one device chip including 0.5 mm of its surrounding materials in x and y direction was created.

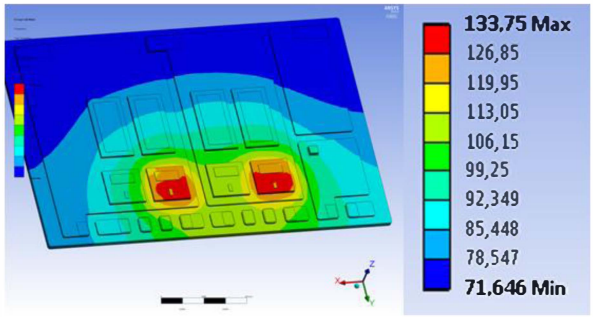

Figure 1: Thermal simulation results of single sided cooling version after 3 power cycles with a cycle time of 3 s and an on-time of 1.5 s.

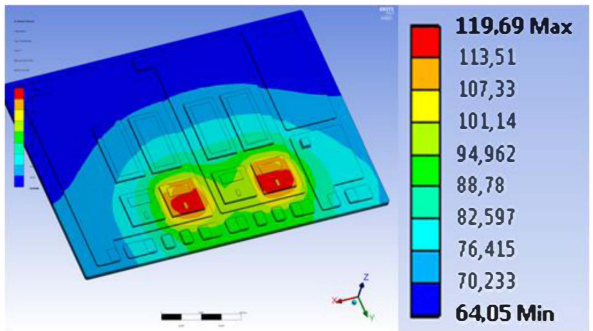

Figure 2: Thermal simulation results of the double sided cooling version after 3 power cycles with a cycle time of 3 s and an on-time of 1.5 s.

The local sub-model used thermal boundary conditions from the larger model on each side of the stack. Identical convection conditions on top and bottom surfaces and identical power pulses and cycle times were used. The results are shown in Figure 3. Maximum temperature attained on the SiC device chip was 82.2 °C.

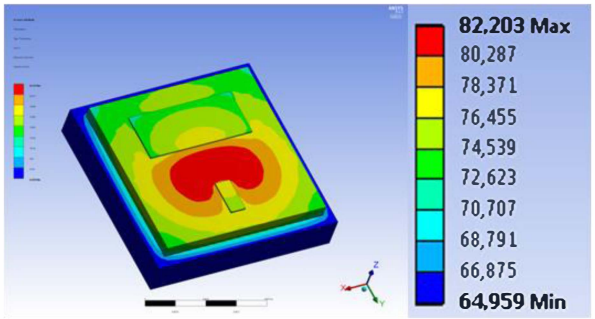

Figure 3: Thermal simulations of double sided local model.

A more realistic model of the single sided cooling version, where the top DBC has been removed and the epoxy molding material covers all of the top surfaces of the active switching devices (bond wires are not included) has also been simulated.

Results of the thermal simulation of this model are shown in Figure 4 for a powering of two transistors for 180 s. The maximum temperature increases in this case compared to the results shown in Figure 1.

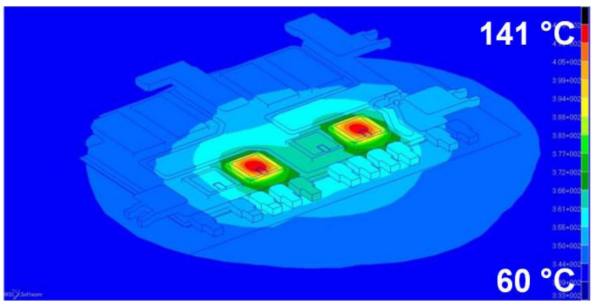

Figure 4: Simulation results on SiC power module for active cycling after t_{on}=180s

3. Thermo-Mechanical Analysis

3.1 Single Sided Cooling Version

Numerical simulation of the thermo-mechanical response of a single sided power module to assembly and test conditions have been performed to analyze and systematically evaluate the response of the device under thermal and mechanical load conditions. To visualize weak points of the design, FE modeling has been successfully used in identifying process steps and loading conditions mainly contributing to deformations and stresses in the module. Stresses and strains within the interconnection system induced by thermal loads from processing and expected operation in automotive applications have been investigated to find relevant

failure mechanisms and to facilitate a more relevant reliability assessment. An FE model of the module and a sub-model of a bond wire interconnect has been generated as shown in Figure 5.

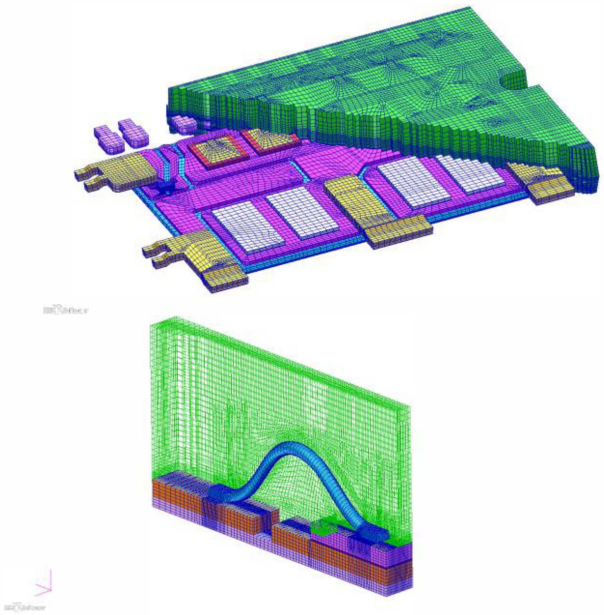

Figure 5: FE models of the SiC power module and the local wire bond.

The simulations of the package behavior located accumulating plastic and creep strains over the process steps and through active thermal cycling. A typical process flow includes soldering on DBC substrate and transfer molding. Thermo-mechanical simulations were used to investigate soldering and molding processes followed by power cycling on a dedicated test bench. Process simulation was performed with individual materials added analogue to the real technological process to take into account intrinsic stresses induced by thermal mismatch at various steps of production.

Thermo-mechanical reliability investigations addressed mainly equivalent creep strains accumulating during assembly and cycling, the latter serving as failure criterion for low cycle solder fatigue. The creep model used in this work for steady state creep is based on an exponential function of stress described in [8]:

$$\frac{d\gamma_s}{dt} = C\sinh[(\alpha\tau)]^n \; e^{-Q_a/kT} \qquad (1)$$

Where the constant C = 277984, τ is the applied stress, α = 0.02447 and represents the stress level at which the power law breaks down, n = 6.40599 and the activation energy Q_a = 0.56414. Equation 1 represents the shear strain rate. The relationship between the shear and tensile stress and strain is:

$$\gamma = \sqrt{3}\varepsilon, \text{ and } \tau = 1/\sqrt{3}\sigma\,, \qquad (2)$$

where γ and ε are the shear and tensile strains and τ and σ are shear and tensile stresses.

Figure 6 shows the incremental increase in creep deformation in the solder die attach of the active devices after 180 s power on and cooling down to RT. The simulated power dissipation was 65 W per device chip. The model predicts a roughly 3‰ maximum rise in creep at the die attach.

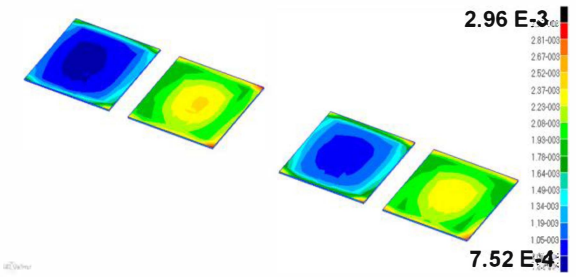

Figure 6: Equivalent creep strain increment accumulated during one power cycle with t_{on} of 180s

Rupture of the wire bond interconnection to the SiC devices is expected to be a failure cause in power cycling due to the high stiffness of the semiconductor material. Sub-modeling has been employed to investigate stressing of the bond under thermo-mechanical loading during power cycling.

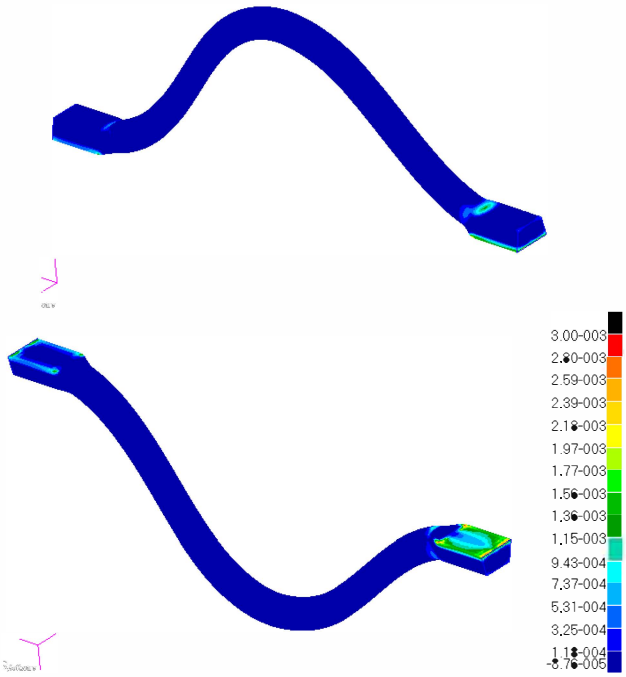

Figure 7: Equivalent plastic strain increment accumulated in the bond wire during one power cycle with t_{on} of 180 s.

For the Al wire bond subjected to repetitive plastic deformation a Coffin-Manson expression for the number of cycles to failure has been widely applied [9]:

$$N = a\,\varepsilon_{pl}^{-b} \qquad (3)$$

It correlates the plastic strain in the damaged region with the cycles to failure by a power law with constants obtained from stress experiments. The coefficients are always related to dedicated cycling experiments and not transferrable [10].

3.2 Double Sided Cooling Version

The strain behavior of sintered nanosilver particles has been investigated by [11-14]. Since the melting temperature of the silver is much higher, the operational temperature of many applications is comparatively low. For example, the homologous temperature of eutectic tin-based solders at normal operating temperatures (-40 °C - 125 °C) ranges from typically 0.4 - 0.8 T_m, while for the sintered silver it ranges from 0.18 - 0.32 T_m. This suggests that creep effects should be lower in sintered silver joints compared to solder joints. Dudek et al [14] developed a model based on bulk silver material with added porosities and concluded that different failure mechanisms can be expected compared to eutectic solders, primarily since the sintered silver layers do not decouple the stresses in the device chip from the substrate as effectively as is the case for solder die attach.

A plastic strain model from [14] and a time hardening model derived from [12] have been used to model plastic strain and primary creep strain in the sintered silver layers. The time hardening model is described as:

$$\frac{d\varepsilon}{dt} = C_1 \sigma^{C_2} t^{C_3} e^{-C_4/T} \qquad (3)$$

Where σ is the stress, t is time and T is the temperature. The constants $C_{1\text{-}4}$ are listed in Table 1.

Table 1: Time hardening model constants.

C_1	C_2	C_3	C_4
9,81	3,26E-3	-1.0	5.7063E+9

The local model used in the thermal analysis had a complicated geometry at the top side device connections (not shown in any of the figures), which made meshing and solving difficult. Instead, a new local model which has simplified top side connections was created. The new local model simply has a DBC substrate overlaying the device with an unstructured copper layer connected to both base and emitter sintered silver contacts. Apart from this, the model was set up as close as possible to the previous local model.

The thermal loading was identical to that described in Section 2 with three power dissipation pulses of 70 W with a cycle time of 3 s and an on-time of 1.5 s. Thermal simulations on the simplified model confirmed a similar output as the previous model which was used as the thermal loading in the thermo-mechanical model. With the simplified model, thermal results were not automatically available from the larger model via sub-modeling and the thermal boundary conditions had to be transferred manually. The stress-free temperature in the model was set to 180 °C.

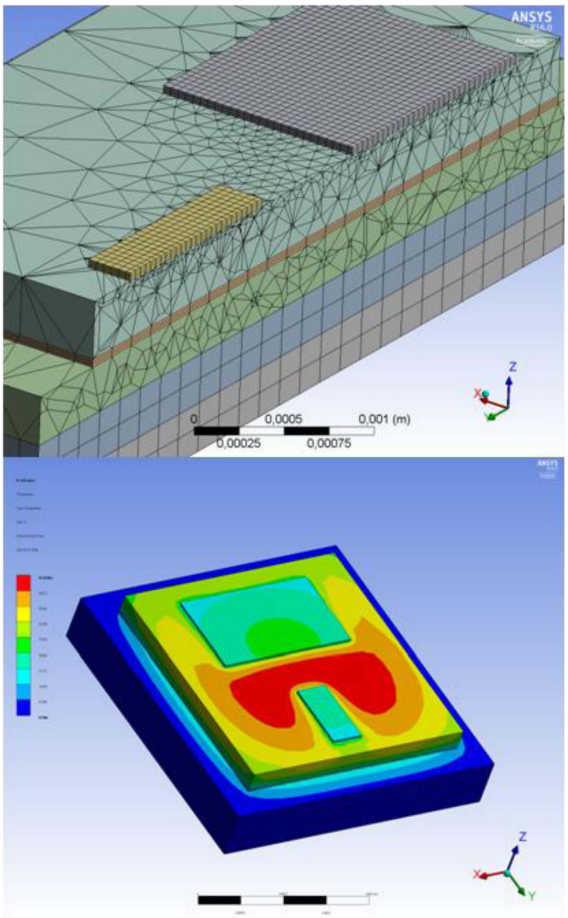

Figure 8: Meshing through a cross section of the model and thermal simulation results of a modified local model with simplified geometry.

The results of the thermo-mechanical analysis are shown in Figures 9 and 10. The model predicts an equivalent (von-Mises) stress of around 160 MPa at the edges of the sintered silver layers on top of the device chip. The model predicts a small area of maximum 2.3 % strain at the corners of the sintered layers, which is higher than the values on the stress-strain curve used [14] and unrealistically high. Simulated plastic strains on the top base and emitter sintered layers away from the base corners are around to 0.7 %.

The model does not predict any creep strains at all at the simulated thermal loading.

4. Discussion of Results

As expected, thermal simulations predict lower temperatures at the active switching devices in the models with cooling on both top and bottom. The predicted temperature decrease with double sided cooling was 15-42 %. This is not surprising since the temperature decrease is expected to be lower than 50 % because of the difference in the layout of the DBC copper layers connecting top and bottom of the device chip. This asymmetry causes a lower reduction in thermal resistance on the top side than on the bottom side of the active devices. The results of the thermal simulations in Figures 1-3 and 8 show that the geometry of the epoxy molding material also influences the temperature profile. The temperature is higher where the molding material is in contact with the device chip comparing 1 W/(mK) to 250 W/(mK) for the silver die attach material. The area where the temperature is high has epoxy blocking the temperature flow. The effect is even clearer in Figures 3 and 8 showing the results from the local models, while it is not predicted in the more realistic one sided cooling model where the mold covers all of the device chips.

The simulated maximum temperature of the single sided thermal model including the top DBC layer was 133 °C compared to the more realistic single sided model at 141 °C. The model with the DBC layer predicts that the extra layer acts as a heat spreader/sink and effectively lower the predicted temperatures on the active devices compared to the more realistic model with only epoxy molding material on the top side of the devices.

The thermo-mechanical creep modeling on the single sided cooling power module predicted a roughly 3‰ maximum rise in creep strains on both the active devices and the local wire bond after 180 s power on then cool down to room temperature. In general, creep strain rates during real operations will likely be larger with all switching devices powered alternately. The high CTE mismatch between DBC and SiC devices is the primary cause of significant strains and stresses evolving in the die attach (Figure 6). Accumulating die attach creep will lead to solder fatigue and thereby an increase of the thermal resistance to the substrate. For the local bond wire model, two major failure causes can be expected: heel cracking and bond lift, respectively. The simulation results shown in Figure 7 indicate that the wire bond interface to the transistor metallization is the area which is most prone to generate bond lift failure due to plastic strains developing from alternating power states.

The model for the double sided version predicts very high plastic strains in the corners of the sintered layers, which in part is considered to be edge effects in the simulation and not present in the real assembly. Another conclusion may be that it is beneficial to have increased porosity at the corners of the sintered layers to reduce strain in these areas. Away from the corners of the base layer, plastic strains of up to 0.7 % are found.

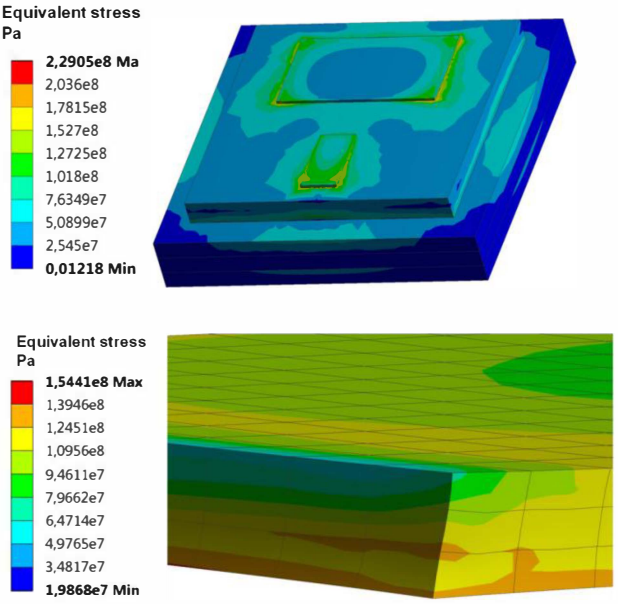

Figure 9: Equivalent (von-Mises) stress in the sintered silver layers and a close-up of the sintered layer at the BJT base contact.

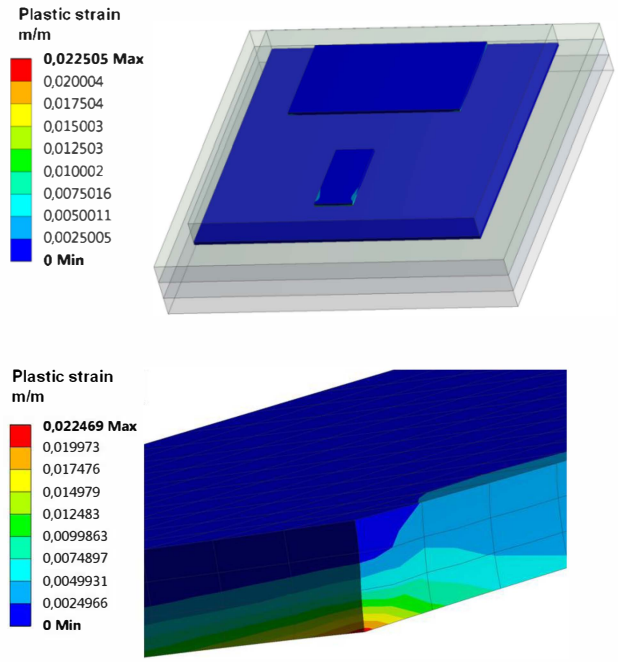

Figure 10: Plastic strain in the sintered silver layers and a close-up of the sintered layer at the BJT base contact.

The model does not predict any creep strains in the sintered layers, which is most likely a result of the short total simulated cycling time. The total cycle time was 8.85 s, including three power pulses with on-times of 1.5 s each.

The double sided thermo-mechanical model included a stress-free temperature of 180 °C. This is a

simplification of the actual fabrication processing steps, which results in less thermal strains in the simulations.

In addition, the local model used for the thermo-mechanical analysis had a simplified geometry connecting the top side contacts of the active device with a single layer of copper. In reality, the base and emitter contact pads are of course connected to separate parts of the DBC copper layer. This means that any heat transfer between them has to pass through the low thermally conductive epoxy molding material in the real modules, while, in the model, heat is spread directly through the copper layer. This is anticipated to cause the simulations to underestimate the strains accumulated in the silver sinter layers on top side of the active device chip.

5. Conclusions

Thermal and thermo-mechanical simulations used to investigate the stress and strain response to thermal loading of power modules with single and double sided cooling have been presented. The thermal simulation models predict a reduction of maximum temperature on the active switching devices from 141.3 C to 119.7 C or lower when utilizing double sided cooling. Creep modeling on the single sided cooling power module showed that roughly 3‰ maximum rise in creep strains on both the active devices and the local wire bond can be expected. The double sided cooling thermo-mechanical model predicts plastic strain at the sintered silver layers of up to 0.7 % and no creep strains. This is believed to be a result of the short thermal loading in the model and is expected to change in an expanded model, which adequately simulate the individual processing steps and a more severe thermal loading.

In conclusion, simulations predict that double sided cooling of power modules can lower the operational temperature by between 15-42 %, which will lead to smaller or fewer devices for a given power requirement specification. Lower operational temperatures can also improve reliability margins and increase life-time of the power electronics devices and packaging.

Acknowledgements

The authors would like to thank the European Commission for supporting these activities within the COSIVU project under grant agreement number 313980.

References

[1] Ciappa, M. (2002). Selected failure mechanisms of modern power modules. Microelectronics Reliability, 42(4-5), 653-667.

[2] Mitic, G., Beinert, R., Klofac, P., Schultz, H. J., & Lefranc, G. (1999). Reliability of AlN substrates and their solder joints in IGBT power modules. Microelectronics Reliability, 39(6-7), 1159-1164.

[3] Lu, H., Bailey, C., & Yin, C. (2009). Design for reliability of power electronics modules. Microelectronics Reliability, 49(9-11), 1250-1255.

[4] Weitzel, C. E., Palmour, J. W., Carter Jr., C. H., Moore, K., Nordquist, et al., (1996). Silicon carbide high-power devices. IEEE Transactions on Electron Devices, 43(10), 1732-1741.

[5] Cooper Jr., J. A., and Agarwal, A. (2002). SiC power-switching devices - the second electronics revolution? Proceedings of the IEEE, 90(6), 956-968.

[6] Hoene, E., Ostmann, A., Lai, B. T., Marczok, C., Müsing, A., & Kolar, J. W. (2013). Ultra-low-inductance power module for fast switching semiconductors. Paper presented at the PCIM Europe Conference Proceedings, 198-205.

[7] Bai, J. G., Zhang, Z. Z., Calata, J. N., & Lu, G. -. (2006). Low-temperature sintered nanoscale silver as a novel semiconductor device-metallized substrate interconnect material. IEEE Transactions on Components and Packaging Technologies, 29(3), 589-593.

[8] Schubert, A., Walter, H., Dudek, R., Michel, B., Lefranc, G., et al., (2001). Thermo-mechanical properties and creep deformation of lead-containing and lead-free solders. Paper presented at the Proceedings of the International Symposium and Exhibition on Advanced Packaging Materials Processes, Properties and Interfaces, 129-134.

[9] Chidambaram, N. V. (1991). A numerical and experimental study of temperature cycle wire bond failure. Paper presented at the Proceedings - Electronic Components Conference, 877-882.

[10] Ramminger, S., Seliger, N., and Wachutka, G. (2000). Reliability model for al wire bonds subjected to heel crack failures. Microelectronics Reliability, 40(8-10), 1521-1525.

[11] Chen, G., Sun, X. -., Nie, P., Mei, Y. -., Lu, G. -., & Chen, X. (2012). High-temperature creep behavior of low-temperature-sintered nano-silver paste films. Journal of Electronic Materials, 41(4), 782-790.

[12] Chen, G., Zhang, Z. -., Mei, Y. -., Li, X., Lu, G. -., & Chen, X. (2013). Ratcheting behavior of sandwiched assembly joined by sintered nanosilver for power electronics packaging. Microelectronics Reliability, 53(4), 645-651.

[13] Li, X., Chen, G., Wang, L., Mei, Y. -., Chen, X., & Lu, G. -. (2013). Creep properties of low-temperature sintered nano-silver lap shear joints. Materials Science and Engineering A, 579, 108-113.

[14] Dudek, R., Döring, R., Sommer, P., Seiler, B., Kreyssig, K., et al (2014). Combined experimental-and FE-studies on sinter-Ag behavior and effects on IGBT-module reliability. Paper presented at the 2014 15th International Conference on Thermal, Mechanical and Multi-Physics Simulation and Experiments in

Microelectronics and Microsystems, EuroSimE 2014.