APPLIED PHYSICS LETTERS 107, 113103 (2015)

Effect of high-k dielectric and ionic liquid gate on nanolayer black-phosphorus field effect transistors

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(Received 30 April 2015; accepted 25 August 2015; published online 15 September 2015)

Nanolayer black phosphorus (BP) is a direct bandgap semiconducting two dimensional crystal, showing immense promise for future nanoelectronic devices. Here, we report the effect of high-k dielectric and ionic-liquid gate in BP field effect transistors (BP FET). An ambipolar behavior is observed in pristine BP FETs with current modulation of 10^4. With a high-k HfO_2 encapsulation, we observed identical switching performance in the BP FETs, however, with noticeable enhancement in mobility at room temperature. In comparison to the pristine device, the HfO_2 encapsulation showed a contrasting decrease in mobility at lower temperatures. BP FETs with electric double layer ionic liquid gate showed a drastic improvement in the subthreshold swing (SS) to 173 mV/dec and operation voltages less than 0.5 V in comparison to solid state SiO_2 back gated devices. Our results elucidate the effect of different electrostatic conditions on BP transistor channels and open up ways for further exploration of their prospects for nanoelectronic devices and circuits.
 [http://dx.doi.org/10.1063/1.4930236]

Moore's law has driven the semiconductor industry towards down-scaling of transistors for faster device performance, less power consumption, cheaper and large-scale fabrication.[1] However, such scaling cannot continue indefinitely due to challenges like short channel effects, leakage, mobility reduction, and fabrication issues.[1] Further development requires exploration of advanced channel materials with high carrier mobility to replace the conventional silicon.[1] The discovery of two dimensional (2D) crystal graphene with high mobility channels has enabled the fabrication of high frequency devices and has unveiled alternative ways to study Dirac physics.[2,3] However, graphene in its pristine form lacks a band gap which is essential for switching in logic circuits.[4] Henceforth, the search for semiconducting 2D materials with a sizable bandgap has resulted in the discovery of crystals of transition metal dichalcogenides (such as MoS_2) and black-phosphorus (BP).[5–9] While, MoS_2 is an n-type semiconductor, the BP shows an ambipolar behavior with dominant p-type conduction. The sub-nanometer dimensionality of these 2D materials gives rise to drastically different qualities when manipulated and structured at atomic scale, making them highly significant from both scientific and technological perspectives.

The interest in BP is primarily due to its direct bandgap, which varies from 0.3 to 1 eV with the number of atomic layers.[6,10] Recently, field effect and photo transistors of BP with high on/off ratios, ambipolar behavior with high hole carrier mobilities, and structural anisotropy have been demonstrated.[6,11–14] Most of these devices were made with Ti/Au source-drain contacts and thick SiO_2 dielectric as the back gate. These reports revealed the presence of a sizable Schottky barrier ~200 meV at Ti/BP interfaces.[11] Such a large barrier at the metal-BP interface remains a hurdle in the fabrication of Ohmic contacts, which are essential for electronic devices[15,16] and viable for spintronic applications.[15] Other strategies to improve performance constitute the use of high k-dielectrics and high capacitance ionic liquid gate for better control over the carrier density and low device operation voltage of the BP channel. It was also observed that the 2D semiconductors are susceptible to surface degradation with exposure to humidity and air exposure over time.[12] Encapsulation using high-k dielectric not only protects the channel against such surface degradation but has also been seen to influence the electrostatic conditions modifying the channel properties. These behaviors necessitate the investigation of the effect of dielectric encapsulated BP channels to realize devices with high reliability. Additionally, ionic liquids (IL) have been used as dielectric for gating field effect devices because of their ability to electrostatically dope the semiconducting channel with carrier densities up to 10^{15} cm^{-2}, which are two orders of magnitude higher than that achieved using solid state gates.[17] Recently, interesting physics has been explored with IL gates on different electronic materials, for example, a metal to insulator transition in VO_2,[18] ferromagnetism in GaMnAs,[19] superconductivity and ambipolar behavior of MoS_2,[20,21] Dirac physics in topological surface states,[22] and very recently insulator to metal transition in BP.[23] Therefore, it is of considerable interest to further investigate the influence of high-k dielectrics and ionic liquid gate on the performance of BP field effect transistors.

In this article, we explore the influence of BP channel encapsulation with a high-k HfO_2 dielectric and electronic double layer transistors with ionic liquid gates. The effects of these electrostatic modifications to the BP channel on the field effect performance, and carrier mobility have been investigated here. Our measurements at different source-drain voltages, gate voltages, and temperatures in both electron and hole conduction regimes provide

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understanding of such BP devices and their prospect in nanoelectronics.

In Figure 1, we present the schematics of devices used in our experiments and a fabricated BP FET. We used BP flakes mechanically exfoliated from bulk BP crystals (procured from Smart elements) onto a SiO_2(285 nm)/Si substrate. The selected flakes were found to have a thickness ~5 nm with width ~2–3 μm as measured from atomic force microscopy and optical microscopy techniques respectively.[24] Ferromagnetic tunnel contacts of TiO_2(1 nm)/Co(65 nm)/Al(4 nm) were prepared over these BP flakes with gaps ~1 μm through nanofabrication techniques of electron beam lithography and e-beam evaporation methods. The thin layer of TiO_2 acts as a tunnel barrier that considerably alleviates the band bending and dramatically reduces the Schottky barrier to few (<50) meV from a high value ~ 200 meV present at the metal/BP interface.[24] Devices with such ferromagnetic tunnel contacts are prospective schemes for spintronic applications.[25,26] For the solid state back gate device, the SiO_2/n-Si substrate was used to control the BP carrier concentration (Fig. 1(a)). In order to investigate the effect of high-k dielectrics on BP channels, devices with an HfO_2 capping layer of 20 nm over the BP channel (shown in Fig. 1(b)) were prepared by atomic layer deposition (ALD) technique at 350 °C. For ionic liquid gate devices, a small droplet of the DEME-TFSI ionic liquid (Sigma Aldrich 727679) was applied onto the devices, covering the BP layer and the source, drain and gate electrode (LG) as depicted in Fig. 1(c). We have performed a detailed characterization of contact resistances and transistor behavior of fabricated BP devices. To extract the Schottky barrier height, we performed temperature dependent drain–source I_{ds}–V_{ds} characteristics of the device at different gate voltages. The Schottky barrier height was found to be <50 meV for BP/TiO_2/Co contacts. The details of the Schottky barrier calculations with TiO_2/Co contacts have been presented elsewhere.[24]

BP FET without capping-layer: We first investigate the field effect transistor characteristics of BP with SiO_2/n-Si back gate as depicted in Fig. 1(a). For these devices, the BP flakes were intentionally aged for one month after the electron beam lithography with PMMA capping to verify reliability and aging effect. Such aged sample of crystals like MoS_2 have been observed to show better current stability.[27] The output characteristics of drain-source current (I_{ds}) while sweeping the drain-source voltage (V_{ds}) were measured at several applied gate voltages (V_g) (Fig. 2(a)). The transfer characteristics were recorded by sweeping the V_g while measuring the I_{ds} for different V_{ds} (Figs. 2(b) and 2(c)). The measured transfer characteristics are typical for ambipolar behavior of BP with an asymmetry in I_{ds}, which is due to the position of the Co Fermi level close to the valence band of the BP.[6,24] The negative and positive gate voltages correspond to hole and electron doping in BP, respectively.

We extract the field effect mobility μ in BP from the slope in the linear region of the measured transfer characteristics using expression (1)

$$\mu = [(dI_{ds})/(dV_{bg})] \times [L/(WC_iV_{ds})], \quad (1)$$

where L is the length, W is the width of the BP channel, and C_i is the capacitance between the channel and the back-gate per unit area ($C_i = \varepsilon_0\varepsilon_r/d$; $\varepsilon_r = 3.9$ for SiO_2; d = oxide

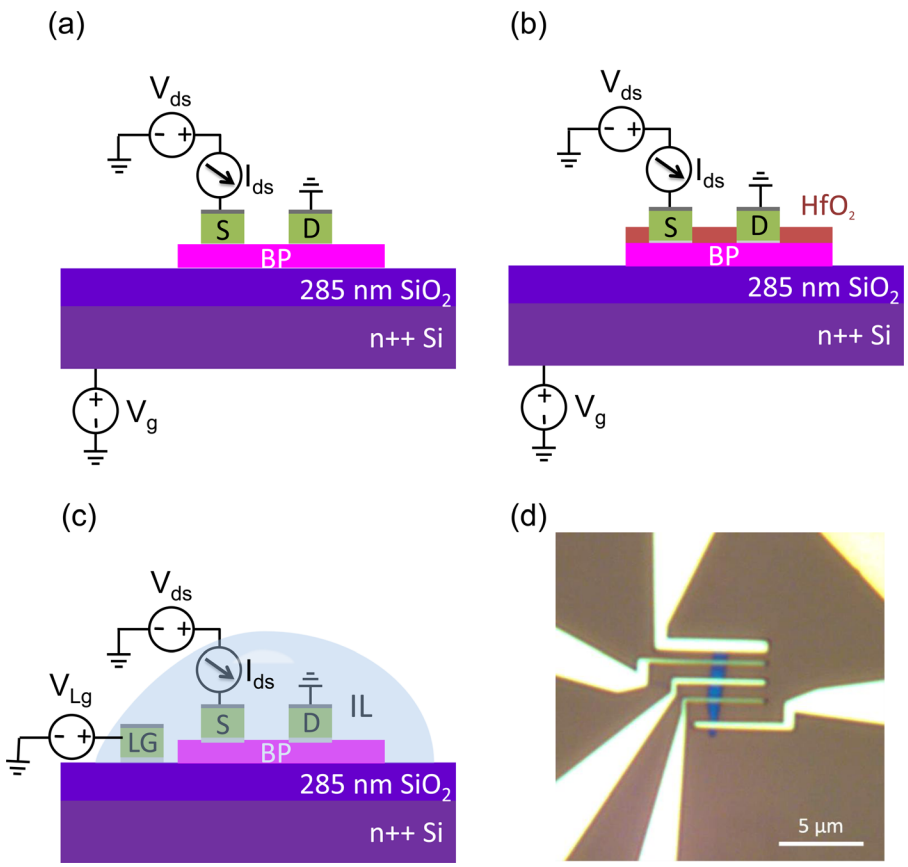

FIG. 1. Nanolayer black phosphorous (BP) field effect device: (a) Schematic of a BP FET with source, drain, and SiO_2/Si back gate. (b) BP FET with HfO_2 top encapsulation layer and source, drain, and SiO_2/Si back gate. (c) BP electric double layer transistor with ionic liquid gate. (d) Optical image of 5 nm thick BP FET with TiO_2 (1 nm)/Co contacts on SiO_2/Si substrate.

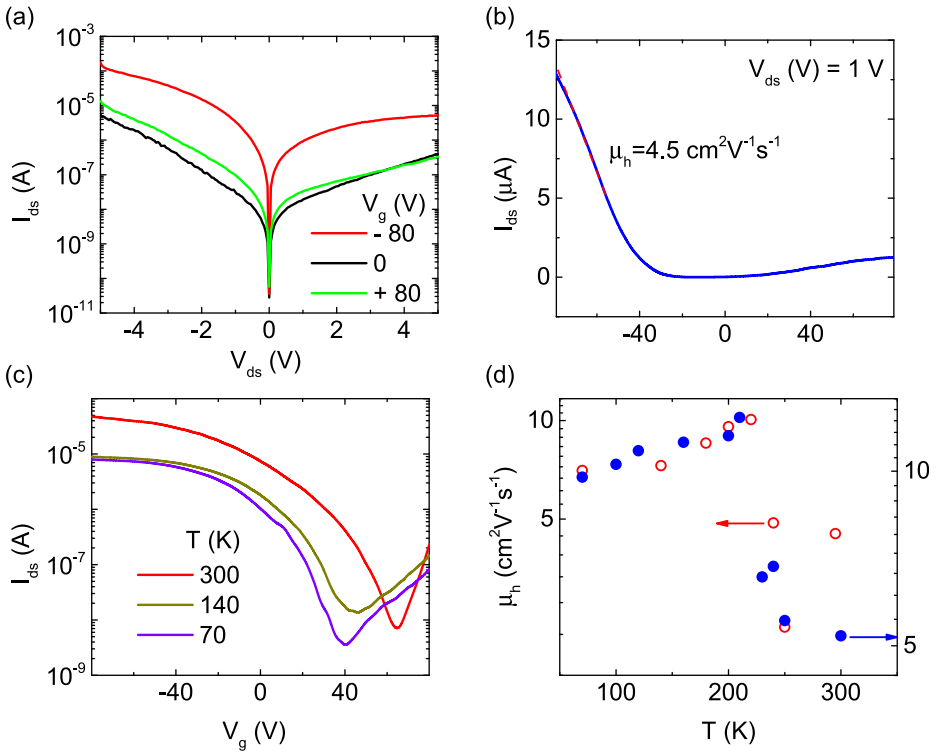

FIG. 2. Characterization of BP FETs. (a) Output characteristics I_{ds}–V_{ds} measured in high bias range for different gate voltages (V_g). (b) Transfer characteristic I_{ds}–V_g for $V_{ds} = 1$ V. The effective field-effect mobility for holes in BP channel is 4.5 $cm^2\ V^{-1}\ s^{-1}$ as calculated from the subthreshold slope of the transfer curves. (c) Transfer characteristics at different temperatures in logarithmical scaling reveal an $I_{on}/I_{off} > 10^4$ for hole and $> 10^2$ for electron conduction regimes. (d) Temperature dependence of the hole mobility for two different BP channels with equal thickness.

thickness of 285 nm). The effective field-effect mobility is found to be ~4.5 $cm^2\ V^{-1}\ s^{-1}$ for holes at room temperature. These devices also show a reasonable transistor on/off (I_{on}/I_{off}) performance $>10^4$ for hole and $>10^2$ for electron conduction regimes. We would like to note that in comparison to the freshly prepared BP FETs[24] although the aged devices showed mobility reduction by more than an order in magnitude, the transistor on/off performance remained unaffected with aging of the devices. Such information of aged BP FETs are important as devices used in practical applications need to perform reliably over a period of time.

We further examined the temperature dependence of the carrier mobility to uncover the factors that could limit the mobility in our BP FETs. Transfer characteristics measured in the temperature range 77 K–300 K are shown in Fig. 2(c). The transistor on/off performance is found to increase slightly at low temperature for both electrons and hole conductions in comparison to the value at 300 K. As displayed in Fig. 2(d), the hole mobility is found to increase with lowering the temperature and saturates below 125 K. Such behavior of the mobility at low temperature is consistent with scattering from charged impurities,[6,24,28] which can be presented on the BP surface or at the BP/SiO_2 interface. The drop in mobility from 200 to 300 K can be attributed to the electron–phonon scattering which is the dominant mechanism at higher temperatures.[6,24,28,29]

BP FET with HfO_2 capping-layer: A high-k dielectric substrate or capping-layer can affect the performance of thin-film transistors. On one hand, the introduction of surface disorder can reduce the charge carrier mobility,[30] and on the other hand, the dielectric screening can enhance the mobility.[5,31] It has been reported that high-k capping-layers on MoS_2 FETs can strongly dampen the Coulomb scattering of the charge carriers.[5] For the case of BP thin-film FETs, unresolved questions about the role of the high-k dielectric substrate and capping-layers still remain. Recently, a transition from p-type to ambipolar behavior of BP has been observed in Al_2O_3 top gated device.[32]

Here, we investigate the effect of a high-k HfO_2 encapsulation on BP transistors with TiO_2/Co source-drain contacts. The output characteristics I_{ds}–V_{ds} revealed linear behavior at small bias voltages with the onset of non-linearity at high V_{ds}. In Fig. 3(a), we present the output characteristics I_{ds}–V_{ds} for different gate voltage (I_{ds} in log scale). Figures 3(b) and 3(c) show the measured transfer characteristics, which are typical for the ambipolar behavior of BP. In comparison to the device without HfO_2 capping layer, we find a shift in the threshold voltage V_{th} for these devices. The effective field-effect mobility at room temperature is found to show an increment to 11.2 $cm^2\ V^{-1}\ s^{-1}$ for hole conduction regimes, which is more than double the mobility obtained without the capping layer.

The temperature dependence of the transfer characteristics was studied to understand the various factors that affect the mobility in our BP channel covered with HfO_2. The transistor on/off performance increases by more than an order of magnitude for both electron and hole conduction at 100 K in comparison to the value at 300 K (Fig. 3(c)). With an on/off ratio up to 10^4 for hole regime and up to 10^2 for electron regime over the entire temperature range, the device showed transistor performance similar to device performance without capping layer. The hole mobility as a function of temperature is shown in Fig. 3(d), which shows a monotonic increase up to room temperature. This is in sharp contrast to the behavior observed for the device without HfO_2 capping, where the mobility showed a down turn (Fig. 2(d)) in phonon limited temperature range closer to 300 K. Such behavior could possibly arise from the dominance of scattering from freshly created charged impurities at the interface of HfO_2 and BP. In addition, the presence of a top layer of HfO_2 can further contribute to the quenching of effective phonon-carrier scattering. Further studies till higher temperatures and theoretical

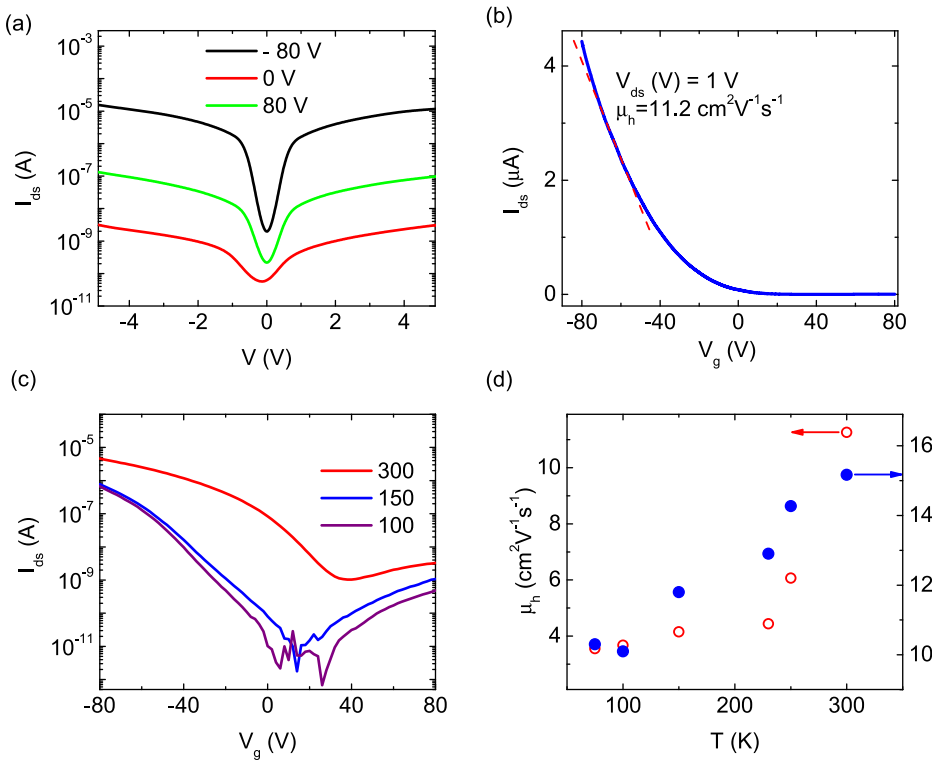

FIG. 3. BP FET with HfO_2 cap layer. (a) Output characteristics I_{ds}–V_{ds} measured for different gate voltages at room temperature (V_g). (b) Transfer characteristic I_{ds}–V_g for different V_{ds} in a linear scaling. (c) Transfer characteristic in logarithmical scaling for $V_{ds} = 1$ V measured at different temperatures. (d) Temperature dependence of hole mobility for two different channels having similar thickness.

modelling could shed light on the exact mechanism of such temperature dependent behavior with HfO_2 on BP.

BP electric double layer transistor with ionic liquid gate: We also examined the effect of an electrolytic gate on the BP transistor performance. The electrolytic or ionic liquid (IL) gate is a unique way to induce high carrier densities in transistor channels. The IL forms an electric double layer at the interface and thus acts as a nano-gap capacitor with an extremely large capacitance.[17] A droplet of ionic liquid (Diethylmethyl(2-methoxyethyl)ammonium bis(trifluoromethylsulfonyl)imide; Sigma-Aldrich: 727679) was applied onto the surface of the BP, also covering a side gate electrode (Schematic Fig. 1(c)). An applied gate voltage drives either anions or cations onto the channel surface under positive or negative bias, respectively. The ions and induced carriers ($\sim 10^{14}\,cm^{-2}$) form an equivalent capacitance of $\sim$1.5 mF/cm^2.[21] Figs. 4(a) and 4(b) show the transfer characteristics of a device measured with a SiO_2 back gate (BG) before applying the IL. The device shows a reliable transistor performance with I_{on}/I_{off} ratio of 10^4, hole mobility $\sim 8.5\,cm^2\,V^{-1}\,s^{-1}$, subthreshold swing (SS) $\sim$ 9 V/dec. Gating with the IL reduced the operating gate voltage considerably to less than 0.5 V compared to that in the SiO_2 BG configuration (80 V) (Figs. 4(c) and 4(d)). The carrier mobility is calculated (using $C_{ILG} = 1.5\,\mu F\,cm^{-2}$) to be around $5.7\,cm^2\,V^{-1}\,s^{-1}$, which is close to $8.5\,cm^2\,V^{-1}\,s^{-1}$ with the SiO_2 BG configuration. An improvement in the SS has also been observed, which reduced drastically from $\sim$9 V/dec in SiO_2 BG device to 170 mV/dec with IL gating. This value of SS is very close to the standard value of 60 mV/dec for commercial Si MOSFET devices.[28] We observe a transistor behavior with good current saturation and a current I_{on}/I_{off} ratio exceeding 10^2 for holes. It is observed that the off-state current has been increased by two orders with IL gate, while the on-state current remains the same. The increase of the off-state current could be due to the fixed charges in the dielectric layer influencing the Schottky barrier at the contacts.[21] Another reason could be due to the role of interface trap density at the BP top surface in contact with the IL gate. The absence of ambipolarity in the IL device has been observed, which may be due to a limited window of gate sweep performed in our measurements. Also the shift of the minimum current to positive voltage can be attributed to the presence of fixed charges at the interfaces. We note that the contacts showed considerable deterioration after 30 min of measurements. Such degradation can be avoided by employing noble metals such as gold or platinum for electrodes or capping layer in future. Our experiments indicate that the electrostatic conditions at the surface of the channel can influence the performance and properties in BP FETs with unique outcomes. We believe that the performance in our devices can be further improved by the use of high quality BP devices using van der Waals heterostructures of BP with 2D dielectric crystals such as hexagonal boron nitride.[33–38]

In conclusion, we have investigated the effect of high-k dielectrics and ionic liquid gating on BP field effect transistors with low Schottky barrier source-drain contacts. With a high-k HfO_2 encapsulated layer on BP, we observed a reliable ambipolar transistor performance with on/off ratio up to 10^4 for the hole regime and up to 10^2 for the electron regime, similar to uncapped devices. However, we observed an increase in mobility with temperature for the HfO_2 capped device indicating some thermal activated transport. This is in contrast to the decrease in mobility at higher temperatures seen in the uncapped BP device due to phonon assisted scattering processes. In the BP electric double layer transistor employing an ionic liquid gate, we observed a drastic improvement in the subthreshold swing (173 mV/dec) and device operation below 0.5 V. Our experiments elucidate that the use of high-k dielectric capping and ionic liquid gate can lead to reliable and improved

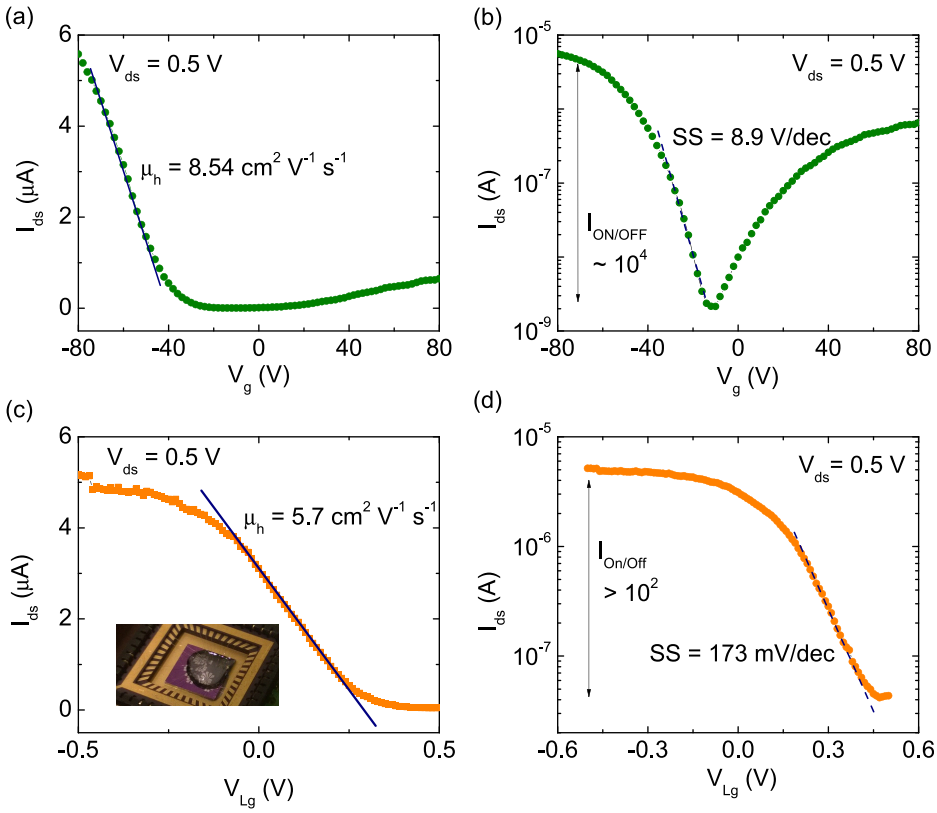

FIG. 4. BP electric double layer transistor with ionic liquid gate (a) BP FETs with SiO_2 back gate before application of ionic liquid. Transfer characteristics of BP FETs with SiO_2 back gate measured at the drain-source bias $V_{ds} = 0.5$ V. (b) the same transfer characteristics as in Fig. 4(a) in log scale. (c) Electric double layer transistor with ionic liquid gate. Transfer characteristics of the BP IL-gated FETs measured at the drain-source bias $V_{ds} = 0.5$ V. Inset—Device of an IL-gated BP FET. (d) The same transfer characteristics as in Fig. 4(c) in log scale.

device performance in BP field effect transistors. This paves the way for BP electronic, spintronic, and optoelectronic devices with electrostatic control of charge carriers by different methods and further exploration of device physics.

The authors acknowledge the support from colleagues of Quantum Device Physics Laboratory and Nanofabrication Laboratory at Chalmers University of Technology. This research was financially supported by Nano Area of Advance program at Chalmers University of Technology, EU FP7 Marie Curie Career Integration grant, and Swedish Research Council Young Researcher Grant.

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