Linearization of dual-input Doherty power amplifiers

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***Abstract*—This paper studies the linearity of dual-input Doherty power amplifiers. We propose a linearization scheme that uses a combination of an efficiency-optimized static splitter and a vector-switched digital predistorter. The performance of the proposed linearization scheme is evaluated on a dual-input Doherty power amplifier operating at 2.0 GHz with 42 dBm peak output power. Experimental results show that the proposed linearization scheme achieves a normalized mean square error of -43.7 dB and an adjacent channel power ratio of -55.8 dBc with a power added efficiency of 42.4%.**

***Index Terms*—digital Doherty, digital predistortion, dual-input Doherty, linearization, power amplifiers.**

I. Introduction

The dual-input Doherty power amplifier (DPA), also referred to as digital Doherty amplifier, is an attractive transmitter architecture for current and future wideband communications systems [1]. A block diagram of a dual-input DPA is shown in Fig. 1. It consists of two parallel amplifiers, a main amplifier and a peaking amplifier, and an impedance inverter network. Unlike single-input DPAs, dual-input DPAs eliminate the analog input splitter, allowing independent control of the input signals to the main and peaking PA. In this way, the input power to both amplifiers can be efficiently distributed so that the power wasted in the peaking branch is minimized when the peaking PA is turned off [1]. In addition to that, the phase relation between branches can be independently controlled at different frequencies thus enabling frequency re-configuration and wider bandwidth implementations [2].

Although improvements in efficiency and bandwidth have been achieved [1], [3], the linearization of dual-input DPAs has not been studied extensively in the literature. In this paper, two aspects of dual-input DPA linearization are studied: power efficiency and bandwidth of the input signals. It is shown that by using a combination of an efficiency-optimized static splitter and a vector-switched digital predistorter, the linearity of dual-input DPAs can be improved while maintaining high efficiency. It is also shown that due to the wide bandwidth of the signals after the static splitter, residual spectral regrowth is found at the output of the amplifier. To circumvent this problem, an improved linearization scheme is proposed. Experimental results show that the proposed scheme can considerably reduce the residual spectral regrowth providing an alternative for the linearization of dual-input DPAs.

This paper is organized as follows. Section II describes the linearization procedure for dual-input DPAs from the derivation of the efficiency-optimized static splitter to the digital predistortion (DPD). Section III presents the measurement setup. Experimental results and discussions are given in Section IV. Finally, the conclusions are provided in Section V.

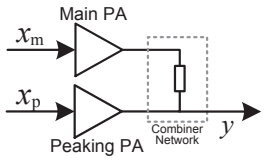


Fig. 1. Block diagram of a dual-input Doherty power amplifier.

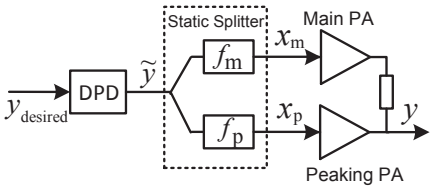


Fig. 2. Linearization scheme for dual-input Doherty power amplifiers.

II. Linearization Technique

As Fig. 1 illustrates, for the operation of dual-input DPAs, two RF input signals have to be designed in the digital domain. The signal design should be made to fulfill two requirements: to provide an output signal that complies with the linearity requirements and that provide high power efficiency. Due to the complexity of fulfilling both requirements simultaneously, the signal design is done in two steps. First, a static splitter is derived to provide input signals that drive the PA in a power efficient way and to compensate the amplifier static nonlinearities. Then, the linearity is further enhanced by adding a digital predistorter before the static splitter, as illustrated in Fig. 2. First the derivation of the static splitter is treated.

A. Static Splitter

In order to ensure high efficiency operation, the optimal combination of input signals x_{m} and x_{p}, as depicted in Fig. 1, has to be identified. This is performed by driving both amplifiers with static continuous wave signals having different combinations of input amplitudes $|x_{\mathrm{m}}|$ and $|x_{\mathrm{p}}|$ and phase differences $\Delta\phi$ between x_{m} and x_{p} and recording the corresponding output signal y and power added efficiency (PAE).

The recorded PAE vs output power is shown in Fig. 3(a), where each blue dot corresponds to a combination of $|x_{\mathrm{m}}|$, $|x_{\mathrm{p}}|$ and $\Delta\phi$. Different combinations of $|x_{\mathrm{m}}|$, $|x_{\mathrm{p}}|$ and $\Delta\phi$ may provide the same output power but with different PAE. Therefore, a search is performed to identify the input signals $|x_{\mathrm{m}}|$, $|x_{\mathrm{p}}|$ and $\Delta\phi$ that maximize the PAE at each output power level, see Fig. 3(a).

In this work, ADS harmonic balance simulations were performed to test several combinations of $|x_{\mathrm{m}}|$, $|x_{\mathrm{p}}|$, and $\Delta\phi$ to obtain initial guesses for the input signals. This reduces

measurement time and the risk to destroy the PA due to high input drive levels.

The resulting efficiency-optimized signals $|x_{\mathrm{m_{opt}}}|$, $|x_{\mathrm{p_{opt}}}|$, and $\Delta\phi_{\mathrm{opt}}$ and output phases $\angle y$ versus output amplitude $|y|$ are shown in Fig. 3(b). Note that, as small phase deviations did not influence the final efficiency, the optimal phase difference was kept constant at 92 degrees.

The relation between $|y|$ and the efficiency-optimized signals, $|x_{\mathrm{m_{opt}}}|$, $|x_{\mathrm{p_{opt}}}|$, $\Delta\phi_{\mathrm{opt}}$ and output phase $\angle y$, are used to define AM/AM and AM/PM corrections for the main and peaking PAs,

$$A_{\mathrm{m}}(|y|) = |x_{\mathrm{m_{opt}}}| \qquad A_{\mathrm{p}}(|y|) = |x_{\mathrm{p_{opt}}}| \tag{1}$$

$$\phi_{\mathrm{m}}(|y|) = -\angle y \qquad \phi_{\mathrm{p}}(|y|) = -\Delta\phi_{\mathrm{opt}} - \angle y \tag{2}$$

where A_{m} and ϕ_{m} are the AM/AM and AM/PM corrections for the main PA; and A_{p} and ϕ_{p} are the AM/AM and AM/PM corrections for the peaking PA.

The corrections in (1) and (2) are approximated using piecewise polynomials. The approximated corrections $\widehat{A}_{\mathrm{m}}$, $\widehat{A}_{\mathrm{p}}$, $\widehat{\phi}_{\mathrm{m}}$, and $\widehat{\phi}_{\mathrm{p}}$ are used to define the static splitter functions f_{m} and f_{p}, in Fig. 2, that map any input signal $\tilde{y}$ to the control signals to main and peaking PAs x_{m} and x_{p}. The static splitter functions are defined by

$$x_{\mathrm{m}} = f_{\mathrm{m}}(\tilde{y}) = \widehat{A}_{\mathrm{m}}(|\tilde{y}|)e^{j(\angle\tilde{y}+\widehat{\phi}_{\mathrm{m}}(|\tilde{y}|))} \tag{3}$$

$$x_{\mathrm{p}} = f_{\mathrm{p}}(\tilde{y}) = \widehat{A}_{\mathrm{p}}(|\tilde{y}|)e^{j(\angle\tilde{y}+\widehat{\phi}_{\mathrm{p}}(|\tilde{y}|))} \tag{4}$$

where $|\tilde{y}|$ and $\angle\tilde{y}$ represent the amplitude and phase of the input signal to the static splitter $\tilde{y}$. Note that, the static splitter functions f_{m} and f_{p} invert the static PA nonlinearity by providing input signals x_{m} and x_{p} to achieve a desired output signal. Therefore, these functions act like an efficiency-optimized quasi-static pre-distorter for the dual-input DPA.

B. Digital Predistortion

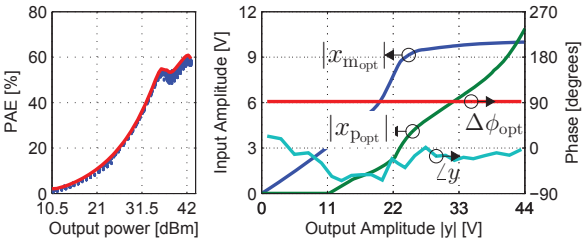
The static splitter cannot compensate dynamic distortions. Therefore, the linearity is enhanced using a digital predistorter, as shown in Fig. 2. Note that the combination of the static splitter and the PA may be considered as single-input-single-output system.

A vector-switched generalized memory polynomial (VS-GMP) is used as model for the DPD [4]. The VS-GMP classifies the input signal into a number of regions based on their amplitudes, and models each region separately. The VS-GMP model is therefore suitable to linearize amplifiers with difficult nonlinearities as is the case for dual-input DPAs [5].

III. Measurement Setup

The measurement setup is illustrated in Fig. 4. A dual-channel arbitrary waveform generator (AWG Agilent M8190A) was used to generate the two RF input signals. The PA output signal was captured using a vector signal analyzer (Agilent N9030A).

The delay mismatch between RF branches at the reference plane *A*, Fig. 4, was determined before the static characterization using an oscilloscope (R&S RTO1044). The delay was



(a) (b)

Fig. 3. Static measurements results (a) PAE vs output power (b) Efficiency-optimized input signals derived from static measurements.

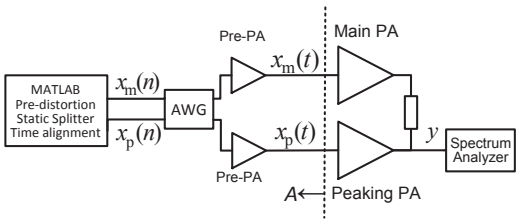


Fig. 4. Block diagram of the measurement setup.

calculated using time-domain cross-correlation followed by frequency-domain phase shift [6]. The delay was compensated before the control signals were uploaded to the AWG.

The amplifier used was the dual-input DPA presented in [3]. The amplifier was operated at 2.0 GHz at a peak output power of 42 dBm. A 5 MHz LTE signal with 8.5 dB peak-to-average power ratio was used in the experiments.

IV. Experimental Results and Discussions

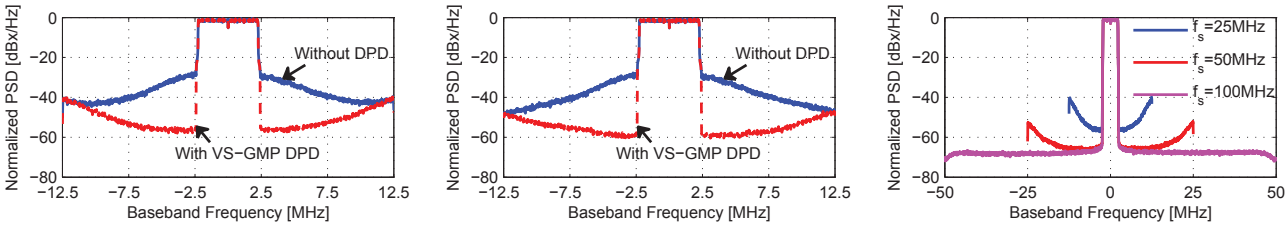
The input signals to the PA were calculated using the static splitter derived in (3) and (4). The model used for the DPD was a VS-GMP with 16 regions, nonlinear order 5, memory depth 3 and cross-term length 1.

Fig. 5(a) shows the spectrum of the output of the amplifier, before and after applying DPD using a sampling rate of 25 MHz. After DPD, the adjacent channel power ratio (ACPR) was reduced from -30.7 dBc to -53.2 dBc with a PAE of 43%. The linearization results are summarized in Table I.

As seen from Fig. 5(a), the output signal spectrum contains residual spectral regrowth towards the edges of the spectrum. This indicates the presence of aliasing distortion in the control signals to the PA. This aliasing distortion is introduced because the sampling rate used in their generation is much smaller than their bandwidth, as shown in Fig. 6 for the control signal x_{m}.

In order to reduce the effects of aliasing distortion, the scheme in Fig. 7 is proposed. The pre-distorted signal $\tilde{y}$, initially upsampled 5 times (5 MHz bandwidth with 25 MHz sampling rate), is upsampled L times before the static splitter. The high sampling rate input signals x_{m} and x_{p} are then lowpass filtered to eliminate any frequency components outside the available bandwidth. After that, the input signals are downsampled to the original sampling rate, to drive the dual-input DPA.

The results obtained using this approach are shown in Fig. 5(b) and in Table I. Compared with the results in Fig. 5(a),



(a) (b) (c)

Fig. 5. Linearization results (a)using the linearization scheme in Fig. 2 and 25 MHz sampling rate, (b) using the linearization scheme in Fig. 7 and 25 MHz sampling rate, (c) using the linearization scheme in Fig. 2 and different sampling rates.

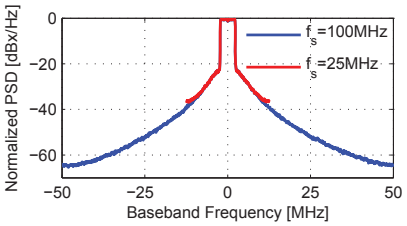


Fig. 6. Spectrum of the input signal to the main power amplifier.

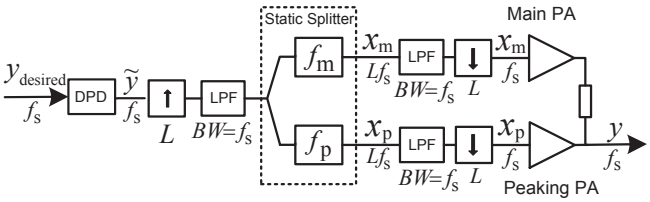


Fig. 7. Linearization scheme proposed to eliminate aliasing distortion caused by the large bandwidth of the control signals x_{m} and x_{p}. f_{s} represents the initial sampling rate, L is the upsampling factor, and BW is the available bandwidth.

the spectral regrowth at 12.5 MHz offset was reduced by more than 9 dB even before applying DPD. The NMSE and ACPR after DPD were further reduced to -43.7 dB and -55.8 dB, respectively. Nevertheless, spectral regrowth is still present at the output signal spectrum.

The remaining spectral regrowth can be either caused by limited linearization capabilities of the model, or bandwidth limitations. In order to test this, measurements using higher sampling rates were used. The results after DPD are shown in Fig. 5(c) and in Table I. Note that the ACPR was reduced by 10 and 11 dB when the sampling rates were increased to 50MHz and 100 MHz, respectively. Moreover, the residual spectral regrowth at the edges of the spectrum was considerably reduced as the sampling rate was increased, reaching the noise floor when 100 MHz was used. Thus, the model has sufficient linearization capabilities, but the limited bandwidth of the signal is causing the residual spectral regrowth. This is a significant finding that requires further investigation.

These results demonstrate that the linearity of dual-input DPAs can be improved using the linearization scheme described in Section II. In order to completely eliminate the spectral regrowth, the linearization requires higher sampling rates. However, high sampling rates are not desired in real applications. This is because they require fast and power hungry digital-to-analog converters (DAC) and analog-to-digital converters (ADC). Consequently, the linearization scheme proposed in Fig. 5(b) may provide an alternative to improve the linearity of dual-input DPAs without increasing the DAC and ADC requirements.

V. Conclusions

The linearity of dual-input DPAs has been studied. It is shown that by using a combination of an efficiency-optimized static splitter and a vector-switched digital predistorter the linearity of the amplifier can be improved by almost 20 dB while maintaining high efficiency. Due to the wide bandwidth of the signals after the static splitter, residual spectral regrowth is still found at the edges of the output signal spectrum. To address this issue, a linearization scheme is proposed to reduce the residual spectral regrowth. The results show that the proposed approach can reduce the residual spectral regrowth by more than 9 dB without increasing DAC or ADC demands.

TABLE I
Summary of the Linearization Results

DPD type	f_s (MHz)	NMSE (dB)	ACPR (dBc)	P_{out} (dBm)	PAE (%)
Splitter [1]	25	-23.5	-30.7	33.3	43.8
VS-GMP [1]	25	-43.1	-53.7	33.4	43.7
Splitter [2]	25	-23.6	-31.0	33.3	42.4
VS-GMP [2]	25	-43.7	-55.8	33.3	42.4
VS-GMP[1]	50	-46.6	-63.6	33.3	43.9
VS-GMP[1]	100	-48.9	-64.7	33.3	43.9

[1]calculated using linearization scheme in Fig. 2.
[2]calculated using linearization scheme in Fig. 7.

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