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Microwave noise characterization of graphene field effect transistors

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The microwave noise parameters of graphene field effect transistors (GFETs) fabricated using chemical vapor deposition graphene with 1 μm gate length in the 2 to 8 GHz range are reported. The obtained minimum noise temperature (T_{min}) is 210 to 610 K for the extrinsic device and 100 to 500 K for the intrinsic GFET after de-embedding the parasitic noise contribution. The GFET noise properties are discussed in relation to FET noise models and the channel carrier transport. Comparison shows that GFETs can reach similar noise levels as contemporary Si CMOS technology provided a successful gate length scaling is performed. [http://dx.doi.org/10.1063/1.4861115]

Graphene[1] is promising as a channel material in high frequency and low noise field effect transistors (FETs). This is a consequence of the unique conical dispersion,[2] with superior mobility (10^5 cm^2/V s) for both type of carriers and intrinsic saturation velocity approaching the Fermi velocity (10^8 cm/s).[3] Since the realization of the first top-gated[4] graphene field effect transistor (GFET) considerable effort has been exerted to push it towards higher frequencies. Nevertheless, issues such as mobility degradation caused by the gate dielectric and underlying substrate[5] or high metal to graphene contact resistance[6] still remain. Hence, only after de-embedding, the highest intrinsic f_{max} and f_T values reported till date for a GFET are 70 GHz (Ref. 7) and 427 GHz,[8] respectively.

In addition to enhancing operating frequencies for envisioned future graphene electronics, it is important to understand the various noise processes in graphene devices. In certain applications, such as direct detectors, graphene benefits directly from its low levels of low frequency 1/*f* noise.[9] On the other hand, when GFETs operate at microwave frequencies in amplifiers, 1/*f* noise is less important and thermally generated noise dominates. In this regime, the performance is quantified by the minimum noise temperature (T_{min}), for high frequency operation a figure-of-merit equally important to f_T and f_{max}. Thus, T_{min} requires to be determined with highest possible accuracy, preferably from device level noise measurements, which provide all four transistor noise parameters.[10] Importantly for device optimization, this enables accurate modeling which separates the thermal noise contributions within the device, intrinsic and extrinsic, contributing to T_{min}. Moreover, it allows the de-embedding of measured noise temperature using correlation matrices.[11] To date, only noise characterization of an amplifier[12] and a resistive subharmonic mixer[13] utilizing GFETs have been reported. The T_{min} of 1 μm GFET made from exfoliated graphene[12] was predicted[10] to be ~330 K and ~75 K at 1 GHz for the extrinsic and intrinsic devices, respectively.

In this paper, results obtained from noise parameter measurements of GFETs using graphene grown by chemical vapor deposition (CVD) are presented. Additionally, noise models of the GFET gate and drain noise, excluding[10] and including[14] correlation, are validated and the results are related to channel carrier transport.

Graphene in this work was grown on copper foil in a cold-wall low-pressure CVD system (Black Magic, AIXTRON Nanoinstruments Ltd.) with CH_4 as precursor gas according to an established recipe.[15] After the deposition, graphene was transferred onto a SiO_2 (300 nm)/Si substrate following a bubbling transfer procedure.[16] The schematic diagram of GFET fabrication steps is shown in Fig. 1. Starting with graphene on the intended substrate (Fig. 1(a)), the GFET patterning was performed using electron beam (e-beam) lithography in four steps. In the first step, source/drain contacts were patterned, 1 nm Ti/15 nm Pd/100 nm Au was evaporated by electron beam and lifted off (Fig. 1(b)). Subsequently, two 1 nm thick Al layers were deposited and oxidized on a hotplate at 170 °C for 5 min (Fig. 1(c)). Mesas were patterned in the next e-beam step. Oxide and graphene were etched around the mesas by HCl and O_2 plasma, respectively (Fig. 1(d)), so that graphene remained only in the active device region. This alignment is crucial to minimize gate leakage current (I_G) and also for drain-source current (I_{DS}) to flow only through the channel and in turn increase transconductance (g_m). The 1 nm Al evaporation and oxidation step was repeated five times for a total thickness of ~10 nm for the Al_2O_3 gate oxide. In the subsequent e-beam step, gate fingers were patterned and 10 nm Ti/300 nm Au was evaporated and lifted off (Fig. 1(e)). In the last e-beam step, larger source/drain/gate pads for

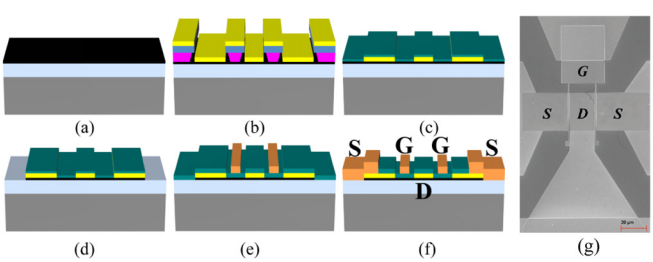

FIG. 1. Schematic of the GFET fabrication steps.

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probing were patterned and oxide was etched from the overlap area of the smaller contacts using HCl. Finally, 10 nm Ti/305 nm Au was evaporated and lifted off (Fig. 1(f)). The gate length was $L = 1\,\mu$m and the device width was $W = 2 \times 30\,\mu$m. A relatively long channel length was chosen to achieve efficient gate modulation. The access length between gate fingers and source/drain contact was $L_a = 100$ nm. The SEM image of a final device is shown in Fig. 1(g). The small signal equivalent circuit of the device is shown in Fig. 2, which is similar to a standard FET equivalent circuit. The gate and drain pad resistances, R_{pg} and R_{pd}, arise from the insufficiently insulating substrate. The intrinsic part of the device is marked by a dashed rectangle in Fig. 2.

The measurements were performed in the 2-8 GHz range using an automated ATN electronic tuner system. The S- and noise parameters were measured at room temperature with an Anritsu 3797C vector network analyzer (VNA) and an Agilent N8975A noise figure analyzer (NFA), respectively, using a multiple impedance configuration. An optimum gate voltage, $V_{GS} = 0.08$ V, yielding the highest possible g_m at a drain bias of $V_{DS} = -1.5$ V and $I_{DS} = 22$ mA was used. The high drain bias results in a difference between the gate source and gate drain voltages, as opposed to a back gate configuration. Still, the bias point is sufficient to the negative side of the minimum conductivity point to result in a majority of hole carriers, unipolar conduction, throughout the GFET channel.[17] The bias is essential to obtain a high enough gain, reducing the uncertainty in the noise measurement. Operating at comparatively lower or higher drain bias either increased the uncertainty or degraded the GFETs by exerting electrical stress. The gate leakage current was $I_G \approx 100$ pA, which is beneficial for a minimum level of shot noise ($\overline{i_{gs}^2} = 2qI_G\Delta f$) and thus negligible contribution at the measured noise level.

The extrinsic f_T (from short circuit current gain $|h_{21}| = 1$) and f_{max} (Mason's unilateral gain $U = 1$) of the GFETs calculated from as-measured S-parameters were on the order of 10.5 GHz and 13 GHz, respectively. The measured and modeled S-parameters of a representative GFET are shown in Fig. 3.

The high frequency noise of a two-port network, such as a FET, is expressed through the noise temperature, T_n. It depends on the source reflection coefficient, Γ_s, presented to the device input according to

$$T_n = T_{min} + \frac{4T_0R_n|\Gamma_s - \Gamma_{opt}|^2}{Z_0(1-|\Gamma_s|^2)|1+\Gamma_{opt}|^2}, \quad (1)$$

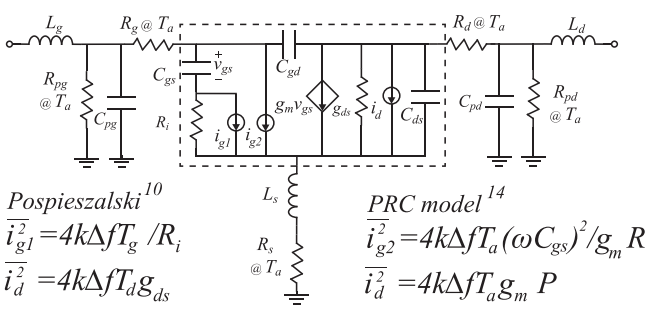

FIG. 2. GFET small signal circuit with noise current definitions. In the PRC model, $Cor = jIm(\overline{i_g \cdot i_d^*})/\sqrt{\overline{i_g^2} \cdot \overline{i_d^2}}$.

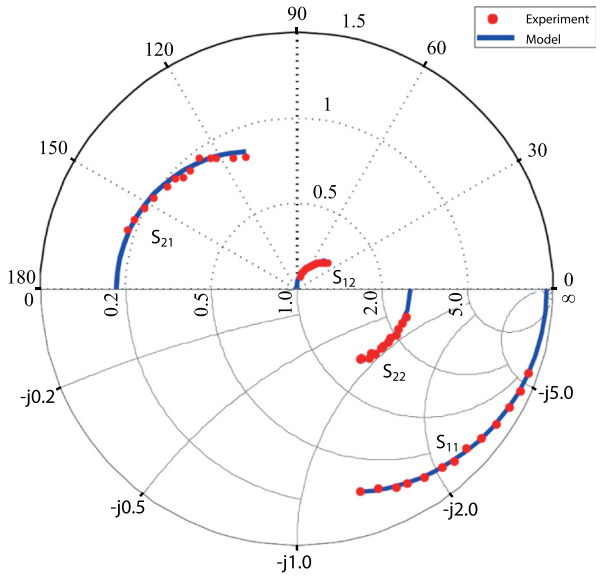

FIG. 3. Measured and modeled S-parameters of the GFET.

where Z_0 is the reference impedance and $T_0 = 290$ K. The noise parameters defined in Eq. (1) are the minimum noise temperature (T_{min}), optimum source reflection coefficient (Γ_{opt}), where $T_n = T_{min}$ is attained, and the noise resistance (R_n) quantifying the sensitivity to increased noise temperature with $\Gamma_s \neq \Gamma_{opt}$. The measured noise parameters, as well as the calculated intrinsic device counterparts after de-embedding device parasitics, are shown in Figs. 4–6, respectively.

The extracted values of the parasitic components of the GFET and the corresponding intrinsic device parameters are listed in Table I. The source and drain contact resistances are expressed as $R_s = R_d = R_a + R_{m-g}$, where $R_a = R_{sheet}\frac{L_a}{W}$ is the resistance coming from the access region unaffected by the top gate and $R_{m-g} = \rho_c/W$ is the metal to graphene contact resistance. R_s and R_d are considered to be equal due to the symmetric device layout. To obtain R_s and R_d, the sheet resistance of graphene, $R_{sheet} = 583\ \Omega/\square$, and contact resistivity, $\rho_c = 76\ \Omega\mu$m, were extracted via transfer length method (TLM) measurements.[18] Although R_{sheet} is considerably higher than the values of highly doped III–V cap layers in HEMTs, the final value $R_s = R_d = 135\ \Omega\mu$m is comparable to state-of-the-art HEMT technology. The gate resistance was obtained to be 54 Ω/mm from DC end-to-end measurement, i.e., measuring the DC resistance of the gate metalization stack and accounting for the small-signal operation

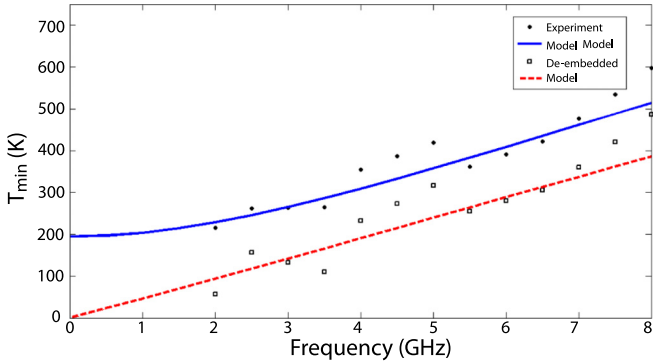

FIG. 4. Measured and modeled minimum noise temperature of the extrinsic and de-embedded GFET.

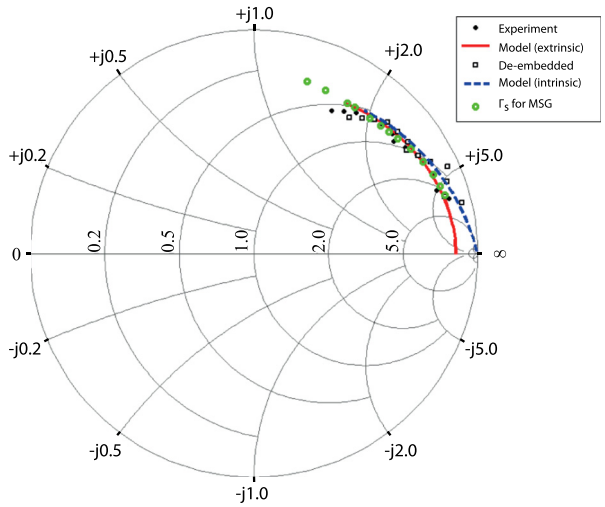

FIG. 5. Measured and modeled optimum source reflection coefficient of the extrinsic and de-embedded GFET.

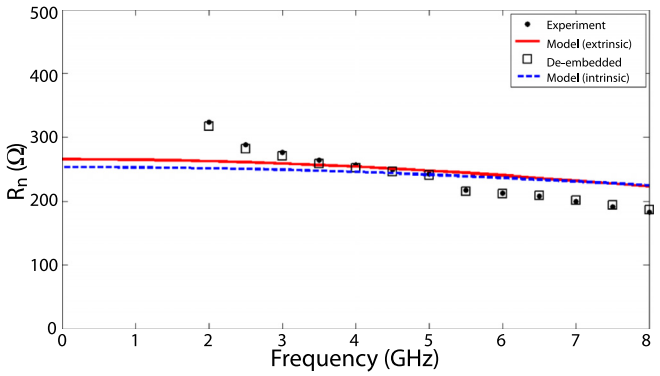

FIG. 6. Measured and modeled noise resistance of the extrinsic and de-embedded GFET.

according to $R_{g,RF} = R_{g,DC}/3$. The remaining parasitic components of the GFET were extracted using separately fabricated open and short structures. From the extrinsic GFET, the parasitics were de-embedded to obtain the intrinsic device parameters using two-port parameter manipulations.[19] Subsequently, the intrinsic noise parameters were obtained by the noise correlation matrix approach.[11] The noise current sources for the drain and induced gate noise are shown in Fig. 2. In the Pospieszalski model,[10] these are described by uncorrelated temperatures T_d of R_{ds} and T_g of R_i. On the other hand, P and R of the PRC model have an imaginary correlation factor jC.[14] The parasitics contribute thermal noise characterized by the ambient temperature, T_a.

Also shown in Figs. 4–6 are the model fits with $T_d = 1950$ K and $T_g = 700$ K, corresponding to $P = 4$, $R = 0.7$, and $C = 0.4$. Ideally in a FET, fluctuations in the drain current and gate voltage are perfectly correlated, $C \rightarrow 1$, which is closely fulfilled in HEMTs under low noise bias.[20] The comparably low correlation in the GFET, despite the excellent aspect ratio $(t_{Al_2O_3}/L_g)$, indicates degraded electrostatics possibly due to traps in the gate oxide. High quality gate stacks are thus essential to increase the cancellation of gate and drain noise[20] and improve the GFET microwave noise level. At the relatively high drain current used, the power dissipation creates an electron temperature above ambient.[21] This is reflected in a gate temperature $T_g > T_a$. The measured noise parameters obey the relation $1 \leq 4G_{opt}R_nT_0/T_{min} < 2$, where $G_{opt} = Re[Y_{opt}]$ and Y_{opt} is the source admittance when $T_n = T_{min}$. Thus, the use of the noise models[10] is validated. The difference between extrinsic and intrinsic T_{min} lies mainly in R_{pg}, which is related to the insufficiently insulating Si substrate, rather than an inherent limitation of GFETs. A related issue is the modeled minimum extrinsic noise temperature ($T_{min,ex}$), which does not go through 0 K at zero frequency (Fig. 4). De-embedding of R_{pg} results in minimum intrinsic noise temperature ($T_{min,in}$) identical 0 K at zero frequency for the GFET. In addition to T_n, also the transistor gain is affected by the input impedance. For comparison, the source reflection coefficient for maximum stable gain (G_{MSG}) is also plotted in Fig. 5. It is apparent that the required Γ_s for maximum gain is close to Γ_{opt} for minimum noise.

To compare the noise performance of GFETs with other technologies, an appropriate frequency, $f = 2$ GHz, is chosen considering the GFETs' f_T and f_{max}. For mature technologies, the device gate lengths are shorter and reported measurement frequencies in the literature are generally higher. Consequently, the normalized figure of merit $T_{min}/f/L$ (K/GHz/μm) is used to enable a more equitable comparison. The comparison of f_T, T_{min}, and $T_{min}/f/L$ of microwave FET technologies with GFETs at $T_a = 300$ K is presented in Table II. In the case of GFETs, $T_{min} = T_{min,in}$ is used in the comparison. For mature technologies, the intrinsic and extrinsic noise temperatures are similar and $T_{min} = T_{min,ex}$ is used.

For GFETs at 2 GHz, $T_{min,ex} = 210$ K and $T_{min,in} = 100$ K (from the model trend in Fig. 4) with $G_a = 10.6$ dB, i.e., the associated gain with the input matched for minimum noise, $\Gamma_s = \Gamma_{opt}$. In comparison to the recent 45 nm Si CMOS technology node[22] using strained silicon and metal gates with corresponding reduction in T_{min}, GFETs show similar performance in terms of noise judging from the $T_{min}/f/L$ values keeping in mind that the improvement in T_{min} saturates at short gate lengths. This requires a successful scaling of the gate length with maintained performance for the GFET. Subtracting the pad noise, the GFET is not yet comparable to GaAs MESFETs[23] or III-V HEMT technologies.[24,25]

A limiting factor for the microwave noise is the reduced carrier mobility in GFETs, in this case the hole mobility $\mu_p = 450$ cm^2/Vs. The mobility indicates device operation in

TABLE I. Extracted parasitic and intrinsic parameters for the small-signal noise model in Fig. 2 with $T_a = 297$ K.

Inductors	pH	Capacitors	fF	Resistors	Ω	Noise models	Ref. 10/Ref. 14	Conductances	mS
L_g	27	C_{pg}/C_{pd}	27/23	R_g/R_i	1/18	T_g/R	700 K/0.7	g_m	16
L_s	10	C_{gs}/C_{gd}	130/86	R_{pg}/R_{pd}	4000/4800	T_d/P	1950 K/4	g_{ds}	8
L_d	70	C_{ds}	5	R_s/R_d	2.2	C	0/0.4		

TABLE II. Room temperature noise performance comparison of FETs. f is the frequency at which T_{min} was measured.

Technology	L (μm)	f (GHz)	f_T (GHz)	T_{min} (K)	$T_{min}/f/L$ (K/GHz/μm)
GFET	1	2	10.5	100[a]	50
Si CMOS[22]	0.045	2	395	6.8[b]	76
GaAs MESFET[23]	0.90	2	10.5	43[b]	24
GaAs pHEMT[24]	0.25	2	100	13.7[b]	27
InP HEMT[25]	0.15	93	186	225.7[b]	16

[a]$T_{min} = T_{min,in.}$
[b]$T_{min} = T_{min,ex.}$

a linear regime, rather than velocity saturation, despite the high average field in the channel $\sim 1.4\,\mathrm{V}/\mu\mathrm{m}$.[17] An upper limit estimate for the carrier velocity is set by the minimum carrier density, $n_0 = 2 \times 10^{12}\,\mathrm{cm}^{-2}$, from thermal generation[2] and substrate impurities,[17] i.e., $v < I_{DS}/(Wqn_0) \sim 1 \times 10^7\,\mathrm{cm/s}$. This is in reasonable agreement with $v_{sat} = 1 - 2 \times 10^7\,\mathrm{cm/s}$ at $T_a = 300\,\mathrm{K}$ ambient with $n = 2$–$10 \times 10^{12}\,\mathrm{cm}^{-2}$ as limited by low energy SiO_2 phonons.[17] This is in contrast to optimum low noise bias for III-V transistors, where V_{DS} and V_{GS} are set for velocity saturation and low I_{DS}, respectively.

An observed mobility increase at cryogenic temperatures in suspended graphene is likely to provide reduced noise temperature, due to the decay of scattering from acoustic phonons. Nevertheless, on SiO_2 substrate mobility is mainly limited by Coulomb scattering from charged impurities with little temperature dependence.[26] Thus, also at cryogenic temperature, the noise performance will be limited by the substrate. Opposed to outer noise limiting mechanisms, inherently graphene has a low density of states close to the Dirac point.[2] This limits g_m for a certain Fermi level shift, with disadvantageous effect on $T_{min} \propto 1/f_T \propto 1/g_m$.[10] Opening of $E_g > 0$ by a nanoribbon channel[2] could boost f_T and thus T_{min} further.

In summary, the device level noise characterization of a GFET at microwave frequencies is reported in this paper. The presented results are comparable with Si CMOS. A key step to improve the noise level is to enhance the channel mobility and reach saturated carrier transport. The substrate is then critical for v_{sat} to be limited only by highly energetic phonons like in suspended graphene.[27] Achieving gain for a wider range of biases enables a more complete study with enhanced measurement accuracy.

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