THESIS FOR THE DEGREE OF DOCTOR OF PHILOSOPHY

Cryogenic Ultra-Low Noise InP High Electron Mobility Transistors

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Abstract

Indium phosphide high electron mobility transistors (InP HEMTs), are today the best transistors for cryogenic low noise amplifiers at microwave frequencies. Record noise temperatures below 2 K using InP HEMT equipped cryogenic low noise amplifiers (LNAs) were demonstrated already a decade ago. Since then, reported progress in further reducing noise has been slow.

 This thesis presents new technology optimization, modeling, measurements and circuit implementation for the cryogenic InP HEMT. The findings have been used to demonstrate a new record minimum noise temperature of 1 K at 6 GHz. The thesis considers aspects all the way from material, process and device design, to hybrid and monolithic microwave integrated circuit (MMIC) LNAs.

 The epitaxial structure has been developed for lower access resistance and improved transport characteristics. By investigating device passivation, metallization, gate recess etch, and circuit integration, low-noise InP HEMT performance was optimized for cryogenic operation.

 When integrating the InP HEMT in a 4-8 GHz 3-stage hybrid LNA, a noise temperature of 1.2 K was measured at 5.2 GHz and 10 K operating temperature. The extracted minimum noise temperature of the InP HEMT was 1 K at 6 GHz.

 The low-frequency $1/f$ noise in the 1 Hz to 1 GHz range and gain fluctuations in the 1Hz to 100 kHz range have been measured for six different types of HEMTs, and compared to two different SiGe heterojunction bipolar transistors (HBTs). The results showed that radiometer chop rates in the kHz range are needed for millimeter wave radiometers with 10 GHz bandwidth.

 A comparative study of GaAs metamorphic HEMTs (mHEMTs) and InP HEMTs has been performed. When integrated in a 4-8 GHz 3-stage LNA, the InP HEMT LNA exhibited 1.6 K noise temperature whereas the GaAs mHEMT LNA showed 5 K. The observed superior cryogenic noise performance of the InP HEMT compared to the GaAs MHEMT was related to a difference in quality of pinch-off as observed in I-V characteristics at 300 K and 10 K.

 To demonstrate the low noise performance of the InP HEMT technology, a 0.5-13 GHz and a 24-40 GHz cryogenic monolithic microwave integrated circuit (MMIC) LNA was fabricated. Both designs showed state-of-the-art low noise performance, promising for future radio astronomy receivers such as the square kilometer array.

Keywords: ALD, cryogenic, DC power dissipation, GaAs MHEMT, gain fluctuations, InP HEMT, LNA, low noise, MMIC

List of publications

Appended papers

The thesis is based on the following papers:

[A]   J. Schleeh, J. Halonen, B. Nilsson, P. Å. Nilsson, L.J. Zeng, P. Ramvall, N. Wadefalk, H. Zirath, E. Olsson and J. Grahn, "Passivation of InGaAs/InAlAs/InP HEMTs using Al_2O_3 atomic layer deposition", in *23rd IEEE International Conference on Indium Phosphide & Related Materials*, IPRM, pp. 63-66, May 2011.

[B]   J. Schleeh, G. Alestig, J. Halonen, A. Malmros, B. Nilsson, P. Å. Nilsson, J. P. Starski, N. Wadefalk, H. Zirath, J. Grahn, "Ultra-low power cryogenic InP HEMT with minimum noise temperature of 1 K at 6 GHz", in *IEEE Electron Device Letters*, vol. 33, no. 5, pp. 664-666, May, 2012.

[C]   J. Schleeh, H. Rodilla, N. Wadefalk, P. Å. Nilsson, J. Grahn, "Characterization and Modeling of Cryogenic Ultra-Low Noise InP HEMTs", in *IEEE Transactions on Electron Devices*, vol. 60, no. 1, pp. 206-212, Jan., 2013.

[D]   H. Rodilla, J. Schleeh, P. Å. Nilsson, N. Wadefalk, J. Mateos, J. Grahn, "Cryogenic performance of low-noise InP HEMTs: a Monte Carlo Study", in *IEEE Transactions on Electron Devices*, vol. 60, no. 5, pp. 1625-1631, May, 2013.

[E]   S. Weinreb and J. Schleeh, "Multiplicative and additive low frequency noise in microwave transistors", accepted for publication in *IEEE Microwave Theory and Techniques*, 2013.

[F]   J. Schleeh, H. Rodilla, N. Wadefalk, P. Å. Nilsson, J. Grahn, "Cryogenic noise performance of InGaAs/InAlAs HEMTs grown on InP and GaAs substrate", in *Solid-State Electronics*, vol. 91, pp. 74-77, Jan., 2014.

[G]   J. Schleeh, N. Wadefalk, P. Å. Nilsson, J. P. Starski, J. Grahn, "Cryogenic Broadband Ultra-Low Noise MMIC LNAs for Radio Astronomy Applications", in *IEEE Microwave Theory and Techniques*, vol. 61, no. 2, pp. 871-877, Feb., 2013.

Other papers

The following papers are not included in the thesis due to overlap in content or a content going beyond the scope of this thesis:

[a]   J. Schleeh, N. Wadefalk, P. Å. Nilsson, J. P. Starski, G. Alestig, J. Halonen, B. Nilsson, A. Malmros, H. Zirath, J. Grahn, "Cryogenic 0.5-13 GHz Low Noise Amplifier with 3 K mid-band noise temperature", in Proceedings of *IEEE MTT-S International Microwave Symposium*, 2012.

[b]   J. Schleeh, P. Å. Nilsson, J. P. Starski, N. Wadefalk, J. Grahn, " InP HEMTs Optimized for Ultra Low Noise Operation", Best paper award at *GigaHertz Symposium, Stockholm, Sweden*, 2012.

[c]   J. Schleeh, H. Rodilla, N. Wadefalk, P. Å. Nilsson, J. Grahn, "Cryogenic Ultra-Low Noise Amplification-InP PHEMT vs. GaAs MHEMT", in *25th International Conference on Indium Phosphide and Related Materials (IPRM 2013)*, p 99-100, 2013.

[d]   H. Rodilla, J. Schleeh, P. Å. Nilsson, J. Grahn, " Optimized InP HEMTs for low noise at cryogenic temperatures", in *24th International Conference on Indium Phosphide and Related Materials (IPRM 2012)*, p 241-4, 2012.

[e]   P. Å. Nilsson, H. Rodilla, J. Schleeh, N. Wadefalk, J. Grahn, "Influence of gate-channel distance in low-noise InP HEMTs ", in *25th International Conference on Indium Phosphide and Related Materials (IPRM 2013)*, p 103-4, 2013.

Notations and abbreviations

Notations

B_{RF} Pre-detection bandwidth
C_{gs} Gate-source capacitance
C_{gd} Gate-drain capacitance
C_{ds} Drain-source capacitance
C_{pg} Gate pad capacitance
C_{pd} Drain pad capacitance
ε_r Relative permittivity
f Frequency
f_{max} Maximum oscillation frequency
f_T Cut-off frequency
g_m Transconductance
G_{ds} Output conductance
G Gain
I_d Drain current
I_{ds} Drain-source current
I_{DD} Drain current to LNA
I_g Gate current
L_g Gate inductance
L_d Drain inductance
L_s Source inductance
μ Mobility
n_s Sheet carrier concentration
q Elementary Charge
R_c Contact resistance
R_d Drain resistance
R_g Gate resistance
Ri Intrinsic gate-source resistance
R_j Intrinsic gate-drain resistance
R_s Source resistance
R_{sh} Sheet resistance
R_{on} on-resistance
T_e Noise temperature
$T_{e,min}$ Minimum measured noise temperature

$T_{e,avg}$	Average noise temperature
T_d	Equivalent drain resistance temperature
T_g	Equivalent gate resistance temperature
T_{min}	Minimum noise temperature
T_{sys}	System noise temperature
V_d	Drain voltage
V_{ds}	Drain-source voltage
V_{DD}	Drain voltage applied to LNA
V_g	Gate voltage
V_{gs}	Gate-source voltage
V_i	Input noise voltage
V_{IN}	Input voltage
V_{OUT}	Output voltage
V_T	Threshold voltage
W	Transistor width

Abbreviations

2-DEG	Two Dimensional Electron Gas
ALD	Atomic Layer Deposition
DSN	Deep Space Network
GaAs	Gallium Arsenide
HBT	Heterojunction Bipolar Transistor
HEMT	High Electron Mobility Transistor
InP	Indium Phosphide
LNA	Low Noise Amplifier
MBE	Molecular Beam Epitaxy
MC	Monte Carlo
MESFET	Metal-Semiconductor Field Effect Transistor
MIM	Metal-insulator-metal
MMIC	Monolithic Microwave Integrated Circuit
NGAS	Northrop Grumman Aerospace Systems
NF	Noise Figure
mHEMT	Metamorphic High Electron Mobility Transistor
PECVD	Plasma Enhanced Chemical Vapor Deposition
SiGe	Silicon Germanium
SKA	Square Kilometer Array
TFR	Thin Film Resistor
TMA	Trimethylaluminium
VLBI	Very Long Baseline Interferometry

Contents

Chapter 1.

Introduction

Human knowledge is expanding in all directions. Astronomers look deeper into space, and physicists discover new quantum particles. As evidence for these findings often consists of ultra-weak electromagnetic signals, the demand for lower noise reception is substantial. To accommodate this advancement, today's ultra-low noise technology needs to be pushed further.

By cryogenically cooling the low noise amplifier (LNA) to around 10 K, thermal noise is strongly reduced. Today, the indium phosphide high electron mobility transistor (InP HEMT) is the established technology for cryogenic ultra-low noise microwave amplification [1]. Record average noise temperature of 1.8 K in a 4-8 GHz LNA was demonstrated already ten years ago [2]. Since then, reported progress in further reducing noise temperature has been absent.

One reason is a shifted research focus toward higher frequencies, with an attempt to overlap the THz gap. Ultra-scaled HEMTs today have gate lengths of 35 nm and below. These HEMTs enable very high frequency of operation, with f_T and f_max approaching 1 THz, but suffer from elevated gate leakage currents, reduced quality of pinch-off, and an increased cryogenic noise temperature at microwave frequencies as a result.

A second reason is that cryogenic LNAs normally are designed with InP HEMTs intended for room temperature operation. Excellent noise performance at room temperature does however not necessarily imply good noise performance at cryogenic temperature [3]. To push the ultra-low noise technology even further, the InP HEMT needs to be directly optimized for cryogenic operation at the intended frequency band.

In this thesis, new state-of-the-art cryogenic ultra-low noise InP HEMT is reported. By using an optimized epitaxial design and HEMT process, state-of-the-art device performance has been achieved for cryogenic amplification up to around 40 GHz.

A number of alternative technologies for LNAs have been reported in the literature. The less expensive metamorphic InGaAs/InAlAs/GaAs HEMT has proven competitive with the InP HEMT with respect to cut-off frequency f_T and noise figure (NF) at room temperature. However, at cryogenic temperature operation, the noise is still considerably higher than the InP HEMT [4]. The more narrow bandgap InAs/AlSb HEMT, with potentially very good low noise properties at extremely low power dissipation, still

suffers from high gate current, high output conductance and impact ionization degrading the noise performance [5]. Also the SiGe heterojunction bipolar transistor (HBT) has been investigated for cryogenic low noise operation. It is suitable for applications requiring extremely stable transconductance g_m, but tolerating higher noise temperature than the InP HEMT technology [6]. An example is the wideband radiometer which becomes gain stability limited by its chopping rate.

In Chapter 2, a description of the low-noise optimized InP HEMT technology is given. The gate recess, a novel passivation method utilizing atomic layer deposition (ALD), and access resistance considerations are discussed, and concluded with an example of a state-of-the-art noise result. In Chapter 3, the InP HEMT technology is analyzed with respect to DC, RF, low-frequency and microwave frequency noise. The characterization is based on both electrical measurements and Monte Carlo (MC) simulations. In Chapter 4, the InP HEMT technology is compared with the similar GaAs mHEMT technology. Finally in chapter 5, the cryogenic ultra-low noise InP HEMT technology developed in this work is demonstrated in a full MMIC LNA process.

Chapter 2.

InP HEMT Technology

The noise performance of the cryogenic LNA is intimately coupled to the transistor in use. A key quest for this thesis is therefore to evaluate how the transistor technology can be improved. The InP HEMT technology is today a technology for high-performance transceivers up to several hundreds of GHz. The unique low noise properties are a result of the high gain and transconductance, in combination with the lateral topology reducing electron scattering (opposite to the HBT vertical topology forcing current through interfaces). However, the properties are not necessarily optimized for cryogenic low-noise applications.

In this Chapter, a state-of-the-art cryogenic low noise InP HEMT technology is presented. Four aspects in the InP HEMT have been subject to study: epitaxial design, gate recess formation, device passivation and access resistances. Their impacts on device performance are temperature dependent, which makes them key components in the optimization of cryogenic InP HEMTs.

The InP HEMTs were formed by mesa etching, ohmic contact formation, gate patterning using electron-beam lithography, followed by contact pad formation, device passivation, and air bridge formation. For more details on the device fabrication, see paper [B].

In the end of the chapter, a record noise result obtained by this InP HEMT technology is demonstrated.

2.1   Epitaxial design

The purpose of the InP HEMT structure is to increase mobility without loss of sheet carrier concentration by separating the free electrons from their donor impurities. At cryogenic conditions, where the electron mean free path is less limited by thermal scattering, impurity locations and geometric boundaries become even more important design properties.

The epitaxial layers, grown from bottom to top on InP substrate, are buffer, channel, spacer (part of barrier), delta doping, barrier and cap. The purpose of the buffer is to overgrow dislocations and defects of the rough InP wafer and enable a crystalline base

TABLE 2.1 EPITAXIAL STRUCTURE OF INVESTIGATED InP HEMTs

	Material	Doping	Thickness
Cap	$In_{0.53}Ga_{0.47}As$	Si: 5×10^{19} cm^{-3}	10-20 nm
Barrier	$In_{0.52}Al_{0.48}As$		8-11 nm
δ-doping		Si: 5×10^{12} cm^{-2}	
Spacer	$In_{0.52}Al_{0.48}As$		3 nm
Channel	$In_{0.65}Ga_{0.35}As$		15 nm
Buffer	$In_{0.52}Al_{0.48}As$		250-500 nm
Substrate	InP		75-100 µm

for the following epitaxial layers. The indium content of the channel should be maximized without introducing too much strain with risk for reduced mobility or even lattice dislocations. The spacer layer thickness must be carefully optimized to completely separate the delta doping from the 2-dimensional electron gas (2-DEG) without loss of sheet carrier concentration and formation of a parasitic channel. The thickness and composition of the barrier layer highly determines the gate Schottky diode, device transconductance, threshold voltage and access resistance between channel and cap layer. The cap layer should be designed with high doping concentration for lowest possible access resistance.

In general the channel is scaled toward higher indium content, and consequently reduced thickness when aiming for high frequency performance. In the same way a reduction of the barrier thickness improves transconductance, but increases capacitance, limits the breakdown voltage and most importantly increases the gate leakage current. The cap layer is limited in thickness due to gate formation difficulties.

The HEMT epitaxial structure used in this thesis were grown on 2" to 4" InP wafers by molecular beam epitaxy (MBE). The epitaxial structures used are shown in TABLE 2.1.

Hall measurements were performed at temperatures between 4 K and 300 K as described in paper [D]. As the majority of the electrons were situated in the highly doped cap layer, this had to be removed to separately measure the channel. The cap removal was done using the succinic acid solution used for the gate recess in section 2.2. The temperature dependence of the electron mobility μ and sheet carrier concentration n_s are plotted in Fig. 2.1 and Fig. 2.2.

At room temperature, μ was measured to 6000 cm^2/Vs with cap, and 12000 cm^2/Vs with cap etched away. When cooled to 10 K, μ improved to 58000 cm^2/Vs with cap, and 66000 without cap. The sheet carrier concentration n_s, with cap, dropped from $19x10^{12}$ cm^{-2} at 300 K to $6.4x10^{12}$ cm^{-2} at 10 K. With cap etched away, n_s was $1.4x10^{12}$ cm^{-2}, independent of temperature.

A STEM image of the cross section of the gate region, with marked epitaxial layers, is shown in Fig. 2.3. The micrograph confirms the thicknesses of the designed layers of the InP heterostructure in TABLE 2.1, and shows no sign of material imperfections. Another InP HEMT cross section, developed by Northrop Grumman Aerospace Systems (NGAS) for high frequency operation at room temperature, is shown in Fig. 2.4 [7]. Compared to the epitaxial structure in this thesis, the structure is observably similar, but the layer thicknesses are much larger.
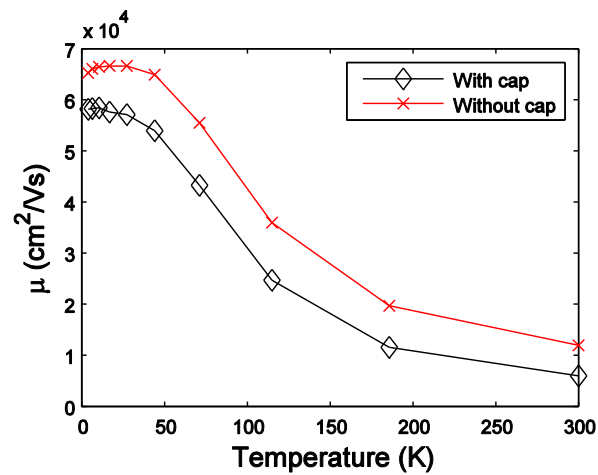
Fig. 2.1. Temperature dependence of electron mobility extracted from Hall measurements of InP HEMT epitaxial structure. The measurement was done both with 20 nm cap layer and with cap etched away using the succinic gate recess solution used in section 2.2. Courtesy of Dr. Helena Rodilla.
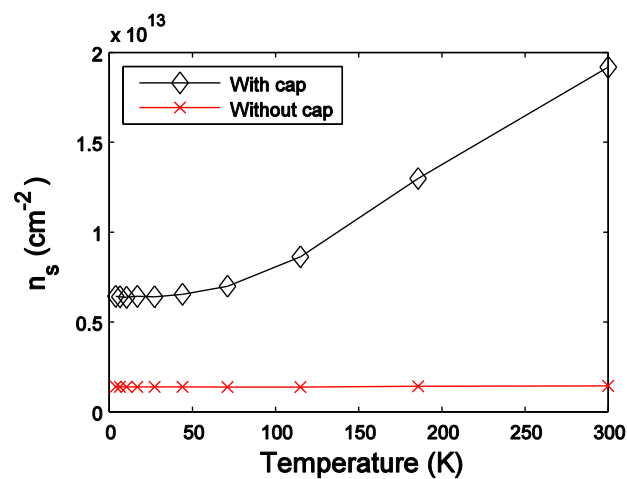

Fig. 2.2. Temperature dependence of sheet carrier concentration extracted from Hall measurements of InP HEMT epitaxial structure. The measurement was done both with 20 nm cap layer and with cap etched away using the succinic gate recess solution used in section 2.2. Courtesy of Dr. Helena Rodilla.

2.2   Gate recess design

The gate recess is by far the most critical step in the InP HEMT process. The main purpose of the recess is to remove the highly doped cap layer before forming the gate. With cap residues left under the gate, the Schottky contact between gate metal and barrier is deteriorated. As a result, gate leakage current levels are increased and gate control is deteriorated.
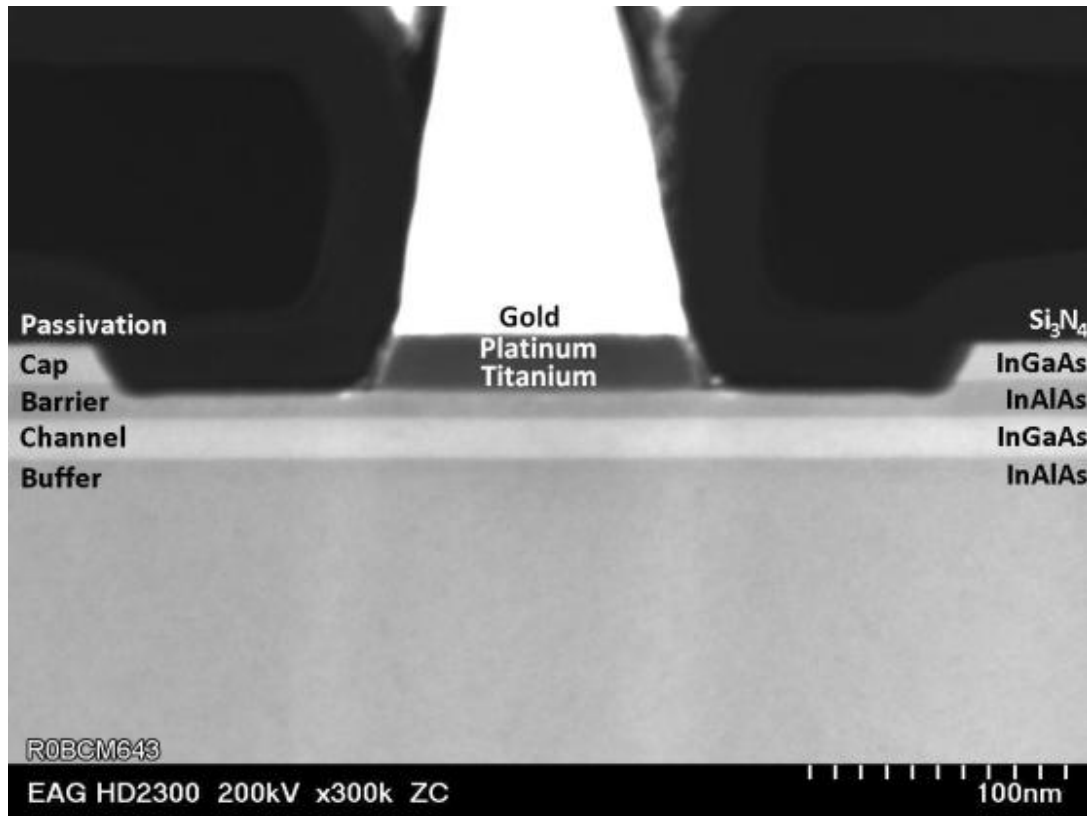
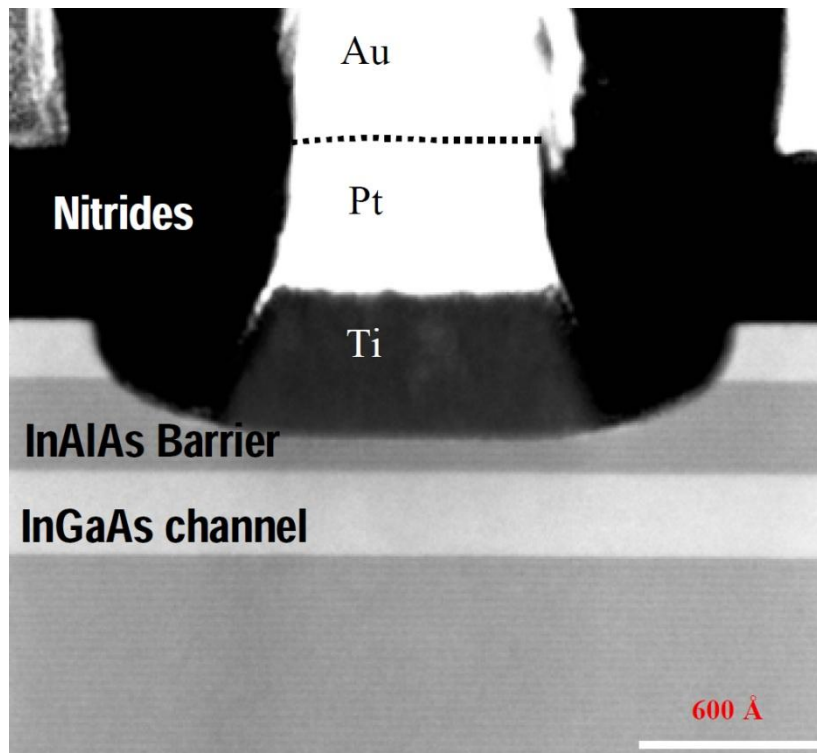Fig. 2.3. Cross sectional STEM image of the gate region of the 130 nm InP HEMT developed in this thesis.

Fig. 2.4. Cross sectional STEM image of the gate region of a 100 nm InP HEMT from Northrop Grumman Aerospace Systems. Compared to Fig. 2.3, the gate recess is more belly shaped due to a different gate recess method. Courtesy of Dr. Richard Lai. [7]

However, even with the entire cap removed, both depth and width of the gate recess influence device characteristics. To avoid unnecessary parasitic capacitance, source, drain and gate potentials need to be separated with a wide enough gate recess. On the other hand, a wide gate recess increases the parasitic access resistance from the contacts to the intrinsic channel. Also the breakdown voltage is affected by the gate recess width as the electric field between the three nodes is increased with decreasing distance.

Another factor limiting the gate recess width, and etch method, is the formation of imperfections and electrical traps deteriorating device performance. By minimizing the recess width, the area with traps is minimized. But to fully suppress their impact, optimized device passivation needs to be performed.

The depth of the recess strongly influences the threshold voltage and the gate leakage current. The closer the gate Schottky barrier is situated to the channel, the more carriers are depleted from the channel, resulting in an increased threshold voltage. Similarly, with a shorter gate to channel distance, the gate Schottky threshold is reduced, meaning a less positive gate potential is needed for a positive gate current. Ultimately, for a useful transistor behavior, the threshold voltage needs to be lower than the gate Schottky threshold voltage; hence giving a limit to the gate recess depth.

In InP HEMT MMIC production, based on carefully extracted transistor models from previous production batches, the gate recess needs to be precisely controlled from wafer run to wafer run. This is done by carefully controlling the etch solution composition, temperature and etch time. If this cannot be done precisely enough, a highly selective etch solution can be used. The selectivity, defined as the ratio between etch speed in the cap and barrier materials, is determined by the relative concentrations of acid and oxidizer in the etch solution. A highly selective etch solution will remove the cap quickly, but slow down when reaching the barrier layer, making etch time less critical. Using a thin InP etch stop layer between the cap and barrier layers can increase the selectivity even further (not done in this work).

For the gate recesses process in this work, a highly selective succinic acid solution was used. The shape of the gate recess can be seen in Fig. 2.3. In Fig. 2.4, showing the NGAS InP HEMT cross section, a non-selective recess etch is used. Compared to the gate recess of the InP HEMTs in this work, which is wide and flat, the recess is much narrower and has a belly shape.

2.3   Device passivation

The surface created by the gate recess is a crystal boundary, with all its defects, located in direct connection with the intrinsic transistor. Passivation of these surface-related defects is of largest importance for the final electric device performance.

The standard passivation method for InP HEMTs is to deposit Si_3N_4 by plasma enhanced chemical vapor deposition (PECVD) [8, 9]. In this thesis, also a new passivation method for InP HEMTs has been tested. The method, atomic layer deposition (ALD) depositing Al_2O_3 is a previously untested passivation method for InP HEMTs. The benefit with ALD compared to PECVD is the inherent thickness control and uniformity [10]. Improved device performance has been reported for ALD Al_2O_3 passivation of AlGaN/GaN HEMTs and GaAs MESFETs [11, 12].

To compare the two methods, pieces from the same test wafer were either passivated with the standard Si_3N_4 PECVD deposited at 300ºC or Al_2O_3 ALD at 250ºC with
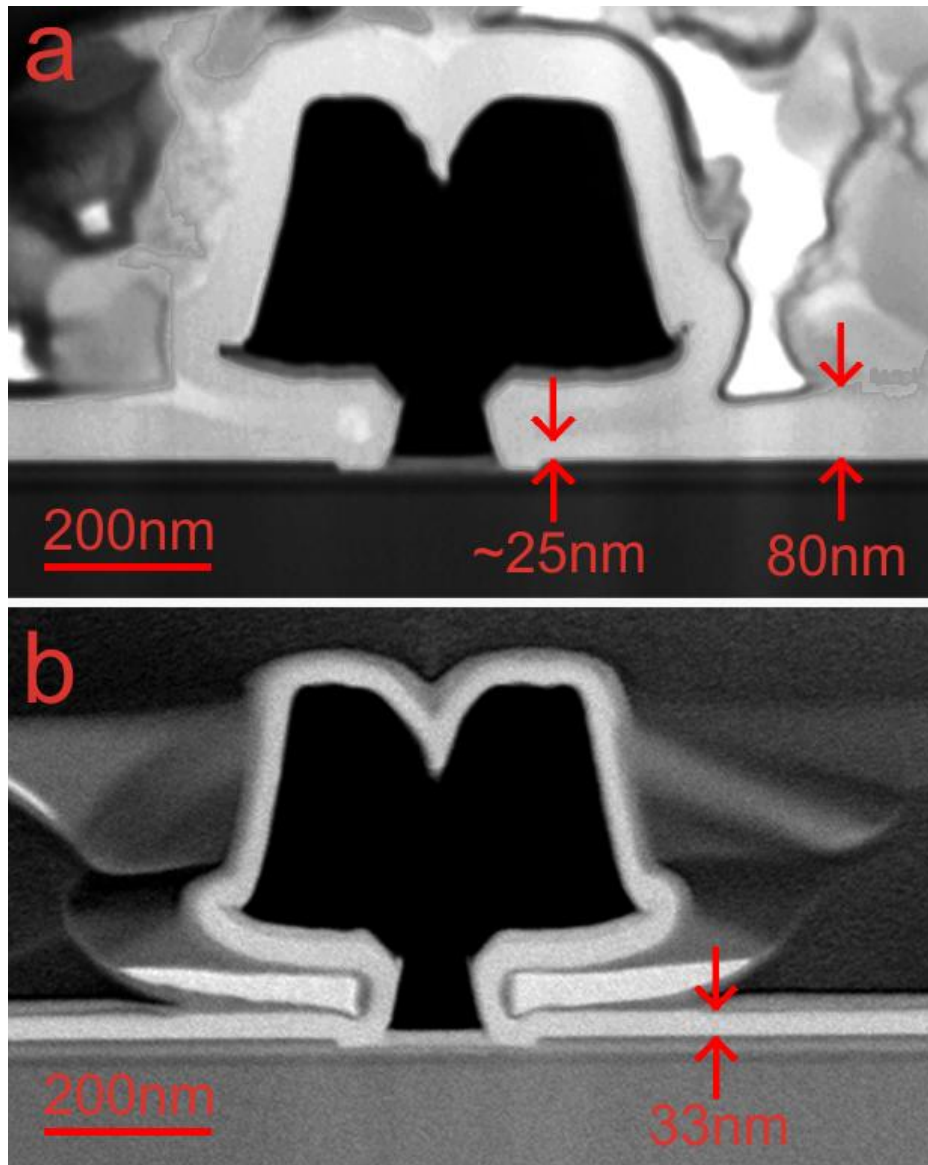
Fig. 2.5: TEM image of the gate region of a) Si_3N_4 PECVD and b) Al_2O_3 ALD passivated InP HEMT. The thickness of the passivation is marked.

trimethylaluminium (TMA) as Al precursor and H_2O as oxygen precursor. Details about the study are given in paper [A].

Fig. 2.5 shows cross sectional STEM images of two InP HEMTs passivated with either the PECVD or ALD method. As seen in Fig. 2.5a, the thickness of the PECVD deposited Si_3N_4 layer was around 80 nm. The ALD passivation was performed in 300 cycles during one hour resulting in a total Al_2O_3 thickness of 33 nm. As seen in Fig. 2.5, the ALD passivation layer was fully uniform, whereas the PECVD passivation layer thickness was reduced at the most important area under the gate hat.

DC measurements were performed both before and after the device passivation. Small-signal microwave measurements were performed after device passivation. I-V device characteristics before and after passivation are shown in Fig. 2.6. The unpassivated InP HEMT typically exhibited a maximum drain current density of 340 mA/mm. The maximum extrinsic transconductance before passivation was 0.6 S/mm at $V_{ds} = 1$ V. The

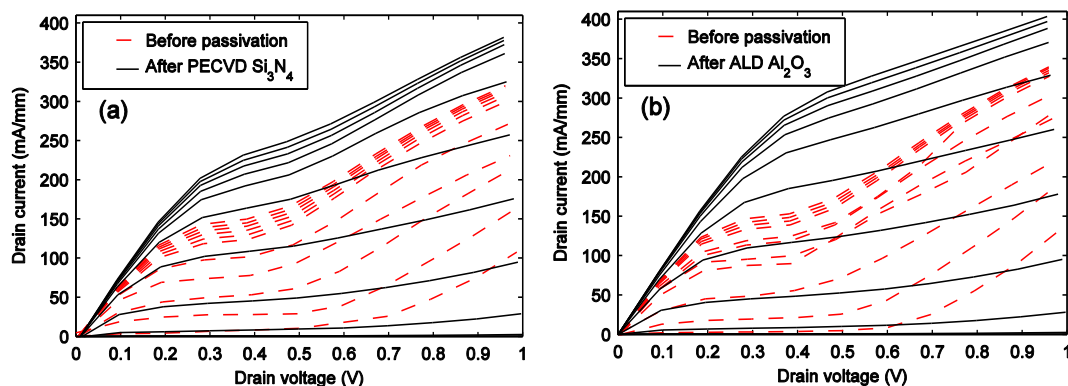Fig. 2.6: I-V characteristics of 2x50 μm InP HEMTs before and after passivation with (a) PECVD Si_3N_4 and (b) ALD Al_2O_3. Gate voltage was swept in steps of 0.1 V from -0.4 V (lower curve) to 0.6 V (upper curve).

gate current was around 1 μA/mm with a dip to 4 μA/mm under impact ionization, which appeared for V_{ds} above 0.8 V. All unpassivated devices showed the same kink phenomena in accordance with [13]. For this low bias region, this is considered to be a consequence of surface traps in the sensitive recess area adjacent to the gate, and not impact ionization.

Irrespective of passivation method, an increase in maximum drain current density with about 20% was observed; see Fig. 2.6. The change in gate current was negligible for both passivation methods. A significant difference between PECVD and ALD passivated HEMTs was observed in the reduction of the kink in the I-V characteristics; As seen in Fig. 2.6, the kink was fully suppressed for the ALD passivated devices whereas only a minor improvement could be seen for the PECVD devices indicating that the ALD is superior to PECVD in passivation of surface traps in the InP HEMTs. One explanation for the superior ALD passivation is the dramatic reduction of Ga^{3+} and As^{3+} oxidation states after the first TMA half cycle of ALD as previously reported in Ref. [14] for $In_{0.2}Ga_{0.8}As$. Similar mechanisms may also be valid for the passivation of the $In_{0.4}Al_{0.6}As$ barrier for the InP HEMTs in this study.

A reduction of the output conductance was evident after both passivation methods. An increase in maximum extrinsic transconductance of about 30% was observed regardless of passivation method.

No obvious difference in C_{gd} (160 fF/mm) and C_{gs} (800 fF/mm) between ALD and PECVD passivated HEMTs was seen. This is explained by the higher relative permittivity of the thin ALD Al_2O_3 ($\varepsilon_r = 9.8$) passivation compared to the thicker PECVD Si_3N_4 ($\varepsilon_r = 7$), resulting in similar effective permittivity. A further reduction of the ALD Al_2O_3 thickness is expected to reduce the parasitic capacitances and enhance the device RF performance.

2.4   Parasitic access resistances

Access resistances are key parameters in the optimization of low noise HEMTs [3]. One reason for superior performance at cryogenic temperatures is the reduction of parasitic resistances with temperature. As the electron-phonon scattering decreases with temperature, both semiconductor and metal sheet resistances decreases. However, as the
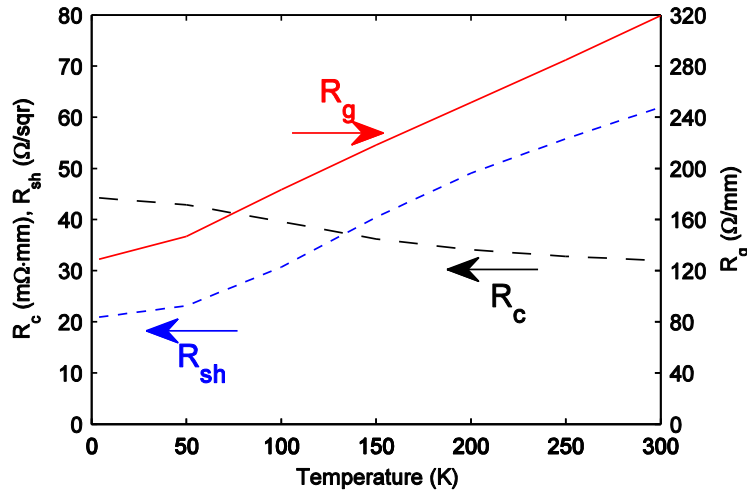
Fig. 2.7: Temperature dependence of R_g, R_{sh} and R_c.

ohmic contact resistance R_c increases with reduced temperature, the total access resistance might not improve at all.

To optimize R_c and the epitaxial sheet resistances R_{sh} for the InP HEMTs the thickness and Si doping of the cap layer was increased from 10 nm and 1×10^{19} cm^{-3} to 20 nm and 5×10^{19} cm^{-3}, respectively. With a metal stack consisting of Ni/Ge/Au and an annealing temperature of 280 °C, R_c of 0.03 Ω·mm at 300 K was obtained. But most importantly as seen in Fig. 2.7, when cooled down to 4 K, R_c only increased incrementally to 0.04 Ω·mm.

The gate resistance R_g, optimized using a 130 nm T-gate technology, decreased from 320 Ω/mm at 300 K to 120 Ω/mm at 4 K. Also R_{sh} was improved from 60 Ω/□ at 300 K to 20 Ω/□ at 4 K. Notable is that R_{sh} and R_g decrease linearly between 300 K and 50 K, where they start to saturate. This means that at temperatures below 50 K the main limitation for the carrier mobility is not phonon scattering, but rather boundary scattering as the mean free path of the electrons becomes comparable to the geometrically small gate and epitaxial dimensions.

It is observed that R_c and R_{sh} obtained in this work are 40-60 % and 50-70%, respectively, better than an optimized 100 nm gate length GaAs MHEMT technology with a very similar temperature dependence [4]. R_g is observed to be similar to [4].

The resulting source and drain resistance R_s and R_d, used in small signal modeling, was 0.13 Ω·mm and 0.14 Ω·mm at 6 K, and 0.24 Ω·mm and 0.26 Ω·mm at 300 K, respectively.

2.5   State-of-the-art ultra-low noise InP HEMTs

Utilizing the reported above, a new state-of-the-art 130 nm gate length ultra-low noise InP HEMT could be demonstrated, see paper [B]. Key changes were the increase of cap thickness and doping, improved gate recess using highly selective succinic acid and optimized ohmic contacts with small temperature dependence. Since no systematic study on the InP HEMT temperature dependence for different device passivations was carried out, the standard PECVD Si_3N_4 passivation was eventually chosen for the optimized ultra-low noise InP HEMT
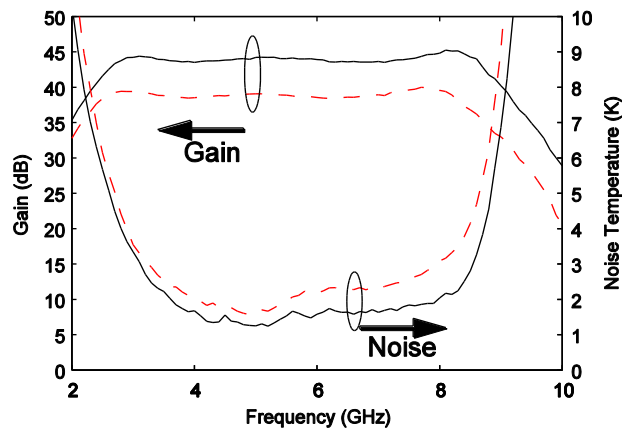
Fig. 2.8: Comparison of gain and noise temperature between 4x50 um InP HEMTs in this study (black curves) and previous state-of-the-art Cryo3 InP HEMTs [2] (red curves) measured at ambient temperature of 10 K in the same LNA in the same measurement system. The amplifier was in both cases biased at optimum low noise bias. Bias for the InP HEMTs in this thesis work was Vd=0.45V and Id=9.3mA. Bias with Cryo3 InP HEMTs was Vd=0.6V and Id=10mA.

The noise temperature and gain as a function of frequency at 10 K of a 4-8 GHz LNA equipped with these 130 nm InP HEMTs is shown by the solid black curve in Fig. 2.8. [2]. A lowest noise temperature $T_{e,min}$ of 1.2 K was measured at 5.2 GHz. Across the 4-8 GHz band, the average noise temperature $T_{e,avg}$ was 1.6 K. Moreover, the average gain of the amplifier was 44 dB, with input and output return loss better than 15 dB, in the entire band. The total power consumption of the LNA at the optimum low noise bias was only 4.2 mW. The extracted T_{min} at 10 K, shown in Fig. 2.9, was 1 K at 6 GHz.

When the LNA was biased for ultra-low power consumption of 0.33 mW ($V_{DD} = 0.1$ V, $I_{DD} = 3.3$ mA), the in-band noise temperature and gain still exhibited numbers of 2.5-4.3 K and 27-34 dB, respectively. At room temperature, the measured LNA noise temperature was typically 25-30 K with a gain of 44 dB at a power consumption of 56 mW ($V_{DD} = 1.25$ V, $I_{DD} = 45$ mA).

In TABLE 2.2, the results are compared to previously published state-of-the art LNAs operating in the same frequency band at 10-15 K ambient temperature. When equipped with the InP HEMTs from this work, the 4-8 GHz LNA exhibited a significantly lower $T_{e,min}$ and $T_{e,avg}$ than previously published results. The difference in gain per mW dissipated power was even larger, and almost a factor of two higher than the second best result [15].

As the measured noise temperature of cryogenic LNAs is extremely low, measurement uncertainties make indirect comparisons between different labs difficult. To validate the state-of-the-art result, 100 nm gate length InP HEMTs with 4x50 μm device size used in [2] (Cryo3 devices) were benchmarked against the InP HEMTs in this thesis using the same 4-8 GHz LNA and identical measurement procedure. The comparison, measured at the optimum low noise bias point of each HEMTs at 10 K, is shown in Fig. 2.8. The average noise temperature with the Cryo3 InP HEMTs was 2.2 K with an average gain of 39 dB. Hence 0.6±0.1 K better LNA noise performance was obtained when equipped with InP HEMTs from this thesis compared to the Cryo3 InP HEMTs used in [2].

The superior low noise performance of the InP HEMT is believed to be a result of the optimized epitaxial structure and gate recess resulting in high transconductance and f_T at low drain current. Also the low access resistances were a prerequisite for this low noise temperature. Finally the low gate current enabled the InP HEMTs to perform well at very

TABLE 2.2
DATA FOR STATE OF THE ART 4X50 μM INP HEMT LNAS AT 10-15 K

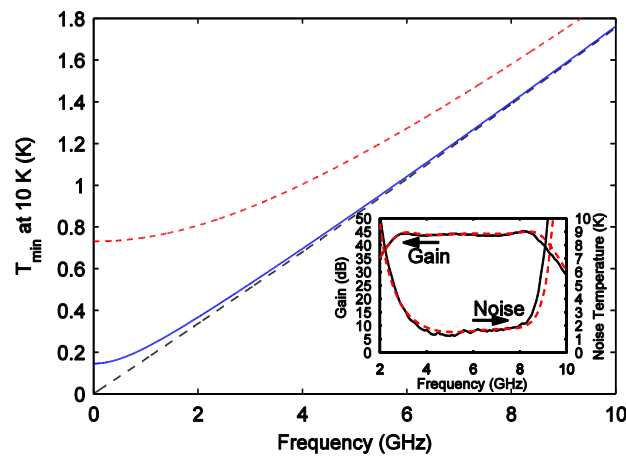| Ref.	Freq. (GHz)	$T_{e,min}$ (K)	$T_{e,avg}$ (K)	Gain/stage (dB)	Gain/power (dB/mW)
This work	4-8	1.2	1.6	14.7	10.5
[2]	4-8	1.4	1.8	13.5	2.5
[15]	4-8	3.1	3.5	13.5	6.8
[16]	4-12	3.3	4.5	11.3	-
[17]	4-12	2.7	3.5	13.7	1.7

Fig. 2.9: Extracted T_{min} of a 4x50 μm InP HEMT exhibiting 20 nA/mm gate current at 10 K (blue solid) compared with the same device without gate current (black long dash) and with 0.5 μA/mm gate current (red short dash). The InP HEMT was biased at $V_{ds} = 0.35$ V and $I_d = 3.1$ mA. Inset shows a comparison between simulated (red dashed) and measured (black solid) noise temperature and gain of the 3-stage LNA using an extracted transistor model.

low frequencies where shot noise from the gate Schottky barrier normally limits performance. In Fig. 2.9 the importance of low gate current is emphasized by showing two modeled InP HEMTs either with zero gate current or with a representative gate current of 0.5 μA/mm.

2.6 Conclusions

Ultra-low-noise InP HEMTs with 130 nm gate length have been designed and fabricated for cryogenic temperature operation. The epitaxial structure has been developed for high mobility and sheet carrier concentration, in combination with minimized access resistances. The gate recess has been optimized for high gate control, low gate leakage current and process repeatability. Compared to the InP HEMT produced by NGAS, the gate recess in this thesis work was flat and wide due to the selective etch method.

   Different passivation methods were tested. The ALD method better removed trap related I-V-kinks than the PECVD passivation. With respect to RF, no significant difference was found.

   Based on noise measurements of a 4-8 GHz 3-stage hybrid IF LNA, extracted T_{min} of an InP HEMT fabricated in this thesis work was 1 K at 6 GHz.

Chapter 3.

InP HEMT Characterization

To characterize InP HEMTs with respect to low noise under cryogenic conditions around 10 K is a complex task. There are several noise sources in the InP HEMT which exhibit both bias and temperature dependence.

This Chapter starts with a brief background to the noise sources in an InP HEMT. A differentiation between low-frequency and microwave noise characterization is done. After this, the Monte Carlo (MC) simulation method is shortly described. The MC simulations, based on experimental results, are used to explain the mechanisms behind the intrinsic transistor behavior. Following, the DC and microwave characteristics, and how they are related to noise performance are discussed. Finally, the chapter is ended with noise results and discussions both related to low-frequency and microwave noise properties.

3.1   Noise sources in the InP HEMT

The most important physical noise sources in semiconductor devices are thermal noise, generation-recombination noise, shot noise, hot-electron noise and low-frequency ($1/f$) noise [18]. Depending on application and operation, each and every one of these noise sources can be anything from negligible to the solely dominant source. For InP HEMTs, at high frequencies >20 GHz, the hot-electron noise and thermal noise from the heavily scaled transistor geometries are the dominant sources. At intermediate frequencies between 1 and 20 GHz, also shot noise from the gate Schottky diode can become a strong noise source if gate leakage current is present. At even lower frequencies, below 1 GHz, the low-frequency $1/f$ noise becomes dominant. Moreover, at room temperature, the thermal noise contribution is strong for all frequencies above the $1/f$ noise limit, while its contribution at cryo temperatures is strongly reduced. In this thesis, a distinction between the low-frequency $1/f$ noise and microwave frequency noise characterization is made.
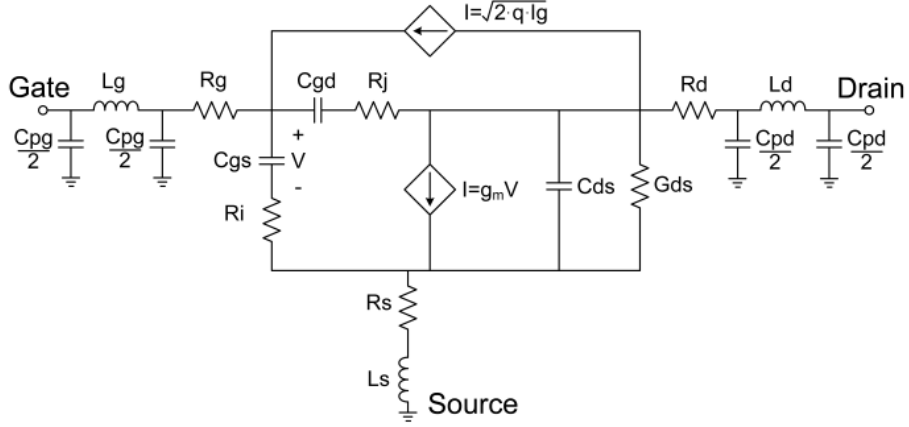
Fig. 3.1: Equivalent circuit of InP HEMT.

3.1.1   Microwave noise

To predict the microwave noise behavior of InP HEMTs in relation to frequency, bias and ambient temperature, noise models based on small signal parameters are widely used [3, 19, 20]. In Fig. 3.1 the small signal model used for the InP HEMTs in this work is shown. For this model, omitting the gate current, an expression for the minimum noise temperature T_{min} was suggested by Pospieszalski [20]. If all resistive elements in the small signal model are equipped with temperatures and all noise sources are treated as thermal noise sources, an expression for the minimum noise temperature is obtained:

$$T_{min} \approx 2\frac{f}{f_T}\sqrt{R_t T_g G_{ds} T_d} \qquad (1)$$

$R_t = R_s + R_g + R_i$, G_{ds} is the output conductance and T_g and T_d are the gate and drain resistance temperatures respectively. T_g is usually set to ambient temperature while the T_d should be considered as a nonphysical fitting parameter accounting for the bias dependent hot electron noise contribution. In opposite to previous models, this model takes the drain current dependent hot-electron noise into consideration

In [3] only f_T and T_d, among the parameters in (1), are considered to be strong functions of transistor bias. Hence, the optimal bias for low noise operation is obtained by minimizing the value of

$$f(V_{ds}, I_{ds}) = \frac{\sqrt{I_{ds}}}{g_m} \qquad (2)$$

as T_d to a first approximation is proportional to I_d and f_T is proportional to the transconductance g_m.

To account for the shot noise generated by the gate leakage in an InP HEMT a noise current source can be added to the small signal model in Fig. 3.1. At low leakage currents the shot noise can be treated as ideal Schottky noise and its contribution be estimated as

$$i = \sqrt{2qI_g} \qquad (3)$$

where q is the elementary charge and I_g is the measured gate leakage current.

3.1.2 Low-frequency noise and gain fluctuations

The low-frequency noise (also called $1/f$ noise, flicker noise or additive noise) has a power spectrum which varies inversely with frequency. The source of the noise is attributed to electrons trapped and released by lattice defects, impurities, and surface states [21, 22].

The gain fluctuation noise, also termed as multiplicative noise, is less well known but is an important factor for radiometer sensitivity and phase noise of oscillators [23]. It is the random fluctuation of the gain of a transistor and is small, of the order of 10^{-4} to 10^{-6} normalized to the average gain. It has a $1/f$ spectrum similar to that of the low frequency noise.

Since the transistor gain is a function of bias point, and the low-frequency noise affects the bias point, there is a coupling between $1/f$ noise and gain fluctuations. This coupling depends upon the type of bias circuit, i.e. in the case of FET transistors, constant gate voltage bias or constant drain current bias.

To understand the low frequency noise and gain fluctuations, the output voltage of a noisy amplifier can be written as,

$$V_{OUT} = G \cdot (V_{IN} + V_i) \qquad (4)$$

where V_{OUT} is the rms output voltage, G is the voltage gain of the amplifier, V_{IN} is an applied rms input voltage from a source, and V_i is the input noise voltage of the amplifier. The gain fluctuation, ΔG, is exposed by applying $V_{IN} \gg V_i$ and normalizing to a measured V_{OUT} to give,

$$\frac{\Delta G}{G} = \left.\frac{\Delta V_{OUT}}{V_{OUT}}\right|_{V_{IN} \gg V_i} \qquad (5)$$

The input noise voltage, V_i, is determined by setting the applied source voltage to zero and measuring the rms output voltage to give

$$V_i = \left.\frac{V_{OUT}}{G}\right|_{V_{IN}=0} \qquad (6)$$

This input noise voltage includes the thermal noise of the source, which needs to be subtracted from the measurement.

Radiometer Sensitivity Degradation

The rms sensitivity, ΔT, of a Dicke radiometer, per root Hz of post detection bandwidth (equal to $1/(2\tau)$ where τ is the integration time), can be expressed as

$$\frac{\Delta T}{T_{sys}} = 2 \cdot \sqrt{\frac{2}{B_{RF}} + 4 \cdot W \cdot S \cdot N \cdot \left(\frac{\Delta G}{G}\right)^2} \qquad (7)$$

where T_{sys} is the system noise temperature, B_{RF} is the pre-detection bandwidth, $\Delta G/G$ is the fractional voltage gain fluctuation per root Hz, N is the number of stages, W is a transistor width scaling factor, and S accounts for the feedback stabilization of gain of each stage. This equation, and the realization that that the power gain fluctuation squared, $(\Delta G_p/G_p)^2 = 4(\Delta G/G)^2$, is described in previous works [24, 25].

The factor W is the ratio of transistor width used for fluctuation measurement (i.e. 200um) to width of transistors used in the radiometer and results from the consideration that transistor in parallel will add ΔG as root sum squares while G adds linearly; thus, $\Delta G/G$ increases as root W. The factor N is due to cascading of stages and increases $\Delta G/G$ as root N. The factor S is due to feedback stabilization in an amplifier where the feedback may be due to source inductance or drain to gate capacitance. It is best determined by a circuit simulation where g_m is varied and the resulting change in S21 is computed.

It is convenient to express the radiometer sensitivity degradation, D, in terms of the ratio of ΔT to the value with no gain fluctuation,

$$D = \sqrt{1 + 2 \cdot W \cdot S \cdot N \cdot B_{RF} \cdot \left(\frac{\Delta G}{G}\right)^2} \qquad (8)$$

As a realistic example of a millimeter wave radiometer with $W=200/40$, $S=0.6$, $N=9$ stages, $B_{RF}=10$ GHz, and $\Delta G/G = 20$ppm at 1 Hz and 2ppm at 1 kHz, we find $D=9.3$ and 1.2 respectively. Note that the degradation does not depend upon integration time; it depends upon $\Delta G/G$ at the chop rate of the radiometer. Given the $1/f$ dependence fast chopping rates are needed for wide bandwidth radiometers.

3.2   Monte Carlo simulations

The MC simulation method is a powerful technique to understand the physical mechanisms behind the InP HEMT operation [26-30]. As the method simulates the electron movements and interactions in the time domain, it can also accurately predict noise performance. This, in combination with accounting for the ballistic transport, present in these devices due to the high mobility of the channel, makes MC the most appropriate simulation technique for studying low-noise properties of InP HEMTs.

The simulations can safely be performed in a two-dimensional environment as the device is homogeneous along the gate width. The MC simulator used in this work, developed by Dr. Rodilla and further described in paper [D], is a development of a previously established 300 K simulator [29, 31, 32].

The conventional operating temperature of cryogenic LNAs is 4-15 K. Due to quantum effects, the MC simulations could not be performed with accuracy at equally low temperatures. Instead, 77 K was chosen due to the large quantity of experimental material data available at this temperature. For the DC and RF experimental behavior of the cryogenic InP HEMT, there is little difference between 77 K and 10 K operation.
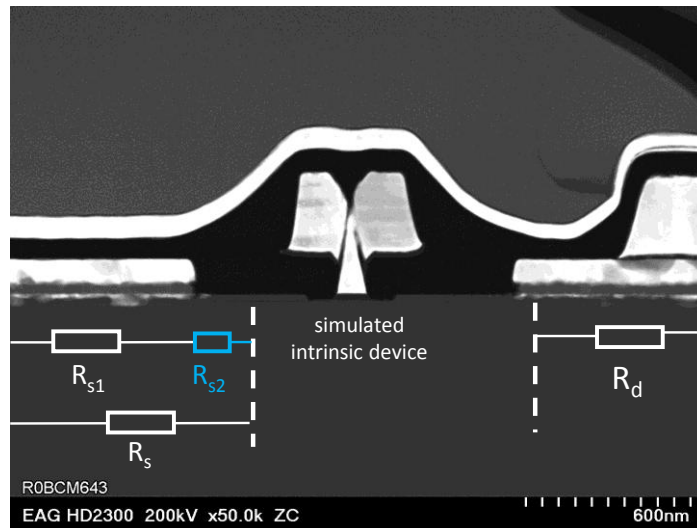
Fig. 3.2. STEM image of the InP-HEMT showing the separation between intrinsic simulated area and external resistances.

To reduce simulation time, only the intrinsic part of the InP HEMT was simulated. The extrinsic part, beyond the limit where it could be treated as simply parasitic resistive, lumped resistive elements contributing to external source and drain resistances were used, see paper [D] for details. A STEM image of the InP HEMT, showing the separation between simulated intrinsic region and external resistances, is shown in Fig. 3.2.

To reproduce the surface charges appearing in the semiconductor/passivation interface on the cap and recess surfaces, a constant surface charge model was considered. The charge denseties in these surfaces were calibrated against the experimental Hall measurements in Fig. 2.1 and Fig. 2.2. The surface charge in the gate recess area was observed to depend on etching process used in the HEMT fabrication.

3.3   DC Characterization

DC and RF characterization was performed at 10 K and 300 K in a Lakeshore model CRX-4K cryogenic probe station. Typical drain current I_d for 2x10 μm gate width devices are shown in Fig. 3.3. Maximum I_d at $V_{ds} = 1$ V was 1 A/mm at 10 K and 0.8 A/mm at 300 K.

At 10 K, a kink is seen in the I–V characteristics at high I_d. Such behavior has been observed previously [1] when operating InP HEMTs at elevated drain currents under cryogenic conditions. However, since the optimal low-noise bias point of the InP HEMT is around 15 mA/mm, i.e. 1.5% of the maximum I_d, the kink phenomenon is far from the bias region of interest for most low noise amplifiers.

In Fig. 3.4, extrinsic DC g_m at 10 K and 300 K is shown against gate voltage V_g. A distinct shift of 0.1 V in threshold voltage V_T, as well as an increased slope of g_m, and improved quality of pinch-off was observed when cooling down to 10 K. Maximum extrinsic g_m at $V_{ds} = 1$ V was 1.8 S/mm at 10 K and 1.4 S/mm at 300 K.

Both Fig. 3.3 and Fig. 3.4 show the traditional way to plot DC behavior of transistors. For ultra-low noise InP HEMTs, the amount of information available from these graphs is however limited. From equation (2), we know that high g_m is important. However, to be utilized for low noise, the same bias point also needs to deliver low I_d. A better way to
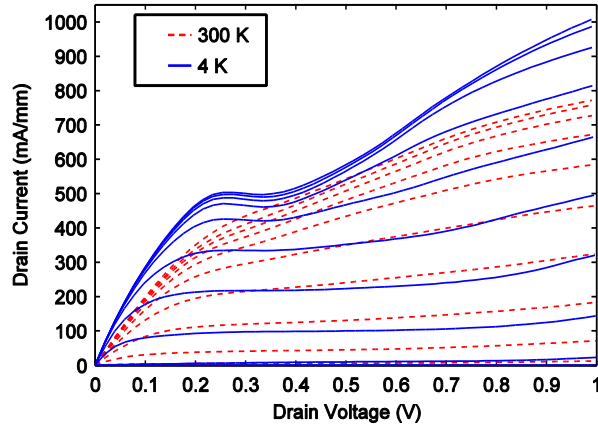
Fig. 3.3: Drain current of a 2x10 µm gate width and 130-nm gate length InP HEMT at 300 K (red dashed) and 10 K (blue solid) ambient temperature. V_{gs} measured from -0.3 V to 0.6 V in steps of 0.1 V.
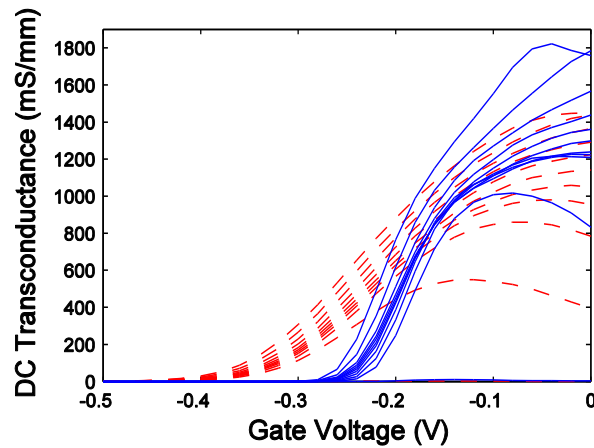

Fig. 3.4. Extrinsic DC g_m of a 2x10 µm gate width and 130-nm gate length InP HEMT at 300 K (red dashed) and 4 K (blue solid) ambient temperature. V_{ds} measured from 0.1 V to 1 V in steps of 0.1 V.

show g_m is to plot it against I_d. This dependence is plotted in Fig. 3.5, which shows a very steep g_m increase at low I_d. A g_m of more than 1 S/mm was observed for I_d of only 50 mA/mm at 4 K. At I_d of 15 mA/mm, g_m increases with 75% to 0.6 S/mm when cooled down to 10 K. At 300 K g_m was around 0.8 S/mm at 75 mA/mm. As seen in Fig. 3.5, g_m was also observed insensitive to V_{ds} at low drain current less than 100 mA/mm at both 300 K and 10 K. This, in combination with the high slope of g_m, enables excellent noise performance at very low power dissipation.

The ratio between I_d and g_m described in Eq. (2) is shown in Fig. 3.6. The curves at 10 K exhibit a clear minimum which corresponds to I_d of 15 mA/mm. At this bias, confirmed by noise measurements, the lowest noise temperature is obtained for the InP HEMT at 10 K. At 300 K, still in agreement with noise measurements, 75 mA/mm was the best low noise bias point. As seen in Fig. 3.6, the minimum was relatively insensitive to V_{ds}. This enables low power dissipation without severe noise temperature increase.

As pointed out in section 3.1, the gate leakage current is of large importance for the InP HEMT noise performance at intermediate frequencies. At optimum low noise bias, the InP HEMT exhibited a very low gate current density I_g of 20 nA/mm at 10 K and
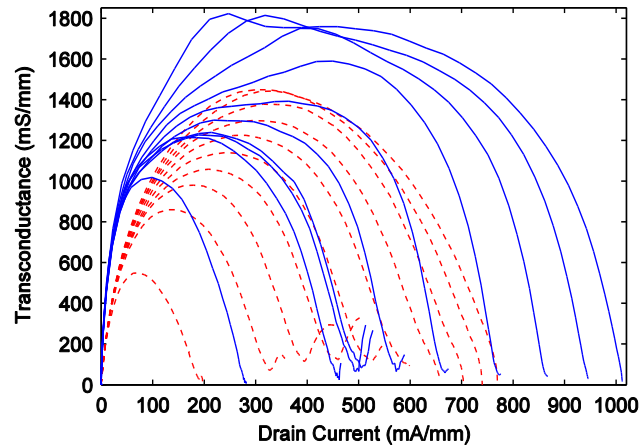
Fig. 3.5: Extrinsic g_m versus I_d of a 2x10 µm gate width and 130-nm gate length InP HEMT at 300 K (red dashed) and 10 K (blue solid) ambient temperature. V_{ds} measured from 0.1 V to 1 V in steps of 0.1 V.
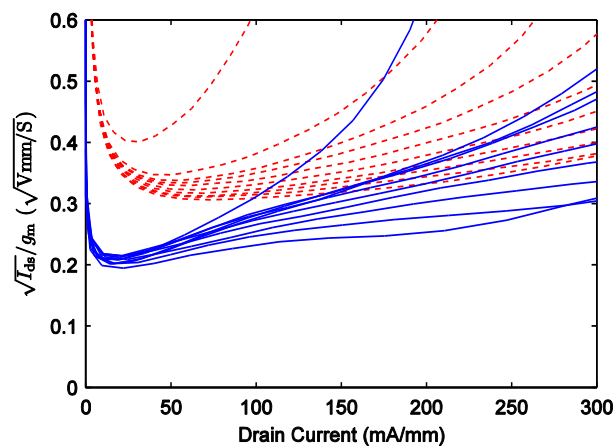

Fig. 3.6: $\sqrt{I_{ds}}/g_m$ versus Id of a 2x10 µm gate width and 130-nm gate length InP HEMT at 300 K (red dashed) and 10 K (blue solid) ambient temperature. Vds measured from 0.1 V (upper curve) to 1 V (lower curve) in steps of 0.1 V.

200 nA/mm at 300 K. The current-voltage characteristics of the gate Schottky diode at $V_{ds} = 0$ V is shown in Fig. 3.7. As clearly illustrated, the gate leakage current at negative gate voltage was heavily suppressed due to the reduction of thermal emission of electrons over the Schottky barrier when cooled down to 10 K.

As observed in Fig. 3.7, a shift in forward voltage of the gate Schottky diode of 0.1 V was observed when cooling down to 10 K. This shift is due to the temperature dependence of the built in potential of the Schottky diode and has previously been observed both for InP HEMTs and GaAs metamorphic HEMTs [33, 34].

In general, the DC characteristics at 300 K of the InP HEMT presented in Fig. 3.3 to Fig. 3.7 show steep increase in DC gm, high quality of pinch-off, and strongly suppressed I_g. As seen in these figures, the properties are strongly enhanced when cooling the InP HEMT to 10 K. Such DC behavior is a strong indication for excellent noise performance [3]. Similar temperature dependences have previously been observed for the Cryo3 InP HEMTs in the DC analysis presented in [35]. In the next section, the analysis will be extended with the microwave characteristics of the InP HEMT at cryogenic and room temperature.
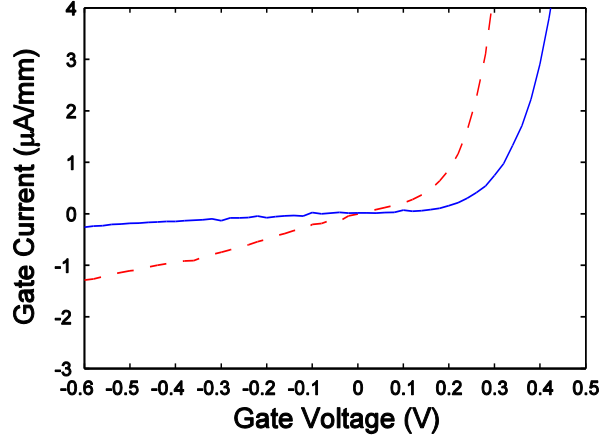
Fig. 3.7. Gate current of a 2x10 µm gate width and 130-nm gate length InP HEMT at 300 K (red dashed) and 10 K (blue solid) ambient temperature. $V_{ds} = 0$ V.

3.4   Microwave Characterization

To obtain the small signal parameters of the model in Fig. 3.1 and especially equation (1), a direct extraction method was used [36, 37]. The gate resistance R_g, which is an input parameter in the direct extraction, was obtained from DC measurements of gate through-line test structures. Values of R_g were 130 Ω/mm at 10 K and 320 Ω/mm at 300 K. The gate Schottky current influence on the S-parameters was negligible for the devices and bias levels used in this work. Therefore, the gate Schottky diode in Fig. 3.1 was modeled without a resistor for the gate leakage.

The small signal parameter extraction was focused on drain currents below 100 mA/mm as the bias point for minimum noise temperature of the InP HEMT was 75 mA/mm at 300 K and 15 mA/mm at 10 K. The most important parameters, which this section will focus on, were the ones in equation (1).(2)

Intrinsic g_m, shown in Fig. 3.8, was observed to increase by more than 100 % to 0.7 S/mm at the best cryogenic low noise bias when cooled down to 10 K. At the optimum low noise bias at room temperature, g_m was 0.8 S/mm at 300 K. At both temperatures, the intrinsic low noise g_m was far below its maximum of 2 S/mm at 10 K and 1.5 S/mm at 300 K, respectively.

C_{gs} and C_{gd} are shown in Fig. 3.9. C_{gs} was observed to be strongly dependent on temperature and drain current when operating close to pinch-off. At I_d of 15 mA/mm, C_{gs} was observed to increase about 30 % when cooled down to 10 K. C_{gd} was much less temperature and bias dependent than C_{gs}.

At pinch-off, C_{gs} and C_{gd} approached the same values of 200-250 fF/mm independent of temperature. In forward mode, $I_d > 200$ mA/mm and not shown in Fig. 3.9, C_{gs} saturated at 800 fF/mm, whereas C_{gd} slightly decreased to 150 fF/mm. The transition between these two boundaries was strongly temperature dependent. Compared to 300 K, as seen in Fig. 3.9, C_{gs} at 10 K increased very abruptly with I_d and reached the saturated value of 800 fF/mm at much lower I_d than at 300 K.

g_m, C_{gs} and C_{gd} combined give an estimate of f_T, which is the first parameter in equation (1). f_T is plotted against I_d in Fig. 3.10. A clear improvement of f_T at low I_d was observed when cooling down to 10 K. At the optimum low noise bias at 10 K, f_T increased by 60% from 80 to 130 GHz when cooled down from 300 K to 10 K. At the
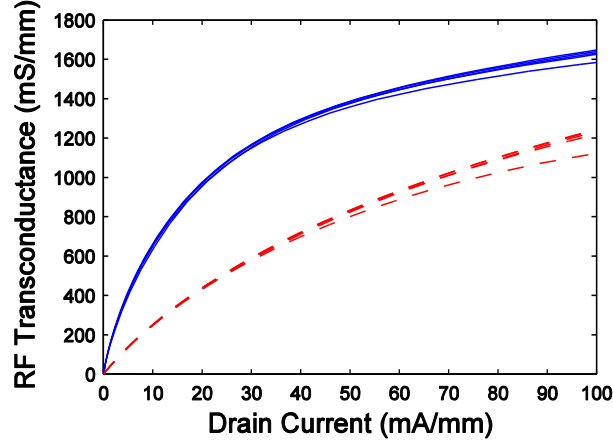
Fig. 3.8. Intrinsic g_m of a 2x100 µm gate width and 130-nm gate length InP HEMT at 300 K (red dashed) and 10 K (blue solid) ambient temperature. V_{ds} measured from 0.2 V (lower curve) to 1 V (upper curve) in steps of 0.2 V.
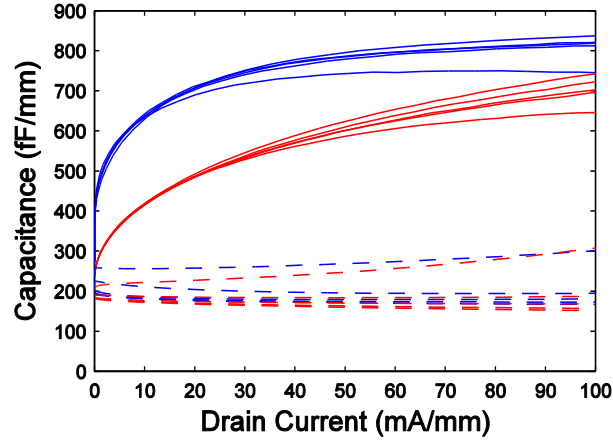

Fig. 3.9. C_{gs} (solid) and C_{gd} (dashed) of a 2x100 µm gate width and 130-nm gate length InP HEMT at 300 K (red) and 10 K (blue) ambient temperature. V_{ds} measured from 0.2 V (upper curve) to 1 V (lower curve) in steps of 0.2 V.

optimum low noise bias at 300 K, f_T increased by 60% from 80 to 130 GHz when cooled down from 300 K to 10 K. At the optimum low noise bias at 300 K, f_T was 185 GHz, i.e. considerably higher than the optimum at 10 K.

The reason for the lower f_T at the optimum bias at 10 K than at 300 K was the lower bias. As a lower I_d can achieve a higher g_m, the balance of equation (2) was shifted toward lower values of both I_d and g_m (equivalently f_T).

The last bias dependent microwave parameter in equation (1) is the intrinsic G_{ds}, which is shown in Fig. 3.11. G_{ds} is found to increase with I_d, and the way it does depends on temperature. When cooled to 10 K, the magnitude and slope of G_{ds} at low I_d is increased, while at higher I_d, the temperature change in G_{ds} was very small. As seen in Fig. 3.11, a degradation of G_{ds} is observed for low V_d below 0.4 V at both 10 K and 300 K.

The model parameters in Eq. (1) without bias dependence are R_s and R_g and their equivalent temperature T_g. At 300 K, R_s and R_g were 0.24 Ω·mm and 310 Ω/mm. At 10 K the values were 0.13 Ω·mm and 130 Ω/mm, respectively. Intrinsic R_i was fairly insensi-
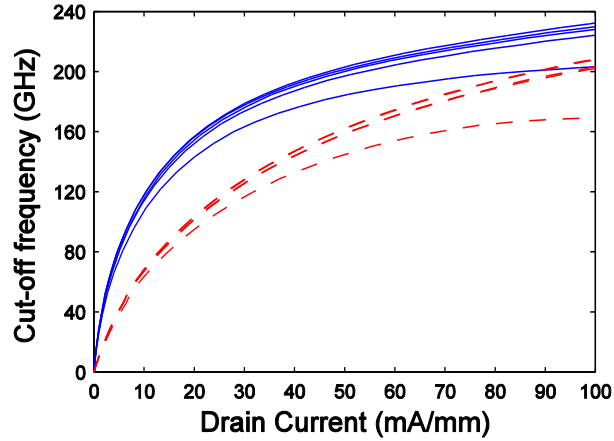
Fig. 3.10. Intrinsic cut-off frequency f_T at 300 K (red dashed) and 10 K (blue solid) at low I_d. V_d stepped between 0.2 V (lower curve) and 1 V (upper curve) in steps of 0.2 V.
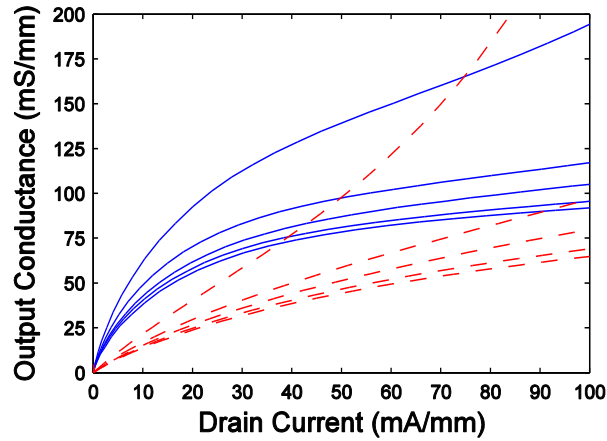

Fig. 3.11. Intrinsic G_{ds} of a 2x100 µm gate width and 130-nm gate length InP HEMT at 300 K (red dashed) and 10 K (blue solid) ambient temperature. V_{ds} measured from 0.2 V (upper curve) to 1 V (lower curve) in steps of 0.2 V.

tive to bias but strongly dependent on temperature, and was improved from 0.85 Ω·mm at 300 K to 0.45 Ω·mm at 10 K.

3.5   Noise Characterization

To accurately measure noise temperature is a challenging task. At low frequencies, very long integration times are needed and radio frequency interference (RFI) deteriorate the spectrum, at intermediate frequencies the noise levels are of the same order as the measurement uncertainties, and at high frequencies the frequency itself makes measurements difficult. Adding to this are the difficulties with impedance mismatch and instability of non-impedance matched HEMT measurements.

   In this section, the noise behavior of the InP HEMT at 300 K and 10 K is analyzed at both low frequencies and microwave frequencies, and related to the DC and RF results presented in section 3.3 and 3.4.

3.5.1   Microwave Noise Characterization

At cryogenic microwave conditions, direct noise parameter measurements of InP HEMTs are unreliable. Instead, 2x100 µm InP HEMTs were integrated in a 3-stage hybrid 4-8 GHz LNA as described in paper [B]. Noise temperature for the LNA was measured at 10 K using a cold attenuator setup, directly calibrated against a setup at NIST claiming a noise temperature uncertainty of less than 0.18 K and gain uncertainty of less than 0.1 dB [38]. Repeatability of the measurements was better than 0.1 K.

To extract the noise parameters of the InP HEMT, the noise model in Fig. 3.1 was integrated in a calibrated AWR Microwave Office model of the LNA. By setting the physical temperature of all resistive elements except G_{ds} to ambient temperature, and fitting the measured and simulated noise and gain by tuning T_d, all noise parameters could be extracted. The gate leakage current noise source between gate and drain in the noise model was set to the DC gate leakage current level at the investigated bias point.

In Fig. 3.12 extracted T_d is plotted against I_d. In accordance with [3], where T_d was extracted at room temperature and I_d between 40 and 360 mA/mm, T_d is observed to be almost linearly dependent on I_d even at 10 K and as low I_d as 1 mA/mm. At 300 K, T_d was found to be much higher, in the order of 2000 K for bias as in Fig. 3.12, but still linearly dependent on I_d. However, due to the increased thermal noise contribution at 300 K, the extraction of T_d is very sensitive to errors in the small signal extraction of the gate side resistances R_g and R_i. Because of this the error in T_d extraction was much higher at 300 K than at 10 K, and no graph is presented here. Another recent study showing a similar I_d dependence on T_d is presented in [39].

With the extracted T_d in Fig. 3.12, the minimum noise temperature of the InP HEMT could be extracted. In Fig. 3.13 T_{min} at 6 GHz is plotted against I_d at 10 K. Without consideration of the shot noise contribution from the gate leakage current, the lowest T_{min} was less than 1.2 K. When considering the gate current, T_{min} increased by 0.2 K at 6 GHz.

Independent of the gate current, the optimum low noise bias was $V_d = 0.6$ V and I_d around 15 mA/mm. This is also in agreement with the LNA measurements in paper [C], which exhibited a lowest noise temperature of 1.4 K at I_d of 15 mA/mm per stage. At 300 K the optimum low noise bias was obtained at 75 mA/mm.

To validate the noise model suggested in [20], equation (1) was evaluated with the extracted f_T, R_t, G_{ds} and T_d at 10 K and plotted in Fig. 3.13. This expression of T_{min} agrees very well with the simulated T_{min}, as seen in Fig. 3.13.

All extracted model parameters for optimum low noise bias at 10 K and 300 K are shown in Table 3.1. The small variations in parasitic inductances seen in Table 3.1 are due to small resistive and capacitive elements excluded from the model for simplicity. The associated error is estimated to be incremental.

The InP HEMTs in this work are based on a single delta-doping 3 nm above the channel. The principle of this structure is to separate the carriers from the donors using a thin spacer. The result is a high mobility electron gas in the narrow bandgap channel, and a positively charged delta-doping in the wide bandgap barrier. The magnitude and distribution of the electron gas in the channel is influenced by many factors, where the strongest are gate bias, Coulomb attraction between carriers and delta-doping, thermal diffusion, and charged traps.

To understand the carrier distribution dependence on gate voltage, Monte Carlo simulations were used. Fig. 3.14 shows the average electron velocity of the electrons in the channel at 300 K and 77 K. Independent on temperature, the velocity peaked at the
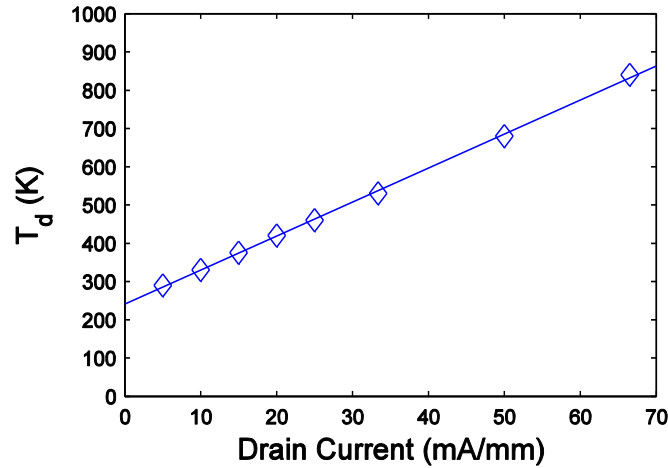
Fig. 3.12. Drain resistor temperature T_d at 10 K extracted at different I_d densities. V_d was 0.6 V for all extraction points and I_d was swept between 1 mA and 13.3 mA for each 2x100 µm InP HEMT.
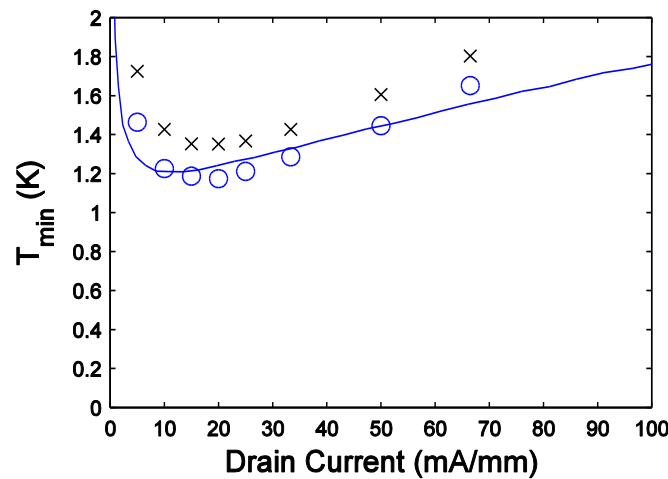

Fig. 3.13. Extracted T_{min} at 6 GHz and 10 K with (black x) and without (blue o) consideration of the gate current. The noise model suggested in [20] and based on extracted f_T, R_t, G_{ds} and T_d is shown by the blue curve.

drain side of the gate where the electric field was at maximum. The increase in maximum average electron velocity upon cooling (about 17% as seen in Fig. 3.14), explains part of the observed g_m increase seen in Fig. 3.4 and Fig. 3.5 [27]. The physical mechanism behind the electron velocity increase is the reduced electron-phonon scattering rate, leading to an increased electron mean electron free path.

The increased electron velocity does however not by itself explain the 100% g_m increase seen at the optimum cryogenic low noise bias. The second part of the explanation is the vertical electron distribution below the gate. This distribution, simulated with MC, is shown for different gate bias at 77 K in Fig. 3.15. As seen in the graph, when the gate was forward biased, the carriers were distributed in the top part of the channel due to the Coulomb attraction between the negative electrons and the positive delta-doping and gate potential. At reverse bias, the negative gate voltage canceled the attraction from the delta-doping and pushed the remaining electrons toward the buffer.

TABLE 3.1
EXTRACTED VALUES FOR THE SMALL-SIGNAL MODEL OF 2×100 μM INP HEMT AT OPTIMUM
LOW NOISE BIAS AT 300 K AND 10 K. UNITS ARE V, mA, mS, Ω, fF, pH AND K.

		300 K	10 K
Bias	V_{ds}	0.6	0.6
	I_d	15	3.3
	V_{gs}	-0.14	-0.18
Intrinsic	C_{gs}	132	138
	C_{gd}	34	37
	C_{ds}	52	46
	g_m	213	176
	R_i	3.9	2.2
	R_j	33	25
	G_{ds}	13	11
Parasitics	C_{pg}, C_{pd}	19	20
	L_g	35	46
	L_s	0	0
	L_d	36	47
	R_g	5	2.2
	R_d	1.3	0.7
	R_s	1.2	0.6
Noise	T_d	2800	400

This property of the carrier distribution is also confirmed by the DC and RF measurements in section 3.3 and 3.4. At low current, when the carriers were distributed far away from the gate, gate-to-carrier distance was large and g_m and C_{gs} were low as seen in Fig. 3.8 and Fig. 3.9. When the bias was increased, the electron distribution was shifted up towards the gate as seen in Fig. 3.15, and the gate-to-carrier distance was reduced, with increased g_m and C_{gs} as a result. When the carriers reached the top of the channel, gate-to-carrier distance became limited by the barrier and spacer thickness, and g_m and C_{gs} saturated.

When cooling down to 10 K, the thermal diffusion in the channel becomes strongly reduced. This means that the carrier distribution becomes more dependent on the gate bias and delta-doping attraction. Hence, the mean carrier distribution is expected to shift toward the delta-doping and be more sensitive to gate bias.

From an electrical perspective this means that a smaller depletion potential, and hence less negative gate voltage, is required to pinch the current at 10 K compared to 300 K. As seen in Fig. 3.3 this is confirmed by the distinct shift in V_T.

Also the higher slope of g_m versus V_g close to pinch-off in Fig. 3.3 is explained by an increased carrier confinement as a smaller change in V_g results in an increased change in g_m.

The improvement of intrinsic g_m at low drain currents as seen in Fig. 3.8 also indicates a more confined carrier concentration close to the gate when cooling down to 10 K.

Finally, a strong evidence for a change in carrier concentration is the temperature dependence of C_{gs} at low I_d. As the gate-to-carrier distance is inversely proportional to C_{gs}, the location of the carriers is indirectly given by C_{gs}.

As seen in Fig. 3.9, C_{gs} varies between two specific on and off values. At pinch-off, where C_{gs} and C_{gd} are equal, all carriers in the channel below the gate are depleted and
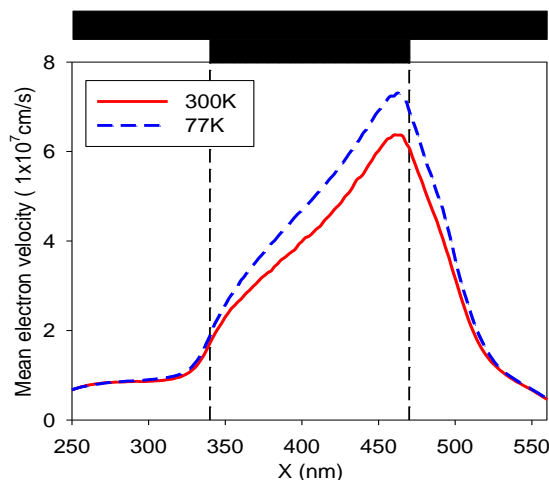
Fig. 3.14. Monte Carlo mean electron velocity profile along the channel under the gate at 300 K (red continuous line) and 77 K (blue dashed line) for V_d=0.6 V and I_d=250 mA/mm.
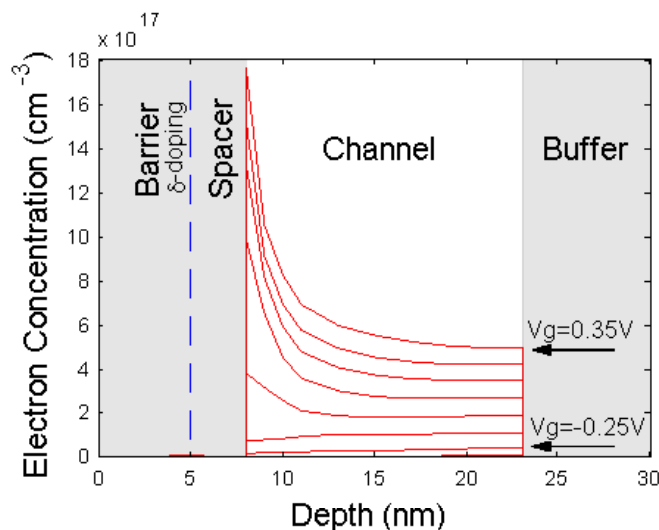

Fig. 3.15. Monte Carlo simulations showing the gate bias dependence of the electron distribution in the InP HEMT below the gate at 300 K. The epitaxial layers, as well as the delta-doping, are marked in the graph. Extrinsic gate voltage was swept between -0.35 V (lower curve) and 0.35 V (upper curve) in steps of 0.1 V. The corresponding drain currents were 5, 28, 99, 225, 403, 536, 605 and 649 mA/mm.

the capacitance is low. As gate voltage is increased, current starts to flow in the lowest part of the channel as the depletion region retreats, and C_{gs} increases as gate-to-carrier distance reduce. When the depletion region is fully withdrawn from the channel, C_{gs} saturates as gate-to-carrier distance cannot reduce further until the barrier is populated.

3.5.2   Low Frequency Noise Characterization

To measure gain fluctuations down to a level of 1ppm, a special test set shown in Fig. 3.16 was used. As the gain fluctuations were assumed independent of RF frequency, a low test frequency of 10.7 MHz was used. A balanced bridge approach was used to cancel AM fluctuations in the source. By using a HP3561 spectral analyzer at the output, the spectral density in $mW/\sqrt{Hz}$ was measured. To calibrate the measurements, a resistive divider at the output of the DUT was used. When activated, the gain was
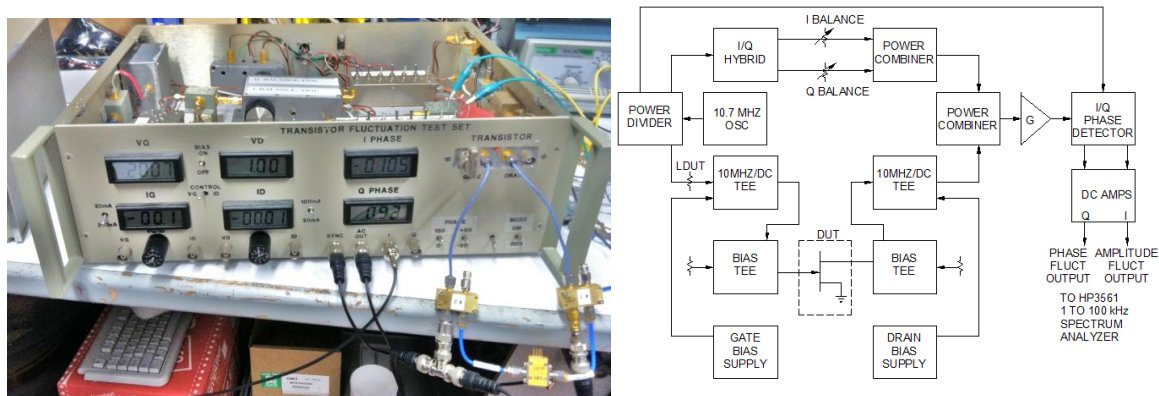
Fig. 3.16: Photograph and block diagram of test set for measuring gain fluctuations in transistors. The 10.7 MHz test signal through the transistor is approximately canceled by manual adjustment of I and Q attenuators and the resulting error signal is amplified by G and phase detected to give both amplitude and phase fluctuations.

reduced by 1%. The calibrated gain fluctuations were hence given by dividing the spectral density by the difference obtained with the resistive divider.

The low-frequency noise of the transistors was measured with three different instruments to cover the nine orders of magnitude, 1 Hz to 1 GHz, of frequency range. For the lowest frequencies, 1 Hz to 100 KHz, a HP3561 spectrum analyzer directly measuring the transistor output noise voltage was used. Between 10 kHz and 100 MHz an Agilent E4407B spectrum analyzer was used both in the same direct way as the HP3561 analyzer, and in a Y factor setup together with a Noisecom NC3210 calibrated noise diode source. For the highest frequencies, between 100 MHz and 1 GHz, an automated Y factor method with an Agilent N8975 noise figure analyzer and Agilent N4000A smart noise source was used.

Six types of HEMT and two types of SiGe HBTs were tested; see paper [E] and [40-46] for details. A global view of the data showed that all devices had approximately a $1/f$ low-frequency noise and gain fluctuation spectrum. The 1 Hz NF were in the relatively small range, 69 to 81 dB, for all the HEMTs in spite of different foundries, gate lengths (35 nm to 130 nm), materials (InP and GaAs, and wide temperature range (300 K to 22 K). The SiGe HBT 1 Hz NF varied between 27.3 dB and 42.8 dB at 300 K.

Although the gross differences between HEMTs were not large, they can have considerable effect upon radiometer sensitivity. The InP HEMTs in this thesis work had 5 to 10 dB lower NF than the other 5 HEMTs at 1 Hz and 300 K. No inherent NF difference between GaAs and InP substrates could be observed.

The gain fluctuations at 300 K and 1 Hz varied from 15 to 110 ppm for all the HEMTs and 3.6 to 4.5 ppm for the HBT's. This variation is significant for radiometers with slow switching rates and would need to be verified by tests of many samples at the desired switch rate. At 1 kHz the fluctuations were in the 1 to 10 ppm range with the lower limit determined by the noise limit of the test set.

Plots of both noise and $\Delta G/G$ at 300 K and 22 K for three different HEMTs are shown in Fig. 3.17 and Fig. 3.18. In general the NF curves have $1/f$ dependence with superimposed temperature-dependent deviations. The deviations can be related to the energy levels of traps as discussed in [21].

The HEMTs had 4 to 8 dB higher 1Hz NF at 22 K than at 300 K except for the TPQ13 where the NF did not change. The 1 Hz gain fluctuations were also higher at 22 K by factors of 1.5 to 8. For frequencies in the 10 Hz to 1 MHz range there was little change
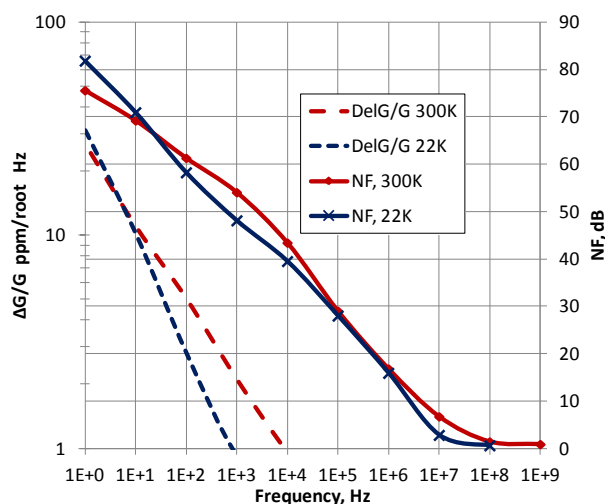
Fig. 3.17. Gain fluctuation and noise figure of OMMIC GaAs HEMT at 300 K and 22 K. $V_d = 0.6$ V and $I_d = 12$ mA (80 mA/mm)
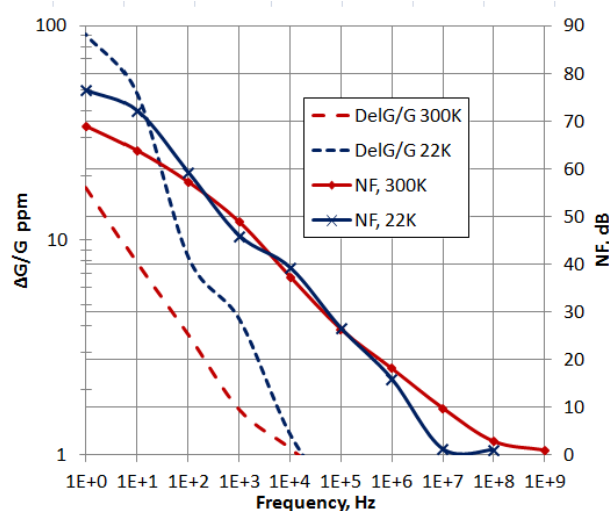

Fig. 3.18. Gain fluctuation and noise figure of InP HEMT from this thesis work at 300 K and 22 K. $V_d = 0.6$ V, $I_d = 15$ mA (75 mA/mm) at 300 K and $V_d = 0.6$ V, $I_d = 3.7$ mA (18.5 mA/mm) at 22 K.

between 22 K and 300 K while above 1 MHz the cold transistors had lower noise due to thermal effects and increased carrier confinement (paper [C]).

The 300 K low-frequency noise and ΔG/G dependence on drain current for the InP HEMT in this work is illustrated in Fig. 3.19. At 1 Hz there was little change in NF while the ΔG/G decreased by a factor of 7 at the highest bias of 44 mA/mm, at all frequencies from 1 Hz to 1 kHz.

An important question is whether the gain fluctuations are caused by perturbation of the gate DC bias voltage by the low-frequency noise. This ΔG/G due to the low-frequency noise was obtained by measuring the sensitivity of gain to bias with a network analyzer, and multiplying this coefficient with the measured voltage low-frequency noise.

The resulting comparisons are ambiguous. For the OMMIC and Triquint HEMTs the gain fluctuation due to NF closely matches the measured gain fluctuations from 1 Hz to 10 kHz as seen in Fig. 3.20 for the OMMIC device. For the InP HEMT in this thesis
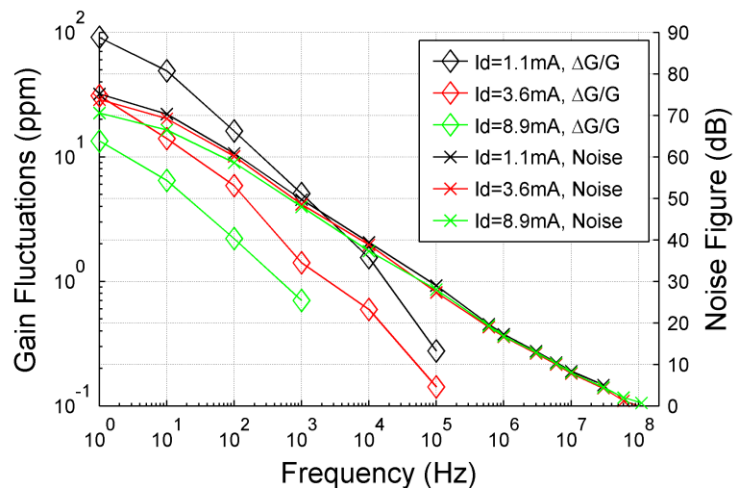
Fig. 3.19. Gain fluctuation and noise figure of 2x100 μm InP HEMT from this thesis work at 300 K for $V_d = 0.6$ V and 3 different values of I_d.
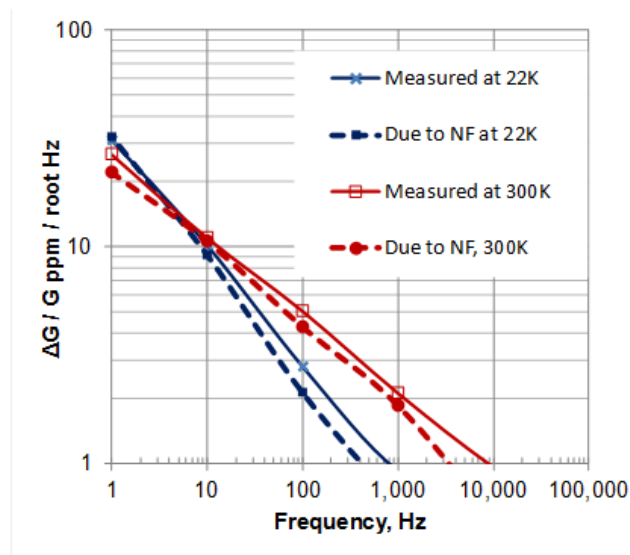

Fig. 3.20. Gain fluctuation of OMMIC GaAs mHEMT at both 300 K and 22 K measured directly and as predicted by the noise figure and sensitivity to bias.

work, the measured $\Delta G/G$ was much less than that expected from NF at both 300 K and 22 K. For the NGC 100 nm device the opposite was true. The values for all the samples at 300 K and 22 K at 1Hz are given in paper [E].

  These different gain fluctuations may be due to the location of traps and how the noise must be represented in the non-linear model of the transistor. For modeling NF at 50 ohm source impedance the low-frequency noise can be represented as a voltage source in series with the gate and in this case this voltage would affect the gain through the measured bias sensitivity coefficient. However, for some transistors this may not be the correct model for predicting non-linear effects such as g_m variations. The low-frequency noise then needs to be represented by an additional source in the drain circuit and this additional source does not change the bias point. For this case the gain fluctuation will be less than predicted from the NF. The opposite case of higher gain fluctuation than predicted would occur if g_m is fluctuating due to traps which do not produce low-frequency noise.

3.6   Conclusions

A detailed DC, S-parameter and noise analysis has been performed on ultra-low noise 130 nm gate length InP HEMTs. A small signal noise model was extracted and evaluated for different bias conditions and temperatures. It has been concluded that InP HEMTs optimized for cryogenic low noise operation are characterized by high f_T and g_m at very low I_d conditions when cooled down.

The temperature dependence of V_T, g_m, C_{gs} and C_{gd}, in combination with MC simulations, suggests that the electron carrier distribution is more confined and closer to the top of the channel where the gate control is enhanced when cooled down to cryogenic temperatures. An increased average electron velocity upon cooling, partly explaining the increased g_m, was observed using MC simulations.

A global view of low-frequency noise and gain fluctuations over a wide range of transistor types and over many orders of magnitude in frequency has been presented. The variations of $1/f$ noise and gain fluctuations were found to be relatively small between InP and GaAs HEMTs with 35 nm to 130 nm gate length. Both low-frequency noise and gain fluctuations at 1Hz, opposite to the microwave noise, increased by factors of three in most cases when cooling from 300 K to 22 K.

In some devices the low-frequency noise was determined to cause the measured gain fluctuations by modulating the bias point of the transistor, which has the secondary effect to change the gain. In other devices this was not true, and both more and less gain fluctuation than predicted by the bias point change was observed. A new equation for the degradation in radiometer sensitivity due to gain fluctuation has been presented, and the degradation is reported for all tested transistors. The results show that radiometer chop rates in the kHz range are needed for millimeter wave radiometers with 10 GHz bandwidth.

Chapter 4.

GaAs mHEMT comparison

In recent years, large progress has been achieved in the development of the InGaAs/InAlAs/GaAs metamorphic HEMT (GaAs mHEMT) as a substitute for the expensive InP HEMT technology. The GaAs mHEMT wafers are based on GaAs bulk material and thus less expensive and less brittle than InP. Moreover, the GaAs mHEMT technology can to a larger extent utilize the developed GaAs MESFET and HEMT production infrastructure unavailable for the InP HEMT technology. Room temperature performance such as cut-off frequency f_T, of the GaAs mHEMT is now almost equal to the InP HEMT [47, 48]. However, for cryogenic applications, reported noise results are still in favor for the InP HEMT [48, 49].

In this chapter DC, RF and noise performance of identical InGaAs/InAlAs HEMTs grown on InP and GaAs substrates are compared at both 10 K and 300 K, see paper [F] for details.

Except for the substrate and graded metamorphic buffer, the epitaxial structure was identical for the InP HEMT and GaAs mHEMT, as described in Chapter 2. For the GaAs mHEMT, the 500 nm $In_{0.52}Al_{0.48}As$ buffer was grown on a 300 nm $In_{0-0.52}Al_{1-0.48}As$ linearly graded metamorphic buffer on top of the GaAs substrate. The InP HEMT was grown as described in section 2.1. The 300 K channel mobility and sheet carrier density was 11400 cm^2/Vs and 2.8×10^{12} cm^{-2} for the InP HEMT, and 9900 cm^2/Vs and 3.0×10^{12} cm^{-2} for the GaAs mHEMT, respectively. The room temperature channel mobility and sheet carrier density product differed by only 7%. The wafers were processed side by side in a 130 nm gate length HEMT process, thereby minimizing process variations.

4.1   DC and microwave comparison

Uniformity and yield of the two wafers were high, and no significant differences between devices were observed. The drain current I_d is plotted against gate voltage V_g in Fig. 4.1. At room temperature, the subthreshold I_d was slightly lower for the InP HEMT compared to the GaAs mHEMT. When cooled down to 10 K, the difference was strongly increased and a superior pinch-off for the InP HEMT was evident from Fig. 4.1. Maximum I_d at
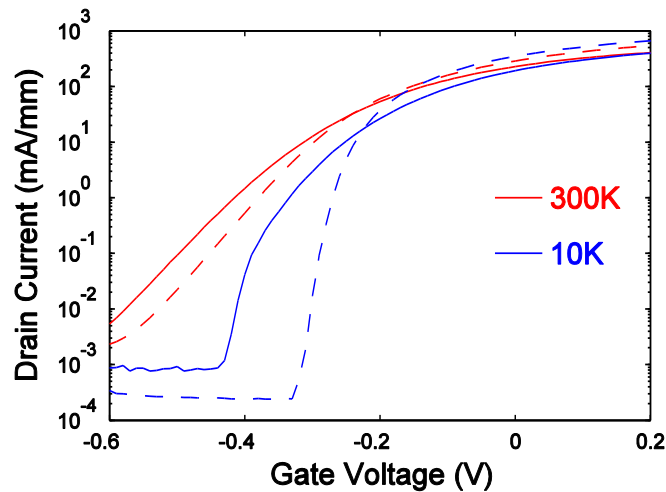
Fig. 4.1. Subthreshold I_d versus V_g at V_{ds} of 0.6 V for 2x100 µm gate width InP HEMT (dashed) and GaAs mHEMT (solid) measured at 300 K (red) and 10 K (blue) ambient temperature.

Fig. 4.2. Gate-to-source capacitance C_{gs} versus I_d at V_{ds} of 0.6 V for 2x100 µm gate width InP HEMT (dashed) and GaAs mHEMT (solid) measured at 300 K (red) and 10 K (blue) ambient temperature.
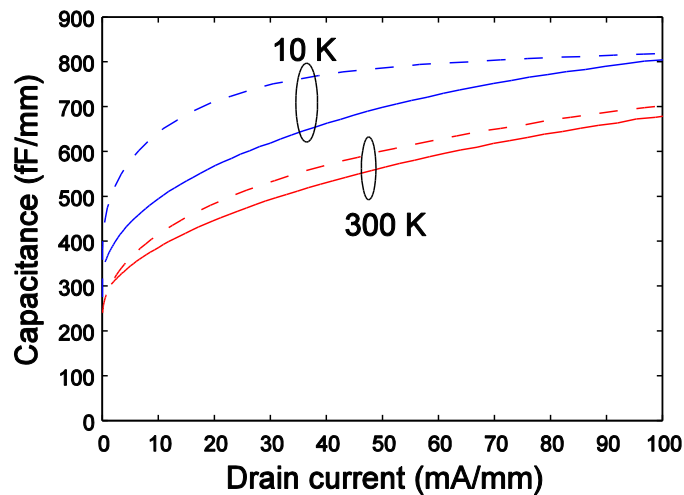
$V_d = 1$ V was 470 mA/mm (510 mA/mm) for the GaAs mHEMT and 630 mA/mm (890 mA/mm) for the InP HEMT at 300 K (10 K).

   The pinch-off voltage in a HEMT is strongly dependent on the gate-to-carrier distance as described in section 3.3. This means, given identical geometric dimensions as shown in paper [F], that the intrinsic carrier confinement in the two HEMTs can be relatively compared. The further the carriers are situated from the gate, the more negative voltage is needed to deplete them. Hence, evidently from Fig. 4.1., there is a shift in carrier concentration toward the top of the channel when cooled down; see paper [C]. This effect is stronger when the HEMT is grown on InP substrate compared with metamorphic GaAs.

   Another parameter, exposing the intrinsic carrier distribution as discussed in section 3.4, is C_{gs}. In Fig. 4.2, C_{gs} for both technologies is observed to be temperature and current dependent as in Fig. 3.9. At 300 K, the shape of C_{gs} was very similar for the two devices,
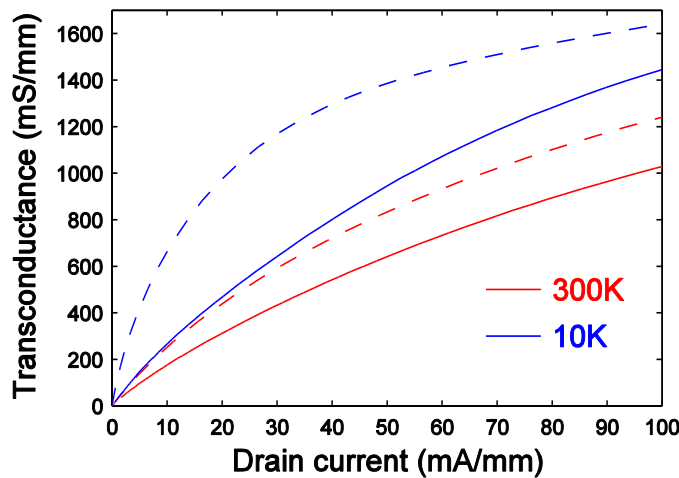
Fig. 4.3. Transconductance g_m versus I_d of 2x100 µm gate width InP HEMT (dashed) and GaAs mHEMT (solid) measured at 300 K (red) and 10 K (blue) ambient temperature and V_{ds} of 0.6 V.

with a slightly higher magnitude for the InP HEMT. When cooled down to 10 K, the difference is increased in both magnitude and shape: The InP HEMT rapidly increased to a saturation of 800 fF/mm already at I_d around 50 mA/mm, whereas the GaAs mHEMT saturated much slower at the same C_{gs} value for I_d of 200-300 mA/mm (not shown in Fig. 4.2).

At sufficient forward bias, when the HEMT channels were fully populated, C_{gs} saturated at 800 fF/mm for both buffer technologies, irrespective of temperature. At pinch-off, with channel fully depleted, C_{gs} reduced to its bias and temperature independent capacitance given by the geometric HEMT structure.

The identical extreme values of C_{gs}, at full forward and full pinch, explicitly confirm the conclusion of identical geometric dimensions drawn from the cross sectional STEM images in paper [F]. Furthermore, the different shape of the curves in Fig. 4.2 is thus a result of different carrier distributions for the same I_d. For a low I_d of 15 mA/mm, the optimum cryogenic low noise bias for the InP HEMT, C_{gs} was 680 fF/mm for the InP HEMT and 530 fF/mm for the GaAs mHEMT. Hence, compared to the GaAs mHEMT, the carrier distribution at low bias for the InP HEMT was confined closer to the top of the channel where gate control is larger. The best low noise bias of the GaAs mHEMT was I_d of 50 mA/mm. At this current level C_{gs} was 700 fF/mm, which hence corresponds to a relative carrier distribution similar to the InP HEMT at its optimum of 15 mA/mm.

A third parameter related to carrier distribution, as discussed in section 3.4, is the response of g_m versus I_d. As seen in Fig. 4.3, the low bias g_m was improved upon cooling for both technologies, however the difference was more pronounced for the InP HEMT than the GaAs mHEMT. At the optimum low noise bias at 10 K, both device technologies exhibited a g_m value of 800 mS/mm. However, as the I_d needed to obtain this value was much higher for the GaAs mHEMT, a higher noise temperature is predicted for the GaAs mHEMT in accordance with section 3.5.
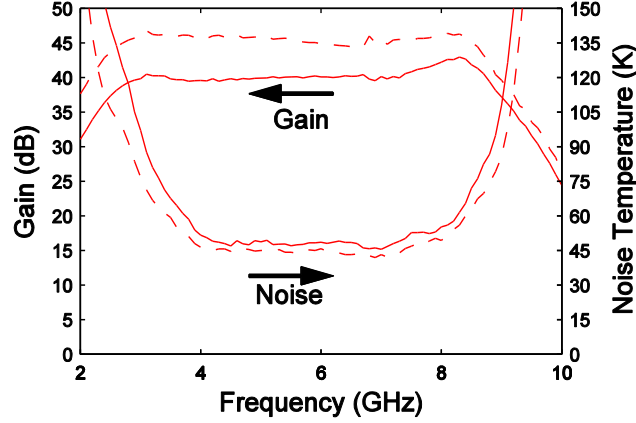
Fig. 4.4. Noise temperature and gain of a 3-stage 4-8 GHz LNA equipped with 2x100 µm GaAs mHEMTs (solid) or InP HEMTs (dashed) measured at 300 K. The amplifier was biased for best noise performance at $V_{dd} = 1.25$ V and $I_{dd} = 45$ mA for both HEMT technologies.
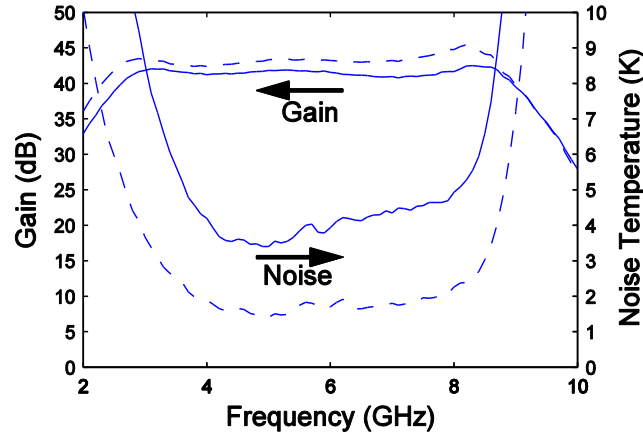

Fig. 4.5. Noise temperature and gain of a 3-stage 4-8 GHz LNA equipped with 2x100 µm GaAs mHEMTs (solid) or InP HEMTs (dashed) measured at 10 K. The amplifier was biased for best noise performance at $V_{dd} = 0.92$ V and $I_{dd} = 30$ mA (50 mA/mm per HEMT) when equipped with GaAs mHEMTs, and $V_{dd} = 0.7$ V and $I_{dd} = 9$ mA (15 mA/mm per HEMT) when equipped with InP HEMTs. V_d over the transistor was 0.6 V for both HEMTs.

4.2   Noise comparison

To accurately compare noise performance, 2x100 µm InP HEMT and GaAs mHEMT were integrated and measured separately in the same benchmarking 4-8 GHz hybrid 3-stage LNA as used in section 3.5.1. At 300 K, see Fig. 4.4, the average noise temperature (gain) in the 4-8 GHz band was 45 K (45 dB) for the InP HEMT and 49 K (40 dB) for the GaAs mHEMT. This corresponds to a 9% noise difference between the two HEMTs. At 10 K, see Fig. 4.5, the average noise temperature (gain) in the same frequency band became 1.7 K (43 dB) for the InP HEMT, and 4.0 K (41 dB) for the GaAs mHEMT. The relative difference hence increased to 135%.

   The estimated noise difference from extrinsic parasitic elements, such as the slightly elevated contact resistance of the GaAs mHEMT, was negligible. For a 2x100 µm device size, the difference corresponded to 0.3 Ω elevated drain and source resistance. At 300 K,
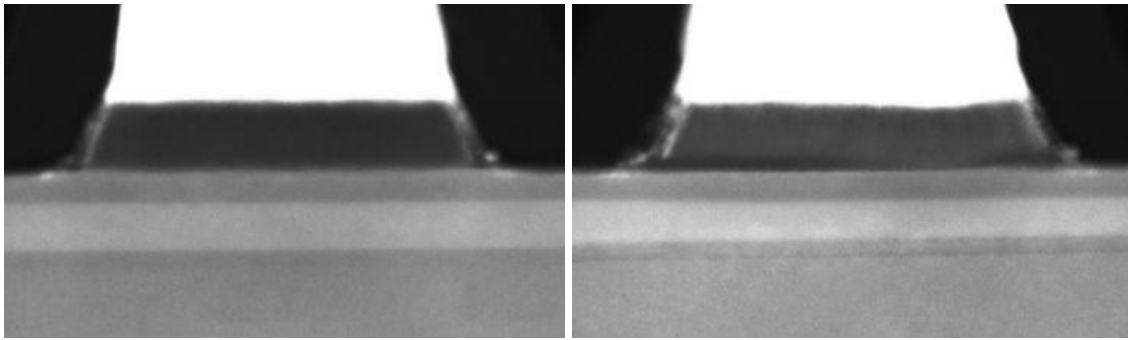
Fig. 4.6. Magnification of the gate region of the InP HEMT (left) and GaAs mHEMT (right). 130 nm gate length measured at barrier interface.

the resulting increase in noise temperature due to the higher contact resistance is estimated to be 0.7 K. At 10 K, this thermal noise contribution is strongly reduced, and the added contribution to noise temperature is less than 0.04 K.

Instead, as the S-parameters of the GaAs mHEMT and InP HEMT were close to identical when biased at their optimal low noise bias point, the majority of the noise difference was attributed the different I_d levels and interface roughness. Extraction of the equivalent drain resistor temperature T_d showed greatly elevated intrinsic noise for the GaAs mHEMT. At 15 mA/mm, T_d was 400 K for the InP HEMT and 1000 K for the GaAs mHEMT. At 50 mA/mm, the optimum low noise bias for the GaAs mHEMT, T_d was 700 K for the InP HEMT and 1350 K for the GaAs mHEMT.

In Fig. 4.6, magnified STEM images of the active device regions are shown for the two HEMTs. The samples used to make the STEM images were about 100 nm thick. By looking at the hetero junctions, it is clear that the InP HEMT image is sharper. This means that the scattered transmission through the InP HEMT is more even along the interfaces. In other words, this indicates that the GaAs mHEMT channel thickness is less uniform and has rougher interfaces compared to the InP HEMT. The strain in the top of the buffer layer, related to a change in MBE growth temperature during deposition, is also more pronounced in the GaAs mHEMT. This suggests that the metamorphic buffer suffers from more structural imperfections than the corresponding InP HEMT buffer. As a result, interface scattering, resulting in elevated noise temperature, is higher in the less confined 2-DEG of the GaAs mHEMT compared to the InP HEMT.

The microscopic observations coupled to electrical characterization of identically grown and processed InP HEMT and GaAs mHEMT point to the significance in buffer engineering in the latter technology. If the buffer layer is optimized for reduced defects, e.g. through a thicker buffer layer and optimized growth conditions, the GaAs mHEMT is expected to demonstrate improved noise performance also at cryogenic temperature.

4.3   Conclusions

An ultra-low noise InP HEMT and a GaAs mHEMT have been characterized and compared with respect to DC, RF and noise performance. The analysis showed superior DC, RF and noise improvement upon cooling the HEMTs grown on InP compared with GaAs substrate. The reason for this is believed to be a better electron confinement within the channel grown for the InP pHEMT technology.

Chapter 5.

InP HEMT MMIC Technology

Many of the largest present, and future, telescopes for radio astronomy have a collecting area divided into arrays of smaller reflectors [50-52]. The planned square kilometer array (SKA) will cover 0.1-25 GHz and the 1 km^2 collecting area will be made out of thousands of reflectors, each equipped with several receivers covering different frequency bands, or even with focal plane arrays. The demand for ultra-wideband receivers, which allows coverage of decades of bandwidth with a minimum number of receivers, is obvious.

The widest band cryogenic LNAs based on InP HEMTs reported so far usually exhibit around 100% of bandwidth. A cryogenic InP HEMT MMIC LNA used in the Arecibo radio telescope has a noise temperature of 3.5 K with 41 dB of gain at 4-12 GHz measured at ambient temperature of 12 K [4].

In this chapter, two InP HEMT MMICs are presented. The first is an adaptable cryogenic ultra-broadband 0.5-13 GHz LNA, whose input impedance can be adjusted to match an arbitrary source. This LNA addresses the need for future large arrays either as IF amplifier for SIS or Schottky mixer or directly connected to the feed.

The second is a cryogenic 24-40 GHz WR28 waveguide MMIC LNA designed to be connected directly to a horn antenna. Since it is connected with a low loss WR28 waveguide interface directly to the antenna feed, this LNA is suitable for astronomy projects such as deep space network (DSN) or very long baseline interferometry (VLBI).

Both amplifiers are thoroughly investigated, both with respect to scattering parameters and noise performance, and are benchmarked against state-of-the-art cryogenic LNAs operating in similar frequency ranges. Further details of the LNAs are given in paper [G]

5.1   MMIC design

Accurate small signal and noise models of the InP HEMT are crucial for a successful LNA design. The InP HEMT process, described in Chapter 2, needs to be repeatable, and thorough device characterization as described in Chapter 3 are prerequisites for successful circuit design.
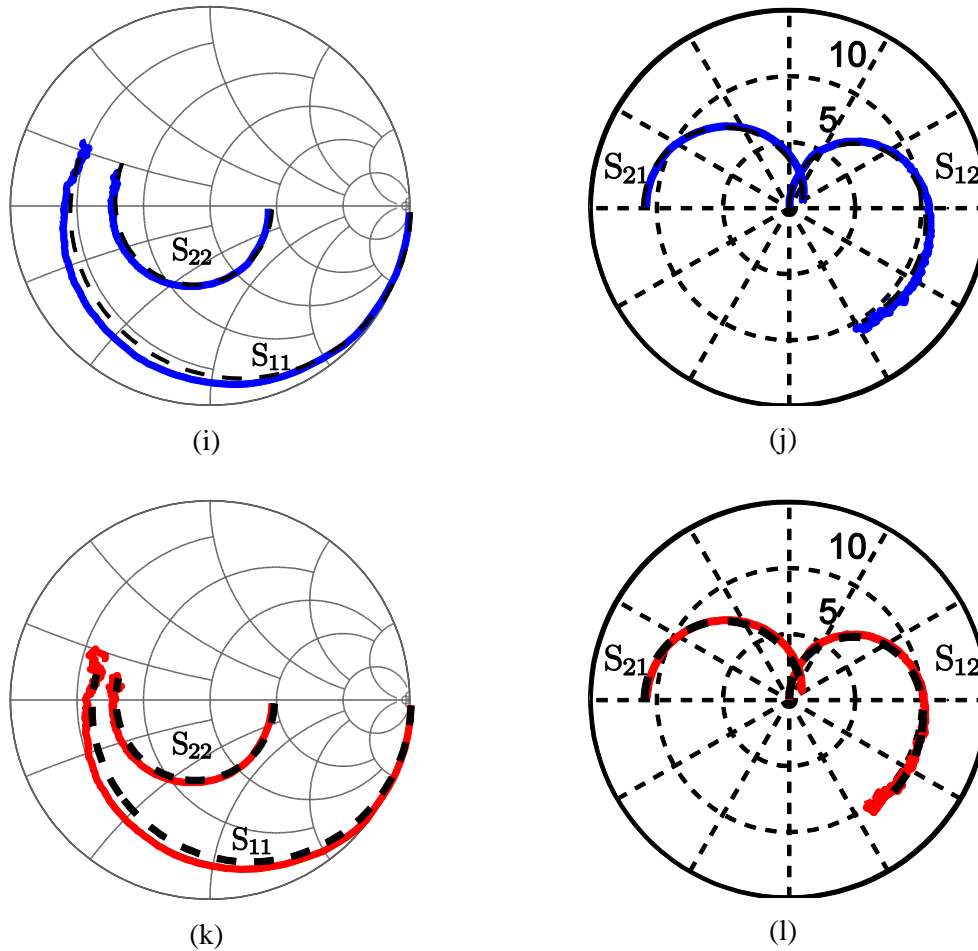
Fig. 5.1. Comparison between extracted small signal model (black dashed) and measured S-parameters of a 2x100 μm InP HEMT at 10 K (blue) and 300 K (red) ambient temperature. The bias points of the InP HEMT were 15 mA/mm at 10 K and 75 mA/mm at 300 K. The scale in (b) and (d) is 1 for S_{21} and 0.01 for S_{12}.

A comparison between measured S-parameters of a 2x100 μm InP HEMT and the extracted small signal model from Chapter 3, is shown for both 10 K and 300 K in Fig. 5.1. The bias points of the InP HEMT in Fig. 5.1 were the optimum noise bias at each temperature; 15 mA/mm at 10 K and 75 mA/mm at 300 K.

These bias points, which correspond to the optimum T_{min} of the InP HEMT, do however not necessarily have to coincide with the optimum bias point for the noise temperature of the entire LNA. Especially at high frequencies, where the gain of the first stage is low, also the second stage noise contribution becomes significant. In such cases, an increased bias might actually reduce noise temperature as the higher value of g_m reduces noise contribution from the second stage and enables an overall lower LNA noise temperature. Trade-off drain current bias used for the two MMIC LNAs in this chapter were 25 mA/mm for the 0.5-13 GHz LNA and 40 mA/mm for the 24-40 GHz LNA.

Network matching was designed using metal-insulator-metal (MIM) capacitors, thin film resistors (TFRs), via-holes and microstrip lines. To ensure stability, TFR resistors were placed between each capacitive or inductive element on all MMIC designs. By designing these resistors with at least 50% margin for process variations, all possible resonances and oscillations were proactively prevented.
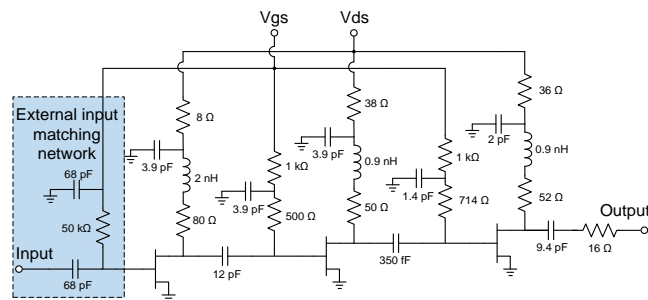
Fig. 5.2. Schematic of the 3-stage 0.5-13 GHz MMIC LNA with external matching network on RT Duroid 6002 substrate.
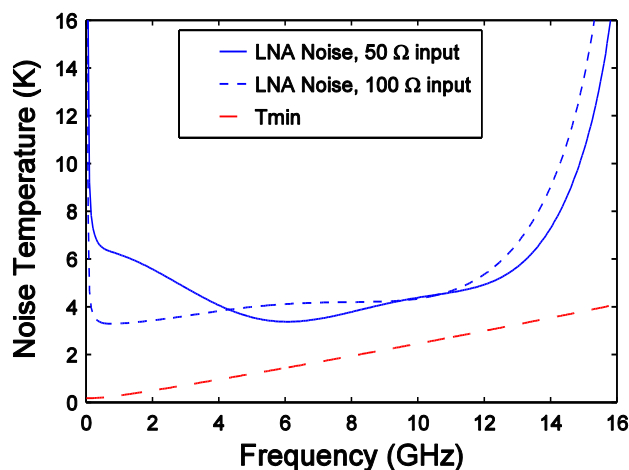

Fig. 5.3. Extracted T_{min} of a 2x100 μm InP HEMT at 15 K (red dashed) compared to the simulated noise temperature of the amplifier connected to a 50 Ω source impedance (blue solid) and 100 Ω source impedance (blue dashed). The 3-stage LNA was biased for wide bandwidth operation at $V_d = 1$ V and $I_d = 15$ mA. The resulting InP HEMT bias, also used for T_{min} extraction, was $V_{ds} = 0.6$ V and $I_d = 5$ mA per stage.

5.2   0.5-13 GHz Ultra Broadband Ultra Low Noise InP MMIC LNA

Apart from the InP HEMT itself, the input matching network of the first stage ultimately determines the noise performance of the whole amplifier. To minimize substrate, and especially metal losses, and consequently degraded noise performance, an external input matching network on a 0.381 mm (15 mil) low loss, low permittivity, and temperature stable RT Duroid 6002 substrate with 17 μm copper cladding, was used. The selected combination of relative permittivity and thickness of the substrate enabled high impedance matching with relatively wide microstrip lines, resulting in reduced metal losses. The overall simulated reduction of LNA noise, due to the external input matching network, was on average 2 K within the 0.5-13 GHz band, when compared to an internal input matching network.

To improve stability, and decrease the magnitude of S_{11} for better matching, a source inductance was introduced in the first transistor using a narrow microstrip line to a via-
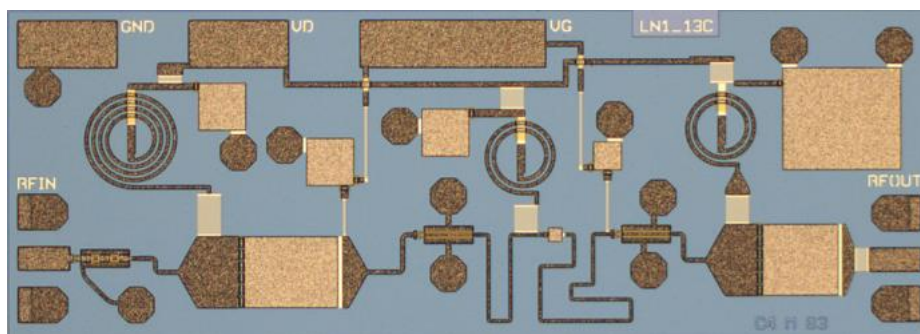
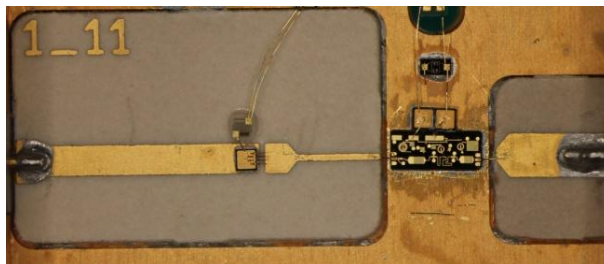Fig. 5.4. A photograph of fabricated 3-stage 0.5-13 GHz MMIC LNA

Fig. 5.5. A photograph of 3-stage 0.5-13 GHz MMIC mounted in a housing together with an
external input matching circuit.

hole. A schematic of the 3-stage LNA, showing the external input matching network, is given in Fig. 5.2. All three stages utilize 2x100 μm gate width devices with a common bias network.

When matching the first transistor for minimum noise, the gain curve linearly declined with frequency. This gain tilt was easily compensated with the following stages. But with a low gain in the first stage, the noise contribution from the second stage became significant at the upper frequency band limit. By using the trade-off bias point with 25 mA/mm drain current, this effect was reduced. As seen in Fig. 5.3, T_{min} was close to linearly dependent on frequency, and was 1.8 K at 6 GHz.

As a compromise, the input matching network was designed to noise match the first transistor at the upper frequency limit, while minor mismatch at the lower frequencies was accepted as trade-off. By doing this, the noise temperature of the amplifier could be held relatively constant with frequency and close to the minimum noise temperature at the upper frequencies, as seen in the simulations of the 3-stage LNA in Fig. 5.3. The second and third stages were then matched for flat gain and stability. The bias point for the simulations in Fig. 5.3 was $V_d = 1$ V and $I_d = 15$ mA, resulting in an individual bias of $V_{ds} = 0.6$ V and $I_d = 5$ mA (25 mA/mm) for each InP HEMT. A photograph of the 2 mm $\times$ 0.75 mm MMIC can be seen in Fig. 5.4.

In some applications, e.g. as an IF-amplifier for Schottky or SIS mixers, it is advantageous to omit the standard 50 Ω interface as often higher impedance is needed. Fig. 5.3 shows simulated performance of the LNA using an input matching network optimized for 100 Ω source impedance. With this input matching the bandwidth of the amplifier increases to 0.1-13 GHz using the same RT Duroid 6002 substrate for the circuit.

A housing with SMA input and output connectors was designed and machined to package the 1-13 GHz MMIC LNA. A photograph of a mounted MMIC with input matching network can be seen in Fig. 5.5.

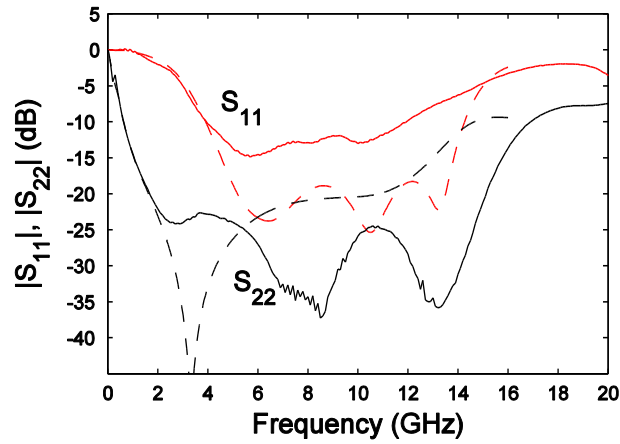Fig. 5.6. Measured (solid) and simulated (dashed) S-parameters of a 0.5-13 GHz LNA module at 300 K. V_d = 2.35 V and I_d = 45 mA.
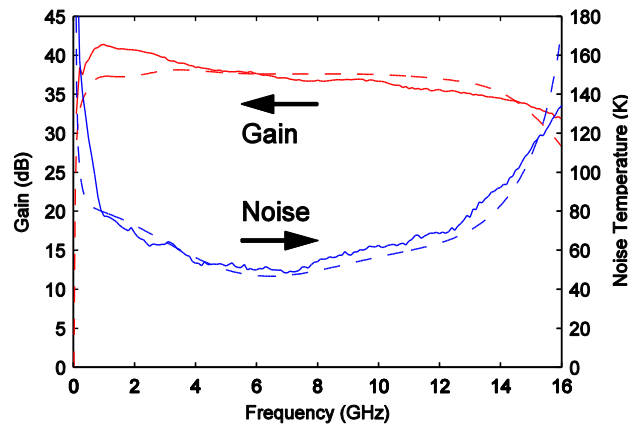

Fig. 5.7. Measured (solid) and simulated (dashed) gain and noise temperature of a 0.5-13 GHz LNA module at 300 K. V_d = 2.35 V and I_d = 45 mA
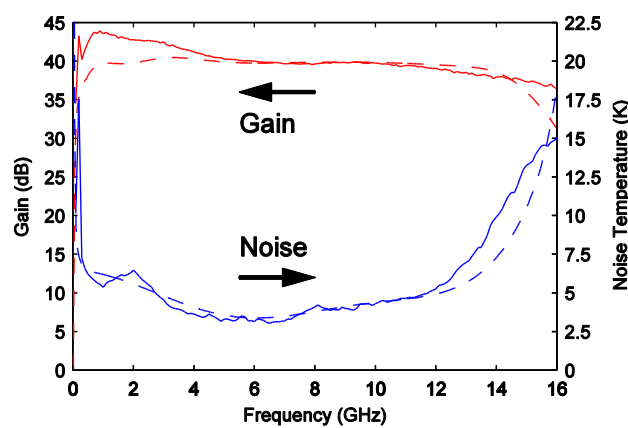

Fig. 5.8. Measured (solid) and simulated (dashed) gain and noise temperature of 0.5-13 GHz LNA module at 15 K. V_d = 1 V and I_d = 15 mA
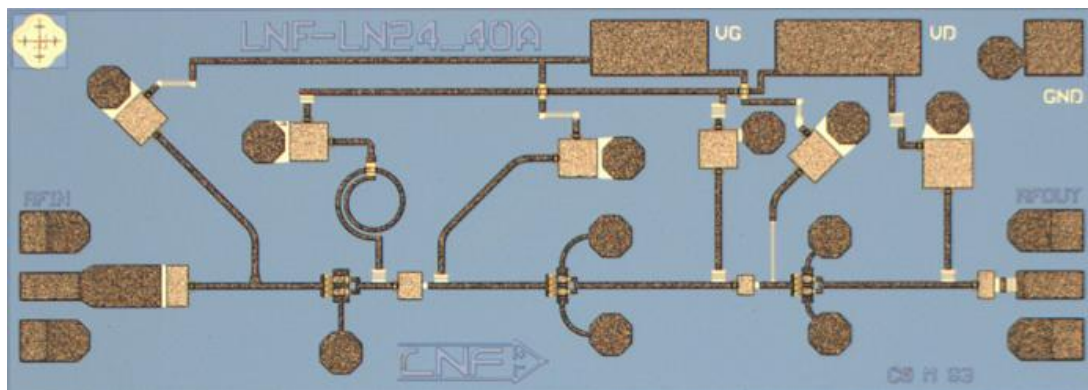
Fig. 5.9. Photograph of fabricated 3-stage 24-40 GHz MMIC LNA

5.2.1   Measurements and Characterization

As seen in Fig. 5.6, input return loss (S_{11}) was traded off against noise performance at low frequencies, but was better than 7 dB between 3 and 13 GHz. Output return loss (S_{22}) was better than 8 dB within the whole band.

Fig. 5.7 shows the measured noise temperature and gain (S_{21}) at room temperature. The LNA had relatively flat gain between 34 dB and 40 dB in the whole 0.5-13 GHz band. The lowest noise was 48 K and was achieved around 7 GHz. The gain, consistent with the S-parameter measurements, was above 34 dB in the whole band.

As seen in Fig. 5.8, the lowest noise temperature at cryogenic condition was 3 K at 7 GHz and below 7 K in the whole 0.5-13 GHz band. The gain was slightly increased compared to room temperature and was higher than 38 dB in the whole band.

5.3   24-40 GHz Low Noise InP MMIC LNA

The benefit with an external input matching network is lower loss and increased flexibility. The drawback, in addition to the increased fabrication work load, is the presence of lumped components and bond wires. At low frequencies these components work fine, and are easy to predict, but in the 24-40 GHz range modeling becomes difficult and very precise assembly is needed to match simulations. Further, the bond pad leading to the first gate on the MMIC is close to 50 ohm and electrically long at high frequencies. This effectively cancels out the desired high impedance of the external matching network. Instead, an internal input matching network was chosen for the three stage 24-40 GHz LNA. The first transistor was a 4x25 μm gate width device matched for low noise. The device size was chosen for best noise match within the frequency band. The following two stages utilized 4x15 μm gate width devices matched for flat gain. The smaller device sizes of the second and third stages result in lower capacitances and hence a less frequency dependent gain. The gain was further flattened with bias stubs shorter than λ/4 on the second and third stages. All transistors utilized a common bias network which distributed equal current densities to all stages. A schematic of the 3-stage LNA is given in Fig. 5.10. The simulated cryogenic noise and gain of the LNA, together with T_{min}, is shown in Fig. 5.10. T_{min}, close to linearly dependent on frequency, was 10 K at 40 GHz. The bias point for the simulation was $V_{ds} = 0.7$ V and $I_d = 4$ mA (40 mA/mm)
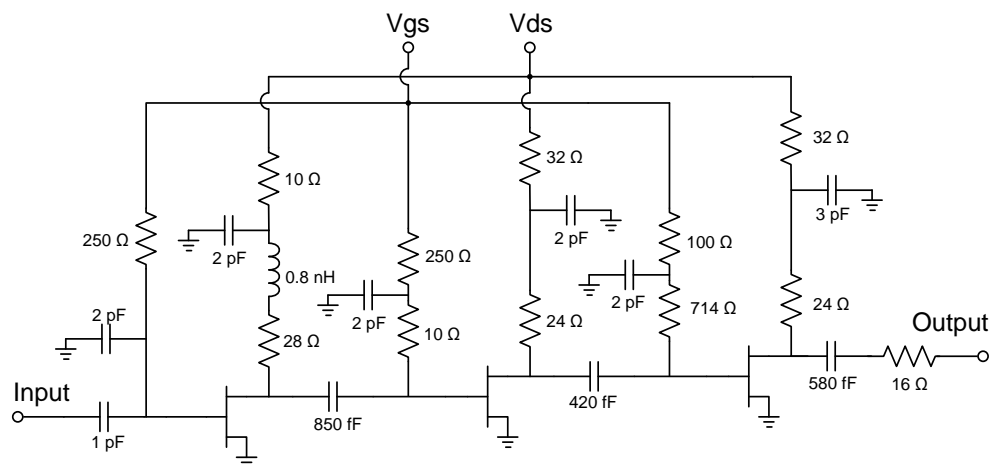
Fig. 5.10. Schematic of the 3-stage 24-40 GHz MMIC LNA.
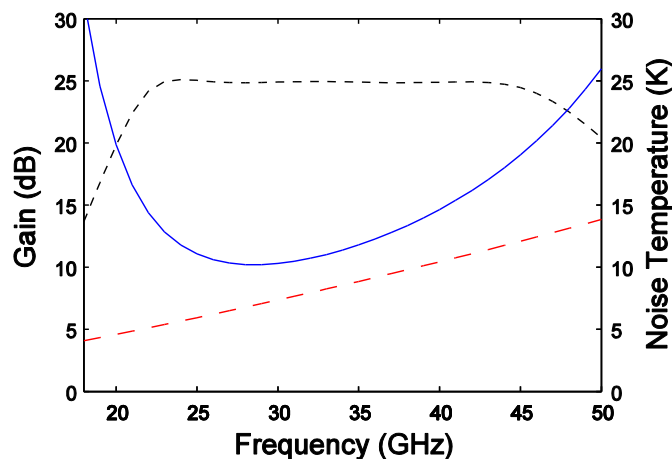

Fig. 5.11.   Extracted T_{min} of a 4x25 μm InP HEMT at 15 K (red dashed) compared to the simulated noise temperature (blue solid) and gain (black dashed) of the 24-40 GHz. The first InP HEMT (used for extraction of T_{min}) was biased at $V_{ds} = 0.7$ V and $I_d = 4$ mA and the second and third were biased at $V_{ds} = 0.7$ V and $I_d = 2.5$ mA. The total LNA bias was $V_d = 1.2$ V and $I_d = 9$ mA.

for the first transistor and $V_{ds} = 0.7$ V and $I_d = 2.5$ mA (42 mA/mm) for the second and third transistors. The total LNA bias was $V_d = 1.2$ V and $I_d = 9$ mA. A photograph of the 2 mm × 0.75 mm MMIC can be seen in Fig. 5.9.

5.3.1   Measurements and Characterization

The 24-40 GHz MMIC LNA was packaged in a WR28 waveguide housing. Waveguide to thin film microstrip transitions made on 0.10 mm (4 mil) alumina was used to couple the LNA to the waveguides [53]. Alumina was selected due to its good mechanical stability for very thin substrates. The loss of the transition was measured to 0.35 dB at 300 K, and simulated to 0.1 dB at 10 K. A photograph of the mounted MMIC with waveguide probes can be seen in Fig. 5.12.

   The best low noise bias of the 24-40 GHz LNA at room temperature was $V_d = 1.4$ V and $I_d = 27$ mA. As seen in Fig. 5.13, input and output return loss (S_{11} and S_{22}) was better than 9 dB within the whole frequency band.
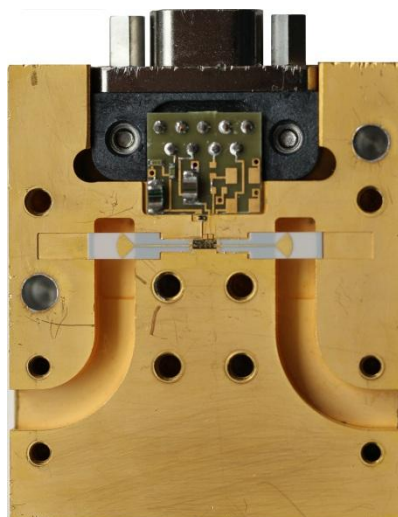
Fig. 5.12. A photograph of 3-stage 24-40 GHz MMIC LNA with waveguide to thin-film microstrip transitions mounted in housing.

Fig. 5.13. Measured (solid) and simulated (dashed) S_{11} (red) and S_{22} (black) of a 24-40 GHz LNA module at 300 K. $V_d = 1.4$ V and $I_d = 27$ mA.

Fig. 5.14 shows the measured noise temperature and gain (S_{21}) at room temperature. The LNA had relatively flat gain between 26.5 dB and 29.5 dB in the whole 24-40 GHz band. The lowest noise was 110 K and the average noise was 125 K in the 24-40 GHz band. The gain, consistent with the S-parameter measurements, but higher than simulated, was in average 27.5 dB. The sharp decrease of gain and increase of noise at 22 GHz are due to the cut-off frequency of the WR28 waveguide. Also the gain spikes at the upper frequency limit are attributed to the waveguide as more than one mode is supported at these frequencies. The estimated noise contribution from the waveguide probe loss was 30 K.

When cooled down to 15 K, the optimum low noise bias of the LNA was $V_d = 1.2$ V and $I_d = 9$ mA. As seen in Fig. 3.13, the lowest noise temperature at cryogenic condition was 10 K at 27 GHz and in average 13.2 K in the whole 24-40 GHz band. The gain was slightly increased compared to room temperature and was in average 28 dB in 24-40 GHz band. The simulated noise contribution from the waveguide probe was 0.5 K.

A comparison of the two LNAs with previously published LNAs, working in similar frequency ranges, is presented in Table 5.1. It is observed that the two LNAs presented in
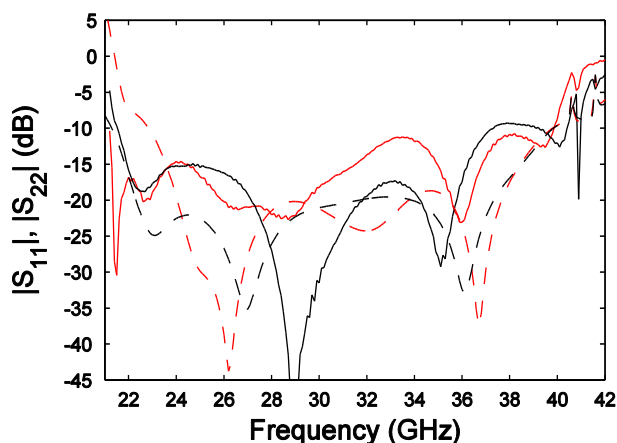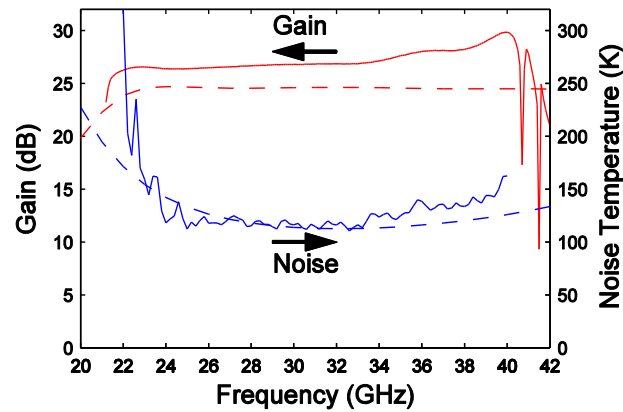
Fig. 5.14. Measured (solid) and simulated (dashed) gain and noise temperature of a 24-40 GHz LNA module at 300 K. $V_d = 1.4$ V and $I_d = 27$ mA.
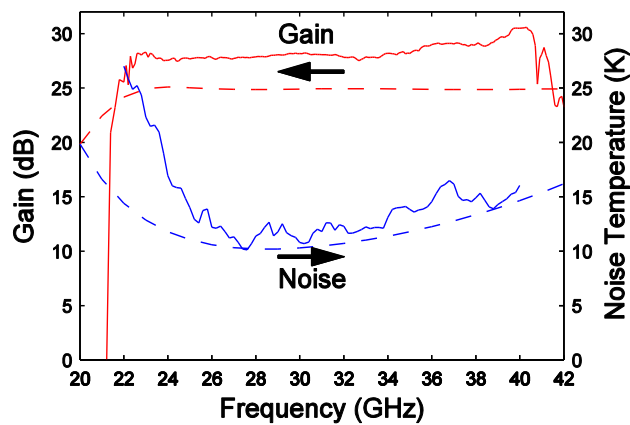
Fig. 5.15. Measured (solid) and simulated (dashed) gain and noise temperature of a 24-40 GHz LNA module at 15 K. $V_d = 1.2$ V and $I_d = 9$ mA.

this work both showed state-of-the-art results in the combination of high bandwidth and low noise. Furthermore, both amplifiers exhibited among the highest gain/stage, which in combination with the high bandwidth makes the result very useful for wide band antenna systems in radio astronomy.

5.4   Conclusions

Two broadband cryogenic MMIC LNAs have been fabricated, mounted in modules and tested at 300 K and 10 K ambient temperature. The circuits are of large interest in several radio astronomy projects, such as SKA, requiring the lowest noise temperature available. The noise temperature of the 0.5-13 GHz LNA was 3 K at the lowest point and below 7 K in the entire frequency band. The 24-40 GHz LNA exhibited a lowest noise temperature of 10 K and an average noise temperature of 13.2 K. These results confirm the potential of the ultra-low noise InP HEMT process described in Chapter 2 and Chapter 3.

TABLE 5.1
COMPARISON OF CRYOGENIC WIDE-BANDWIDTH LNAS

Ref.	Freq. (GHz)	Bandwidth (%)	$T_{e,min}$ (K)	$T_{e,avg}$ (K)	Gain/stage (dB)
[54]	1-11	167	2.3	3.9	11.1
[17]	4-12	100	2.7	3.5	13.3
[16]	4-12	100	3.3	4.5	11.3
[49]	4-12	100	-	5.3	10.5
[55]	4-12	100	5.8	8.1	8.7
This work	0.5-13	185	3.0	4.4	12.7
[56]	26-40	42	8	12.5	9
[57]	26-40	42	9.3	11.4	7.2
[49]	25-34	31	-	15.2	8
This work	24-40	50	10	13.2	9.3

Chapter 6.

Conclusions

In this thesis, ultra-low-noise InP HEMTs with 130 nm gate length have been designed and fabricated for cryogenic temperature operation. The epitaxial structure, gate recess, passivation and access resistances have been optimized, resulting in a new state-of-the-art minimum low noise temperature of 1 K at 6 GHz.

A detailed DC, S-parameter and noise analysis has been performed. A small signal noise model was extracted and evaluated for different bias conditions and temperatures. The temperature dependence of V_T, g_m, C_gs and C_gd, in combination with MC simulations, suggested that the carrier distribution is more confined and closer to the top of the channel where the gate control is higher when cooled down to cryogenic temperatures.

A study of low-frequency noise and gain fluctuations over a wide range of transistor types and over many orders of magnitude in frequency has been presented. The variations in low-frequency noise and gain fluctuations were found to be relatively small between InP and GaAs HEMTs with 35nm to 130 nm gate length. Both low-frequency noise and gain fluctuations at 1Hz, opposite to the microwave noise, increased by factors of three in most cases when cooling from 300 K to 22 K.

In some devices, the gain fluctuations were dependent on the low-frequency noise. In others this was not true, and both more and less gain fluctuation than predicted was observed. A new equation for the degradation in radiometer sensitivity due to gain fluctuation has been presented. The results show that radiometer chop rates in the kHz range are needed for millimeter wave radiometers with 10 GHz bandwidth.

To evaluate the emerging GaAs mHEMT technology as a substitute for InP HEMTs, ultra-low noise InP HEMTs and GaAs mHEMTs have been compared. The analysis showed superior DC, RF and noise improvement upon cooling the HEMTs grown on InP compared with GaAs substrate. This was proposed to be related to better electron confinement within the channel of the InP HEMTs compared to the GaAs mHEMTs fabricated with the metamorphic buffer technology in this work.

To demonstrate the cryogenic noise performance in monolithic LNAs, two broadband cryogenic MMICs have been designed and fabricated based on the optimized InP HEMT technology developed in this thesis. The MMICs were mounted in modules and tested at

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300 K and 10 K ambient temperature. The noise temperature of the 0.5-13 GHz LNA was 3 K at the lowest point and below 7 K in the entire frequency band. The 24-40 GHz LNA exhibited a lowest noise temperature of 10 K and an average noise temperature of 13.2 K. These state of the art results for cryogenic LNAs confirm the potential of the ultra-low noise InP HEMT process. The circuits demonstrated in this thesis are of large interest in several radio astronomy projects such as SKA requesting the lowest noise temperature in the receivers.

Chapter 7.

Future Work

To further develop the InP HEMT technology, and our understanding thereof, four specific research topics are suggested.

The first is to push for ultra-low noise at higher frequencies beyond W-band at cryogenic operation. For frequencies higher than around 40 GHz, the 130 nm gate length is too large. Today's InP HEMT processes utilizing gate lengths of 35 nm and below usually need very high I_d for optimum operation. To scale the process described in this thesis toward 35 nm gates and beyond, with a maintained high quality of pinch-off, low current operation and focus on cryogenic operation, would probably lower today's minimum noise temperature at high frequencies (>100 GHz) considerably.

The second topic is the Pospieszalski parameter T_d. To better understand this parameter, focused electrical and material science analysis needs to be performed to couple the I_d and temperature dependence, observed in this thesis, to physical mechanisms in the intrinsic InP HEMT.

The third topic is the thermal properties of the HEMT at cryogenic conditions. The typical operation of a cryogenic low noise InP HEMT is less than one percent of the maximum power. At room temperature, the self-heating is negligible. When approaching 0 K, however, the specific heat of InP approaches zero exponentially [58]. Practically, this means that very little heating power is needed to heat up the channel. Such self-heating could be the reason for not seeing any noise temperature improvement when cooling below 10 K ambient temperature.

The final topic is to solve the so called "Low frequency problem". When large multi-finger InP HEMT transistors (≥4 fingers, ≥200 μm total gate width) are cooled down, their IV-characteristics is deteriorated, S21 gets a spike at low frequencies and S22 makes an inductive loop. According to [59], the problem is both oscillation and trap related. By solving this problem, low frequency LNAs today requiring 2-finger devices, would improve a lot due to lower gate resistance, resulting in new state-of-the-art results up to 10 GHz.

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