

Development of a Cross-Correlator System for Space-Borne Earth Observation Interferometric Imaging

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Synthetic aperture radiometry in the microwave region constitutes a new way of performing earth observation. Previously applied from a low earth orbit, there are now efforts being put into placing such an instrument in a geostationary earth orbit (GEO); this includes the geostationary atmospheric sounder (GAS) and the geostationary synthetic thinned aperture radiometer (GeoSTAR). These instruments will provide temperature and moisture distribution data from the atmosphere in a spatial and temporal resolution that was previously unattainable, due to cloud occlusion and large aperture requirements. A key component in these kinds of synthetic aperture instruments is the cross-correlator.

A digital cross-correlator chip with 64 inputs has been implemented in a 65-nm CMOS process. It performs pair-wise, one-bit, zero-lag cross-correlation between all input signals. Tests have confirmed functionality at clock frequencies of at least 2.5 GHz. Power consumption has been measured to 0.13 mW/prod/GHz at nominal voltage. Radiation tests of the digital correlator chip have been performed at the Radiation Effects Facility at Texas A&M University. A variety of ion beams were used in a number of different testing scenarios to find weaknesses of the design, such as readout logic single event upsets (SEU) causing severe data corruption. Cross-sectional data from the radiation tests have been run through the Space Environment Information System (SPENVIS) to predict SEU behavior for GEO. An average SEU rate of $\sim 1/\text{day}$ is expected when using 10 mm Al shielding. It is expected that errors in significant bits can be detected and discarded while less significant errors will be masked by integration.

An 8-channel comparator chip, with the purpose of performing sampling of the analog input signals, has been implemented in a 130-nm BiCMOS process. Features such as core and output driver bias control have been included for performance/power consumption tuning. Clock return output, flip-flop sampling and current mode logic (CML) output drivers facilitate integration of the proposed correlator system, Fig. 1. Per-channel tuning pins are included for adjustment of input dc offsets. The comparator chip has been experimentally verified to perform sampling at a rate of at least 2.5 GS/s.

The 64-input correlator system, currently under development, will bring together eight comparators and one digital correlator in a single unit. We expect that this correlator system will be working at 1 GS/s within a power budget of 2.5 W, making it well suited for space application.

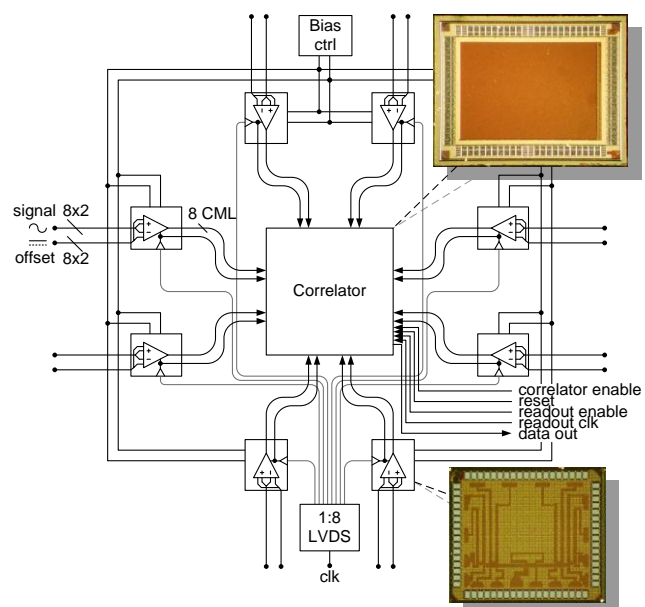


Fig. 1. Cross-correlator system schematic and die photos.