Thesis for the degree of Doctor of Philosophy

On Formal Methods for Large-Scale Product Configuration

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Cover: Supervisor for interactive product configuration, see Figure 5.8 on page 63.

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to my family

Abstract

In product development companies mass customization is widely used to achieve better customer satisfaction while keeping costs down. To efficiently implement mass customization, product platforms are often used. A product platform allows building a wide range of products from a set of predefined components. The process of matching these components to customers' needs is called product configuration. Not all components can be combined with each other due to restrictions of various kinds, for example, geometrical, marketing and legal reasons. Product design engineers develop configuration constraints to describe such restrictions. The number of constraints and the complexity of the relations between them are immense for complex product like a vehicle. Thus, it is both error-prone and time consuming to analyze, author and verify the constraints manually. Software tools based on formal methods can help engineers to avoid making errors when working with configuration constraints, thus design a correct product faster.

This thesis introduces a number of formal methods to help engineers maintain, verify and analyze product configuration constraints. These methods provide automatic verification of constraints and computational support for analyzing and refactoring constraints. The methods also allow verifying the correctness of one specific type of constraints, item usage rules, for sets of mutually-exclusive required items, and automatic verification of equivalence of different formulations of the constraints. The thesis also introduces three methods for efficient enumeration of valid partial configurations, with benchmarking of the methods on an industrial dataset.

Handling large-scale industrial product configuration problems demands high efficiency from the software methods. This thesis investigates a number of search-based and knowledge-compilation-based methods for working with large product configuration instances, including Boolean satisfiability solvers, binary decision diagrams and decomposable negation normal form. This thesis also proposes a novel method based on supervisory control theory for efficient reasoning about product configuration data. The methods were implemented in a tool, to investigate the applicability of the methods for handling large product configuration problems. It was found that search-based Boolean satisfiability solvers with incremental capabilities are well suited for industrial configuration problems.

The methods proposed in this thesis exhibit good performance on practical configuration problems, and have a potential to be implemented in industry to support product design engineers in creating and maintaining configuration constraints, and speed up the development of product platforms and new products.

Keywords: Product configuration, constraint satisfaction, Boolean satisfiability, knowledge compilation, supervisory control theory.

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Alexey Voronov
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List of Publications

This thesis is based on the following appended papers:

Paper 1. Alexey Voronov, Knut Åkesson, Anna Tidstam, Johan Malmqvist and Martin Fabian. *Toward better support for authoring and maintaining product configuration constraints.* Submitted (2012).

Paper 2. Alexey Voronov, Knut Åkesson, Anna Tidstam and Johan Malmqvist. *Verification of Item Usage Rules in Product Configuration.* Proceedings of 9th International Conference on Product Lifecycle Management PLM-12, Montreal, Canada, 2012.

Paper 3. Alexey Voronov, Knut Åkesson and Fredrik Ekstedt. *Enumerating partial configurations.* Proceedings of Configuration Workshop at 22nd International Joint Conference on Artificial Intelligence IJCAI-11, Barcelona, Spain, 2011.

Paper 4. Koen Claessen, Niklas Een, Mary Sheeran, Niklas Sörensson, Alexey Voronov and Knut Åkesson. *SAT-Solving in Practice, with a Tutorial Example from Supervisory Control.* Journal of Discrete Event Dynamic Systems 19(4), pp. 495–524, 2009.

Other relevant publications co-authored by Alexey Voronov:

Anna Tidstam, Lars-Ola Bligård, Fredrik Ekstedt, **Alexey Voronov**, Knut Åkesson, Johan Malmqvist. *Development of Industrial Visualization Tools for Validation of Vehicle Configuration Rules.* Proceedings of 9th International Symposium on Tools and Methods of Competitive Engineering, pp. 14, 2012.

Sajed Miremadi, **Alexey Voronov**. *Symbolic Reduction of Guards in Supervisory Control Using Genetic Algorithms.* Technical report. Göteborg: Chalmers University of Technology, 2012.

Alexey Voronov, Knut Åkesson. *Verification of Process Operations Using Model Checking.* Proceedings of IEEE International Conference on Automation Science and Engineering CASE'2009. pp. 415-420, 2009.

Alexey Voronov, Knut Åkesson. *Verification of Supervisory Control Properties of Finite Automata Extended with Variables.* Technical report. Göteborg: Chalmers University of Technology, 2009.

Alexey Voronov, Knut Åkesson. *Supervisory Control using Satisfiability Solvers.* Proceedings of 9th International Workshop on Discrete Event Systems WODES'2008, pp. 81-86, 2008.

List of Acronyms

AI	–	Artificial Intelligence
API	–	Application Programming Interface
BDD	–	Binary Decision Diagram
BMC	–	Bounded Model Checking
BOM	–	Bill of Materials
CNF	–	Conjunctive Normal Form
CSP	–	Constraint Satisfaction Problem
CTL	–	Computation Tree Logic
DNNF	–	Decomposable Negation Normal Form
sd-DNNF	–	Smooth Deterministic DNNF
EFA	–	Extended Finite Automaton
FPT	–	Fixed Parameter Tractability
FSA	–	Finite State Automaton
IUR	–	Item Usage Rule
LTL	–	Linear Temporal Logic
MDD	–	Multivalued Decision Diagram
MUS	–	Minimal Unsatisfiable Subformula
PDM	–	Product Data Management
PLM	–	Product Lifecycle Management
SAT	–	Boolean Satisfiability Problem
SCT	–	Supervisory Control Theory
SMI	–	Set of Mutually-Exclusive Required Items

Contents

Part I

Introductory chapters

Chapter 1

Introduction

Modern manufacturing is very challenging. On one hand, broad competition pushes manufacturers to keep costs down. One of the most widespread practices for keeping costs down is mass production, pioneered by Henry Ford more than a century ago. By extreme standardization and unification it is possible to reduce costs. A famous quote by Ford (1922) says: “Any customer can have a car painted any colour that he wants so long as it is black”, which emphasizes standardization. On the other hand, customers want individualized solutions. For example, a buyer of a commercial truck knows how the vehicle will be used, and does not want to pay for extra cargo capacity or driving range. Such individualization contradicts mass production.

Mass customization, envisioned by S. M. Davis (1987), bridges the gap between mass production and custom-made products. Mass customization is a production strategy focused on the broad provision of personalized products and services produced almost as cheaply as mass products (Pine II et al. 1993; Piller and Stotko 2002; Hvam et al. 2008; Fogliatto et al. 2012). The key to implementing mass customization is to use *product families* and *product platforms*. A product family is a group of related products that is derived from a product platform to satisfy a variety of market niches (Simpson et al. 2006). A product platform is a “set of common components, modules, or parts from which a stream of derivative products can be efficiently developed and launched” (Meyer and Lehnerd 1997). The process where customer needs are matched to the company’s standardized components and procedures is called *configuration*. Configuration, according to Mittal and Frayman (1989), is “a special type of design activity, with the key feature that the artifact being designed is assembled from a set of pre-defined components that can only be connected together in certain ways”. Given the complexity of most modern products, configuration would be almost impossible without information system support.

There are different approaches to implement information systems for configuration. Sabin and Weigel (1998) divide them in three groups: *case-based*, *rule-based* and *model-based*. Case-based systems (Kolodner 1992) store all previously sold products as cases, and use these cases as a basis for each new order, possibly making necessary design adaptations either manually or automatically. The advantage of case-based systems is that they do not require large amounts of work upfront for designing a product platform. However, the absence of a carefully designed platform prevents the manufacturer from fully realizing the benefits of unification and economy of scale. Rule-based systems (Hayes-Roth 1985) use *production rules* of the form IF *condition* THEN *consequence* to encode what actions should be performed to obtain a valid configuration, and when each action should occur with respect to other actions. Rule-based systems suffer from severe maintenance problems (Barker et al. 1989) due to the tight coupling between the domain knowledge and the inference engine, both encoded in the same set of rules. Model-based systems were developed to address the limitations of case-based and rule-based systems. The main assumption of model-based system is the existence of a *model* of the product being configured. Such a model consists of decomposable entities and interactions between their elements. The model facilitates the separation between what is known and how the knowledge is used (Hamscher 1992).

Model-based systems can be further sub-classified. The models for model-based configuration can be created using *description logic* (McGuinness and Wright 1998; McGuinness 2003), *features* (Kang et al. 1990; Thiel and Hein 2002; Batory 2005), *ontologies* (Asikainen et al. 2007; Yang et al. 2008), *answer set programming* (Soininen et al. 2001), *preference programming* (Junker and Mailharro 2003) and *constraints* (Mittal and Frayman 1989; Junker 2006). This thesis focuses on constraint-based systems. Constraints provide a simple yet flexible and powerful framework for modeling rapidly-changing products (Schuh et al. 2009). Constraint-based systems are widely used in automotive manufacturing companies like Renault (Amilhastre et al. 2002; Astesana, Cosserat, et al. 2010), DaimlerChrysler AG (Sinz et al. 2003) and Volvo Trucks (Lindroth 2011).

High complexity of constraints, as well as frequent introduction of new products and components, makes manual handling of configuration constraints error-prone and time consuming. Software tools can help engineers analyze and maintain configuration constraints. A number of methods and tools have been reported in the literature that aim to help engineers, including tools for verification and validation of knowledge-based systems (Gupta 1993; Preece et al. 1997; Tsai et al. 1999; Desharnais et al. 2011), verification of automotive configuration data (Amilhastre et al. 2002; Sinz et al. 2003; Astesana, Bossu, et al. 2010; Astesana, Cosserat, et al. 2010), visualization tools for dealing with decisions that cannot yet be automated (Baumeister and Freiberg 2010), virtual builds (Fuxin 2005), automatic analysis of feature models (Benavides et al. 2010), and refactoring of feature models (Alves et al. 2006; Thüm et al. 2009). However, being specialized, these methods and systems do not cover all possible configuration problems. For example, to the best of authors knowledge, the problem of efficient enumeration of valid partial configuration has not been addressed, and the problem of supporting engineers in analyzing constraints and possibly improving them was not covered exhaustively.

This thesis focuses on the following research questions:

1. What kind of computer support can be implemented to help engineers maintain, verify and analyze product configuration constraints? (Approached in Papers 1, 2 and 3).

2. How to enumerate valid partial configurations efficiently? (Paper 3).

3. How to compactly represent product configuration data for answering product configuration questions efficiently? (Approached in Chapters 4 and 5).

The amount and complexity of constraints make analysis computationally demanding: there might be tens of thousands of constraints and 10^{100} of possible products. Moreover, configuration problem can often be seen as a generalization of the well-known problem of Boolean satisfiability[1], which is a classical problem that belongs to the set of NP-complete problems (Cook 1971), and to date there is no algorithm known that can solve an arbitrary problem instance with a time complexity that is better than exponential in the size of the input (Hertli et al. 2011). However, there is a lot of work done on handling practical instances of NP-complete problems, for example, in the hardware verification community (Burch et al. 1990), which resulted in efficient methods to solve generic satisfiability problems. These methods include, for example, Binary Decision Diagrams (Bryant 1986), Boolean Satisfiability Solvers (Biere, Heule, et al. 2009) and Constraint Programming (Apt 2003; Dechter 2003). This thesis identifies important challenges in working with configuration constraints that can be tackled using recent advancements in methods and tools for solving satisfiability problems.

The main contributions of this thesis are:

1. A number of methods for automatic verification of configuration constraints and for computational support of manual inspection of constraints (Paper 1).

2. A method for verifying the correctness of one specific type of constraints (Item Usage Rules) for sets of mutually-exclusive required items, and a method for automatic verification of equivalence of different formulations of the constraints (Paper 2).

3. Three methods for enumerating valid partial configurations efficiently, and benchmarking of the methods on an industrial dataset (Paper 3).

4. A novel encoding of configuration data that allows checking the validity of partial configurations without exhaustive search, by using Supervisory Control Theory introduced by Ramadge and Wonham (1989); the encoding is suitable for configuration tools that are interactive (Chapter 5).

5. A method for solving Supervisory Control Theory problems—namely synthesis of deadlock-free and controllable supervisors—using Boolean satisfiability solvers (Paper 4).

[1] It is difficult to give a precise reference for Boolean satisfiability problem: logic as a science dates back to Aristotle (384-322 B.C.) (Johansen and Rosenmeier 1998); Boolean functions and variables are named after George Boole (1815-1864) who laid the foundations for an algebraic notation for logic, and this notation was later popularized by William Stanley Jevons (1835-1882) (Gardner 1958); the most widely-cited algorithm that initiated active research in computer methods for solving Boolean satisfiability problem is due to M. Davis and Putnam (1960). More historical notes can be found in the book "Logic machines and diagrams" by Gardner (1958), and more details about the state-of-the-art in Boolean satisfiability can be found in "Handbook of Satisfiability" edited by Biere, Heule, et al. (2009)

6. A prototype implementation of a product configuration engine.

The methods presented in this thesis were implemented in a prototype for rapid experimentation with configuration problems. Methods for enumerating valid partial configurations (Paper 3) and for explaining invalid partial configurations (Paper 1) were further developed for an automotive company by a spin-off company from this research project, Confirmlogic AB, and a pilot project for integrating the methods into daily work process was initiated at that automotive company.

This thesis consists of two parts. Part I is a general introduction to the field and puts the appended papers into context, except for Chapter 5, which has not been published before and is a novel contribution of this thesis. Part II contains the appended papers.

Chapter 2

Challenges in working with configuration constraints

Creation and maintenance of configuration constraints is an important part of development of mass-customized products. The constraints have to be developed before the sales process can start, to specify what can and can not be produced. While ordering the product, a customer can customize or configure the product within the configuration constraints. Once a customer orders a product, the assembly process typically starts. This workflow is illustrated in Figure 2.1.

The process of developing configuration constraints consists of three steps, as illustrated in Figure 2.1: authoring, verification and validation, and release (Watts 2012; *VDA 4965* 2010). Among these tree steps, the main contributions of this thesis are in the second step (verification and validation), but some contributions affect also the authoring step. The third step (release) is where configuration constraints are made available for use by sales and manufacturing departments. The following sections introduce the authoring and the verification and validation steps.

2.1 Authoring

Authoring of configuration constraints can be seen as a knowledge acquisition activity of Knowledge Based Systems. According to Neubert (1993), authoring consists of four standard steps: *elicitation, interpretation, formalization,* and *implementation.* A request to modify a product initiates the *elicitation* step, where a product design engineer, acting as a domain expert, creates a natural language description of what should be done. The natural language description is then translated into a semi-formal description in the *interpretation* step. The interpretation step is needed between the elicitation and formalization steps, as a mediator between knowledge (or information technology) engineers and domain experts (represented by product design engineers) (Angele et al. 1998). In the *formalization* step, a formal logic description of the constraints is created from the semi-formal description. In the last step, *implementation*, the constraints are stored in an information system, for example, by typing the constraints into an editor.

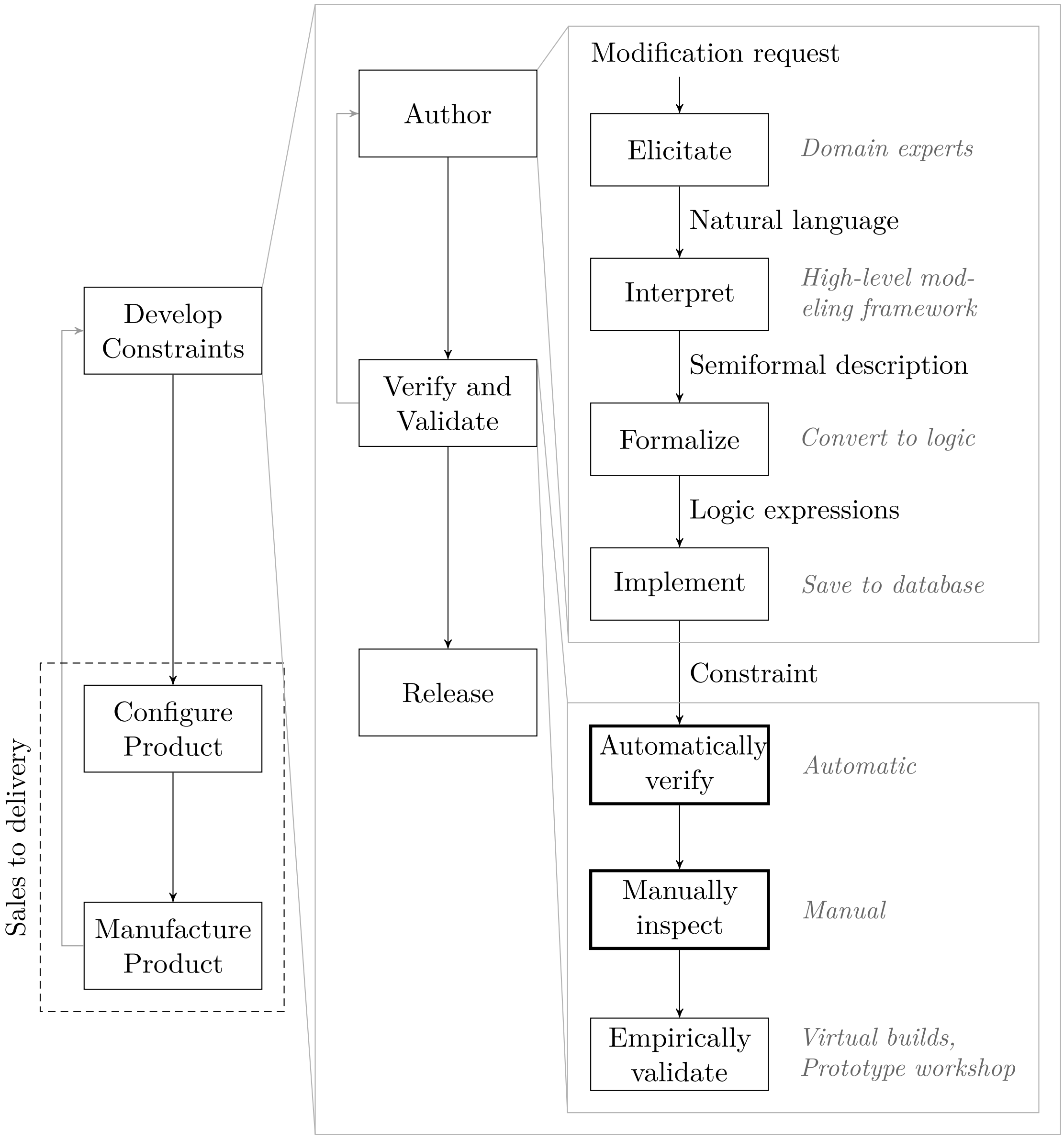


Figure 2.1: Configuration constraints workflow.

Product design engineers author two types of constraints, according to the two tiers of configuration introduced by Haag (1998): high-level customer oriented configuration constraints and low-level manufacturing oriented configuration constraints. The high-level constraints are eventually released for use by the sales department, while the low-level constraints that specify which parts to use for which customer order—together with drawings, assembly instructions and other necessary information—are released to the manufacturing department. This process is illustrated in Figure 2.2.

In the high-level customer-oriented configuration, products are broken down into configurable parts and features referred to as *families*. In a valid product, each family assumes exactly one *variant* from a predefined finite set. Later we give a formal definition to these terms. Combinations of variants will from here on be called *configurations*. A *complete* configuration has exactly one variant assigned to each family in the complete set of families. A *partial* configuration has variants assigned to some families, but not to all. Some configurations are not technically buildable, and some are not desirable for marketing or legal reasons. Configurations that fulfill all limitations are called *valid*. A partial configuration is *valid* if it can be extended to a valid complete configuration. *Variant constraints* define which configurations are valid and which are invalid.

An example of how high-level configuration constraints might look is shown in Table 2.1. The constraints appear in several stages. The first stage is *Authorization*, its constraints specify which variants are allowed for each product type, where a *product type* is a coarse partition of products into types. For example, for an automotive manufacturer such types could be sedan “S60” or station wagon “V70”. The second stage, *Irrelevant configurations*, are constraints that come from marketing, planning and legal departments, which specify configurations that are not to be sold, thus should not be designed. Such irrelevant configurations are depicted by the connected arrows in Table 2.1. For example, the 1.2L engine should not be combined with the *Sport* model. The third stage is where engineers add constraints that forbid some configurations due to engineering reasons, for example, physical constraints or safety, such as the *Sport* model is not to be manufactured with *Diesel* engine. Partial configurations forbidden by engineers are also depicted by connected arrows in Table 2.1.

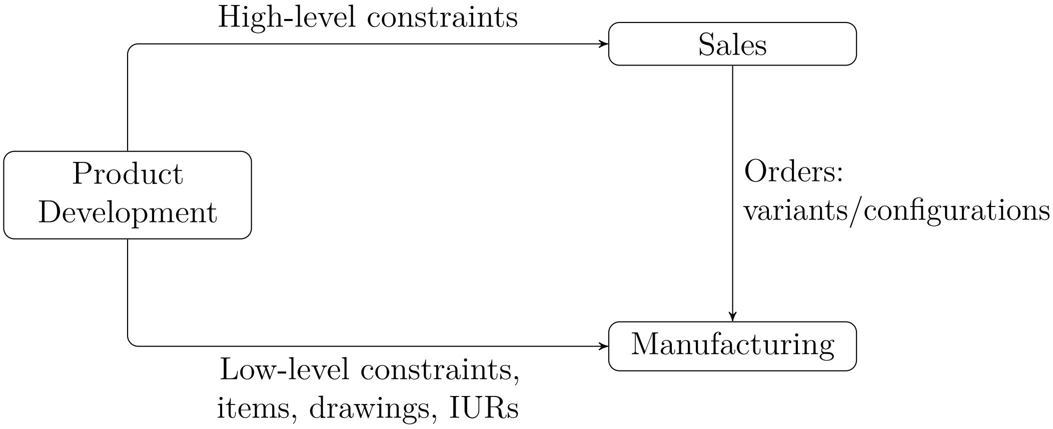
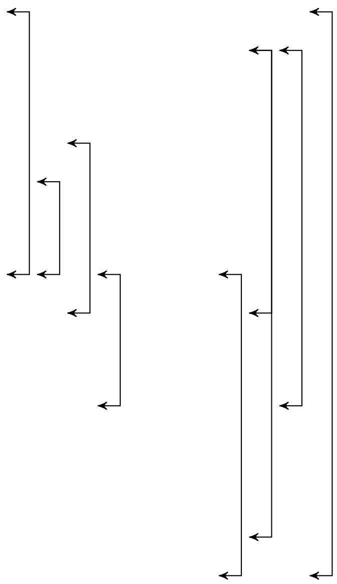

High-level constraints
Sales
Product Development
Orders: variants/configurations
Manufacturing
Low-level constraints, items, drawings, IURs

Figure 2.2: Two-tier configuration.

Table 2.1: Example of possible configuration constraints. *Authorization* constraints specify product type to variant relation. *Irrelevant configurations* constraints specify which configurations are forbidden by, for example, marketing, planning and legal departments. *Engineering restrictions* constraints specify which configurations are forbidden due to engineering reasons.

Families and Variants	Authorizations by Product Type			Irrelevant configurations	Engineering restrictions
	Type A	Type B	Type C		
Volume					
1.2	✓	✓	✓		
1.6	✓		✓		
Turbo					
Yes	✓	✓	✓		
No	✓	✓	✓		
Sport					
Yes	✓	✓	✓		
No	✓		✓		
City					
Yes	✓	✓	✓		
No	✓		✓		
Fuel					
Gasoline	✓	✓	✓		
Diesel	✓	✓	✓		



In the low-level manufacturing-oriented configuration, the structure is defined by *items*. Each item can be either included or not in a *Bill of Materials* (BOM). *Item Usage Rules* (IURs) define which items are selected for each concrete product based on the customer selection of variants for families. IURs, in the form presented here, were reported to be used in automotive industry in (Tidstam and Malmqvist 2010). An IUR is a production rule of the form IF *condition* THEN *item*, where *condition* is a complete or partial configuration (from the high-level customer-oriented tier) that triggers the inclusion of the *item* into the BOM. IURs can be considered as a method for encoding part lists; for a comparison of a number of methods of encoding part lists see, for example, (Sinz 2006). An example of IURs is shown in Table 2.2, where each line contains one IUR. The left part of the table (*Families and variants*) contains the *inclusion condition* part of the IUR, and the right part contains the item to be included in a BOM. For example, the first row of Table 2.2 says that IF the customer ordered family *Volume* to take variant *1.6*, *Turbo* and *Sport* families to take variants *Yes*, and family *City* to take variant *No*, THEN the 1.6L turbocharged engine item denoted *E16T* should be included into the BOM for assembly. An item, such as *E12* in Table 2.2, can be included by several IURs, and identical inclusion conditions can participate in different IURs, thus forcing inclusion of several items.

Table 2.2: IURs. In each row a condition for including an item is specified. For example, the first row specifies that if Volume=1.6 and Turbo=yes and Sport=yes and City=no and Fuel=gasoline then and only then item E16T should be included. For multi-row items (*E12* in this example), an item is included if and only if any of the rows is satisfied.

Families and variants					
Volume	Turbo	Sport	City	Fuel	*Item(s)*
1.6	yes	yes	no	gasoline	*E16T*
1.6	no	no	no	diesel	*E16D*
1.2	no	no	yes	gasoline	*E12*
1.2	no	no	no	gasoline	*E12*

All configurations that are valid with respect to high-level configuration constraints have to be fully designed on the low-level, including specifications of items, IURs and detailed items designs, to be ready for a customer order. This is a so-called *assemble-to-order* strategy, which requires all designs for products that customers can order to be done beforehand, as opposed to an *engineer-to-order* strategy, where a design is created only when a customer orders it. Assemble-to-order allows shorter delivery times compared to engineer-to-order, and is thus the strategy of choice in most automotive companies. However, in the truck industry some companies combine assemble-to-order with more individual solutions that may require additional engineering support.

There can still be a large number of allowed configurations even after authorizations and other constraints have removed many configurations. For instance, there are about 10^{21} possible "Renault Trafic" vehicles (small delivery vans) at Renault (Astesana, Cosserat, et al. 2010), and at least 10^{103} car configurations possible to order for the E-class line of Mercedes-Benz (Kübler et al. 2010). Such a large number of complete vehicle designs is impossible to create explicitly. Instead, the product is broken down into loosely coupled *function groups*, and the complete design of a product is a set of designs from function groups. If we take a hypothetical example of breaking down a product into 20 function groups, and if each function group can be represented by one design chosen from 10, then these $20 \times 10 = 200$ (sub)designs will describe 10^{20} complete products. To implement such product breakdown, each function group is connected with a subset of families. Engineers in a function group have to create detailed designs for all valid partial configurations only within the subset of families. To conform to the assemble-to-order strategy, an engineer responsible for a function group has to prepare all design documents beforehand for all possible valid partial configurations within the function group. If some partial configurations cannot possibly result in a valid product, for example, due to physical limitations, an engineer has to create constraints to prevent customers from ordering such configurations.

Engineers rarely create the whole product platform from scratch. Instead, they do incremental additions to the product offering. Consider, for example, introducing a car with an electrical engine, or even with a hybrid powertrain. To introduce a new engine, it is necessary to add a new variant to the families responsible for the engine. Most likely, the new engine will not work for all configurations, thus it is necessary to add some variant rules to specify when the new engine can be selected. It is also necessary to create IURs that will specify concrete items to be used in the assembly whenever a customer selects a configuration with the new variant.

There might be several problems with the new constraints and IURs, for example, they might forbid configurations that otherwise should be valid, or they can allow something that will not be possible to assemble, or the new rules might simply be redundant and unnecessary. Some of these problems can be discovered as late as on the manufacturing floor, which might result in costly manual adjustments or re-negotiations of the order with the customer. To prevent proliferation of errors from development to manufacturing, the configuration data should be fully verified and validated before it is released to the sales and manufacturing departments.

2.2 Verification and validation

Once the constraints have been authored, the next step in configuration constraints development is verification and validation. According to Boehm (1984), verification is ensuring that the system is built right, while validation is ensuring that the right system is built. Meseguer and Preece (1995) clustered verification and validation activities into four groups: inspection, static verification, empirical testing and empirical evaluation. *Inspection* is performed manually by domain experts—"by eye"—to detect semantically incorrect knowledge in the knowledge base. By manual inspection we will also mean activities involving computational methods that nevertheless require domain expert knowledge to make a decision about the correctness of the system. *Static verification* checks the consistency of a knowledge base using computational support. *Empirical testing* checks correctness by executing the system on sample data sets. Static verification and empirical testing are both combined in this thesis into a group *automatic computation*, since both have potential to be performed automatically, that is, by a software tool, algorithmically, without user intervention. *Empirical evaluation* checks suitability of the configuration constraints for the final user, including manufacturing and sales departments. Prototype workshops and virtual builds, among other methods, can be used to perform such validation (Fuxin 2005).

The verification and validation stage of the constraints development process has gained significant attention in the scientific community, not the least for its high complexity but also due to its wide application to all knowledge-based systems. Over the years a number of tools and methods for verification and validation of knowledge based systems have been created, see e.g. (Preece et al. 1997; Tsai et al. 1999) for reviews. These tools include *consistency checkers*, which detect conflicting and redundant knowledge in a knowledge base; *completeness checkers*, which detect missing or deficient knowledge; *testing tools*, which check correctness using test cases. Despite great attention, however, these tools do not cover specific needs of design engineers in the automotive industry. Feature models (Kang et al. 1990) were proposed for use in automotive product configuration (Thiel and Hein 2002), but have not found widespread use there, possibly due to high duplication of variants and difficulties with introduction of changes, as discussed in (Bühne et al. 2004). However, feature models enjoyed a substantial amount of attention, for example as a tool for modeling software, and as such, a number of methods have been developed for automated analysis and verification. Benavides et al. (2010) reviewed 53 studies and presented a catalog with 30 operations for automated analysis of feature models. Due to a connection between feature models and constraints (Batory 2005), some of the ideas can be readily applied to support product design engineers in automotive companies. Sinz and Küchlin were the first to address the needs of product development engineers in automotive companies by introducing formal methods for verification of product configuration data (Küchlin and Sinz 2000; Sinz et al. 2003), including checks for inadmissible variants, superfluous items, inclusion of mutually-exclusive items, necessary variants and temporal consistency. Later, a number of verification questions, including consistency, validity, completeness, conflict analysis and model counting, were proposed by Astesana et al. (Astesana, Bossu, et al. 2010; Astesana, Cosserat, et al. 2010) for working with product configuration at Renault. Astesana and co-workers also proposed the development of new solvers to handle such questions, without considering how to compute the answers to these questions with the existing solvers. However, there are still problems that manufacturing companies are facing that have not been addressed in the literature. The remainder of this chapter addresses such problems.

2.2.1 Automatic verification

Automatic verification can catch errors without the need for human intervention, and may be executed every time the new constraints are introduced, or old ones changed. This subsection introduces three problems that can be addressed by automatic verification. Originally, these problems were introduced in Papers 1 and 2.

Verifying that new rules do not forbid reference configurations

The complexity and interplay between configuration constraints make it difficult to figure out whether a new constraint is "correct" or not. For example, adding a constraint that forbids configurations that should normally be valid is clearly undesirable. To help prevent situations like these, Paper 1 proposes to create a kind of a "safety net" around the rules, using a number of *reference configurations*. These configurations must always be possible to build, and if they become invalid due to some rules, then more thorough analysis is required.

The reference configurations can be either *complete*, involving variants for all families, or *partial*, with variants assigned only to a subset of families. Partial reference configurations are valid only if they can be extended to valid complete reference configurations. Verifying that a complete reference configuration satisfies a new constraint is easy, while it is much more difficult to verify whether a partial reference configuration satisfies the constraint.

Reference configurations, as well as their counter-part *forbidden reference configurations* that must always remain invalid, are illustrated in Figure 2.3. Reference configurations can also be used as positive and negative examples for model-based diagnosis (Felfernig, Friedrich, Jannach, et al. 2004).

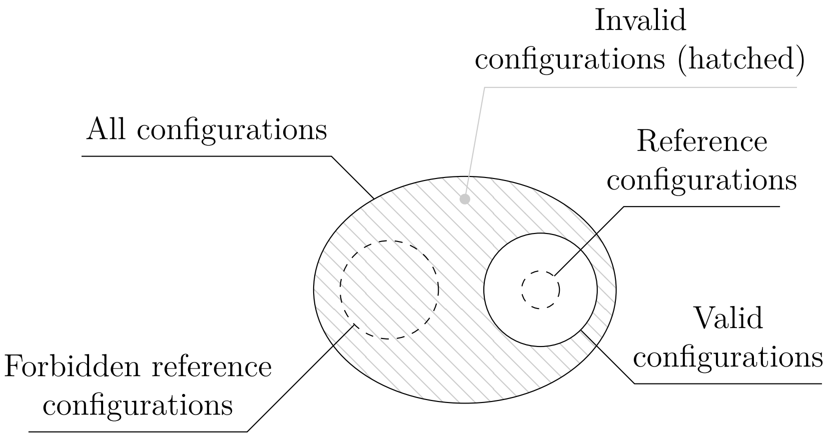
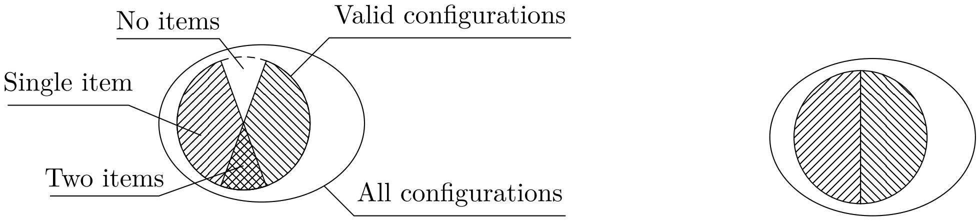


Figure 2.3: Configurations space.

Verifying Item Usage Rules for Mutually-Exclusive Items

IURs specify the connections between variants and items. Since an IUR specifies how an item depends on families' variants, but not on other items, it is easy to end up in a situation where, for example, a car has no engine. Such *at-least-one* condition for a car must be satisfied by, for example, steering wheel items, chassis items, cabin items, windshield items etc. Many of these examples also have a corresponding *at-most-one* condition, for example, a car must have only one steering wheel (there are exceptions though: hybrid cars have more than one engine, some waste collection trucks have two steering wheels etc). Together, at-least-one and at-most-one conditions form *exactly-one* conditions. A set of items that must satisfy an exactly-one condition will be called *Set of Mutually-exclusive required Items* (SMI) (Tidstam, Bligård, et al. 2012; Voronov, Åkesson, Tidstam, et al. 2012), where *mutually-exclusive* means that no two items are allowed together, and *required* means that at least one item is necessary (SMIs are also called *generic items* (Veen 1992)). Exactly-one conditions can be illustrated as in Figure 2.4, which highlights that every valid configuration should have exactly one item assigned from a SMI.

Since there is no support for defining relations directly between items, and since it is necessary to maintain backward compatibility with the existing system, Paper 2



(a) Incorrect: some configurations with one item, some with two, and some with none.

(b) Correct: disjoint and covers all configurations (ensures both *at most* and *at least* one item per configuration).

Figure 2.4: Configurations for a SMI with two items.

proposes to add verification of exactly-one condition for SMIs on top of the variant constraints and IURs, and to use such verification every time the configuration data changes.

Beyond verification: authoring Item Usage Rules using partial configurations

When authoring IURs for a SMI, it is necessary to ensure that each valid configuration will have exactly one item from the SMI. This can be ensured by verifying the exactly-one property, as described above in Section 2.2.1. However, we can also consider a systematic way to create IURs that guarantees the exactly-one condition. A systematic way to use valid partial configurations as a basis for IURs is presented in Paper 1. Valid partial configurations for a given set of families do not coincide, since two different partial configurations for a set of families will never result in the same complete configuration. Thus, IURs based on valid partial configurations will make sure that items do not overlap. Valid partial configurations could also reveal some configurations that are valid, but must be forbidden, since there is no item to assign to them. This creates an iterative process. From the variant constraints the valid partial configurations are computed, from analysis of the valid partial configurations and IURs more variant constraints are potentially created, and the process repeats. This workflow is illustrated in Figure 2.5.

Computing valid partial configurations is a computationally difficult task. One way to enumerate all partial configurations and check each of them for validity, but even to check whether a single partial configuration is valid, it is necessary to take into account all possible extensions of that configuration and see if any of them satisfies all the constraints. Only checking a partial configuration against each constraint in isolation is not enough. For example in Table 2.1, if we take partial configurations involving

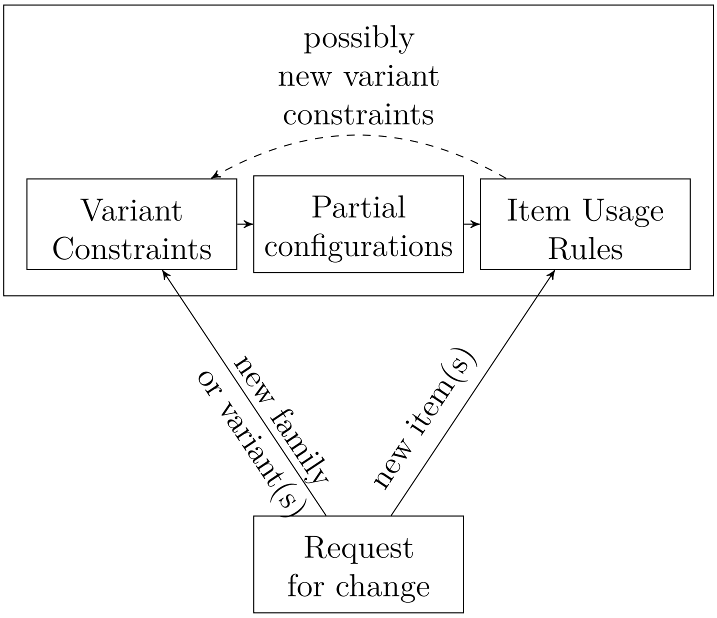


Figure 2.5: Workflow when using partial configurations to create item usage rules.

only *Volume* and *Turbo*, there is no direct constraint that connects these two families. Thus, it might seem that any combination of them is allowed. However, the partial configuration $\{$ *Volume=1.2*, *Turbo=Yes*$\}$ is not valid, because there are constraints connecting *Volume* with *Sport* and *Sport* with *Turbo*. This example illustrates that to verify properties of a subset of families it might be necessary to take into account other families as well. There could be a huge number of ways to extend a partial configuration to a complete one. For example, if there are 100 families, and a function group consists of two families, it is necessary to try all combinations of variants of the 98 remaining families, which will be 2^{98} if each family has only two variants; it is infeasible to explicitly check each of these configurations. Paper 3 introduces three efficient methods to compute valid partial configurations.

The number of valid partial configurations, and the IURs based on them, depend on the families used for partial configurations. It might be beneficial from a maintenance point of view to change the set of families used to create the IURs, but this might result in other problems, some of which are considered next.

2.2.2 Computational support for manual inspection

Apart from the automatic verification tasks introduced above, there are more tasks engineers might face, for example, authoring and modifying IURs, or discovering opportunities to improve the structure of the constraints. Such tasks can greatly benefit from computational support. For example, constraints can be rewritten automatically in different form depending on the needs of an engineer. Implicit relationships between items or families can also be made explicit automatically, as well as the effects of changes in constraints. These tasks are considered in this subsection.

Rewriting Item Usage Rules in terms of other families

When the IURs are already created, an engineer might want to rewrite an IUR in terms of other families, but keep intact the configurations for which the item is selected (Tidstam, Bligård, et al. 2012; Voronov, Åkesson, Tidstam, et al. 2012). This can be done in order to simplify and shorten an IUR, or to facilitate a better understanding of an IUR by showing it from "a different angle". Automatic rewriting from one set of families to another can contribute to the sustainability of the development by allowing different engineers to view IURs in their preferred ways.

Not all subsets of families are suitable for rewriting of an IUR. Adding more families is always safe. At worst, the size of the IUR will grow (possibly exponentially) due to the expansion of partial configurations into a number of more specific ones. Removing families, on the other hand, can lead to situations when it is ambiguous whether an item should be included or not, since when a family is removed, a number of more specific partial configurations can become a single less-specific partial configuration. Consider, for example IURs in Table 2.3a. If more families are added, a partial configuration for item *E12* splits into two more specific partial configurations, as illustrated in Table 2.3b. When some families are removed, two more-specific partial configurations become one less-specific partial configuration, as illustrated in Table 2.3c, making it impossible to create IURs that would uniquely define which item should be included.

Paper 2 introduces a way to verify that it is safe to delete a family from a given IUR, and, more generally, to verify that an alternative set of families is suitable for rewriting a given IUR.

Rewriting IURs is just one example of how constraints can be modified without changing their external behavior or meaning. The next subsection considers more such modifications.

Identifying refactoring opportunities

Software code *refactoring* is the process of changing a software system in such a way that the external behavior of the code is not altered, yet the internal structure of the code is improved (Fowler et al. 1999). The definition of refactoring can be extended to configuration constraints, where refactoring would be defined as changing the constraints without changing the valid configurations defined by the constraints, the reference configurations, or the forbidden reference configurations. The previously introduced rewriting of IURs in terms of other families can be regarded as one form of

Table 2.3: IURs.

(a) Initial IURs.

Families and variants				
Volume	Turbo	Sport	Fuel	*Item(s)*
1.6	yes	yes	gasoline	*E16T*
1.6	no	no	diesel	*E16D*
1.2	no	no	gasoline	*E12*

(b) IURs with extra family. Partial configuration for item *E12* split into two more-specific partial configurations.

Families and variants					
Volume	Turbo	Sport	City	Fuel	*Item(s)*
1.6	yes	yes	no	gasoline	*E16T*
1.6	no	no	no	diesel	*E16D*
1.2	no	no	yes	gasoline	*E12*
1.2	no	no	no	gasoline	*E12*

(c) IURs with families removed. Partial configurations for items *E16T* and *E16D* become one less-specific partial configuration.

Families and variants	
Volume	*Item(s)*
1.6	*E16T* or *E16D*
1.2	*E12*

refactoring. Paper 1 introduces more refactoring opportunities connected to the variant constraints. It should be noted that refactoring was also introduced for knowledge bases (Baumeister, Puppe, et al. 2004), which are related to configuration constraints.

Some configuration constraints might be implicit in the configuration data, or implied by other constraints. Some of such implicit constraints can be made explicit when refactoring, allowing to remove some of the presently-explicit constraints. It can also be discovered that an item has IURs, but there is no valid configuration that satisfies them, so the item is redundant and can be removed. Here is a number of refactoring questions:

- Does one item depend on another?
- Must two items always be selected together?
- Can two items ever be selected together?
- Is an item, or a variant, or a family redundant?

Answers to these questions can help engineers to understand the system and identify areas for refactoring.

What-if analysis: showing configurations that become invalid after introducing a new constraint

When adding a constraint, it might be difficult to foresee the effects of it. Unwanted side-effects may be introduced, for example, configurations that were allowed before adding the constraint may become forbidden. This may affect other teams concurrently working on the product. Thus, it is important to be able to assess the effects of adding, or removing, constraints to/from an existing constraint set. Paper 1 introduces a method to compute which valid configurations—either partial or complete—that are introduced or removed by a given modification of constraints.

2.3 Reconfiguration and Interactive Configuration

Reconfiguration is needed when a change in configuration constraints or user choices happens, and there is a need to find a new valid configuration (Crow and Rushby 1994; Männistö et al. 1999). Usually, such new valid configuration should be as close as possible to the original invalid configuration. The actual change that have to be made to the assignment is called a *repair* (Kreuz and Roller 1999; Felfernig, Friedrich, Schubert, et al. 2009; Schubert et al. 2011). Another relevant notion is *diagnosis* (Reiter 1987). Diagnoses can be used as a basis for reconfiguration (Crow and Rushby 1994), and this approach has been applied for product configuration, see, for example, (Felfernig, Friedrich, Jannach, et al. 2004). Corrective explanations (O'Callaghan et al. 2005) can also be considered as a reconfiguration. Reconfiguration is useful, for example, when dealing with aging and evolution of the product (Kreuz and Roller 1999; Manhart 2005; Falkner and Haselböck 2010; Friedrich et al. 2011), software upgrades

(Trezentos et al. 2010; Abate et al. 2012) and accommodating failures (Hadzic and Andersen 2005), as well as a feature in interactive product configuration.

Interactive product configuration (Gelle and Weigel 1996; Hadzic, Subbarayan, et al. 2004; Janota 2010) is a well-studied and widely implemented area of product configuration, and the most visible by customers. For example, a customer can configure a car on a manufacturer website, interactively choosing desired options while the configurator will ensure that the customer always selects only valid combinations of options. The user should have the possibility to choose values in any order, and the whole process should be *backtrack-free* and *complete*. *Backtrack-free* means that a user should always be able to finish the configuration procedure (select values for all variables) without a need to alter any of the earlier decisions. *Complete* means that if a configuration is valid, a user should have a way to achieve it. Interactive configuration sometimes also include a possibility to undo some of the earlier choices, we will call such actions *undo-actions*. Interactive configuration without undo-actions we will call *forward-only*. Another addition to reconfiguration can be *reconfiguration*, where an invalid configuration is changed into a valid one. During interactive configuration it can happen that the user wants to select a value that is not in the valid domain. In such a case, some of the previous choices have to be undone in order to make the new assignment valid. We will call such problem *interactive configuration with reconfiguration*. Reconfiguration can also be used outside of interactive configuration.

Enumeration of valid partial configurations, introduced in Paper 3, can be performed efficiently if there is an efficient interactive configurator. In the case of a forward-only configurator, each partial configuration can be checked for validity using the configurator. If a configurator supports undo-actions, the configurator can be used to generate a depth-first search tree from possible assignments, where each node of the tree will be an assignment of one value, and each terminal leaf of the tree will correspond to one partial configuration.

Chapter 5 introduces a novel method to efficiently represent configuration data needed for interactive configuration and reconfiguration.

2.4 Conclusions

This chapter introduced a number of problems in authoring and verification of configuration constraints that can be addressed by computational tools. Chapter 3 introduces formal methods and notation that can be used to describe these problems, and outlines how to apply the methods to the problems introduced here. Afterwards, Chapter 4 briefly introduces efficient algorithms and tools that can be used to solve large configuration instances.

Chapter 3

Introduction to Formal Methods

In computer science, formal methods are a particular kind of mathematically based techniques for systematic, rather than ad hoc, specification, design, and verification of software and hardware systems (Wing 1990). Formal methods for specification use mathematical notation to describe system requirements on some appropriate level of abstraction; formal specification can later guide the (non-formal) design process. Formal methods for verification check whether a model of a systems fulfills a given specification, usually by either examining the entire state-space of the system as done in Model Checking (Emerson and Clarke 1980; Clarke, Grumberg, et al. 2000), or by applying inference rules as done in Automated Theorem Proving (Robinson 1965; Duffy 1991). Formal design methods, called also *synthesis methods*, create a model of a system form a specification.

Formal methods have found the most widespread application in verification of hardware and software systems (Woodcock et al. 2009). In automotive product development formal methods were applied to embedded software, for example, to design and analyze a gear controller (Lindahl et al. 1998; Lindahl et al. 2001), to verify a car central locking system (Amnell and Jansson 2001), and to model and verify an infantry fighting vehicle rear ramp control system (Uckun 2011). However, if we include the use of all logic-based methods into the definitions of formal methods, then the use of many knowledge-based systems in product development—and especially the methods for their verification (Suwa et al. 1982; Gupta 1993; Preece et al. 1997; Tsai et al. 1999; Desharnais et al. 2011)—become relevant too. If we narrow the scope down to supporting automotive engineers in formally verifying correctness of the product configuration data, then the most relevant formal methods include efficient methods for representing configuration data and reasoning about it (Veron et al. 1999; Küchlin and Sinz 2000; Amilhastre et al. 2002; Pargamin 2002), as well as methods to formalize specific engineering problems and provide means to answer them (Amilhastre et al. 2002; Sinz et al. 2003; Astesana, Bossu, et al. 2010; Astesana, Cosserat, et al. 2010).

This chapter introduces constraint satisfaction, which is used in this thesis to model configuration data and to answer many verification questions. This chapter also introduces a synthesis method that is used in Chapter 5 to represent the configuration data for answering some of the configuration questions.

3.1 Constraint Satisfaction

We encounter constraints in everyday life, for example, when determining a seating arrangement for a dinner party, or when choosing a movie that a large group of friends will like. Constraint problems have three characteristic attributes: *variables*, their *domains* and *constraints*. *Variables* are objects that can take on a variety of values. The set of possible values for a given variable is called its *domain*. For the dinner party seating arrangement problem we may use chairs as variables. Each variable has the same domain – the set of all guests. *Constraints* impose limitations on the values that a variable, or a combination of variables, may be assigned. An example may be that the host and the hostess must sit at the two ends of the table, and that a feuding pair of guests should not sit next or opposite to each other. Many problems can be modeled in more than one way. For example, in the seating arrangement the guests may be the variables instead of the chairs, with the chairs being the domain of each variable. Such modeling difference is not important in the seating example due to a one-to-one correspondence between guests and chairs, but for other problems it might matter. A model that includes variables, their domains and constraints is called a *constraint problem*[1].

A *solution* or a *valid assignment* is an assignment of a single value from its domain to each variable such that no constraint is violated. A problem may have one, many, or no solutions. A problem that has one or more solutions is *satisfiable* or *consistent*. If there is no possible assignment of values to variables that satisfies all the constraints, then the problem is *unsatisfiable* or *inconsistent*.

Typical analysis of constraint problems is to determine whether a solution exists, finding one or all solutions, finding whether a partial instantiation can be extended to a full solution, and finding an optimal solution relative to a given cost function. Such tasks are referred to as *constraint satisfaction problems* (CSPs).

CSP for finite-domain variables belongs to the set of NP-complete problems (Cook 1971), and to date there is no algorithm known that can solve an arbitrary problem instance with a time complexity that is better than exponential in the size of the input (Hertli et al. 2011). However, if a problem instance possesses special structure (for example Horn formulas or 2-SAT, see Section 4.4), then the instance is polynomial-time solvable (Aspvall and Plass 1979; Dowling and Gallier 1984; Maaren 2000). The industrial problems that we tested do not belong to any of the known polynomial-time solvable classes. However, many solvers were still able to solve the industrial problems in a very short time (much faster than theoretically-predicted worst-case running time). Section 4.4 attempts to provide an explanation for that discrepancy.

The following section introduces the formal notation for constraint satisfaction.

[1] Freuder and Mackworth (2006) attribute the emergence of constraint satisfaction as a new paradigm within artificial intelligence and computer science to the 1965 paper by Golomb and Baumert "Backtrack programming" (Golomb and Baumert 1965).

Formal notation

Formally, a CSP is a triple $\mathcal{P} = \langle X, D, C \rangle$, where $X = \langle x_1, x_2, \ldots, x_n \rangle$ is an n-tuple of variables, $D = \langle D_1, D_2, \ldots, D_n \rangle$ is an n-tuple of corresponding finite domains, and $C = \{C_1, C_2, \ldots, C_J\}$ is a set of constraints. A constraint C_j is a pair $\left\langle R_{S_j}, S_j \right\rangle$, where R_{S_j} is a relation on the variables in $S_j = \mathit{scope}(C_j)$, and $\mathit{scope}(C_j) \subseteq X$ is a set of variables over which C_j is defined. In other words, R_{S_j} is a subset of the Cartesian product of the domains of the variables in S_j. In this thesis the relations are limited to propositional formulas over atomic propositions $x_k = v$ where $v \in D_k$.

A solution to the CSP $\mathcal{P}$ is an n-tuple $\mathcal{A} = \langle a_1, a_2, \ldots, a_n \rangle$ where $a_i \in D_i$ and each C_j is satisfied in that R_{S_j} holds on the projection of $\mathcal{A}$ onto the scope S_j. In a given task one may be required to find the set of all solutions, denoted by $\mathit{sol}(\mathcal{P})$, to determine if that set is non-empty, or just to find any solution, if one exists. If $\mathit{sol}(P)$ contains at least one solution, the problem $\mathcal{P}$ is said to be *satisfiable*, otherwise it is *unsatisfiable*.

A *complete assignment* to a CSP $\mathcal{P}$ is a function $f : X \to D$ which is defined for all $x_k \in X$. A complete assignment f is *valid* when its codomain (the target set of f, or the values for each variable) forms a solution. A *partial assignment* to $\mathcal{P}$ is a partial function $g : X \to D$ defined for variables $x_k \in Y \subseteq X$. We will write $\mathit{scope}(g) = Y \subseteq X$ to denote the set of variables of g. We will call a partial assignment *valid* if and only if it can be extended to a valid complete assignment, i.e. there exists a function h defined for $X \setminus Y$, such that codomains of g and h together form a solution.

One of the methods to encode constraints is by using *propositional formulas* (Chrysippus (c. 279 B.C. – c. 206 B.C.) is credited for the development of a coherent system of propositional logic (Johansen and Rosenmeier 1998)). A propositional formula is a formula that consists of a single propositional literal, or is a conjunction ("and", $\wedge$), disjunction ("or", $\vee$) or negation ("not", $\neg$) of propositional formulas. A propositional literal is either a positive or negative *atomic proposition*. An atomic proposition can be, for example, an expression saying that a variable takes a specific value, like "$x = 2$", or a Boolean variable. A *Boolean variable* (named after George Boole (1815-1864) who laid the foundations for an algebraic notation, which was later popularized by William Stanley Jevons (1835-1882) (Gardner 1958)) is a variable that have domain $\{0, 1\}$, or alternatively $\{$*(F)alse*, *(T)rue*$\}$. A propositional formula that consists only of Boolean variables is a *Boolean formula*. The problem of finding an assignment to the Boolean variables such that the Boolean formula evaluates to true is called *Boolean satisfiability problem* (SAT).

A propositional formula is said to be in *conjunctive normal form* (CNF) if it is a conjunction of *clauses*, where a *clause* is a disjunction of literals; for example, $(A \vee B \vee C) \wedge (B \vee D)$ is in CNF, while $(A \wedge B) \vee C$ is not in CNF. A Boolean formula in CNF can be represented using a set notation. A clause $l_1 \vee l_2 \vee \ldots \vee l_m$ is expressed as a set of literals $\{l_1, l_2, \ldots, l_m\}$. Moreover, a CNF $\alpha_1 \wedge \alpha_2 \wedge \ldots \wedge \alpha_n$ is expressed as a set of clauses $\{\alpha_1, \alpha_2, \ldots, \alpha_n\}$. Consider the following CNF over Boolean variables A, B, C, D:

$$(A \vee B \vee \neg C) \wedge (\neg A \vee D) \wedge (B \vee C \vee D).$$

Using set notation, it can be expressed as:

$$\{\{A, B, \neg C\}, \{\neg A, D\}, \{B, C, D\}\}.$$

A CNF Δ is *inconsistent* if it contains an empty clause: $\emptyset \in \Delta$. Moreover, if a CNF Δ contains no clauses, it is *consistent*: $\Delta = \emptyset$.

A *conditioning* of a CNF Δ on a literal L, denoted $\Delta|L$, is the process of replacing every occurrence of literal L by the constant *True*, replacing $\neg L$ by the constant *False*, and simplifying accordingly. All clauses that contain L become satisfied and can be removed from Δ. All clauses that contain $\neg L$ can be simplified by removing $\neg L$ from them (as it is *False* and no longer have any effect). All clauses that contain neither L nor $\neg L$ remain in $\Delta|L$ without change. *Unit resolution* is a conditioning procedure that takes the literal from a *unit clause*, where a *unit clause* is a clause that contains only one literal.

Having the notation covered, the next subsections introduce the basic building blocks of CSP and SAT solvers. Later, Chapter 4 and Paper 4 provide more methods to handle industrial problem instances.

3.1.1 Basic constraint satisfaction solver

A general algorithm for CSP solvers is illustrated by the procedure CSP-Solve in Algorithm 3.1 (Apt 2003). The algorithm is parameterized by the procedures Preprocess, Propagate-Constraints, Happy, Atomic, Split and Proceed-by-Cases. The Proceed-by-Cases procedure recursively invokes CSP-Solve.

Algorithm 3.1 CSP-Solve

```
Preprocess
Propagate-Constraints
if not Happy
  if Atomic
    done
  else
    Split
    Proceed-by-Cases
```

The first procedure in the algorithm is Preprocess, which prepares the problem for solving. It can convert a problem formulation to the form suitable for the solver or perform simplification of the problem to speed up the future solving process.

The procedure Happy checks whether the goal for the initial CSP has been achieved. The goal depends on the applications, but the most common goals are:

- some solution has been found,
- all solutions have been found,
- an inconsistency has been detected,

- an optimal solution with respect to some objective function has been found.

Atomic checks whether it is possible to split the current problem into smaller ones. If a solution or inconsistency has been found, the problem cannot be split.

The Split procedure divides the current problem into two or more subproblems, with the union of subproblems equivalent to the current problem. Splitting can be done on the domains of the variables or on the constraints. For example, if branching is done on a variable with domain size of three, then it is possible to split the problem into three sub-problems, each of which will have to deal with a single value for the variable. As an example of splitting on a constraint, consider a constraint that is a disjunction (OR). Such disjunction constraint can be split into multiple parts, with each subproblem having only one disjunct from the complete disjunction; if the subproblem for any of the disjuncts is satisfiable, then the original problem itself is satisfiable.

Proceed-by-Cases recursively invokes CSP-Solve for each subproblem (case) produced by the Split procedure. The cases are usually treated in a depth-first manner, turning the whole solving procedure into a backtracking depth-first search (Golomb and Baumert 1965). It starts at a root node and proceeds to the first descendant. The process is repeated until either the descendant node is a leaf or an inconsistency is found. If a leaf is a valid solution, the search terminates. Otherwise, the search backtracks to the previous node and continues by selecting the next unexplored descendant. If the search backtracks to the root node when all its descendants have already been explored, the search terminates declaring absence of solutions. The search can backtrack more than one level at a time, which is called non-chronological backtracking (Stallman and Sussman 1977; Bruynooghe 1981). It is also possible to remember the reason for the conflict in order to not repeat such partial assignments in the future (Stallman and Sussman 1977; R. Davis 1984; Dechter 1986; Dechter 1990).

The Propagate Constraints procedure reduces the search tree by inferring information from existing constraints. The simplest form is *node consistency*: if there is a unary constraint (i.e. defined only over one variable), then all values that do not satisfy the constraint should be removed from the domain of the variable. *Arc consistency* (Mackworth 1977) generalizes this to binary constraints: for each value of a variable in a binary constraint there should be a value in the domain of the other variable, such that the resulting pair satisfies the constraint. *Path consistency* (Montanari 1974) uses implicit induced constraints on triples of variables, i.e. considers all paths of size two among binary constraints to prune domains. *Generalized arc consistency* is an extension of arc consistency to constraints with more than two variables in their scope. A variable is generalized arc consistent with a constraint if every value of the variable can be extended to all the other variables of the constraint in such a way that the constraint is satisfied (Freuder 1978).

The CSP architecture presented in Algorithm 3.1 is very general and allows solving a variety of problems. SAT-solvers, on the other hand, can be seen as an extreme specialization of the CSP algorithm; they are considered in the next section.

3.1.2 Basic Boolean satisfiability solver

The basic procedure for Boolean satisfiability solving was presented by M. Davis and Putnam (1960), and later modified into a more memory-efficient search procedure by M. Davis, Logemann, et al. (1962). The resulting algorithm—commonly referred to as *DPLL*, by the initials of its authors—is given in Algorithm 3.2.

Algorithm 3.2 DPLL(Δ)

```
1  input: CNF $\Delta$
2  output: SATISFIABLE or UNSATISFIABLE
3  $\Delta' = $ Unit-Resolution($\Delta$)
4  if $\Delta' = \emptyset$
5    return SATISFIABLE
6  else if $\emptyset \in \Delta'$
7    return UNSATISFIABLE
8  else
9    choose a literal $L$ in $\Delta'$
10   if DPLL($\Delta'|L$) = SATISFIABLE
11     return SATISFIABLE
12   else if DPLL($\Delta'|\neg L$) = SATISFIABLE
13     return SATISFIABLE
14   else
15     return UNSATISFIABLE
```

It is easy to see similarities between Algorithms 3.1 and 3.2. The unit resolution in line 3 of Algorithms 3.2 is a simple form of constraint propagation, which propagates all clauses that consist of a single literal (unit clauses) by conditioning the problem on those literals. Lines 4-7 of Algorithm 3.2 are a merge of both tests for Happy and Atomic. Split is implemented by choosing a literal in line 9 of Algorithms 3.2, and Proceed-by-Cases is implemented by a recursive call to the DPLL procedure on a conditioned CNF.

The original DPLL algorithm presented here was invented half a century ago. Modern efficient implementations of SAT algorithm depart from the original DPLL in various ways. An overview of some of the most important modifications is given in Chapter 4 and Paper 4. Modern SAT algorithms have very good performance, and they are often used to solve problems that were modeled as CSP (Prestwich 2009), by converting CSP to SAT. Such conversion is briefly introduced in the following section.

3.1.3 Encoding constraint satisfaction problems as Boolean satisfiability problem

Often problems are modeled using CSP, and then converted to SAT to take advantage of many efficient SAT tools (Prestwich 2009). Wide range of efficient tools use a common encoding of Boolean satisfiability problem called DIMACS CNF format. The format requires the problem to be described in terms of only Boolean variables, and the constraints have to be CNF clauses; a CSP with finite-domain variables and propositional constraints can be converted to (Boolean) SAT with CNF constraints with a polynomial increase of the problem size.

> The DIMACS CNF format is as following. The file starts with zero or more comment lines, indicated by the character `c` at the beginning of the line. After the comment lines, there is a “header string” `p cnf n m` that indicates that the instance is in CNF format; n is the number of variables; m is the number of clauses. The header string is followed by the clauses. Each clause (a disjunction of literals) is encoded as a sequence of literals, where each literal is represented by a number between $-n$ and n, the clause ends with 0 on the same line; a clause cannot contain the opposite literals i and $-i$ simultaneously. A positive number i denotes the corresponding variable x_i. A negative number $-i$ denotes the negations of the corresponding variable $\neg x_i$. An example file content for the formula $(x_1 \vee \neg x_5 \vee x_4) \wedge (\neg x_1 \vee x_5 \vee x_3 \vee x_4) \wedge (\neg x_3 \vee \neg x_4)$ can look as the following:
>
> ```
> c
> c start with comments
> c
> p cnf 5 3
> 1 -5 4 0
> -1 5 3 4 0
> -3 -4 0
> ```

To provide a brief introduction to the conversion from CSP to SAT, the encoding of finite-domain variables using Boolean variables, and encoding of arbitrary propositional formula using CNF is given in the following two sections.

Encoding finite-domain variables using Boolean variables

Two of the most widespread encodings of finite-domain variables using Boolean variables are *direct encoding* (Kleer 1989; Walsh 2000) (also called *one-hot encoding* (Biere and Kunz 2002)) and *log encoding* (Iwama and Miyazaki 1994; Walsh 2000). Direct encoding assigns one Boolean variable to each value. The Boolean variable indicates if the value is assigned to the variable or not. Thus, the number of Boolean variables is equal to the number of values in the domain. Log encoding assigns a unique integer in the interval from 0 to $n-1$ to each value in the domain, where n is the size of the domain. In this case $\lceil \log_2 n \rceil$ Boolean variables are needed to encode the values.

Direct encoding requires extra constraints to encode that exactly one value can be selected for each variable. Exactly-one constraints can be split into two constraints: at-least-one and at-most-one. At-least-one constraints can be encoded using a single disjunction of n literals. At-most-one constraints, on the other hand, is more difficult to encode. The simplest encoding of an at-most-one constraint would require n^2 disjunctions of the form $(\neg x_i \vee \neg x_j), i \neq j$, where x_i and x_j belong to the domain of the variable; this encoding is called *quadratic* in this thesis due to the number of extra constraints needed. Other encodings exist (Sinz 2005; Frisch and Giannaros 2010; Ben-Haim et al. 2012; Manthey et al. 2012), including generalizations of at-most-one to at-most-k called *cardinality constraint*. One of the encodings is *ladder encoding*

(Gent and Nightingale 2004), which introduces a linear number of new constraints and a linear number of extra variables. Ladder and quadratic encodings are used in this thesis to encode at-most-one constraints for direct encodings of finite-domain variables.

Log encoding does not require at-least-one and at-most-one constraints, as mutual exclusiveness is implicit in the encoding. However, to encode variables with domains of sizes not a power of 2, log encoding requires constraints to forbid spurious assignments that would correspond to integers between n and $2^{\lceil \log_2 n \rceil} - 1$. Despite the benefit of reduced number of variables needed by log encoding, the drawback of log encoding is that unit propagation on the log encoding is less effective than unit propagation on the direct encoding (Walsh 2000), which might result in worse SAT-solver performance.

Encoding propositional formulas into CNF

To convert a propositional formula to CNF, one can use the rules of Boolean algebra. The conversion can be exemplified by transforming formula $(A \wedge B) \vee \neg(C \wedge \neg D)$, where A, B, C, D are Boolean variables:

$$\begin{gathered}(A \wedge B) \vee \neg(C \wedge \neg D) = \\ (A \wedge B) \vee (\neg C) \vee D = \\ (A \vee \neg C \vee D) \wedge (B \vee \neg C \vee D)\end{gathered}$$

Logic transformations might result in exponential growth of the formula, for example, when converting Disjunctive Normal Form (disjunction of conjunctions) to CNF.

Another approach to convert a formula to CNF is to use Tseitin transformation (Tseitin 1968), which introduces auxiliary variables and results only in polynomial growth of the formula. For the example above, Tseitin transformation would introduce two new variables, X and Y, and the following extra formulas for the new variables:

$$\begin{gathered}X \leftrightarrow (A \wedge B) \\ Y \leftrightarrow (C \wedge \neg D)\end{gathered}$$

where $P \leftrightarrow Q$ stands for $(P \rightarrow Q) \wedge (Q \rightarrow P)$. Also, $P \rightarrow Q$ stands for $(\neg P) \vee Q$. Then the original formula can be replaced by the following clauses:

$$\begin{array}{ll}
X \vee \neg Y & \%\ \textit{Original formula} \\
(\neg X) \vee A & \%\ X \rightarrow A \\
(\neg X) \vee B & \%\ X \rightarrow B \\
(\neg A) \vee (\neg B) \vee X & \%\ (A \wedge B) \rightarrow X \\
(\neg Y) \vee C & \%\ Y \rightarrow C \\
(\neg Y) \vee (\neg D) & \%\ Y \rightarrow \neg D \\
(\neg C) \vee D \vee Y & \%\ (C \wedge \neg D) \rightarrow Y
\end{array}$$

For smaller formulas, like the one above, Boolean algebra transformations give smaller CNF, but for bigger formulas, Tseitin transformation is necessary to avoid exponential growth of the formula. Consider, for example, converting $(A \land B \land C) \lor (D \land E \land F) \lor (G \land H \land I)$, which would result in 27 clauses using Boolean algebra, and only in 13 clauses and 3 extra variables using Tseitin transformation.

Satisfiability problems are well-suited for answering verification questions. For example, SAT often serves as a target representation for answering verification questions in model checking (Biere, Cimatti, et al. 1999). However, some problems might benefit from other formal methods such as synthesis. One synthesis method, supervisory control synthesis, is introduced in the next section. Furthermore, there is a relation between verification and synthesis, and in Paper 4 we introduce the first encoding of some of supervisory synthesis problems as SAT problems. The next section briefly introduces supervisory control theory and synthesis problems.

3.2 Synthesis using Supervisory Control Theory

Verification answers only *yes* or *no* to the question whether a specification is fulfilled or not by the system, possibly with a proof for *yes*, and a counter-example for *no*. But it is possible to go further. For example, the supervisory control theory (SCT) (Ramadge and Wonham 1989; Cassandras and Lafortune 2008) provides a way to synthesize (automatically compute) a safety device, called a *supervisor*, that restricts the behavior of an uncontrolled process, the *plant*, in such a way that the desired behavior of the controlled system, a *specification*, is fulfilled. The synthesized supervisor controls the plant so that it always stays within the limits defined by the specification, by dynamically disallowing the generation of events that might lead to a behavior outside the specification, see Figure 3.1.

SCT includes a certain type of "controllability". The supervisor is mainly a safety device that prevents the plant from executing events that would take the controlled system outside the specified behavior. However, not all events can be prevented from occurring; some events are *uncontrollable*, and the supervisor must never (try to) disable any of the uncontrollable events, since these events may be spontaneously generated by the plant.

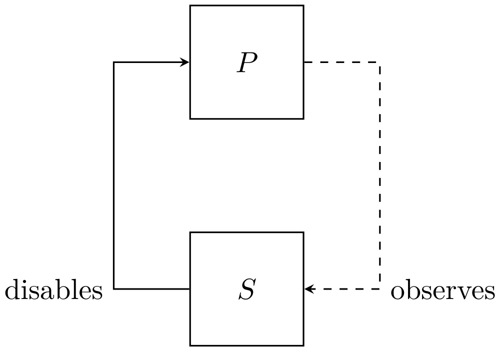


Figure 3.1: Plant P supervised by a supervisor S. P spontaneously generates events from a set allowed by S. The generated events are observed by S, which generates a new set of disabled events for P.

In addition to controllability, it is desired for the supervisor to be *non-blocking*. A non-blocking supervisor guarantees that at least one *marked* state is reachable from any state that the closed-loop system (plant and supervisor) is allowed to reach. Marked states typically represent (sub-)tasks that the system must always be able to finish.

Ramadge and Wonham (1987) have shown that for a given plant and a controllable and non-blocking with respect to the plant specification, there always exists an optimal supervisor guaranteeing that the specification will not be violated, while at the same time allowing the system to always fulfill at least one of its defined (sub-)tasks. The optimality criterion for the supervisor is to restrict the given plant as little as possible. Such a supervisor is said to be *maximally permissive* or equivalently *minimally restrictive*.

Synthesis can be viewed as a series of verification tasks, where the process model (the plant) allows an automatic alteration of the suggested, and negatively verified, supervisor candidate. The original specification can be viewed as the first supervisor candidate; if it is verified to be correct (controllable and non-blocking) then no further processing is necessary. Otherwise, a new supervisor candidate will be created by removing undesired behavior from the previous supervisor candidate, and the process repeats. Thus, by construction, a synthesized supervisor will always be verified to be correct.

SCT and CSP have some similarities. In CSP, given a set of constraints, the task is to find a set of satisfying assignments. In SCT, given a model of a plant, plus a given set of constraints (specification), the task is to find another model (supervisor), such that this model interacting with the plant satisfies the constraints.

From complexity point of view, answering whether there exist a supervisor with respect to a modular finite-state automata system that guarantees reaching a marked state is NP-hard (Gohari and Wonham 2000), and verifying the admissibility of a single supervisor with respect to a modular finite-state automata system is PSPACE-complete (Rohloff and Lafortune 2005), while CSP for finite-domain variables and SAT are NP-complete (Cook 1971).

Modeling formalism

As a modeling formalism for supervisory control theory problems, *finite state automata* may be used. Formally, a deterministic finite state automaton (*FSA*), denoted by A, is defined as a five-tuple (Cassandras and Lafortune 2008):

$$A = \langle Q, \Sigma, f, q_0, Q_m \rangle \,,$$

where Q is the finite set of *states*; Σ is the finite set of *events*, i.e. the *alphabet*, associated with the transitions in A; $f : Q \times \Sigma \to Q$ is the partial *transition function*: $f(q, \sigma) = p$ means that there is a transition labeled by event σ from state q to state p; $q_0 \in Q$ is the *initial* state; and $Q_m \subseteq Q$ is the set of *marked* states.

The transition function can be written in infix notation; for example, $q \xrightarrow{\sigma} p$ denotes a transition from state q to state p associated with event σ. This notation is further extended in the natural way to sequences of events of finite length.

The transition function, f, is partial and thus not all events are defined from all states. The *active event function* $\Gamma(q)$ denotes the set of all events σ for which $f(q,\sigma)$ is defined; this set is called the *active event set.* If $\sigma \in \Gamma(q)$ we say that the event σ is *enabled* in state q. The active event function is implicitly defined from the transition function f.

A state q_i is called *reachable* if there exists a sequence of events that leads from the initial state (q_0) to state q_i.

Typically, a model of a plant or a specification consists of different submodels focusing on different aspects. A specific composition operator *parallel composition* (also called *synchronous composition*), see for example (Cassandras and Lafortune 2008), may be used to compose a full model (plant or specification) from multiple submodels.

Parallel composition models interaction. In a parallel composition of automata, an event σ can occur only from a joint state where each automaton has σ enabled. Let $A_1 = \langle Q^1, \Sigma^1, f^1, q_0^1, Q_m^1 \rangle$ and $A_2 = \langle Q^2, \Sigma^2, f^2, q_0^2, Q_m^2 \rangle$. The parallel composition of A_1 and A_2 is the automaton

$$A_1 || A_2 = \left\langle Q^1 \times Q^2, \Sigma^1 \cup \Sigma^2, f^{1||2}, (q_0^1, q_0^2), Q_m^1 \times Q_m^2 \right\rangle .$$

The transition function, $f^{1||2}$, is defined as

$$f^{1||2}((q^1,q^2),\sigma) := \begin{cases} (f^1(q^1,\sigma), f^2(q^2,\sigma)) & \text{if } \sigma \in \Gamma^1(q^1) \cap \Gamma^2(q^2) \\ (f^1(q^1,\sigma), q^2) & \text{if } \sigma \in \Gamma^1(q^1) \backslash \Sigma^2 \\ (q^1, f^2(q^2,\sigma)) & \text{if } \sigma \in \Gamma^2(q^2) \backslash \Sigma^1 \\ \textit{undefined} & \textit{otherwise.} \end{cases}$$

$\Gamma^{1||2}$ follows from the definition of $f^{1||2}$ and is given by

$$\Gamma^{1||2}(q^1,q^2) = \left(\Gamma^1(q^1) \cap \Gamma^2(q^2)\right) \cup \left(\Gamma^1(q^1) \backslash \Sigma^2\right) \cup \left(\Gamma^2(q^2) \backslash \Sigma^1\right) .$$

Only the reachable states are of importance during analysis; thus it is common to keep only the reachable subset of $Q^1 \times Q^2$ in the composition. The parallel composition operator is associative and commutative (Cassandras and Lafortune 2008), and can thus be extended in a straightforward way to compose an arbitrary number of automata.

Controllability Let P and S be two automata. Let Σ_u be the set of uncontrollable events and Σ^S be the alphabet of S. A state $(q^P, q^S) \in Q^P \times Q^S$ in the synchronized automaton $P||S$ is controllable if the following statement holds:

$$\Sigma^S \cap \Sigma_u \cap \Gamma(q^P) \subseteq \Gamma(q^S), \textit{ assuming } \Sigma^S \subseteq \Sigma^P .$$

Uncontrollable states are the states in $P||S$ where P enables an uncontrollable event, but S disables the same event (i.e. S has the event in its alphabet, but does not have the event in the active event set of the current state). Let P be the plant and S be a specification, and Σ_u be the set of uncontrollable events. S is controllable with respect to P and Σ_u if all reachable states of $P||S$ are controllable. It is known (Ramadge and Wonham 1987) that for a given specification and plant, a supervisor, which guarantees that the entire specification can be achieved, exists if and only if the specification is *controllable* with respect to the plant. This means that the specification must be such that it can be enforced without having to (try to) disable any uncontrollable events. If the original specification is not controllable with respect to the plant, a controllable sub-behavior of the specification has to be computed. It is known that the union of all controllable sub-behaviors of a specification with respect to a plant is also controllable thus a *supremal controllable sublanguage* exists. The supervisor's task is to restrict the behavior of the plant such that the supremal controllable sublanguage is achieved. If no controllable sublanguage exists, which implies that the supremal controllable sublanguage is empty, then no supervisor exists; in such a case it is necessary to change the plant or the specification.

Non-blocking Let $A = \langle Q, \Sigma, f, q_0, Q_m \rangle$ be an automaton. A reachable state $q \in Q$ is said to be non-blocking if there is a path from q to some marked state:

$$\exists s \in \Sigma^*, \text{ such that } \exists q_m \in Q_m \text{ where } q \xrightarrow{s} q_m$$

An automaton is said to be *non-blocking* if all of its reachable states are non-blocking. In words, the system is non-blocking if from any reachable state there is a path to some marked state.

Deadlocks A reachable state $q \in Q$ is a deadlock state if there is no transition leaving the state:

$$\Gamma(q) = \emptyset.$$

In many applications it is desirable to have no deadlocks, but in some applications deadlocks arise naturally. For example, if a manufacturing system has to produce a fixed number of parts, then, after those parts are produced, the system is in a desired deadlock. Such deadlocks at the end of a set of tasks can often be avoided either by adding a transition back to the initial state, or by adding self-loops at the desired final states, or by making desired final states marked. The remaining (non-marked) deadlocks would usually indicate some undesired behavior of the system, and the need for controlling the system. Thus, the synthesis procedure should make sure that we the closed-loop system is not allowed to reach non-marked deadlock states.

Supervisor synthesis algorithm A simple algorithm for synthesis of a non-blocking and controllable supervisor (Cassandras and Lafortune 2008) starts by computing the first supervisor candidate as the synchronous composition of the plant and specification automata. Then uncontrollable and blocking states are removed from the candidate repeatedly until there are no more uncontrollable or blocking states left. This way, the resulting supervisor is controllable and non-blocking by construction.

Example: applying Supervisory Control Theory to a robot and a machine

As an example, let us consider one robot and one machine as shown in Figure 3.2. The plant consists of the two automata shown in Figure 3.3a and 3.3b that model the robot and the machine. It is assumed that the robot will spontaneously release a manufacturing part (corresponding to the *put*-event) in the machine after it has picked it up. Thus, the put-event is uncontrollable. Uncontrollable events are prefixed with an exclamation mark (!) in the figure. We would like the system to fulfill the following specification (Figure 3.3c): after each *(!)put* event there should follow event *load* followed by *unload_A*. This guarantees that the robot will not put a new part into the machine before the machine has consumed the current part. It also restricts the machine to use output buffer A only. In this example, the plant, P, is given by $Robot||Machine$ and the specification S consists of a single automaton. In general, both a plant and a specification can consist of multiple sub-plants and sub-specifications.

The full synchronous composition of R, M and S is shown in Figure 3.4. It contains two uncontrollable states, which the synthesis algorithms removes to produce the four-states supervisor. The supervisor resulting from synthesis algorithm for Robot, Machine and Specification example is shown in Figure 3.5.

The example illustrated the basic concepts of SCT, including modeling the system using finite state automata and synthesizing a controllable and non-blocking supervisor. Chapter 5 shows how to use SCT to solve product configuration problems.

3.3 Conclusions

To summarize, this chapter introduced basic mathematical concepts used in this thesis: CSP, SAT and SCT. CSP and SAT are used to represent configuration problems in Papers 1, 2 and 3. Approaches for solving large satisfiability problems arising from

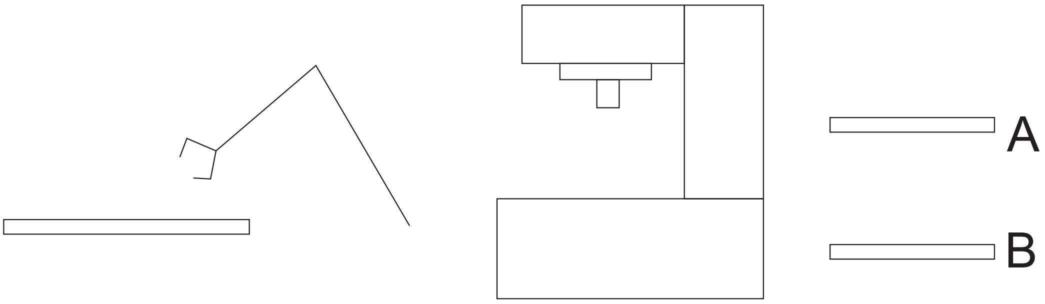
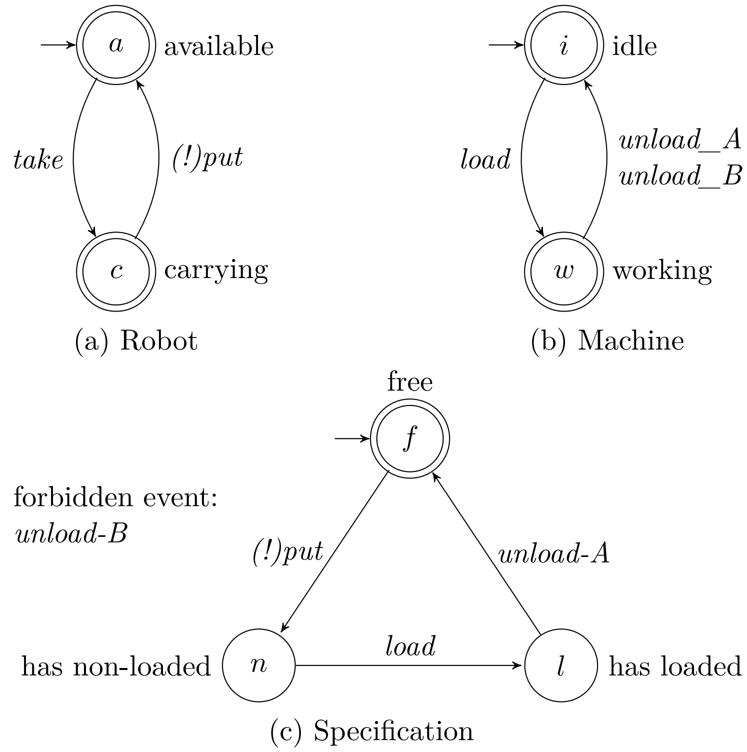


Figure 3.2: A robot and a machine. The robot takes parts from the input buffer and puts them on the machine. The machine loads the part brought by the robot, and after processing unloads it to the output buffer A or B.



(a) Robot

(b) Machine

(c) Specification

Figure 3.3: Automata models of the plant, consisting of the robot and the machine, and the specification. The exclamation mark (!) before an event name indicates that the event is uncontrollable. The alphabets are as following: $\Sigma^{Robot} = \{take, !put\}$, $\Sigma^{Machine} = \{load, unload\_A, unload\_B\}$, and $\Sigma^{Spec} = \{!put, load, unload\_A, unload\_B\}$. Note that the specification has no transition labeled *unload_B*, but this event is in the alphabet of the specification, thus *unload_B* is never allowed by the specification.

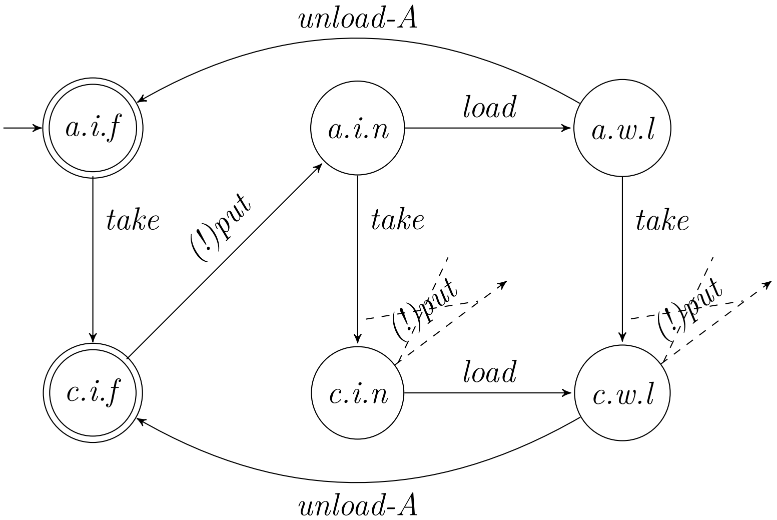


Figure 3.4: The synchronous composition $R||M||S$, with uncontrollable states $s.i.n$ and $c.w.l$ denoted by dashed crossed-out arrows pointing away from the states.

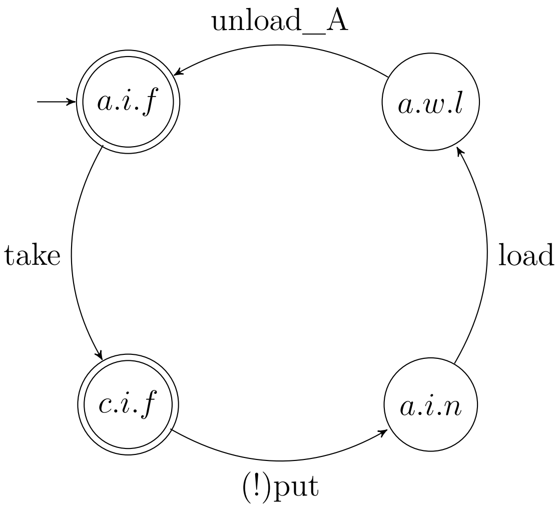


Figure 3.5: Minimally restrictive supervisor for the robot and the machine from Figure 3.3

large configuration problems are presented in Chapter 4. SCT is used to represent configuration problems in Chapter 5. Using SAT to encode SCT problems is presented in Paper 4. The next chapter looks at efficient methods to solve large problem instances arising in product configuration.

Chapter 4

Solving large-scale problems

Chapter 2 introduced some challenges in product development, and Chapter 3 introduced some techniques for formalizing product configuration problems and outlined how these techniques can be used to solve the problems in Chapter 3. This chapter briefly introduces different computational methods that were suggested for working with large-scale configuration problems, and empirically evaluates some of them. The chapter starts with the modern SAT-solvers and the key features that improved their performance compared to the basic DPLL algorithm presented in Section 3.1.2. Then, knowledge compilation methods are introduced, which separate the computations into an "expensive" offline phase and a "cheap" online phase, providing the ability to reuse the offline computation for many online queries about the same data. The chapter goes on to compare several implementations of known methods on industrial configuration data. The benchmark reveals that SAT-solvers provide answers in a much shorter time than the theoretically predicted worst-case running time, and in the last section of this chapter we investigate this discrepancy (but we have not found an answer yet, and further investigations are needed).

4.1 Search-based Boolean Satisfiability Solvers

A search-based Boolean Satisfiability Solver, or a SAT-solver, has to, given a formula in CNF, find an assignment to the Boolean variables such that the formula evaluates to true, if possible. An equivalent formulation is to say that *each clause* should have at least one literal that is true under a certain assignment. Such a clause is said to be *satisfied*. If there is no assignment satisfying all clauses, the CNF formula is said to be *unsatisfiable*. Propositional formulas that are not in CNF can be transformed into CNF using the methods discussed in Section 3.1.3.

A simple and complete SAT algorithm can be achieved by a standard backtracking search. During the search, a *partial assignment* is maintained, where some variables are assigned to 0 or 1 (alternatively to *True* or *False*), and others are unassigned. The backtracking search picks a variable, assigns it to 0 or 1 (this is called a *decision*), and repeats the procedure for the subproblem. If no solution is found, the other value is tried. If a conflict is found (all literals in a clause are false), there is no need to branch further. If all clauses have at least one literal true, then a solution has been found.

Sometime partial assignments can force the values of other variables, which is called *constraint propagation.* Consider the following three CNF clauses:

$$(\neg a \vee b) \wedge (\neg a \vee c) \wedge (\neg b \vee \neg c \vee d)$$

If a partial assignment is $a = 1$, then there is no other way to satisfy the first clause other than assign $b = 1$. In the same way the assignment is propagated to $c = 1$. Theses two assignments, in turn, will lead to $d = 1$. Such propagation takes place when all but one literal of a clause are false, and can be implemented very efficiently (Moskewicz et al. 2001).

Constraint propagation can be run after every assignment, resulting in the DPLL algorithm presented in Section 3.1.2, which until the inception of modern SAT solvers was the predominant approach to SAT.

The major differences of modern solvers from DPLL can be summarized as following:

- It is not a recursive procedure. Instead, an explicit stack of assignments is used for backtracking.
- When a conflict is found, the solver learns from it. From each conflict, a *conflicting clause* is derived and added to the set of clauses. The conflict clause strengthens the propagation without changing the satisfiability of the formula.
- Backtracking is no longer restricted to return to the previous decision. If the last k decisions were irrelevant to the conflict, all of them are undone, together with their propagated assignments.

These differences resulted in a new name for modern SAT-solvers: Conflict-Driven Clause Learning (CDCL) solvers (Marques-Silva and Sakallah 1996; Marques-Silva, Lynce, and Malik 2009).

The algorithm of a modern CDCL SAT-solver can be summarized as in Algorithm 4.1 (Claessen et al. 2008).

Algorithm 4.1 CDCL-SOLVE

```
forever:
    PROPAGATE-CONSTRAINTS
    if NO-CONFLICT
        if NO-UNASSIGNED-VARIABLE then return SAT
        MAKE-DECISION
    else
        if NO-DECISIONS-WERE-MADE then return UNSAT
        ANALYZE-CONFLICT
        UNDO-ASSIGNMENTS
        ADD-LEARNED-CLAUSE
```

Another important part of a solver is how it makes decisions. The most successful heuristic so far tries to bias decisions towards variables that were recently involved in the conflicts. This helps to find as many conflicts as possible in a small region of the search space, which should result in a set of short clauses that capture the reasons for the conflicts better than the original clauses.

The mentioned features of the SAT-solvers' algorithms and well-selected and tuned heuristics have made SAT-solvers very powerful computing tools successfully applied to many practical problems (Marques-Silva 2008). In particular, SAT-solvers were successfully used for product configuration (Küchlin and Sinz 2000; Sinz et al. 2003; Janota 2008; Janota 2010).

Often, especially in many product configuration problems, the same data is used to answer many queries, which makes starting the search "from scratch" less desirable. Instead, it is possible to keep learned clauses as in incremental solving (Een and Sörensson 2003), or to compile the whole problem into a tractable representation, as done in the knowledge compilation approaches considered in the next section.

4.2 Knowledge compilation methods

Knowledge compilation is a family of approaches that addresses intractability of many Artificial Intelligence problems. A propositional model is compiled in an offline phase in order to support some online queries in polytime. Many knowledge compilation methods exist, see, for example, (Cadoli and Donini 1997; Darwiche and Marquis 2002) for reviews, but the most widespread knowledge compilation method is Binary Decision Diagram, which is considered in the following subsection.

4.2.1 Binary Decision Diagrams

Binary Decision Diagrams (Lee 1959; Akers 1978; Bryant 1986) can be used to efficiently find a satisfying assignment to SAT. A Boolean formula can be represented as a decision tree, where nodes of the tree represent variables, and edges of the tree represent values of the variables. An example tree for the function $a \wedge b$ is shown in Figure 4.1a. Each decision node is labeled by a Boolean variable and has two child nodes called the *low child* and the *high child*, respectively. The edge from a node to a low (high) child represents an assignment of the variable to 0 (1). Terminal leafs represent the final value that the function will take when variables are assigned the values found on the path from the root of the tree to the leaf. Since the function is Boolean, there are only two unique terminal leafs: 0 and 1. By keeping only two unique leafs (and calling them 0-terminal and 1-terminal), the tree will become a rooted, directed, acyclic graph, which consists of decision nodes and two terminal nodes 0-terminal and 1-terminal. This graph is called a Binary Decision Diagram (BDD). A BDD is called *ordered* if different variables appear in the same order on all paths from the root. A BDD is said to be *reduced* if the following two rules have been applied to its graph: (i) any isomorphic subgraphs are merged, and (ii) any node whose two children are isomorphic is eliminated. In what follows, we will call such a reduced ordered BDD simply BDD. An example of such a BDD is shown in Figure 4.1b. In practice, BDDs are generated and manipulated in their fully reduced form, without ever building the decision tree. *Multi-valued decision diagrams* (MDDs)

(Kam et al. 1998) are a generalization of BDDs to variables with arbitrary finite-sized domains.

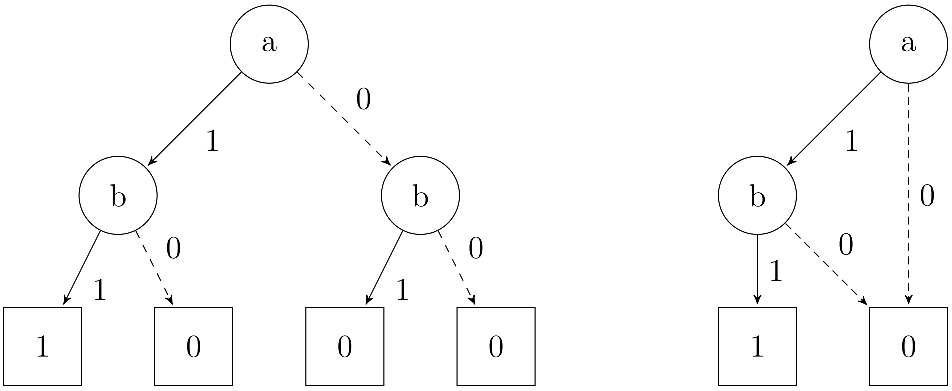
BDDs have several important benefits. First of all, it is a compact representation of a Boolean function, which saves space compared to some other representations. Secondly, it is easy to manipulate BDDs: all usual logical operations (AND, OR, NOT, NAND, etc.) can be performed directly on BDDs. A BDD with a fixed variable ordering is also a canonical representation of a Boolean function, which makes it easy to check functions for equivalences.

The disadvantage of BDDs is that they are sensitive to the variable ordering (Bryant 1986). The problem of choosing the best variable ordering is NP-complete (Bollig and Wegener 1996). An example of the difference between a good and a bad variable ordering for a BDD is shown in Figure 4.2.

Despite the fact that BDDs have been successfully used for product configuration (Hadzic, Subbarayan, et al. 2004; Subbarayan, Jensen, et al. 2004), for many practical problem instances BDDs can require a large amount of memory. Other knowledge compilation methods may provide more succinct representations of a problem instance at the expense of reduced number of supported polytime queries and transformations. Such knowledge compilation methods relevant to product configuration are outlined in the next subsection.

4.2.2 Other knowledge compilation methods

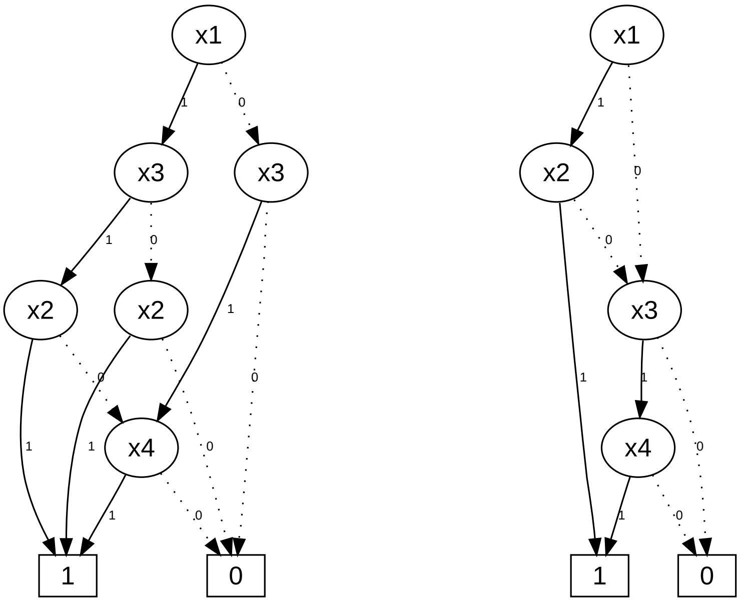
Darwiche and Marquis (2002) presented a summary of knowledge compilation methods (a "knowledge compilation map"), along with the properties of each method and polytime supported queries. Later, the map was extended with more methods, for example, Tree-of-BDDs (Subbarayan, Bordeaux, et al. 2007; Fargier and Marquis 2009). Among knowledge compilation methods, the most relevant to product configuration are Decomposable Negation Normal Form (Darwiche 1998; Darwiche 2001a), Cluster trees (Dechter and Pearl 1989; Pargamin 2002), Automata (Amilhastre et al. 2002), Multivalued Decision Diagrams (Kam et al. 1998; Hadzic and Hansen 2008), Tree-driven automata (Fargier and Vilarem 2004), AND/OR Multivalued Decision Diagrams



(a) Decision tree

(b) BDD

Figure 4.1: Decision tree and reduced ordered BDD for function $a \wedge b$.



(a) Bad variable ordering (b) Good variable ordering

Figure 4.2: Good and bad variable orderings for formula $(x_1 \wedge x_2) \vee (x_3 \wedge x_4)$.

(Mateescu and Dechter 2006) and Tree-of-BDDs (Subbarayan 2005). These data structures are briefly introduced below.

Decomposable Negation Normal Form

Decomposable Negation Normal Form (DNNF) (Darwiche 1998; Darwiche 2001a) is a data structure of which BDD is a special case. A propositional formula is in negation normal form (NNF) if and only if it is one of the following:

- a *literal*, which is a positive or negative *atomic proposition* (*atom*);
- a conjunction of formulas in NNF;
- a disjunction of formulas in NNF.

A formula in NNF is *decomposable* (DNNF) if and only if for any conjunction no atoms are shared by any conjuncts (in other words, for every conjunction the following must hold: for any two children of the conjunction, the sets of atoms do not overlap). A formula in NNF is *deterministic* (d-NNF) if for every disjunction, every pair of disjuncts is logically inconsistent (only one child of a disjunction can be true for any given assignment). A formula in NNF is *smooth* (s-NNF) if for every disjunction the set of atoms is equal to the set of atoms of each of its children (all children of a disjunction have the same sets of atoms). If a formula in DNNF is both smooth and deterministic, we write sd-DNNF.

DNNF is more succinct than BDDs and its compilation time is often shorter than that of BDDs (Subbarayan, Bordeaux, et al. 2007; Voronov, Åkesson, and Ekstedt 2011). DNNF supports smaller number of tractable operations than BDD (Darwiche and

Marquis 2002), while still allowing polynomial-time (in the size of the DNNF and/or the number of solution) counting of solutions (on sd-DNNF), existential quantification of atoms (forgetting) (Darwiche 1999) and solutions enumeration (Darwiche 2001b).

DNNF was proposed for use in product configuration for solutions (or valid configuration) counting to measure documentation maturity and estimate complexity of detecting errors in product configuration; these methods may be useful when comparing configuration data, as well as for historical analysis (Kübler et al. 2010). Paper 3 of this thesis proposes to use efficient operations on DNNF to introduce a polytime algorithm (once the DNNF is compiled) for enumeration of valid partial configurations.

Cluster trees

The cluster tree approach (Dechter and Pearl 1989) (also called join tree, junction tree, clique tree) relies on finding clusters of variables such that the interactions between the clusters are tree-structured, which allows solving the queries about a compiled problem by efficient tree algorithms. For example, cluster trees were proposed for use in product configuration at Renault (Pargamin 2002; Pargamin 2003). The same clustering idea underlines the tree decomposition used in DNNF compilation (Darwiche 1999; Darwiche 2004), which makes the result of cluster tree compilation similar to the result of DNNF compilation. Thus, we will not analyze the cluster tree approach separately from DNNF.

Automata and multi-valued decision diagrams

Automata were proposed for interactive configuration and explanation of invalid configurations by Amilhastre et al. (2002), with the compilation procedure based on the work of Vempaty (1992), who proposed to use automata to solve CSPs. Such automata closely resemble MDDs. Automata and MDDs have similar sizes of compiled representation (Hadzic and Hansen 2008), which are typically smaller than the sizes of BDDs for product configuration problems (Amilhastre et al. 2002; Hadzic and Hansen 2008). Amilhastre et al. (2002) report the size of the compiled automata representation to be 3.4 Mb vs 29.5 Mb for BDDs for the product configuration data of Renault Megane with 10^{12} valid configurations. Approximate compilation of MDDs (Hadzic, Hooker, et al. 2008) can give further space and time reductions while still providing useful data for interactive product configuration tasks. Given such properties, the methods appear to be promising, and might be a topic of future work.

Tree-driven automata

Tree-Driven Automata (Fargier and Vilarem 2004) can be compared to d-DNNF, but relaxing the requirement of only having Boolean variables. Although tree-driven automata have been proposed for product configuration (Fargier and Vilarem 2004), neither empirical evaluations nor implementations are available, which makes it difficult at the moment to estimate the benefits of this method.

AND/OR Decision Diagrams

Each node in an AND/OR BDD (Mateescu and Dechter 2006) represents a formula of the form: $(((a_1 \wedge a_2 \wedge \cdots \wedge a_n) \wedge x) \vee ((b_1 \wedge b_2 \wedge \cdots \wedge b_m) \wedge \neg x))$, where a_i and b_i are functions represented by the children of the node and x is the decision variable of the node. Hence, AND/OR BDDs define a subset of d-DNNF and satisfy the decomposable property. The AND/OR MDDs (Mateescu and Dechter 2006) are multi-valued versions of AND/OR BDDs. Compiled tree-driven automata (Fargier and Vilarem 2004) are essentially the same as (although developed independently from) AND/OR MDDs (Mateescu and Dechter 2006), with minor difference in the compilation approach, which is guided by a tree-decomposition for tree-driven automata, and by variable-elimination based algorithms for AND/OR MDDs, while variable elimination and cluster-tree decomposition are, in principle, the same (Dechter and Pearl 1989). AND/OR MDDs were proposed for use in product configuration (Mateescu, Dechter, and Marinescu 2008; Mateescu and Dechter 2008), but no empirical evaluation is available yet. Comparing performance of the tools for AND/OR MDD and d-DNNF compilation may be a topic of future work, especially since at least the binary code[1] of an AND/OR MDD compiler is available.

Tree-of-BDDs

Tree-of-BDDs is a data structure that was introduced to address the problem of huge BDDs that turn up in for many configuration problems (Subbarayan 2005). It uses tree decomposition of the constraint graph and compiles each individual BDD. The method relies on the total size of the partial BDDs being smaller than the size of the monolithic BDD. The compilation time for Tree-of-BDDs can be shorter than for d-DNNF (Subbarayan, Bordeaux, et al. 2007). However, Tree-of-BDDs supports less number of polytime operations. For example, the operation of checking the validity of an extra clause can not be performed on Tree-of-BDDs as efficiently as on sd-DNNF (Subbarayan, Bordeaux, et al. 2007; Fargier and Marquis 2009), which limits the applicability of Tree-of-BDDs for answering at least some of the configuration questions. Still, promising performance (Subbarayan, Bordeaux, et al. 2007) and available implementation[2] make Tree-of-BDDs an interesting topic for future work.

4.3 Solver benchmark

The previous sections introduced many methods that were used to tackle configuration problems. Often some tools implementing some methods are better on some problem instances, but not on all, as many comparisons show (Walsh 2000; Bennaceur 2004; Bordeaux et al. 2006; Hamadi and Bordeaux 2007; Pan and Vardi 2005; Mendonça 2009; Pohl et al. 2011). This section benchmarks several tools to find the most appropriate one to work with the product configuration data of our industrial partners in the research project. The tools were selected based on good performance in benchmarks

[1] `http://graphmod.ics.uci.edu/group/aomdd`

[2] `http://www.itu.dk/people/sathi/tob/`

within their specific disciplines, as well as on the implementation of well-known algorithms and availability of the source-code that could be investigated.

4.3.1 Testbed

For a comparison we use a truck configuration problem, we will call it Dataset A. We also use three car configuration problems from DaimlerChrysler AG, C210_FVF, C211_FW and C638_FKA (Küchlin and Sinz 2000; Sinz et al. 2003). A set of smaller problems was constructed based on Dataset A by reducing the number of constraints in it to see how the running time increases with the problem size. Dataset A has 53818 constraints and 511 variables; average domain size is 6.37. Details about the other three problems are given in Table 4.1.

The constraints in Dataset A are of two types. The first type of constraints represents forbidden combinations of values of the following form:

$$\neg\left((x_{k_1} = a_{k_1}) \wedge \ldots \wedge (x_{k_L} = a_{k_L})\right).$$

Each constraint of this type contains from two to ten values. The second type of constraints represents direct implications of the following form:

$$(\neg(x_k = a_k)) \vee (x_l = a_l),$$

Both of these two types of constraints can be directly converted to CNF clauses when using direct encoding (that is, encoding each value with one Boolean variable):

$$(\neg(x_{k_1} = a_{k_1}) \vee \ldots \vee \neg(x_{k_L} = a_{k_L})).$$

The problems C210_FVF, C211_FW, C638_FKA are in DIMACS CNF format[3], which means that all variables have Boolean domain, and each constraint is a disjunction of literals, where a literal is either a positive or negative atomic proposition.

4.3.2 Algorithms and tools

Six tools were used for the tests. The constraints were converted to a format suitable for each tool. Solvers and formats are illustrated in Figure 4.3 and described below.

[3] http://www.cs.ubc.ca/~hoos/SATLIB/Benchmarks/SAT/satformat.ps

Table 4.1: Details for problems C210_FVF, C211_FW, C638_FKA.

Problem	Boolean Variables	CNF Clauses
C210_FVF	439	1853
C211_FW	327	3186
C638_FKA	528	5346

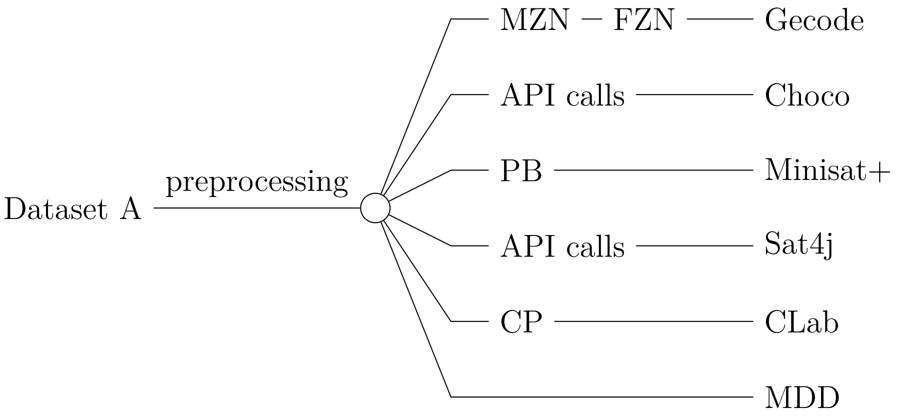


Figure 4.3: The tools and intermediate formats used. MZN, FZN – MiniZinc and FlatZinc file formats, PB – Pseudo Boolean file format, CP – CLab file format.

Two general-purpose constraint solvers were used, Gecode 3.2.2[4] and Choco 2.1.1[5]. Input data for Gecode was in MiniZinc/FlatZinc formats (Nethercote et al. 2007). MiniZinc files were created for all the problems, and then the MiniZinc files were converted to FlatZinc format using G12 MiniZinc-to-FlatZinc converter[6]. Input data of Choco was loaded via its API. Due to the direct use of the API and not a file format, all timing results for Choco exclude the time needed for reading the data from a disk, and include only the time needed to populate in-memory data structures of the solver and the time to execute the solving procedure.

As SAT-solvers, Sat4j 2.1.0 (Le Berre and Parrain 2010), Minisat+ and Minisat 2.0 (Een and Sörensson 2004; Een and Sörensson 2006) were used. The input data of Sat4j was loaded through the API, hence the disk reading time is not included in the timing results, similar to Choco. Minisat+ was used for Dataset A with input data in Pseudo-Boolean format[7] (Een and Sörensson 2006), and Minisat 2.0 was used for C210_FVF, C211_FW, C638_FKA with the data in DIMACS CNF format. The reason for using Minisat+ instead of the plain Minisat for Dataset A is that Minisat+ takes care of encoding finite-domain variables into Boolean variables.

As a BDD-based tool, CLab 1.0 (Jensen 2004b) was used with input data in the CLab file format (Jensen 2004a).

Another BDD/MDD-tool was implemented, as part of this research, in C++ using a BDD representation with logarithmic encoding of finite-domain variables. The C/C++ package BuDDy was used for this purpose (Lind-Nielsen 2002). The pre-ordering algorithms from (Narodytska and Walsh 2007) were implemented for sorting variables and constraints, using the inflation parameter $r = 1.5$ in the clustering step. A simplified version of the MCL clustering algorithm (Dongen 2000) was used, skipping the truncation heuristics and the sparse matrix multiplication tools. No post-ordering of the variables was included.

[4] http://www.gecode.org

[5] http://choco.sourceforge.net

[6] http://www.g12.csse.unimelb.edu.au/minizinc/

[7] For format description, see http://www.cril.univ-artois.fr/PB05/

Other knowledge compilation methods were not included in the benchmark due to lack of time. However, preliminary tests with d-DNNF compilers c2d (Darwiche 2004) and DSHARP (Muise et al. 2012) have shown that they can compile up to 80% of constraints of Dataset A, but both failed to compile the complete dataset due to the memory limit of 1 GB.

All tools were run with default settings and no extra tuning. It is possible to argue that it is not fair to take a solver and just use it with no tuning, especially since it was shown that automatic parameter tuning of a solver can significantly increase its performance (Hutter et al. 2009). However, the industry would like to have a trouble-free no-support tool that just works, especially since the sets of variables and constraints are changing continuously, and it might be prohibitively expensive to continuously re-tune or re-evaluate solvers.

The tools used for benchmarking were state-of-the-art at the time the experiments were conducted (2009), but at the moment of writing (2012) new tools and updates have become available. It might be a topic of future work to make new experiments with the newly available tools.

4.3.3 Benchmarking time to compile and get the first answer

In the first benchmark a solver was to answer whether there exists at least one valid configuration, and it is known in advance that there exists one for each problem (all instances are satisfiable). The main goal was to evaluate whether the compilation time for knowledge compilation methods is acceptable or not, as well as whether the search-based tools can handle the data.

The time limit for all the tools was 1 hour, and memory limit was 1 GB. All benchmark problems were executed on a 2.33 GHz Intel Core 2 Duo processor with 3.25 GB of RAM; only one core was used in the benchmark due to single-threaded implementations of the algorithms.

Results Timing results for Dataset A are presented in Figure 4.4. Timing results for problems C210_FVF, C211_FW, C638_FKA are presented in Figure 4.5. The results show that BDD and MDD based tools were not able to compile the complete Dataset A, while all search-based tools were able to successfully handle it. Runtime variation between search-based tools differed not significantly, and any of them would suit to answer whether there exist at least one valid product configuration. The results also show that Minisat+ performs worse than Minisat, with the most probable explanation being that the former solver performs a re-encoding.

Often we are interested in more intricate questions, and answering them with the help of search-based tools would require answering multiple (related) questions. Answering multiple related questions can significantly benefit from incremental solving, which is discussed in the next section.

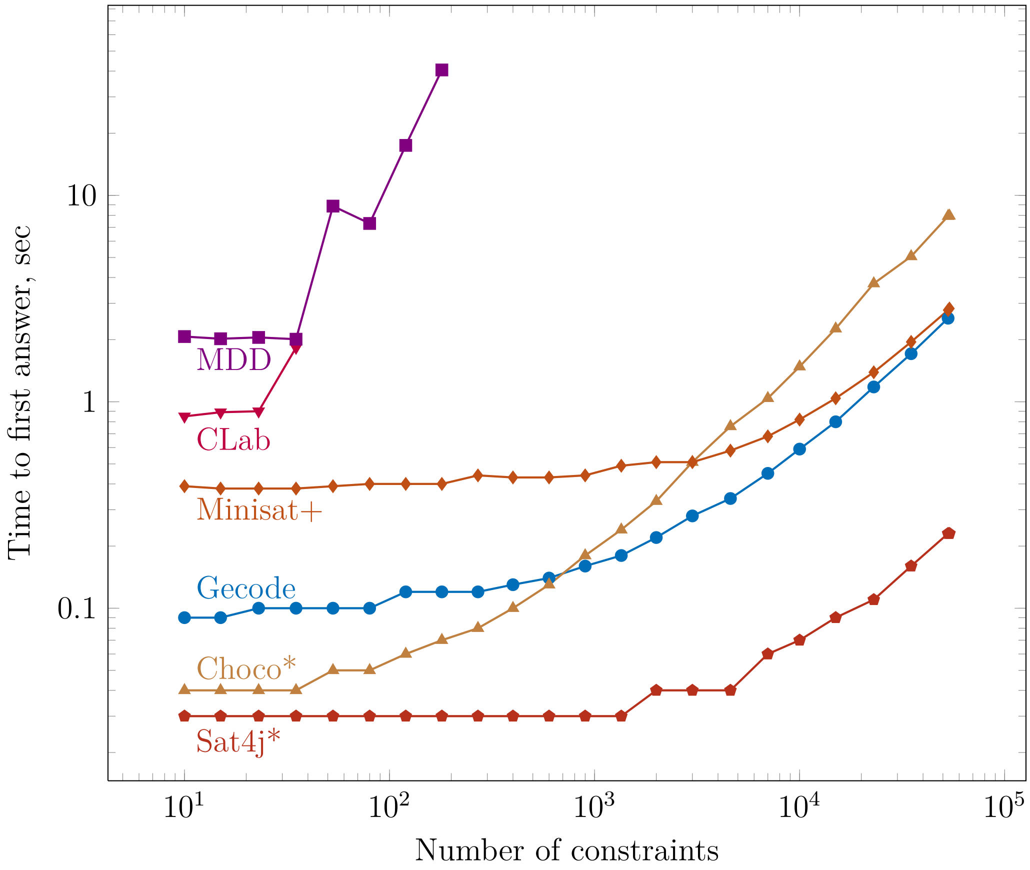


Figure 4.4: Time to get the first answer from each solver for Dataset A benchmark and its reduced versions.

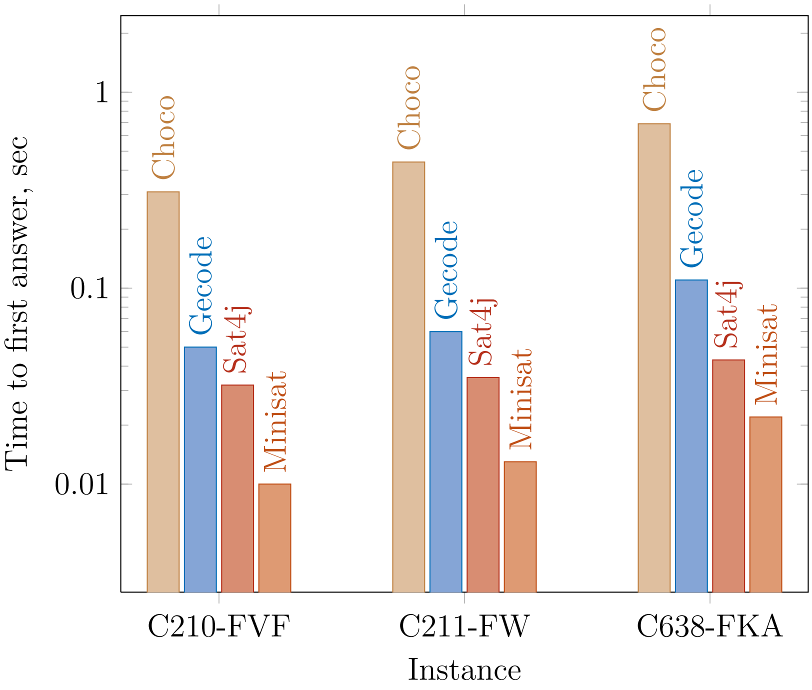


Figure 4.5: Time to get the first solution, DaimlerChrysler AG benchmarks.

4.3.4 Benchmarking time to get consecutive answers: incremental solving

Some problems can be solved by search-based solvers through iteratively solving a number of related instances. Traditional examples that require multiple SAT-solver queries are Bounded model checking (BMC) (Clarke, Biere, et al. 2001) and Incremental Construction of Inductive Clauses for Indubitable Correctness (IC3) (Bradley and Manna 2007; Bradley 2011). However, product configuration also has problems that can be solved by multiple queries to a solver, for example, enumeration of valid configurations (see Paper 3), verification of Item Usage Rules (see Paper 2), and interactive product configuration. Since solving multiple related instances is useful for product configuration, knowledge compilation methods including BDDs and MDDs seem very appealing. We wanted to evaluate whether search-based tools—especially the ones capable of incremental solving (Een and Sörensson 2003)—can come close to the performance of compiled data structures, and whether the average running time of the search-based tools is acceptable and how often the search-based tools show worst-case behavior.

Interactive configuration was chosen as a benchmark for measuring both the speed-up gained from incremental solving and the average run-time. In the interactive configuration a user selects values for the variables one-by-one, and the configurator must guarantee backtrack-freeness (no dead ends) and completeness (all valid configuration should be reachable by the user) of the process by restricting the user choices to the valid domains. We measured how long it takes to compute whether a value belongs to the valid domain of a variable. Since the configuration instance is the same, it allows reusing some inferred information between the queries.

The most widespread incremental interface of a SAT-solver is the incremental interface of Minisat proposed in (Een and Sörensson 2003), which allows forcing values for a set of variables without modifying the state of the model or data. Since user choices are exactly the assignments of values to variables, such incremental solving fits well for interactive configuration. To test whether a value belongs to the valid domain, the value is temporarily added to the user choices and forced in the solver. If there exists a satisfiable assignment, then the value belongs to the valid domain and the user is permitted to select the value. Otherwise, the value is outside of the valid domain of the variable, and the user is not allowed to select it. To test multiple values and variables, a simple simulator was implemented. It simulated user actions of choosing values for variables. Among all unassigned variables, a variable was selected randomly. The time to compute whether each value of the chosen variable belongs to the valid domain was measured. Then, one value from the valid domain was selected and fixed, and the process was repeated one level deeper. From several such simulations, the average and the maximum times were computed.

The CSP solvers considered (Choco and Gecode) had no incremental capabilities built-in. Implementing such functionality might be difficult, and even more difficult would be to maintain the codebase of a solver afterwards, since the main users of the solvers do not demand this feature, and it will be a burden for the core developer. Thus, CSP solvers were not considered in this benchmark. Incremental capability for

Gecode was implemented within a MSc thesis (Sachenkova and Thapaliya 2011), and experiments have shown that the speedup is less than the speedup achievable by a Minisat-like SAT-solver.

For MDDs, a simple test of validity of one value of one variable was taken, which was based on operations Restrict and Compute One Solution. Theoretical time bounds for MDDs predict that the run-time would be very similar between different variables and values, thus the simulator used for Sat4j was not used for MDDs.

Other knowledge compilation methods might be suitable for interactive configuration, but due to lack of time they were not included in the benchmark, and might be a topic of future work. Especially interesting is sd-DNNF with computed partial derivatives described in (Darwiche 2001b), as the use of derivatives allows to reason about changes only, without the need to reevaluate values for the complete data structure.

Results Experimental results are presented in Figure 4.6. The data shows that MDD was an order of magnitude faster than Sat4j. It also shows that there is a significant speed-up when using incremental capabilities of Sat4j compared to starting the solver "from scratch". The data also shows that the average runtime of the solver, as well as observed longest run-times, are acceptably short.

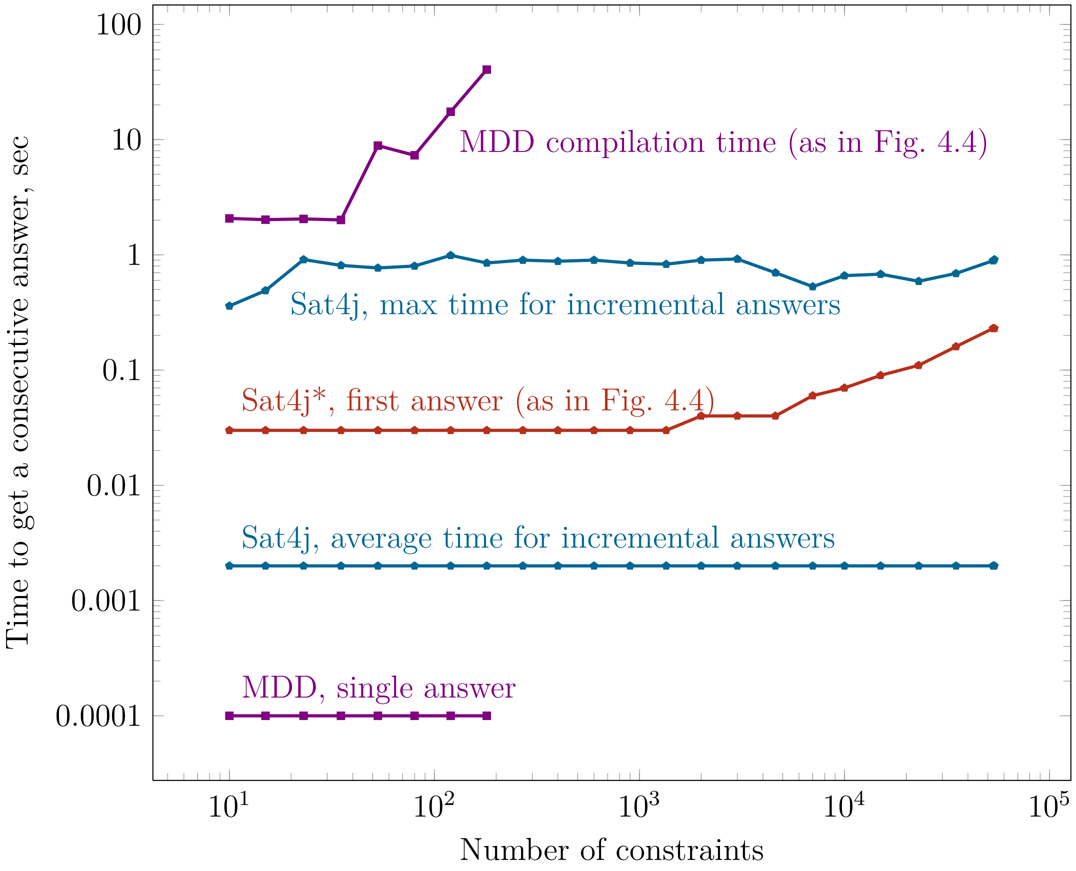


Figure 4.6: Incremental solving for Dataset A and its reduced versions.

4.4 Explaining efficiency

Our experiments have shown that SAT-solvers work very well on some industrial configuration problems (Voronov, Åkesson, and Ekstedt 2011; Voronov, Åkesson, Tidstam, et al. 2012), and not so well on, for example, supervisory control problems (Voronov and Åkesson 2008). Since both mentioned problems are similar in the number of variables and the number of constraints, the difference in SAT-solver performance must lie not in the size of the problems, but perhaps in differences in the problem structures. This section looks at *Parameterized Complexity* (Downey and Fellows 1999), which attempts to characterize problems in more refined ways than purely by the problem size as in traditional complexity analysis, allowing to better explain and predict the difference between the problems.

In classical complexity theory the computational complexity of a problem is considered exclusively in terms of the *input size*, and structural properties of problem instances are not represented. The framework of *Parameterized Complexity* addresses this issue (Downey and Fellows 1999; Flum and Grohe 2006; Niedermeier 2006). Parameterized complexity tries to find a parameter $k = \pi(F)$ of instances F that is smaller than the size n of the instance, such that there is an algorithm with running time polynomial in n, and exponential only in k, that is, $2^k \cdot n^{\mathcal{O}(1)}$. Such algorithms are called *fixed parameter tractable* (fpt) algorithms.

As an example, a typical problem in this thesis has thousands of variables and tens of thousands of constraints. The best known worst-case run-time bound for 3-SAT is $\mathcal{O}(1.321^n)$, where n is the number of variables (Hertli et al. 2011). For $n = 1000$ such a bound would suggest runtimes of order of at least 10^{100} seconds (for comparison, the age of the universe is estimated to be about 10^{17} seconds). However, the observed practical runtimes are less than a second. A possibility to explain such short runtimes would be a fpt-algorithm with polynomial runtime in n, and exponential in some fixed parameter $k \ll n$.

One important notion related to fpt-algorithms is a *backdoor* (Williams et al. 2003). A *backdoor set* is a set of variables such that when instantiated, the problem becomes “easy”, that is it simplifies to some tractable class. There is a number of such tractable classes to which original problems can be simplified, for example, Horn formulas, which have at most one positive literal in each clause, Renameable Horn formulas (RHorn), which have a variable renaming that makes a formula into a Horn formula, or 2-SAT, which have at most two literals per clause. Horn and 2-SAT are linear-time solvable (Dowling and Gallier 1984; Aspvall and Plass 1979), and RHorn is polynomial-time solvable (Lewis 1978). An algorithm that efficiently solves the simplified problem is called a *sub-solver.* A *strong* backdoor set is one for which the sub-solver can find a satisfying assignment or decide unsatisfiability for *any* instantiation of the variables in the backdoor set. A *weak* backdoor set is one for which the sub-solver can provide a satisfying assignment for *at least one* instantiation (finding such instantiation is still hard). Weak backdoors are not relevant for unsatisfiable instances, which have no satisfying assignments, while strong backdoors are relevant for both satisfiable and unsatisfiable instances. Since an instance becomes efficiently-solvable by a sub-solver after any instantiation of the variables in a strong backdoor set, the instance can be considered fixed parameter tractable with respect to the size of the backdoor set. Experiments with identification of backdoors for automotive problems were performed in (Dilkina et al. 2007; Samer and Szeider 2008; Li and Beek 2011).

Another important and widely-studied property of SAT instances is *treewidth* (Robertson and Seymour 1984), which informally can be described as a “tree-likeness” of a constraints graph. The most prominent graph representation of a CNF formula F is the *primal graph* $G(F)$. The vertices of $G(F)$ are the variables of F; two variables x, y are joined by an edge if they occur in the same clause, that is, if $x, y \in \mathrm{var}(C)$ for some $C \in F$. A *tree decomposition* of a graph $G = (V, E)$ is a tree $T = (V', E')$ together with a labeling function $\chi : V' \to 2^V$ associating to each tree node $t \in V'$ a bag $\chi(t)$ of vertices in V such that the following tree conditions hold:

1) every vertex in V occurs in some bag $\chi(t)$;

2) for every edge $xy \in E$ there is a bag $\chi(t)$ that contains both x and y;

3) if $\chi(t_1)$ and $\chi(t_2)$ both contain x, then each bag $\chi(t_3)$ contains x if t_3 lies on the unique path from t_1 to t_2.

An example of a graph and its tree decomposition is shown in Figure 4.7.

The *width* of a tree decomposition is $\max_{t \in V'} |\chi(t)| - 1$. The *treewidth* of a graph is the minimum width over all its tree decompositions. The treewidth of a graph is a measure for its acyclicity, i.e., the smaller the treewidth the less cyclic the graph is. In particular, a graph is acyclic if and only if it has treewidth 1.

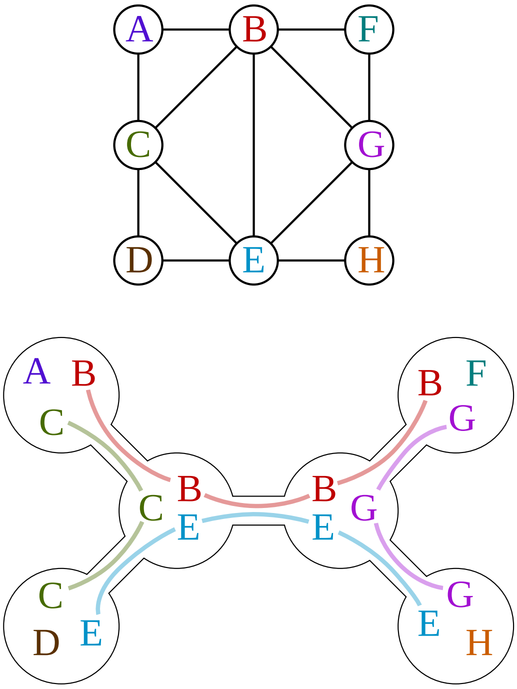


Figure 4.7: Sample graph and its tree decomposition. Adapted from (Eppstein 2007).

If its tree decomposition is given, an instance can be solved using a bottom-up dynamic programming approach on the tree decomposition, making the problem fixed-parameter tractable for instances with bounded treewidth (Gottlob et al. 2002).

The next subsection investigates the backdoor sizes and the tree-width of two industrial instances.

4.4.1 Evaluating industrial product configuration instances

Sizes of RHorn backdoors (Kottler et al. 2008; Dilkina et al. 2007) and tree-width were computed for two industrial product configuration instances. The results are shown in Table 4.2. As seen from the table, we could not find a parameter less than 75, which would suggest that the worst-case running time should be in the order of 2^{75} operations; so that if a modern computer performs about 10^9 operations per second, the running time would be more than 10^{13} seconds, which is much more than the observed running times of less than one second. To achieve one second as an upper bound, a parameter $k \approx 30$ would be needed. Thus, neither RHorn backdoor sizes nor tree-width of the instances can explain the good SAT-solver performance on these instances.

Tree-width was earlier studied as a candidate for explaining a good run-time behavior of SAT-solvers on industrial instances of the 2009 SAT competition (Mateescu 2011). It was found that many instances that were solved fast in practice have rather large tree-width (Mateescu 2011), which supports our observation that tree-width might not be suitable for explaining good performance of SAT-solvers.

Since none of the parameters we considered can explain the good experimental performance of SAT-solvers, there is a need for better problem characterization methods.

Table 4.2: Backdoor sizes and tree-width bounds for two industrial product configuration problems. Ladder and quadratic encodings of finite-domain variables are discussed in Section 3.1.3.

Property	**Problem A**		**Problem B**	
	Encoding		Encoding	
	Ladder	Quadratic	Ladder	Quadratic
General properties				
CNF variables	5901	3206	1907	1596
CNF clauses	65183	91644	9010	11270
Max clause length	108	108	60	60
Avg clause length	2.5	2.3	2.5	2.4
FPT properties				
Tree-width upper bound	488	1579	414	432
Tree-width lower bound	136	135	76	75
RHorn backdoor set size upper bound	1255	2243	398	433
RHorn backdoor set size lower bound	1255	1254	187	185

4.5 Conclusions

We evaluated several knowledge compilation tools and several search based tools for use with product configuration data from our industrial collaborator. The results show that MDD fails to compile the complete dataset within the time and memory limits, while search-based tools can successfully handle the complete dataset. SAT-solvers with incremental interface appear to work extremely well for the data we used. Other knowledge compilation methods require further investigations. We also investigated the reasons for good performance of some of the tools, and have not found yet a definitive explanation.

Chapter 5

Using Supervisory Control Theory for Interactive Product Configuration

Compiling configuration constraints into a representation that allows efficient reasoning—a technique called *knowledge compilation* introduced in Section 4.2—can save significant amounts of time when answering multiple queries on the same configuration problem. Examples of multiple queries on the same data include enumeration of valid partial configurations, interactive configuration, or in situations when multiple users use the same data. However, traditional knowledge compilation methods—like Binary Decision Diagrams (BDDs) introduced in Section 4.2.1—usually have high memory requirements, which might be a limiting factor for using compiled data structures on low-memory devices. Another application that requires small sizes of compiled data structures is a client-server architecture, where a server sends all the data necessary for configuration to a client over a limited-bandwidth channel. Applications like these motivated, for example, a technique for BDD compression (Hansen and Tiedemann 2007), a technique for compression of Multivalued Decision Diagrams (Hadzic, Hansen, and O'Sullivan 2008), and a new knowledge compilation technique—Tree-of-BDDs—based on a decomposition of the data (Subbarayan 2005). However, even more compact representations of the configuration data are desirable, and this might potentially be achievable by using a different approach – Supervisory Control Theory (SCT) introduced in Section 3.2. To the best of our knowledge, SCT, and particularly SCT synthesis, has not been used for product configuration problems before.

The product configuration tasks that are approached by SCT in this chapter are *forward-only interactive configuration*, *interactive configuration with undo-actions*, and *reconfiguration*, all introduced in Section 2.3. Moreover, efficient interactive configuration can be used to efficiently enumerate valid partial configurations too, as explained in Section 2.3.

We propose to use SCT for product configuration in an approach that consists of the following steps:

1) encode variables (families) and constraints, as well as additional specifications when needed, as automata;

2) synthesize a supervisor;

3) use the supervisor in combination with the original automata to efficiently answer the interactive configuration or reconfiguration queries.

Automata have been previously used for solving Constraint Satisfaction Problems (CSP) (Vempaty 1992), as well as product configuration problems (Amilhastre et al. 2002). However, in these approaches a CSP is represented by a monolithic automaton resulting from applying product and minimization algorithms (Hopcroft and Ullman 1979; Kimura and Clarke 1990), which might have size exponential in the size of the original CSP. Our approach does not require to monolithically compose all automata. Instead, our approach relies on supervisory synthesis algorithms to do the necessary computations. Synthesis algorithms, in turn, can either do a brute-force monolithic synchronization of all automata, or use more efficient strategies, including compositional synthesis that avoids synchronizing all automata (Mohajerani et al. 2011), or symbolic synthesis that uses BDDs to improve efficiency (Hoffmann and Wong-Toi 1992; Vahidi et al. 2006). Moreover, SCT allows representing a supervisor not only as a monolithic automaton, but also as a set of automata (Mohajerani et al. 2011), or as logic expressions (Miremadi et al. 2011), which might potentially require less memory than other representations.

5.1 Encoding interactive product configuration using supervisory control theory

Different capabilities of interactive configuration require different levels of sophistication of encodings. We will start with the simpler forward-only interactive configuration and will add undo-actions and reconfiguration afterwards. All encodings create an automaton for each variable and each constraint, these are treated as plants. Undo-actions and reconfiguration require an extra automaton, which is treated as a specification. Specification for the forward-only interactive configuration does not have separate automata, and is expressed as marked states only.

The overall algorithm is illustrated in Algorithm 5.1. The algorithm converts all constraints to Conjunctive Normal Form (CNF) to simplify the encoding; such conversion is described in Section 3.1.3. The algorithm encodes all variables and constraints as automata; the encodings are different between forward-only configuration and configuration with undo-actions. For configuration with undo-actions and reconfiguration, the algorithm encodes extra specifications to ensure backtrack-freeness and correct reconfiguration. Plants and specifications automata are designated from previously created automata. Then, a non-blocking and controllable supervisor is synthesized; this synthesis procedure is denoted as NBC. The synthesized supervisor in conjunction with the original automata can be used for answering appropriate product configuration queries. The following sections describe the encodings in details.

Algorithm 5.1 Supervisor-for-Configuration-using-SCT

```
input: A CSP $\mathcal{P} = \langle X, D, C \rangle$ with finite-domain variables
  and propositional constraints
output: A supervisor for forward-only configuration,
  configuration with undo-actions, or reconfiguration
$C'$ = Convert-constraints-to-CNF($C$)
for $x \in X$:
  Encode-Variable-as-Automaton($x$)
for $c \in C'$:
  Encode-Clause-as-Automaton($c$)
Encode extra specifications when necessary
Define plants and specifications from created automata
Sup ← NBC(Plants, Specifications)
return Sup
```

5.1.1 Encoding forward-only interactive configuration

An automata encoding of a CNF formula F (which can be generalized to finite-domain variables as well) is as following. For each variable $x_i \in \mathit{scope}(F)$ introduce an automaton A_{x_i} with two states: an "unassigned" (initial) state $s^u_{x_i}$ and an "assigned" state $s^a_{x_i}$. Let the only marked state be $s^a_{x_i}$, since the product is not fully configured until every variable have a value assigned. Two transitions will lead from the unassigned state to the assigned state: one transition labeled x^T_i and the other transition labeled x^F_i, corresponding to assignment of the Boolean value True and False to the variable, respectively. The alphabet of the automaton is $\{x^T_i, x^F_i\}$. Formally, the automaton for the variable x_i is as follows:

$$A_{x_i} = \left\langle Q_{x_i}, \Sigma_{x_i}, f_{x_i}, q^0_{x_i}, Q^m_{x_i} \right\rangle,$$

where

$$\begin{aligned}
Q_{x_i} &= \{s^u_{x_i}, s^a_{x_i}\} \text{ is the set of states,}\\
\Sigma_{x_i} &= \{x^T_i, x^F_i\} \text{ is the alphabet,}\\
f_{x_i} &= s^u_{x_i} \xrightarrow{\Sigma_{x_i}} s^a_{x_i} \text{ is the transition function,}\\
q^0_{x_i} &= s^u_{x_i} \text{ is the initial state, and}\\
Q^m_{x_i} &= \{s^a_{x_i}\} \text{ is the set of marked states.}
\end{aligned}$$

For each clause $c_j \in F$, introduce an automaton, again with two states: the initial state where the clause is unsatisfied $s^u_{c_j}$, and another state $s^s_{c_j}$ where the clause is satisfied. The satisfied state will be the only marked state. For each literal in the clause, introduce a transition from the unsatisfied state to the satisfied one, labeled by the appropriate assignment of values (x^T_k for positive literal and x^F_k for negative literal). To allow multiple literals to be satisfied within the same clause, the satisfied state $s^s_{c_j}$ will have self-loops transitions for all of the literals. The alphabet of the automaton for the clause c_j will be $\{x^T_k \mid x_k \in c_j\} \cup \{x^F_k \mid (\neg x_k) \in c_j\}$. Formally,

$$A_{c_j} = \left\langle Q_{c_j}, \Sigma_{c_j}, f_{c_j}, q^0_{c_j}, Q^m_{c_j} \right\rangle,$$

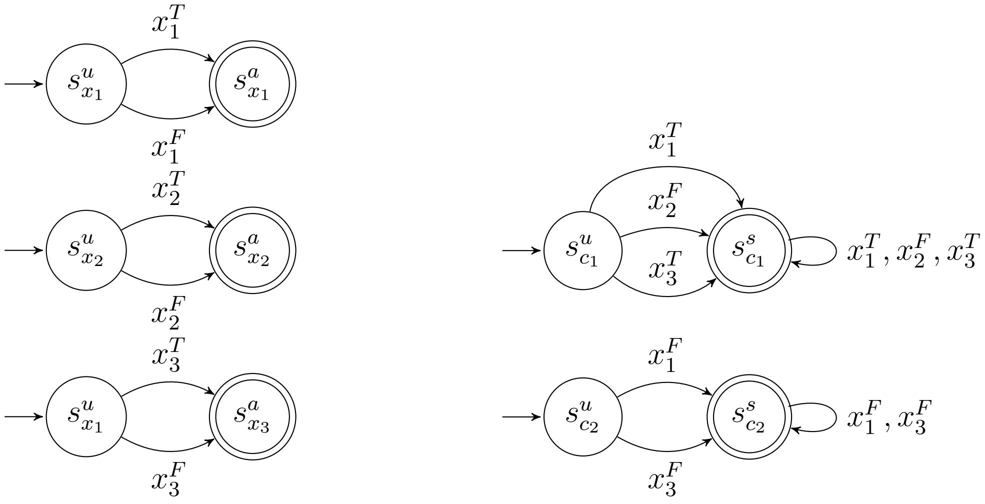
where

$$\begin{aligned}
Q_{c_j} &= \{s^u_{c_j}, s^s_{c_j}\} \text{ is the set of states,}\\
\Sigma_{c_j} &= \{x^T_k \mid x_k \in c_j\} \cup \{x^F_k \mid (\neg x_k) \in c_j\} \text{ is the alphabet,}\\
f_{c_j} &= \{s^u_{c_j} \xrightarrow{\Sigma_{c_j}} s^a_{c_j}\} \cup \{s^s_{c_j} \xrightarrow{\Sigma_{c_j}} s^s_{c_j}\} \text{ is the transition function,}\\
q^0_{c_j} &= s^u_{c_j} \text{ is the initial state, and}\\
Q^m_{c_j} &= \{s^s_{c_j}\} \text{ is the set of marked states.}
\end{aligned}$$

The complete model is a synchronous composition of automata for variables and clauses. However, a supervisor can be synthesized without explicitly constructing the automaton for synchronous composition. Automata for variables and clauses can be both considered as plants, while specification is expressed as marked states. However, since there are no uncontrollable events in this model, the distinction between plant automata and specification automata is not important for this model. A non-blocking supervisor for the complete model will ensure that taking any enabled events will lead to the marked state, which corresponds to the situation when all variables are assigned and all clauses are satisfied.

As an example, consider CNF $F = (x_1 \vee -x_2 \vee x_3) \wedge (-x_1 \vee -x_3)$. The variables x_1, x_2 and x_3 can be encoded into automata as shown in Figure 5.1a, and the two clauses can be encoded as shown in Figure 5.1b. The synthesized supervisor for the model is shown in Figure 5.2, where supervisor is shown with solid lines, while solid plus dashed lines represent the synchronous composition of variables and clauses automata (before synthesis).

The supervisor resulting from the synthesis has a lot of symmetry, since the order in which the variables are assigned is not fixed, resulting in the number of paths leading to the marked states being exponential in the number of variables. Restricting the order of variables will reduce the size of the supervisor, but will also reduce the flexibility of user choices. An automaton for restricting the order in which the variables are assigned to x_1, x_2, x_3 is shown in Figure 5.3. The supervisor for this order is shown in Figure 5.4.



(a) Automata for variables x_1, x_2 and x_3. The alphabets, top to bottom: $\{x_1^T, x_1^F\}$, $\{x_2^T, x_2^F\}$, $\{x_3^T, x_3^F\}$.

(b) Automata for constraints. Alphabets are: $\{x_1^T, x_2^F, x_3^T\}$, $\{x_1^F, x_3^F\}$.

Figure 5.1: Encoding CNF $F = (x_1 \lor \neg x_2 \lor x_3) \land (\neg x_1 \lor \neg x_3)$ as automata.

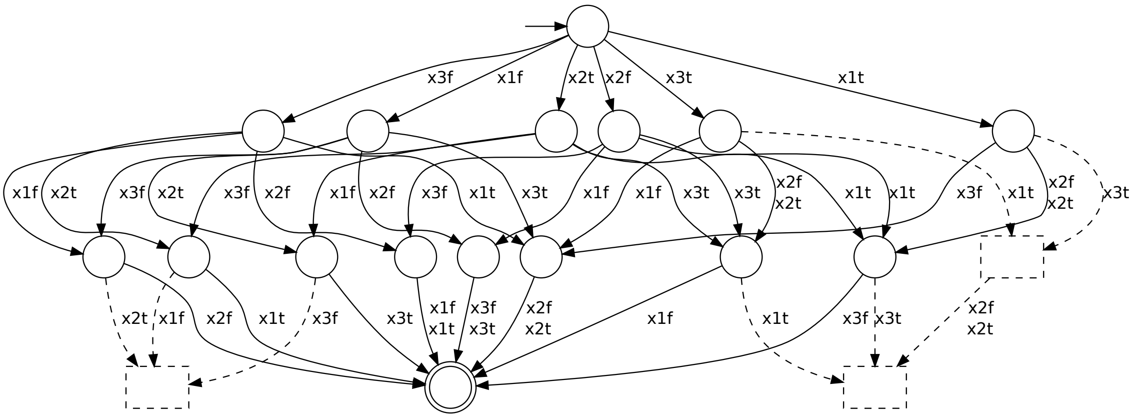


Figure 5.2: The automaton illustrating the supervisor (solid lines) and the states and transitions reachable by the unsupervised plant, but disabled by the supervisor (dashed lines).

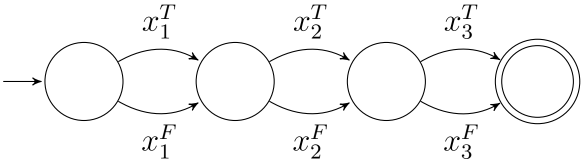


Figure 5.3: A specification to restrict the order of assigning the values to the variables to x_1, x_2, x_3.

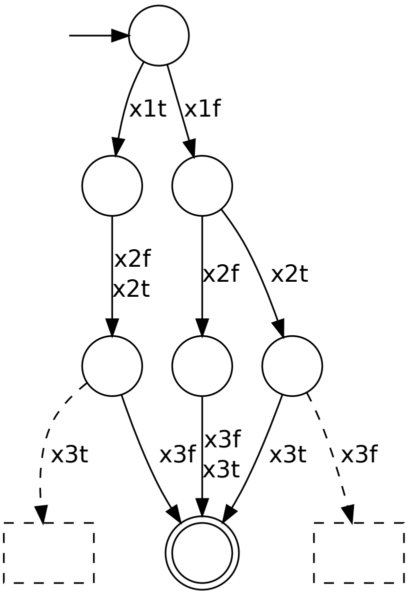


Figure 5.4: The automaton illustrating the supervisor (solid lines) assuming a fixed order of assignment (x_1, x_2, x_3) of the variables. Dashed nodes and transitions are reachable by the unsupervised system with the fixed order of variables, but are disabled by the supervisor.

5.1.2 Encoding interactive configuration with undo-actions

To illustrate undo-actions and reconfiguration, as well as to introduce by example an encoding for finite-domain variables, we will use a hypothetical car configuration example (similar to the example in Table 2.1, but slightly modified). The variables and their domains are shown in Table 5.1, and constraints are shown in Table 5.2.

To support undo-actions, variables are encoded by automata with $n + 1$ states, where n is the domain size of the variable, see Figure 5.5 for the encoding of the variable *Body*. One state, initial, is not marked and corresponds to the variable being unassigned. The other n states correspond to the values the variable can be assigned to (we will call these states *assigned* states). These assigned states are marked. The set of "assign" events is the same as in forward-only case, one event for one value of the variable. Each such event leads from the initial state to the corresponding assigned state. Each assign-event has a corresponding *undo*-event that leads back from the assigned state to the initial (unassigned) state. Due to the multi-valued nature of the variables, the negation of a variable is no longer encoded directly, and has to be represented in the constraints as a disjunction of all other values of the domain of the variable. For example, $\neg(\mathit{Body}{=}\mathit{Mini})$ have to be encoded as $(\mathit{Body}{=}\mathit{Sedan} \lor \mathit{Body}{=}\mathit{Suv})$.

Encoding of constraints requires three additions compared to the Boolean forward-only case. First, all negative literals have to be converted to disjunctions of positive literals. Second, due to undo-actions, encoding of a clause requires a separate state for each possible number of satisfied literal in the clause. However, since all literals are positive, and no two literals representing values of the same variable can be satisfied simultaneously, the number of states is limited by the number of variables, and not the number of literals. The number of states in an automaton for a clause with the scope of k variables will be $k + 1$. Assign-events for each literal lead from a state to the state corresponding to one more satisfied literal, for example, from 0 satisfied literals (unsatisfied clause) to 1 satisfied literal, from 1 to 2, etc. Thirdly, undo-events lead from a state to the previous one (for example, from 2 to 1, etc). Complete encoding of the constraint $\neg(\mathit{Body}{=}\mathit{Mini} \land \mathit{Engine}{=}\mathit{Gasoline})$, which can be rewritten as $(\mathit{Body}{=}\mathit{Sedan} \lor \mathit{Body}{=}\mathit{Suv} \lor \mathit{Engine}{=}\mathit{Diesel} \lor \mathit{Engine}{=}\mathit{Electric})$, is shown in Figure 5.6.

The specification needed to ensure the correct behavior for user undo actions is shown in Figure 5.7. This specification introduces two events *user_assign, user_unassign* that correspond to the user choices. The user can choose one of the two options:

- continue with the configuration by selecting event *user_assign*;

Table 5.1: Variables and their domains for the car configuration example.

Variable	Values
body	mini, sedan, suv
engine	gasoline, diesel, electric
transmission	manual, automatic, evt

Table 5.2: Constraints for the car configuration example.

$\neg((body = mini) \wedge (engine = gasoline))$
$\neg((body = mini) \wedge (engine = diesel))$
$\neg((body = sedan) \wedge (engine = electric))$
$\neg((body = suv) \wedge (engine = gasoline))$
$(engine = electric) \rightarrow (transmission = evt)$
$(transmission = evt) \rightarrow (engine = electric)$

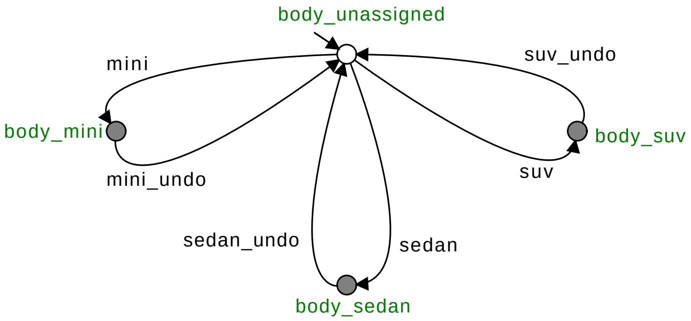


Figure 5.5: Automaton encoding variable *Body* with values *Mini*, *Sedan* and *Suv*.

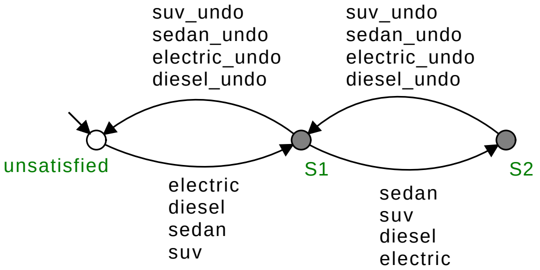


Figure 5.6: Automaton encoding constraint $\neg(\,Body{=}Mini \wedge Engine{=}Gasoline\,)$.

- undo some previous assignment by selecting event *user_unassign*.

Event *user_assign* is uncontrollable, making sure that the supervisor will always avoid dead ends and will be prepared to move "forward" with configuration, without relying on the user undo actions (backtracking) to get out of dead ends. Event *user_unassign* is controllable, since it must be disabled when no assignments have been made; making *user_unassign* uncontrollable would result in the specification being uncontrollable with respect to the plant, leading to a null supervisor. Consider automaton in Figure 5.7. Firing *user_unassign* leads to the state from where only undo-events are possible. However, if there are no events to undo, as is the case in the beginning of the configuration process, or after all assignments were already undone, the system will end up in a deadlock. To remove this deadlock, the supervisor have to disable the event *user_unassign*, thus this event have to be controllable.

The supervisor contains 101 states and 197 transitions, and it is illustrated in Figure 5.8. To give an intuition of interactive configuration session without relying on a drawing a supervisor, consider the following paths from the initial state to a marked state, where each row indicates the enabled events, and "∗" indicates the event taken:

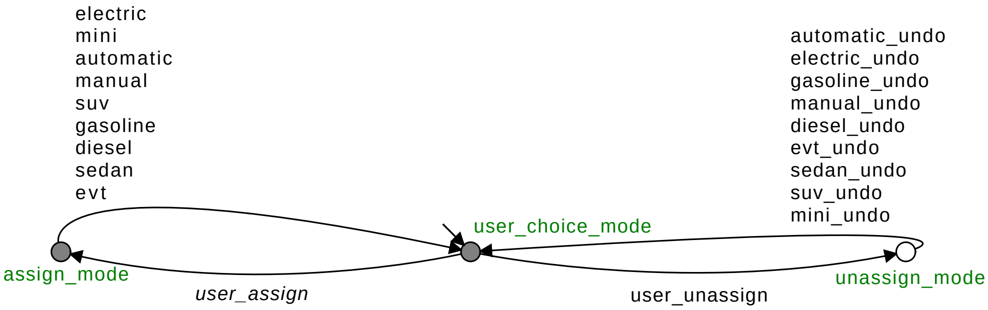


Figure 5.7: Automaton encoding backtrack-freeness for undo-actions.

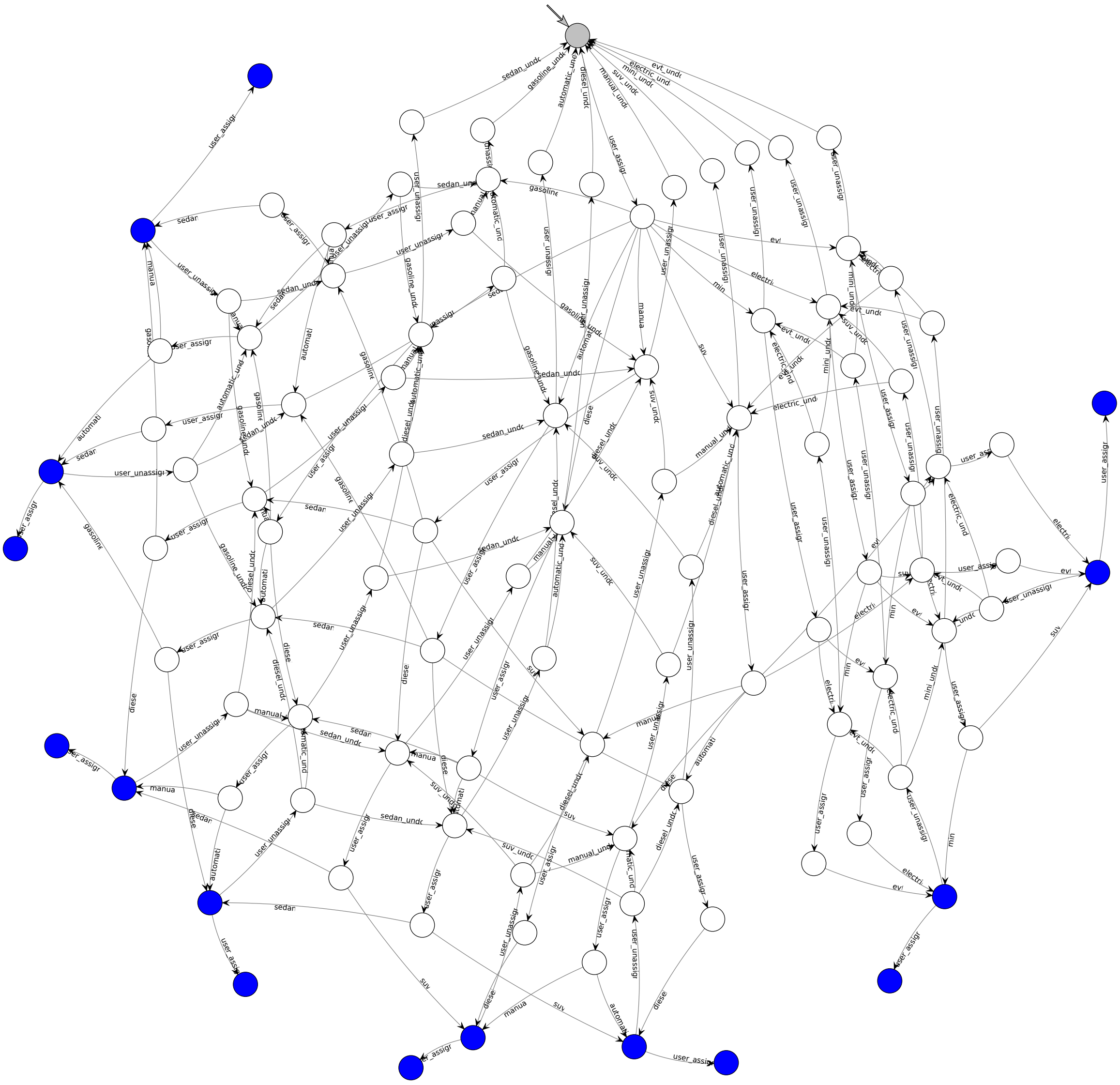


Figure 5.8: Illustration of the supervisor for interactive configuration with undo-actions for the car configuration example.

```
*user_assign
*mini, sedan, suv, gasoline, diesel, electric, manual, automatic, evt
*user_assign, user_unassign
electric, *evt
*user_assign, user_unassign
*electric
(done)

*user_assign
*mini, sedan, suv, gasoline, diesel, electric, manual, automatic, evt
*user_assign, user_unassign
electric, *evt
user_assign, *user_unassign       % example of undo-actions
*mini_undo, evt_undo
*user_assign, user_unassign
mini, suv, *electric
*user_assign, user_unassign
mini, *suv
(done)
```

The paths illustrate the choices offered to and made by the user. The intuition behind the supervisor is as following: after the user chooses *user_assign*, the supervisor disables all assignments that can not result in a valid complete configuration. The user is only offered the choices that will lead to a valid complete configuration (marked state) without the need for any undo-actions.

5.1.3 Encoding interactive configuration with undo-actions and reconfiguration

The reconfiguration procedure will be built on top of the solution for undo-actions. The specification needed to ensure the correct behavior for user undo actions and reconfiguration introduces three extra event, *user_force*, *user_force_start_undo* and *user_force_done* to the previously introduced events *user_assign* and *user_unassign*. This specification is shown in Figure 5.9. The *user_force* event can be either controllable or uncontrollable, the synthesis procedure results in the same supervisor. We chose to make it uncontrollable, to emphasize that the system should always be prepared for the user executing this action. Event *user_force_start_undo* is also uncontrollable. Event *user_force_done* is controllable, to ensure that the user has undone enough assignments to make partial configuration valid. With such specification, there are three options to choose from, when selected variants correspond to a valid partial configuration:

- continue with the configuration by selecting event *user_assign*;
- undo some previous assignment by selecting event *user_unassign*;
- enter a reconfiguration mode by selecting event *user_force*.

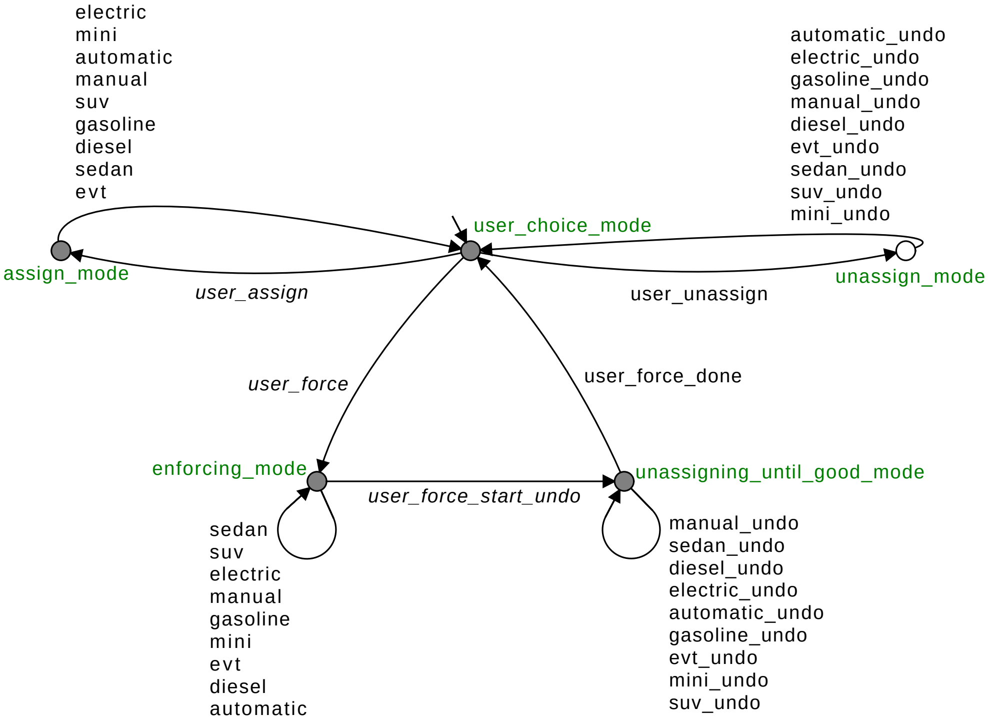


Figure 5.9: Automaton encoding user undo action and reconfiguration.

Naturally, these choices can be hidden from the user interface, presenting the user only with the variants (click once to assign a variant, click the variant second time to undo the assignment), firing the necessary events in the background.

The supervisor for undo actions and reconfiguration is illustrated in Figure 5.10. Unfortunately, with 229 states and 617 transitions, it is too big to be visualized properly on the standard printed page. The following path from the initial state to a marked state might give some intuition of the supervisor:

```
*user_assign, user_force
*mini, sedan, suv, gasoline, diesel, electric, manual, automatic, evt
*user_assign, user_unassign, user_force
electric, *evt
user_assign, *user_unassign, user_force    % example of undo-actions
*mini_undo, evt_undo
mini, *suv, electric
user_assign, user_unassign, *user_force    % example of reconfiguration
gasoline, *diesel, electric, user_force_start_undo
gasoline, electric, *user_force_start_undo
diesel_undo, *evt_undo, suv_undo
diesel_undo, suv_undo, *user_force_done
*user_assign, user_unassign, user_force
*automatic, manual
(done)
```

However, in this example even when the user chooses to force *Engine=Diesel*, there is an immediate offer to undo this choice. To make sure that the system offers to undo

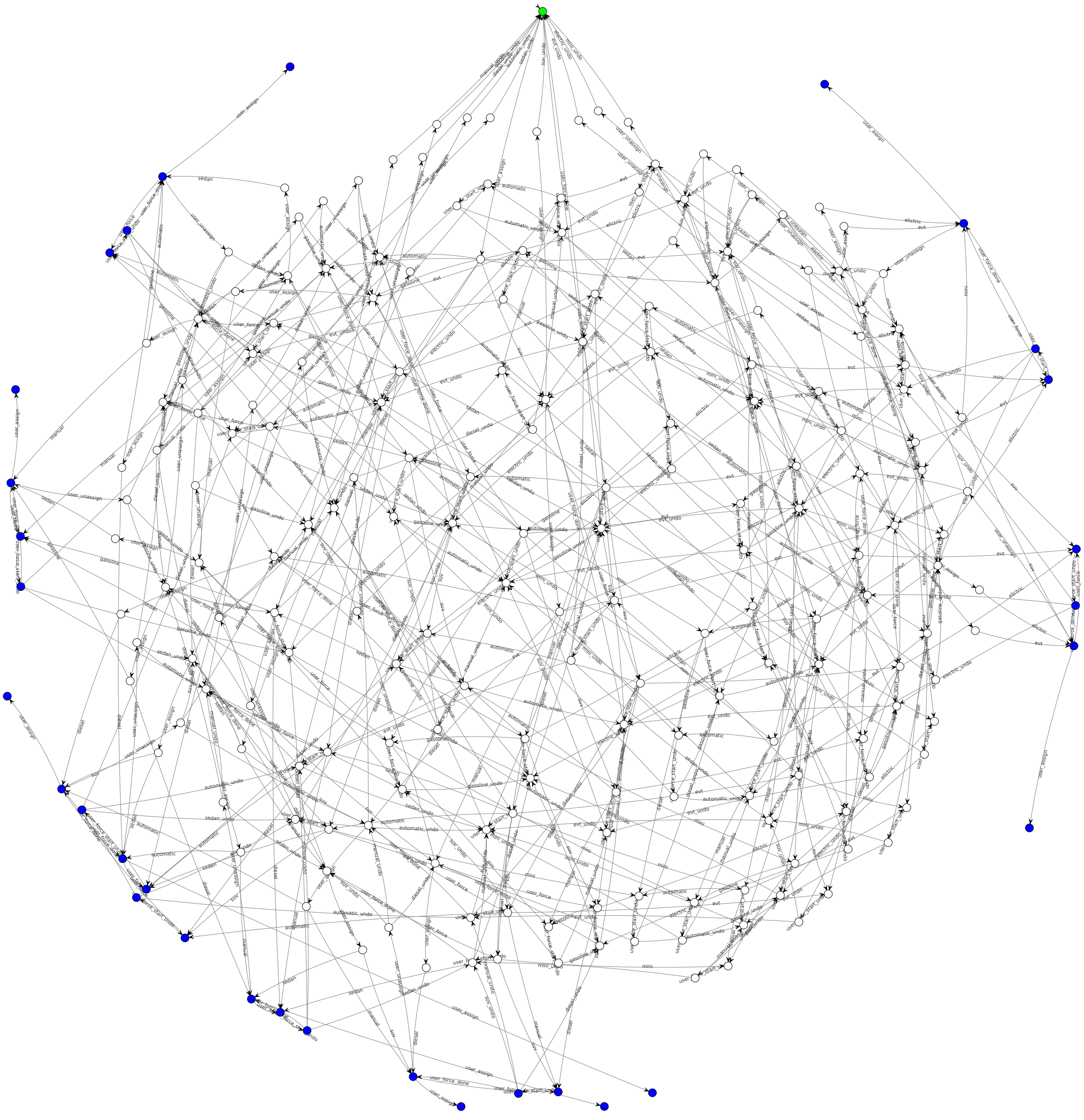


Figure 5.10: Illustration of the supervisor with undo-actions and reconfiguration for car configuration example.

only the choices that were not forced, the automata for the variables can be modified as shown in Figure 5.11. After event *user_force*, the automaton allows assigning values to the variable, but does not allow to unassign them until reconfiguration is over, that is, until the event *user_force_done* is fired. The supervisor for such automata contains 682 states and 1359 transitions.

This solution allows the user to undo actions and helps the user reconfiguring invalid configurations.

5.2 Representing the supervisor

The supervisor in Figure 5.4 had to disable only two transitions that led to blocking states. Instead of representing the supervisor as an automaton with unwanted transitions disabled, it is possible to augment existing automata with conditions that will specify when the transition is allowed. Such conditions are called *guards*. The supervisor represented by such guards can potentially be smaller than, for example, the BDD for representing the data necessary for the configuration process. The algorithm for computing such guards was introduced in (Miremadi et al. 2011). The generated guards might be compared to extra constraints added by, for example, Adaptive-Consistency algorithm (Dechter and Pearl 1987) for ensuring backtrack-freeness of the CSP search.

The supervisor in Figure 5.4 can be represented by two symbolic guards shown in Table 5.3, one guard for event x_3^T, which would allow x_3^T to be fired only when the automaton for clause c_2 is in the state $s^s_{c_2}$, that is, clause c_2 is already satisfied, and one guard for event x_3^F, allowing it to be fired only when in the state $s^s_{c_1}$, that is, when

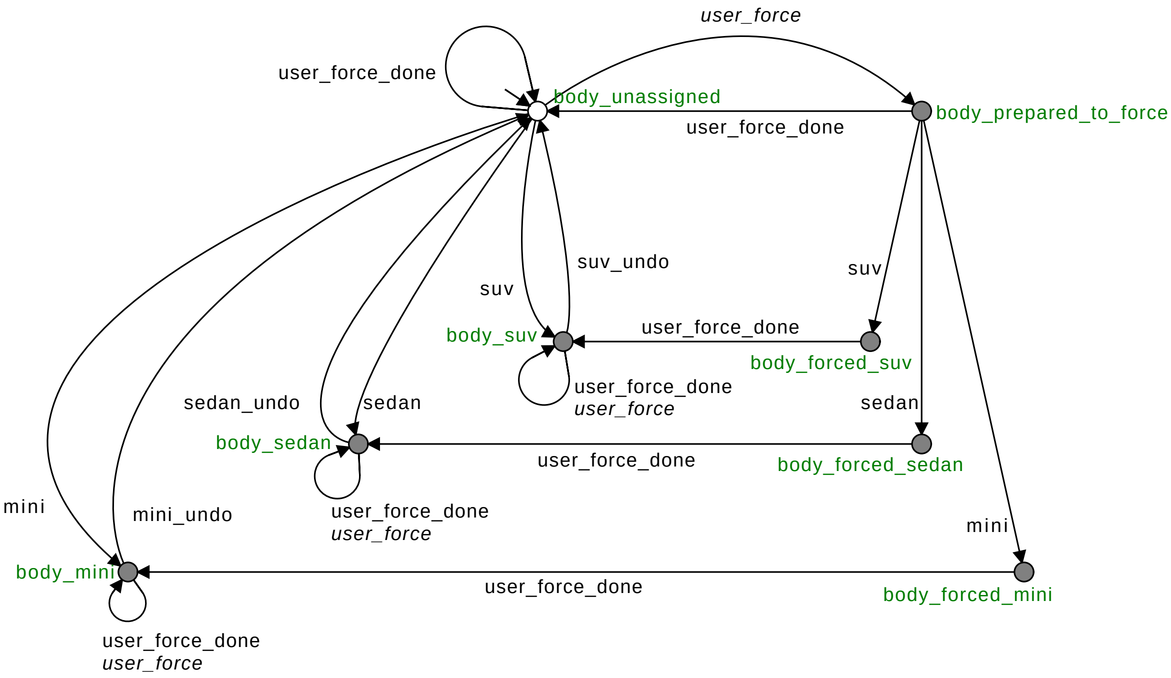


Figure 5.11: Automaton for variable *Body* that ensures that the enforced value is not offered for immediate undo (compare to Figure 5.5).

clause c_1 is already satisfied. The intuition behind the first guard is that, because x_3 is the last variable to be assigned, if by the time of choosing a value for x_3 clause c_2 is not satisfied yet, the only way to satisfy it is to choose x_3^F, thus to choose x_3^T clause c_2 should be satisfied by the other variables.

Similarly, the guards can be computed for the supervisor shown in Figure 5.2; these guards are shown in Table 5.4. Note that the guards represent only what and when the supervisor disables (or enables, if such representation is more compact). The supervisor does not have to keep the information about the complete state-space of the synchronous composition of the original automata.

Another promising approach to compact supervisor representation is to use compositional synthesis algorithms (Mohajerani et al. 2011). These algorithms apply abstraction techniques to the automata, as well as use multiple automata to represent the synthesized supervisor; the resulting supervisor can thus be called an *abstracted modular supervisor*. Preliminary experiments with compositional algorithms indicate that it might be possible to create a supervisor for product configuration instances that are larger than the ones that can be handled by other SCT methods. Comparison with BDDs and other knowledge compilation methods is a topic of future work.

5.3 Conclusions

Modeling interactive product configuration problem as an SCT problem allows compilation of the configuration constraints into a supervisor compactly represented by either symbolic guards or an abstracted modular supervisor. These representations of the supervisor can potentially be more compact than the other knowledge compilation methods used for product configuration, for example BDDs, while still providing

Table 5.3: Guards for the supervisor shown in Figure 5.4.

Event	Guard
x_3^T	$s_{c_2}^s$
x_3^F	$s_{c_1}^s$

Table 5.4: Guards for the supervisor shown in Figure 5.2.

Event	Guard
x_1^T	$s_{c_1}^s \wedge s_{x_3}^a \wedge s_{c_2}^u$
x_1^F	$s_{c_1}^u \wedge s_{x_3}^a \wedge s_{x_2}^a$
x_2^T	$s_{c_1}^u \wedge s_{x_3}^a \wedge s_{x_1}^a$
x_2^F	true
x_3^T	$s_{c_1}^s \wedge s_{x_1}^a \wedge s_{c_2}^u$
x_3^F	$s_{c_1}^u \wedge s_{x_2}^a \wedge s_{x_1}^a$

polynomial-time in the size of the compiled representation answers to important product configuration queries.

A limitation of the presented reconfiguration solution is that it does not help the user to find the shortest (or optimal with respect to some other criterion) way to repair a configuration. Future work may be to introduce optimization. Optimization can be implemented by showing the user for each event the minimum number of steps necessary to reach a marked state, or simply disable by the supervisor all undo-choices that do not lie on any of the shortest paths to a marked state. Work on optimization is ongoing in the SCT community (Miremadi 2012), and the model presented here will be usable for that purpose.

Chapter 6

Summary of Appended Papers

Paper 1.

Alexey Voronov, Knut Åkesson, Anna Tidstam, Johan Malmqvist and Martin Fabian. *Toward better support for authoring and maintaining product configuration constraints.* Submitted, 2012.

Paper 1 introduces a number of methods to help engineers maintain, verify and analyse product configuration constraints, including a method for automatic detection of errors in constraints, a method for authoring constraints for mutually-exclusive items, methods for improving internal structure of constraints for their better maintainability, and a method for efficiently computing the effects of adding or removing constraints. Computational performance of the proposed methods is tested on configuration data from automotive industry, and the results show that the methods can work very efficiently on such data.

Paper 2.

Alexey Voronov, Knut Åkesson, Anna Tidstam and Johan Malmqvist. *Verification of Item Usage Rules in Product Configuration.* Proceedings of 9th International Conference on Product Lifecycle Management PLM-12, Montreal, Canada, 2012.

Paper 2 introduces problems engineers face when working with Item Usage Rules (IURs), which specify which items are included in a bill of materials for a customer order. The paper considers ensuring that exactly one item from a predefined set is included in each product, as well as the problem of rewriting an IUR without changing the configurations that the IUR covers.

Paper 3.

Alexey Voronov, Knut Åkesson and Fredrik Ekstedt. *Enumerating partial configurations.* Proceedings of Configuration Workshop at 22nd International Joint Conference on Artificial Intelligence IJCAI-11, Barcelona, Spain, 2011.

Paper 3 focuses on the problem of efficient enumeration of valid partial configurations, which is used to provide a scoped view of a product, as well as for supporting engineers in authoring IURs. The paper provides motivation, pedagogical examples, detailed algorithms and empirical evaluation of different approaches to compute valid partial configurations.

Paper 4.

Koen Claessen, Niklas Een, Mary Sheeran, Niklas Sörensson, Alexey Voronov and Knut Åkesson. *SAT-Solving in Practice, with a Tutorial Example from Supervisory Control.* Journal of Discrete Event Dynamic Systems 19(4), pp. 495–524, 2009.

Paper 4 gives an overview of SAT-solving, and introduces a SAT-solver based approach to SCT problems, providing methods for SCT verification of controllability and deadlock-freeness, as well as SAT-based iterative synthesis procedure for controllable and deadlock-free supervisor.

Chapter 7

Conclusions and Future Work

This thesis introduces a number of methods for automatic verification of product configuration constraints and for computational support of manual inspection of constraints. These methods may ease elimination of errors and speed up the development process of a product platform, which in turn can increase the competitiveness of a company.

The conclusions are grouped around the research question (RQ).

RQ-1. *What kind of computer support can be implemented to help engineers maintain, verify and analyze product configuration constraints?*

For automatic verification of product configuration constraints, Paper 1 proposes to use reference configurations and Paper 2 proposes to use sets of mutually exclusive items to verify variant constraints and Item Usage Rules (IURs) after each modification of the constraints, similar to running unit tests in software engineering, which can speed up the detection of errors. Paper 1 proposes a method that can be used for both verification and authoring of IURs; this method is based on using valid partial configurations to verify or author IURs. How to compute valid partial configurations efficiently in investigated in Paper 3. These methods for automatic verification can reduce the number of errors and speed up the process of developing correct configuration constraints.

For supporting manual inspection, this thesis introduced a method to automatically verify that an IUR can be rewritten using a given subset of product variables (families). Rewriting an IUR can be useful as a maintenance operation, and it is important that it does not introduce errors. Rewriting an IUR is just one operation from a larger class of *refactoring* operations that improve the structure of constraints, but do not change their external behavior or meaning. The thesis also proposes a number of methods for discovering refactoring opportunities. When changing constraints, it might be difficult to foresee the effects of the change. This thesis introduces a method for efficiently computing the configurations that become allowed or forbidden when constraints are added or removed; this can be used when an engineer adds or removes constraints to automatically notify all other engineers that are influenced by the change, which can greatly improve the communication between engineers in a concurrent engineering setting.

RQ-2. *How to enumerate valid partial configurations efficiently?*

Valid partial configurations for large industrial product configuration data can be efficiently enumerated using SAT-solvers, as introduced in Paper 3. sd-DNNF might also be used for rather large product configuration instances. Problem instances that could be handled by sd-DNNF are larger than those that could be handled by MDDs, but not as large as those that could be handled by SAT. Performance of the proposed SCT-based method (Chapter 5) for enumerating valid partial configurations requires further investigations.

RQ-3. *How to compactly represent product configuration data for answering product configuration questions efficiently?*

SAT-solver with incremental solving can be very efficient in handling large product configuration problems from automotive industry. However, it is difficult to predict their running time, and there are no acceptable worst-case running time guarantees. Knowledge compilation methods can be used to create data structures that would provide acceptable guarantees on the worst-case running time. Among existing knowledge compilation methods for product configuration, sd-DNNF, AND/OR MDDs and Tree-of-BDDs look the most promising, although further investigations and benchmarking are necessary (see Chapter 4). We proposed a new knowledge compilation method for interactive product configuration based on Supervisory Control Theory (Chapter 5), but its applicability for large product configuration instances and benchmarking against other methods remains a topic of future work.

To summarize, this thesis introduces a number of formal methods for handling large-scale product configuration data. These methods can reduce the errors in creating and maintaining product configuration constraints, and speed up the development of product platforms. This thesis also opens up new questions for future work outlined below.

Future Work

One of the industrial partners in the research project adopted SAT-based methods for enumerating valid partial configurations described in Paper 3. It would be interesting to conduct a follow-up study to find out how helpful the methods are for real engineers, what improvements can be made to the methods, and whether more companies might benefit from deploying similar tools.

This thesis introduced a method for verifying that an IUR can be rewritten using a given set of families. This verification can be used within the optimization procedure. Such optimization procedure can automatically find the best set of families with respect to some criteria, for example, some engineers might want to have as many families as possible in an IUR to see all relevant details, while other engineers might prefer as few families as possible, to keep only essential information. Automatic rewriting can contribute to sustainability of the workplace by allowing engineers to chose their preferred representation method.

Verification and analysis queries in this thesis were formulated and programmed by researchers based on informal descriptions provided by engineers. To shorten the time from an idea to an implementation, and to improve the methods' adoption, an investigation of user-friendly methods to create queries about configuration constraints is needed, with the aim, for example, to create a language for constraint queries similar to database query languages, to be directly usable by engineers.

This thesis treated product configuration constraints as logic only. Taking into account the sources of constraints—for example, that some constraints are geometrical, and some constraints originate from marketing—might allow richer feedback to engineers, to facilitate understanding and improve decisions (for example, an engineer can relax marketing constraint much easier than a physical constraint). Further investigation is needed on how to connect such meta-data with constraints, and how to use it to create better explanations, and which other benefits it might bring and at which cost.

The methods presented in this thesis might be used to efficiently compute visualizations of configuration data similar to the ones presented in (Tidstam 2012; Tidstam, Bligård, et al. 2012; Pleuss et al. 2011; Ziyang 2010; Hadzic and O'Sullivan 2008). However, how to do that and which visualizations can be computed efficiently is not clear. Visualization methods might be very important when dealing with decisions that can not yet be automated (Baumeister and Freiberg 2010).

This thesis compares performance of some SAT, BDD, MDD and sd-DNNF tools, while other knowledge compilation methods are not benchmarked, including Tree-of-BDDs, AND/OR MDDs, as well as the SCT-based representation proposed in this thesis. Comparing as many existing tools as possible on a wide range of representative benchmarks could allow finding the best method for working with product configuration data.

This thesis attempts to find fixed-parameter-tractable properties in industrial product configuration instances. However, not all known tractable classes are investigated, and the number of industrial instances in the study was limited. As future work, one might extend the study with other tractable classes, for example, single lookahead unit resolution (SLUR) (Franco and Van Gelder 2003; Čepek et al. 2012) and matched formulas (Franco and Van Gelder 2003; Szeider 2003), as well as with more instances from other companies. Finding suitable fixed-parameter-tractable properties for industrial instances would allow improving and specializing both search and knowledge compilation procedures, which would result in faster answers.

Explanations of unsatisfiability in this thesis are based on extracting a Minimal Unsatisfiable Subformula (see Paper 1). However, this extraction does not take into account how complicated the resulting formula is for an engineer. Exploring human-friendly presentations of unsatisfiability and human understanding of formulas, for example, as in (Strannegård et al. 2009), could allow better explanations that can speed up comprehension and save engineers' time.

To make SAT-based algorithms more efficient for SCT problems as presented in Paper 4, one might start by looking at symmetry breaking (see, for example, (Sakallah

2009) for an introduction to symmetry and satisfiability), better encodings, and new verification approaches. Symmetry can be exemplified by multiple paths leading to the same state, while to verify a system it is often enough to analyze only one path. Symmetry can be avoided, for example, by adding extra constraints (Crawford et al. 1996), or by using solvers that take symmetry into account (Sabharwal 2009). Better encodings can also speed up the solving process. SAT solvers tend to work well with encodings that allow to achieve Generalized Arc Consistency via Unit Propagation only (Walsh 2000; Bacchus 2007). Such encodings exist for both automata transitions (for example, *grammar* constraint from (Bacchus 2007)) and for cardinality constraints that specify mutual exclusiveness of automata states (Bailleux and Boufkhad 2003; Sinz 2005; Marques-Silva and Lynce 2007; Bailleux 2010; Frisch and Giannaros 2010; Ben-Haim et al. 2012). Previously, Linear Temporal Logic (LTL) properties were the focus for SAT-based tools, and it is not possible to encode the non-blocking property using LTL. Recently, an approach to use SAT-solvers to check Computation Tree Logic (CTL) properties was proposed (Hassan et al. 2012), and CTL can be used to express non-blocking (Kumar and Jiang 2002). Using this approach for verifying CTL properties can allow verifying the non-blocking property and synthesizing non-blocking supervisors using SAT-solvers.

To summarize, there is a number of directions that can be pursued starting from this thesis to help engineers working with product configuration constraints.

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