THESIS FOR THE DEGREE OF DOCTOR OF PHILOSOPHY

Single Phase Active Power Factor Correction Converters

Methods for Optimizing EMI, Performance and Costs

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Abstract

In this thesis, front-end solutions with single-phase power factor correction (PFC) capability are studied. The reduction of current harmonics using various PFC techniques is investigated and related to the EN 61000-3-2 standard. Moreover, power electronics issues concerning diode recovery characteristics, boost inductor design and MOSFET switching speed considerations for optimizing the overall EMI and efficiency performance of continuous mode active PFC Converters are studied. In addition, the design and construction of a 1200 W continuous conduction mode (CCM) PFC circuit prototype, used for making various measurements, is presented and discussed.

With the main objective of this dissertation being optimizing performance and cost indices of continuous mode PFC converters, the results of this research work are presented in three main parts.

Firstly issues related to generation of harmonic currents by AC-DC single-phase rectifier-capacitor filter circuits when connected to the utility network, the legal obligations set forth by the European standard EN 61000-3-2 for limiting generation of low-frequency harmonics and different PFC techniques and strategies useful for meeting this standard, are studied. A novel approach of having a central PFC circuit for domestic and commercial loads leading to lower current harmonic distortion without the need to install (expensive) active rectifiers in each end-user device is proposed.

Secondly, based on various measurement results, some new methods to optimize overall EMI and efficiency performance of continuous mode active PFC circuits are presented. These methods resulted in performance improvements by way of higher efficiency, cost reduction and reduction in radiated and conducted EMI by over 10 to 23 dB μV.

Lastly, all papers published in various journals and conferences from the above work, are presented.

Keywords: Active and Passive Power Factor Correction (PFC), Harmonic Currents, Diode Recovery Time, Snap Factor, EMI, Quasi Peak, Antenna Factor.

List of Publications

This thesis is based on the work contained in the following publications:

Paper A
Supratim Basu, Math H.J.Bollen and Tore M.Undeland, *PFC Strategies in light of EN 61000-3-2,* **EPE PEMC 2004 Conference**, Riga, Latvia, 1-3 September 2004.

Paper B
Supratim Basu and Math.H.J.Bollen, *A Novel Common Power Factor Correction Scheme for Homes and Offices,* **IEEE Transactions on Power Delivery**, Vol.20, No.3, July 2005.

Paper C
Supratim Basu and Tore M.Undeland, *Design Considerations for Optimizing Performance & Cost of Continuous Mode Boost PFC Converters,* **IEEE Nordic Workshop on Power and Industrial Electronics (NORPIE 2004),** Trondheim, Norway, 14-16 June 2004.

Paper D
Supratim Basu and Tore M.Undeland, *Diode Recovery Characteristics Considerations for Optimizing Performance & Cost of Continuous Mode Boost PFC Converters*, **EPE Journal**, Vol. 16 . n^{o} 1 , February 2006.

Paper E
Supratim Basu and Tore M.Undeland, *Inductor Design Considerations for Optimizing Performance & Cost of Continuous Mode Boost PFC Converters,* 20th Annual **IEEE Conference, APEC 2005** at Texas, USA, 6-10 March 2005.

Paper F
Supratim Basu and Tore M.Undeland, *Diode Recovery Characteristics Considerations for Optimizing EMI Performance of Continuous Mode Boost PFC Converters,* **11th European Conference on Power Electronics and Applications, EPE 2005,** at Dresden, Germany, 11-14 September 2005.

Paper G
Supratim Basu and Tore M.Undeland, *A Novel Design Scheme for Optimizing EMI and Efficiency of Continuous Mode PFC Converters,* **17th IEEE International Symposium on Electromagnetic Compatibility,** Singapore, February 27-March 3, 2006.

Paper H
Supratim Basu and Tore M.Undeland, *A Novel EMI Reduction Design Scheme for Continuous Mode PFC Converters,* Accepted for Publication**-IEEE Nordic Workshop on Power and Industrial Electronics (NORPIE 2006),** Lund, Sweden, 12-14 June 2006.

Paper I
Supratim Basu and Tore M.Undeland, *A Novel Design Scheme for Optimizing Efficiency and EMI of Continuous Mode PFC Converters,* Submitted to **- IEEE Transactions on Electromagnetic Compatibility**, February 2006.

Preface

The effect of poor power factor and harmonics generated by rectifier-capacitor filter circuits, encountered commonly in the input circuit of most off-line converters of electronic equipment, has been a matter of concern for long. At higher power levels (200 W to 500 W and higher) these problems become even more severe and thus harmonics must be filtered. This has led to the development of the IEC 61000-3-2 standard and its adoption by the European Community.

To mitigate the problems described above, power factor correction (PFC) circuits are being increasingly used. These PFC circuits could be of active or passive types. The passive PFC circuit comprises of a distortion-limiting network that helps in meeting the standard without suppressing the harmonics completely or improving the converter's power factor to unity. The active PFC circuit is a high frequency converter that provides near unity load power factor, with the load generating negligible harmonics, and this is also consistent with the goals of switch mode conversion (small size and lightweight). With power supply applications demanding significantly increased power densities of above 18 W / cubic inch, an increase in switching frequency, reduction in switching losses and EMI are a necessity.

The work presented here proposes new application areas for PFC circuits with reference to the IEC 61000-3-2 standard. Associated power electronics issues are also explored and design considerations that help improve overall performance of active PFC circuits are proposed. No work was done on various control schemes of these converters.

The work involved in this thesis has been carried out at the Department of Electric Power Engineering of Chalmers University of Technology Sweden, the Department of Electric Power Engineering of Norwegian University of Science and Technology (NTNU) Norway, and Bose Research (P) Ltd. India.

Acknowledgement

I would like to express my sincere appreciation to those who made this work possible: Professors, friends and family.

Firstly, I would like to express my gratitude and admiration for my advisors Professor Tore M. Undeland and Professor Math H. J. Bollen, whose valuable scientific guidance and encouraging attitude have motivated much of the research described in this dissertation. I consider myself fortunate to have worked under their guidance. I thank them for their support, belief, patience, fairness and constructive feedback. They taught me something beyond just techniques for solving problems. They taught me attitude, initiative, and passion for what I believe in. I have to thank them for the many opportunities they have given me over the years.

I also take this opportunity to thank my colleagues for the pleasant times at the department, and Associate Professor Torbjörn Thiringer for all his constructive views and discussions.

I would like to thank Professor Kankar Bhattacharya who initiated this research project and has supported my work during the years.

I would also like to thank my colleague Shibu K., without whom this thesis would not have been finished in the way it has.

I would like to express my greatest admiration for my parents who constantly motivated and encouraged me to keep working towards this goal. I also thank all my other family members for all the support given during difficult times. I thank my wife Debrupa for her “always available” support and help.

List of Acronyms

AC: Alternating Current

CCM: Continuous Conduction Mode

CENELEC: European Committee for Electrotechnical Standardization

CISPR: International Committee for Radio Interference

CM: Common Mode

CRM: Critical Conduction Mode

DCM: Discontinuous Conduction Mode

DC: Direct Current

DM: Differential Mode

EMI: Electromagnetic Interference

IEC: International Electrotechnical Committee

LISN: Line Impedance Stabilization Network

LN: Line-to-neutral

MOSFET: Metal Oxide Semiconductor Field Effect Transistor

PFC: Power Factor Correction

PWM: Pulse Width Modulation

RMS: Root Mean Square

THD: Total Harmonic Distortion

ZVS: Zero-Voltage Switching

Contents

Chapter 1

Introduction

Most electronic equipment is supplied by 50 Hz or 60 Hz utility power, and in almost all of them power is processed through some kind of a power converter. Usually, power converters use a diode rectifier followed by a bulk capacitor to convert AC voltage to DC voltage. It is predicted that more than 60% of utility power will be processed through some form of power electronics equipment by the year 2010. Most of this equipment will have a rectifier with capacitive filter circuit front end. Unless some correction circuit is used, the input rectifier with a capacitive filter circuit will draw pulsating currents from the utility grid resulting in poor power quality and high harmonic contents that adversely affect other users. The situation has drawn the attention of regulatory bodies around the world. Governments are tightening regulations, setting new specifications for low harmonic current, and restricting the amount of harmonic current that can be generated. As a result, there is a need for a reduction in line current harmonics necessitating the need for power factor correction (PFC) and harmonic reduction circuits.

Improvements in power factor and harmonic distortion can be achieved by modifying the input stage of the diode rectifier filter capacitor circuit. Passive solutions can be used to achieve this objective for low power applications. With a filter inductor connected in series with the input circuit, the current conduction angle of the single-phase full-wave rectifier is increased leading to a higher power factor of about 0.8 and lower input current distortion. With smaller values of inductance, these achievements are degraded. However, the large size and weight of these elements, in addition to their inability to achieve unity power factor or lower current distortion significantly, make passive power factor correction more suitable at lower power levels.

Active PFC solutions are a more suitable option for achieving near unity power factor and sinusoidal input current waveform with extremely low harmonic distortion. In these active solutions, a converter with switching frequencies higher than the AC line frequency is placed between the

output of the diode bridge rectifier and the bulk capacitor. The reactive elements of this converter are small, because their size depends on the converter switching frequency rather than the AC line frequency. The function of this converter is to make the load behave as an ideal resistive load and thus eliminate the generation of line current harmonics. However, adding a high frequency switching converter in series with the input circuit naturally causes a reduction in overall efficiency of the whole converter due to the losses contributed by this active PFC circuit. Moreover, the active PFC circuit contributes to an increase in overall costs, increase in EMI, and reduction in reliability due to an increase in the number of components.

An active PFC circuit obviously forms a very important part of any AC-DC converter today. It is, therefore, of even greater importance that the cost and performance of these active PFC circuits should be optimized.

1.1 Problem Overview and Research Goals

The preceding discussion on the need for Power Factor Correction (PFC), tightening regulations restricting the amount of harmonic current that can be generated, Power Factor Correction methods, and the need to use the high frequency continuous conduction mode active PFC circuit for higher power converters demonstrates the need for further research in these areas. Specifically, the following three areas need to be addressed.

In Europe it is now required by law that any equipment that can be connected to the public mains network has to satisfy the EN 61000 3-2 requirements of limiting the input line current harmonics. As unity power factor is not required by this standard, limiting the input current harmonics is enough. However, with many amendments to this standard, it is important to understand the standard and evaluate PFC techniques that helps meet the standard and also optimize overall cost and performance.

Any active PFC converter provides input power factor correction and generates a regulated boosted high voltage DC for a world-wide AC input range between 85 V to 270 V. The initial total cost of limiting the input current harmonics and providing power factor correction can be large. Today, PFC circuits are being widely used for applications needing converters with power rating greater than 300 W. It is important, therefore, to understand and investigate the possibility of having a

common power factor correction circuit for an installation and thus save costs. The CCM PFC converter is the preferred choice for this as this topology is more suitable for medium to high power applications.

With the active CCM PFC converter being the most commonly used PFC topology for medium to high power applications, another objective is to investigate the various power electronics issues of the CCM PFC converter and thus evolve methods that can optimize cost and performance of these PFC circuits.

The aim of this research work is to investigate the need for PFC circuits including identifying new applications that help reduce harmonic currents and optimize performance and costs of high-frequency active PFC circuit topologies. The focus is to investigate methods to improve EMI, improve efficiency and optimize the size of the boost inductor in a CCM PFC circuit. Thus the overall objective of this thesis is to develop methods that reduce overall system costs and improve performance and cost of CCM PFC circuits.

1.2 Previous Work

A lot of work has been done on various PFC circuit topologies and lately, there has been an immense active interest in single stage PFC [1.1,1.2] circuits that generate an isolated DC output. The single aim of all the above work has been to reduce cost [1.3] and optimize performance of active PFC circuits. Industrial PFC digital controllers are also now available [1.4] and sometimes used. Dedicated analog single stage PFC controllers [1.5] and resonant PFC controllers [1.6,1.7] are also used in the power electronics industry.

In spite of all these developments, the CCM mode PFC circuit is still the most popular due to its excellent overall performance. Some work has been done earlier on EMI [1.8] performance, boost inductor winding methods [1.9] and boost diode recovery related losses [1.10]. This dissertation attempts to work further on these areas.

Chapter 2

Aim of the Work and Contribution

The aim of this thesis is to understand the need for power factor correction towards meeting tightening regulations that restrict the amount of harmonic currents that can be generated. Moreover, another goal is to also understand the need to use active PFC circuits, particularly high frequency CCM PFC circuits for higher power converters, and improve performance of these converters. Thus, the final objective is to develop methods that improve performance and reduce overall costs of systems with PFC circuits. To meet these objectives, various problem areas were identified and the research results published in various international journals and conferences.

2.1 Specific Problem Areas and Publications

Most modern electronic apparatus use some form of AC to DC power conversion within their architecture and it is these power converters that draw pulses of current from the AC network during each half cycle of the supply waveform. The amount of reactive power drawn by a single apparatus (a domestic television for example) may be small, but within a typical street there may be a hundred or more TV sets or other types of equipment drawing reactive power from the same supply phase, resulting in a significant amount of reactive current flow and generation of harmonics. The effect of poor power factor and harmonics generated by equipment that can be connected to the public mains network is a matter of concern today. Thus Harmonics must be filtered and this has led to the creation of the EN 61000-3-2 standard and its adoption by the European Community. The standard does not require the load power factor to be unity and requires only limiting of the input current harmonics.

Paper A discusses the causes of input current distortion in AC-DC single phase rectifier-capacitor filter circuits and provides an understanding of the mandatory low-frequency harmonic limits of the European standard EN 61000-3-2 that is applicable to these circuits. Different Power Factor Correction (PFC) techniques and strategies useful for meeting this

standard and mitigate this problem, are explored in this paper. Some simulations and measurement results are also presented.

These PFC techniques and strategies include the use of passive PFC chokes and active PFC circuits. The most commonly used PFC topology for medium to high power applications that provides input power factor correction and generates a regulated boosted high voltage DC in the face of varying input AC between 85 V to 270 V, is the CCM boost converter. Based on this CCM boost converter, **Paper B** proposes a novel central power factor correction scheme. In this paper, the disadvantages of having a passive power factor correction circuit to meet the mandatory EN 61000-3-2 standard and the advantages of having a common central power factor correction scheme over having individual active or passive power factor correction circuits, are investigated and documented. Higher reliability and the ability of this common central power factor correction scheme to provide an in-built uninterrupted power supply (UPS) with automatic universal worldwide operation for all loads connected to it, are highlighted.

Applications today demand significantly increased power densities of up to 18 W / cubic inch. Thus designers today constantly seek efficiency optimization in every part of their design. Moreover, increasing power densities require an increase in the switching frequency and reduction in size of EMI components. Thus, understanding and control of specific power electronics issues is an important prerequisite towards optimizing the cost and performance of these PFC circuits. **Paper C** and **Paper D** explore ways, including the use of SiC diodes, to increase the efficiency and switching frequency of continuous mode boost PFC circuits. The dependence of electrical and thermal performances of these PFC circuits on the characteristics of the power switching devices is studied. By making measurements on a practical 600 W and 1000 W PFC circuit prototype, these papers show how every specific application would need a unique design solution to optimize cost and performance.

In a CCM boost PFC converter, the boost inductor design is usually straight forward but the variables that decide the size of this inductor are usually difficult to quantify and often depend heavily on the designers choice. **Paper E** explores the effect of these variables on the overall performance of a PFC converter, by making extensive measurements of conducted EMI, inductor temperature rise and converter efficiency. Three inductance design values are compared and verified with measurements on a 1200 W prototype operating at about 70 kHz. Based on these measurements, a systematic design approach is suggested.

For a CCM boost PFC converter, the boost rectifier diode ratings can be computed easily while the selection of the diode recovery characteristics is usually always decided by the final cost and efficiency requirements of the design. By making extensive measurements on a 600 W and 1000 W prototype operating at about 100 kHz, **Paper F** explores the effect of diode recovery characteristics and its snap factor characteristics for three different diode types, on the overall EMI and efficiency performance of a CCM boost PFC converter.

The switching speed of a Power MOSFET being user controllable, faster switching speeds reduce switching losses and improve efficiency. However, excessive di/dt due to fast switching would cause current overshoots, ringing and boost rectifier recovery current spikes leading to generation of large EMI. It is also commonly known that the snappier the diode's recovery characteristics, the higher would be the generated EMI. Thus Silicon Carbide (SiC) diodes with zero recovery time is expected to generate the least EMI. **Paper G** and **Paper I** explores the effect of these variables on the overall performance of a 1000 W prototype PFC Converter operating at about 100 kHz. By making extensive measurements of conducted / radiated EMI and converter efficiency, for different MOSFET switching speeds and diode types, a systematic design approach is suggested by which higher switching speeds required for higher efficiency and higher frequency operation, does not significantly increase the generated EMI.

The radiated fields emanating from the boost inductor, due to the type of core used or winding direction or winding method, couple to the EMI filter and other components and induce differential mode and common mode noise. The worst case is when a gapped magnetic core is used for the inductor. Moreover, increased turns for achieving higher inductance, necessary for reducing inductor ripple current for improving efficiency, result in winding overlap in the inductor and this increases the inter winding capacitance of the inductor resulting in higher noise feed-through. **Paper H** explores the effect of these variables on the overall performance of a 100 W AC-DC Converter prototype with a PFC Converter operating at about 70 kHz and a downstream discontinuous flyback converter synchronized to the PFC converter. By making extensive measurements of conducted and radiated EMI, for various winding schemes, a systematic novel design approach is highlighted by which it was possible to reduce conducted EMI by more than 23 dBμV for a 100 W converter.

Chapter 3

Need for Power Factor Correction and Solutions

With most electronic equipment being connected to the electricity distribution network, the non-sinusoidal input line current drawn by these equipment due to input line rectification generates current harmonics that causes severe problems. These include increased magnitudes of neutral currents in three-phase systems, overheating of transformers and induction motors. This creates the need for some kind of power conditioning. Thus, the need to limit the harmonic content of line currents drawn by electronic equipment connected to the electricity distribution networks, results in the need for *Power Factor Correction - PFC*.

3.1 Definitions

Power factor is defined as the ratio of the average power to the apparent power drawn by a load from an AC source. Assuming an ideal sinusoidal input voltage source, the power factor can be expressed as the product of the distortion power factor and the displacement power factor, as given in (3.1). The distortion power factor K_d is the ratio of the fundamental root-mean-square (RMS) current $(I_{rms(1)})$ to the total RMS current (I_{rms}). The displacement power factor K_θ is the cosine of the displacement angle between the fundamental input current and the input voltage [3.1].

$$PF = K_d K_\theta \tag{3.1}$$

The distortion power factor K_d is given by the following equation.

$$K_d = I_{rms(1)} / I_{rms} \tag{3.2}$$

The displacement power factor K_θ is given by the following equation.

$$K_\theta = \cos\theta \tag{3.3}$$

The displacement power factor K_θ can be made unity with a capacitor or inductor but making the distortion power factor K_d unity is more difficult. When a converter has less than unity power factor, it means that the converter absorbs apparent power that is higher than the active power it consumes. This implies that the power source should be rated to a higher VA rating than what the load needs. In addition, the current harmonics generated by the converter deteriorates the power quality [3.2] of the source, which eventually affects other equipment.

High power factor and low harmonics do not go hand-in-hand. Though there is no a direct correlation between the two, the following equations link total harmonic distortion *(THD)* to power factor in some way.

$$THD\ (\%) = 100 \times \sqrt{\frac{1}{K_d^{\,2}} - 1} \tag{3.4}$$

The distortion power factor K_d is also given by the following equation.

$$K_d = \frac{1}{\sqrt{1 + \left(\frac{THD(\%)}{100}\right)^2}} \tag{3.5}$$

Therefore, when the fundamental component of the input current is in phase with the input voltage, $K_\theta = 1$.We then have,

$$PF = K_d\, K_\theta = K_d \tag{3.6}$$

Substituting (3.5) in (3.6), we have

$$PF = \frac{1}{\sqrt{1 + \left(\frac{THD(\%)}{100}\right)^2}} \tag{3.7}$$

Moreover, a perfectly sinusoidal current could also have a poor power factor if its phase was not in line with the voltage. From (3.7) it is apparent that a 10% THD corresponds to a Power Factor of approximately 0.995. Thus it is clear that specifying limits for each of the harmonics will help in the control of input current “pollution” better, both from the standpoint of minimizing the circulating currents and reducing the interference with other equipment. So, while the process of shaping this input current is commonly called “power factor correction,” the measure of its effectiveness towards complying with international regulations is the amount of reduction in the harmonic content of the input current.

3.2 Need for Power Factor Correction

The Off-Line Rectifier

The input stage of any AC-DC converter comprises of a full-bridge rectifier followed by a large filter capacitor. The input current of such a rectifier circuit comprises of large discontinuous peak current pulses that result in high input current harmonic distortion. The high distortion [3.3] of the input current occurs due to the fact that the diode rectifiers conduct only for a short period. This period corresponds to the time when the mains instantaneous voltage is greater than the capacitor voltage.

Since the instantaneous mains voltage is greater than the capacitor voltage only for very short periods of time, when the capacitor is fully charged, large current pulses are drawn from the line during this short period of time. The typical input current harmonic distortion for this kind of rectification is usually in the range of 55% to 65% and the power factor is about 0.6. **Fig. 3.1a** shows the schematic of a typical single-phase diode rectifier filter circuit while **Fig. 3.1b** shows the typical simulated line voltage and current waveforms. The actual current wave shape and the resulting harmonics depend on the line impedance. **Fig. 3.1c** and **Fig. 3.1d** show the simulated odd line current harmonics normalized to the fundamental for different line impedance values.

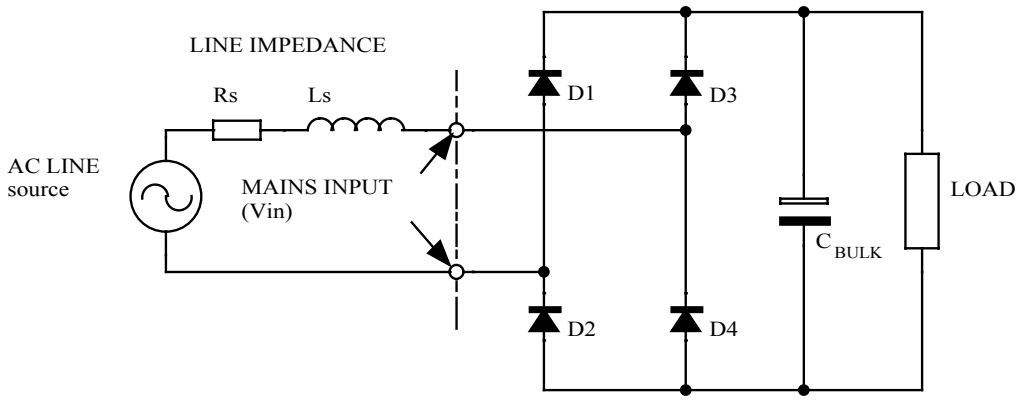

Fig. 3.1a. Typical input stage schematic of an off-line switching power supply.

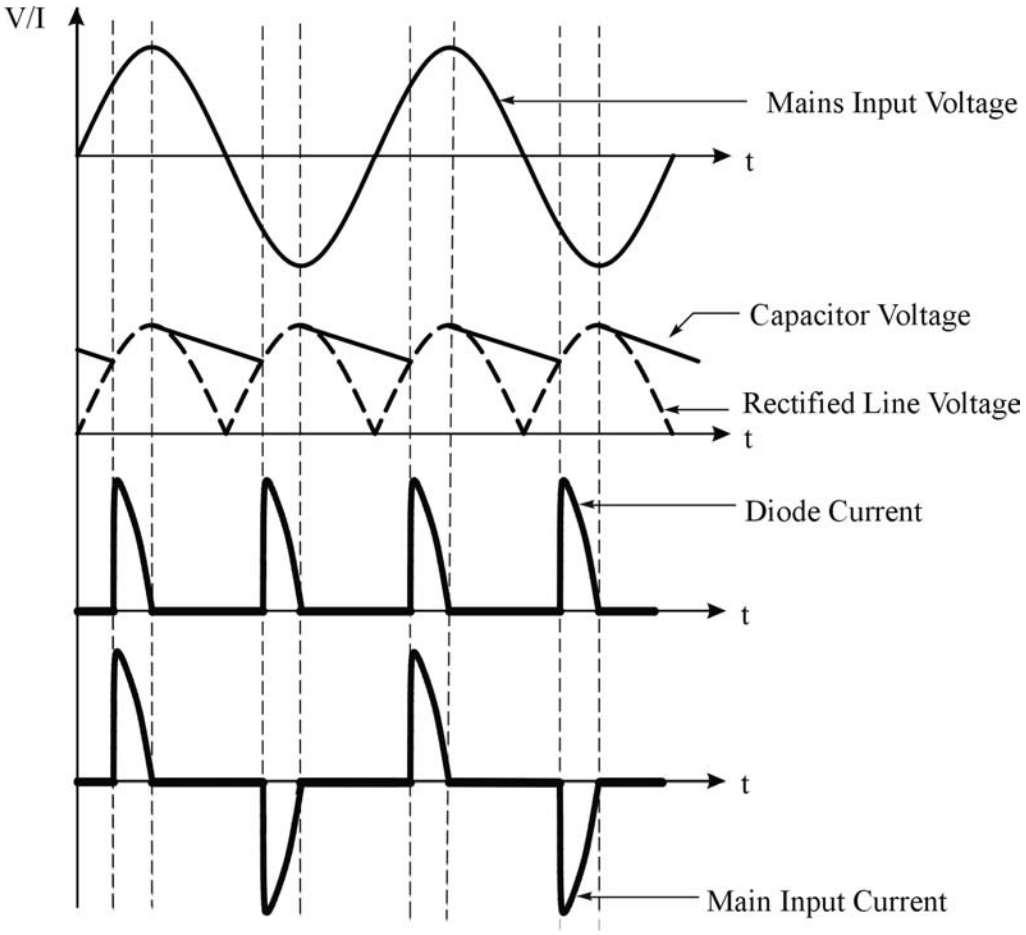

Fig. 3.1b. Typical line current and voltage waveforms.

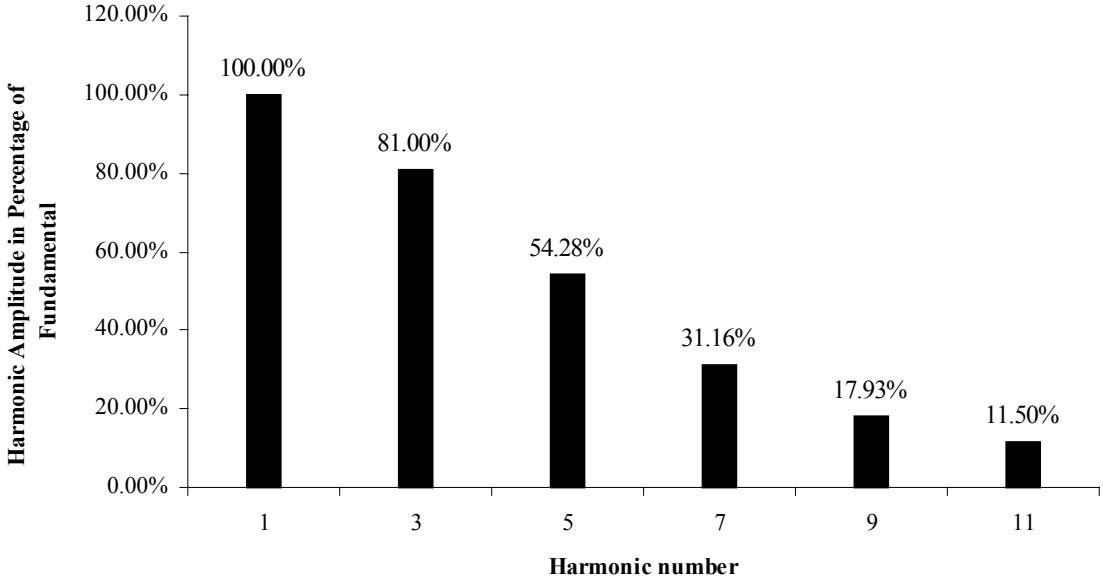

Fig. 3.1c. Odd line current harmonics normalized to the fundamental for the condition when the load is near the distribution transformer resulting in higher harmonic currents due to lower input line impedance.

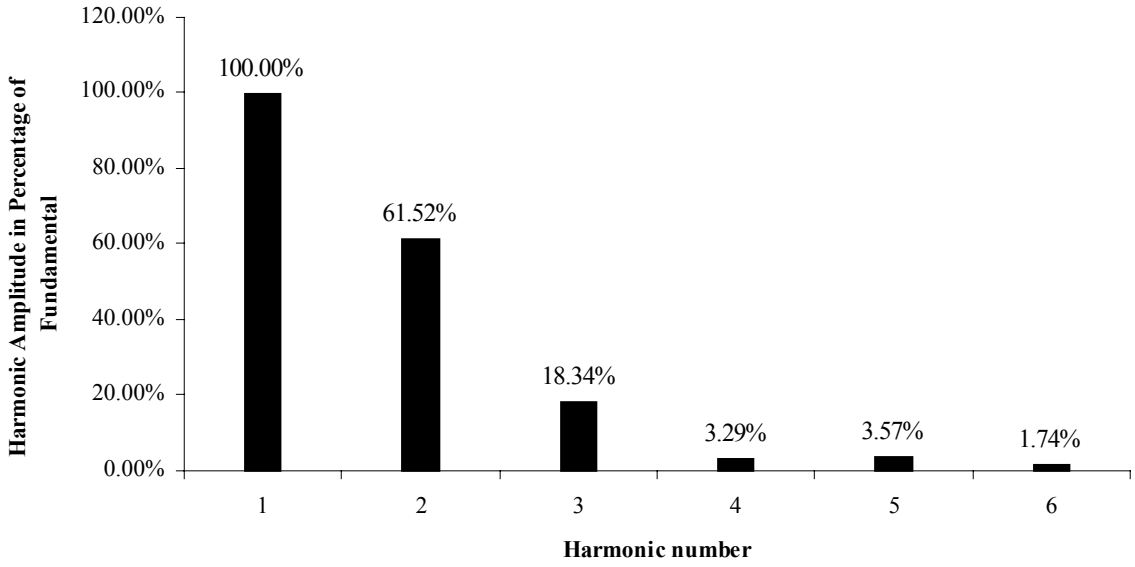

Fig. 3.1d. Odd line current harmonics normalized to the fundamental for the condition when the load is away from the distribution transformer resulting in lower harmonic currents due to higher input line impedance.

Practical measurements were made with a 1 kW constant power load comprising of a switch mode AC-DC converter. To emulate a low line impedance condition, measurements were made at a location near to the distribution transformer. The observed input voltage and current drawn by the converter is shown in the oscillogram of **Fig. 3.1e**. Channel 1 shows the input voltage while Channel 2 shows the input current. It can be seen that the input peak current is very high and is about 20 A. The corresponding input voltage peak is also distorted due to the drop in the line impedance caused by this peak current.

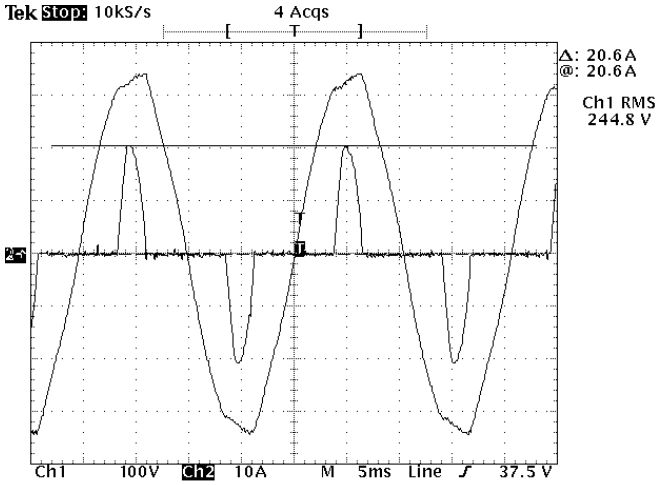

Fig. 3.1e. Voltage and current waveforms for a 1 kW constant power load for the condition when the load is near the distribution transformer resulting in higher input peak currents due to lower input line impedance.

After this, measurements were made for the same 1 kW constant power load comprising of a switch mode AC-DC converter, at a location far away from the distribution transformer. This emulated a higher line impedance condition. The observed input voltage and current drawn by the converter is shown in the oscillogram of **Fig. 3.1f**. Channel 1 shows the input voltage while Channel 2 shows the input current. It can be seen that the input peak current is now much lower, to about 13 A. It can be observed that the corresponding input voltage peak is now also much less distorted due to this reduced peak current.

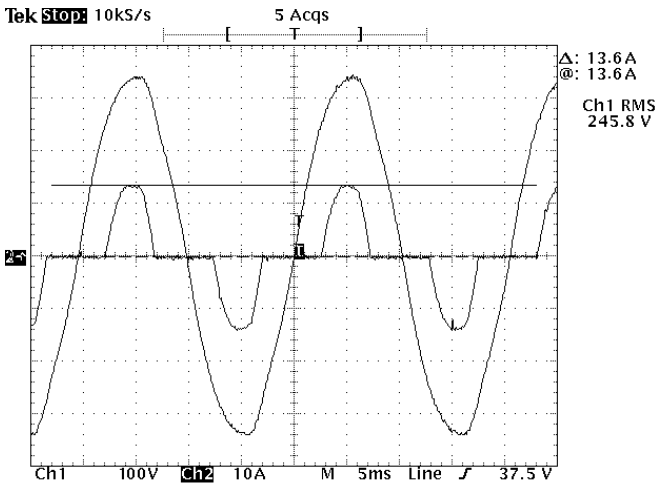

Fig. 3.1f. Voltage and current waveforms for a 1 kW constant power load for the condition when the load is away from the distribution transformer resulting in lower input peak currents due to higher input line impedance.

Conventional AC rectification is thus a very inefficient process, resulting in waveform distortion of the current drawn from the mains. This produces a large spectrum of harmonic signals that may interfere with other equipment [3.4, 3.5, 3.6]. A circuit similar to that shown in **Fig. 3.1a** is used in most mains-powered AC-DC converters. At higher power levels (200 to 500 watts and higher) severe interference with other electronic equipment may become apparent due to these harmonics sent into the power utility line. Another problem is that the power utility line cabling, the installation and the distribution transformer, must all be designed to withstand these peak current values resulting in higher electricity costs for any electricity utility company.

Thus, summarizing, conventional AC rectification has the following main disadvantages:

- It creates harmonics and electromagnetic interference (EMI).
- It has poor power factor.
- It produces high losses.
- It requires over-dimensioning of parts.
- It reduces maximum power capability from the line.

3.3 Requirements as Per Law

Thus, the harmonics generated as a result of conventional AC rectification must be filtered and this has prompted a need for setting limits for the line current harmonics generated by equipment connected to the electricity distribution network. Standardization activities in this area have been carried out for many years. As early as 1982, the International Electrotechnical Committee (IEC) published its standard IEC 555-2, which was also adopted in 1987 as the European standard EN 60555-2, by the European Committee for Electrotechnical Standardization (CENELEC). The IEC 555-2 Standard was later replaced in 1995 by the IEC 1000-3-2 standard and subsequently adopted by CENELEC as the European standard EN 61000-3-2 [3.7].

Today, in Europe, compliance to the EN 61000-3-2 is a legal requirement. After many amendments, the standard today applies to any equipment with a rated current up to and including 16A RMS per phase and which is to be connected to the 50Hz, 230V single-phase or 400V three-phase mains network. Depending on the type of equipment and its probable frequency of daily usage, all electrical equipment are categorized into four classes, namely, Class A, B, C and D. Specific maximum limits are set for the harmonic content of the line current drawn by the equipment. Of these, the Class D limits are the most difficult to meet, as the limit depends on the equipment's power rating and applies to equipment that is connected to the utility network for a significant part of its life cycle resulting in the greatest impact on the power supply network. Personal computers and television sets are examples of such equipment. Also, an important waiver is that other than lighting equipment, limits do not apply for equipment with rated power of 75 W or less (it may be reduced to 50 W in the future).

Thus, any equipment connected to the public utility grid in the European Union is covered by these four classes. Each class has its own set of limits for harmonic currents. Briefly, these different limits are as under:
Class A equipment: All equipment that does not fit into the other three classes are categorized as Class A equipment. This class set the absolute maximum current values allowed for each harmonic and these are given in **Table 3.1**. Limits do not change with equipment rating.

Class B equipment: All portable tools are categorized as Class B equipment. Harmonic current limits are absolute maximum values. As power tools are used infrequently/for short periods, Class B limits are the least restrictive and set the absolute maximum current allowed for each harmonic to 1.5 times the Class A limits.

Class C equipment: All lighting products, including dimming devices, with an active input power higher than 25 W are categorized as Class C equipment. There are limits on the second harmonics and also on all odd harmonics. The limits are expressed in terms of the fundamental current's percentage. The maximum current percentage allowed for each harmonic, to meet Class C limits, is shown in **Table 3.2**.

Class D equipment: All equipment like computers and television sets that are frequently used for longer periods are categorized as Class D equipment. The limits depend on the power rating of the equipment. The current limit for Class D is expressed in terms of mA per Watt of the power consumed. Thus, the acceptable limit of the harmonic current being generated by a load is proportional to its power rating. Hence, low power equipment have a lower absolute limit of harmonic current. These limits are given in **Table 3.1**.

Table 3.1: EN 61000-3-2, Class A & Class D
Harmonic Current limits

Harmonic order (n)	**Class A**	**Class D**	
	Absolute limit (No Power limit)	Relative limit (600 W ≥ Power >75 W)	Absolute limit (600 W ≥ Power >75 W)
	Maximum permissible harmonic current (A)	Maximum permissible harmonic current per watt (mA/W)	Maximum permissible harmonic current (A)
Odd Harmonics			
3	2.30	3.4	2.30
5	1.14	1.9	1.14
7	0.77	1.0	0.77
9	0.40	0.5	0.40
11	0.33	0.35	0.33
13	0.21		
15 ≤n≤ 39 (Class A)		Use following equations	
13 ≤ n ≤ 39 (Class D)	2.25/n	3.85/n	2.25/n
Even Harmonics			
2	1.08		
4	0.43		
6	0.30	Not Applicable	
8 ≤ n ≤ 40 (Class A)	1.84/n		

Table 3.1. Limits for Class A and Class D equipment.

Table 3.2: EN 61000-3-2, Class C
Harmonic Current limits

Harmonic order (n)	Maximum permissible harmonic current expressed as a percentage of the input current at the fundamental frequency
2	2
3	30 × circuit power factor
5	10
7	7
9	5
11≤n≤39	3

Table 3.2. Limits for Class C equipment.

Paper A discusses in detail the causes of input current distortion in AC- DC single phase rectifier- capacitor filter circuits and the mandatory low-frequency harmonic limits of the European standard EN 61000-3-2. Different Power Factor Correction (PFC) techniques / strategies useful for complying with the standard are discussed in detail.

For higher power and higher voltage applications, the IEEE 519-1992 Standard [3.8] gives recommended practices and requirements for harmonic control in electrical power systems, for both individual consumers and utilities. The limits for line current harmonics are given as a percentage of the maximum fundamental frequency component of the load current demand I_L, at the Point of Common Coupling in the utility. The limits depend on the short-circuit current at the Point of Common Coupling resulting in lower limits for weaker grids. However, since standards are evolving, changes can be expected in the future.

3.4 Passive Power Factor Correction Methods

As described earlier in **Section 3.1**, power factor depends on both harmonic content and displacement power factor. Moreover, the EN 61000-3-2 standard sets limits on the harmonic content of the load current and does not specifically regulate the power factor or the total harmonic distortion of the line current. In consideration of the above, the following can be concluded.

- A high power factor can be achieved even with a substantial harmonic content. The power factor is not significantly degraded by harmonics, unless its amplitude is quite large.
- Low harmonic content does not guarantee high power factor.

Thus, PFC circuits for nonlinear loads have their primary goal to reduce the harmonic content of the line current. PFC circuit solutions can be broadly categorized as *passive* or *active* circuits. In *passive* PFC, only passive elements are used in addition to the diode bridge rectifier, to improve the shape of the line current. The output voltage is not regulated and it follows the line variations. In *active* PFC, active switches are used in conjunction with inductors. The output voltage is usually regulated for line variations. The switching frequency further differentiates the active PFC solutions into two classes, the *low -frequency* and the *high-frequency* active PFC. In *low-frequency* active PFC circuits, the switching is synchronized to the line voltage. In *high-frequency* active PFC circuits, the switching frequency is much higher than the line frequency.

3.4.1 Improving Harmonics by Reducing the Filter Capacitance of Rectifier Filter Circuits

Fig. 3.2a shows the schematic of a typical single-phase diode rectifier filter circuit. The simplest way to improve the shape of the line current for this circuit is to use a lower filter capacitance. This increases the output DC voltage ripple but helps increase the rectifier conduction interval resulting in a lower input peak current. This also helps in reducing the harmonic content and improves the power factor but this is far from the ideal solution. For a constant power load with output capacitor values of 68 μF and 470 μF, the simulated input current waveforms are shown in **Fig. 3.2b** while the output ripple waveforms is shown in **Fig. 3.2c**. For each of these filter capacitor values, the odd line current harmonics are normalized to the fundamental and shown in **Fig. 3.2d** and **Fig. 3.2e** respectively. This scheme has such severe limitations since it does not substantially reduce the harmonic currents and the high output voltage ripple makes it unacceptable for most applications.

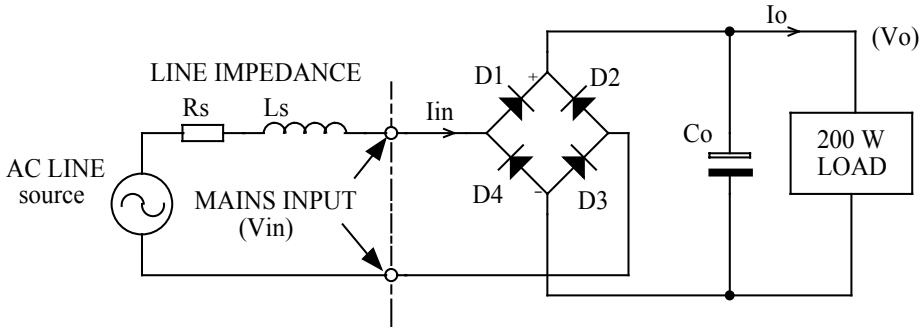

Fig. 3.2a. Schematic of a typical single-phase rectifier filter circuit with filter capacitor C_o= 68 μF and C_o= 470 μF.

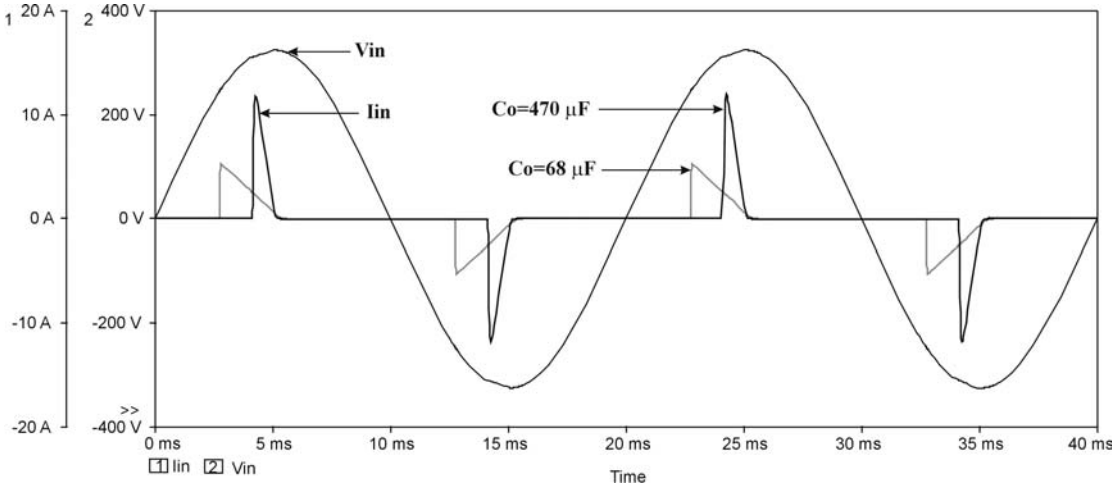

Fig. 3.2b. Simulated input voltage and current waveforms with filter capacitor C_o= 68 μF and C_o= 470 μF.

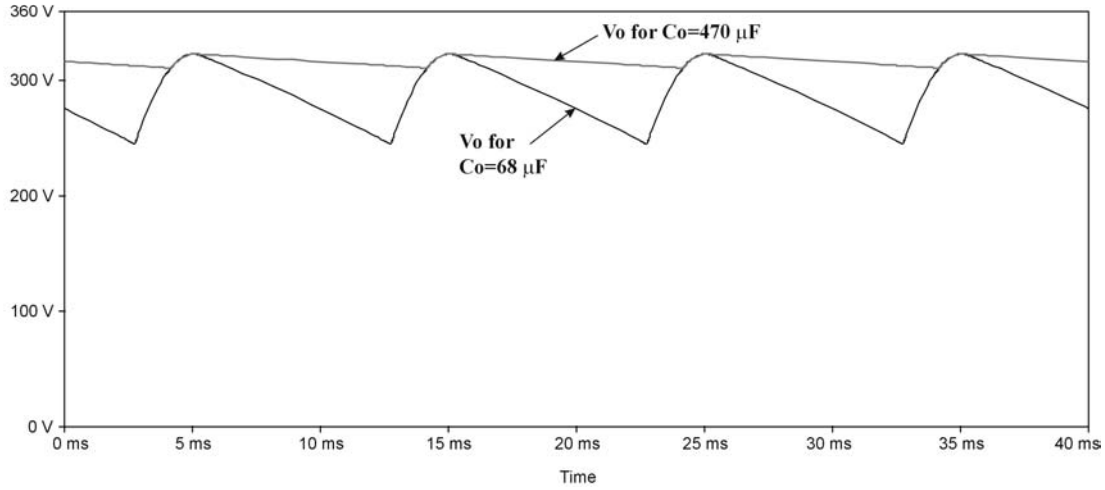

Fig. 3.2c. Simulated output ripple waveforms with filter capacitor C_o= 68 μF and C_o= 470 μF.

It is apparent from above that in this scheme the output ripple increases as the output capacitor is reduced. Usually, this increased output ripple is not a major concern at low power levels since the load is usually a switch mode converter and it can easily adjust its duty cycle to deliver a constant load power.

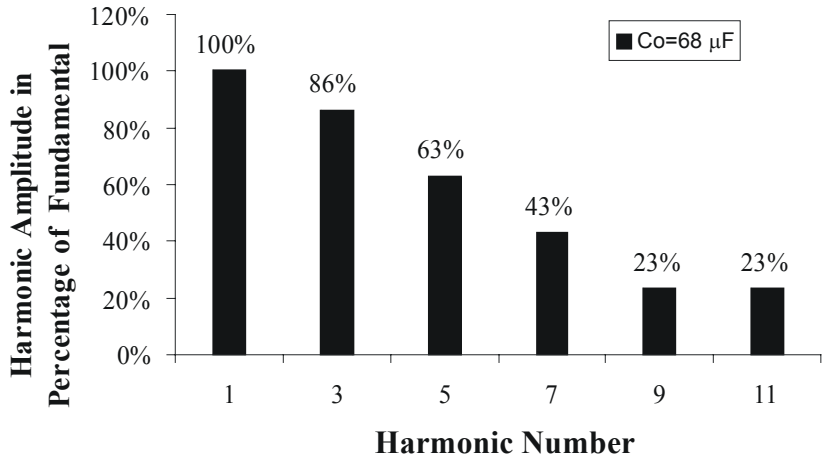

Fig. 3.2d. Odd line current harmonics normalized to the fundamental with filter capacitor C_o= 68 μF**.**

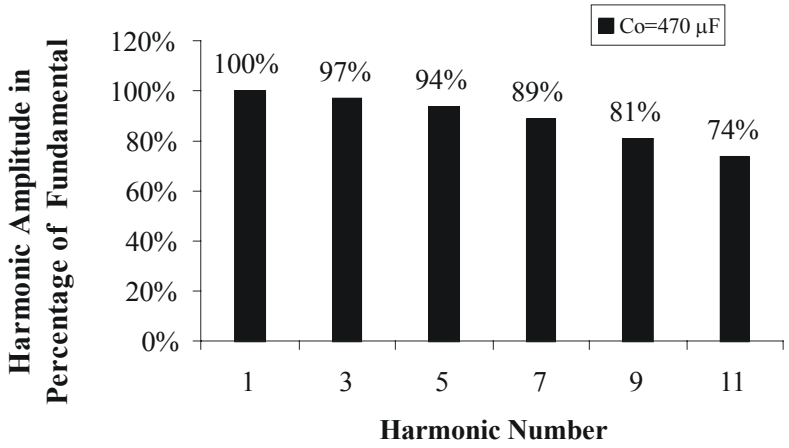

Fig. 3.2e. Odd line current harmonics normalized to the fundamental with filter capacitor C_o= 470 μF**.**

3.4.2 Passive PFC

Passive PFC circuits use additional passive components in conjunction with the diode bridge rectifier. Various combinations of these passive components in different circuit locations give rise to many possible schemes. Only those schemes that are commonly used are covered in the following sections.

3.4.2.1 Passive PFC with Inductor on the AC Side

As shown in **Fig. 3.3a**, one of the simplest and popular methods to achieve PFC is to add an inductor on the AC side of the diode bridge in series with the line voltage. This improves the power factor considerably along with the reduction in the input current harmonics. Achieving a power factor of about 0.82 is practical. The output voltage is not regulated and the output DC voltage ripple increases with load. Popularly this is known as the passive PFC [3.9] and today it is possible to buy these inductors off the shelf.

The simulated input current waveforms for a 200 W constant power load, are shown in **Fig. 3.3b** for inductance values of 5 mH and 25 mH. For each of these inductance values, the odd current harmonics normalized to the fundamental is shown in **Fig. 3.3c** and **Fig. 3.3d** respectively.

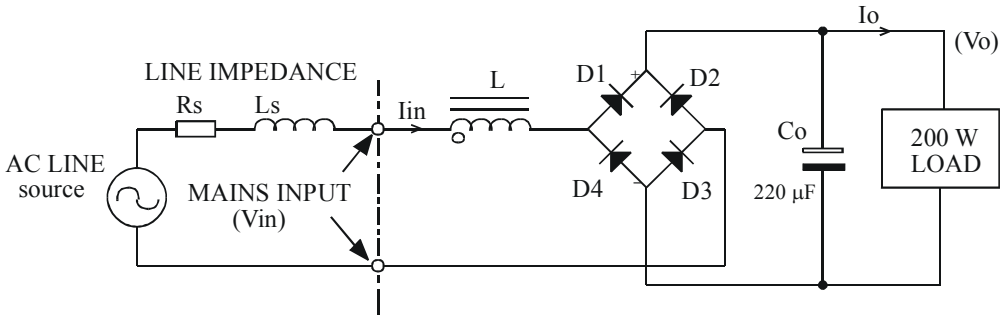

Fig. 3.3a. Typical schematic of a single-phase rectifier filter circuit with passive PFC circuit.

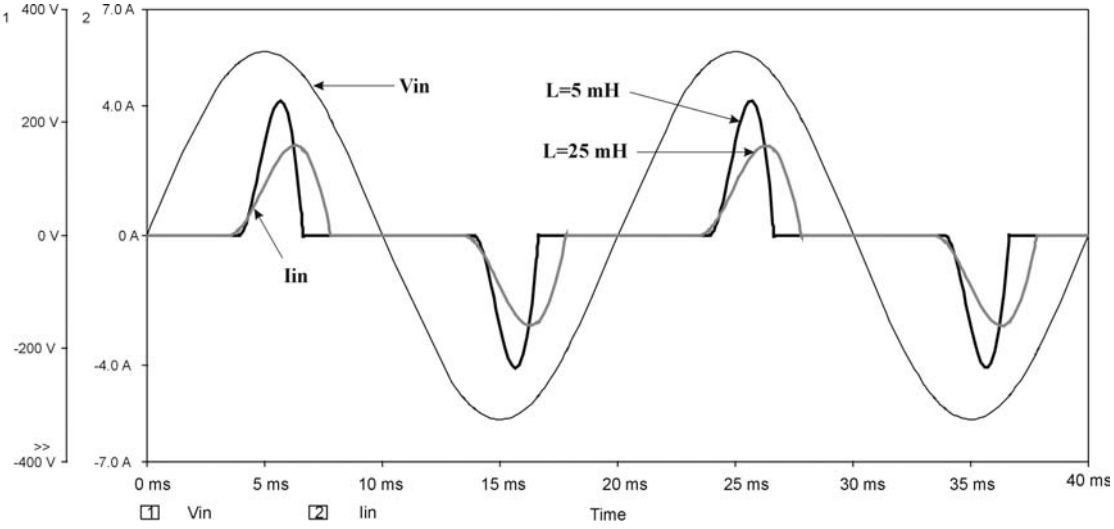

Fig. 3.3b. Simulated current and voltage waveforms for a 200 W constant power load with passive PFC circuit and inductance values of 5 mH and 25 mH.

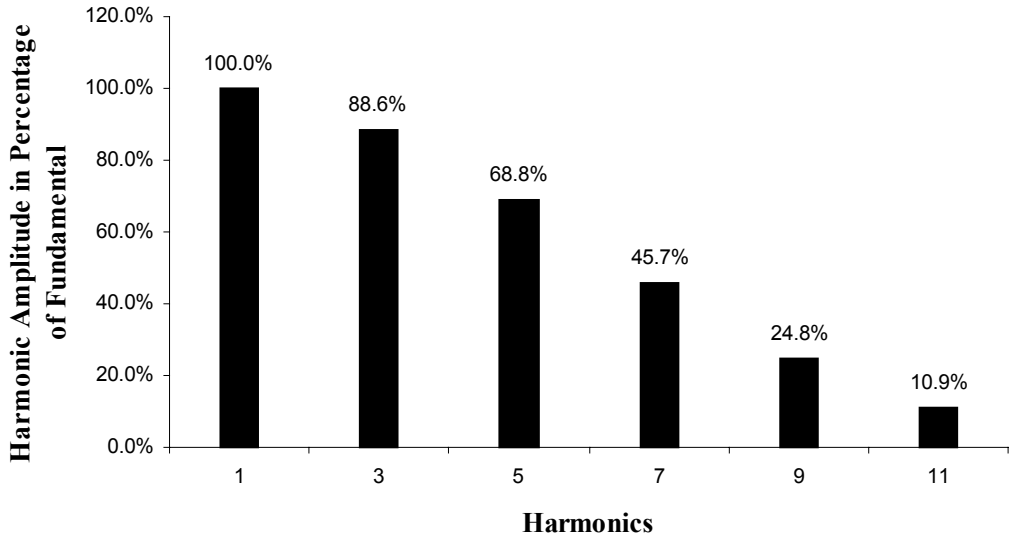

Fig. 3.3c. Odd line current harmonics normalized to the fundamental for a 200W constant power load with passive PFC circuit and 5 mH inductance.

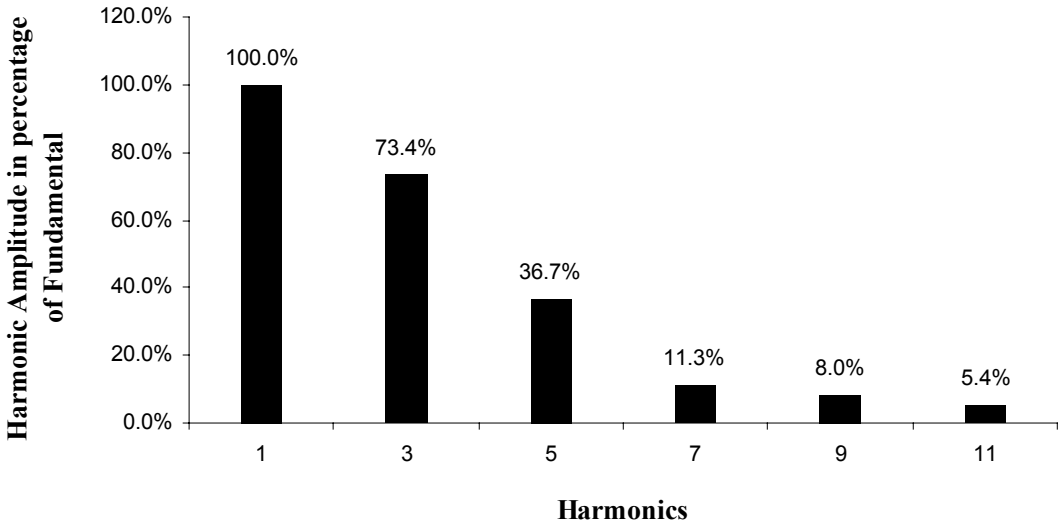

Fig. 3.3d. Odd line current harmonics normalized to the fundamental for a 200W constant power load with passive PFC and inductance value of 25mH.

3.4.2.2 Passive PFC with Inductor on the DC Side

For the next scheme shown in **Fig. 3.4a**, the inductor is placed on the DC side [3.10, 3.11]. If the inductor current is continuous for a given load current, the power factor can be as high as 0.9. Of course, this requires a relatively large inductance. When the inductor current becomes discontinuous due to reduction in load or when a lower inductance value is used, the input current wave shape becomes similar to that shown in **Fig. 3.3b** and the power factor also deteriorates to about 0.8.

For a 200 W constant power load with inductance values of 40 mH and 180 mH, the simulated input current waveforms are shown in **Fig. 3.4b**. For each of these inductors, the odd current harmonics normalized to the fundamental is shown in **Fig. 3.4c** and **Fig. 3.4d** respectively.

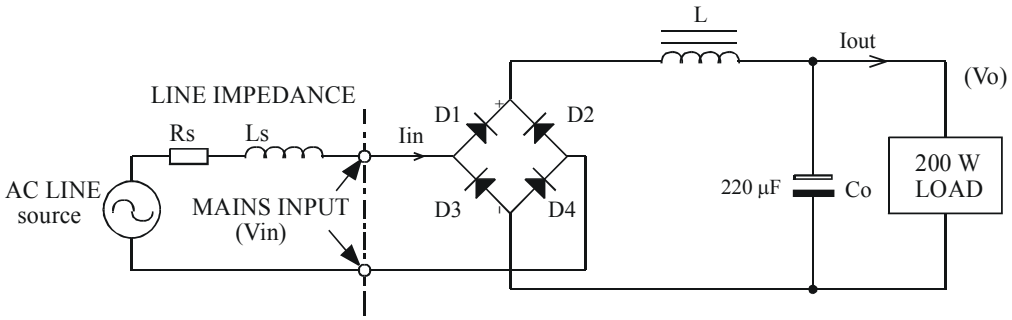

Fig. 3.4a. Typical schematic of a single-phase rectifier filter circuit with passive PFC circuit and the inductor on DC side.

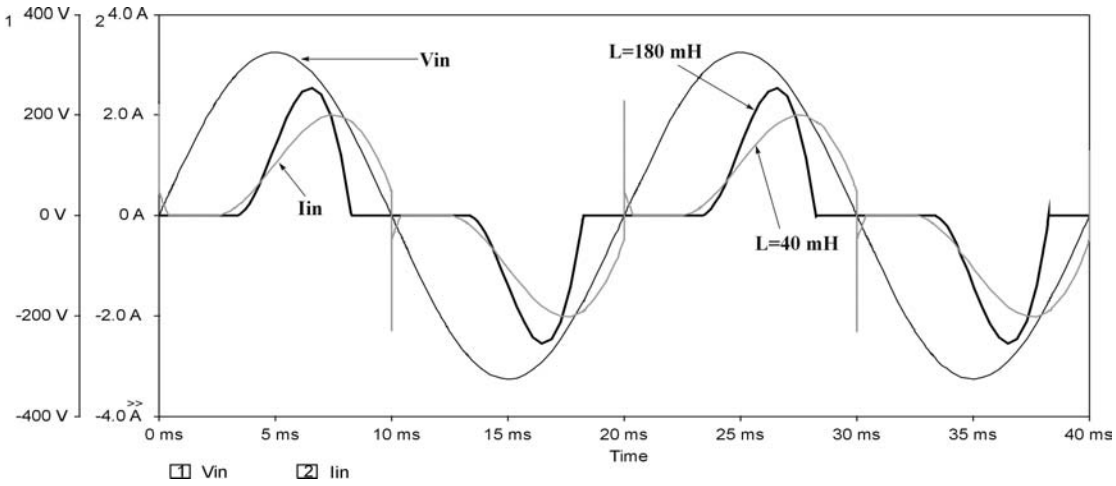

Fig. 3.4b. Simulated input current and voltage waveforms for a 200 W constant power load with passive PFC circuit and the inductor on the DC side for with inductance values of 40 mH and 180 mH.

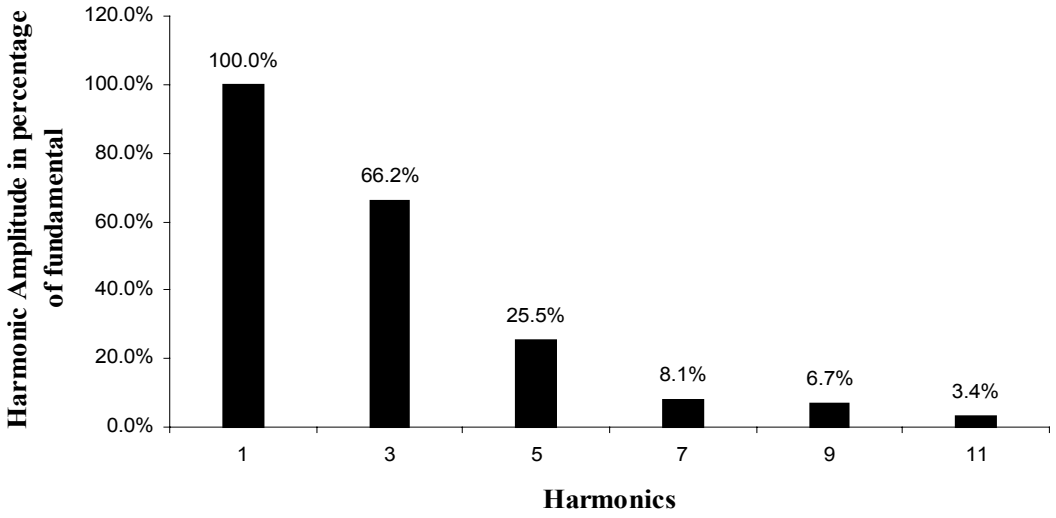

Fig. 3.4c. Odd line current harmonics normalized to the fundamental for a 200 W constant power load with passive PFC circuit and the inductor on the DC side with inductance value of 40 mH.

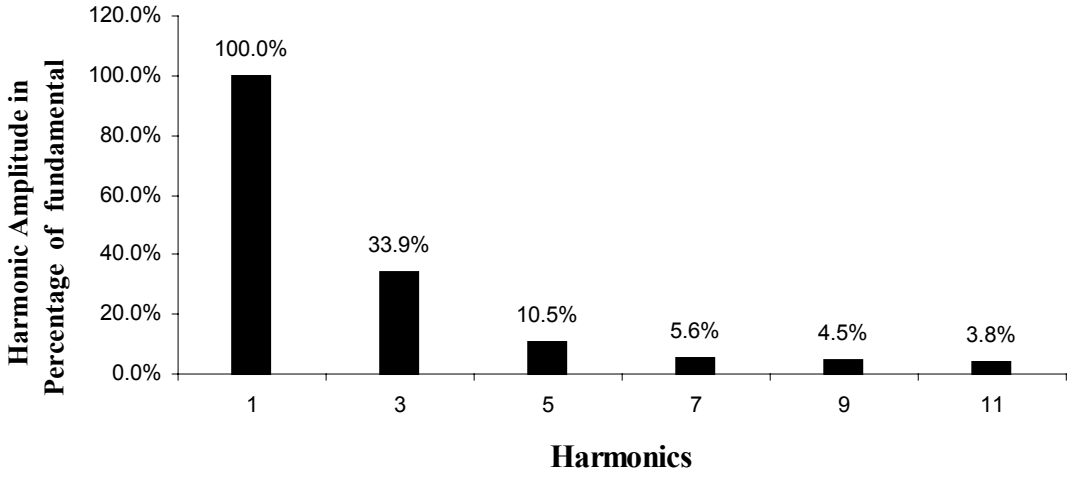

Fig. 3.4d. Odd line current harmonics normalized to the fundamental for a 200 W constant power load with passive PFC circuit and the inductor on the DC side with inductance value of 180 mH.

There are also several solutions based on resonant networks. When introduced in-between the AC source and the load, these attenuate the harmonics. Examples include a series resonant type band-pass filter tuned at the line-frequency or a parallel-resonant type band-stop filter tuned at the third harmonic. However, these solutions are not commonly used due to the large values of inductance and capacitance required for these networks.

3.4.2.3 Passive PFC with Harmonic Trap Filter

Another solution that is often used is a harmonic trap filter. This consists of a series resonant network, connected in parallel to the AC source and tuned to the harmonic frequency that must be attenuated. Usually two harmonic traps are used and these are tuned at the dominant 3^{rd} and 5^{th} harmonics. **Fig. 3.5a** shows the schematic of this scheme with a constant power load of 300 W. Here too, the output voltage is not regulated and the output DC voltage ripple increases with load. This scheme is not investigated in detail as it is expensive, requires large inductors and is frequency sensitive.

Simulated input current and input voltage waveforms for a harmonic trap filter based PFC scheme is shown in **Fig. 3.5b.** The odd line current harmonics normalized to the fundamental is shown in **Fig. 3.5c**. It can be seen that this scheme gives excellent power factor and input current wave shape at the expense of large reactive components.

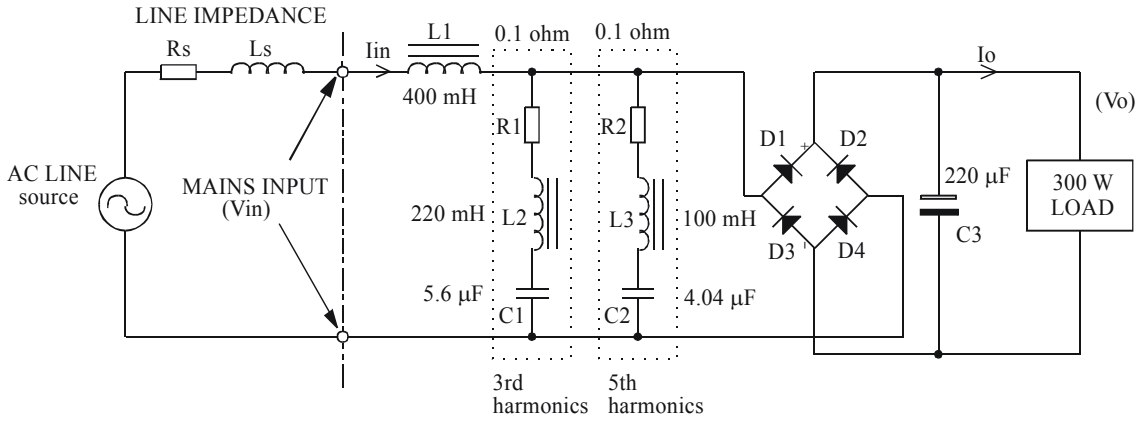

Fig. 3.5a. Typical schematic of a single-phase rectifier filter circuit with harmonic trap filter for passive PFC circuit.

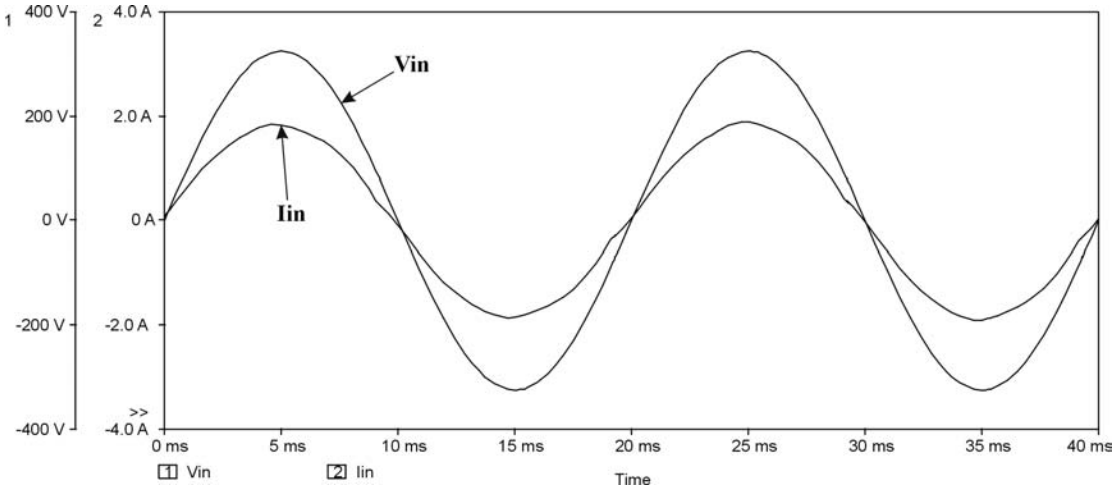

Fig. 3.5b. Simulated input current and voltage waveforms for a 300 W constant power load with harmonic trap filter for passive PFC circuit.

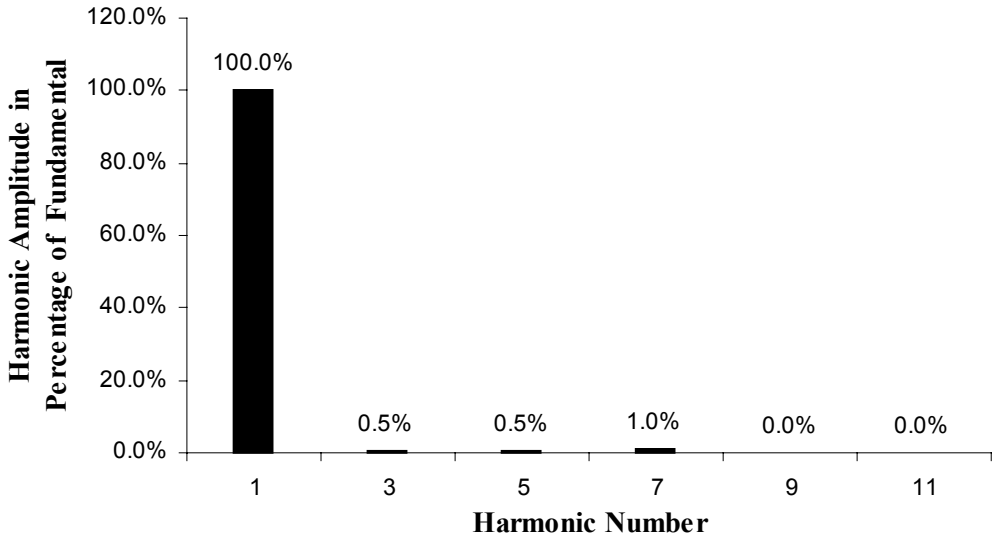

Fig. 3.5c. Odd line current harmonics normalized to the fundamental for a 300 W constant power load with harmonic trap filter for passive PFC circuit.

3.4.2.4 Passive PFC using Valley Fill Rectifier

Fig. 3.6a represents the schematic for a 200W constant power load valley-fill rectifier [3.12]. The circuit reduces the harmonic content of the line current but the output voltage varies significantly because of the large output ripple voltage. This solution is often used for lighting ballast circuits [3.13].

Simulated input current and voltage waveforms for a valley fill rectifier based PFC scheme with a 200 W constant power load and two different capacitance values of 470 μF and 100 μF, is shown in **Fig. 3.6b** while the output voltage waveforms are shown in **Fig. 3.6c**. For these capacitance values, the odd line current harmonics normalized to the fundamental is shown in **Fig. 3.6d** and **Fig. 3.6e**.

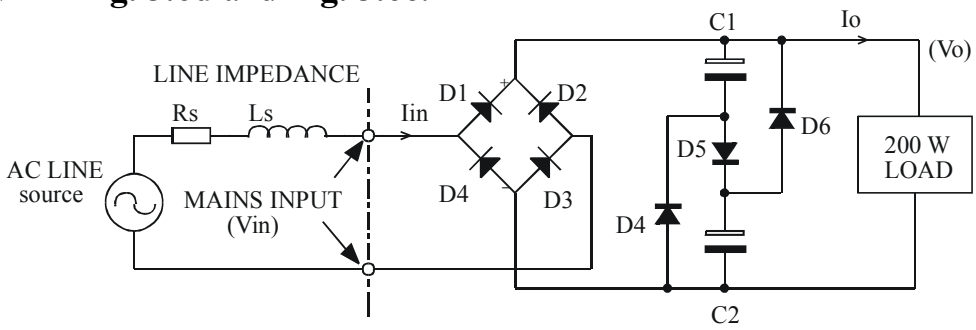

Fig. 3.6a. Typical schematic of a single-phase rectifier filter circuit for a valley fill rectifier based passive PFC circuit.

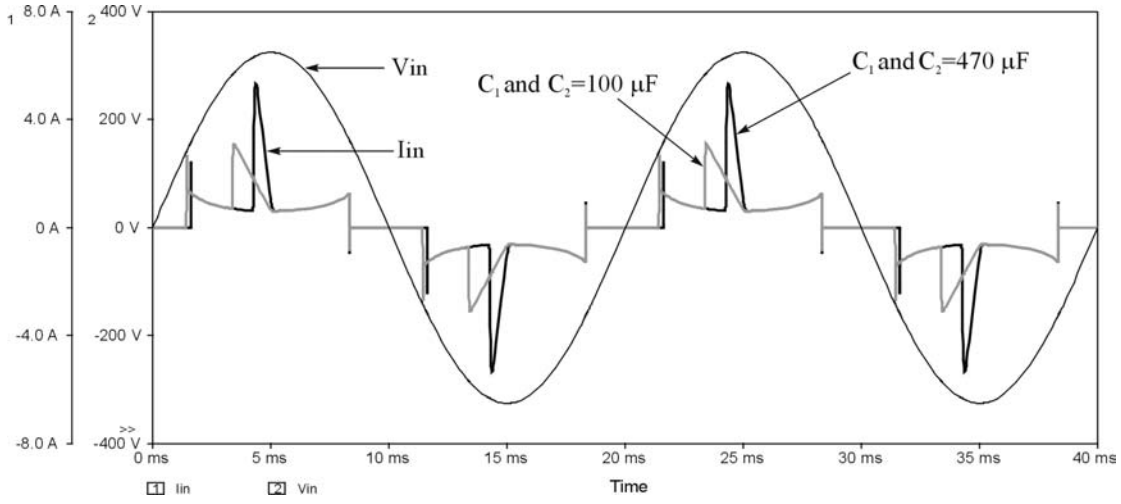

Fig. 3.6b. Simulated input current and voltage waveforms with a 200 W constant power load for a valley fill rectifier based passive PFC circuit with capacitance values of 100 μF and 470 μF.

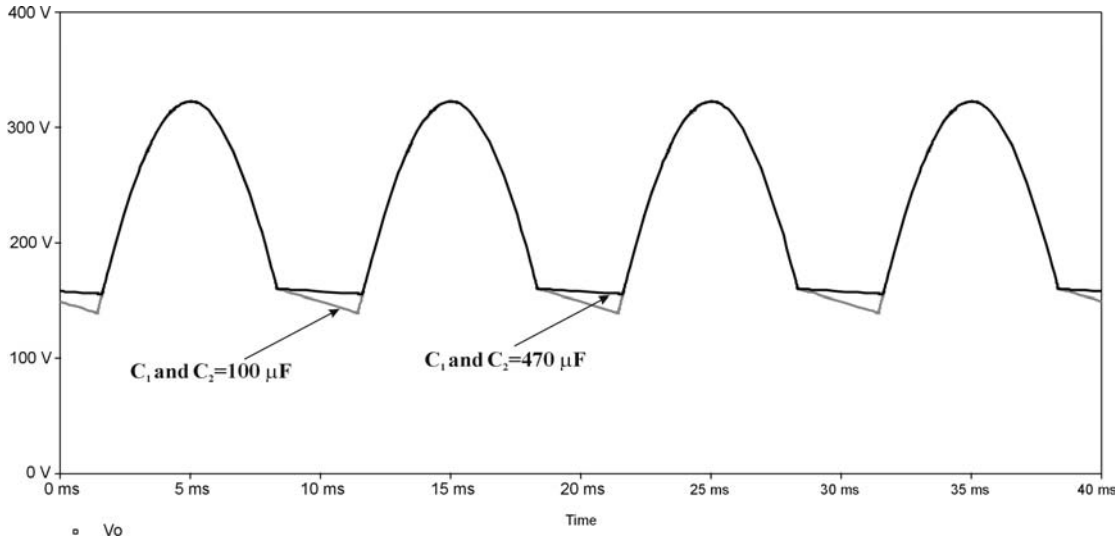

Fig. 3.6c. Simulated output voltage waveform with a 200 W constant power load for a valley fill rectifier based passive PFC circuit with capacitance values of 100 μF and 470 μF.

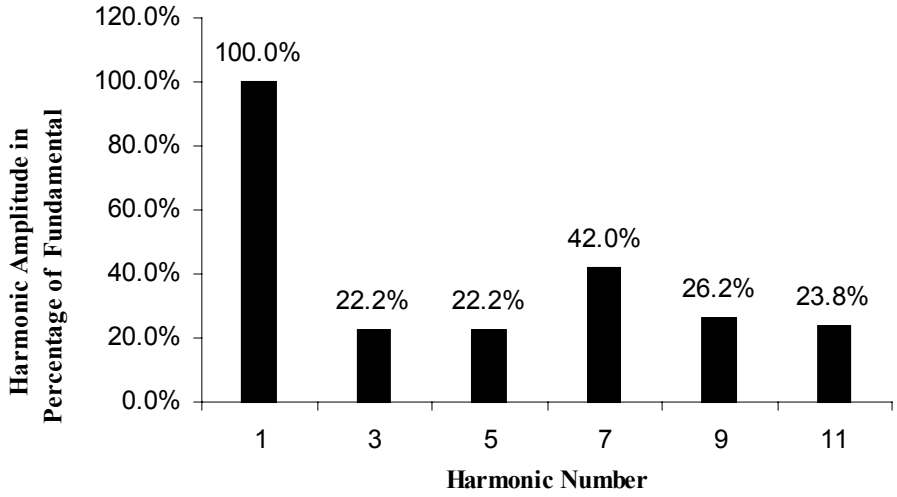

Fig. 3.6d. Odd line current harmonics normalized to the fundamental with a 200W constant power load for a valley fill rectifier based passive PFC circuit with capacitance value of 100 μF.

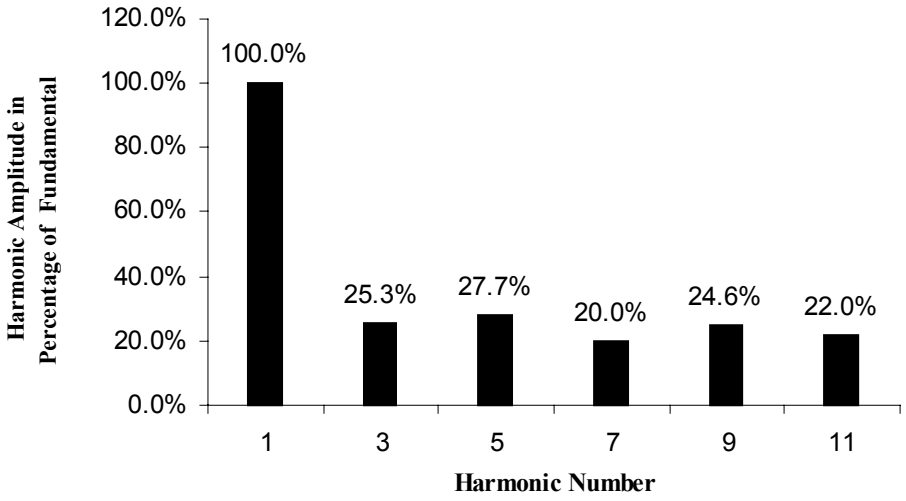

Fig. 3.6e. Odd line current harmonics normalized to the fundamental with a 200W constant power load for a valley fill rectifier based passive PFC circuit with a capacitance value of 470 μF.

3.4.2.5 Limitations of Passive PFC Circuits

The simplicity, reliability, insensitivity to noise and surges and the non-generation of any high-frequency EMI offered by passive power factor circuits are of significant usefulness. However, the bulky size of these filters, their poor dynamic response, complexity and high cost, the lack of voltage regulation and their sensitivity to line-frequency, limits their use to below 200 W applications. Moreover, even though line current harmonics are reduced, the fundamental component may show an excessive phase shift resulting in reduction in power factor.

3.5 Active Power Factor Correction Methods

Active PFC circuits that have better characteristics and do not have many of the above drawbacks are reviewed in the following sections.

3.5.1 Low Frequency Active PFC

An active low frequency PFC circuit for a 250W constant power load is shown in **Fig. 3.7a**. Input Power factors as high as 0.95 can be achieved with an active low frequency PFC circuit design. In this scheme, the switch (SW) is bi-directional and it is operated for a constant period after the line voltage zero crossing. After this constant on-period after the line voltage zero crossing or when the output voltage tries to increase beyond

the set limits, this switch (SW) is turned off. This forces an increase in the conduction angle [3.14] of the input bridge rectifiers, giving rise to an acceptable current waveform. Simulated input current and voltage waveforms for an active low frequency PFC circuit with a 250 W constant power load and two different inductance values of 150 mH and 75 mH, is shown in **Fig. 3.7b**. The odd line current harmonics normalized to the fundamental is shown in **Fig. 3.7c** and **Fig. 3.7d**.

This scheme has the advantage that it generates less EMI, requires a smaller inductor when compared to the passive PFC and the simple low frequency circuit is more reliable and efficient when compared to the active high frequency PFC scheme described later.

However, when compared to the high frequency active PFC circuit, the reactive elements are larger and the regulation of the output voltage is slower.

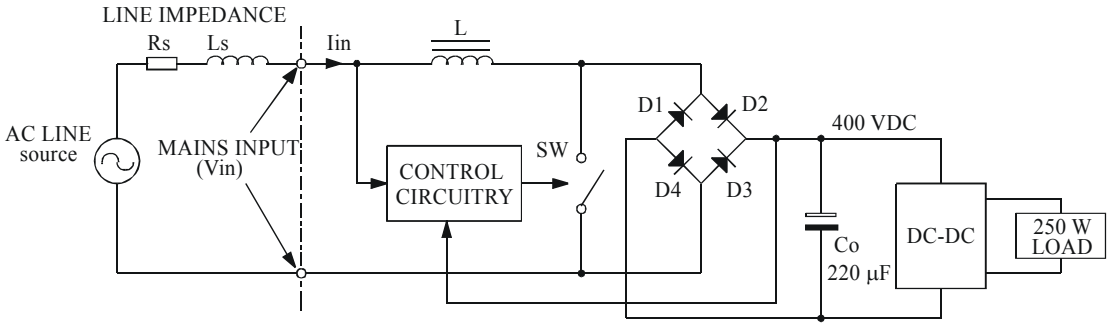

Fig. 3.7a. Typical schematic of a low frequency active PFC circuit.

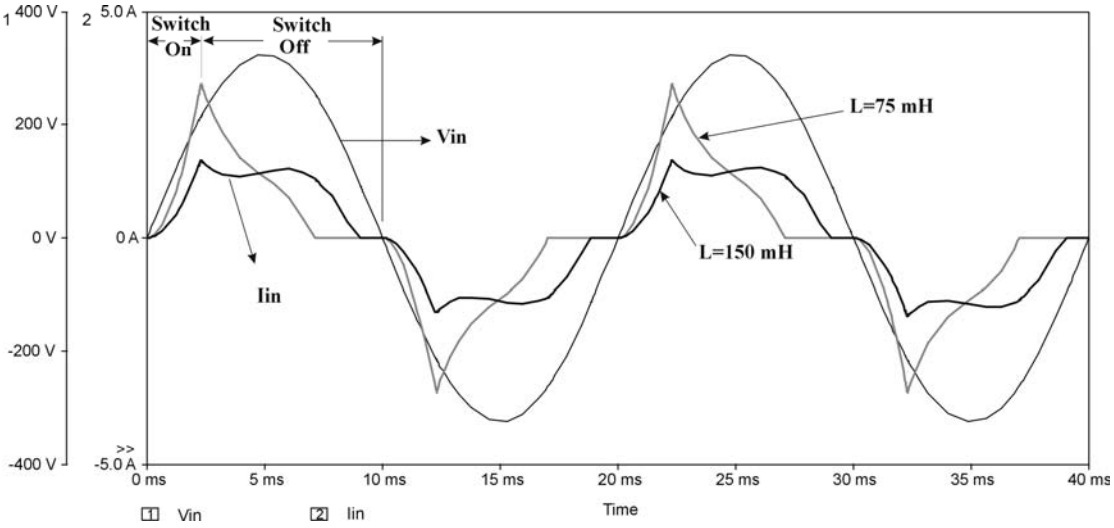

Fig. 3.7b. Simulated input current and voltage waveforms for a 250 W constant power load with low frequency active PFC circuit and inductance values of 75 mH and 150 mH.

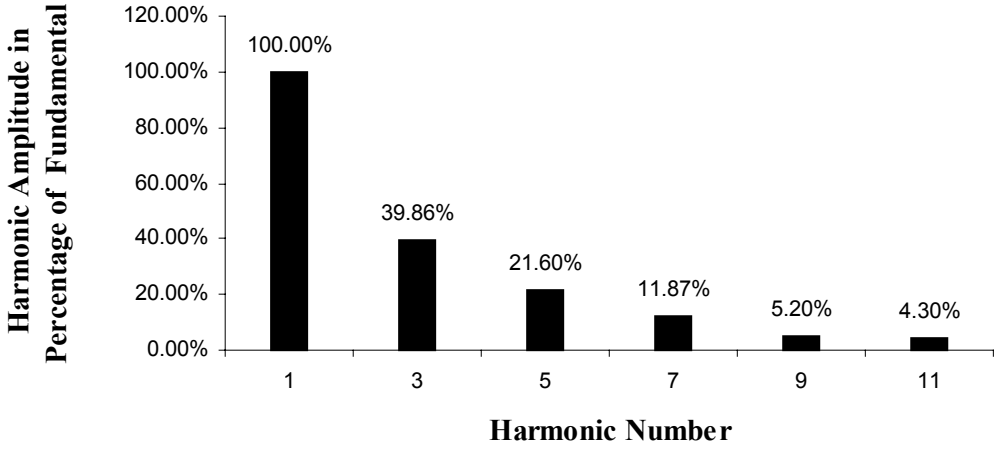

Fig. 3.7c. Odd line current harmonics normalized to the fundamental with a 250 W constant power load for a low frequency active PFC circuit with an inductance value of 75 mH.

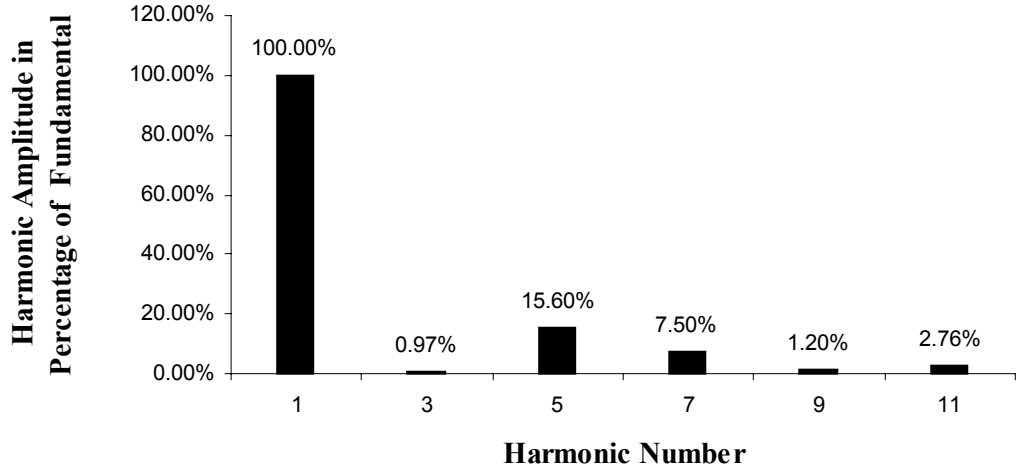

Fig. 3.7d. Odd line current harmonics normalized to the fundamental with a 250 W constant power load for a low frequency active PFC circuit with an inductance value of 150 mH.

3.5.2 High Frequency Active PFC

The high frequency active PFC circuit can be realized by placing a buck or a boost or a buck-boost converter in between the bridge rectifier and the filter capacitor of a conventional rectifier filter circuit and operating it by a suitable control method that would shape the input current. For all converter topologies, the switching frequency is much higher than the line-frequency, the output voltage ripple is twice the line-frequency and the output DC is usually regulated.

The PFC output voltage can be higher or lower, depending on the type of converter being used. With a buck converter the output voltage can be lower, for a boost converter the output voltage can be higher, while for a buck-boost converter the output voltage can be higher or lower than the maximum amplitude of the input voltage. The inductor current in these converters can be either continuous or discontinuous. In the continuous conduction mode (CCM) the inductor current never reaches zero during one switching cycle while in the discontinuous conduction mode (DCM), the inductor current is zero during intervals of the switching cycle. However, though the inductor current can be continuous in all the three types of converters, the high frequency switching current components of the AC input current can be continuous only in the case of the boost converter. This is because for the buck and the buck-boost converter, the converter switch interrupts the input current in every switching cycle.

This is apparent from the operating characteristics of each converter described below. The given waveforms are representative and shown only for explanation of the topology specific characteristics. In reality, the switching frequency is much higher than the line-frequency and the input AC current waveform is dependent on the type of control being used. The inductors are assumed to be in the CCM of operation.

3.5.2.1 Buck Converter Based Active PFC

A buck converter based PFC circuit that steps down the input voltage is shown in **Fig. 3.8a** and **Fig. 3.8b** shows its associated waveforms. However since the converter can operate only when the instantaneous input voltage $V_{in(t)}$ is higher than the output voltage V_o, there is no current flow from the AC input during the period t_1 and t_2. This gives the line current envelope a distortion near the input voltage zero crossing. Moreover, even if the inductor current is continuous, the input switching current of the converter is discontinuous as the high frequency switch S interrupts the input current during every switching cycle. Thus, the input current has significant high-frequency components that increases EMI and filtering requirements.

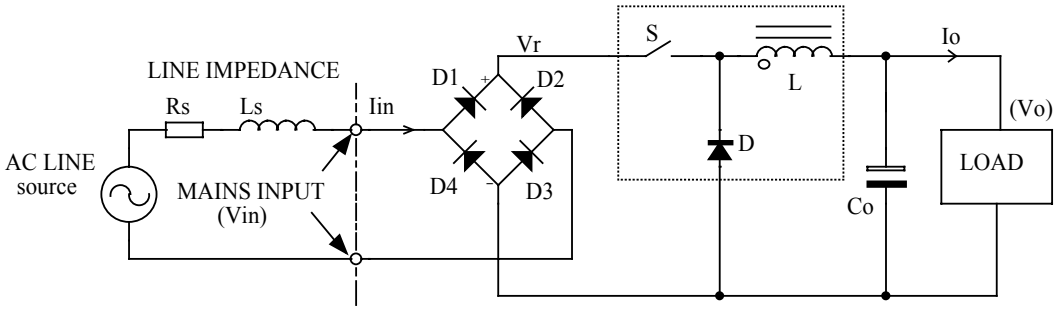

Fig. 3.8a. Buck converter based high frequency active PFC circuit.

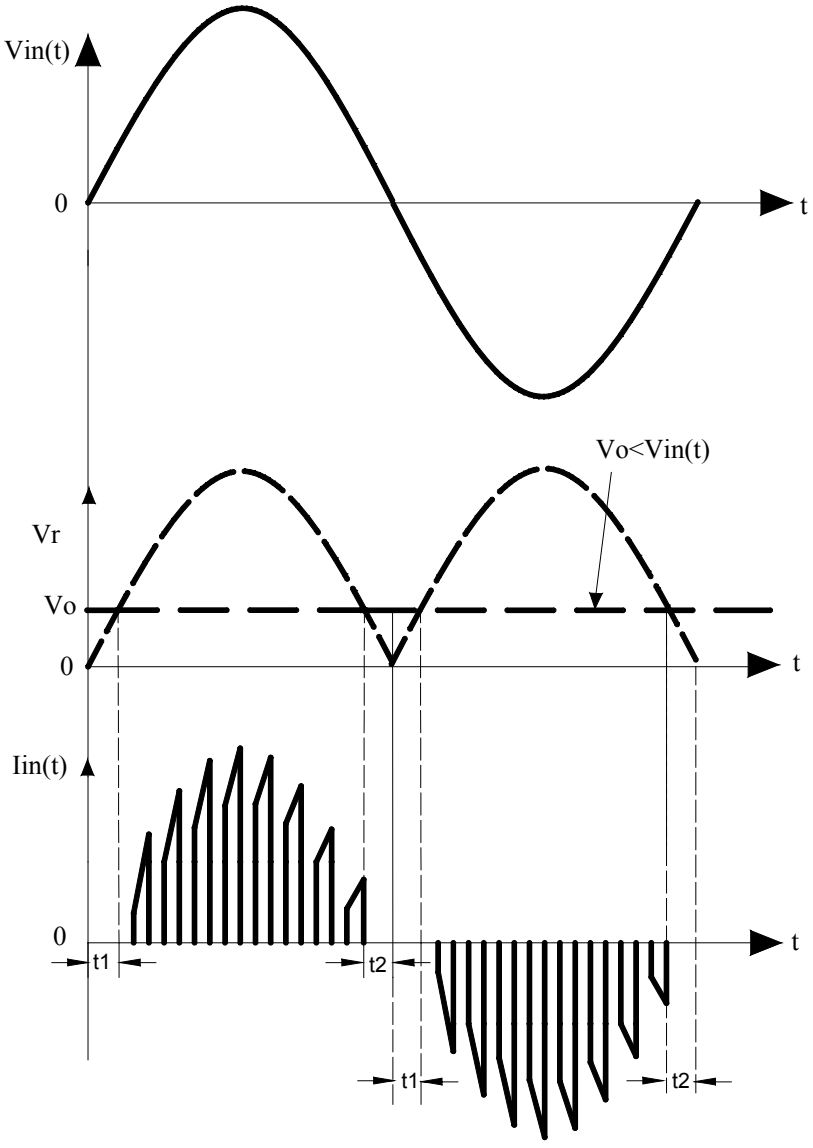

Fig. 8b Current and voltage waveforms of a Buck converter based PFC circuit.

3.5.2.2 Boost Converter Based Active PFC

The boost converter, the most common topology used for power factor correction, can operate in two modes – continuous conduction code (CCM) and discontinuous conduction mode (DCM). The transition mode control, also referred to as critical conduction mode (CRM) or boundary conduction mode, maintains the converter at the boundary between CCM and DCM by adjusting the switching frequency.

A CCM boost converter based PFC circuit and its associated waveforms are shown in **Fig. 3.9a** and **Fig. 3.9b**.

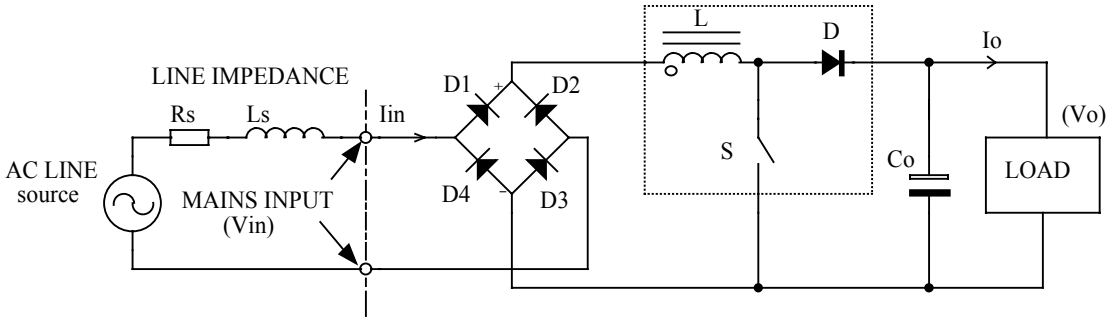

Fig. 3.9a. Boost converter based high frequency active PFC circuit.

This topology steps up the input voltage. Since the converter can operate throughout the line-cycle, the input current does not have crossover distortions. This gives the line current envelope no distortion near the input voltage zero crossing. Moreover, the input switching current of the converter is continuous as the boost inductor is placed in series with the input, and the high frequency switch S does not interrupt the input current. Thus, the input current has lesser high-frequency components resulting in lower EMI and reduced filtering requirements. The output capacitor C_o limits the switch S's turn-off voltage to almost the output voltage through diode D and thus protects the switch.

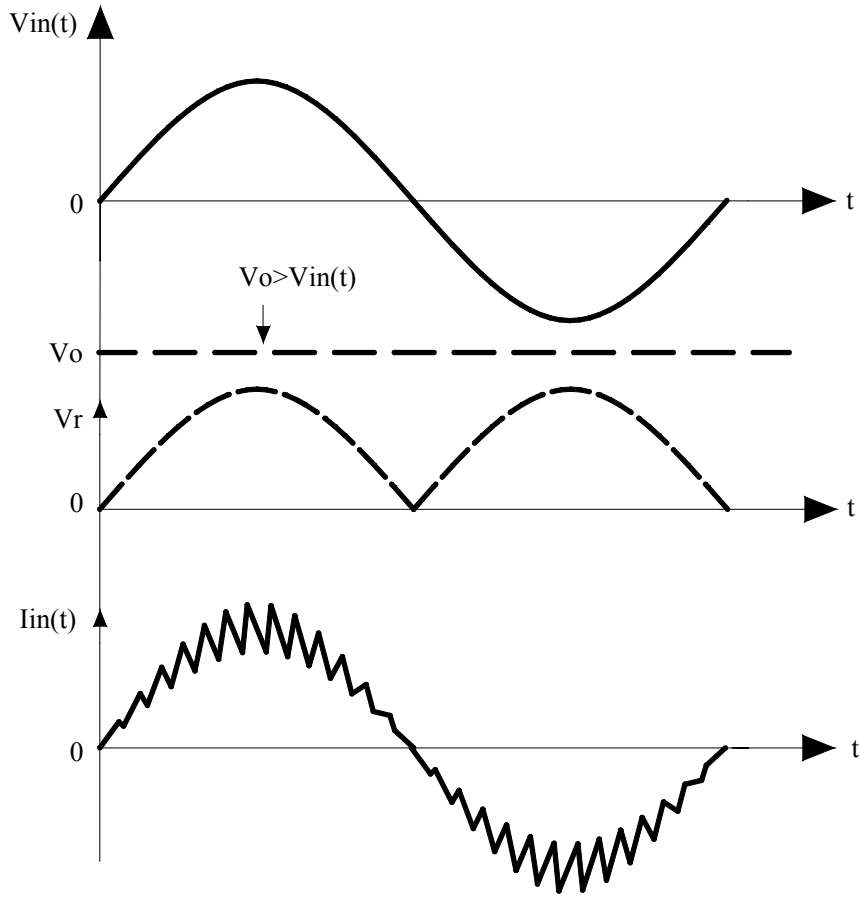

Fig. 3.9b. Current and voltage waveforms of a CCM boost converter based PFC circuit.

In the above converter, the control scheme can force the current in the inductor to be either continuous or discontinuous. The DCM converter operates at fixed frequency and has switching current discontinuities in comparison to the CCM or CRM techniques. Due to the large peak currents and EMI associated with the DCM converter, it is rarely or never used. These large peak currents are due to the dead time needed at certain instantaneous input voltages to remain discontinuous over all input line variations. On the other hand the CRM converter typically uses a variation of hysteretic control with the lower boundary equal to zero current. It is a variable frequency control technique that has an inherently stable input current control while eliminating reverse recovery rectifier losses. For a given set of input and output parameters, the on-time remains the same, but the off- time is varied. The result of this is that the switching frequency of the power converter, is highest when the instantaneous input voltage is the lowest, and vice versa.

The power stage equations and the transfer functions of the CRM converter are the same as the CCM converter. Transition mode forces the inductor current to operate just at the border of CCM and DCM. The current profile is also different and affects the component power loss and filtering requirements. The peak current in the CRM boost converter is twice the amplitude of the CCM boost converter leading to higher conduction losses. The peak-to-peak ripple is twice the average current, which affects MOSFET switching losses and AC losses in the boost inductor. The main trade-off in using the CRM boost converter is lower losses due to no reverse recovery in the boost diode at the expense of higher inductor ripple and peak currents. As presented in **Paper C**, with the present availability of very fast diodes, this issue is now a declining concern for designers today.

For medium to higher power applications, where the input filter requirements dominate the size of the magnetics, the CCM boost converter is a better choice due to lower peak currents (which reduces conduction losses) and lower ripple current (which reduces input filter requirements and inductor AC losses).

For these reasons, the CCM converter is popular and used widely for PFC circuit applications where the power rating is greater than 100 W.

The inductor current for a 100 W converter operating in the CCM and CRM mode, are compared in **Fig. 3.10**. The peak inductor current is shown as I_{peak} while the average inductor current is shown as $I_{average}$.

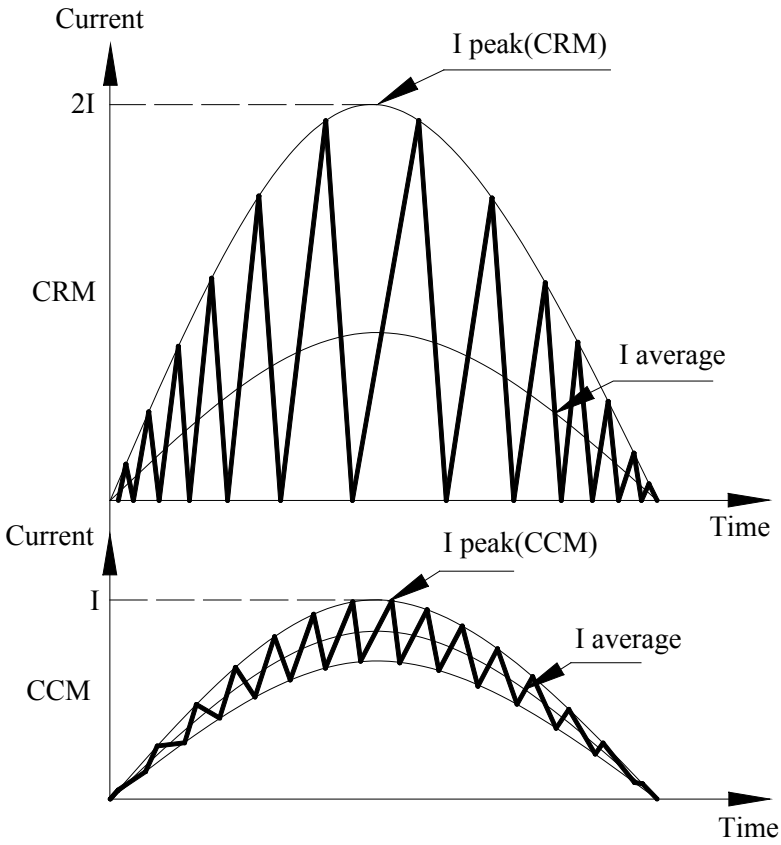

Fig. 3.10. Comparison of inductor current for CCM and CRM operating modes.

3.5.4.3 Buck-Boost Converter Based Active PFC

Lastly, the buck-boost converter based PFC circuit and its associated waveforms are shown in **Fig. 3.11a** and **Fig. 3.11b**. This can step up or step down the input voltage. The output voltage is inverted, which translates into higher voltage stress for the switch. Since the converter can operate throughout the line-cycle, the input current does not have crossover distortions. This gives the line current envelope no distortion near the input voltage zero crossing. However, even if the inductor current is continuous, like the buck converter, the input switching current of the converter is discontinuous as the high frequency switch S interrupts the input current. Thus, the input current has significant high-frequency components that increases EMI and filtering requirements.

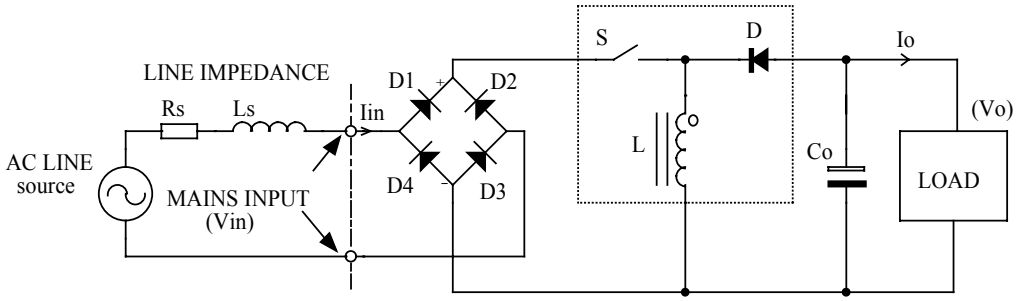

Fig. 3.11a. Buck-boost converter based high frequency active PFC circuit.

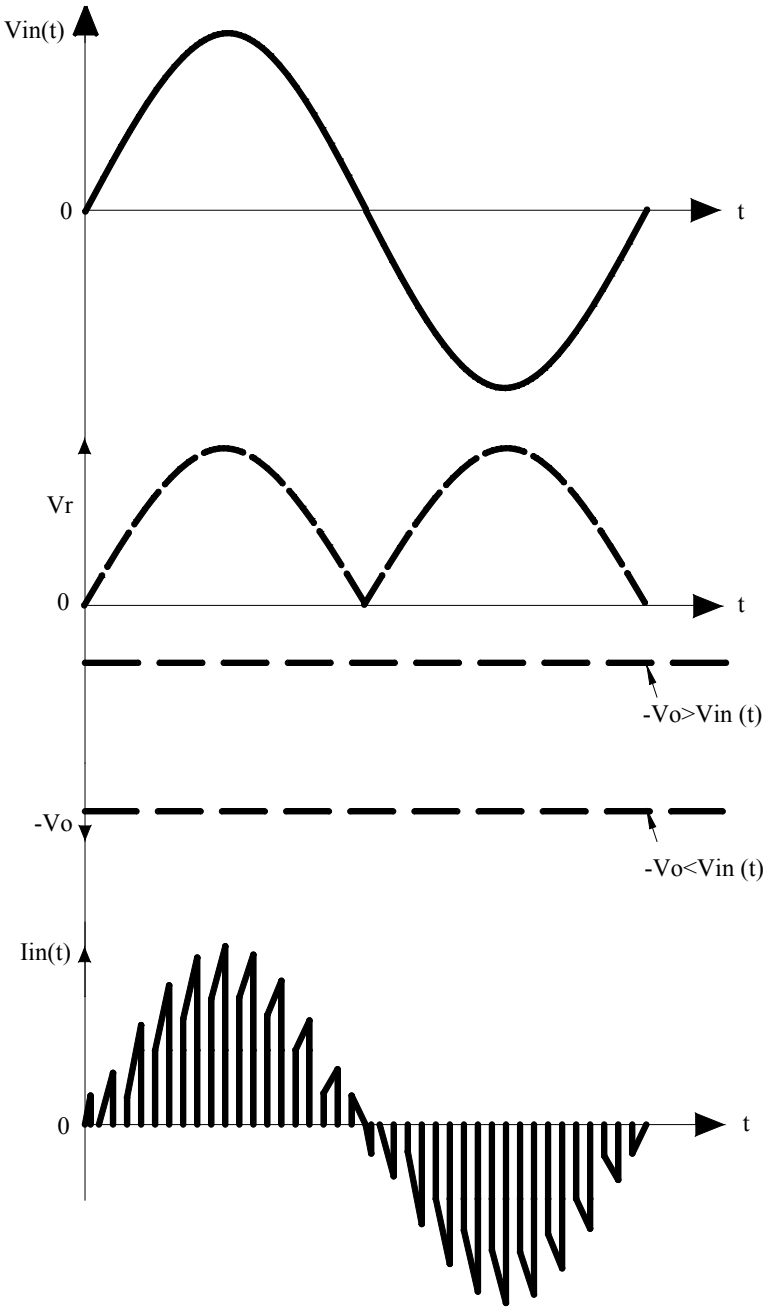

Fig. 3.11b. Current and voltage waveforms of buck-boost converter based PFC circuit.

3.6 The Future of Power Factor Correction

Today PFC techniques are being increasingly used in most new off- line power converter designs. This is motivated both by the concerns listed above and by the regulatory requirements, and this is an overall positive development for equipment users and the power utilities. Most PFC circuits are now active rather than passive, and while this results in exceptional PFC performance, it requires that additional circuitry be added. The added circuitry can have the following negative impacts on the system:

- Additional cost and complexity for the power converter.
- Lower power converter reliability due to additional components.
- Slightly lower efficiency due to additional conversion stage.

In spite of these limitations, including an active PFC is most often a very good design trade-off for the power system. The above concerns are usually more than offset by the reduced input current, undistorted current waveforms, universal input operation and additional useful power capability of converters that utilize PFC.

Thus, active power factor correction is an emerging need for all AC-DC converter designs, and optimizing cost and performance of these continuous mode PFC circuits is the need of the day.

Chapter 4

A Novel Power Factor Correction Scheme

As discussed earlier, the internal circuits of most small electronic equipment does not work directly from the rectified supply voltage derived from the mains network. Instead an in built DC-DC converter converts the rectified high voltage derived from the mains network to much lower isolated voltages like 5 V or 12 V, usable directly by the equipment's internal semiconductor circuits.

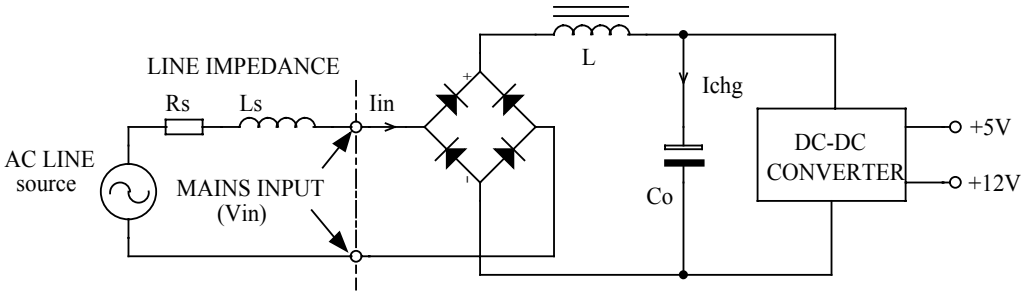

Fig. 4.1 Simplified block diagram of the input circuit of most small electronic equipment.

Fig. 4.1 represents a simplified block diagram of the input circuit of most small electronic equipment. The mains voltage is rectified to get an unregulated high voltage across the filter capacitor, (C_o). The harmonic currents generated by the charging of this capacitor are attenuated by the series connected choke (L), to provide passive power factor correction. Assuming a line variation of 230 V ± 20 %, the DC voltage across the filter capacitor would vary between the $V_{in(\min)}$ and $V_{in(\max)}$ limits given below.

$$V_{in(\min)} = 0.8 \times 230 \times \sqrt{2} = 260 \text{ V} \quad (4.1)$$

$$V_{in(\max)} = 1.2 \times 230 \times \sqrt{2} = 390 \text{ V} \quad (4.2)$$

The downstream DC-DC converter in the above figure has a line regulation range from 260 V to 390 V. It is interesting to observe that these small electronic equipment would work equally well when connected to a DC power source [4.1] of any polarity, provided the output voltage of this DC source is between 260 V and 390 V. The input bridge

rectifier makes it practical for the equipment to work with DC input of any polarity. The passive power factor correction choke would have no function while operating with DC. Operation with DC naturally results in no harmonic currents at the input. Thus we can conclude that most small electronic equipment would work equally well with a DC voltage of about 390 V.

The common power factor correction scheme proposed in **Paper B** exploits this fact. It proposes to operate all small electronic equipment from a common central DC network or bus. With no limitation to the polarity of the input DC that may be connected to these equipment, it is practical to connect without any limitation as many devices as the DC source could support. The power rating for each device and the number of devices that the DC source would need to support will decide the total power rating of the DC source. The source of power for this DC source could be batteries or another AC-DC converter that generates harmonics, unless the common converter has an active power factor correction front-end at the input.

As shown in **Fig. 4.2**, a common active PFC circuit could be used for this DC source. The figure shows the simplified block diagram of the proposed scheme where thirty small electronic equipment work together. Using the same margins as discussed before, the voltage in the low voltage DC system could be between 260 V and 390 V.

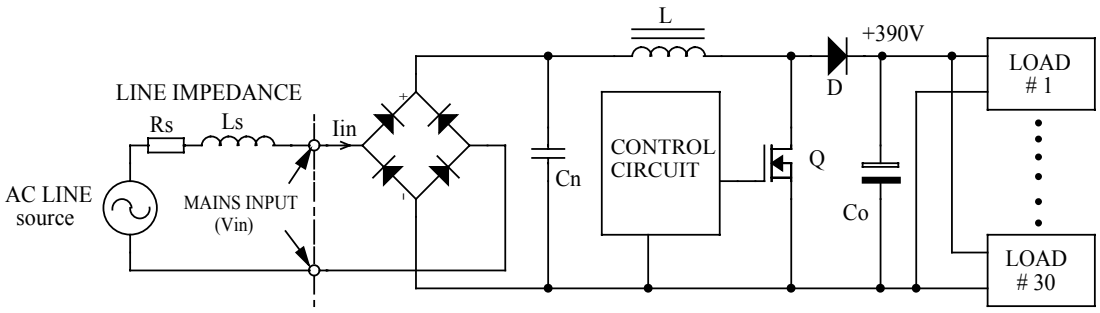

Fig. 4.2. The Common active PFC circuit scheme.

Thus, we have a central common power factor correction scheme that runs thirty computer systems without generating any significant harmonic currents at unity power factor. Other advantages of having a common central power factor correction scheme is higher reliability, significant lower cost and an in-built uninterrupted power supply (UPS) with automatic universal worldwide operation of all loads connected to it. **Paper B** discusses these issues and the benefits of this scheme.

Chapter 5

Power Electronics Considerations

As described earlier, a variety of PFC circuit topologies [5.1] can be used which include the boost converter and the buck converter. Though soft switched Zero-Voltage-Transition (ZVT) techniques [5.2, 5.3] can be used for switching all the above topologies, the hard switched boost converter PFC circuit [5.4] is more popular due to its simplicity and ability to achieve a low distortion input current waveform. For reasons explained in **Section. 3.4.4.2**, the Continuous Conduction Mode (CCM) and Critical Conduction Mode (CRM) PFC circuit topologies are the most popular. However, both have their advantages and disadvantages. In the following section, the CCM boost converter is explained in detail. After this, the CRM and CCM PFC converters are compared.

As with all switch mode converter topologies, the only way to reduce size, improve power density and cost is to increase the switching frequency. However increasing the switching frequency brings along with it a set of well known problems that include increased EMI and losses. Similar problems also apply to the CCM PFC converter. Thus design optimization is a management of tradeoffs. For example, increasing MOSFET switching speed reduces switching losses but increases EMI while using a Silicon Carbide Schottky diode for the boost rectifier helps to reduce MOSFET turn-on losses but increases costs. Similarly, reducing the boost inductor ripple current improves efficiency and reduces EMI but increases the inductor size and cost. Again, increasing the total number of turns on the boost inductor reduces the inductor ripple current but increases EMI due to the increase in inter-winding capacitance of the overlapping turns. Thus an improvement in one area affects the performance of another. In this thesis, each of the components of a CCM PFC converter is investigated in detail and methods for optimization proposed.

5.1 The CCM Boost Converter

Since the remaining part of the work is now based on a CCM PFC circuit, a detailed discussion on the boost converter is presented below.

A CCM boost converter schematic is shown in the **Fig. 5.1a**. The equivalent circuit of the converter when the MOSFET turns on is shown in **Fig. 5.1b**, while **Fig. 5.1c** shows the condition when the MOSFET has turned off.

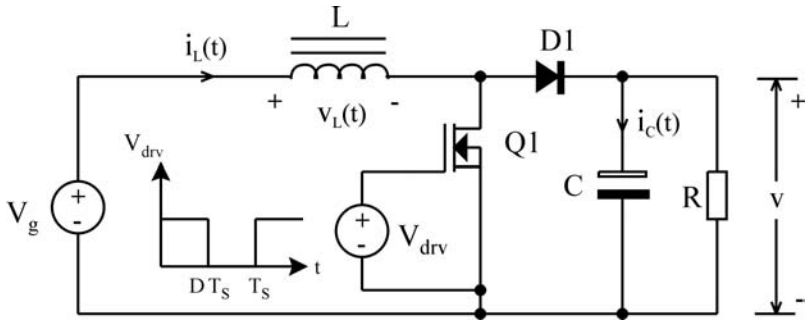

Fig. 5.1a Schematic of a CCM boost converter.

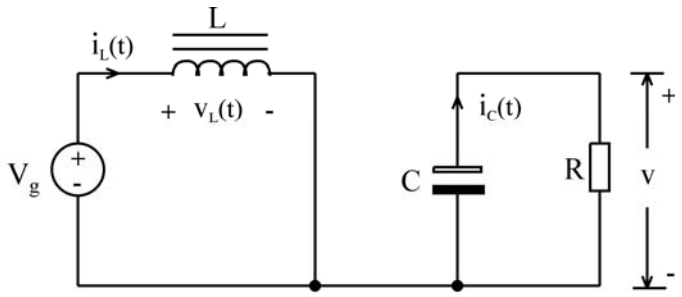

Fig. 5.1b Equivalent circuit of the CCM boost converter when Q1 turns ON.

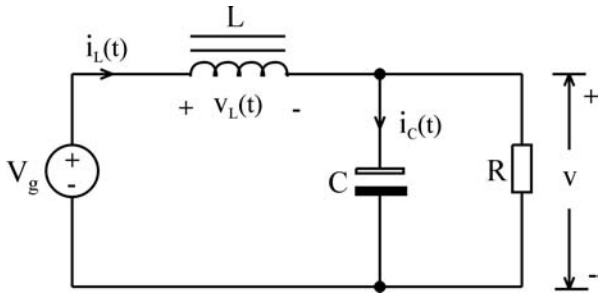

Fig. 5.1c Equivalent circuit of the CCM Boost converter when Q1 turns OFF.

When the MOSFET Q1 turns on, one end of the inductor is connected to the input negative and diode D1 is reverse biased. The load current flows out of the charged output capacitor C.

Thus during this interval, the inductor voltage and capacitor current is,

$$v_L = V_g \tag{5.1}$$

$$i_C = -\frac{v}{R} \approx -\frac{V}{R} \tag{5.2}$$

When the MOSFET turns off, the inductor is connected to the output through the diode D1. Thus during this interval the inductor voltage and capacitor current is,

$$v_L = V_g - v \approx V_g - V \tag{5.3}$$

$$i_C = i_L - \frac{v}{R} \approx I - \frac{V}{R} \tag{5.4}$$

Using linear approximation, we assumed $v \approx V$ and $i_L = I$ in the above equations.

Now, from the above equations, the inductor voltage and capacitor current waveforms are plotted in **Fig. 5.2**. D is the on-time duty cycle of the MOSFET and T_S is the switching period.

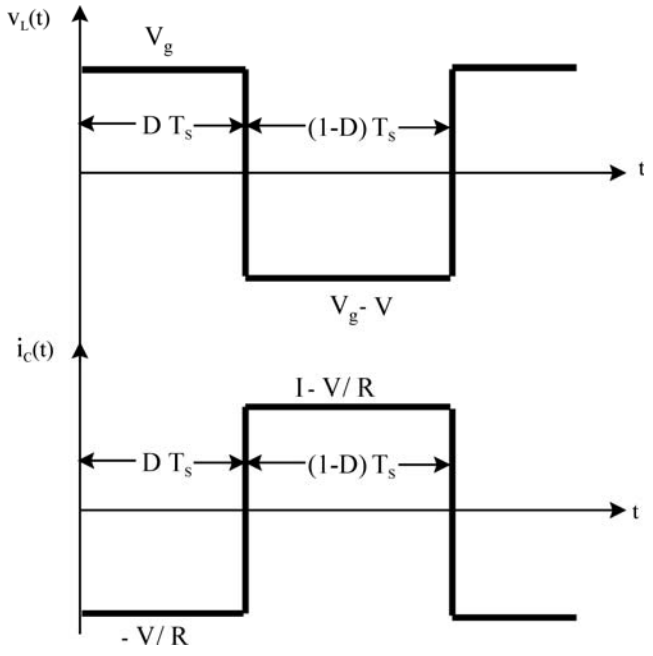

Fig. 5.2 Inductor voltage and capacitor current wave forms.

The total volt-seconds applied to the inductor over one switching period is given by,

$$\int_0^{T_S} v_L(t)dt = (V_g)DT_S + (V_g - V)(1-D)T_S \tag{5.5}$$

Equating this expression to zero and collecting terms, we have

$$V_g(D+1-D) - V(1-D) = 0 \tag{5.6}$$

$$V = \frac{V_g}{(1-D)} \tag{5.7}$$

From the above, it is apparent that the output voltage increases as D increases. However, when component non-idealities are included, there is a limit to the maximum possible output voltage of a boost converter.

The DC component of the inductor current (I) is derived from the fact that the total charge on the output capacitor is always balanced. When the MOSFET turns on, the load current depletes the charge from the output capacitor while the capacitor recharges once the MOSFET turns off.

The net charge in the capacitor is found by integrating the above capacitor current waveform $i_C(t)$, over one switching period we have,

$$\int_0^{T_S} i_C(t)dt = \left(-\frac{V}{R}\right)DT_S + \left(I - \frac{V}{R}\right)(1-D)T_S \tag{5.8}$$

Equating this equation to zero and collecting terms we get,

$$-\frac{V}{R}(D+1-D) + I(1-D) = 0 \tag{5.9}$$

$$I = \frac{V}{(1-D)R} \tag{5.10}$$

Substituting equation (5.7) above, we get

$$I = \frac{V_g}{(1-D)^2 R} \tag{5.11}$$

From the plot of this equation shown in **Fig. 5.3**, it is apparent that the inductor current's DC component increases as the duty cycle increases.

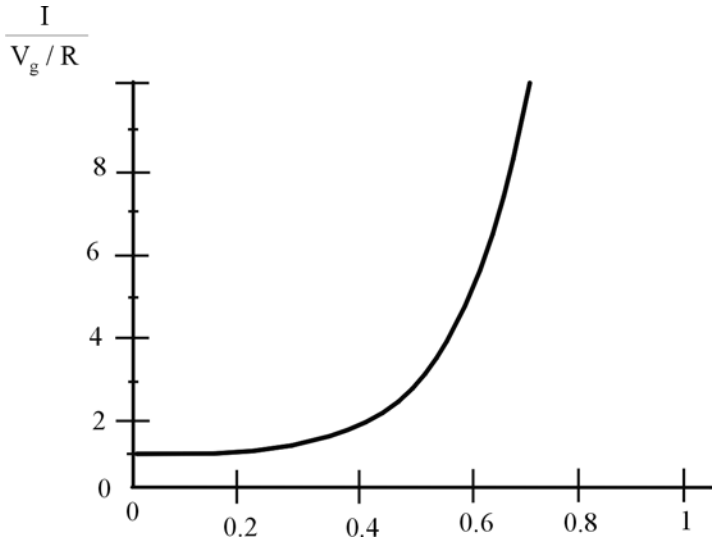

Fig. 5.3 Variation of DC component of Inductor current with Duty cycle.

The inductor current's DC component is greater than the load current since the boost converter's output voltage is greater than the input voltage. The inductor winding resistance and semiconductor voltage drops, through which the inductor current flows, are sources of power loss. Thus, as the inductor current increases with increasing duty cycle, the efficiency also decreases.

Referring to **Fig. 5.1a**, when the MOSFET turns ON, the slope of the inductor current is given by,

$$\frac{di_L(t)}{dt} = \frac{v_L(t)}{L} = \frac{V_g}{L} \tag{5.12}$$

When the MOSFET turns OFF, the inductor current slope is given by,

$$\frac{di_L(t)}{dt} = \frac{v_L(t)}{L} = \frac{V_g - V}{L} \tag{5.13}$$

Fig. 5.4 shows the inductor current waveform with Δi_L representing the total inductor ripple current.

$$\Delta i_L = \frac{V_g}{L} DT_S \tag{5.14}$$

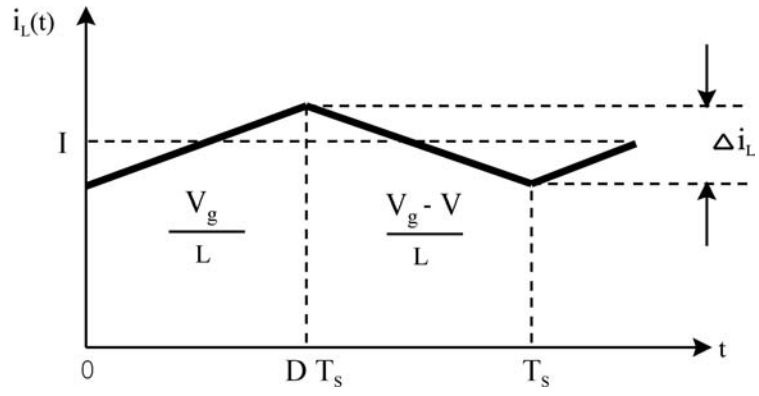

Fig. 5.4 Inductor current wave form.

From the above expression, it is apparent that the inductor ripple current increases with lower inductance. The increase in ripple increases the RMS inductor current and this decreases efficiency and increases conducted emission.

When non-idealities are included in the model of the boost converter shown above in **Fig. 5.1**, the boost converter model can be represented as shown in **Fig. 5.5a** and **Fig. 5.5b**. The inductor winding resistance is represented as R_L, the MOSFET on-resistance as R_{on}, the boost diode's forward drop as V_D and its resistance as R_D in these models.

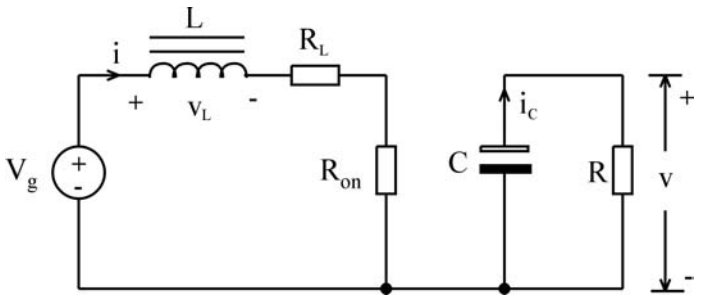

Fig. 5.5a Equivalent circuit of the CCM boost converter when Q1 turns ON.

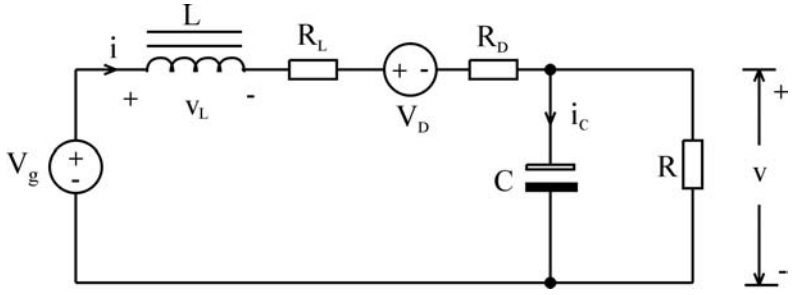

Fig. 5.5b Equivalent circuit of the CCM boost converter when Q1 turns OFF.

Thus when the MOSFET turns-on, from **Fig. 5.5a** we have,

$$v_L(t) = V_g - iR_L - iR_{on} \approx V_g - IR_L - IR_{on} \tag{5.15}$$

$$i_C(t) = -\frac{v}{R} \approx -\frac{V}{R} \tag{5.16}$$

When the MOSFET turns off, the inductor current forward biases the diode. The circuit model is represented as in **Fig. 5.5b**. Approximating again the inductor voltage and capacitor current by their DC components, we have the inductor voltage and capacitor current as,

$$v_L(t) = V_g - iR_L - V_D - iR_D - v \approx V_g - IR_L - V_D - IR_D - V \tag{5.17}$$

$$i_C(t) = i - \frac{v}{R} \approx I - \frac{V}{R} \tag{5.18}$$

Inductor voltage and capacitor current waveforms are shown in **Fig. 5.6**.

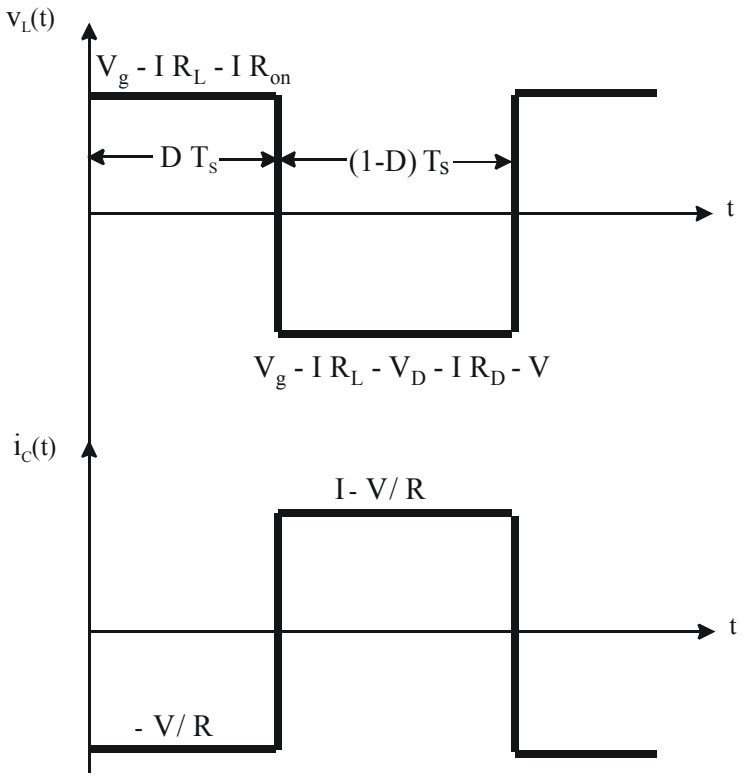

Fig. 5.6 Inductor voltage and capacitor current wave forms.

5.2 MOSFET Switching Speed Considerations and EMI

As fast switching speeds result in high frequency Fourier components, the slope of the switching waveform is a key parameter that should be considered for a good EMC design. Thus, an acceptable compromise between switching speed, power losses and EMI is necessary. Therefore, a first step is to understand how the slopes of the drain current relate to the parameters of the driving circuit design.

Fig. 5.7 shows a typical circuit driving a MOSFET. The MOSFET's input capacitance C_{iss}, the Miller capacitance C_{Miller}, the output capacitance C_o, the gate current I_g, the applied drain voltage V_{dd}, the load R_L, the load current I_{load} and gate voltage V_g is clearly shown in this circuit. To minimize the turn-off switching losses the turn-off gate resistance (R_{goff}) is set to minimum by the anti-parallel diode D across the turn-on gate resistance $(R_{gon} = R_g)$. V_{Miller} is the voltage across the Miller capacitance C_{Miller} during the turn-on or turn-off transition period of the MOSFET. **Fig. 5.8** shows the MOSFET drain voltage and current waveforms with respect to the corresponding gate voltage for various turn-on switching intervals. It can be observed that once the gate voltage crosses the MOSFET gate turn-on threshold voltage (V_{th}) at interval t_1, the MOSFET begins to turn-on and the input capacitance C_{iss} charges upto the interval t_2. Between the interval t_2 to t_3, the Miller capacitance C_{Miller} charges and the time taken to charge this capacitance is the measure of the drain voltage fall time. Thus, the faster this Miller capacitance C_{Miller} charges, the shorter the time the drain voltage will take to fall, resulting in reduced switching losses and improved efficiency. Thus, charging the Miller capacitance faster by using a lower value of R_g can reduce the turn-on time and thus improve efficiency.

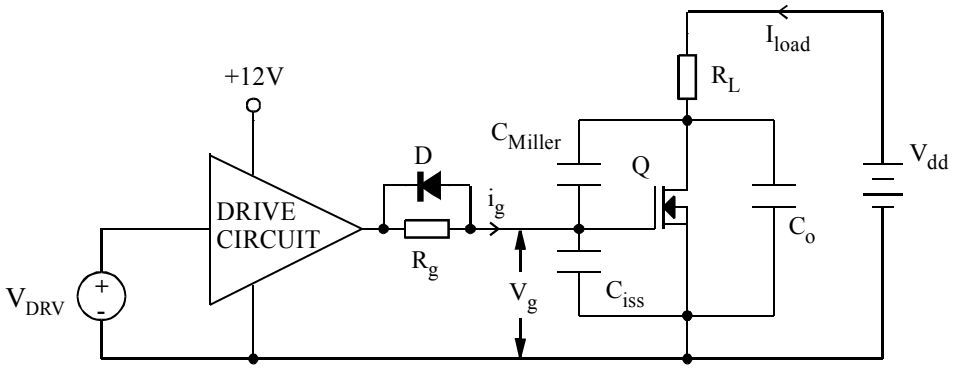

Fig. 5.7 Typical circuit configuration used for driving a MOSFET.

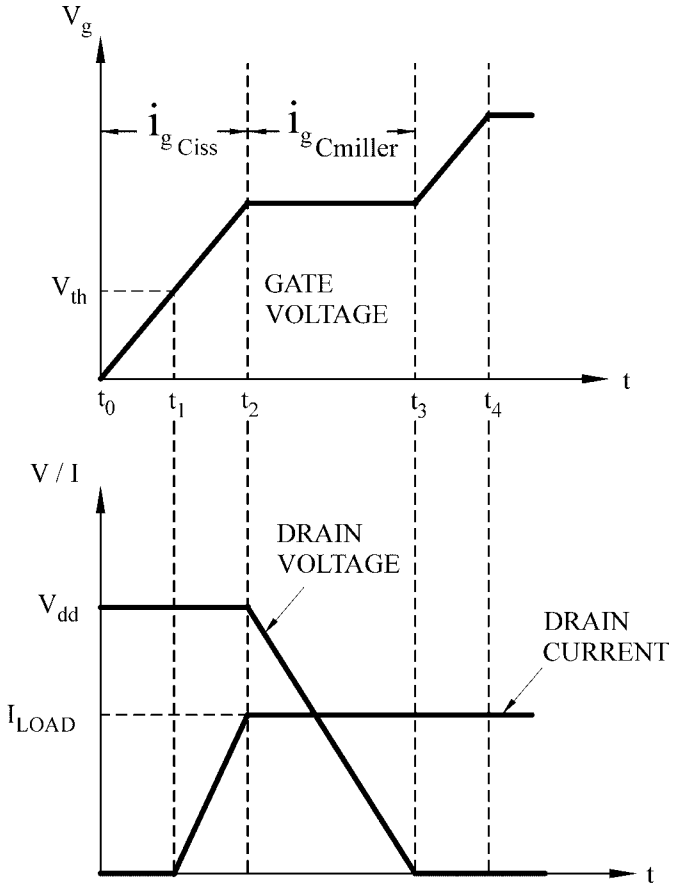

Fig. 5.8 MOSFET gate voltage waveforms with respect to corresponding drain voltage and current for various turn-on-switching intervals.

When power MOSFETs are driven by voltage pulses, the instantaneous drain current slope $\left[\frac{di_d}{dt}\right]$ is related to the rate of the gate charge supplied or removed by the driver circuit and is given by (5.19) and (5.20), which are valid at the switching on and off time intervals respectively.

$$\left[\frac{di_d}{dt}\right]_{on} \approx g_m \frac{V_{dd} - V_{th} - \frac{I_{load}}{2g_m}}{C_{iss} R_{gon}} \tag{5.19}$$

$$\left[\frac{di_d}{dt}\right]_{off} \approx g_m \frac{-V_d - V_{th} - \frac{I_{load}}{2g_m}}{C_{iss} R_{goff}} \tag{5.20}$$

The corresponding gate currents are given by (5.21) and (5.22).

$$i_{gon} = \frac{V_{dd} - V_{Miller}}{R_{gon}} \tag{5.21}$$

$$i_{goff} = \frac{-V_d - V_{Miller}}{R_{goff}} \tag{5.22}$$

According to (5.19) and (5.20), di_d/dt can be controlled by the gate resistance R_g Changing the value of R_g has two effects: a high R_g increases switching losses while a low value R_g generates high EMI. Operation of the *"turn-on"* sequence is described by means of **Fig. 5.9**. In particular, the first plot shows the turn-on waveform for a high value R_g, while the next plot shows the turn-on waveforms for a low value R_g.

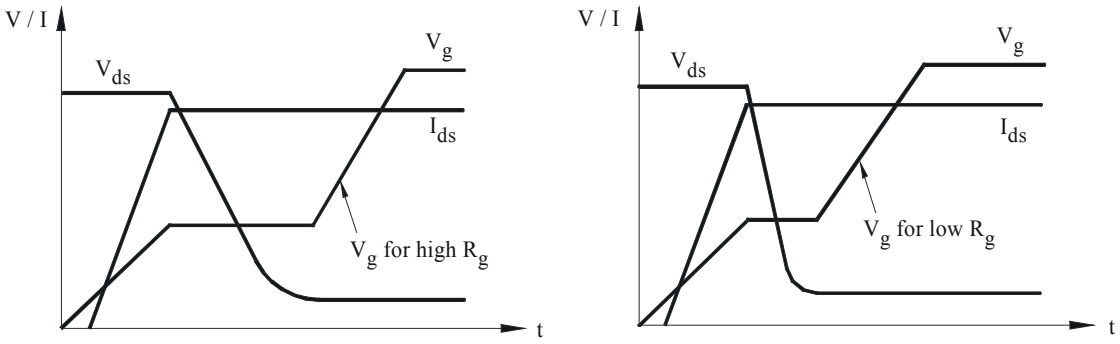

Fig. 5.9. Turn-on behavior for different gate resistance values.

The horizontal section of the gate drive signal V_g is due to the Miller effect. Compared to a high resistance value, a low value R_g charges the gate capacitance faster, thus speeding up the collector voltage fall and resulting in lower switching losses.

An analytical study of the emission problem is possible by investigating the frequency content of the instantaneous drain current i_d and computing its Fourier expansion coefficients. The waveform of the drain current can be represented as a periodic trapezoidal pulse train and its parameters, according to **Fig. 5.10**, are defined as follows:

A = Amplitude; t_r = Rise time; t_f = fall time and τ = Width.

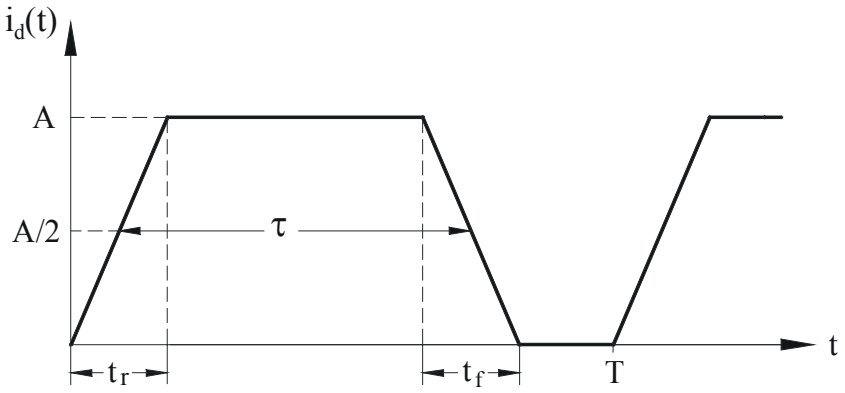

Fig.5.10. Periodic trapezoidal pulse train representing instantaneous drain current i_d.

For the aim of this study, the rise and fall time are respectively considered as the time required for the signal transition from zero to A and from A to zero [5.5]. The expansion coefficients for such a waveform are:

$$c_n = -j\frac{1}{2\pi n}e^{-jn\pi f_0(\tau+t_{on})}\times\left\{\begin{array}{l}\left[\frac{di_d}{dt}\right]_{on}\frac{\sin\left(n\pi f_0 t_{on}\right)}{n\pi f_0}e^{jn\pi f_0\tau}\\ -\left[\frac{di_d}{dt}\right]_{off}\frac{\sin\left(n\pi f_0 t_{off}\right)}{n\pi f_0}e^{-jn\pi f_0\tau}\end{array}\right\} \tag{5.23}$$

Where:

$$\left[\frac{di_d}{dt}\right]_{on}=\frac{A}{t_{on}} \tag{5.24}$$

$$\left[\frac{di_d}{dt}\right]_{off}=\frac{A}{t_{off}} \tag{5.25}$$

If we assume:

$$g_m\frac{V_{dd}-V_{th}-\frac{I_{load}}{2g_m}}{C_{iss}}=K_{on} \tag{5.26}$$

$$g_m\frac{-V_d-V_{th}-\frac{I_{load}}{2g_m}}{C_{iss}}=K_{off} \tag{5.27}$$

by substituting in (5.23), (5.19) and (5.20) modified through (5.26) and (5.27), the following expression coefficients are obtained.

$$c_n = -j\frac{1}{2\pi n}e^{jn\pi f_0(\tau+t_{on})}\times\left[\begin{array}{l}\frac{K_{on}}{R_{gon}}\frac{\sin(n\pi f_0 t_{on})}{n\pi f_0}e^{jn\pi f_0\tau}\\ -\frac{K_{off}}{R_{goff}}\frac{\sin(n\pi f_0 t_{off})}{n\pi f_0}e^{-jn\pi f_0\tau}\end{array}\right] \tag{5.28}$$

Equation (5.28) shows how R_g influences the switching harmonics and hence the EMI.

5.3 Comparing the CCM and CRM PFC converter

Typical inductor current waveforms shown below are only for supporting the explanation of the topology-specific characteristics. In reality, the switching frequency is much higher than the line-frequency and the input current waveform is dependent also on the type of control that is used. With reference to the typical inductor current in a CRM and CCM PFC converter, the main differences are listed below.

Critical Conduction Mode (CRM) PFC Converter.

With respect to a CRM PFC converter's PWM signal, its typical inductor current is shown in **Fig. 5.11**. Analyzing the inductor current in detail, the following advantages and disadvantages of this topology become apparent.

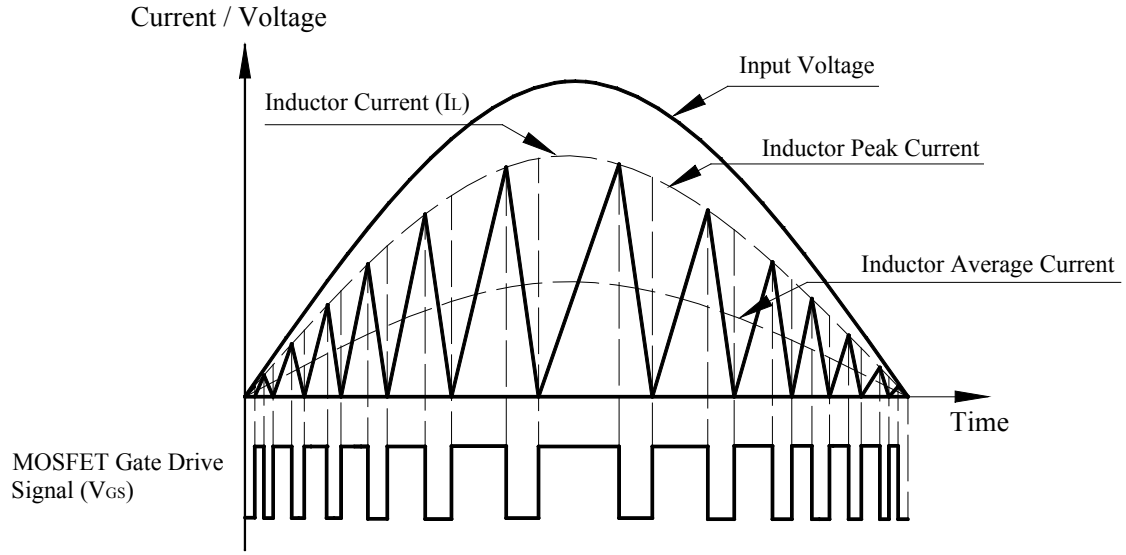

Fig. 5.11. Typical CRM boost inductor current waveform with respect to the input line voltage and switching MOSFET's gate drive signal.

Advantages:

- No losses due to boost-diode reverse-recovery time because the inductor current falls to zero long before the switch is turned on. Though the EMI contributed by the boost diode recovery is less, the large inductor ripple current increases conducted EMI.
- Compared to CCM operation, control is simpler because the switch current is compared to a reference signal (output of a multiplier) directly. This control method has the advantage of simple implementation and still provides very good input current waveform.
- Requires a smaller inductance when compared to the CCM converter.

Disadvantages:

- Variable switching frequency operation. The lowest frequency is at the voltage peak and the highest near the input voltage zero crossing.
- High switching losses due to the high peak-to-average ratio of the inductor current.
- High conduction losses due to high RMS current compared with average line current.
- High differential mode conducted emissions due to high AC ripple content in the input current.
- Higher copper and core losses in the boost inductor due to high RMS current and large AC current components.

Continuous Conduction Mode (CCM) PFC Converter.

With respect to a CCM PFC converter's PWM signal, its typical inductor current is shown in **Fig. 5.12**. Analyzing the inductor current in detail, the following advantages and disadvantages of this topology become apparent.

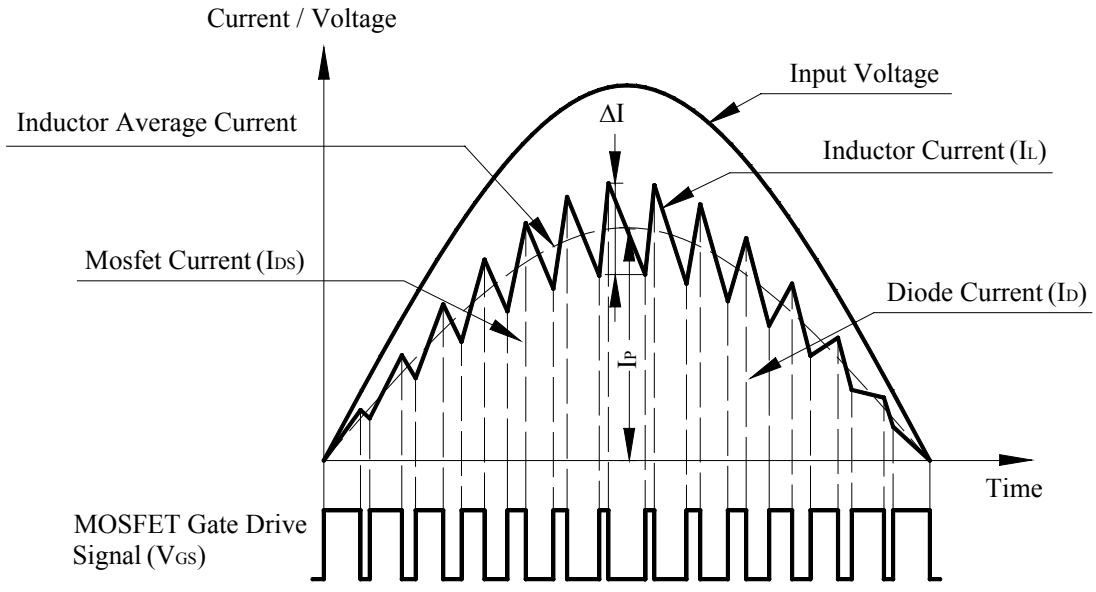

Fig. 5.12. Typical CCM boost inductor current waveform with respect to the input line voltage and switching MOSFET's gate drive signal.

Advantages:

- Lower conduction losses due to lower RMS current through the switch.
- Reduced differential mode conducted emissions due to lower AC ripple content in the input current. This eases the design of the input EMI filter.
- Lower copper and core losses in the boost inductor due to lower RMS current and reduced AC current components.
- Excellent input power factor and low current distortion because a high-gain current control loop forces the input current to be proportional to the line voltage at all times.
- Continuous mode inductor current can easily transition into discontinuous mode under light load conditions without any problem. Line current still tracks line voltage accurately.
- Can compensate for line voltage changes automatically by line voltage feed forward control.

Disadvantages:

- The boost switch incurs high turn-on losses due to forced reverse-recovery of the boost diode.
- The boost inductor is slightly larger for continuous mode operation, because only a portion of stored energy is transferred to the output on each switching cycle.

Thus, the main differences between the CRM and CCM topologies relate to the amplitude of the inductor current and its ripple profile. The current profile effects two parameters - power losses in the power stage components and filtering requirements. However, with the availability of extremely fast diodes today, including the zero recovery time Silicon Carbide diode, the concerns relating to boost rectifier recovery losses in CCM PFC converters are controllable. Thus, with the CCM converter being the preferred topology, the work presented here concerns the CCM PFC converter only. No work was done on the various control schemes of these converters.

Applications today demand significantly increased power densities of above 18 W / cubic inch. Higher MOSFET switching speed, ability of the boost diode to switch off as quickly as possible, reduction in losses in the MOSFET, reduced EMI and proper design of the boost inductor is the key to improving performance of any CCM PFC converter. This research work concerns the above mentioned Power Electronics issues and these are discussed in detail in the following sections.

5.4 Continuous Conduction Mode Power Factor Correction

From the earlier discussions it is apparent that the CCM PFC converter offers the best overall advantages and is, therefore, the most popular. A CCM boost regulator is an excellent choice for the power stage of an active power factor corrector because the input current is continuous and this produces the lowest level of conducted noise and the best input current waveform. The disadvantages of the boost regulator is the high output voltage generated, the converter's inability to provide input /output isolation and the requirement of the output voltage to be greater than the highest expected peak input voltage.

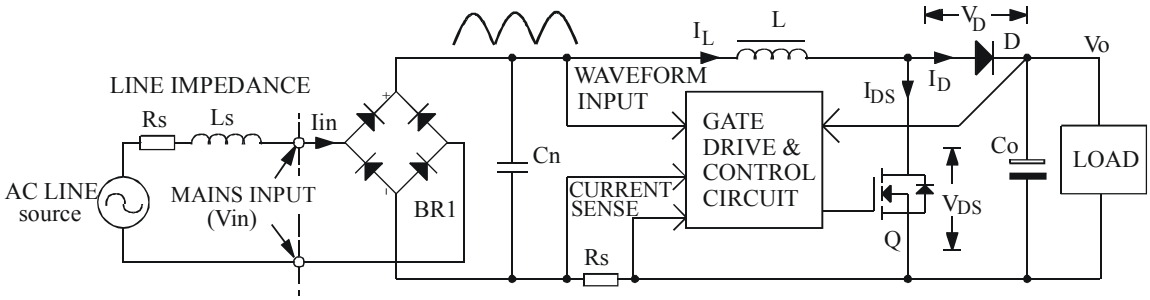

Fig. 5.13 Block diagram of a continuous conduction mode power factor correction circuit.

A system based on the continuous conduction mode (CCM) boost converter is shown in **Fig. 5.13**. The diode bridge rectifies the AC input voltage. The large filter capacitor (*Co*) that would normally be associated with conventional rectification has been moved ahead of the inductor to the output of the boost converter. The capacitor (*Cn*) that follows the input diode bridge, is always small in value and used only for noise control.

Except during very light load conditions, the inductor current never reaches zero during one switching cycle and energy is always stored in the inductor for this operating mode. The *volt seconds* applied to the inductor must be balanced throughout the line-cycle by continuously changing the duty-cycle of the converter using an appropriate control method. Ideally, the boost converter can produce any conversion ratio between one and infinity. Thus, for an universal AC input voltage of 90 V to 264 V, in order to achieve PFC, the converter should be so designed that the output voltage *Vo* is always greater than the highest peak of the input line voltage. Assuming a maximum line voltage of 264 V RMS and

allowing at least a 5% margin, the nominal *Vo* will be 400 V. The relative high output voltage is actually an advantage for the downstream converter since this results in lower current levels in the down stream converter's primary circuit. Another characteristic of the boost converter is that it can produce input currents with very low THD with better transistor utilization than other approaches.

The control of a CCM PFC converter is provided by monitoring the input full wave rectified line voltage wave shape, the inductor current, the magnitude of the input voltage average and the output voltage. These three input signals are combined to modulate the average input current waveform in accordance with the rectified line voltage, while regulating the output voltage for line and load variations. Thus the boost regulator's input current is forced to be proportional to the input voltage waveform by modulating the regulator's MOSFET drive, for achieving power factor correction. To control the input current, either peak current mode control or average current mode control may be used.

Peak current mode control has a low gain and a wide bandwidth current loop. This generally makes it unsuitable for a high performance power factor corrector, since there is a significant error between the programming signal and the current. Thus, a better control method is the average current mode control, where the average of the inductor current, instead of the peak, is compared to the current program level. This offers better noise rejection and stability, when compared to peak current mode control. Because the average of the input current is controlled, a line current waveform of very good quality can be obtained. Consequently, average current mode control is widely used in PFC applications though its implementation is somewhat more complicated when compared with that of the peak current mode control.

An active power factor corrector must control both the input current and the output voltage. The rectified line voltage programs the current loop so that the input to the converter will appear to be resistive. Changing the average amplitude of the current programming signal controls the output voltage. An analog multiplier creates the current programming signal by multiplying a sample of the rectified line voltage with the output of the voltage error amplifier so that the current programming signal has the shape of the input voltage and an average amplitude that could control the output voltage.

Fig. 5.14 shows the basic circuit diagram of a CCM PFC circuit. Among the many possible control methods of a CCM PFC circuit, the one

described here has been used by the industry for a long time. The heart of the circuit is the current modulator. The modulator consists of a linear multiplier, a current amplifier and a Pulse Width Modulation (PWM) comparator.

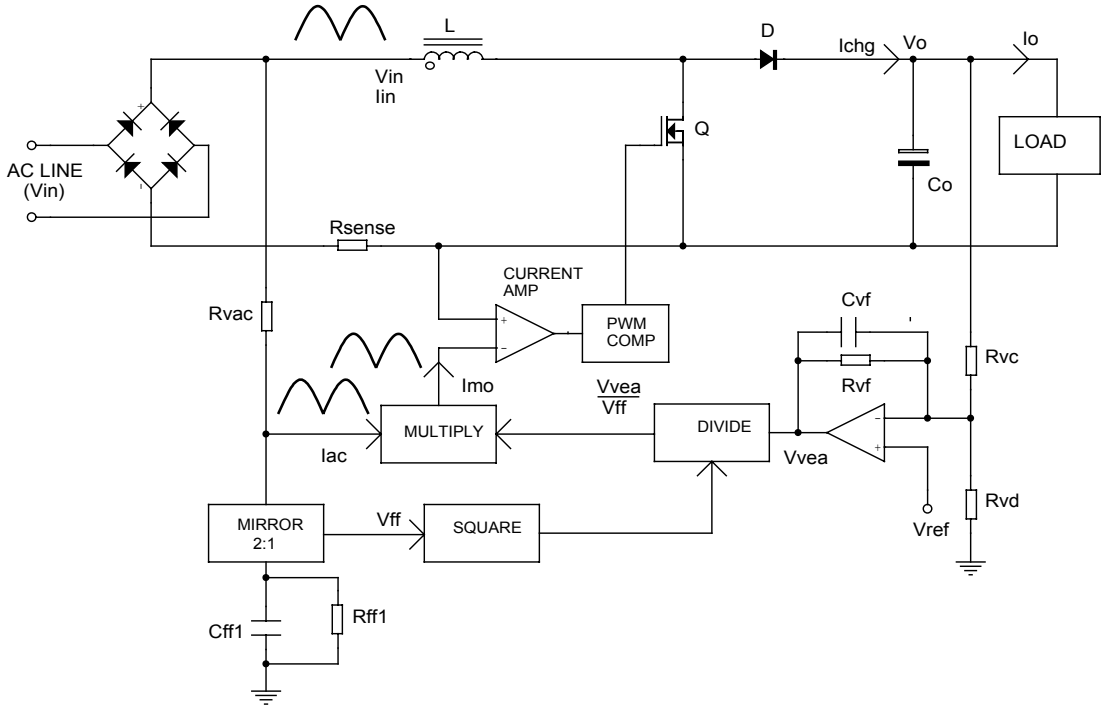

Fig. 5.14. Basic block circuit diagram of a CCM PFC circuit.

These three functional blocks together controls the circuit to force the input current to be sinusoidal. The output of the multiplier is a current programming signal and is named I_{mo}. The multiplier input from the rectified line voltage is a current input and is shown as I_{ac}. The voltage control loop comprises of a squarer and a divider and its output is the other input of the multiplier. R_{vc} and R_{vd} provide output voltage feedback. The voltage error amplifier's output *(V_{vea})* is divided by the square of the AC input voltage average *(V_{ff})* and the result is multiplied by a current signal *(I_{ac})* that represents the rectified input voltage wave-shape. R_{vac} generates this current signal *(I_{ac})* while the AC input voltage average signal *(V_{ff})* is generated by filtering a mirror of this current signal *(I_{ac})*, by R_{ff1} and C_{ff1}. This extra circuitry keeps the gain of the voltage loop constant. The output of the voltage error amplifier changes slowly compared to the line frequency, since the bandwidth of this amplifier is set low by its feedback components R_{vf} and C_{vf}.

The current programming signal I_{mo} is compared with the input current signal across R_{sense} and the current amplifier output accordingly controls the PWM comparator to match the rectified line voltage as closely as possible. This maximizes the input power factor. If the voltage loop

bandwidth was large, it would modulate the input current to keep the output voltage constant and this would distort the input current. Therefore, the voltage loop bandwidth must be less than the input line frequency. But to have a fast output voltage transient response, the voltage loop bandwidth must be made as large as possible. The squarer and divider circuits keeps the loop gain constant so the bandwidth can be as close as possible to the line frequency. This minimizes the transient response, of the output voltage and this is especially important for PFC circuits operating with wide input voltage ranges.

The output of the voltage error amplifier actually controls the power delivered to the load. Thus, if the output of the voltage error amplifier is constant and the input voltage is doubled, then the programming signal will also double but it will also be divided by the square of the feed forward voltage *(V_{ff})*. This will result in the input current being reduced to half its original value. Thus, twice the input voltage multiplied by half the input current results in the same input power as before. The output of the voltage error amplifier then controls the input power level of the power factor corrector. This can also be used to limit the maximum power that the circuit can draw from the power line. If the output of the voltage error amplifier is clamped at some value that corresponds to some maximum power level, then the active power factor corrector will not draw more than that amount of power from the line as long as the input voltage is within its range.

5.5 Optimizing Performance of CCM PFC Circuits

As discussed earlier, it is advantageous if PFC circuits operate in the continuous mode for applications where the output power is higher than 200W. With applications today demanding significantly higher power densities, there is a constant need for higher efficiency and cost optimization, besides an increase in the switching frequency of the converter. The main sources of losses in a CCM PFC converter are the boost rectifier diode, the switching transistor (MOSFET), the boost inductor and the input bridge rectifier. The greatest losses are the switching losses in the MOSFET caused by the boost diode while the inductor contributes to the total losses indirectly.

Switching losses in the MOSFET can be reduced by improving the switching speed of the MOSFET but this makes the boost diode's recovery characteristic snappier leading to excessive ringing and EMI. It is, therefore, natural to expect that this higher associated EMI will require

additional EMI filtering and this could offset the achieved improvements in efficiency and size. With conduction losses being easily reduced by using a lower drop device, the effect of faster switching speeds on EMI and performance of these PFC circuits becomes increasingly important.
The work presented here concerns the causes of these losses and the control of EMI in the continuous mode boost PFC circuits. With reference to the description of the various the power electronic issues of the CCM boost converter presented in section 5.1 and 5.2, the effect of these losses and EMI on the cost and performance of these PFC circuits are studied in this work. Based on these studies and by making measurements on a practical 1200 W PFC circuit prototype, specific design strategies for mitigating these problems leading to optimizing cost and performance of these PFC circuits are proposed.

5.5.1 Optimizing Selection of Power Devices

Understanding the losses in the active components of a CCM PFC circuit explains the benefits of using a very fast boost diode with soft recovery and a fast switching MOSFET with low conduction losses. **Paper C** and **Paper D** discuss in detail how these losses are influenced by the characteristics of these active components. The MOSFET conduction loss is the product of MOSFET RMS current (I_{Qrms}) squared by the MOSFET's on-time drain to source resistance ($R_{DS(ON)}$) at 100°C. Since MOSFET conduction losses depend only on the MOSFET $R_{DS(ON)}$ and are not influenced by the reverse recovery characteristics of the boost diode , the more expensive new generation low $R_{DS(ON)}$ MOSFET types can significantly reduce MOSFET conduction losses. New generation 600 V rated MOSFETs have $R_{DS(ON)}$ as low as 0.006 Ω. Moreover since higher MOSFET switching speed is the key to improving efficiency, increasing switching speed reduces switching losses. Thus switching losses can be reduced by appropriate gate drive circuits that switches the MOSFET faster and the new generation MOSFETS help achieve this as they have low gate charge characteristics.

Switching energy losses occur when the boost inductor current is commutated between the MOSFET and the boost diode. MOSFET switching losses increase with switching frequency, slower switching speed and longer recovery time of the boost diode. Thus using a faster boost diode reduces the MOSFET's turn-on power losses since the switching energy losses caused by the diode's reverse recovery time characteristics, during the commutation of current from the boost diode to the MOSFET, is reduced. PFC Specific ultra-fast diodes and Silicon Carbide Schottky diodes are examples of such diodes with fast or

negligible recovery time. The diode's reverse recovery characteristics describe how it transits from the forward conducting state to the reverse voltage blocking state.

The power losses in the boost diode consist of conduction and switching losses. The switching losses are negligible compared to the conduction losses, if a suitable ultra fast recovery diode is chosen. This is because when the diode is recovering, the voltage drop across it is negligible.

5.5.2 Optimizing Inductor Design

For a given power, choosing a higher inductor ripple current reduces the size of the inductor but this increases core losses in addition to low AC and DC copper losses. A lower ripple current design increases the size of the inductor but makes the inductor design less demanding. Thus, the boost inductor design is the management of trade-offs. A savings in one area can easily make things worse elsewhere with an overall change in EMI or efficiency. So choosing the optimum trade-off is critical for minimizing overall cost and very often, determining the cost trade-offs is even more difficult.

The major losses in the inductor are due to effects of core loss, DC resistance, proximity effect and skin effect. Using low loss materials like Ferrites or Molypermalloy Powder or Ferrous Alloy Powder or Iron based Amorphous cores reduces the core losses. The DC losses are lessened by reducing the coil's DC resistance while the AC losses can be reduced using multiple wires in parallel and reducing the number of winding layers. The AC losses and the core losses in the inductor are directly dependent on the magnitude of the inductor's ripple current. Moreover, for a fixed frequency ripple current magnitude and a given magnetic material, the core losses would depend only on the core weight. Thus smaller core sizes can carry a higher ripple current while larger core sizes will require lower ripple current designs.

It may also appear that though a higher inductor ripple current will increase EMI, this can be easily attenuated by a few extra turns in the line filter. However, for higher power converters, attenuating additional EMI by a few extra turns in the line filter is often difficult, as the line filter's wire conductor diameter is thicker and often increasing turns will require a larger core size. Based on many experimental results, **Paper E** provides a better insight to these issues.

5.5.3 Optimizing EMC Issues

The high-frequency ripple of the input current of switching converters generates differential-mode and common-mode conducted EMI. Typically, the differential-mode EMI is dominant below 1.8 MHz, while the common-mode EMI is dominant above 2 MHz. For common mode EMI attenuation, a common mode EMI filter is necessary. The high-frequency ripple of the input current is the main cause for the differential-mode EMI and a separate additional one-stage differential mode LC filter is often required to attenuate this. Moreover, unstable operation may occur due to the interaction between the EMI filter and the power stage [5.6].

Radiated EMI is another concern. Higher MOSFET switching speeds are required for improving efficiency, increasing switching frequency and reduction in switching losses. However, the faster the MOSFET turns-on, the snappier the boost diode's recovery characteristic becomes. A point is reached where the diode snappiness causes excessive ringing leading to increased radiated EMI.

PCB layout is also very critical. Care should be taken to ensure that all return paths of the switching currents are preferably balanced and that they form minimum loop areas. Track inductance should also be minimized.

Winding direction of turns on the boost inductor also plays a crucial role in reducing EMI. Winding a section from left to right, or vice versa, or starting the winding clockwise or counterclockwise around the core - all have an effect on EMI, and so must be considered in the design. The best scheme is to adopt a winding sequence which will minimize the radiated fields and the inter winding capacitance. Thus the large effect of radiated fields from the boost inductor on the conducted EMI performance of a hard-switched CCM boost PFC converter is a concern.

Based on many experimental results, **Paper F, Paper G, Paper H** and **Paper I** provide a better insight to these issues described above.

Chapter 6

A 1200 W Active PFC Prototype

To develop a better understanding about the effect of different switching devices on the losses and EMI performance of a continuous boost PFC circuit, a 1200 W prototype boost PFC circuit model was built. To meet the requirements of EN 55022 conducted emission levels and having a smaller input EMI filter, any switching frequency below 150 kHz was preferred. Thus for all the different measurements made, the switching frequency was always kept to about 100 kHz or lower and the boost inductor ripple current was limited to less than 25% of its maximum peak value to minimize its AC losses.

SPECIFICATIONS OF 1200W PFC CIRCUIT

GENERAL	
Product	Universal input 1200 W active PFC circuit.
Operating ambient	Full operation **:** -10°C to +40°C
Cooling	Natural convection cooling.
INPUT	
Input range	90 V to 264 V AC/45 Hz to 65 Hz (Nominal: 110 V/220 V AC).
Hold-up time	Better than 10 mS at 110 V AC input, measured at full load.
Input power factor	Power factor better than 0.9 and as per EN 61000-3-2, Class D limits.
Input Circuit	Three wire system with safety earth.
Leakage Current	2.5 mA AC RMS (Max.).
Inrush current	< 40 Amps for less than 5 cycles at 230 V AC input and full load with ON / OFF interval of 1 minute.
Efficiency	Typically 95% at full load, 230 V input and nominal output.
EMI / EMC	
Conducted & Radiated Emission	According EN 55022 Class B for conducted emission and radiated emissions.
Immunity	IMMUNITY FOR AC INPUT LINES a) Fast transients to ± 1 kV and as per EN 61000-4-4. b) Surges to ± 2kV (common mode) and ± 1kV (differential mode), and as per EN 61000-4-5.
OUTPUT	
Nominal Output	Nominal value of +385 V DC with ripple less than 5 V pk-pk.
Max. Load Current	About 3.2 Amps.
Voltage Regulation	Output to be within 385 V ± 5 V at specified ambient, specified input line and specified output current conditions.

The PFC controller was a UCC3817N [6.1] from Texas Instruments. The prototype was so built that changing the switching frequency or the boost inductor or the boost diode for making different measurements was always easily possible. The brief specification of the converter is given above.

The converter was designed to operate in the CCM of operation for the whole line period and range. The prototype was built on a two-layer printed circuit board (PCB) and tested with three different diodes: the SDT12S60 [6.2] SiC Schottky diode from Infineon Technologies, the STTH806TTI [6.3] single package series connected diode from ST Microelectronics and the 15ETX06 [6.4] PFC specific diode from International Rectifier. The PCB layout was developed with great care, so as to minimize the generation of EMI. Overall converter performance was tested to ensure that the design meets the required specifications.

6.1 Converter Block Schematics

The converter design is described in detail with reference to the detailed block schematics given in **Fig. 6.1**. The block schematic represents functionality and does not represent a circuit diagram.

Input AC is connected to CN1 and is EMI filtered. Inrush current limiting is provided by R1. The input AC is rectified by BR1 and filtered by C1 to generate a full wave rectified sinusoidal waveform across it. This capacitance is mainly for noise filtering and therefore its value is not too large to distort the input wave shape information even at low output power and high line input conditions.

The unregulated rectified voltage across C1 is hard switched down stream by a boost converter, which regulates the output voltage across C2 to 385 V for input line changes between 90 V-264 V AC. The output EMI filter is mainly for suppressing radiated emission and connects the final output across CN2. The boost converter operates by switching the boost inductor L1-A through Q1 and rectifying the boosted flyback voltage through D1 and filtering by C2. R14 acts as a minimum load burden to the output. The converter’s boost inductor current is sensed by R2.

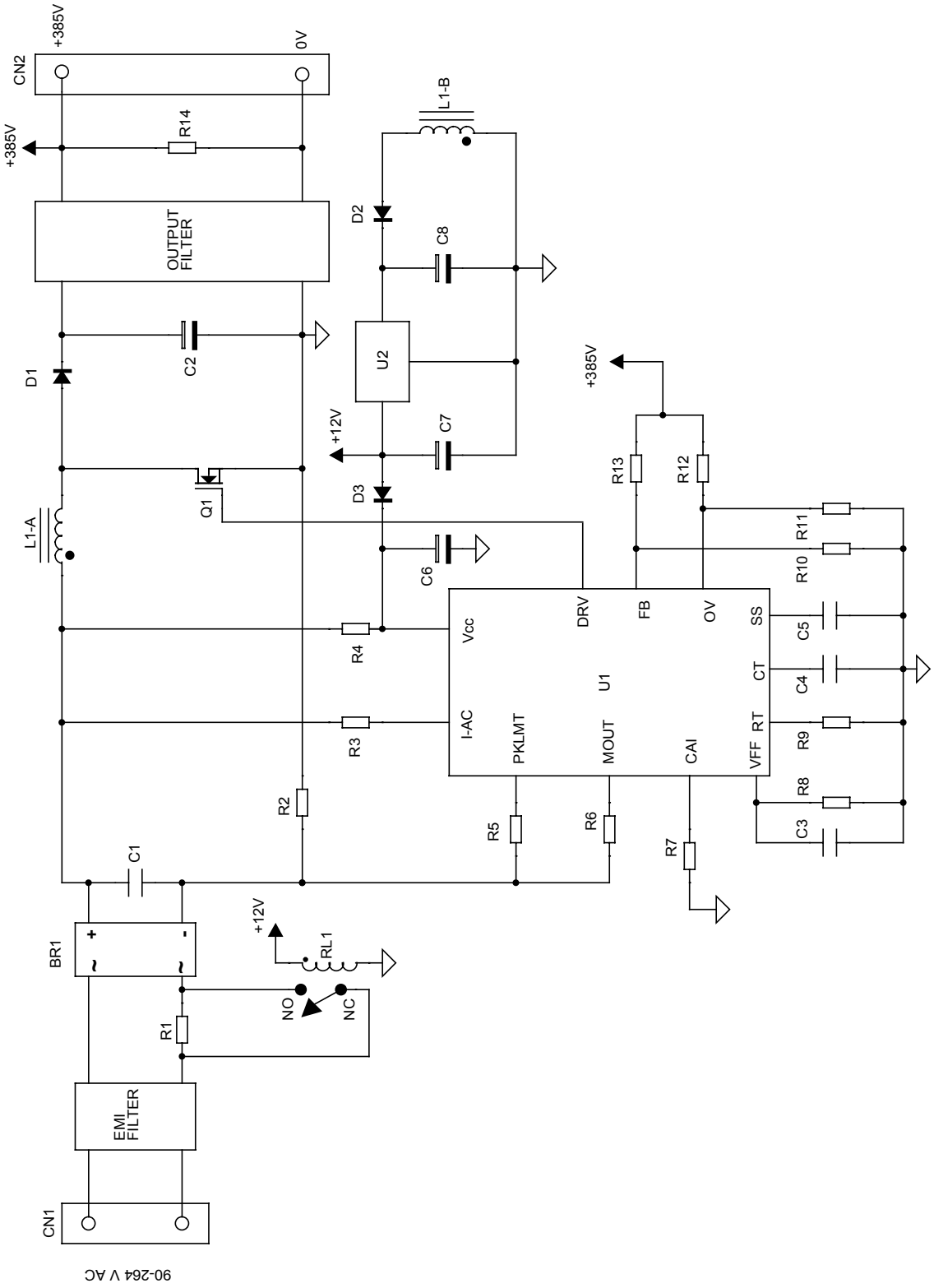

Fig 6.1. Block schematic of the 1200 W PFC circuit.

The boost converter is controlled by the PFC controller U1 to provide output voltage regulation and input power factor correction. The controller senses input voltage wave shape information through R3, inductor current information generated across current sense resistor R2 through R6/R7 and output voltage feedback through R10/R13 and generates PWM pulses to control Q1 and provide input power factor correction. To improve efficiency, the current sense resistor R2 can be replaced with two separate current transformers, with one separate current transformer sensing Q1 current while the other sensing D1 current and subsequently ORing their output to a common burden resistor. Output over voltage protection is provided by R11/R12 while overload current limit is provided by R5. The input wave shape information sensed by R3 is processed by U1 and filtered by C3/R8 to provide input line feed forward control. The converter switching frequency is set by R9/C4 while C5 provides output soft start.

The PFC controller starts up through R4/C6 and is bootstrapped through D3 from the regulated 12 V supply across C7. This regulated auxiliary voltage is generated by linear regulator U2 from the voltage generated across C8 after rectifying the flyback voltage across an additional winding (L1-B) on the boost inductor through D2. This 12 V supply also energizes the relay RL1 to bypass the inrush current limit resistor R1 and thus reduce its dissipation.

6.2 Construction, Schematic Design and Component Selection

A block diagram of the UCC3817 is shown in **Fig. 6.2**. The UCC3817N IC provides all the functions necessary for active power factor corrected pre-regulators. The controller achieves near unity power factor by shaping the AC input line current waveform to correspond to that of the AC input line voltage. Average current mode control maintains stable, low distortion sinusoidal line current.

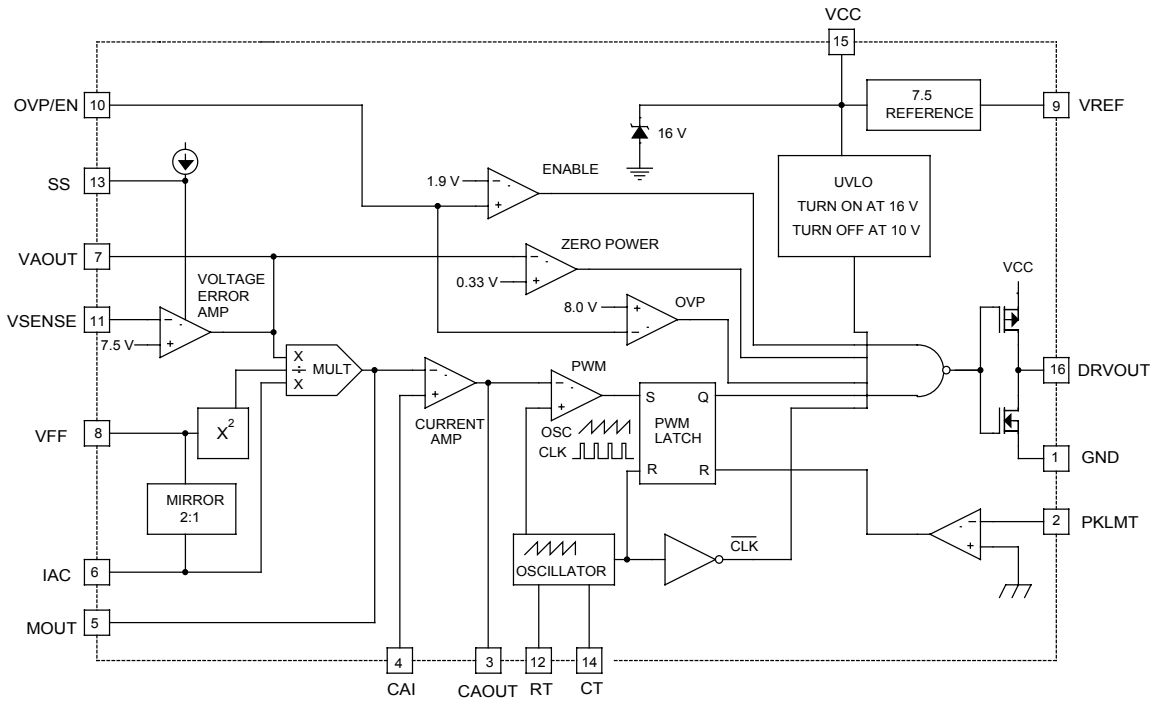

Fig. 6.2. Block diagram of UCC3817.

The top right corner contains the under voltage lock out comparator. The IC's power supply must be within 10 V to 16 V for the device to operate. The inverting input to the voltage error amplifier is connected to pin 11 and is called VSENSE. The non-inverting input to the error amplifier is connected internally to the IC's 7.5 V reference voltage. Moreover this input is also used for providing output soft start function and is implemented by slowly increasing this voltage error amplifier reference through an external capacitor connected at pin 13, and this pin is called SS. This configuration lets the voltage control loop begin operation before the output voltage has reached its operating point and thus eliminates the turn-on overshoot which plagues many power supplies. An internal current source is also provided for charging the soft start timing capacitor at pin 13. The output of the voltage error amplifier, VAOUT, is available on pin 7 of the UCC3817 and this output is also used as an input to the internal multiplier. The other input to the multiplier at pin 6 (IAC) is a current input and this input is used for providing input AC wave shape information from the input bridge rectifier. The DC voltage signal generated at pin 8 by mirroring half of the IAC current into a single pole external filter, is the feed forward input (VFF) signal which is proportional to the input RMS voltage. At low line, the VFF voltage is about 1.4 V. This VFF signal is squared before being fed into the divider input of the multiplier and this multiplier output current flows out of pin 5 (MOUT). This is also connected to the non-inverting input of the current error amplifier. The inverting input of the current amplifier is connected to pin 4. The output of the current error

amplifier connects to the pulse width modulation (PWM) comparator where it is compared with an internal ramp that is similar to the oscillator ramp on pin 14. The timing capacitor at pin 14 (CT), along with the resistor at pin 12 (RT), sets the oscillator and also the boost converter's switching frequency. The oscillator and the PWM comparator drives a set-reset flip-flop, which, in turn, drives a high current driver at pin 16. The internal power supply of the IC is clamped at 16 V. An emergency peak current limit provided on pin 2 (PKLMT) shuts off the output pulses when this pin is pulled slightly below ground. The generated 7.5 V reference voltage output (VREF) is connected at pin 9, the input power supply voltage (VCC) is connected at pin 15 and the IC's ground pin (GND) is connected at Pin 1.

The following paragraphs describe the design basis of the power factor correction boost converter. Please refer to the circuit diagram shown in **Fig. 6.3**.

Given below is the design of the boost inductor, the boost diode, the MOSFET and the output filter capacitor for this 1200 W converter. The circuit works similar to the functional description given in Section 6.2. The designs of other components are not covered. They are done according to the application notes provided by Texas Instruments [6.5, 6.6] and standard engineering design methods.

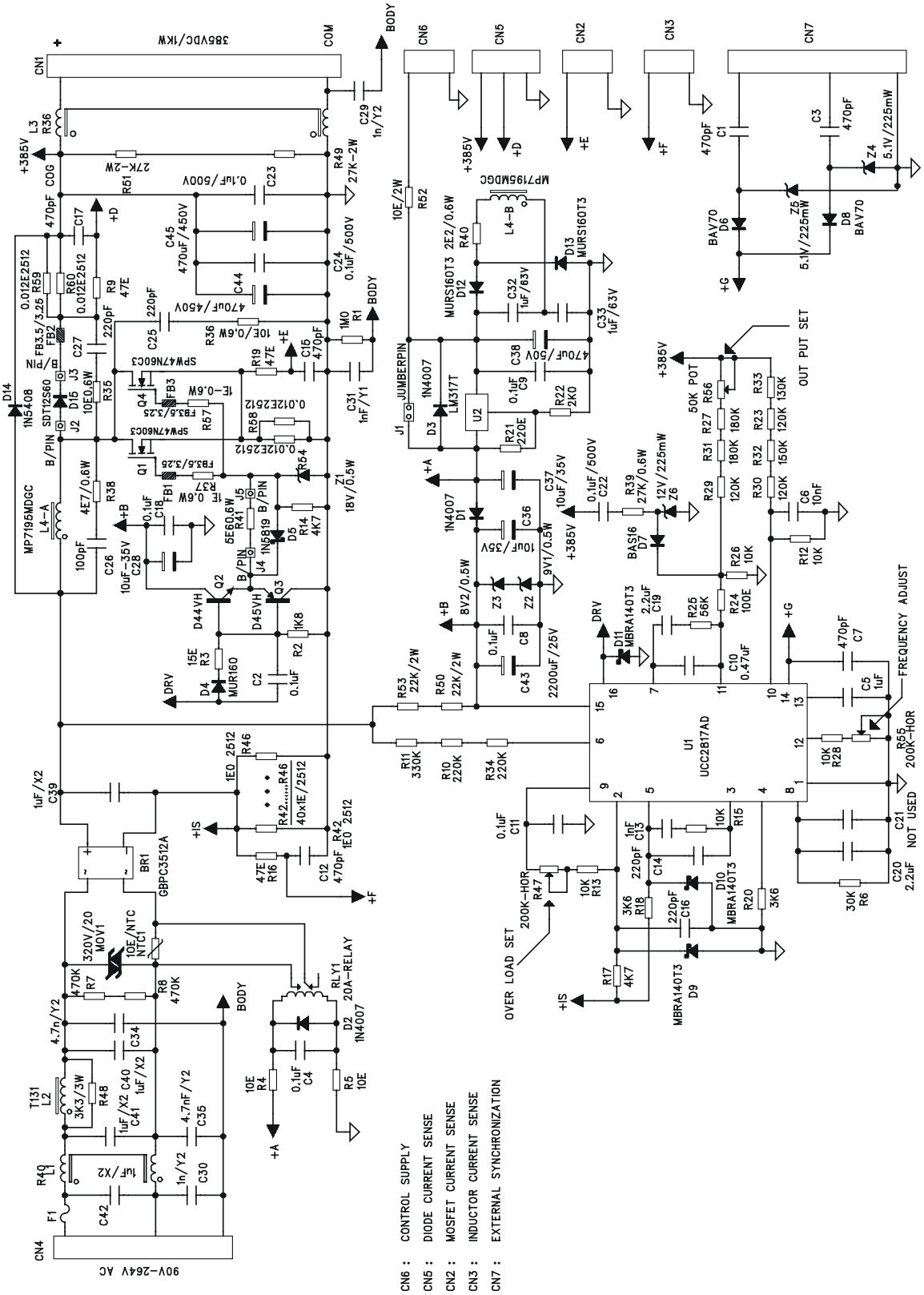

Fig. 6.3. Schematic diagram of the 1200 W PFC circuit.

We now discuss the design of the power circuit components. The boost output capacitor is designed primarily for hold-up time considerations. The required hold-up time is 10 ms. Thus with a maximum output current of 3.2 Amps at 385 V DC output and allowed voltage drop of 40 V in 10 ms, we have the output capacitor (Co) size as:

$$C_o = Io \times holdup\ time / allowed\ voltage \quad (6.1)$$
$$C_o = 3.2\ A \times 10\ ms / 40\ V$$
$$= 800\ \mu F.$$

We have chosen two 470 µF /450 V capacitors (C44, C45) and placed them in parallel. C23/C24 are used as a high frequency by-pass capacitor.

The boost inductor was designed after considering the ripple current and the maximum peak current the inductor shall carry. Taking a 5 V margin, the PFC circuit designed to work from 85 V to 264 V AC. The inductor was designed for the lowest input line condition when the peak inductor current (I_{pk}) is the highest. Selecting a switching frequency (f_s) of 100 kHz, the boost inductance value is computed as below.

$$I_{pk} = (\sqrt{2} \times Max.\ Output\ Power/Efficiency) / (Minimum\ AC\ input\ voltage) \quad (6.2)$$
$$= (\sqrt{2} \times 3.2\ Amps \times 385\ V/0.95) /85V$$
$$= 21.5\ Amps.$$

Choosing a ripple current (ΔI) of 25% of I_{pk}, we have $\Delta I = 5.4A$.

Thus, the maximum peak current $I_{pk(max)}$ is :

$$I_{pk(max)} = I_{pk} + \Delta I / 2 \quad (6.3)$$
$$= 21.5 + 5.4/ 2$$
$$= 24.2\ Amps.$$

The maximum duty cycle (D_{max}), occurs at the lowest line.

$$D_{max.} = (Output\ voltage - Peak\ voltage\ at\ lowest\ line) / (Output\ DC\ voltage) \quad (6.4)$$
$$= (385\ V - 85\ V \times \sqrt{2}) / 385\ V$$
$$= 0.69.$$

The inductor (L) sizing is now done as under.

$$L = Peak\ voltage\ at\ lowest\ line \times D_{max.} / (f_s \times \Delta I) \quad (6.5)$$
$$= 85\ V \times \sqrt{2} \times 0.69/(100\ kHz \times 5.4\ Amps)$$
$$= 154\ \mu H.$$

Care was taken during the inductor's core selection to ensure that the inductor did not saturate at $I_{pk(max)}=24.2\ Amps$ and the required inductance was achieved even at the maximum inductor current.

Different inductor types were used for various experiments. The prototype was tested with various inductance values that would help change the inductor's ripple current. Since inductance changes with load current, it is important to consider that the boost inductor's inductance will not drop below the calculated 154 μH at the lowest line and maximum power, when the inductor current is maximum.

The MOSFETs are selected by their ability to carry the peak inductor current, support the flyback boost voltage and their ability to generate low conduction losses for achieving higher efficiency. In this design two SPW47N60C3 (47 A/600 V/0.07 Ω) [6.7] MOSFETs from Infineon Technologies were used in parallel. The MOSFET's turn-on switching speed was set by R41 while D5 ensured that the turn-off switching speed was very fast. The boost rectifier diode must have a similar voltage and current rating as the MOSFETs. The boost diode (D15) must also be very fast to reduce the MOSFET's turn-on losses. Different diode types were used for various experiments. The prototype was built on a two-layer printed circuit board (PCB) and tested with three different diode types: the SDT12S60 SiC Schottky diode from Infineon Technologies, the STTH806TTI single package series connected diode from ST Microelectronics and the 15ETX06 PFC specific diode from International Rectifier.

The required heat sinks for the power devices are mounted on the PCB. It can be observed that the power devices Q1, Q4, and D15 are placed on one PCB edge while BR1 is placed on the other PCB edge. Thus two separate heat sinks were fixed on the PCB edge and these power devices were clamped on to these heat sinks which are grounded to input safety earth. The PCB layout is given in **Fig. 6.4c** and the photograph of the final prototype is given in **Fig.6.4d**.

Though it is well known that this method of mounting generates the maximum possible common mode noise coupling to the grounded heat sink from the body of Q1, Q4 and D15 (BR1 has an isolated package), this scheme is still very commonly used to bring heat outside the PCB. Thus, this mounting scheme was intentionally selected to investigate the effect of EMI. The devices were isolated from the heat sink by using thermally conductive insulating films, namely K-4 grade silpads from Bergquist. To reduce the common mode noise due to the capacitance

formed between the power device body to the grounded heat sink, a conductive copper sheet of 0.03mm thickness was sandwiched between two K-4 grade silpads and used for fixing the power devices. A teflon wire of 0.57 mm diameter was connected to this copper sheet and after the power device was fixed, the other end of this wire was finally soldered to the source of the MOSFETs. **Fig. 6.4a** shows this mounting method while **Fig. 6.4b** shows a representative diagram of how this was done. These K-4 grade silpads are from Bergquist and their part number is SPK4-0.006-00-1212-NA. Alternately, a ready made EMI-STRATE comprising of a combination of isostrate and copper, from LOCTITE could be used for isolating these devices to the heatsink. The part number for this EMI-STRATE is KD-150-12F.

The power factor correction circuit was natural convection cooled and was tested for full operation to upto 40°C ambient conditions.

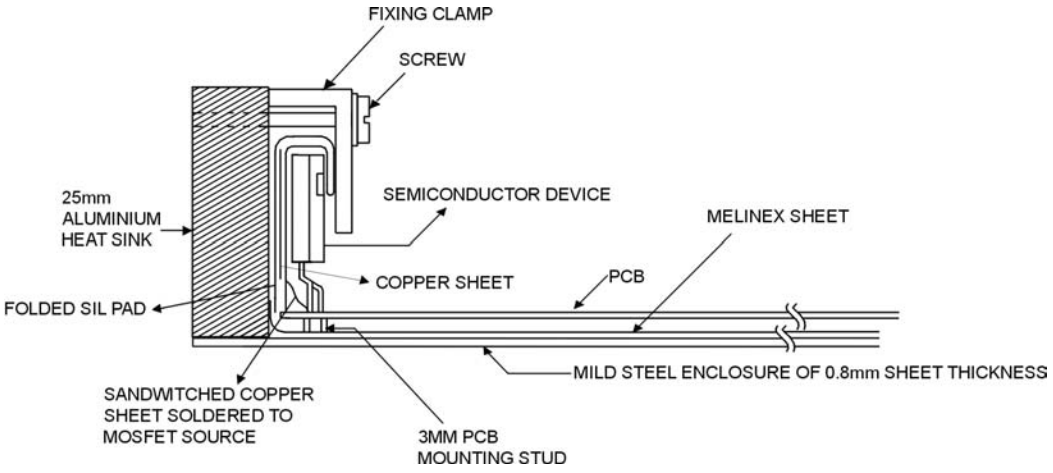

Fig. 6.4a. Mounting method of power semiconductor devices.

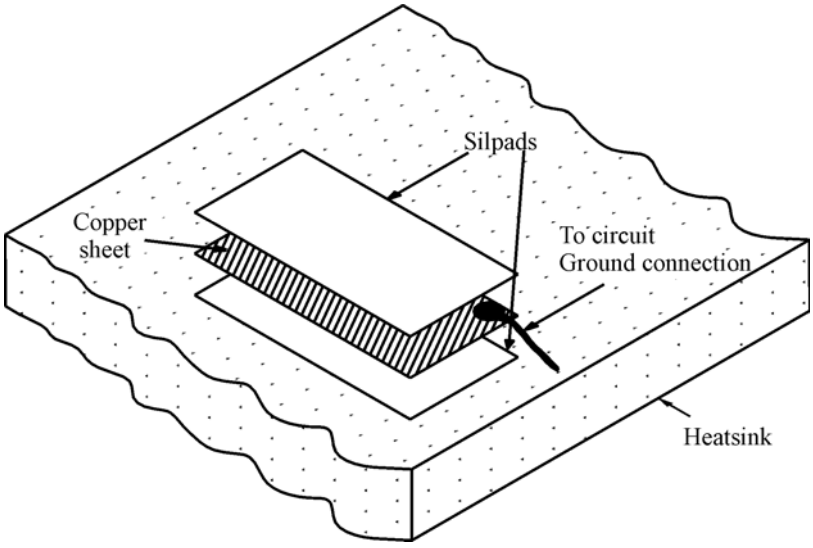

Fig. 6.4b. Representative diagram of a Faraday-shield insulator.

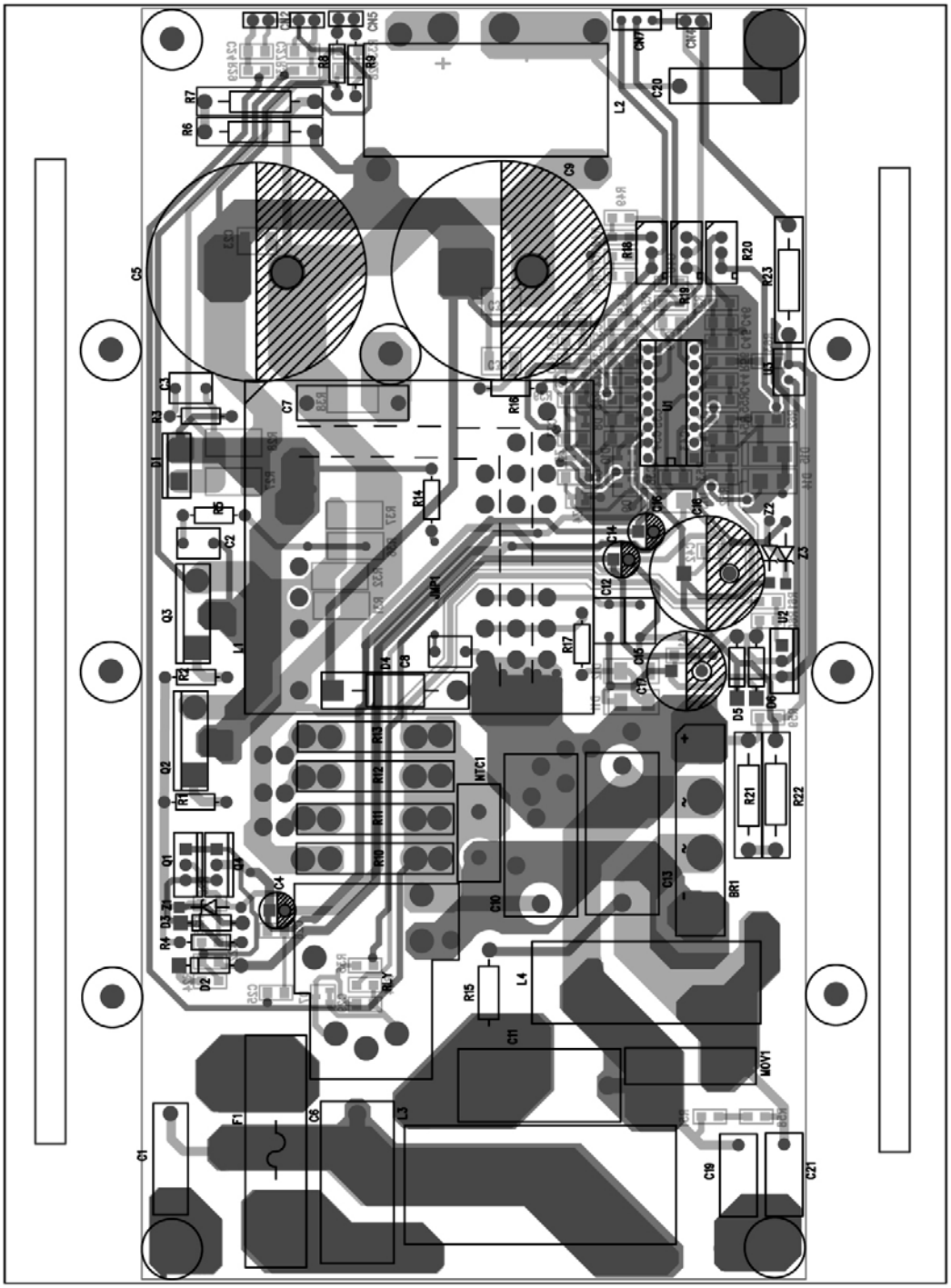

Fig. 6.4d. PCB layout of the 1200 W PFC circuit prototype.

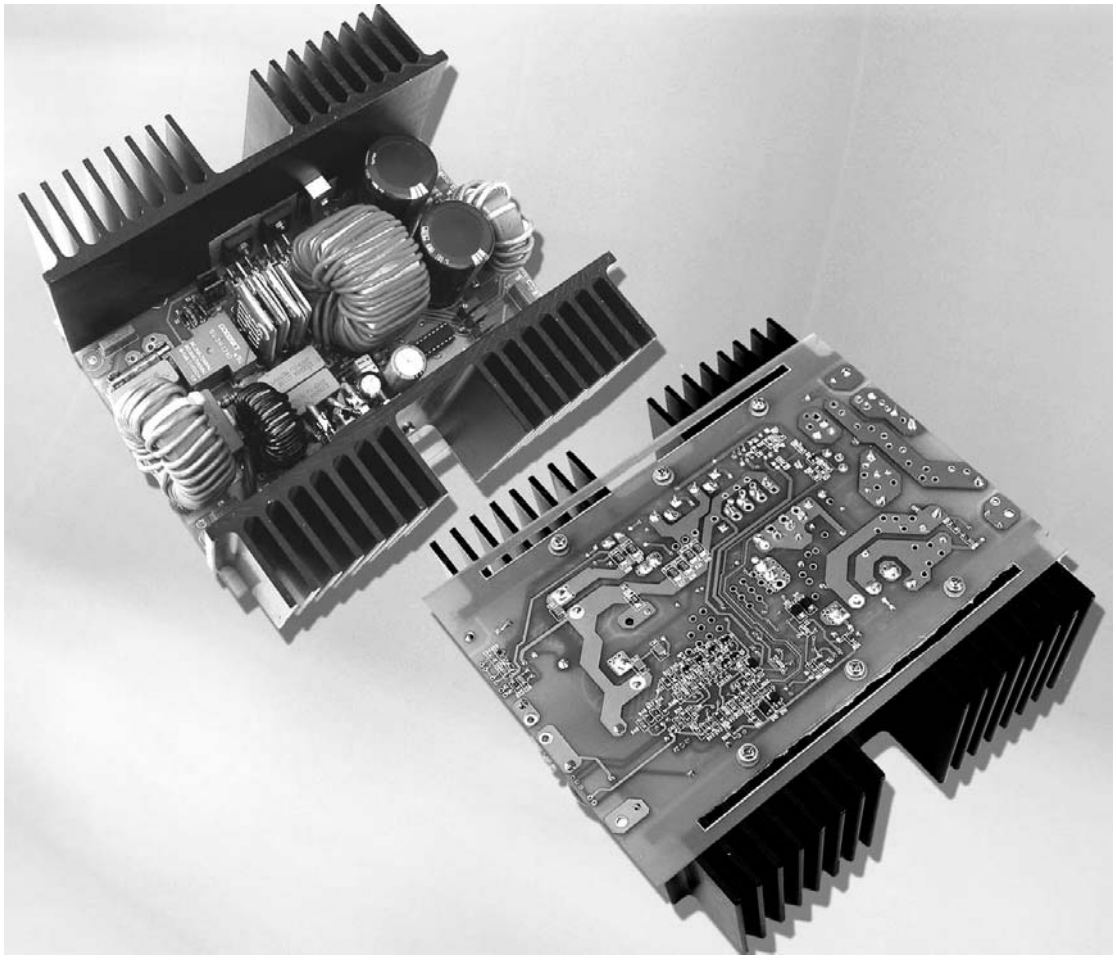

Fig. 6.4d. Photograph of top and bottom view of the 1200 W PFC circuit prototype.

6.3 PCB Layout Considerations and EMI

EMI coupling paths, which connect the interference source with a receptor, may be conducted, radiated, or a combination of both. Differential-mode coupling paths are wires that carry signal or supply current or an adjacent return line that couples interference current propagating through it. Common-mode coupling paths occur when current travels down both the signal or supply line and the return line is in phase or the return is an unintended path, which is often the chassis ground or earth ground.

Interference almost always originates as differential mode, but both electric and magnetic field coupling paths are predominantly common mode, which means that the farther the EMI gets from its source, the higher the percentage of common-mode coupling paths. Low-frequency

energy (<1 MHz) doesn't couple very efficiently, so it is generally confined to the intended wire paths, but above 1 MHz, common-mode coupling paths become increasingly significant. At higher frequencies (greater than or equal to 30 MHz), radiated paths become dominant.

Because common-mode interference, which is very difficult to filter, relies primarily on parasitic coupling paths, it is important to keep those paths to an absolute minimum. This involves controlling both the parasitics in the component itself and parasitics between the intended current path (traces and components) and other system members, which include other components and traces, structural members, and perhaps a heat sink. When addressing this challenge, the following generalizations are made:

- Because of the length of their leads, capacitors have series inductance, which reduces their effectiveness at high frequencies. Particularly film capacitors resonate at a surprisingly low frequency, becoming inductive above resonance.
- As a result of inter-winding capacitance, inductors have shunt capacitance, which reduces their high-frequency effectiveness. In addition, open-flux-path inductors have a magnetic field extending well beyond the inductor envelope.
- Coupling paths from the intended current path to heat sinks and circuit board traces can be a significant concern.

Coping with Internal Interference

Thus, a clear-cut rule for designing for EMI is to control interference as close to its source as possible. The farther the noise currents and fields move away from the source, the harder it is to contain the energy. In the case of power supplies, internally generated high-frequency noise is best controlled right at the source.

Actually, reducing the harmonics produced by the "fast" signal edges doesn't affect efficiency that much - often less than 0.5%. For an EMI peak at 50 MHz in a 50 kHz converter, the 1,000th harmonic is at 50 MHz - this will be of low amplitude and easy to filter. A good converter design will have low high-frequency ringing emissions without the need for a slow switching speed.

The heat-sinks used for dissipating heat can also contribute to the common-mode noise because noise currents can flow between the body of the semiconductor devices and the heat-sink on which they are fixed.

The slight capacitance existing between the semiconductor devices and the heatsink, which usually connects to ground, is the contributor. Even poor coupling through a small parasitic capacitance can cause common-mode noise because the switching signals in the semiconductors have high voltage amplitudes. It may thus be needed to disconnect, or float heat-sinks from ground or alternately use Faraday-shield insulators between semiconductors and heat-sinks to reduce coupling. A similar Faraday-shield insulator was used in the actual prototype. **Fig. 6.4a** and **Fig. 6.4b** is a representative diagram of how this was actually done in the prototype.

Parasitic coupling also may occur between the primary and secondary windings of a transformer. Properly separating the windings as well as the use of Faraday shields, will minimize this form of coupling but such measures cannot completely eliminate coupling and they also increase power-supply costs. However, this does not apply for the PFC circuit prototype we built as the output was not isolated.

Thus, high frequency PCB design and EMI are interrelated. Unless care is taken during design, controlling EMI only by adding more and more filters at a later stage is often not very fruitful or economical. Given below are some of the basic design rules that must be followed.

- PCB traces are not perfect equipotential conductors and can have significant resistance, inductance, mutual inductance with other PCB traces and have mutual capacitive coupling.

- Internal circuit ground node is never at zero potential as PCB traces are not perfect equipotential conductors. Thus, it is often quite difficult to ensure that each circuit block operates with the same ground potential reference. These cause circulating ground loop currents that cause EMI. Understanding circuit ground return currents and limiting ground loop currents in the PCB is often the key to reducing EMI at the source.

- Switching currents in high frequency circuits contains large high frequency harmonics. PCB trace inductance is critical to causing ringing, voltage spikes, switching loss and associated EMI. The longer these currents travel and the larger the current loop area gets, more of B and E fields get generated causing increased radiated EMI. So it is very important to identify the high di/dt switching currents loops and limit the loop currents area in the PCB by design to reduce EMI. One of the best solutions to doing this is to run the return loop current on

the other PCB layer. In this way, the field generated by the top layer conductor balances the field generated by the bottom layer conductor resulting in almost zero loop area.

- Coupling of signals via magnetic fields is another concern. Often magnetic components, particularly components like flyback transformers and inductors that have DC bias and air gap, can radiate strong magnetic fields. These fields induce circulating currents in conductors in the near vicinity and these circulating currents can cause EMI. Consideration of the possible presence of these fields during design is very helpful in reducing EMI.

6.4 Oscillograms, EMI Measurements and Test reports

The PWM output pulses of the UC3817 (pin 16) with respect to the ramp waveform at the timing capacitor (pin 14), is shown in **Fig. 6.5** below. Channel 1 represents the timing capacitor's ramp signal while Channel 2 represents the PWM signal.

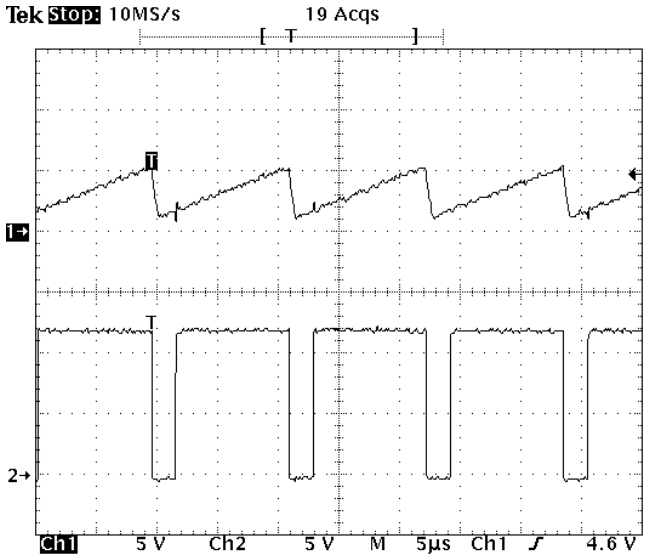

Fig. 6.5. PFC Controller's oscillator ramp waveform and PWM pulses.

These PWM output pulses drive the PFC circuit's power MOSFETs. With the PWM duty cycle varying very widely with the instantaneous line voltage changes, the MOSFETS' waveforms also changes accordingly. The duty cycle is highest when the instantaneous line voltage is the lowest. The oscillogram shown in **Fig. 6.6,** shows the MOSFET's gate and drain waveform for a smaller duty cycle. Channel 1 represents the MOSFET gate source drive signal while Channel 2 represents the corresponding drain source signal.

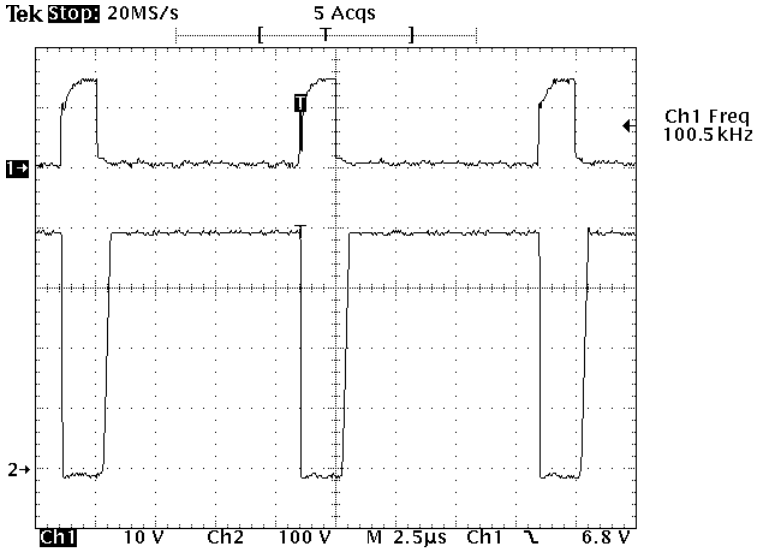

Fig. 6.6. MOSFET's gate and drain waveform for a smaller duty cycle.

The oscillogram shown in **Fig. 6.7**, shows the MOSFET's gate and drain waveform for a larger duty cycle. Channel 1 represents the MOSFET gate source drive signal while Channel 2 represents the corresponding drain source signal.

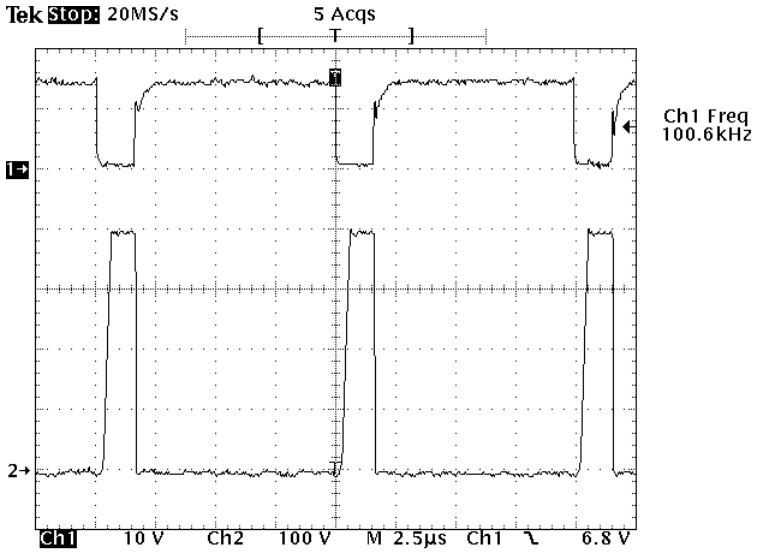

Fig. 6.7. MOSFET's gate and drain waveform for a larger duty cycle.

The input power factor of the PFC Circuit was recorded for 1200 W. The PFC circuit was connected to a variable AC source of 30 A current rating and rated maximum load of 1200 W. With the input varied between 90 V to 264 V AC, the input Power Factor (PF) at 90 V AC, 230V AC and 264 V AC was recorded with the help of a PF meter. The above tests

were conducted again with output set 100 W. The power factor was found to be better than 0.90 for all loads and line conditions.

The oscillogram of **Fig. 6.8**, shows the input current at 230 V AC input and 1200 W output load. Channel 1 shows the input voltage and Channel 2 shows the input current.

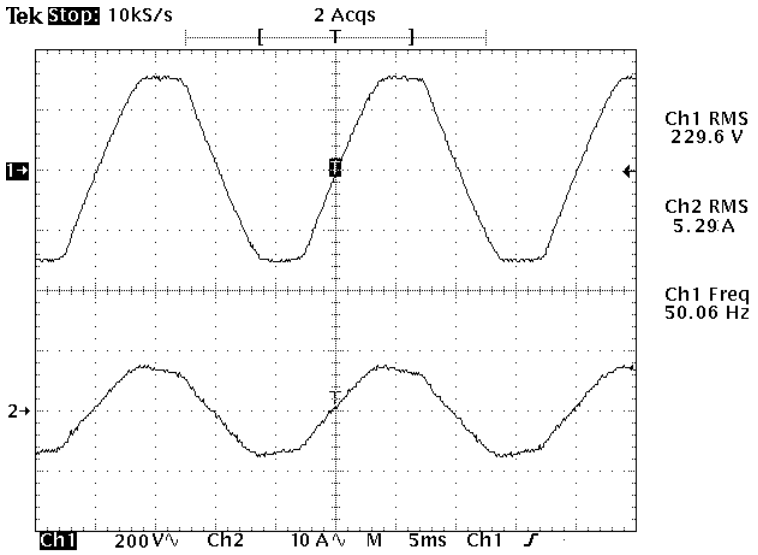

Fig. 6.8. Input voltage and input current for a 1200 W load.

The PFC circuit regulated the output DC voltage to better than 385 V ± 2%, for all line and load conditions. At full load the output was 385 V while at no load condition, the output DC would increase to 392 V. Line regulation was excellent, better than 1%. For all line conditions the efficiency was better than 92%.

EMI/EMC

Conducted and radiated emission was measured for the PFC circuit as per EN 55022 Class – B limits. Length of input AC supply cable from LISN was one metre and length of output DC supply cable to load was 0.5 metre. The boost diode (D15) was a Silicon Carbide diode and the MOSFET turn-on switching speed was set very fast by a 4.7 Ω resistor (R41).

Fig. 6.9 shows the Conducted Emission Spectrum at different frequency bandwidths, with the PFC circuit working at 1200 W load and input voltage set to 230V. QP given at the bottom of the spectrum indicates the computed quasi-peak at the MARKER peak. The highest peak is at the MARKER position and this peak value and the corresponding frequency is given at the top extreme right of each plot.

Conducted Emmision Spectrum in Frequency Range of 150 kHz to 500 kHz

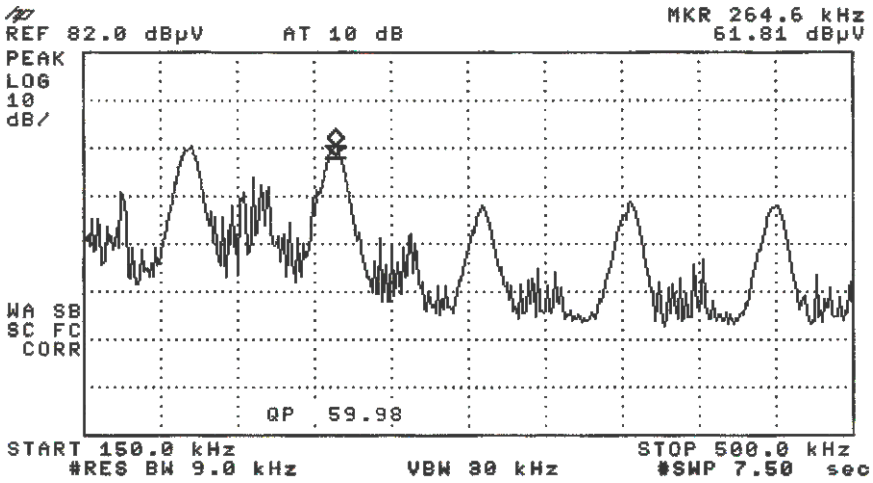

Fig 6.9 a. Highest quasi-peak was recorded at 264.6 kHz and was of magnitude 59.98 dBµV.

Conducted Emmision Spectrum in Frequency Range of 500 kHz to 5.0 MHz

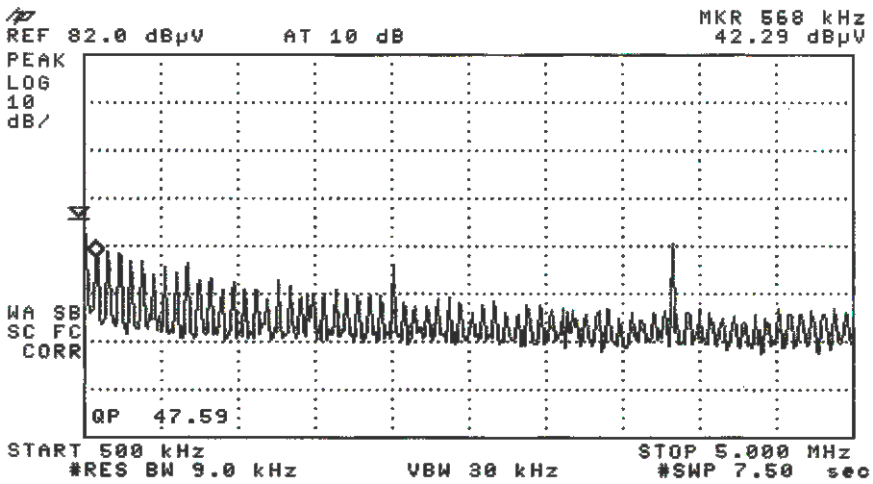

Fig. 6.9 b. Highest quasi-peak was recorded at 568 KHz and was of magnitude 47.59 dBµV.

Conducted Emmision Spectrum in Frequency Range of 5.00 MHz to 30 MHz

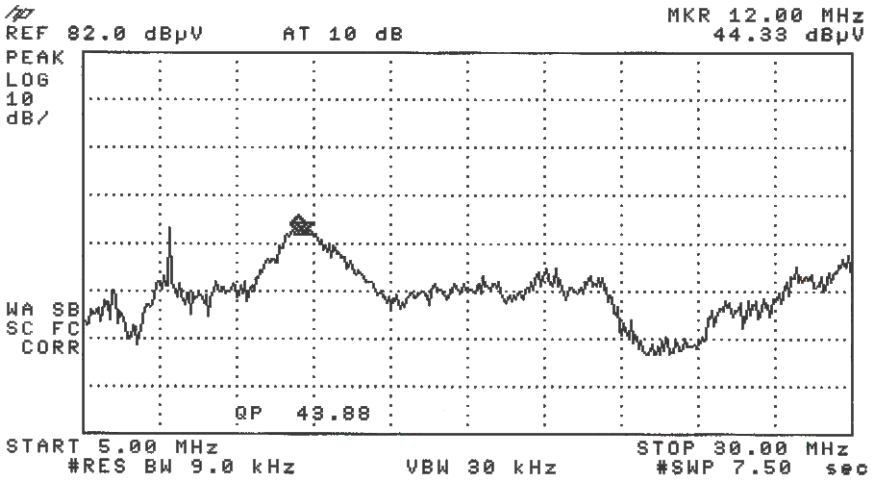

Fig. 6.9 b. Highest quasi-peak was recorded at 12.00 MHz and was of magnitude 43.88 dBµV.

Radiated Emmision Spectrum in Frequency Range of 30 MHz to 230MHz

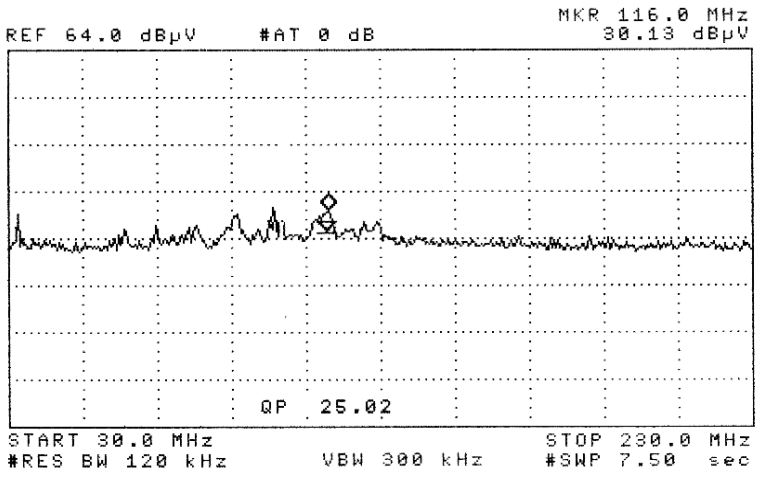

Fig. 6.10 Highest quasi-peak was recorded at 116 MHz and was of magnitude 25.02 dBµV. This value excludes applicable antenna correction factor of about 10 and needs to be added to this result.

Fig. 6.10 shows the Radiated Emission Spectrum at 30 MHz-230 MHz frequency bandwidths, with the PFC circuit working at 1200 W load and input voltage set to 230 V. QP given at the bottom of the spectrum indicates computed quasi-peak at the MARKER peak. The highest peak is at the MARKER position and this peak value and its corresponding frequency is given on the top extreme right of each plot.

The Antenna factor at the measured peak was about 10 and this needs to be added to the recorded peak and quasi-peak values.

Testing was done in a shielded chamber with the antenna at 3-metre distance. The input /output wires were kept short and mutually twisted. As there was no emission in the range of 230MHz to 1GHz, its spectrum was not recorded.

6.5 Other Experiments and Various Results

Having built a working prototype PFC circuit, many component values were changed for making various measurements. Many of these measurements form the basis of this research work. Referring to the schematic of the prototype given in **Fig. 6.3**, J1 to J5 represent locations where component values were often changed for these measurements. Waveforms were often recorded at connector CN2, CN3, CN5 and CN6. Details of these component value changes and the results achieved are presented in detail in the nine publications given at the end of this thesis.

Chapter 7

Conclusion

In this thesis, the causes of input current distortion in AC-DC single phase rectifier- capacitor filter circuits and the mandatory European standard EN 61000-3-2 that limits the low frequency harmonics that can be generated by these rectifier-capacitor filter circuits, are discussed. Different Power Factor Correction (PFC) techniques / strategies useful for meeting this standard and mitigation of this problem, are explored. These include the use of passive PFC chokes and the Continuous Conduction Mode (CCM) boost converter, which is the most commonly used PFC topology for medium to high power applications. The CCM PFC converter provides unity power factor correction and generates negligible harmonics, while the output is regulated to a high voltage DC, in the face of input AC varying between 85 V to 270 V. In this thesis, this feature is exploited to develop a central power factor correction scheme, that could simultaneously run many computer loads. Cost and other advantages of having a central power factor correction scheme over having individual active or passive power factor correction circuits, are investigated and documented. The advantages of having a higher system reliability and an in-built uninterrupted power supply (UPS) with automatic universal worldwide operation of all loads connected to it, are also highlighted.

In spite of its complexity and additional component costs, the reason for the CCM PFC converter being the preferred choice for PFC front-end converters in single-phase AC-DC converters is explained. EMI from these PFC converters is another problem. Typical sources are the switching of the MOSFET or the boost diode at reverse recovery. Design modifications that reduce EMI at its source may be much less costly than incorporating LC-filters later for reducing the interference. From this explanation it is concluded that there is great need for optimization of performance and cost of these CCM PFC converters. By making measurements on a practical PFC prototype for different design schemes and output power, various design methods that significantly improve the

performance and cost of these CCM PFC converters are analyzed and presented in this thesis.

The large dependence of the electrical and thermal performances of these hard-switched CCM PFC converters on the characteristics of the power switching devices, particularly the boost diode, is investigated. The performance improvements achieved by way of reduction in the total component count, increased power density provided by the new generation switching devices, particularly the Silicon Carbide Diode, is highlighted in **Section 5.3** and **Papers C** and **D**.

After this, the effect of the boost inductor's inductance on the electrical and thermal performances of these converters is investigated to achieve higher power density at lower cost. Improvements in efficiency, increased power density and reduced EMI achievable by proper inductor design are presented. Based measurements made on a practical 1200 W rated PFC prototype, a systematic design approach for the boost inductor is proposed.

The large dependence of the converter's EMI performances on the boost diode recovery characteristics, boost MOSFET's switching speed and the inductor winding method is also investigated. The results obtained by making measurements shows that by incorporating a small lossy ferrite bead to one of the boost diode terminals, the radiated EMI performance can actually remain quite unaffected for different diode types like a Silicon Carbide diode or a single junction PFC specific hyper-fast silicon diode or a single package series connected hyper-fast silicon diode. It is also highlighted on how this small lossy ferrite bead can also help achieve a faster MOSFET turn-on switching speed resulting in higher efficiency, without significantly increasing EMI. Significant efficiency improvements and reduction of Radiated EMI of over 14 dbμV/m was demonstrated in this work.

Finally, the large dependence of the radiated fields from the boost inductor and on the conducted EMI performance of these converters is investigated. A simple novel inductor winding method is proposed by which reduction in conducted EMI by more than 23 dBμV for a 100 W PFC converter could be achieved.

7.1 Future Research

Power factor correction circuits will be increasingly used as AC-DC converter front ends in the future. This necessitates further future research. The following topics may be of immediate interest.

- Further to the work that has already been done on single stage PFC converters that generate isolated output, the inability of these converters to work with low output filter capacitance (less than 1000 μF) and using a low cost 500 V switch in the primary circuit needs further investigation.

- Active PFC converters generate EMI and a major part of it is generated as differential mode conducted noise. For higher power converters, a possibility could be to use two interleaved converters. A new control method by which the differential mode EMI of these two interleaved converters could be mutually cancelled would be of great interest. By this, the classical problem of large EMI generated by Critical Conduction Mode (CRM) converters could be solved, and they could then be more extensively used to exploit their other advantages.

- Present day resonant mode PFC circuit topologies are not popular as they increase circuit complexity without being able to provide any significant reduction in EMI or improvement in efficiency. Newer resonant mode topologies that overcome these limitations and improve an active PFC circuit's efficiency to at least 97% at 110 V AC input, will be a significant improvement.

- Digital control of switch mode power supplies with a PFC circuit front end is an evolving field today. New digital control schemes to provide phase shift to reduce switching frequency harmonics in two or more paralleled converters could be very helpful.

- Conducted EMI is the high frequency spectrum of the switching circuits in the PFC converter. A control scheme by which these harmonics generated by one independent converter could be cancelled with another independent converter, without the need for any direct communication, would be very useful.

- The use of active PFC converters reduces the low frequency harmonics generated by AC-DC rectifier circuits but they now generate high frequency harmonics in the form of conducted EMI. The impact of thousands of PFC converters connected to the utility grid on the power quality needs more investigation.

Chapter 8

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Chapter 9

Appendix

9.1 List of Materials

The following pages give the detailed component list of the developed PFC circuit. The legends refer to the schematic diagram given in **Fig. 6.3**.

Material List of PFC Circuit Prototype			
ITEM NO.	**DESCRIPTION**	**PART NUMBER**	**VENDOR NAME**
RESISTORS			
R1	1M, ±1%, 0.25W,Case Size 1206	MCR18 EZH F-105	ROHM
R2	1K8, ±1%, 0.25W,Case Size 1206	MCR18 EZH F-1801	ROHM
R3	15E, ±1%, 0.25W, Case Size 1206	MCR18 EZH F-15R0	ROHM
R4	10E0, ±1%, 0.25W, Case Size 1206	MCR18 EZH F-10R0	ROHM
R5	10E0, ±1%, 0.25W, Case Size 1206	MCR18 EZH F-10R0	ROHM
R6	30K, ±1%, 0.25W,Case Size 1206	MCR18 EZH F-3002	ROHM
R7	470K, ±1%, 0.25W,Case Size 1206	MCR18 EZH F-4703	ROHM
R8	470K, ±1%, 0.25W,Case Size 1206	MCR18 EZH F-4703	ROHM
R9	10K, ±1%, 0.25W,Case Size 1206	MCR18 EZH F-1002	ROHM
R10	220K, ±1%, 0.25W,Case Size 1206	MCR18 EZH F-2203	ROHM
R11	330K, ±1%, 0.25W,Case Size 1206	MCR18 EZH F-3303	ROHM
R12	10K, ±1%, 0.25W,Case Size 1206	MCR18 EZH F-1002	ROHM
R13	10K, ±1%, 0.25W,Case Size 1206	MCR18 EZH F-1002	ROHM
R14	4K7, ±1%, 0.25W,Case Size 1206	MCR18 EZH F-4701	ROHM
R15	10K, ±1%, 0.25W,Case Size 1206	MCR18 EZH F-1002	ROHM
R16	10K, ±1%, 0.25W,Case Size 1206	MCR18 EZH F-1002	ROHM
R17	4K7, ±1%, 0.25W,Case Size 1206	MCR18 EZH F-4701	ROHM
R18	3K6, ±1%, 0.25W,Case Size 1206	MCR18 EZH F-3601	ROHM
R19	10K, ±1%, 0.25W,Case Size 1206	MCR18 EZH F-1002	ROHM
R20	3K6, ±1%, 0.25W,Case Size 1206	MCR18 EZH F-3601	ROHM
R21	220E, ±1%, 0.25W, Case Size 1206	MCR18 EZH F-2200	ROHM
R22	2K0, ±1%, 0.25W,Case Size 1206	MCR18 EZH F-2001	ROHM
R23	120K, ±1%, 0.25W,Case Size 1206	MCR18 EZH F-1203	ROHM
R24	100E, ±1%, 0.25W, Case Size 1206	MCR18 EZH F-1000	ROHM
R25	56K, ±1%, 0.25W,Case Size 1206	MCR18 EZH F-5602	ROHM
R26	10K, ±1%, 0.25W,Case Size 1206	MCR18 EZH F-1002	ROHM
R27	180K, ±1%, 0.25W,Case Size 1206	MCR18 EZH F-1803	ROHM
R28	10K, ±1%, 0.25W,Case Size 1206	MCR18 EZH F-1002	ROHM
R29	120K, ±1%, 0.25W,Case Size 1206	MCR18 EZH F-1203	ROHM
R30	120K, ±1%, 0.25W,Case Size 1206	MCR18 EZH F-1203	ROHM
R31	180K, ±1%, 0.25W,Case Size 1206	MCR18 EZH F-1803	ROHM

R - RESISTORS D - DIODES Q - TRANSISTORS C - CAPACITORS U - IC Z/ZD - ZENER DIODES	PT - PULSE TRANSFORMER CT - CURRENT TRANSFORMER L - INDUCTOR MOV - METAL OXIDE VARISTOR P - POTENTIOMETERS F - FUSE	LD - LIGHT EMITTING DIODE CN/J – CONNECTOR T - TRANSFORMERS NTC - NEGATIVE THERMISTOR FB – FERRITE BEAD RLY1 - RELAY

Material List of PFC Circuit Prototype

ITEM NO.	DESCRIPTION	PART NUMBER	VENDOR NAME
R32	150K, ±1%, 0.25W,Case Size 1206	MCR18 EZH F-1503	ROHM
R33	130K, ±1%, 0.25W,Case Size 1206	MCR18 EZH F-1303	ROHM
R34	220K, ±1%, 0.25W,Case Size 1206	MCR18 EZH F-2203	ROHM
R47	200K,±10%,0.75W,3006P Package,Trimmable Pot.	3006P-1-204	BOURNS
R35	10E, ±5%, 1W, MFR	2306 197 53109	VISHAY BC COMPONENTS
R36	10E, ±5%, 1W, MFR	2306 197 53109	VISHAY BC COMPONENTS
R37	1E0, ±1%, 0.6W, MFR	2322 186 3 1008	VISHAY BC COMPONENTS
R38	4E7,±1%, 0.6W, MFR	2322 186 3 4708	VISHAY BC COMPONENTS
R39	27K,±1%, 0.6W, MFR	2322 186 3 2703	VISHAY BC COMPONENTS
R40	2E2,±1%, 0.6W, MFR	2322 186 3 2208	VISHAY BC COMPONENTS
R41	5E6,±1%, 0.6W, MFR	2322 186 3 5608	VISHAY BC COMPONENTS
R42-R46	(1E, ±1%,1W, Case Size2512) x (40)	CRL2512-FW-0R05E_	ROHM
R48	3K3, ±5%, 3W,Wire Wound Resister	2322 329 03332	VISHAY BC COMPONENTS
R49	22K,±5%, 2W, MFR	2306 198 53 223	VISHAY BC COMPONENTS
R50	22K,±5%, 2W, MFR	2306 198 53 223	VISHAY BC COMPONENTS
R51	22K,±5%, 2W, MFR	2306 198 53 223	VISHAY BC COMPONENTS
R52	10E,±5%, 2W, MFR	2306 198 53 109	VISHAY BC COMPONENTS
R53	22K,±5%, 2W, MFR	2306 198 53 223	VISHAY BC COMPONENTS
R54	0.012E, ±1%,1W, Case Size2512	CRL2512-FW-0R012E_	ROHM
R55	200K, ±10%, 0.75W, 3006P Package, Trimmable Potentiometer.	3006P-1-204	BOURNS
R56	50K,±10%,0.75W,3006P Package,Trimmable Potentiometer.	3006P-1-503	BOURNS
R57	1E0, ±1%, 0.6W, MFR	2322 186 3 1008	VISHAY BC COMPONENTS
R58	0.012E, ±1%,1W, Case Size2512	CRL2512-FW-0R012E_	ROHM
R59	0.012E, ±1%,1W, Case Size2512	CRL2512-FW-0R012E_	ROHM
R60	0.012E, ±1%,1W, Case Size2512	CRL2512-FW-0R012E_	ROHM
CAPACITORS			
C1	470pF, ±5%, 50V, COG, Case Size1206	B37871K5471J060	EPCOS
C2	0.1µF, ±10%, 50V, X7R, Case Size1206	B37872K5104K060	EPCOS
C3	470pF, ±5%, 50V, COG, Case Size1206	B37871K5471J060	EPCOS
C4	0.1µF, ±10%, 50V, X7R, Case Size1206	B37872K5104K060	EPCOS
C5	1µF, ±10%, 16V, X7R, Case Size1206	1206 YC 105 MAT2A	AVX
C6	10nF, ±10%, 50V, X7R, Case Size1206	B37872K5103K060	EPCOS
zC7	470pF, ±5%, 50V, COG, Case Size1206	B37871K5471J060	EPCOS
C8	0.1µF, ±10%, 50V, X7R, Case Size1206	B37872K5104K060	EPCOS
C9	0.1µF, ±10%, 50V, X7R, Case Size1206	B37872K5104K060	EPCOS

R - RESISTORS D - DIODES Q - TRANSISTORS C - CAPACITORS U - IC Z/ZD - ZENER DIODES	PT - PULSE TRANSFORMER CT - CURRENT TRANSFORMER L - INDUCTOR MOV - METAL OXIDE VARISTOR P - POTENTIOMETERS F - FUSE	LD - LIGHT EMITTING DIODE CN/J – CONNECTOR T - TRANSFORMERS NTC - NEGATIVE THERMISTOR FB – FERRITE BEAD RLY1 - RELAY

Material List of PFC Circuit Prototype

ITEM NO.	DESCRIPTION	PART NUMBER	VENDOR NAME
C10	0.47µF, ±10%,50V,X7R, Case Size1206	B37872K5474K062	MURATA
C11	0.1µF, ±10%, 50V, X7R, Case Size1206	B37872K5104K060	EPCOS
C12	0.1µF, ±10%, 50V, X7R, Case Size1206	B37872K5104K060	EPCOS
C13	1nF, ±10%, 50V, X7R, Case Size1206	B37872K5102K060	EPCOS
C14	220pF, ±5%, 50V, COG, Case Size1206	B37871K5221J060	EPCOS
C15	0.1µF, ±10%, 50V, X7R, Case Size1206	B37872K5104K060	EPCOS
C16	220pF, ±5%, 50V, COG, Case Size1206	B37871K5221J060	EPCOS
C17	0.1µF, ±10%, 50V, X7R, Case Size1206	B37872K5104K060	EPCOS
C18	0.1µF, ±10%, 50V, X7R, Case Size1206	B37872K5104K060	EPCOS
C19	2.2µF, ±10%, 16V, X7R, Case Size1206	1206YC225KAT2A	AVX
C20	2.2µF, ±10%, 10V, X7R, Case Size1206	1206ZC225KAT2A	AVX
C21	Not Used		
C22	0.1µF,±10%,500V, X7R,Case Size 1812	VJ1812Y104KXEAT	VISHAY VITRAMON
C23	0.1µF,±10%,500V, X7R,Case Size 1812	VJ1812Y104KXEAT	VISHAY VITRAMON
C24	0.1µF,±10%,500V, X7R,Case Size 1812	VJ1812Y104KXEAT	VISHAY VITRAMON
C25	220pF, ±10%, 2kVDC,High voltage ceramic disc Capacitor,-25°C to +85°C	DEBB33D221KC1B	MURATA
C26	100pF, ±10%, 2kVDC,High voltage ceramic disc Capacitor, +25°C to +85°C	DEBB33D101KC1B	MURATA
C27	220pF, ±10%, 2kVDC,High voltage ceramic disc Capacitor,-25°C to +85°C	DEBB33D221KC1B	MURATA
C28	10µF/35V/±20%,Tantalum Capacitor,-55°C to85°C,P-2.54mm	TAP106M035SCS	AVX
C29	1nF, ±20% ,250VAC,Interterence Supression CapacitorY2, -40°C to +100°C	PHE850EA4100MA01R17	EVOX RIFA
C30	1nF, ±20% ,250VAC,Interterence Supression CapacitorY2, -40°C to +100°C	PHE850EA4100MA01R17	EVOX RIFA
C31	1nF, ±20%,, 440VAC,Interference Suppression CapacitorY1 -40°C +115°C	PME294RB4100MR30	EVOX RIFA
C32	1µF, ±20% , 63V , Stacked-film capacitor, MMK series	MMK5 105M63J04L4 BULK	EVOX RIFA
C33	1µF, ±20% , 63V , Stacked-film capacitor, MMK series	MMK5 105M63J04L4 BULK	EVOX RIFA
C34	4.7nF, ±20% ,300VAC,Interference Suppression CapacitorY2, -55°C to +110°C	PHE850EA4470MA03R17	EVOX RIFA
C35	4.7nF, ±20% ,300VAC,Interference Suppression CapacitorY2, 55°C to +110°C	PHE850EA4470MA03R17	EVOX RIFA
C36	10µF/35V/±20%,Tantalum Capacitor,-55°C to 85° C,P- 2.54mm	TAP106M035SCS	AVX
C37	10µF/35V/±20%,Tantalum Capacitor,-55°C to 85° C, P-2.54mm	TAP106M035SCS	AVX
C38	470µF, ±20%, 50V, -55°C to +105°C,Type VZ, Radial	UVZ1H471MHD	NICHICON
C39	1µF, ±20% ,3000VAC, Interference Suppression CapacitorX2 -55°C to +105°C	PHE840EY7100MD16R06L2	EVOX RIFA
C40	1µF, ±20% ,3000VAC, Interference Suppression CapacitorX2 -55°C to +105°C	PHE840EY7100MD16R06L2	EVOX RIFA
C41	1µF, ±20% ,3000VAC, Interference Suppression CapacitorX2 -55°C to +105°C	PHE840EY7100MD16R06L2	EVOX RIFA
C42	1µF, ±20% ,3000VAC, Interference SuppressionCapacitorX2 -55°C to +105°C	PHE840EY7100MD16R06L2	EVOX RIFA
C43	2200µF, ±20%, 5V,-55°C to +105°C, Type FC-A, Radial, P-7.5mm	EEUFC1E222S(B)	PANASONIC
C44	470µF, ±20%, 450V, -25°C to +85°C, Type 157 PUM-SI, Snap-In	2222 157 57471	VISHAY BC COMPONENTS
C45	470µF, ±20%, 450V, -25°C to +85°C, Type 157 PUM-SI, Snap-In	2222 157 57471	VISHAY BC COMPONENTS

R - RESISTORS D - DIODES Q - TRANSISTORS C - CAPACITORS U - IC Z/ZD - ZENER DIODES	PT - PULSE TRANSFORMER CT - CURRENT TRANSFORMER L - INDUCTOR MOV - METAL OXIDE VARISTOR P - POTENTIOMETERS F - FUSE	LD - LIGHT EMITTING DIODE CN/J – CONNECTOR T - TRANSFORMERS NTC - NEGATIVE THERMISTOR FB – FERRITE BEAD RLY1 - RELAY

Material List of PFC Circuit Prototype

ITEM NO.	DESCRIPTION	PART NUMBER	VENDOR NAME
SEMICONDUCTORS			
D1	If(av)=1A,V(rrm) =1000V, Standard Rectifier.DO-41	1N4007	ONSEMICONDUCTOR
D2	If(av)=1A, V(rrm)=1000V, Standard Rectifier.DO-41	1N4007	ONSEMICONDUCTOR
D3	If(av)=1A, V(rrm)=1000V, Standard Rectifier.DO-41	1N4007	ONSEMICONDUCTOR
D4	If(av)=1A,V(rrm)=600V,Ultra Fast Diode, DO-41	MUR160	ON SEMICONDUCTOR
D5	If(av)=1A,V(rrm)=40V,Schottky Diode, DO-41	1N5819	ONSEMICONDUCTOR
D6	If(av)=200mA,Vrrm=70V,Dual Switching Diode,SOT-23	BAV70	FAIRCHILD
D7	If(av)=200mA,Vrrm=85V, Switching Diode, SOT-23	BAS 16	FAIRCHILD
D8	If(av)=200mA, Vrrm = 70V, Dual Switching Diode,SOT-23 Package	BAV70	FAIRCHILD
D9	If(av)=1A Vrrm =40V,Schottky Diode,SMA Package	MBRA140T3	ON SEMICONDUCTOR
D10	If(av)=1A,Vrrm=40V,Schottky Diode, SMA Package	MBRA140T3	ON SEMICONDUCTOR
D11	If(av)=1A,Vrrm=40V,Schottky Diode,SMA Package	MBRA140T3	ON SEMICONDUCTOR
D12	If(av)=A,Vrrm=600V ultrafast Diode,SMB Package	MURS160T3	ON SEMCONDUCTOR
D13	If(av)=A,Vrrm=600V ultrafast Diode,SMB Package	MURS160T3	ON SEMCONDUCTOR
D14	If(av) =3A, V(rrm) =1000V, Standard recovery Diode,DO-201AD	1N5408	ON SEMICODUCTOR
D15	If(av) =12A,V(rrm) =600V,Silicon Carbite Diode,TO-220AC	SDT12S60	INFINEON
Q1	Vdss=600,Id=47A,Rds-on=0.07E,N-Channel Mosfet, TO-247AC	SPW47N60C3	INFINEON TECHNOLOGIES
Q2	Vceo=80V, Ic=15A, NPN Power Transistor, TO-22OAB	D44VH	ON SEMICONDUCTORS
Q3	Vceo=80V,Ic=15A, PNP Power Transistor, TO-22OAB	D45VH	ON SEMICONDUCTORS
Q4	Vdss=600V,Id=47A,Rds-on=0.07E,N-Channel Mosfet, TO-247AC	SPW47N60C3	INFINEON TECHNOLOGIES
Z1	18V,0.5W,Zenerdiode, DO-35 package	1N5248B	FAIRCHILD
Z2	9.1V,0.5W,Zenerdiode, DO-35 package	1N5239B	FAIRCHILD
Z3	8.2V,0.5W,Zenerdiode, DO-35 package	1N5237B	FAIRCHILD
Z4	5.1V,225mW,Zenerdiode ,SOT-23 package	BZX84C5V1LT1	ON SEMICONDUCTOR
Z5	5.1V,225mW,Zenerdiode ,SOT-23 package	BZX84C5V1LT1	ON SEMICONDUCTOR
Z6	12V,225mW,Zenerdiode ,SOT-23 package	BZX84C12	VISHAY
BR1	35A, 1200V, Bridge Rectifier, GBPC Package	GBPC3512A	INTERNATIONAL RECTIFIER
U1	Low Power PFC Controller DIP 16 Package	UCC3817N	TEXAS INSTRUMENTS
U2	1.5A, Adjustable Regulator,TO-220 Package	LM317T	NATIONAL SEMICONDUCTOR

R - RESISTORS D - DIODES Q - TRANSISTORS C - CAPACITORS U - IC Z/ZD - ZENER DIODES	PT - PULSE TRANSFORMER CT - CURRENT TRANSFORMER L - INDUCTOR MOV - METAL OXIDE VARISTOR P - POTENTIOMETERS F - FUSE	LD - LIGHT EMITTING DIODE CN/J – CONNECTOR T - TRANSFORMERS NTC - NEGATIVE THERMISTOR FB – FERRITE BEAD RLY1 - RELAY

Material List of PFC Circuit Prototype

ITEM NO.	DESCRIPTION	PART NUMBER	VENDOR NAME
MISCELLEANEOUS			
L1	Ferrite Torroi,R-40,AL= 7000 ± 25%, Grade N30	B64290L0659X830	EPCOS
L2	Powdered Iron Core, AL=116	T131-26	MICROMETALS
L3	Ferrite Torroid,R-36, AL= 5750 ± 25%, Grade N30	B64290L0674X830	EPCOS
L4	Amorphous Alloy Distributed Air Gap Torroidal core, AL= 394.1 ± 25% (2 Nos. stacked)	MP7195MDGC	METGLAS
FB1, FB2 FB3	EMI Suppression Bead 3.5mm Diameter, 3.25mm Length	2673000101	FAIR-RITE
MOV1	Vac=320V, Diameter20, Metal Oxide Varistor	B72210S0321K101	EPCOS
RLY1	20A,12V,DC RELAY	G5V-2	OMRON
NTC1	10E ,5A,±20%, NTC Inrush Current Limiter	B57238S0100M000	EPCOS
F1	11.4 X 9.4 X 24.4mm,Semi Enclosed Fuse Holder	Cat No: 4628	KEYESTONE CORPORATION
J1	Berg pin and Jumber socket	-------	HARWIN
CN1	2 way PCB Header, pin spacing 5.08mm	MSTBVA2.5/2 - G5.08	PHEONIX
CN2	2 way PCB Header, pin spacing 5.08mm	MSTBVA2.5/2 - G5.08	PHEONIX
CN3	2 way PCB Header, pin spacing 5.08mm	MSTBVA2.5/2 - G5.08	PHEONIX
CN4	Flying wires soldered on the PCB points	-	-
CN5	3 way PCB Header, pin spacing 5.08mm	MSTBVA2.5/3 - G5.08	PHEONIX
CN6	2 way PCB Header, pin spacing 5.08mm	MSTBVA2.5/2 - G5.08	PHEONIX
CN7	3 PIN MOLEX Connector	22-04-1.31	MOLEX

R - RESISTORS D - DIODES Q - TRANSISTORS C - CAPACITORS U - IC Z/ZD - ZENER DIODES	PT - PULSE TRANSFORMER CT - CURRENT TRANSFORMER L - INDUCTOR MOV - METAL OXIDE VARISTOR P - POTENTIOMETERS F - FUSE	LD - LIGHT EMITTING DIODE CN/J – CONNECTOR T - TRANSFORMERS NTC - NEGATIVE THERMISTOR FB – FERRITE BEAD RLY1 - RELAY

9.2 Publications

This Research work is based on research results published in various international journals and conferences. The collection of these papers is presented after this chapter.

Paper A:

Supratim Basu, Math H.J.Bollen
and Tore M.Undeland

PFC Strategies in light of EN 61000-3-2

Presented at EPE PEMC 2004 conference at Riga, Latvia
1-3 September 2004.

Paper B:

Supratim Basu and Math H.J.Bollen

A Novel Common Power Factor Correction Scheme for Homes and Offices

Published in IEEE Transactions on Power Delivery, Vol.20, No.3, July 2005.

Paper C:

Supratim Basu and Tore M.Undeland

Design Considerations for Optimizing Performance & Cost of Continuous Mode Boost PFC Converters

Presented at IEEE Nordic Workshop on Power and Industrial Electronics(NORPIE 2004), Trondheim, Norway, 14-16 June 2004.

Paper D:

Supratim Basu and Tore M.Undeland

Diode Recovery Characteristics Considerations for Optimizing Performance & Cost of Continuous Mode Boost PFC Converters.

Published in EPE Journal
Vol. 16. n^{o} 1, February 2006.

Paper E:

Supratim Basu and Tore M.Undeland

Inductor Design Considerations for Optimizing Performance & Cost of Continuous Mode Boost PFC Converters

Presented at 20th Annual IEEE conference, APEC 2005 at Texas, USA, 6-10 March 2005.

Paper F:

Supratim Basu and Tore M.Undeland

Diode Recovery Characteristics Considerations for Optimizing EMI Performance of Continuous Mode Boost PFC Converters

Presented at 11th European Conference on Power Electronics and Applications, EPE 2005, at Dresden, Germany, 11-14 September 2005.

Paper G:

Supratim Basu and Tore M. Undeland

A Novel Design Scheme for Optimizing EMI and Efficiency of Continuous Mode PFC Converters

Presented at 17th IEEE International Symposium on
Electromagnetic Compatibility, Singapore,
February 27-March 3, 2006.

Paper H:

Supratim Basu and Tore M.Undeland

A Novel EMI Reduction Design Scheme for Continuous Mode PFC Converters

Accepted for Publication at – IEEE Nordic Workshop on Power and Industrial Electronics (NORPIE 2006), Lund, Sweden, 12-14 June 2006.

Paper I:

Supratim Basu and Tore M.Undeland

A Novel Design Scheme for Optimizing Efficiency and EMI of Continuous Mode PFC Converters

Submitted to - IEEE Transactions on Electromagnetic Compatibility,
February 2006.