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Thermal Constraints for Heterostructure Barrier Varactors

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***Abstract*—Current research on heterostructure barrier varactors (HBVs) devotes much effort to the generation of very high power levels in the millimeter wave region. One way of increasing the power handling capacity of HBVs is to stack several barriers epitaxially. However, the small device dimensions lead to very high temperatures in the active layers, deteriorating the performance. We have derived analytical expressions and combined those with finite element simulations, and used the results to predict the maximum effective number of barriers for HBVs. The thermal model is also used to compare the peak temperature and power handling capacity of GaAs and InP-based HBVs. It is argued that InP-based devices may be inappropriate for high-power applications due to the poor thermal conductivity of the InGaAs modulation layers.**

***Index Terms*—Frequency multiplier, heterostructure barrier varactor (HBV), semiconductor device thermal factors.**

TABLE I
MATERIAL LAYER STRUCTURE FOR A TYPICAL ONE-BARRIER HBV. FOR AN N-BARRIER DEVICE, THE LAYER SEQUENCE 2–7 IS REPEATED N TIMES

	Layer	Material InP	Material GaAs	Thickness [Å]	Doping [cm^{-3}]
9	Contact	$In_{0.53}Ga_{0.47}As$	$In_{0.53}Ga_{0.47}As$	5000	n^{++}
8	Modulation	$In_{0.53}Ga_{0.47}As$	GaAs	3000	$\sim 10^{17}$
7	Spacer	$In_{0.53}Ga_{0.47}As$	GaAs	50	Undoped
6	Barrier	$In_{0.52}Al_{0.48}As$	$Al_{0.70}Ga_{0.30}As$	50	Undoped
5	Barrier	AlAs	AlAs	30	Undoped
4	Barrier	$In_{0.52}Al_{0.48}As$	$Al_{0.70}Ga_{0.30}As$	50	Undoped
3	Spacer	$In_{0.53}Ga_{0.47}As$	GaAs	50	Undoped
2	Modulation	$In_{0.53}Ga_{0.47}As$	GaAs	3000	$\sim 10^{17}$
1	Contact	$In_{0.53}Ga_{0.47}As$	$In_{0.53}Ga_{0.47}As$	5000	n^{++}
0	Substrate	InP	GaAs		n^{++} or S.I.

I. INTRODUCTION

THE HETEROSTRUCTURE barrier varactor (HBV) was first proposed in 1989 by Kollberg [1], and is a symmetric varactor consisting of a high bandgap semiconductor (barrier), sandwiched between moderately doped semiconductors with a lower bandgap (modulation layers), see Table I. This structural symmetry generates only odd harmonics and allows HBVs to operate unbiased, which simplifies the circuit design of higher order frequency multipliers.

So far, HBV multipliers have demonstrated output powers of a few milliwatts around 200–300 GHz [2], [3]. One of the main goals of current HBV research is to find materials and geometries suitable for high-power devices. A frequently mentioned advantage of HBVs is that several barriers can be stacked epitaxially, to increase the power handling capacity of the devices [4]. Theoretically, the power handling capacity can also be improved by increasing the device area. At millimeter wavelengths, however, this is not a viable solution as the impedance levels must be manageable from a circuit point of view. Even with conversion efficiencies as high as 20%, most of the pump power is dissipated in the diode, causing high peak temperatures in the device. The peak temperature depends on the number of barriers N and the thermal conductivity κ of the material used, the device geometry, heat-sinking, and power level. As the HBV device temperature increases, the device performance is severely deteriorated [5]–[7]. In order to increase the understanding of the thermal constraints pertaining to HBVs, and to elucidate the importance of thermal contact resistances and choice of material system, we present an analytical model for the temperature profile throughout a semiconductor mesa as a function of device area and absorbed power. The model is general and can be applied to a wide range of semiconductor mesa devices, and predicts that for HBVs, there is a practical limit to the maximum number of effective barriers $N_{\max}$ and therefore the power handling capacity is limited.

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II. THERMAL MODEL

A. HBV Thermal Model

The one-dimensional temperature profile in a semiconductor can be solved analytically, based on the assumption that the thermal power is dissipated evenly throughout the mesa, and by assuming a constant κ. The latter assumption is justified by the fact that practical device temperatures under operation are limited to a range from room temperature T_0 to, say, $T_0 + 200$ K. In this temperature range κ decreases with temperature, the decrease is typically less than a factor of two for the III–V semiconductors involved. cf. e.g., [8].

Fig. 1(a) presents the assumed geometry. Since the barrier layers are very thin compared to the modulation layers, Table I, we assume a homogenous κ, equal to that of the modulation layer, throughout the structure. The heat flow equation under stationary conditions, assuming a distributed heat source, is

$$\frac{\partial^2 T(x)}{\partial x^2} = -\frac{P_{\text{tot}}}{LA\kappa} \tag{1}$$

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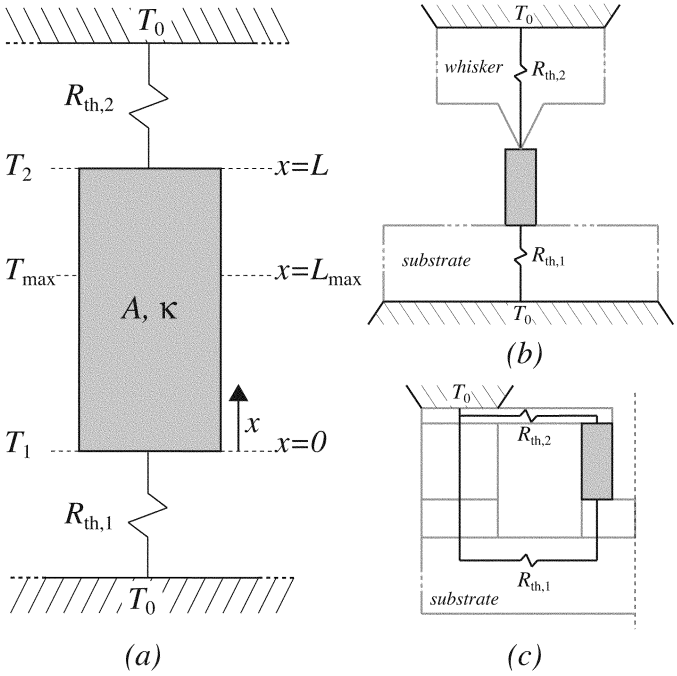

Fig. 1. (a) Schematic view of an HBV mesa of length L, cross-sectional area A and thermal conductivity κ. The mesa is connected to semi-infinite heat-sinks maintained at the temperature T_0 via thermal resistances $R_{\mathrm{th},1}$ and $R_{\mathrm{th},2}$, which determine the boundary temperatures T_1 and T_2. The maximum temperature $T_{\max}$ occurs at $x = L_{\max}$. (b) Thermal resistances for the whisker-contacted geometry. (c) Thermal resistances for the planar geometry.

where $T(x)$ is the temperature at cross section x, and P_{tot} is the total power absorbed in the semiconductor. If the power dissipated in $R_{\mathrm{th},1}$ and $R_{\mathrm{th},2}$ is $P_{\mathrm{diss},1}$ and $P_{\mathrm{diss},2}$, respectively, the boundary conditions to (1) are $T_1 = T(0) = R_{\mathrm{th},1} \times P_{\mathrm{diss},1} + T_0$ and $T_2 = T(L) = R_{\mathrm{th},2} \times P_{\mathrm{diss},2} + T_0$. Now (1) can be solved, observing that $P_{\mathrm{diss},1}/P_{\mathrm{tot}} = L_{\max}/L$ and $P_{\mathrm{diss},2}/P_{\mathrm{tot}} = (L - L_{\max})/L$. The resulting temperature profile is

$$T(x) = T_0 + \frac{P_{\mathrm{tot}}}{2L} \cdot \left[\frac{2A\kappa R_{\mathrm{th},1} R_{\mathrm{th},2} L + R_{\mathrm{th},1} L^2}{L + A\kappa \cdot (R_{\mathrm{th},1} + R_{\mathrm{th},2})} + \left(2R_{\mathrm{th},2} + \frac{L}{A\kappa} - \frac{(2A\kappa R_{\mathrm{th},2} + L)(R_{\mathrm{th},1} + R_{\mathrm{th},2})}{L + A\kappa \cdot (R_{\mathrm{th},1} + R_{\mathrm{th},2})} \right) \cdot x - \left(\frac{1}{A\kappa} \right) \cdot x^2 \right]. \quad (2)$$

By using $\partial T(x)/\partial x = 0$ for $x = L_{\max}$, we can calculate $L_{\max}$. We thus obtain the peak temperature $T_{\max}$ as

$$T_{\max} = T_0 + \frac{P_{\mathrm{tot}}}{2L} \cdot \left[(2A\kappa R_{\mathrm{th},1} + L)(2A\kappa R_{\mathrm{th},2} + L) \cdot \frac{(2A\kappa(R_{\mathrm{th},1} + R_{\mathrm{th},2}) + L)L}{4A\kappa(L + A\kappa(R_{\mathrm{th},1} + R_{\mathrm{th},2}))^2} \right]. \quad (3)$$

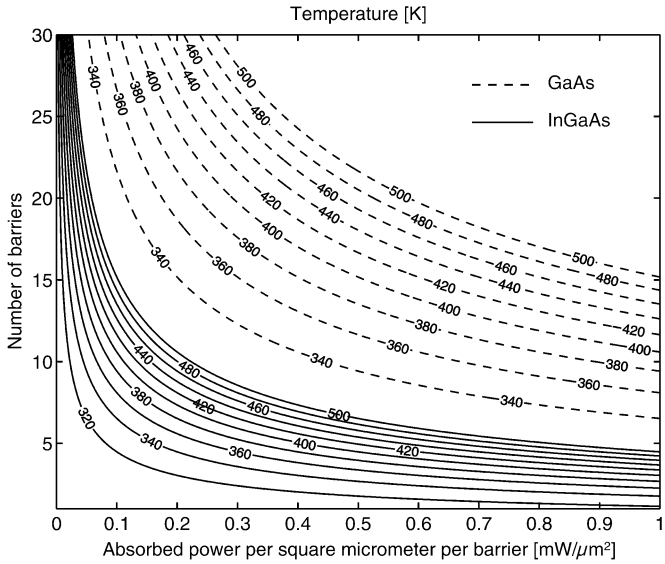

Fig. 2. Temperature at the center of symmetrically contacted HBV mesas with GaAs and InGaAs modulation layers, respectively, obtained from (4). The contacts are assumed to be perfect heat conductors and maintained at $T_0 = 300$ K. $L = l(N+1)$ and $l = 300$ nm.

B. Ideal Case: Perfect Heat-Sinks

If $R_{\mathrm{th},1} = R_{\mathrm{th},2} = 0$, (3) reduces to

$$T_{\max} = T_0 + \frac{P_{\mathrm{tot}} L}{8A\kappa}. \quad (4)$$

Given $T_{\max}$, we can obtain a rough estimate of the theoretical $N_{\max}$. The power density per unit area per barrier is $P_d = P_{\mathrm{tot}}/(A \times N)$. Approximately, $L \approx l(N+1)$, where l is the thickness of the modulation layers, and $N(N+1) \approx N^2$. Then, (4) yields

$$N_{\max} \approx \sqrt{\frac{(T_{\max} - T_0) 8\kappa}{P_d l}}. \quad (5)$$

C. Thermal Resistance of Practical HBVs

In order to illustrate (2), we estimate the thermal resistances for whisker-contacted [1], [9] and planar [10] HBVs. For whisker-contacted diodes [Fig. 1(b)] $R_{\mathrm{th},1}$ can be estimated as described in [11], whilst $R_{\mathrm{th},2}$ is very large and therefore taken as infinite. For planar devices, we assume the diode geometry presented in [6] (for a scanning electron microscope picture see [12]) and use the commercial software FEMLAB to estimate the thermal resistances [Fig. 1(c)].

III. Results

We have used room-temperature values for κ: 400 W/m·K for Cu, 317 W/m·K for Au, 70 W/m·K for InP, 46 W/m·K for GaAs, and 4.6 W/m·K for InGaAs. The values for the semiconductors are for undoped materials, and can be expected to be somewhat higher for doped layers.

A. Ideal Case

Equation (4) is visualized in Fig. 2. In order to estimate $N_{\max}$, we must assume the allowable $T_{\max}$. For GaAs-based HBVs,

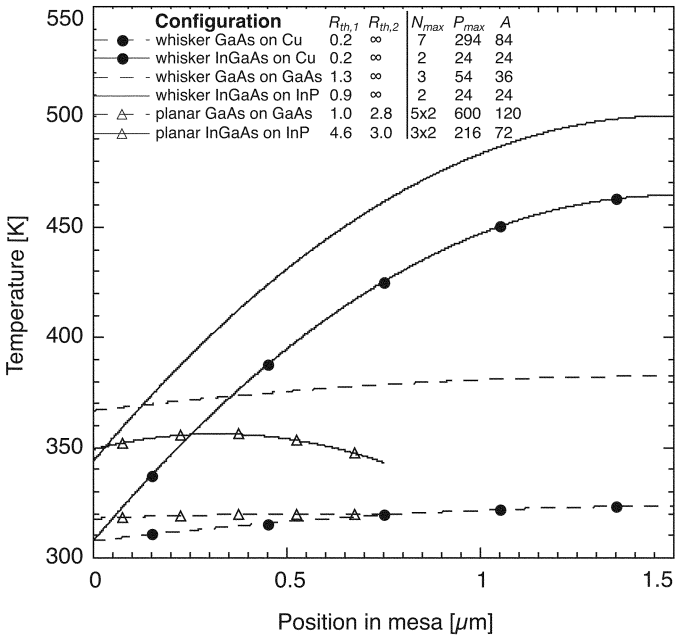

Fig. 3. Temperature profile throughout a four-barrier HBV mesa for various material combinations and geometries, obtained from (2) with $T_0 = 300$ K, $P_{\rm tot} = 50$ mW, $L \approx l(N+1) = 1.5\,\mu$m, and $A = 52\,\mu$m^2. The thermal resistances are given in Kelvin per milliwatt. The planar devices have two two-barrier mesas in series, the length of one mesa is thus half that of the whisker-contacted devices. Calculated values for $N_{\rm max}$ and $P_{\rm max}$, the latter in milliwatts, are also presented, along with the corresponding area in square micrometers.

this temperature, chosen so that the HBV operates in the desired varactor mode, can be extracted from experimental results [5]. For InP-based devices, reliability studies give an indication of the appropriate $T_{\rm max}$; see, e.g., [13] and [14]. This approach suggests $T_{\rm max} = 420$ K for both material systems. For pump frequencies at W-band (75–110 GHz), we typically find $P_d = 0.5$ mW/μm^2, see, e.g., [3]. Using this value, the limiting number of barriers is approximately 17 for GaAs HBVs, and 5 for InP HBVs; see Fig. 2. The power handling capacity is proportional to N^2 and, thus, to κ. So as to compare equal-impedance devices, we assume an InP HBV with an area of 60 μm^2 and a GaAs HBV with an area of $(17/5) \times 60$ μm^2. For frequency multiplication from the W-band, the maximum manageable power level is thus approximately 1.7 W and 150 mW for GaAs and InP-based devices, respectively.

B. Practical Devices

Fig. 3 illustrates temperature profiles from (2). For the planar devices and the whisker-contacted GaAs-based devices, the temperature gradient is small, and a constant average temperature can be assumed in the mesa. With $R_{\rm th,1},\ R_{\rm th,2} \neq 0$, $N_{\rm max}$ decreases drastically and can be derived from (3). The results are displayed in Fig. 3, where the calculated values of $N_{\rm max}$ have been rounded off to the nearest integer, and the area has been normalized as in the previous section, i.e., $A = (60/5) \times N$. To justify the thermal model, we have compared results from (3) with FEMLAB simulations of the maximum temperature in the middle of the active region and found the deviation to be well below 10% for both material systems under investigation.

IV. Conclusion

The poor thermal conductivity of the InGaAs modulation layer causes very high temperatures in InP-based HBVs. Provided that the electron barrier can be made as high as in InP-based HBVs, so as to ensure varactor mode operation, GaAs would therefore be the preferred material for high power applications, due to the ten times higher power handling capacity. InP HBVs are, however, superior to the GaAs counterparts in terms of high conversion efficiencies for moderate power levels.

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